Nanosystems:

Technology,

Architectures and Applications

Giovanni De Micheli

Outline

- **Introduction**
- Technology
  - Devices
  - Circuits
- Architecture
  - Communication infrastructure
  - 3D Integration
- Sensors
- Applications
- Conclusions

Nano-systems

Nano

- Nano-electronics:
  - CMOS < 32nm node
  - Silicon nanowires
  - Carbon nanotubes
  - Flatronics
- Nano-bio-sensing:
  - Size compatibility
  - Electro-chemistry

Systems

- Tera-scale systems:
  - Heterogeneity
  - Sensing, Processing, Communication, SW Transducers
- Complexity:
  - Design
  - Management

Outline

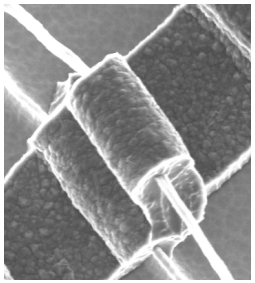
- Introduction
- **Technology**
  - Devices
  - Circuits
- Architecture
  - Communication infrastructure
  - 3D Integration
- Sensors
- Applications
- Conclusions

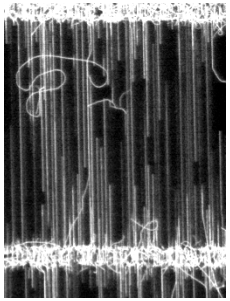
The emerging nano-technologies

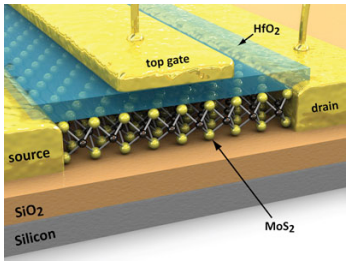
- System technology is build bottom-up, starting from materials and their properties
- New devices exploit functional geometries at the molecular level
  - Quantum confinement
- There is a plethora of new materials and processing steps/flows
  - More than 50 elements in a regular CMOS process
- *Enhanced* silicon CMOS is likely to remain the main manufacturing proces

Beyond CMOS

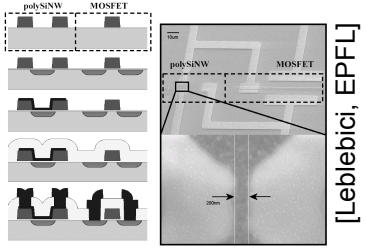
- Nano-technology provides us with new devices



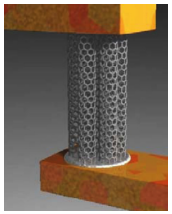




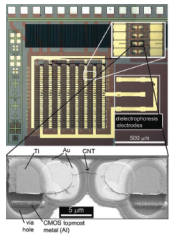
- Can they mix and match with standard CMOS technology ?



[Leblebici, EPFL]



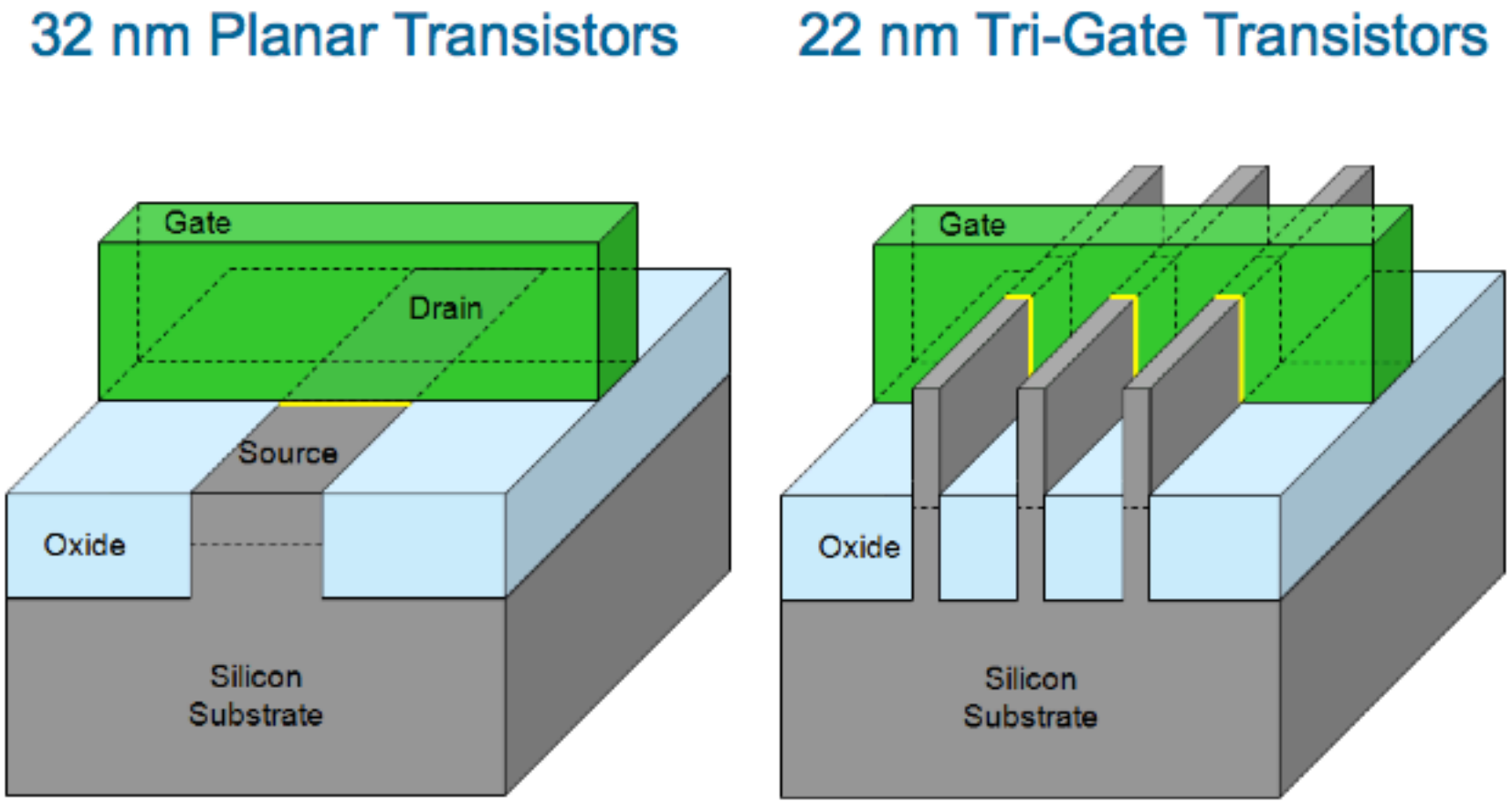
[Infineon]



[Close, Stanford]

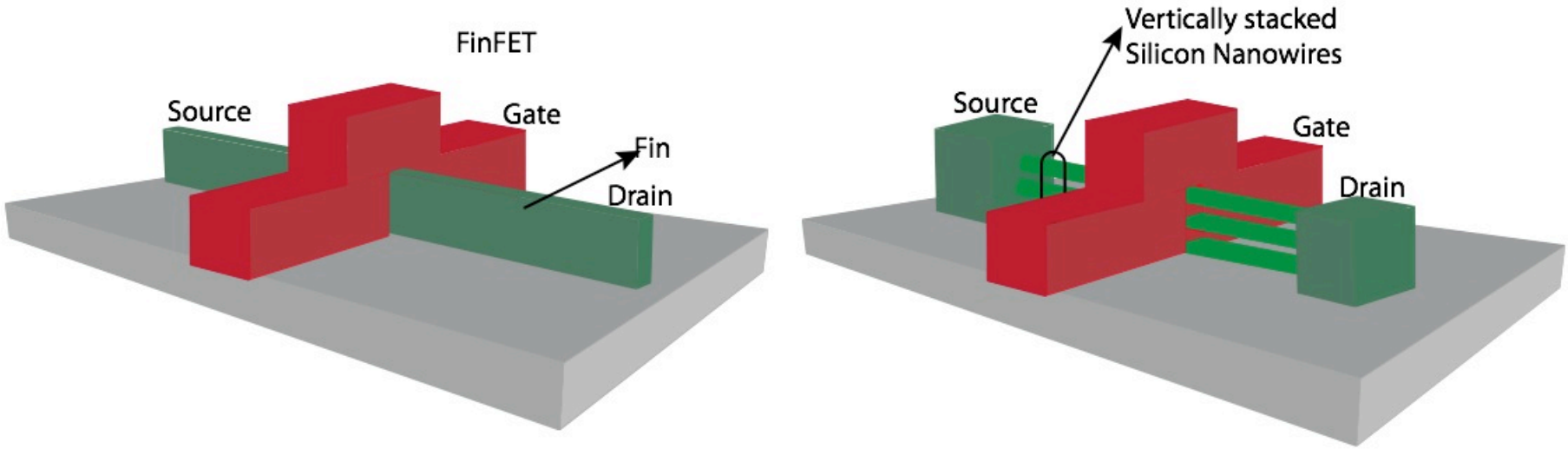
- What is the added value?

22 nm Tri-Gate Transistors



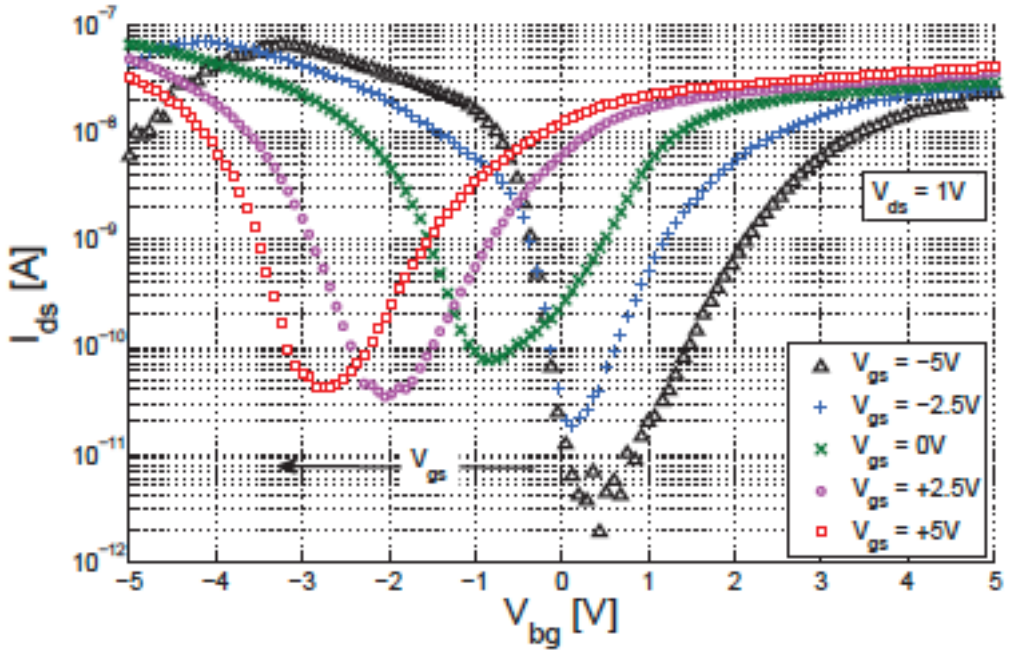
[Courtesy: M. Bohr]

FinFETs versus SiNW FETs



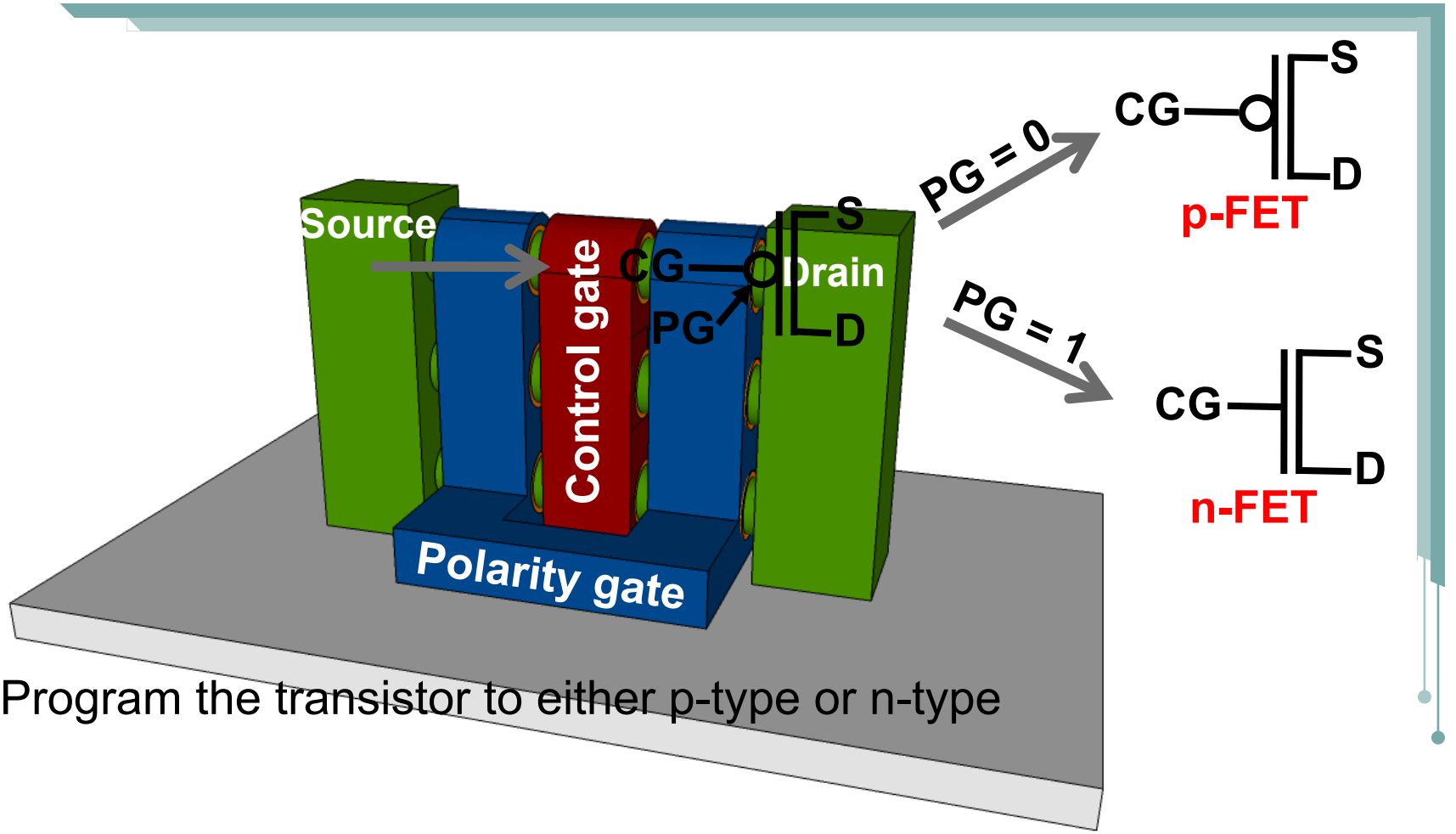
Ambipolarity

- Device characteristics controlled by backgate voltage
  - Four-terminal devices
  - Back gate determines type: *n* or *p*



[Courtesy: Sacchetto, EPFL]

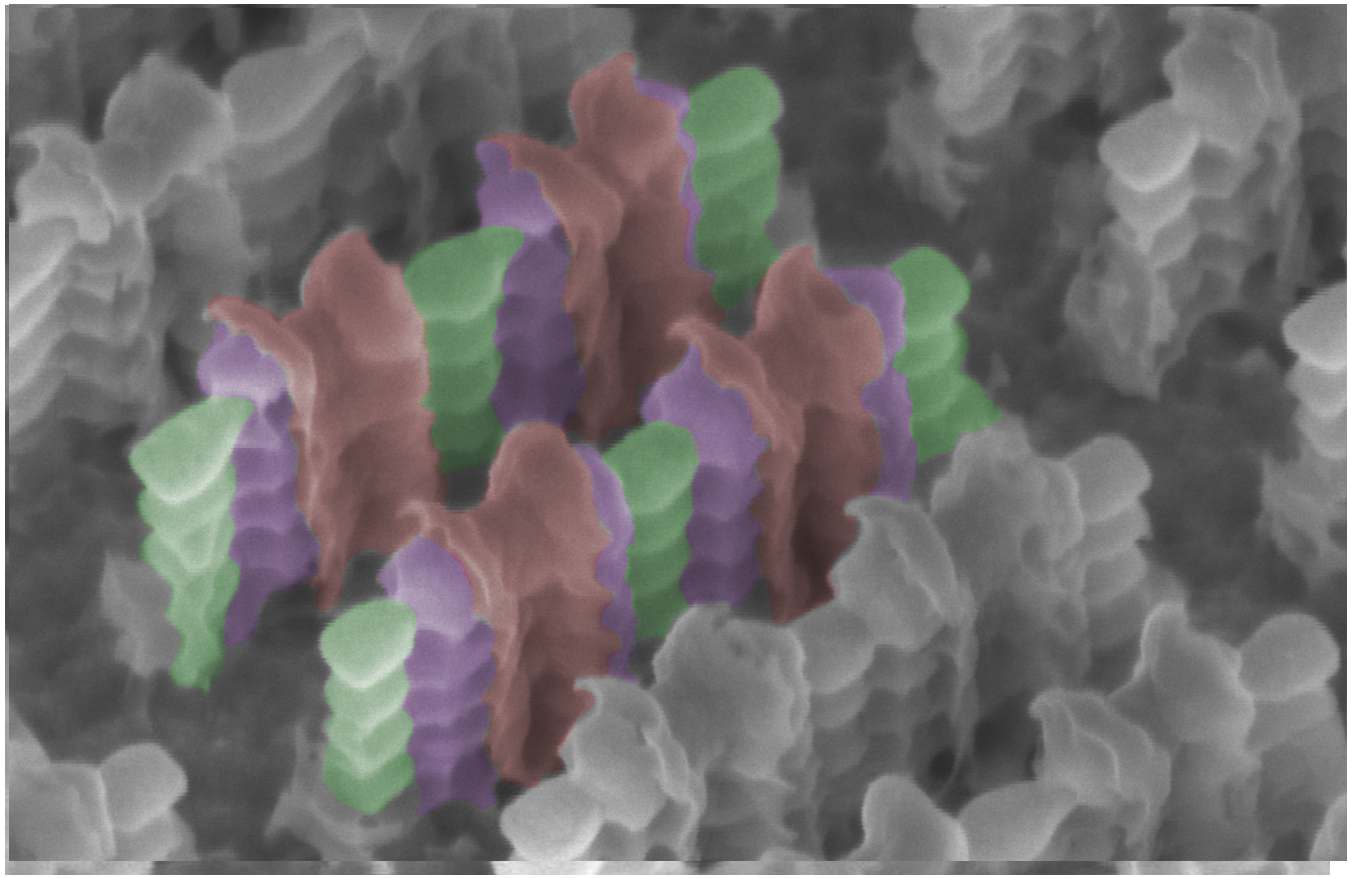
Double Independent gate SiNW FET



- Program the transistor to either p-type or n-type

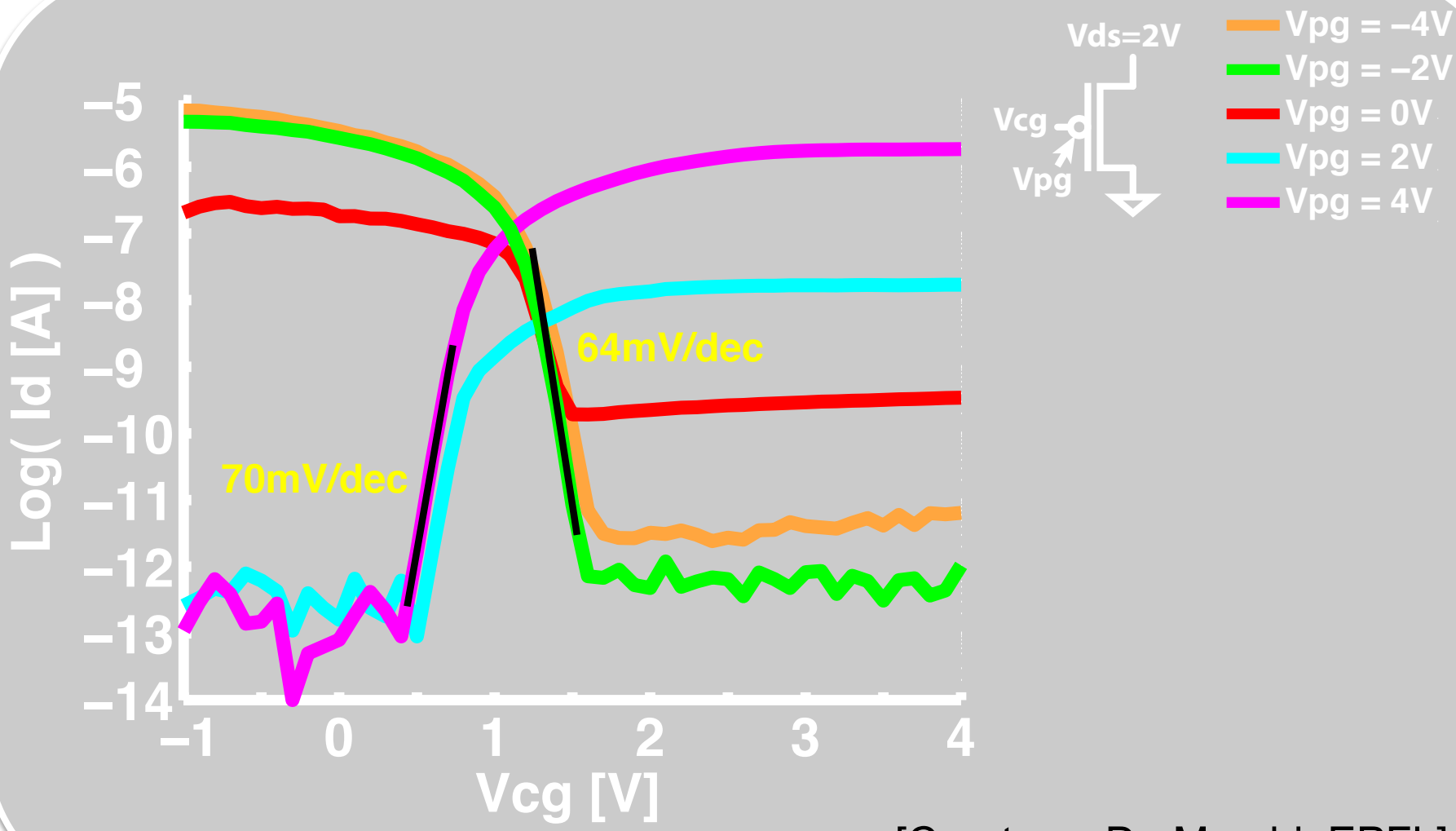
Silicon Nanowire Transistors

- Gate all around transistors
- Double gate to control polarity



[Courtesy: De Marchi, EPFL]

Device I_d/V_{cg}

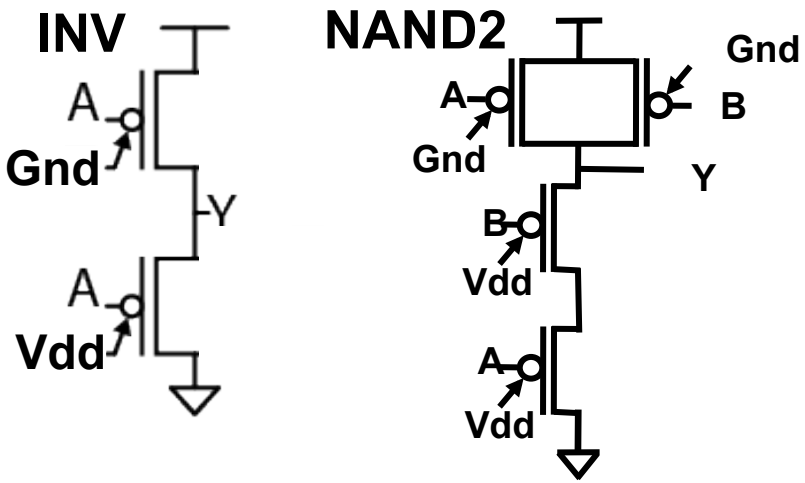


[Courtesy: De Marchi, EPFL]

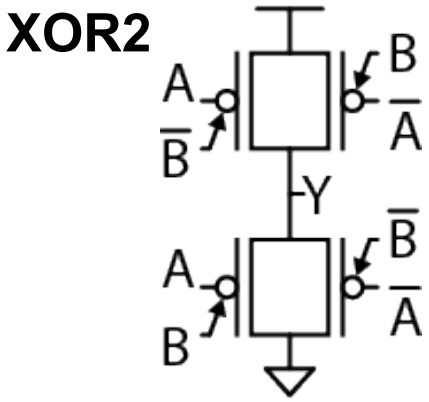
New Design Paradigm: Ambipolar Logic

- CMOS complementary logic efficient only for negative-unate functions (INV, NAND, NOR…etc)
- Ambipolar logic is efficient for both unate and binate functions
- Optimal for XOR and XNOR dominated circuits

Negative Unate functions	Binate functions



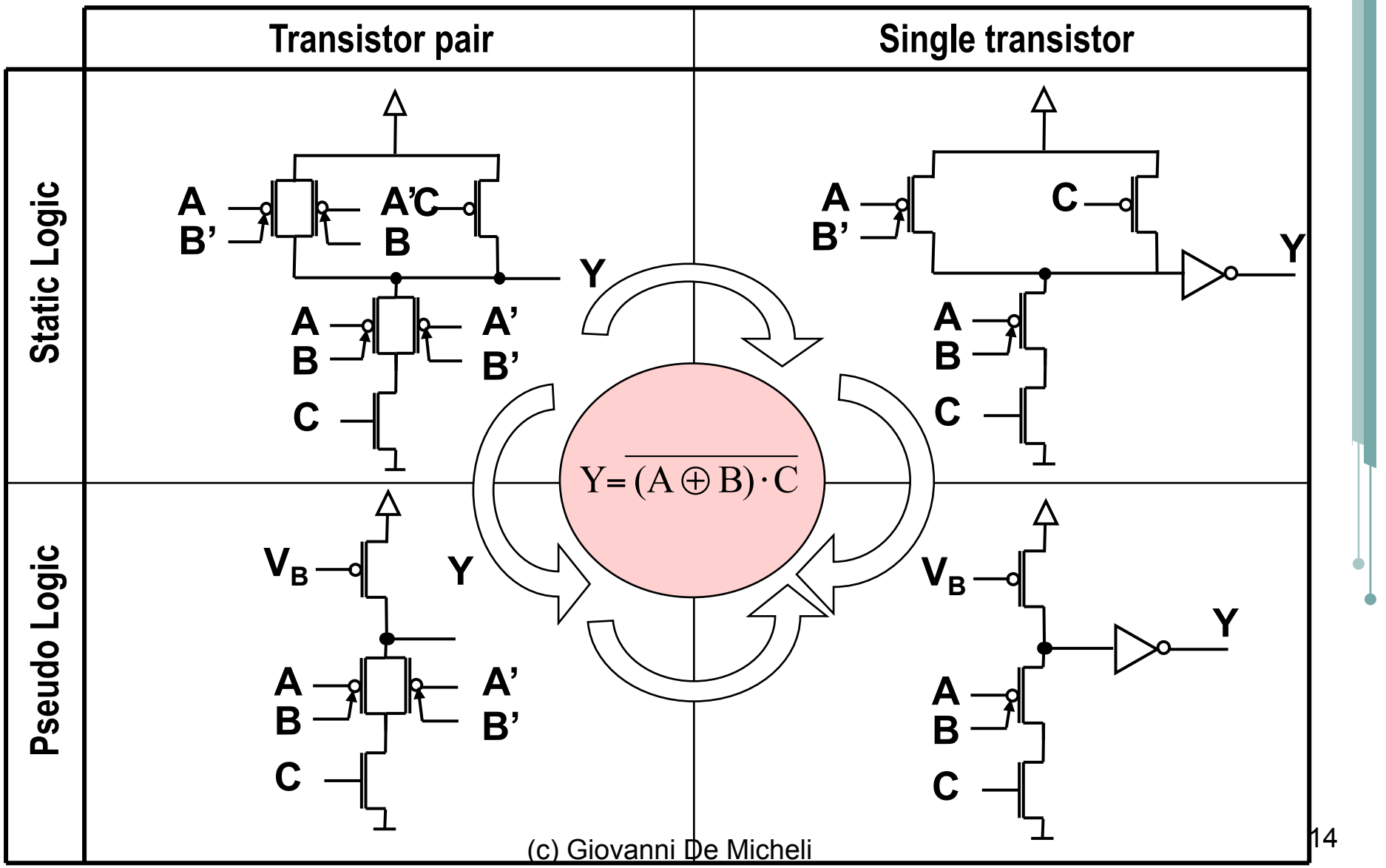
Similar to regular CMOS



Only 4 transistors when compared to 8 transistors with a regular CMOS

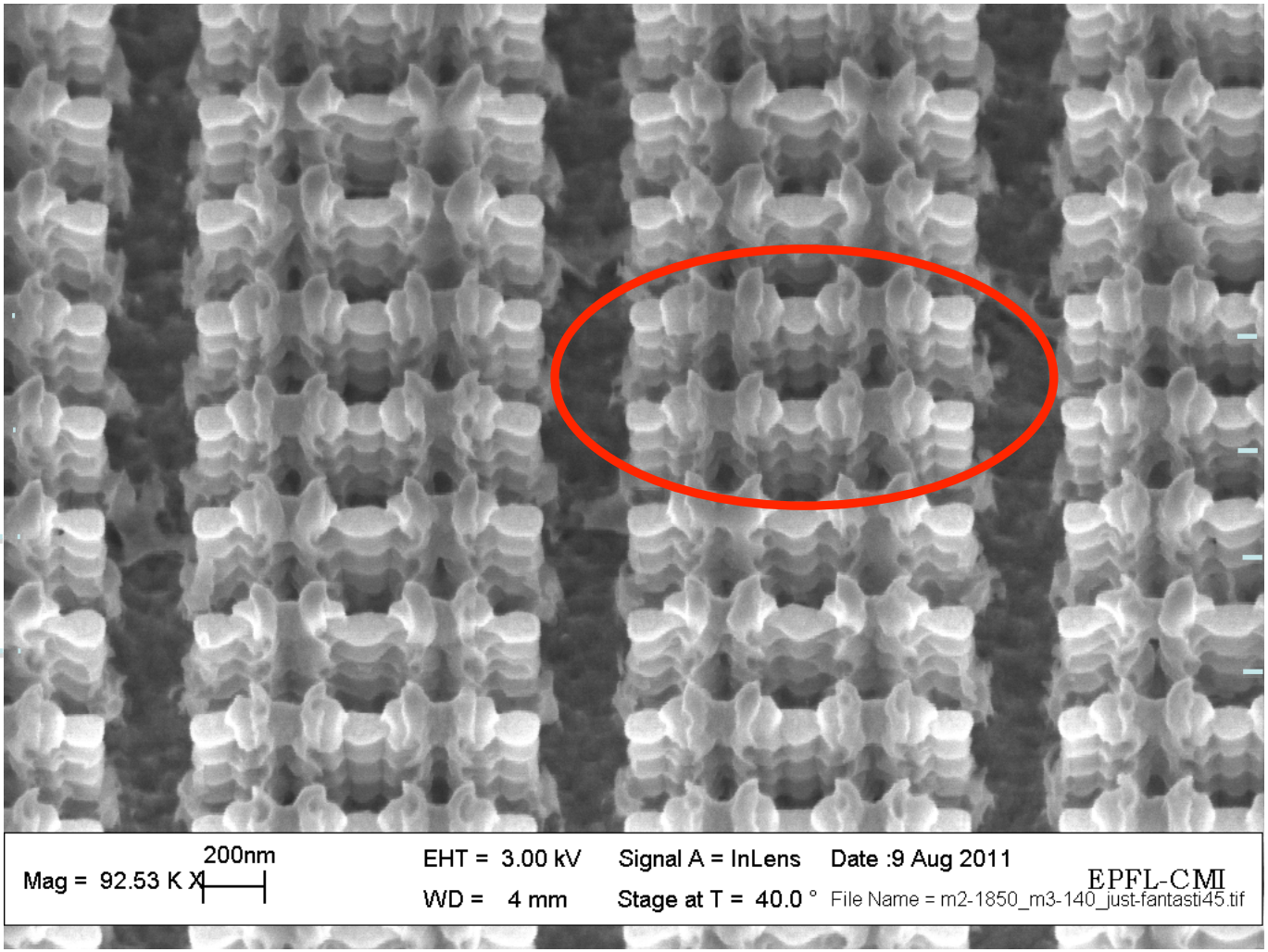
[Courtesy: H. Ben Jamaa, '08]

Alternative logic families



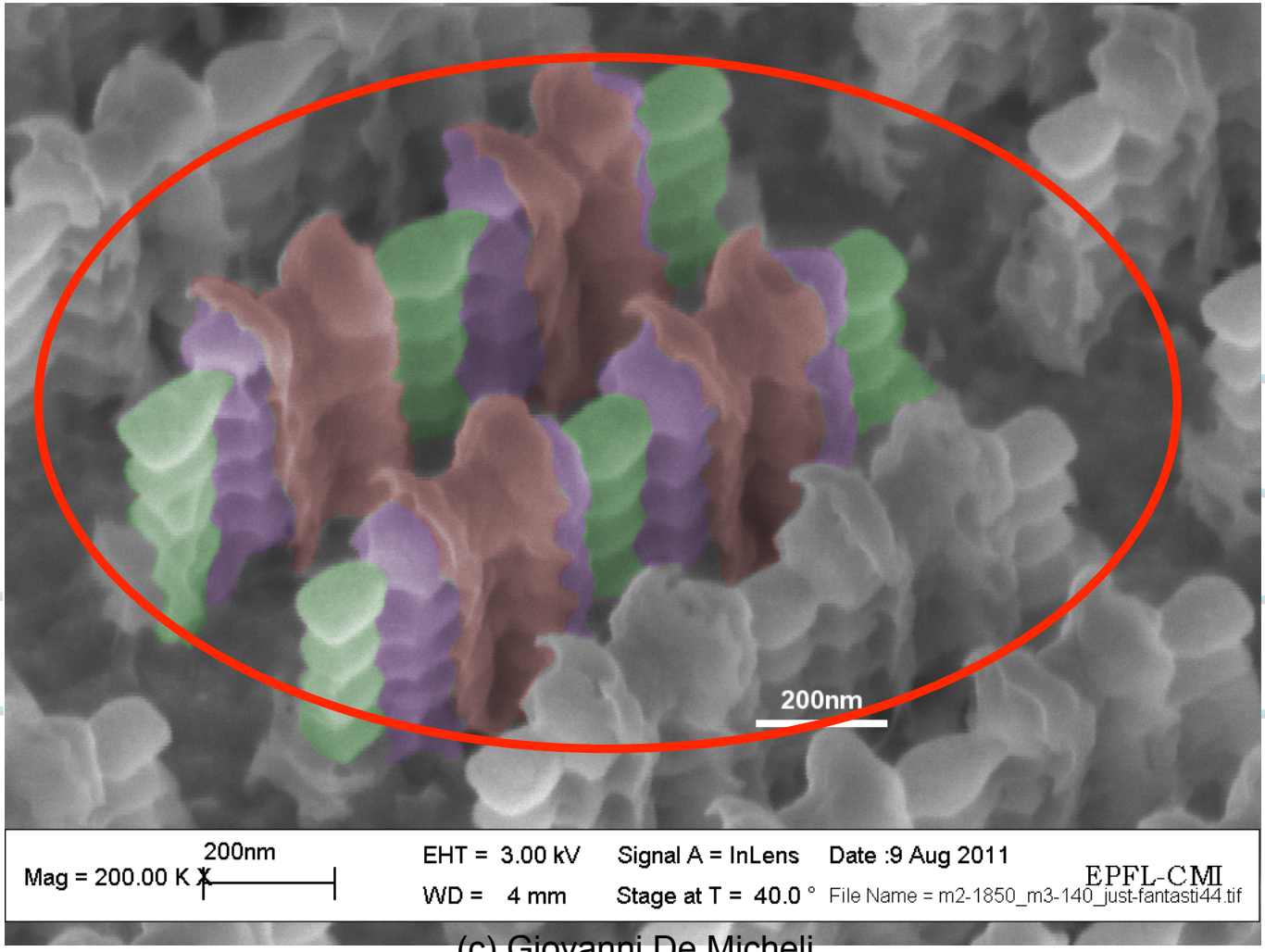
Sea-of-Tiles (SoT)

- Homogeneous array of Tiles

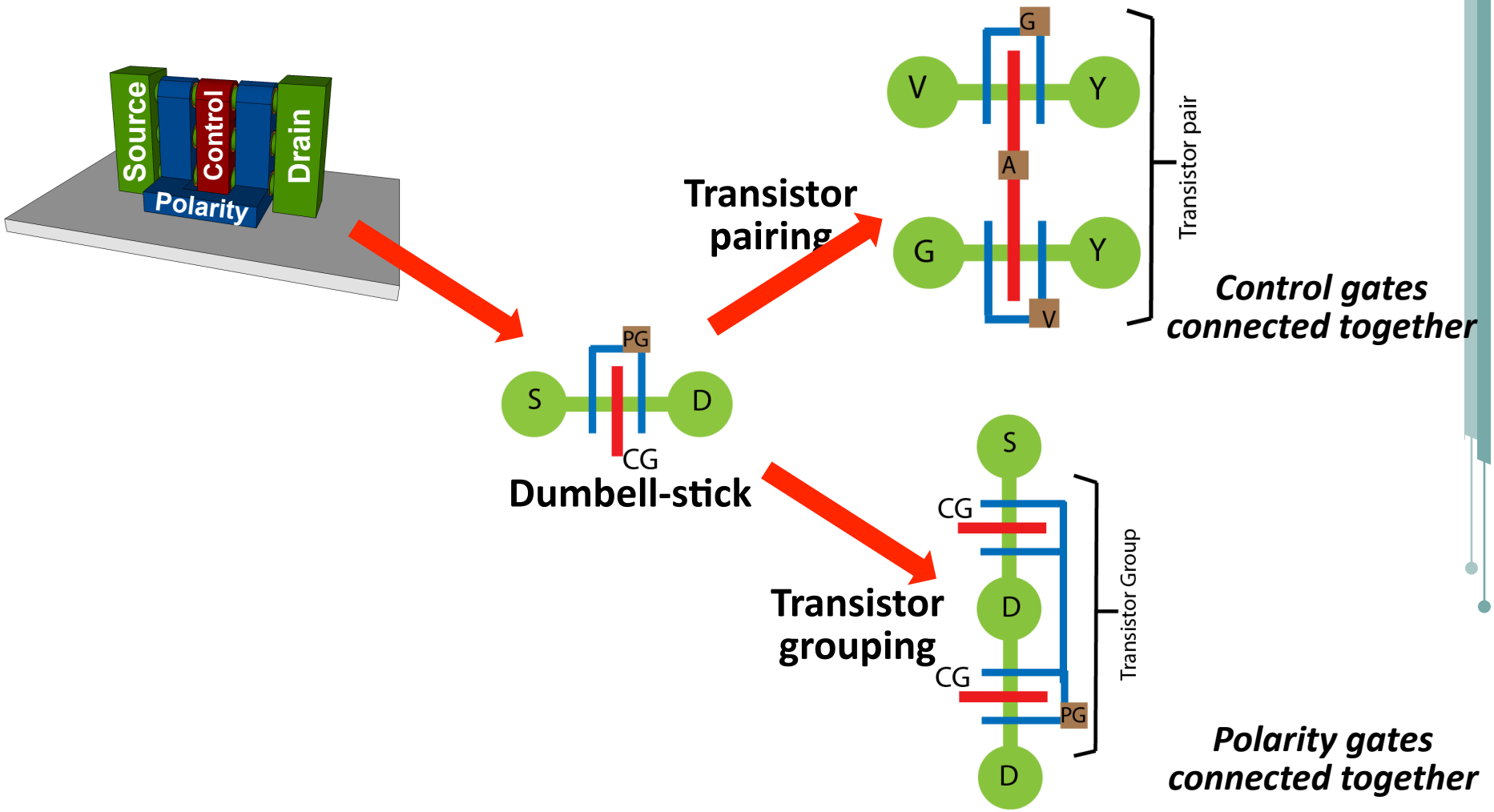


Sea-of-Tiles (SoT)

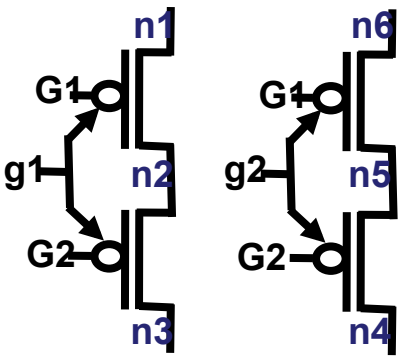
- Homogeneous array of Tiles

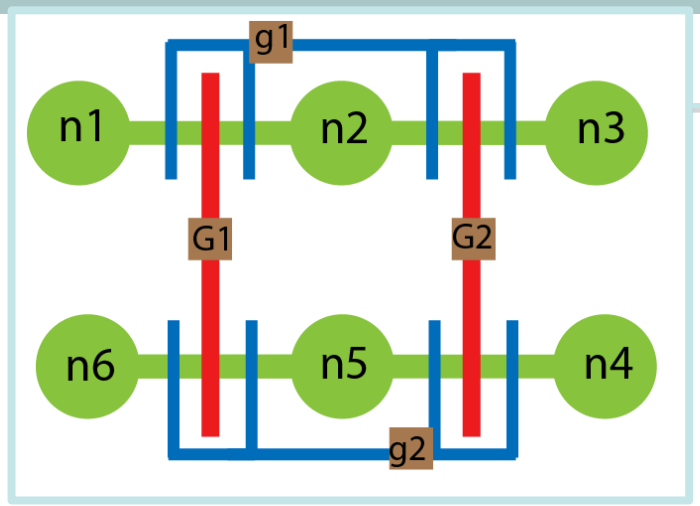


Dumbbell-stick diagrams



Layout abstraction and regularity with *Tiles*

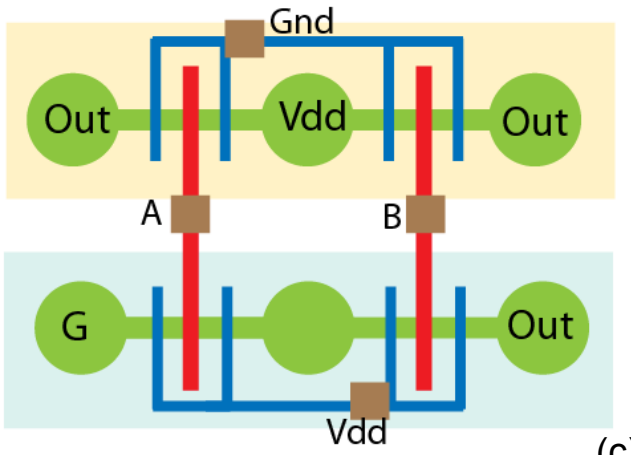




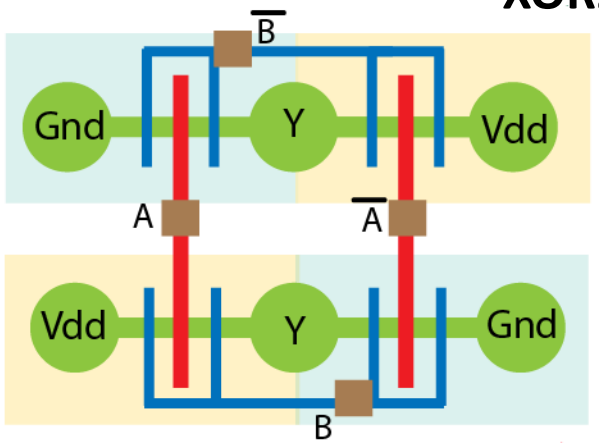
Tile

Two transistor pairs grouped together

NAND2



XOR2

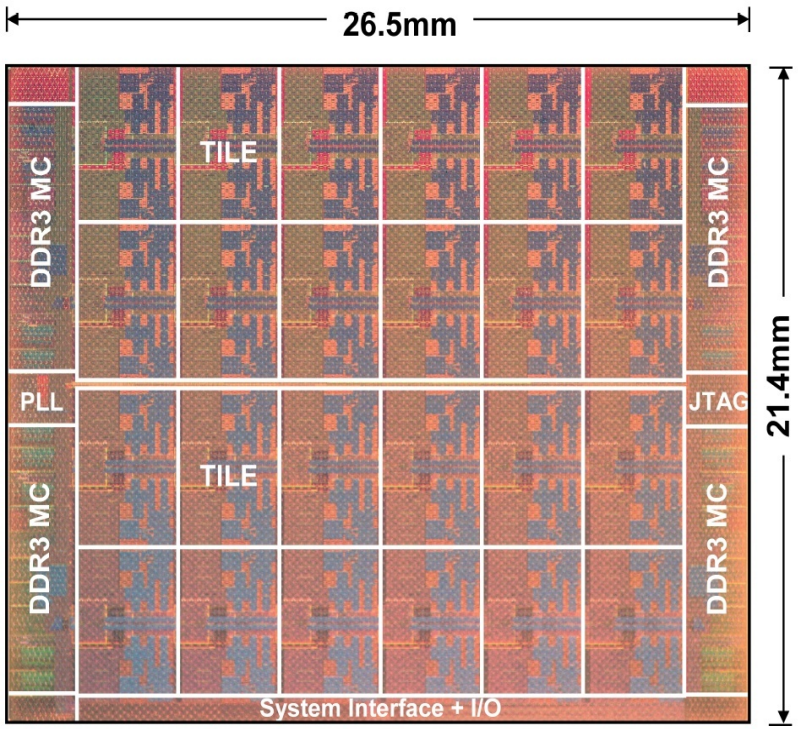


[Courtesy: Bobba, DAC 12]

Outline

- Introduction
- Technology
  - Devices
  - Circuits
- **Architecture**
  - Communication infrastructure
  - 3D Integration
- Sensors
- Applications
- Conclusions

System architectural trends

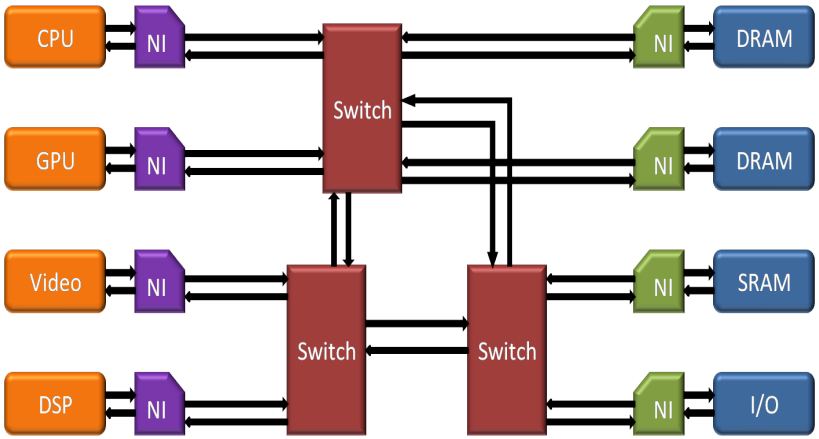


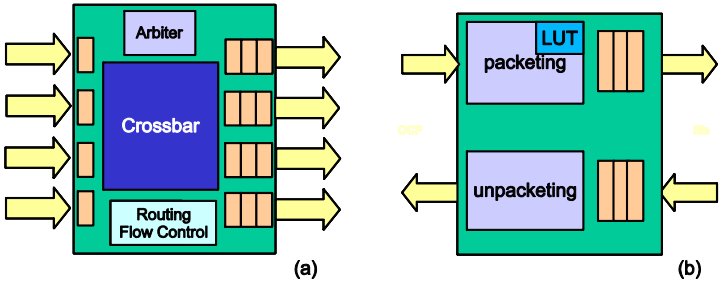
Intel Single-Chip Cloud Computer

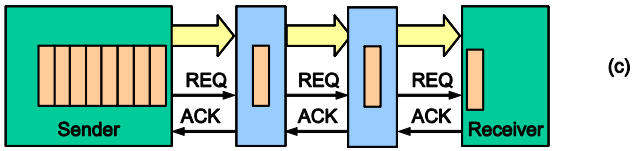
[Courtesy: Howard, ISSCC 2010]

- Many-core processing
  - Frequency scaling has leveled-off
  - Exploit application-level parallelism
- On-chip communication
  - Bottleneck for system performance
- Networks-on-Chip (NoC)
  - Adopted as scalable interconnect

Networks-on-Chip Scalable Interconnect





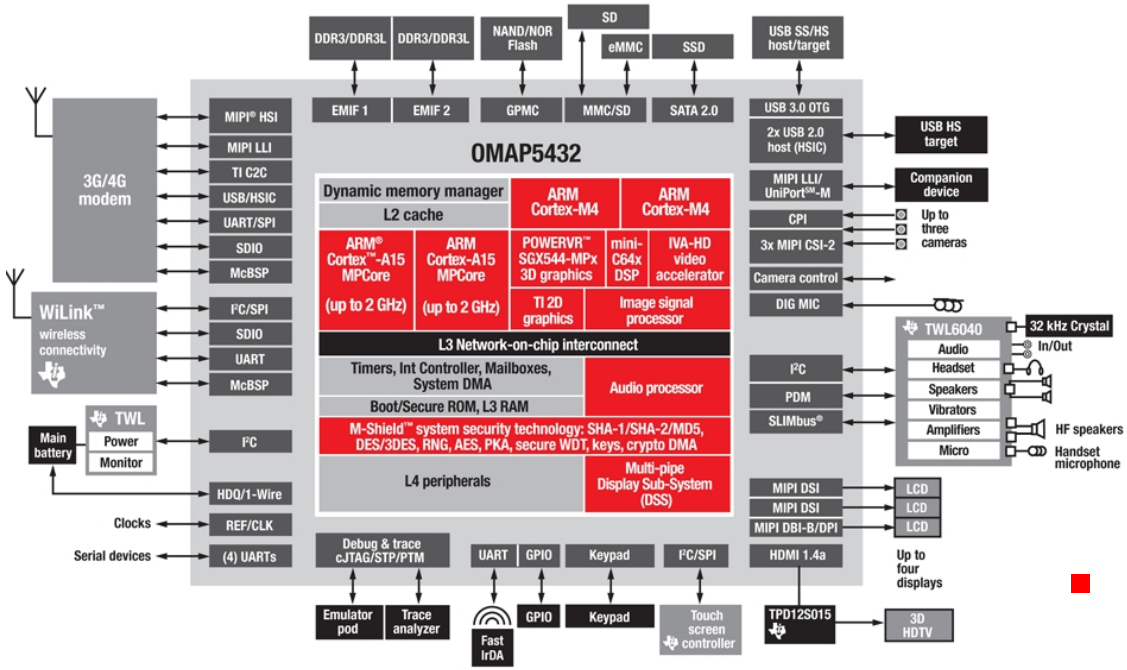


xpipes library

[Courtesy: Stergiou DATE 2005]

- NoC modular architecture
  - Network Interfaces (NIs)
  - Switches
  - Links
- Scalable
  - Multiple parallel transactions
  - Segmented point-to-point wires
- Used in prototypes and products
  - Bone, Intel Polaris, SCC
  - TI OMAP, Tilera TILE-Gx

Specialization for Power Efficiency

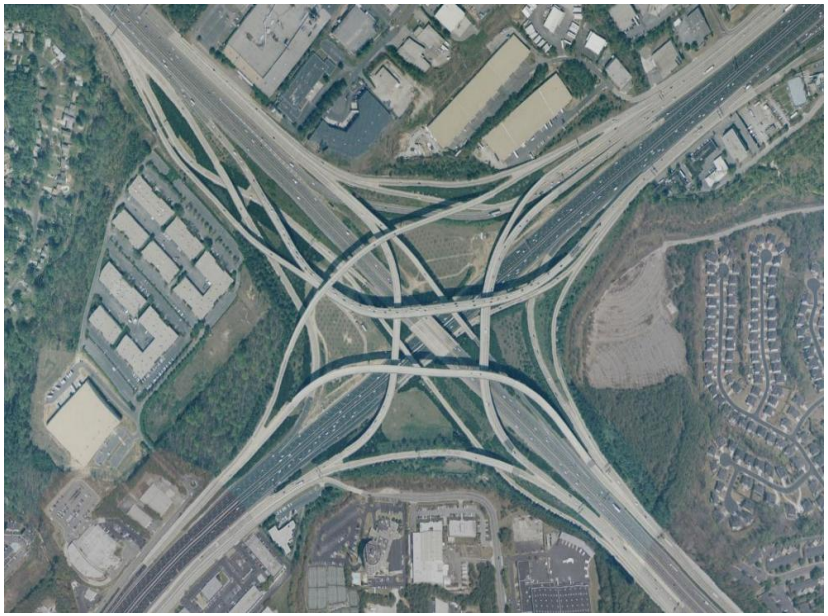


TI OMAP 5 application platform

- Limited power budget for mobile applications
  - Trade-off programmability for power-efficiency
  - Specialized heterogeneous IP-cores
- Communication is a major power consumer
  - Traffic patterns are known
  - Application specific NoC design is needed

Application specific NoCs

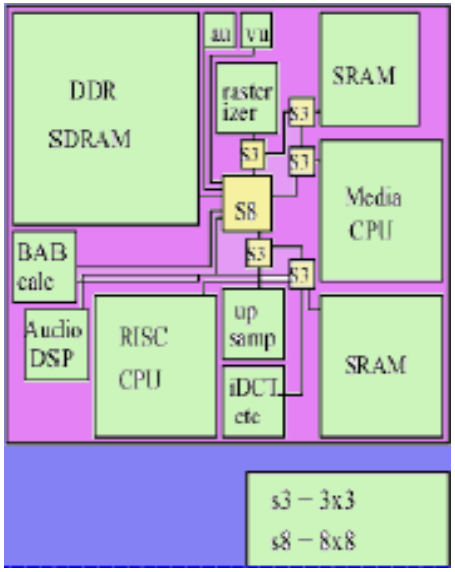
?

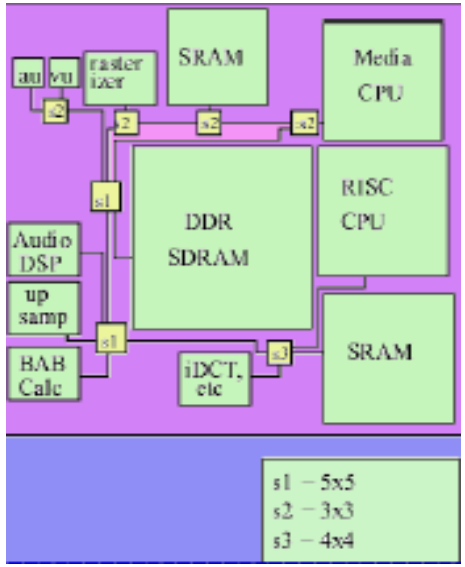


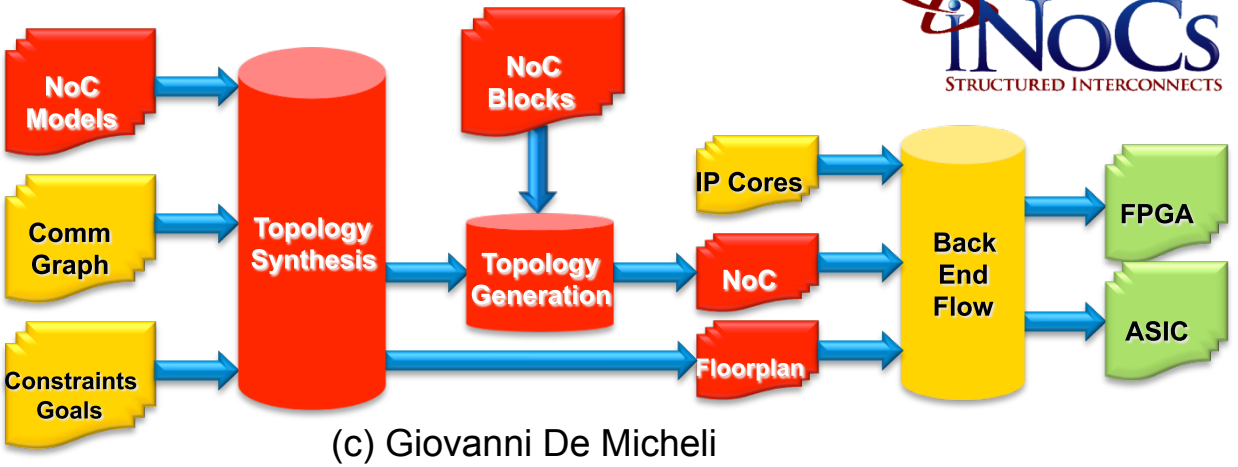
- Challenges
  - Many parameters (i.e., data-size, frequency, connectivity)
  - Tools are required to find the best topology
- New technologies
  - More IP-cores
  - More constraints (i.e., 3D-IC vertical connectivity)

Design automation for NoCs

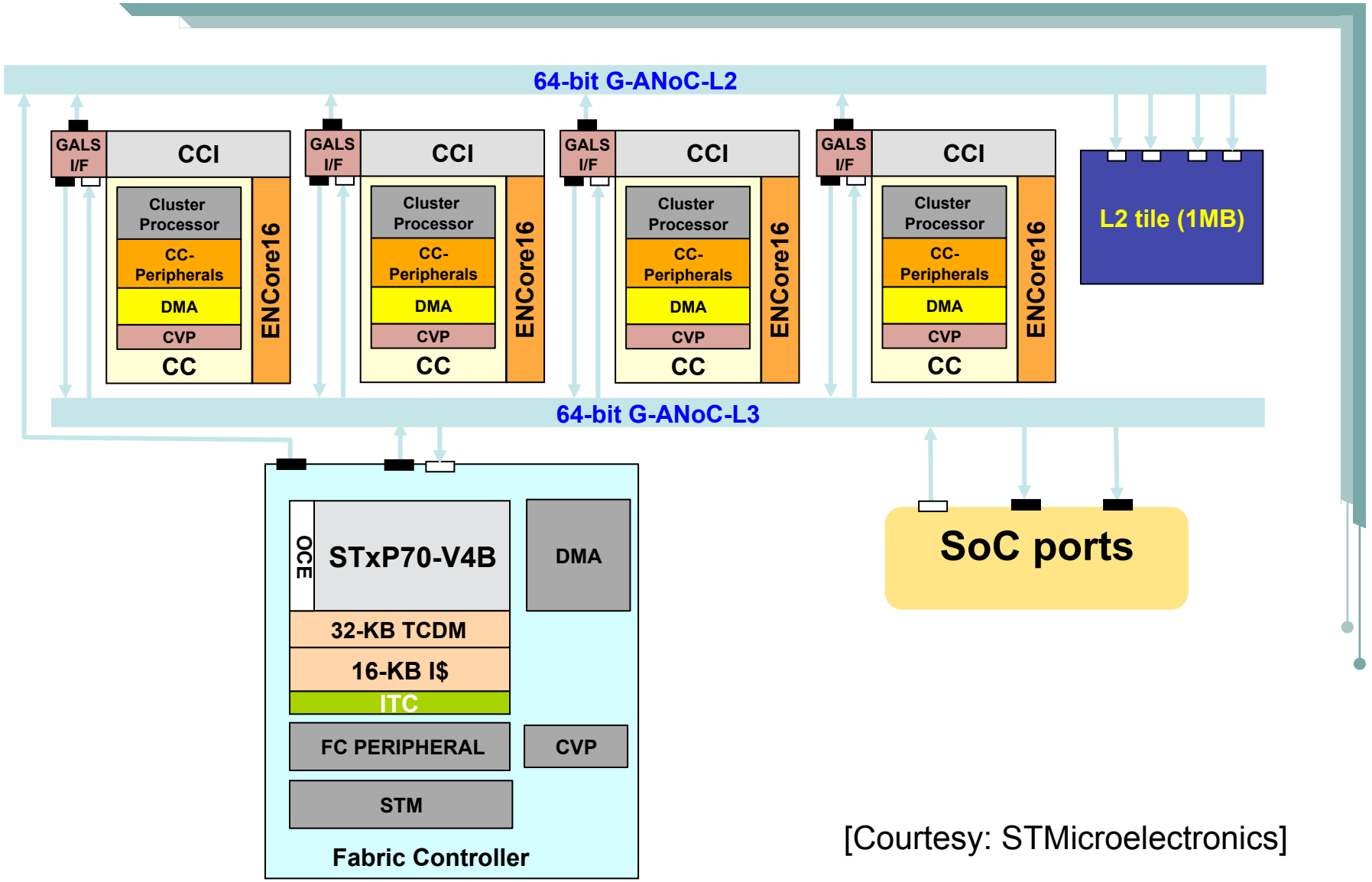
- Large design space
  - What topology ?
  - Which mapping ?
  - Which routes to use ?
- Optimize parameters
  - Link width, buffer sizes
- Simulate, verify, test







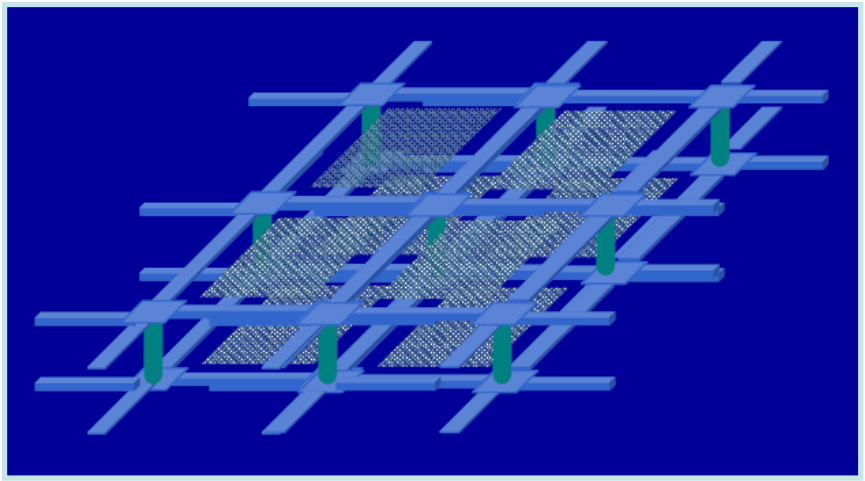
STHORM ANoC



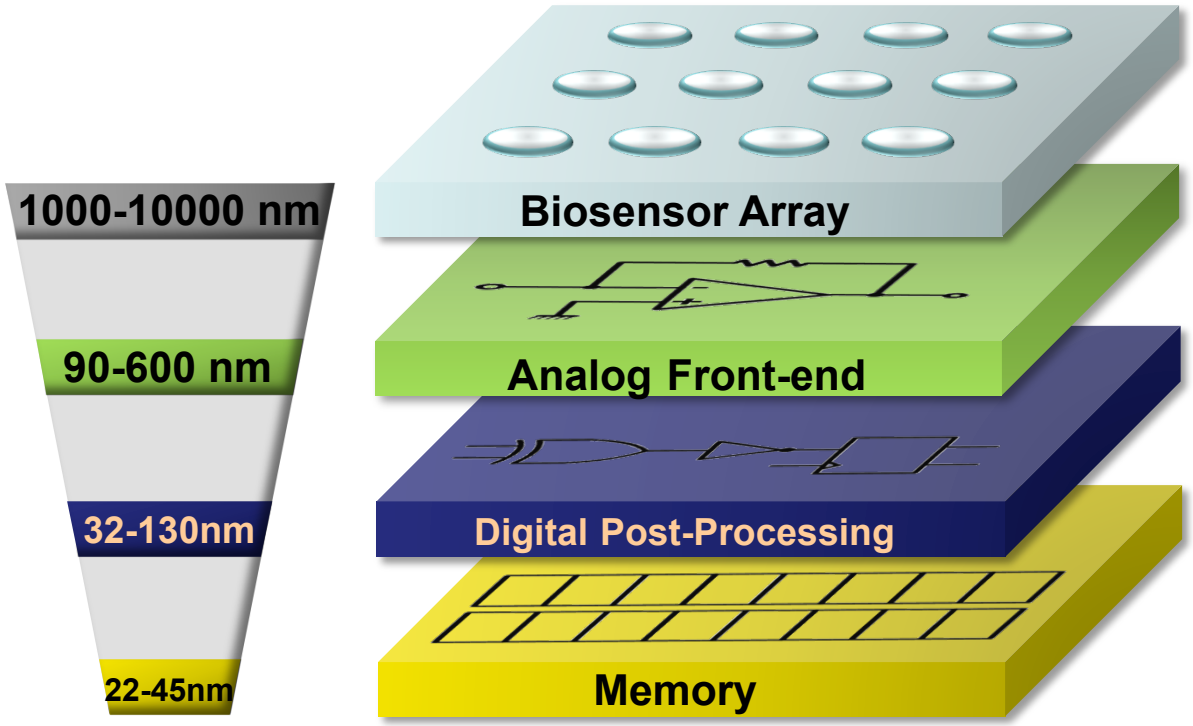
[Courtesy: STMicroelectronics]

3D NoC Design

- Use NoCs to support Wide I/O
- Challenges:
  - Meet application constraints in a 3D structure
    - Bandwidth, latency
    - Which topology, switches, layers and floorplan locations?
  - Meet 3D technology constraints
    - Maximum available TSV constraints
    - Communication between adjacent layers



Extending 3D Integration to sensing



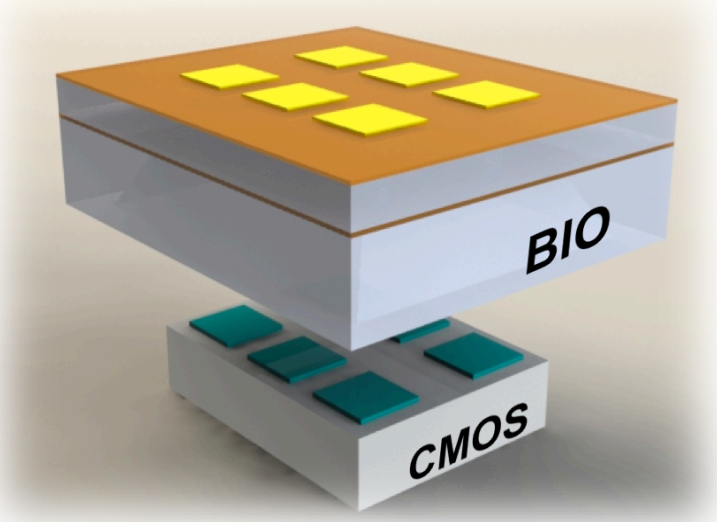
Custom micro-fabrication for the bio-layer

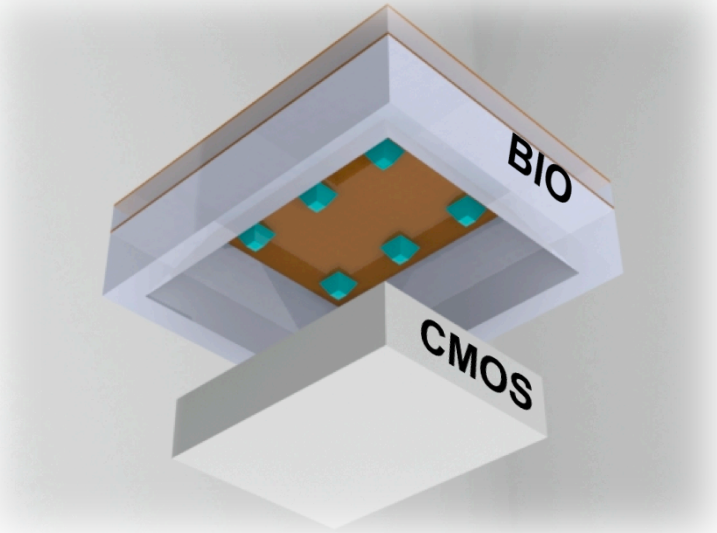
Technologies enabling low noise operation for the analog circuits

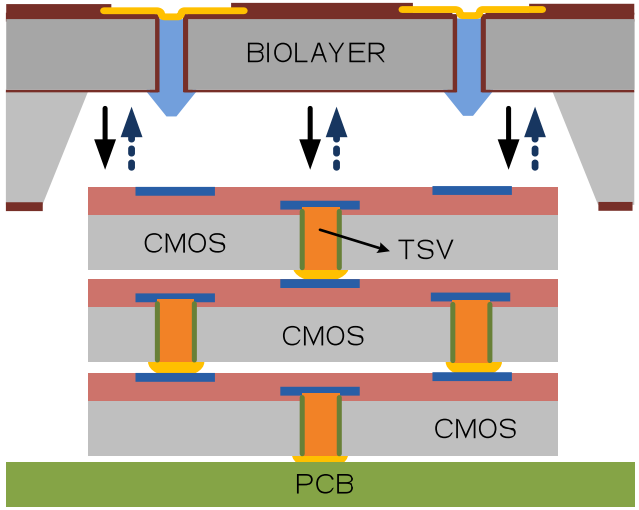
High speed/density CMOS technologies for digital circuits and memories

[Courtesy Guiducci: 2010]

Disposable bio-layer







No need for cleaning. Bio-layer is disposed after each measurement and CMOS layers are used repeatedly

Increased sensitivity and array density due to vertical interconnections from the bio-layer to the readout electronics

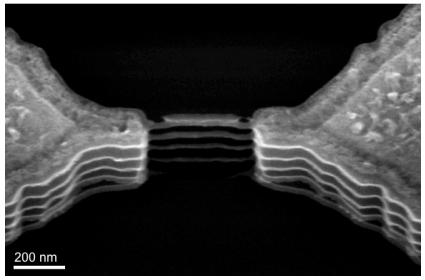
Sophisticated algorithms for highly-specific target identification run on-chip DSP and memory

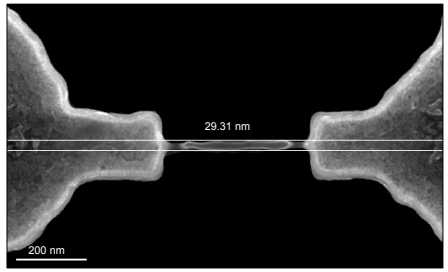
[C. Guiducci 2010]

Outline

- Introduction
- Technology
  - Devices
  - Circuits
- Architecture
  - Communication infrastructure
  - 3D Integration
- **Sensors**
- Applications
- Conclusions

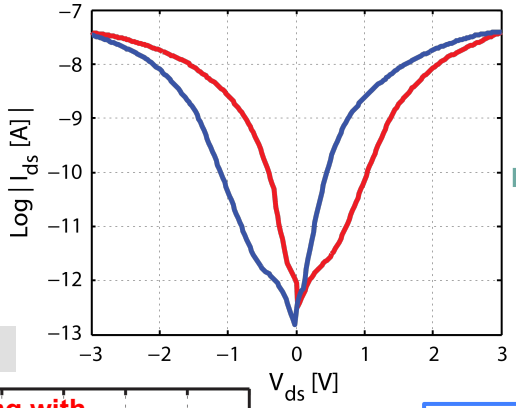
Memristive SiNW-based Biosensors

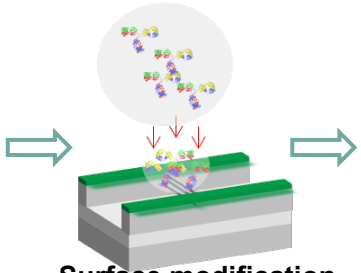


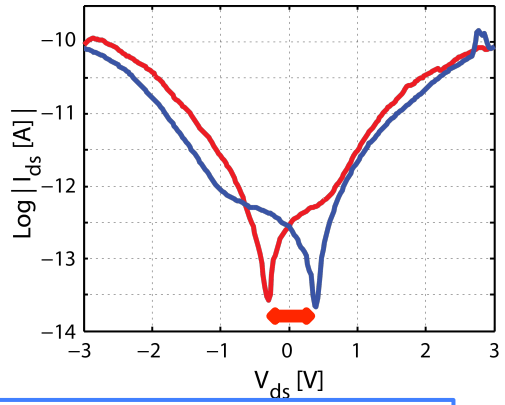


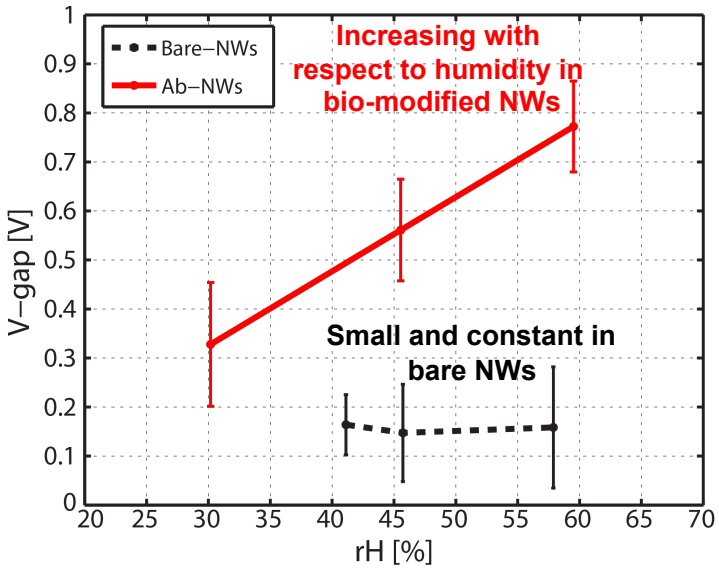
F. Puppo, IEEE T. Nanobiosci., submitted

- Crystalline, free-standing, Silicon Nanowires manifest memristive conductivity due to the nano-scale of the fabricated structures
- The voltage-gap between the forward and backward current minima in I/V curves increases after NW functionalization with antibodies

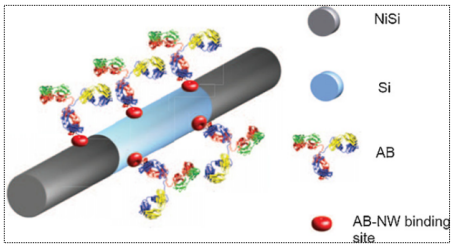






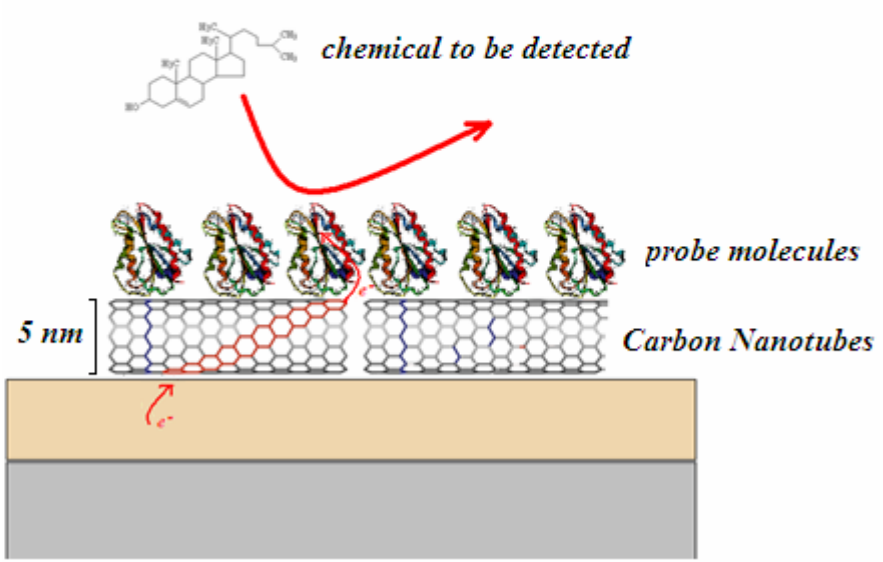


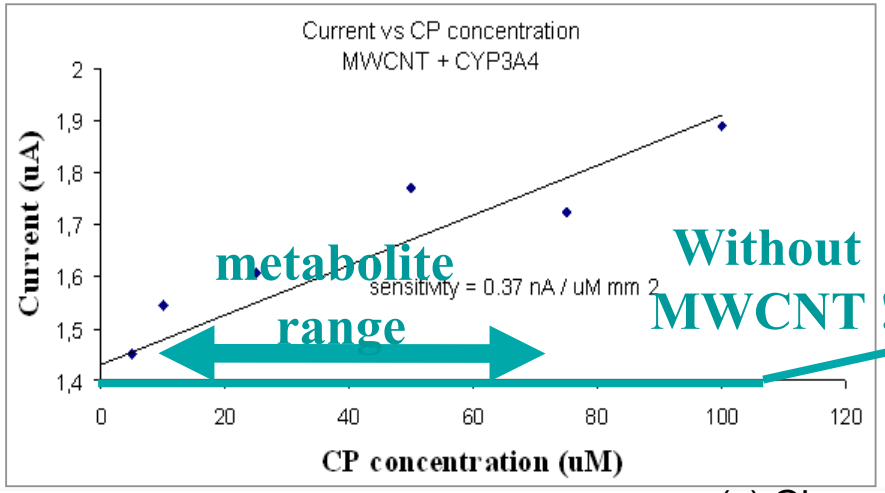
In a controlled humidity range, Si NW device sense antigen molecules (i.e., cancer biomarkers) thanks to molecule up-take (immuno-recognition events) displayed by voltage gap changes.

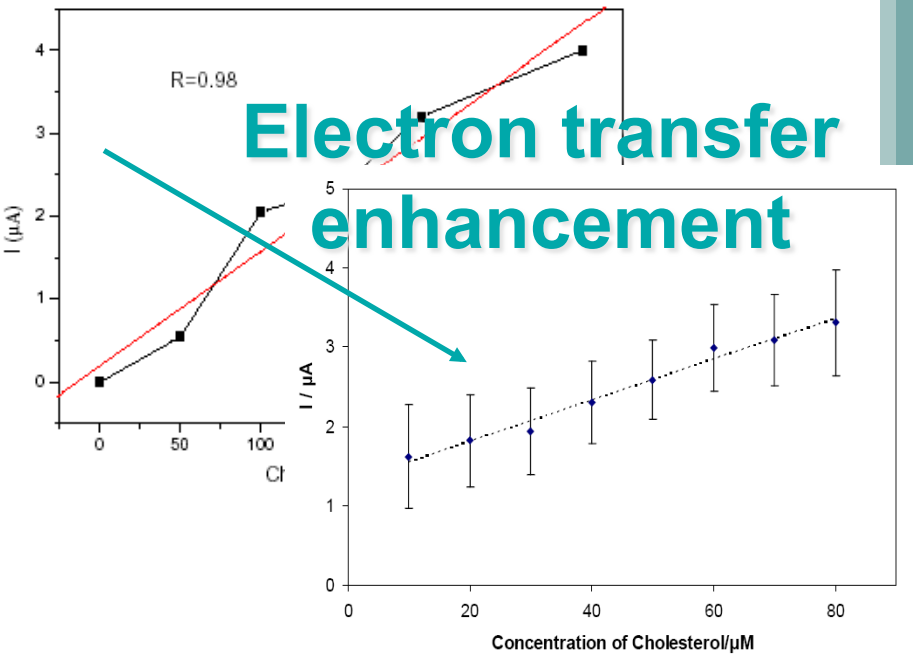


S. Carrara et al. ,
Sens. Actuators B, *2012*

CNT nanostructured sensors

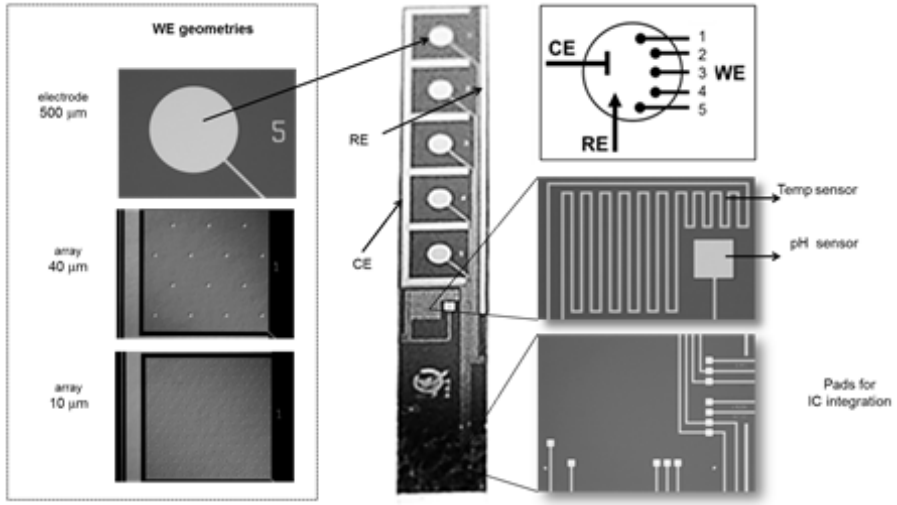


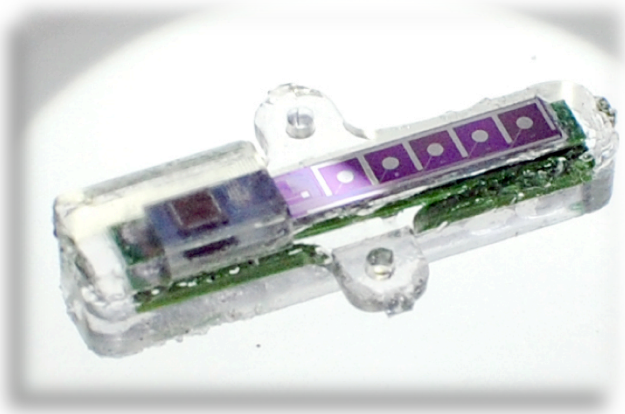


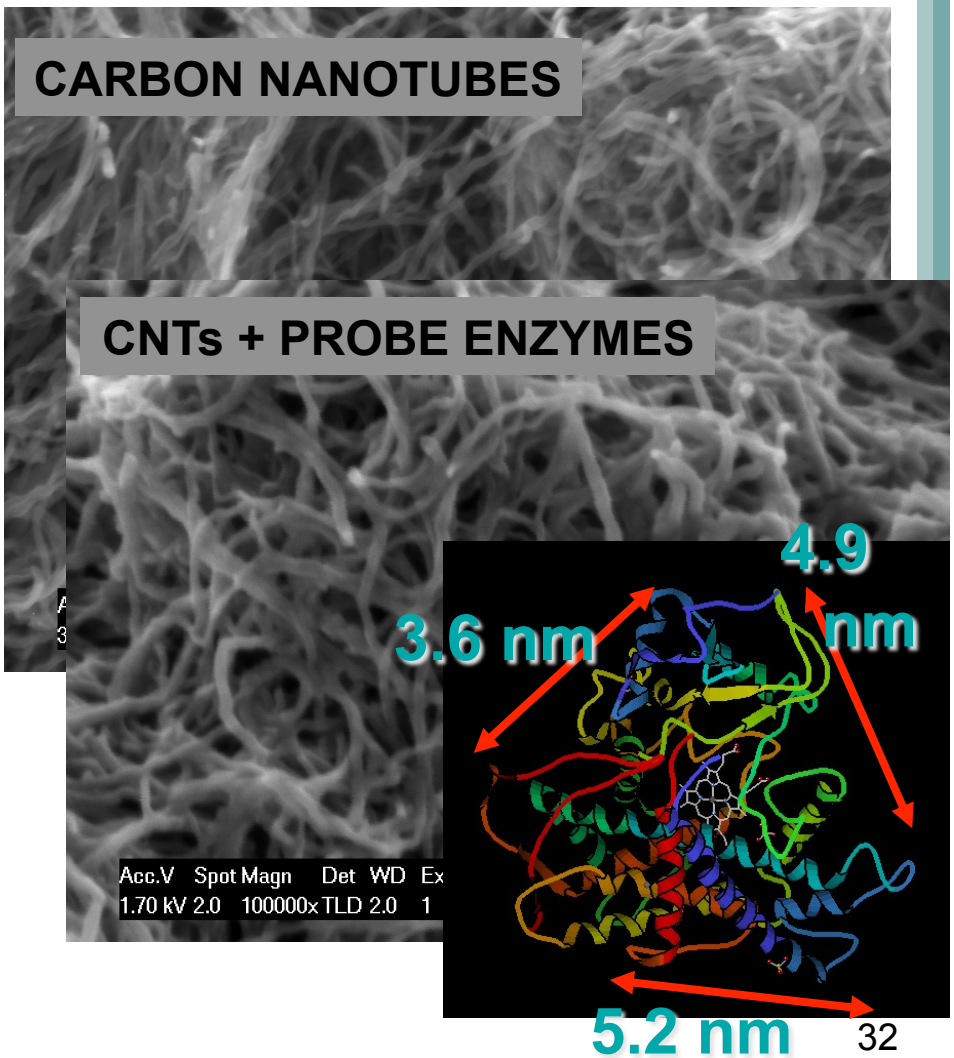


Cyclophosphamide detection - *S.Carrara*

CNT nano-structered electrodes







Outline

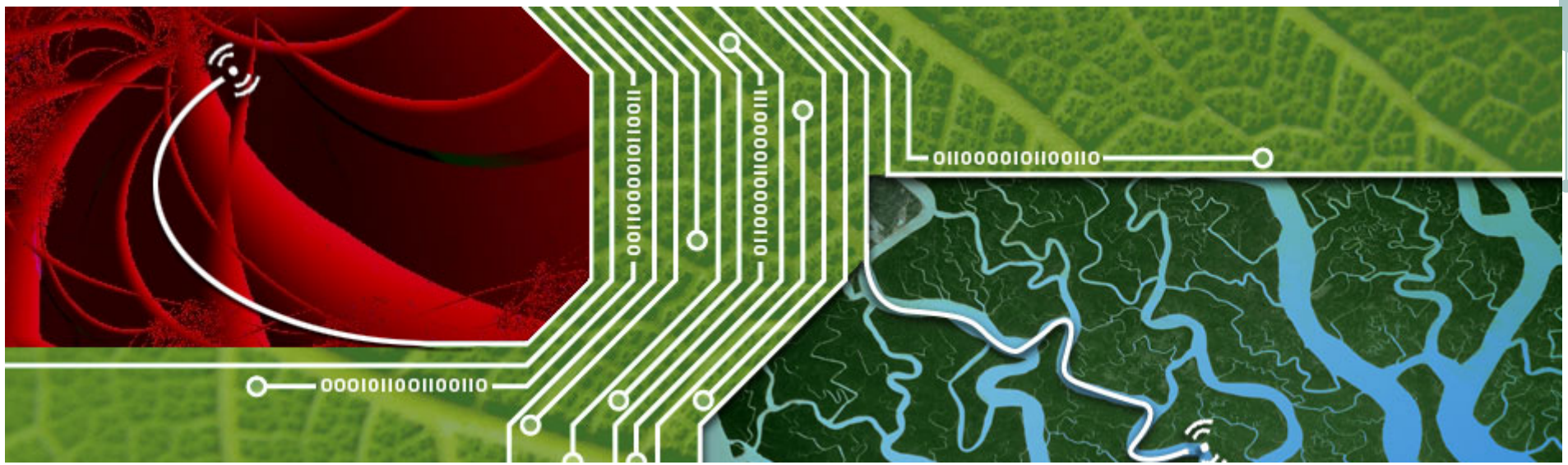
- Introduction
- Technology
  - Devices
  - Circuits
- Architecture
  - Communication infrastructure
  - 3D Integration
- Sensors
- **Applications**
- Conclusions

Nanosystems applications

- Health:
  - Personalized medicine, real-time medical monitoring
- Environment:
  - Weather, pollution monitoring, rock stability
- Energy:
  - Smart grid, data centers, energy-proportional computing
- Computing, communication, control
  - Scientific and consumer applications
- Defense:
  - Design of command and control systems

Nano-Tera.ch

- Health:
  - Personalized medicine, real-time medical monitoring
- Environment:
  - Weather, pollution monitoring, rock stability
- Energy:
  - Smart grid, data centers, energy-proportional computing



Conclusions

- Nano-systems exploit the synergy of devices, circuits and architectures
- New technologies enrich CMOS with novel devices
  - *Silicon nanowire* and *carbon nanotube* devices
  - Controlling *ambipolarity* can be efficiently used in logic design
- New architectures and design styles:
  - *Regularity* of the fabric is key to robustness
  - 3-Dimensional integration gives an extra degree of freedom
- Hybridization of new technologies opens new frontiers

Thank You