A Semi-Analytical Thermal Modeling Framework for Liquid-Cooled ICs

Arvind Sridhar, *Member, IEEE*, Mohamed M. Sabry, *Member, IEEE*, and David Atienza, *Senior Member, IEEE*

Abstract—With the development of liquid-cooled integrated circuits (ICs) using silicon microchannels, the study of heat transfer and thermal modeling in liquid-cooled heat sinks has gained interest in the last five years. As a consequence, several methodologies on the thermally-aware design of liquid-cooled 2-D/3-D ICs and multiprocessor system-on-chips (MPSoCs) have appeared in the literature. A key component in such methodologies is a fast and accurate thermal modeling technique that can be easily interfaced with design optimization tools. Conventional fully numerical techniques, such as finite-element methods, do not render themselves to enable such an easy interfacing with design tools and their order of complexity is too large for fast simulations. In this context, we present a new semi-analytical representation for heat flow in forced convective cooling inside microchannels, which is continuous in 1-D, i.e., along the direction of the coolant flow. This model is based on the well-known analogy between heat conduction and electrical conduction, and introduces distributed electrical parameters in the dimension considered to be continuous, resulting in a state-space representation of the heat transfer problem. Both steady state and transient semi-analytical models are presented. The proposed semi-analytical model is shown to have a closed-form solution for certain cases that are encountered in practical design problems. The accuracy of the model has been validated against state-of-the-art thermal modeling frameworks [1] (errors $\ll 1\%$), with 3X speed-up of our proposed modeling framework.

Index Terms—Forced convective cooling, liquid cooling of ICs, thermal modeling.

I. INTRODUCTION

LIQUID cooling of integrated circuits (ICs) using microchannels has recently gained interest [2]–[4] owing to the rising temperatures of 2-D and vertically-stacked 3-D ICs and multiprocessor system-on-chips (3-D MPSoCs). This cooling technology has been shown to be viable at different levels of packaging, from etching microchannels on a copper cold plate on top of the targeted IC [5], to etching the microchannels directly on the silicon dies in the case of 3-D ICs [4]. In addition to enabling further integration of CMOS circuits while maintaining safe operating temperatures better

than conventional air-cooling, liquid cooling also possesses the potential to increase cooling efficiency and enable energy harvesting when utilized in the large-scale datacenters. Hence, it is touted as a long-term green energy solution for next-generation datacenters [6].

Prototypes of 2-D and 3-D stacked ICs with microchannel liquid cooling have been built by various research groups around the world with promising results [3], [7], [8]. An example from IBM is shown in Fig. 1, where they have developed a 3-D IC emulator with interlayer liquid cooling. Further development of this technology and its large-scale use are strongly dependent upon sound early-stage design tools capable of: 1) accurately predicting the thermal performance of these cooling technologies and 2) prescribing optimized designs and dynamic run-time management tools that can maximize the electrical performance and energy efficiency of these systems while maintaining safe operating temperatures. At the heart of these research efforts is the need to develop an efficient thermal model that can enable fast design-space explorations.

Conventional fine-grained simulations such as the finite-element methods become infeasible for this purpose in the context of EDA owing to prohibitively large simulation times. Even the more compact methods based on finite-difference [1], [10] and other such purely-numerical techniques do not lend themselves to traditional optimization algorithms for fast thermal-aware design due to the significant simulation times of these numerical techniques, as well as the lack of appropriate compatibility for optimization problems. Instead, a vast number of often brute-force searches/machine learning techniques must be employed to find optimal designs, involving thousands of thermal simulations. This leads to long design-times and adds to the cost of production.

In this paper, we present a new semi-analytical thermal model for liquid-cooled ICs to address these issues. The proposed semi-analytical model is discrete (numerical) in 2-Ds, and continuous (analytical) in 1-D, i.e., the direction of coolant flow. We build this model based on the well-known analogy between heat transfer and electrical circuits. In the dimension where the model remains continuous, distributive electrical elements are utilized to create a transmission line-like model for heat transfer, which is a novel approach to studying heat transfer in liquid-cooled ICs. The main contributions of this paper are as follows.

1) A new semi-analytical model is derived that is spatially continuous in 1-D, i.e., along the direction of the flow of coolant. This semi-analytical model is developed for both steady state as well as transient simulations.
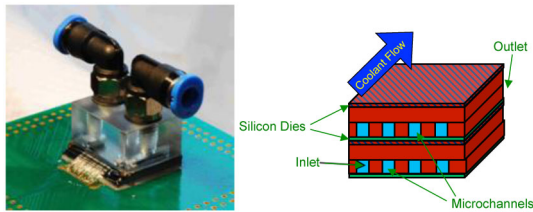
Fig. 1. Liquid-cooled 3-D IC emulator built by IBM [9] and its schematic showing the location of individual dies and the microchannel heat sink.

Fig. 2. Solid thermal cell and its equivalent electrical circuit.

2) A closed-form solution is also derived for the steady state semi-analytical model under certain circumstances.

3) The model has a succinct state-space form for the temperatures and heat flow variables in the model. This form of representation lends itself to significant simulation time reduction, by values up to 3X compared to 3D-ICE [1], with negligible errors ($\ll 1\%$). In addition, this representation can be easily applied in optimal design algorithms. We demonstrate this by discussing two recently advanced and important applications of the proposed model in thermal-aware design of liquid-cooled ICs.

The rest of the paper is organized as follows. Section II reviews the existing literature on the thermal modeling of liquid-cooled ICs. Section III describes the target representative problem being solved using the proposed semi-analytical model. In Section IV, the proposed semi-analytical model is presented and derived from the first principles. First, a steady state semi-analytical model for a test structure with a single microchannel is derived. Closed-form solutions are also derived for certain cases encountered in the design of ICs. Next, the semi-analytical model is extended for the more realistic case of multiple microchannels cooling the heat generated in an 3-D IC. Finally, the proposed model is extended for transient thermal analysis. In Section VI, we discuss the effectiveness of our proposed model when it is deployed in state-of-the-art design optimization schemes that aims to minimize thermal gradients and maximize energy efficiency in liquid-cooled ICs ([11] and [12], respectively). Finally, conclusions are presented in Section VII.

II. RELATED WORK

In this section, we briefly review the existing works on thermal modeling of ICs (both air- and liquid-cooled).

A. Thermal Modeling of Air-Cooled ICs

Thermal modeling of air-cooled ICs is traditionally performed by invoking the equivalence between heat conduction in solids and current flow in resistance–capacitance (RC) circuits. In this analogy, temperature is represented by voltage and heat flow is represented by current. Heat flow follows ohms law, and hence, thermal resistances and capacitances are calculated using the thermal conductivity and heat capacity of the material, respectively. Current sources and voltage sources, then, represent heat sources and boundary conditions respectively. Finite-difference approximation can be applied by diving an IC into small cuboidal blocks called thermal cells and constructing the equivalent circuit for each cell as shown
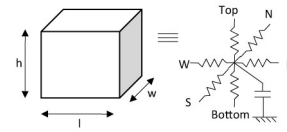
in Fig. 2. Finally, a complete 3-D thermal RC grid is constructed for the entire IC. This model can then be solved using circuit simulators methods to obtain the temperatures in the IC as a function of time. Thermal models such as HotSpot [13] have been proposed in the literature based on this principle.

B. Thermal Modeling for Liquid-Cooled ICs

Thermal modeling of liquid-cooled ICs consists of modeling the heat conduction in the solid parts of the IC as described above, with the addition of the following two new forms of heat transfer.

1) Convective heat transfer at the solid-liquid interface at the microchannel walls.

2) Advective transport of heat downstream from inlet to outlet inside the microchannels due to mass flow.

Traditional theoretical treatments forced convection problem in ducts or microchannels has involved representing the energy balance equations inside the microchannel as partial differential equations and then reducing them into ordinary differential equations based on the specific properties of the given problem. Then, numerical techniques such as finite-element and finite-difference methods are applied to solve for the conjugate conduction-convection problems along the entire length of the microchannels [14], [15]. In numerical fine-grained simulators, such as ANSYS CFX [16], the above modeling problem is solved by dividing the microchannel and the surrounding structures into very small cells/elements, then solving for the velocity profile of the coolant in every element, and finally calculating the heat transfer. Such methods, while being accurate, are extremely slow and are not suitable for the design of liquid-cooled ICs [9], which typically contain hundreds of microchannels resulting in millions of variables to solve for.

Even analytical (nonnumerical) studies of heat transfer in microchannels in mechanical engineering, aerospace engineering and thermal engineering focus on solving of the detailed cross-sectional velocity and temperature profiles for various flow conditions (entrance, developing, developed). They do not represent a compact solution suitable for system-level thermal analysis and optimization in early-stage IC design [14], [17]–[19]. Methods such as [4] can be used to simplify the heat transfer problem by assuming 1-D resistive network from the source of the heat to the inlet temperature, with the convective resistances being calculated using either numerical presimulations or empirical correlations. This model, illustrated in Fig. 3, oversimplifies the heat transfer problem and does not account for nonuniform heat distributions in an IC.

Recently, a finite-difference-based thermal model for liquid-cooled ICs, called 3D-ICE [1], [20], was presented. In this model, the microchannel layers in the IC are divided into thermal cells similar to the other solid layers as described in Section II-A. For the liquid thermal cells corresponding to the microchannels, an equivalent electrical circuit is constructed as shown in Fig. 4.
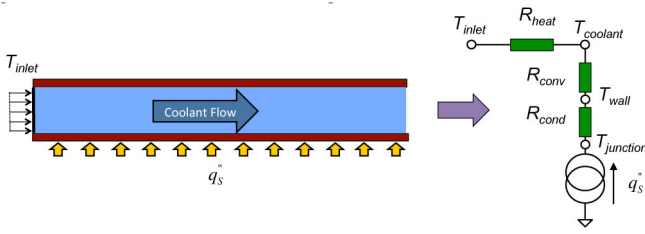
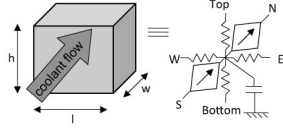Fig. 3. Simple 1-D model for forced convective cooling in microchannels [4].

Fig. 4. Liquid thermal cell and its equivalent electrical circuit in the 3D-ICE model [1].

Fig. 5. Heat transfer geometries. (a) 3-D view of the test microchannel structure. (b) Cross-sectional view of the test structure at distance z from the inlet.

Here, the convective heat transfer from the microchannel walls into the coolant is represented using four convective thermal resistances. The thermal capacitance is used to represent heat storage in the coolant similar to solids. Two voltage-controlled current sources are utilized to represent advection down the channel. This compact heat transfer model inside the microchannel can be connected to the surrounding thermal grid for the sold parts of the IC to create the complete 3-D thermal model for liquid-cooled IC, which can then be solved using circuit simulation techniques as before.

The 3D-ICE model has been proven to be accurate via experimental validation against numerical simulators and measurements from real IC test-stacks [1], [20], [21]. However, the problem sizes still tend to be huge-hundreds of thousands of unknowns for a typical IC. In addition, this method is purely numerical, thus not lending itself to efficient design-space exploration, where design parameters such as microchannel dimensions are varied over a large range and simulations repeated. We demonstrate in the ensuing sections that the proposed semi-analytical approach preserves the accuracy of this method while overcoming the aforementioned challenges. We choose this model as the benchmark to evaluate the accuracy of the proposed semi-analytical model due to two reasons.

1) This model has been extensively validated for accuracy against fine-grained numerical simulations as well as measurements from real liquid-cooled ICs [1], [20], [21].
2) This model allows us the flexibility to incorporate any user-defined heat transfer coefficients that can also be implemented in the proposed semi-analytical model for a fair comparison of the accuracy/efficacy of the proposed model.

III. BASIC CELL STRUCTURE OF THE TARGET MODEL

In order to present the proposed semi-analytical model, we must first consider the nature of the problem and the geometry of the basic cell structure for which we perform heat transfer analysis. As previously shown in Fig. 1, the target cooling technology places a number of microchannels between two silicon layers that contain the computing components. Thus, we start modeling from the basic structural component of the cooling layer, which is a single rectangular strip. This structure is shown in Fig. 5, where it shows a single rectangular microchannel is surrounded by silicon on all four sides.
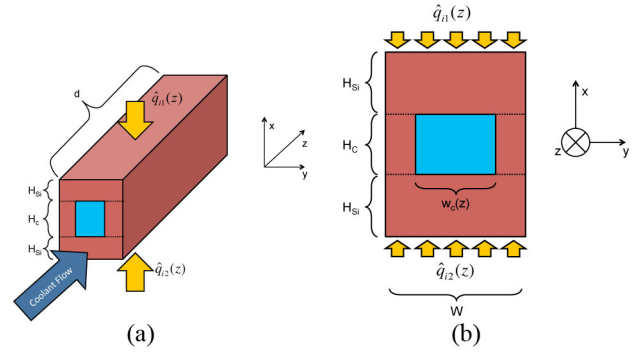
Coolant enters from the inlet (front side in the figure) at a volumetric flow rate of V and exits from the outlet at the rear end. The length of the microchannel is d, measured along the z direction with the inlet at $z = 0$. It is in this direction, that the model is continuous with no discretization. Two slabs of silicon, each of thickness H_{Si} cover the top and the bottom surfaces of the microchannel.

There are active heating elements on the exposed top and the bottom surfaces of these two slabs, respectively as shown in the figure. These active heating elements represent the electronic circuit fabricated on different surfaces that surround the microchannel. The variables corresponding to the top surface is designated with the subscript 1, the variables in the bottom surface with subscript 2, and those in the microchannel with the subscript C. In addition, there are two silicon walls on the sides of the microchannel. The total width of this test structure (measured along the y direction) is W, while the microchannel itself has a width that is a function of the distance from the inlet $w_C(z)$. The height of the microchannel is fixed to H_C. This assumption conforms to the traditional IC manufacturing process where it is easier to change the width of the microchannels by using different masks for etching, compared to varying their height during the fabrication. A realistic two-die IC with interlayer microchannel heat sink can be visualized as multiple such test structures (Fig. 5(a)) stacked one next to the other (along the x direction), where multiple microchannels running parallel to each other dissipate the heat generated at the two silicon surfaces. The heat flux patters on these two dies can be uniform or nonuniform.

A side ($x-z$ plane) view of this structure at a given distance z from the inlet is shown in Fig. 6(a). $T_1(z, t)$, $T_2(z, t)$, and $T_C(z, t)$ are the temperatures in silicon and the microchannel, and $q_1(z, t)$, $q_2(z, t)$, and $q_C(z, t)$ are the heat flows in silicon and microchannel parallel to the coolant flow as indicated in Fig. 6(a). The following assumptions are applied to the test structure for the sake of simplicity and without loss of generality, to model microchannels in ICs.

1) The heat fluxes entering from the top and the bottom surfaces of this structure are assumed to be uniform along the y direction (i.e., along the width of this structure), and hence, are purely functions of distance from the inlet z (and time t, in the case of transient analysis). The heat fluxes from the top and the bottom are thus divided by the width W and expressed as per unit length parameters $\hat{q}_{i1}(z, t)$ and $\hat{q}_{i2}(z, t)$.

2) A constant inlet temperature at the inlet of the microchannel ($T_{C,in}$) serves as the fixed boundary condition for the model. The temperature of the fluid at the outlet is assumed to be purely a function of the heat carried out by it, with no additional heat accumulation/dissipation outside the outlet.

3) All other exposed surfaces in the structure are assumed to be adiabatic with the microchannel heat sink serving as the sole dissipator of heat.

4) Inside the microchannel, the advective heat transport is assumed to be much larger than the conduction of heat in the fluid along the direction of the flow (z), which is reasonable for all practical applications.

With the above assumptions in mind, the goal of the proposed semi-analytical model is to compute the temperatures of the top and bottom silicon surfaces of the cell structure ($T_1(z, t)$, $T_2(z, t)$), and the coolant temperature ($T_C(z, t)$) for any given set of heat flux distributions on the silicon surfaces ($\hat{q}_{i1}(z, t)$ and $\hat{q}_{i2}(z, t)$).

IV. PROPOSED SEMI-ANALYTICAL MODEL

Since discretized units in a thermal modeling problem (thermal cells) are represented using discrete or lumped electrical parameters, we hypothesize that the equivalent electrical representation for models which are continuous in 1-D must employ distributed electrical elements such as per-unit-length resistances and capacitances. With this intuition in mind, we first consider an infinitesimally small section of the test structure, of length Δz at distance z from the inlet as shown in Fig. 6(a). The temperatures at the top and bottom silicon surfaces (junction) and the microchannel (T_1, T_2, and T_C) and the heat flow at these locations in parallel to the microchannel (q_1, q_2, and q_C) are indicated along with the per-unit-length parameters. These parameters are as follows.

1) Per-unit-length heat fluxes $\hat{q}_{i,1}(z)$ and $\hat{q}_{i,2}(z)$ (expressed in W/m) entering the top and bottom silicon junctions.

2) Per-unit-length longitudinal conductance in silicon parallel to the direction of the fluid flow in the microchannel $\hat{g}_l = k_{Si} \cdot W \cdot H_{Si}$ (expressed in W.m/K), where k_{Si} is the silicon thermal conductivity. This parameter is assumed to be independent of the distance z as there is not variation in the silicon cross-sectional dimensions or material properties along its length.

3) Per-unit-length vertical conductance from the silicon junctions to the fluid bulk in the microchannel $\hat{g}_v(z) = \left(\hat{g}_{v,cond}^{-1} + \hat{g}_{v,conv}^{-1} \right)^{-1}$ (expressed in W/m.K), where $g_{v,cond} = k_{Si} \frac{W}{H_{Si}}$ and $g_{v,conv} = h_{eff}(z) \cdot W$. This parameter combines both the vertical conduction in the silicon slab and the effective convection heat transfer ($h_{eff}(z)$) at the solid–liquid interface of the microchannel. Hence, this parameter changes with the distance z, as the microchannel dimensions and fluid flow properties (boundary layer formation, type of flow, temperature, etc.) change.

In addition, there is conduction along the silicon side walls between the top and the bottom junctions. This parameter is neglected in the present analysis for simplicity. It can be
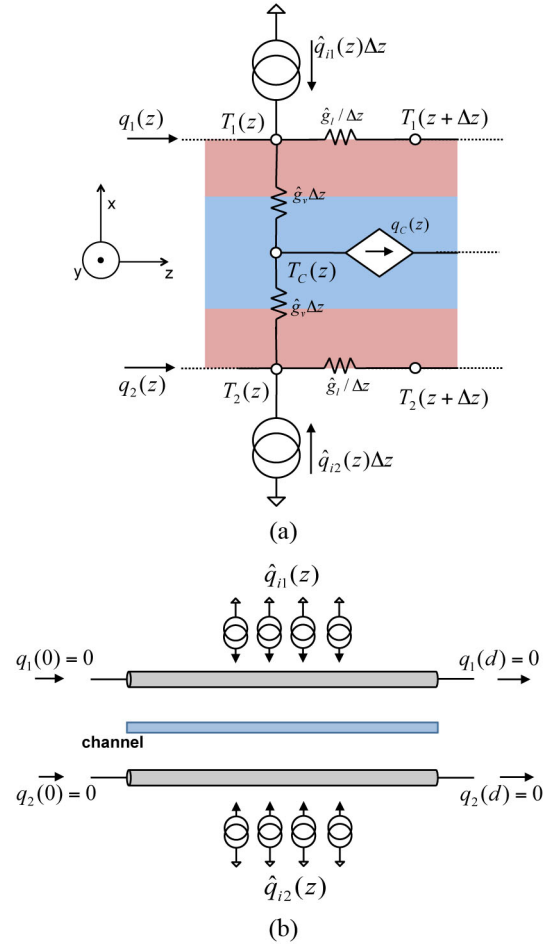

Fig. 6. (a) Infinitesimally small section of the test structure at distance z from the inlet. (b) Equivalent transmission line-like representation for the heat flow in the test structure.

incorporated later in the model without any loss of generality. We first derive and study the steady-state version of the proposed semi-analytical model for the test structure. We will then derive closed-form solutions to this semi-analytical model for specific scenarios. In the next subsection, we extend this model to the more complex case of multiple parallel microchannels cooling an IC. Finally, we will derive the semi-analytical model for transient analysis of the test structure.

A. Steady-State Semi-Analytical Model

Using the parameters defined above, the following set of equations can be written to express the relationship between temperatures and heat flows at the far end of this section ($z + \Delta z$) in terms of the temperatures and heat flows at the near end (z):

$$(1.1) \quad T_1(z + \Delta z) = T_1(z) - \frac{1}{\hat{g}_l / \Delta z} q_1(z)$$

$$(1.2) \quad q_1(z + \Delta z) = q_1(z) - [T_1(z) - T_C(z)] \hat{g}_v \Delta z + \hat{q}_{i1}(z) \Delta z$$

$$(2.1) \quad T_2(z + \Delta z) = T_2(z) - \frac{1}{\hat{g}_l / \Delta z} q_2(z)$$

$$(2.2) \quad q_2(z + \Delta z) = q_2(z) - [T_2(z) - T_C(z)] \hat{g}_v \Delta z + \hat{q}_{i2}(z) \Delta z$$

$$(3) \quad c_v \cdot V \cdot T_C(z) = q_C(z).$$

$$(1)$$

By rewriting the above equations and taking the limit $z \to 0$, we get

$$(1.1) \quad \frac{d}{dz}T_1(z) = -\frac{1}{\hat{g}_l}q_1(z)$$

$$(1.2) \quad \frac{d}{dz}q_1(z) = -[T_1(z) - T_C(z)]\hat{g}_v + \hat{q}_{i1}(z)$$

$$(2.1) \quad \frac{d}{dz}T_2(z) = -\frac{1}{\hat{g}_l}q_2(z) \qquad (2)$$

$$(2.2) \quad \frac{d}{dz}q_2(z) = -[T_2(z) - T_C(z)]\hat{g}_v + \hat{q}_{i2}(z)$$

$$(3) \quad c_v \cdot V \cdot T_C(z) = q_C(z).$$

The above set of equations represent a distributed heat transfer model which is an intermediate step in deriving the final semi-analytical model. There are some important observations to be made in this distributed heat transfer model before proceeding with the derivations, as described next.

In the above sets of equations, note that (2.3) is not a differential equation because the heat flow in the direction of the fluid flow inside the microchannel is a direct function of its temperature at any given point based on the heat flow governing equations in fluids [1] and the assumptions in Section III.

B. Analogy of Telegraphers Equations

Invoking the hypothesis at the beginning of this section that the electrical analogy for heat flow in a nondiscretized dimension must incorporate distributed electrical elements, the first four equations in (2) resemble the telegraphers equations used to describe distributed voltages and currents in a multiconductor transmission line [22]. The analogy between (2) and transmission lines is illustrated in Fig. 6(b). However, there are certain important characteristics of the above distributed heat transfer model that differentiates it from a conventional transmission line in this analogy.

1) There are no delay/lossless terms in the distributed heat transfer model since classical heat transfer follows a diffusive parabolic differential equations model and not a wave equation. Hence, unlike a conventional transmission line, there are only lossy and admittance terms (resistances, conductances, and capacitances).

2) Following the assumptions of adiabatic boundaries at the exposed surfaces of silicon in the previous section, the longitudinal heat flows $q_1(z)$ and $q_2(z)$ near the inlet and the outlet ($z = 0$ and $z = d$) must be zero. These boundary conditions translates to a transmission line which is always open circuited at the input and the output as shown in Fig. 6(b).

3) While the conventional transmission lines are generally modeled using homogenous telegraphers equations [22], the presence of distributed sources ($\hat{q}_{i1}(z)$ and $\hat{q}_{i2}(z)$), renders the corresponding equations for the above distributed heat transfer model inhomogenous requiring special solving techniques.

4) The microchannel, functioning as the heat sink, corresponds to the ground/reference conductor in a conventional transmission line that acts as a return path of currents. This ground line is typically assumed to be the reference node at all points along the length of the transmission line against which voltages are measured. In the
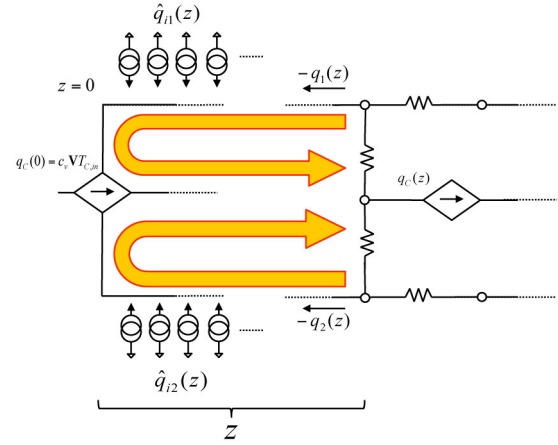

Fig. 7. Illustration of the accumulation of heat inside the microchannel in steady state.

above distributed heat transfer model, however, the channel does not act as an ideal ground since the absolute temperature of the fluid increases as it accumulates heat from inlet to outlet. Hence, this change in the reference voltage must be taken into account and incorporated in the distributed model for the correct simulation of temperatures.

Note that if assumption 3 in Section III was dropped and the dissipation of heat into the ambient was also considered, the model would have an additional distributed thermal resistance connecting one or more layers in the test structure to a ground or voltage reference (corresponding to the ambient temperature) from inlet to outlet, without changing any other aspect of the model derivation or structure.

C. Formulation of the Proposed Semi-Analytical Model

As described above, in order to incorporate the changing fluid temperature from inlet to outlet, we must express the temperature of the fluid $T_C(z)$ in (2.3) in terms of the temperatures and heat flow variables in silicon. This can be accomplished by estimating exactly the amount of heat carried by the fluid at any distance z from the inlet, recognizing that the microchannel is the only heat sink through which all the heat generated inside the test structure can be dissipated. For this, consider Fig. 7. The heat being transported downstream at any distance z, expressed as $q_C(z)$ must be the sum of the following.

1) The amount of heat with which the fluid entered the structure at the inlet, $q_{C,in} = q_C(0) = c_v \cdot V \cdot T_{C,in}$, which is a fixed value, since the inlet temperature is assumed to be constant.

2) The amount of heat generated at the silicon junctions from inlet ($z = 0$) until the current location z. This can be expressed integrating $\hat{q}_{i1}$ and $\hat{q}_{i2}$ for the segment $[0, z]$.

3) The amount of heat entering the region left of the location z (i.e., the region upstream to the current location) from the region right of this location, namely, the region downstream to the current location via longitudinal conduction inside silicon, expressed as $-(q_1(z) + q_2(z))$, as illustrated in Fig. 7.

Hence, we can write

$$T_C(z) = T_{C,in} + \frac{1}{c_v \cdot V} \int_0^z \left(\hat{q}_{i1}(z) + \hat{q}_{i2}(z) \right) dz$$
$$- \frac{1}{c_v \cdot V} \left(q_1(z) + q_2(z) \right). \tag{3}$$

Substituting (3) in (2.1.1–2.2), and writing $Q_{i1}(z) \equiv \int_0^z \hat{q}_{i1}(z)$ and $Q_{i2}(z) \equiv \int_0^z \hat{q}_{i2}(z)$, we get

$$\frac{d}{dz} \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} = \mathbf{A}(z) \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} + \mathbf{U}(z) \tag{4}$$

where

$$\mathbf{T}(z) = \begin{bmatrix} T_1(z) \\ T_2(z) \end{bmatrix}, \quad \mathbf{q}(z) = \begin{bmatrix} q_1(z) \\ q_2(z) \end{bmatrix}$$

$$\mathbf{A}(z) = \begin{bmatrix} 0 & 0 & \frac{1}{\hat{g}_l} & 0 \\ 0 & 0 & 0 & \frac{1}{\hat{g}_l} \\ -\hat{g}_v(z) & 0 & \frac{-\hat{g}_v(z)}{c_v \cdot V} & \frac{-\hat{g}_v(z)}{c_v \cdot V} \\ -\hat{g}_v(z) & 0 & \frac{-\hat{g}_v(z)}{c_v \cdot V} & \frac{-\hat{g}_v(z)}{c_v \cdot V} \end{bmatrix} \quad \text{and}$$

$$\mathbf{U}(z) = \begin{bmatrix} 0 \\ 0 \\ \hat{g}_v(z) T_{C,in} + \frac{\hat{g}_v(z)}{c_v \cdot V} \left(Q_{i1}(z) + Q_{i2}(z) \right) + \hat{q}_{i1}(z) \\ \hat{g}_v(z) T_{C,in} + \frac{\hat{g}_v(z)}{c_v \cdot V} \left(Q_{i1}(z) + Q_{i2}(z) \right) + \hat{q}_{i2}(z) \end{bmatrix}. \tag{5}$$

The above system of equations represents the semi-analytical model for heat transfer in the test structure in steady state. The solution to this system of equations can be written as follows:

$$\begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} = e^{\Gamma(z)} \begin{bmatrix} \mathbf{T}(0) \\ \mathbf{q}(0) \end{bmatrix} + \int_0^z e^{\Gamma(z) - \Gamma(\eta)} \mathbf{U}(\eta) d\eta \tag{6}$$

where

$$\Gamma(z) = \int_0^z \mathbf{A}(\lambda) d\lambda. \tag{7}$$

The matrix exponential and the integration on the RHS in (6) is clearly nontrivial to compute. However, under certain conditions, a closed form solution to the temperatures in the silicon junction can be obtained. The semi-analytical model represented by (4) can be simplified if the width of the microchannel $w_C(z)$ and the corresponding effective heat transfer coefficient $h_{eff}(z)$ are assumed to be constant. This occurs when the flow is considered to be fully developed, which works as a reasonable approximation to the actual flow in many practical applications [23]. Hence, $\hat{g}_v(z) = \hat{g}_v$, $\mathbf{A}(z) = \mathbf{A}$, and $\Gamma(z) = \mathbf{A}z$. Now, (4) can be written as

$$\frac{d}{dz} \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} = \mathbf{A} \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} + \mathbf{U}(z). \tag{8}$$

The solution to the above set of equations depends upon the nature of the functions $\hat{q}_{i1}(z)$ and $\hat{q}_{i2}(z)$. In the next subsection, the derivation of closed-form solutions to this model under specific conditions are described.

D. Closed-Form Solutions to the Proposed Semi-Analytical Model

One important feature of the proposed semi-analytical model is the possibility of deriving closed form solutions to (8). This is due to the fact that typically—in the context of ICs—the heat flux at the silicon junction is either uniform, or is distributed in the form of rectangular areas of different uniform heat flux densities across the 2-D surface of the silicon die. Hence, the functions $\hat{q}_{i1}(z)$ and $\hat{q}_{i2}(z)$ can be partitioned into piece-wise uniform regions and the integrations involved in solving the inhomogeneity of (8) can be performed over these partitions. This is illustrated as follows.

For the single microchannel test structure under consideration, the heat flux can be translated to per-unit-length heat constant flux densities, or piece-wise constant functions of z. That is

$$\hat{q}_{i1}(z) = \begin{cases} \hat{q}_{i1}^1 & 0 \leq z < z_1 \\ \hat{q}_{i1}^2 & z_1 \leq z < z_2 \\ \vdots & \vdots \\ \hat{q}_{i1}^n & z_{n-1} \leq z \leq d \end{cases}$$

$$\hat{q}_{i2}(z) = \begin{cases} \hat{q}_{i2}^1 & 0 \leq z < z_1 \\ \hat{q}_{i2}^2 & z_1 \leq z < z_2 \\ \vdots & \vdots \\ \hat{q}_{i2}^n & z_{n-1} \leq z \leq d \end{cases}$$
$$\text{where } 0 < z_1 < z_2 < \cdots < z_{n-1} < d. \tag{9}$$

Note that the superscripts in the above definitions represent the location number of the corresponding heat flux value and not a mathematical function.

Case A: Assuming uniform heat fluxes, with $\hat{q}_{i1}(z) = \hat{q}_{i1}^0$ and $\hat{q}_{i2}(z) = \hat{q}_{i2}^0$, $\forall z$, the cumulative heat flux functions in (5) can be written as

$$\begin{aligned} Q_{i1}(z) &= \hat{q}_{i1}^0 z \\ Q_{i2}(z) &= \hat{q}_{i2}^0 z. \end{aligned} \tag{10}$$

Thus, (8) reduces to

$$\frac{d}{dz} \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} = \mathbf{A} \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} + \mathbf{B}z + \mathbf{C} \tag{11}$$

where

$$\mathbf{B} = \frac{\hat{g}_v}{c_v \cdot V} \begin{bmatrix} 0 \\ 0 \\ \hat{q}_{i1}^0 + \hat{q}_{i2}^0 \\ \hat{q}_{i1}^0 + \hat{q}_{i2}^0 \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 0 \\ 0 \\ \hat{g}_v T_{C,in} + \hat{q}_{i1}^0 \\ \hat{g}_v T_{C,in} + \hat{q}_{i2}^0 \end{bmatrix}. \tag{12}$$

Solving (11) according to (6), we get

$$\begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} = e^{\mathbf{A}z} \begin{bmatrix} \mathbf{T}(0) \\ \mathbf{q}(0) \end{bmatrix} + \int_0^z e^{\mathbf{A} \cdot (z - \eta)} \left(\mathbf{B}\eta + \mathbf{C} \right) d\eta. \tag{13}$$

Thus, at $z = d$, we can write

$$\begin{bmatrix} \mathbf{T}(d) \\ \mathbf{q}(d) \end{bmatrix} = e^{\mathbf{A}d} \begin{bmatrix} \mathbf{T}(0) \\ \mathbf{q}(0) \end{bmatrix} + \int_0^d e^{\mathbf{A} \cdot (d - \eta)} \left(\mathbf{B}\eta + \mathbf{C} \right) d\eta$$
$$= \mathbf{M} \begin{bmatrix} \mathbf{T}(0) \\ \mathbf{q}(0) \end{bmatrix} + \mathbf{N} \tag{14}$$

where

$$\mathbf{M} = e^{\mathbf{A}d},$$
$$\mathbf{N} = \left[e^{\mathbf{A}d} - \mathbf{A}d - \mathbf{I} \right] \mathbf{A}^{-2} \mathbf{B} + \left[e^{\mathbf{A}d-\mathbf{I}} \right] \mathbf{A}^{-1} \mathbf{C}. \quad (15)$$

The above equation is the closed-form solution to Case A. However, remember that we do not know the temperatures at $z = 0$, i.e., $\mathbf{T}(0)$, but we do know that all heat flows are zero at the terminations (since the exposed surfaces are adiabatic), i.e., $\mathbf{q}(0) = \mathbf{q}(d) = \mathbf{0}$. Next, we rearrange the above solution such that the unknowns are on the LHS; and divide the matrix $\mathbf{M}$ into four equal square sub matrices and the vector $\mathbf{N}$ into two equal parts as follows:

$$\mathbf{M} = \begin{bmatrix} \mathbf{M}_{11} & \mathbf{M}_{12} \\ \mathbf{M}_{21} & \mathbf{M}_{22} \end{bmatrix}, \quad \mathbf{N} = \begin{bmatrix} \mathbf{N}_1 \\ \mathbf{N}_2 \end{bmatrix}. \quad (16)$$

Using the above representation, we finally obtain

$$\begin{bmatrix} \mathbf{T}(0) \\ \mathbf{T}(d) \end{bmatrix} = \begin{bmatrix} -\mathbf{M}_{21}^{-1}\mathbf{N}_2 \\ \mathbf{N}_1 - \mathbf{M}_{11}\mathbf{M}_{21}^{-1}\mathbf{N}_2 \end{bmatrix}. \quad (17)$$

The temperatures $\mathbf{T}(0)$ obtained above can then be substituted back into (13) to obtain the temperatures at any distance z. Hence, the complete temperature distribution at the silicon junction can be reconstructed.

Case B: Assuming piecewise constant heat flux distribution on the silicon junction, the cumulative heat fluxes can be written as

$$Q_{i1}(z) = \sum_{k=1}^{p} \hat{q}_{i1}^k \Delta z_k + \hat{q}_{i1}^{p+1} \left(z - z_p \right)$$
$$Q_{i2}(z) = \sum_{k=1}^{p} \hat{q}_{i2}^k \Delta z_k + \hat{q}_{i2}^{p+1} \left(z - z_p \right) \quad (18)$$

where

$$z_p = \left\{ \max \left(\{z_0, z_1, z_2, \cdots, z_{n-1}\} \right) | z_p \le z \right\}$$
$$\Delta z_k = z_k - z_{k-1}. \quad (19)$$

Here, we set $z_0 \equiv 0$ and $z_n \equiv d$. Hence, (8) now becomes

$$\frac{d}{dz} \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} = \mathbf{A}(z) \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \end{bmatrix} + \mathbf{B}_p z + \mathbf{C}_p \quad (20)$$

where

$$\mathbf{B}_p = \begin{bmatrix} 0 \\ 0 \\ \hat{q}_{i1}^{p+1} + \hat{q}_{i2}^{p+1} \\ \hat{q}_{i1}^{p+1} + \hat{q}_{i2}^{p+1} \end{bmatrix}$$

$$\mathbf{C}_p = \begin{bmatrix} 0 \\ 0 \\ G_i \\ G_i \end{bmatrix}$$

$$G_i = \hat{g}_v T_{C,in} + \hat{q}_{i1}^{p+1}$$
$$+ \frac{\hat{g}_v}{c_v V} \left\{ \sum_{k=1}^{p} \left(\hat{q}_{i1}^k + \hat{q}_{i2}^k \right) \Delta z_k - \left(\hat{q}_{i1}^{p+1} + \hat{q}_{i2}^{p+1} \right) z_p \right\}. \quad (21)$$

Solving the above similar to Case A yields

$$\begin{bmatrix} \mathbf{T}(d) \\ \mathbf{q}(d) \end{bmatrix} = e^{\mathbf{A}d} \begin{bmatrix} \mathbf{T}(0) \\ \mathbf{q}(0) \end{bmatrix} + \sum_{j=1}^{n} \int_{z_{j-1}}^{z_j} e^{\mathbf{A}\cdot(d-\eta)} \left(\mathbf{B}_j \eta + \mathbf{C}_j \right) d\eta$$
$$= \mathbf{M} \begin{bmatrix} \mathbf{T}(0) \\ \mathbf{q}(0) \end{bmatrix} + \mathbf{N} \quad (22)$$

where

$$\mathbf{M} = e^{\mathbf{A}d}$$

$$\mathbf{N} = e^{\mathbf{A}d} \left[\sum_{j=1}^{n} \left\{ \left(z_{j-1} e^{-\mathbf{A}z_{j-1}} - z_j e^{-\mathbf{A}z_j} \right) \mathbf{A}^{-1} \right. \right.$$
$$+ \left(e^{-\mathbf{A}z_{j-1}} - e^{-\mathbf{A}z_j} \right) \mathbf{A}^{-2} \right\} \mathbf{B}_j$$
$$\left. + \left(e^{-\mathbf{A}z_{j-1}} - e^{\mathbf{A}z_j} \right) \mathbf{A}^{-1} \mathbf{C}_j \right]. \quad (23)$$

The equation can be rearranged and the unknown terminal temperatures can be computed similar to Case A.

The above two cases, for which close-form solutions have been derived, cover a small subset of the many different scenarios that could be encountered when designing microchannel heat sinks. But even when the problem becomes more complex and nonlinear, such as when the systems matrix $\mathbf{A}$ becomes a function of distance z because of changing convective resistances in a developing flow or when the microchannel dimensions are no longer uniform but a function of distance, it would still be possible to derive such closed-form solutions if the system parameters are polynomial functions of the distance. Nevertheless, closed-form solutions for such cases become too complex to derive and implement for practical applications. It is much more desirable to use numerical techniques to solve this problem under such circumstances, as will be described in Section V.

E. Steady-State Semi-Analytical Model for Multiple Parallel Microchannels

The theory developed in the previous subsections can be extended to the case of multiple microchannels dissipating heat generated in the two silicon junctions. This conforms closer to the realistic scenario of multiple microchannels cooling an IC with nonuniform 2-D heat flux patterns (called the floorplan) in the active layers (e.g., the nonuniform floorplan of the UltraSPARC T1 [24]). For simplicity, consider Fig. 8(a). Here, the two test structures of width W each (called tracks henceforth) from the previous subsection have been stacked next to each other. In this test structure, in addition to longitudinal heat conduction parallel to the microchannel and the vertical heat conduction between the junction and the microchannel layer, there is also lateral heat conduction in silicon between the two tracks in both layers. This adds a layer of complexity in the derivation of the proposed semi-analytical model.

The corresponding distributed heat transfer model for this structure is illustrated with the help of an infinitesimally small section of this structure in Fig. 8(b). As indicated in this figure, the temperature variables in the different components of this structure are designated as $\{T_{11}(z), T_{21}(z), T_{12}(z), T_{22}(z), T_{C1}(z), T_{C2}(z)\}$, where the first subscript indicates the vertical location of the variable (the number of the layer, along
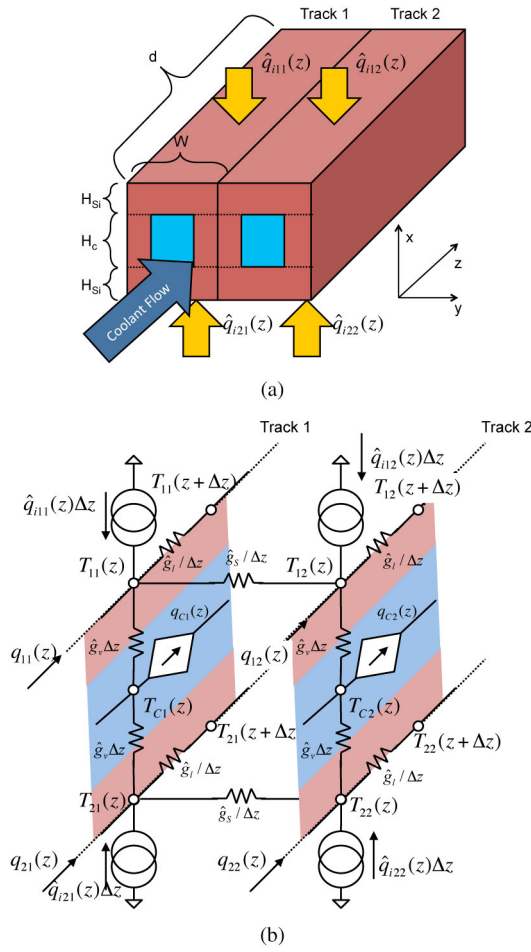
Fig. 8. (a) Test structure with two tracks of microchannels stacked next to each other. (b) Infinitesimally small section of this test structure.

the y direction) and the second subscript indicates the lateral location (the number of the track, along the x direction). The corresponding heat flow and input heat flux variables are $\{q_{11}(z), q_{21}(z), q_{12}(z), q_{22}(z), q_{C1}(z), q_{C2}(z)\}$ and $\{\hat{q}_{i11}(z), \hat{q}_{i21}(z), \hat{q}_{i12}(z), \hat{q}_{i22}(z)\}$.

The state-space equations for the temperature variables in silicon, corresponding to (2.1.1) and (2.2.1), can be written as

$$\frac{d}{dz}\mathbf{T}(z) = \Lambda \mathbf{q}(z) \tag{24}$$

where

$$\mathbf{T}(z) = \begin{bmatrix} T_{11}(z) \\ T_{12}(z) \\ T_{21}(z) \\ T_{22}(z) \end{bmatrix}, \quad \mathbf{q}(z) = \begin{bmatrix} q_{11}(z) \\ q_{12}(z) \\ q_{21}(z) \\ q_{22}(z) \end{bmatrix} \tag{25}$$

$$\Lambda = \begin{bmatrix} -1/\hat{g}_l & 0 & 0 & 0 \\ 0 & -1/\hat{g}_l & 0 & 0 \\ 0 & 0 & -1/\hat{g}_l & 0 \\ 0 & 0 & 0 & -1/\hat{g}_l \end{bmatrix}.$$

Similarly, the state-space equations for the heat flow variables in silicon [corresponding to (2.1.2) and (2.2.2)] can be rewritten, recognizing that there are two directions in which heat is dissipated vertically into the microchannel, and lateral to neighboring track, as

$$\frac{d}{dz}\mathbf{q}(z) = \Psi\mathbf{T}(z) + \mathbf{G_v}\mathbf{T_C}(z) + \hat{\mathbf{q}}_i(z) \tag{26}$$

where

$$\mathbf{T_C}(z) = \begin{bmatrix} T_{C1}(z) \\ T_{C2}(z) \end{bmatrix}, \quad \hat{\mathbf{q}}_i(z) = \begin{bmatrix} \hat{q}_{i11}(z) \\ \hat{q}_{i12}(z) \\ \hat{q}_{i21}(z) \\ \hat{q}_{i22}(z) \end{bmatrix}$$

$$\Psi = \begin{bmatrix} -(\hat{g}_v + \hat{g}_s) & \hat{g}_s & 0 & 0 \\ \hat{g}_s & -(\hat{g}_v + \hat{g}_s) & 0 & 0 \\ 0 & 0 & -(\hat{g}_v + \hat{g}_s) & \hat{g}_s \\ 0 & 0 & \hat{g}_s & -(\hat{g}_v + \hat{g}_s) \end{bmatrix}$$

$$\mathbf{G_v} = \begin{bmatrix} \hat{g}_v & 0 \\ 0 & \hat{g}_v \\ \hat{g}_v & 0 \\ 0 & \hat{g}_v \end{bmatrix}. \tag{27}$$

Here, $\hat{g}_s = k_{Si} \cdot H_{Si}/W$ is the per-unit-length conductance in silicon between the two tracks in the lateral direction. As in (2), we have neglected the vertical conduction between the two layers via the silicon side walls, without loosing generality. This can be easily included by slightly modifying Ψ, specifically by introducing new conductance terms in this matrix corresponding to vertical conduction in these silicon side walls.

Then, similar to (3), the microchannel temperature vector $\mathbf{T_C}(z)$ must be eliminated since it does not lend itself to a state-space representation (as the temperature and the heat flow in channel are directly related to each other). To do this, as in Section IV-A, we must write the heat accumulated in the channels until the distance z, $\{q_{C1}(z), q_{C2}(z)\}$, in terms of the other known and irreducible variables in the system. As before, we note that the heat accumulated in the channel includes the heat that entered at the inlet with the fluid owing to its constant inlet temperature $q_{C,in}$, the amount of input heat generated in both the tracks and in both the layers between $z = 0$ and the current location z, and finally the heat entering the region upstream to the location z from the region downstream to this location via longitudinal conduction in silicon in the respective tracks. However, in the case of multiple channels, there is also the additional component of heat exchanged between the tracks via lateral conduction in silicon, which determines the differences in the amount of heat between the two channels. This can be computed by integrating this lateral heat flow (designated as $q_{s11-12}(z)$ and $q_{s21-22}(z)$ with the default direction of flow from track 1 to track 2) from inlet to z. Hence, we can write

$$T_{Cj} = \frac{1}{c_v V}q_{Cj} = T_{C,in} + \frac{1}{c_v V}\Big[(Q_{i1j}(z) + Q_{i2j}(z)) - (q_{1j}(z) + q_{2j}(z)) - \int_0^z (q_{s11-12} + q_{s21-22})\,dz\Big] \tag{28}$$

where $j \in \{1, 2\}$. From our definition of the lateral heat flow variable, we know that

$$q_{sj1-j2}(z) = \hat{g}_s\left(T_{j1}(z) - T_{j2}(z)\right) \tag{29}$$

where $j \in \{1, 2\}$. Hence, we can introduce new state space variables corresponding to the cumulative lateral heat flow $Q_{s11-12}(z)$ and $Q_{s21-22}(z)$ and eliminate the integral terms in (28) to create the final state-space representation as follows:

$$\frac{d}{dz}Q_{si1-i2}(z) = \hat{g}_s\left(T_{i1}(z) - T_{i2}(z)\right) \tag{30}$$

where $i \in \{1, 2\}$. Now, combining (24), (26), and (30), we get

$$\frac{d}{dz} \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \\ Q_s(z) \end{bmatrix} = \begin{bmatrix} \mathbf{0} & \Lambda & \mathbf{0} \\ \Psi & \Omega & \Theta \\ \Phi & \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{T}(z) \\ \mathbf{q}(z) \\ Q_s(z) \end{bmatrix} + \begin{bmatrix} \mathbf{0} \\ \mathbf{U}(z) \\ 0 \end{bmatrix} \quad (31)$$

where

$$Q_s(z) = Q_{s11-12}(z) + Q_{s21-22}(z)$$

$$\Omega = \begin{bmatrix} -\hat{g}_v/c_v V & 0 & -\hat{g}_v/c_v V & 0 \\ 0 & -\hat{g}_v/c_v V & 0 & -\hat{g}_v/c_v V \\ -\hat{g}_v/c_v V & 0 & -\hat{g}_v/c_v V & 0 \\ 0 & -\hat{g}_v/c_v V & 0 & -\hat{g}_v/c_v V \end{bmatrix}$$

$$\Theta = \begin{bmatrix} -\hat{g}_v/c_v V \\ +\hat{g}_v/c_v V \\ -\hat{g}_v/c_v V \\ +\hat{g}_v/c_v V \end{bmatrix}, \quad \Phi = \begin{bmatrix} +\hat{g}_s \\ -\hat{g}_s \\ +\hat{g}_s \\ -\hat{g}_s \end{bmatrix}^T$$

$$\mathbf{U}(z) = \begin{bmatrix} \hat{g}_v T_{C,in} + \hat{g}_v/c_v V \left(Q_{i11}(z) + Q_{i21}(z) \right) + \hat{q}_{i11}(z) \\ \hat{g}_v T_{C,in} + \hat{g}_v/c_v V \left(Q_{i12}(z) + Q_{i22}(z) \right) + \hat{q}_{i12}(z) \\ \hat{g}_v T_{C,in} + \hat{g}_v/c_v V \left(Q_{i11}(z) + Q_{i21}(z) \right) + \hat{q}_{i21}(z) \\ \hat{g}_v T_{C,in} + \hat{g}_v/c_v V \left(Q_{i12}(z) + Q_{i22}(z) \right) + \hat{q}_{i22}(z) \end{bmatrix}. \quad (32)$$

The above derivation can be extended to the case of more than two tracks in a straightforward manner. For the case of m tracks, $\mathbf{Q_s}(z)$ would be a vector of $(m-1)$ new variables introduced to account for the cumulative lateral heat flow variables between the tracks.

F. Transient Semi-Analytical Model

The semi-analytical model developed in Section IV-A can be extended for the case of transient analysis. Transient analysis in this context entails the prediction of temperatures during a time-interval between the instant when the input heat fluxes switch to a new value until the temperatures settle down to the steady state. As described in Section II, the electrical analogy for transient thermal simulation involves a circuit that contains both resistors and capacitors (an RC circuit). In the proposed semi-analytical model, since we let 1-D in the computational domain remain continuous, this would translate to an RC circuit that contains both distributed resistances and distributed capacitances in this dimension.

This is illustrated by considering again the basic cell structure from Section IV-A. However, for the sake of simplicity and without loss of generality, we consider only one layer of silicon with active heating as shown in Fig. 9(a). Note that in this case, all the variables are a function of both distance z and time t. Here, $T(z, t)$ and $q(z, t)$ refer to the temperature and longitudinal heat flow, respectively, in the silicon junction. $T_C(z, t)$ and $q_C(z, t)$ refer to corresponding variables in the microchannel. $\hat{q}_i(z, t)$ is the known distributed input heat flux function in the silicon junction.

An infinitesimally small section of the new test structure of length Δz at distance z from the inlet, along with its equivalent electrical circuit, is shown in Fig. 9(b). Note that in this circuit, there are additional pathways for the heat flow in the form of distributed capacitances $\hat{C}_{Si} = c_{v,Si} \cdot W \cdot H_{Si}$ and $\hat{C}_C(z) =$
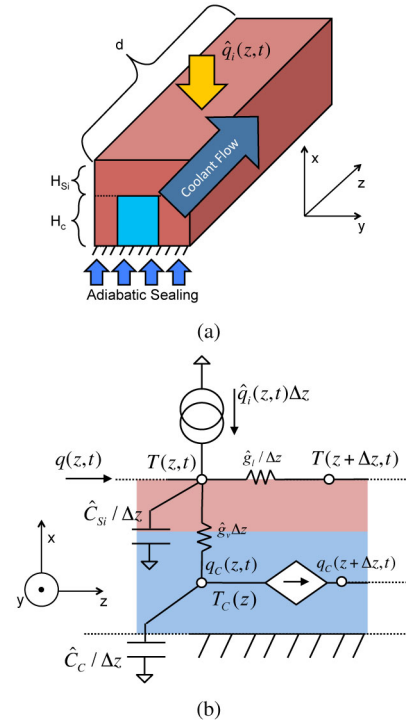

Fig. 9. (a) Test structure for transient analysis. (b) Infinitesimally small section of this test structure.

$c_{v,C} \cdot w_C(z) \cdot H_C$. The difference equations for this small section can be written as

(1) $\quad T(z + \Delta z, t) = T(z, t) - \dfrac{1}{\hat{g}_l/\Delta z} q(z, t)$

(2) $\quad q(z + \Delta z, t) = q(z, t) - [T(z, t) - T_C(z, t)] \hat{g}_v(z) \Delta z$
$$\qquad - \hat{C}_{Si} \Delta z \frac{d}{dt} T(z, t) + \hat{q}_i(z, t) \Delta z$$

(3.1) $\quad c_{v,C} \cdot V \cdot T_C(z) = q_C(z)$

(3.2) $\quad q_C(z + \Delta z) = q_C(z) - [T_C(z, t) - T(z, t)] \hat{g}_v(z) \Delta z$
$$\qquad - \hat{C}_C(z) \Delta z \frac{d}{dt} T_C(z, t). \quad (33)$$

By rearranging the above equations, substituting (33.3.1) in substituting (33.3.2), then taking the limit $\Delta z \to 0$ and finally writing $\kappa(z) = w_C(z) H_C/V$, we get

$$\frac{\partial}{\partial z} \begin{bmatrix} T(z, t) \\ q(z, t) \\ T_C(z, t) \end{bmatrix} = \mathbf{A}(z) \begin{bmatrix} T(z, t) \\ q(z, t) \\ T_C(z, t) \end{bmatrix} + \mathbf{B}(z) \frac{\partial}{\partial t} \begin{bmatrix} T(z, t) \\ q(z, t) \\ T_C(z, t) \end{bmatrix}$$
$$\qquad + \mathbf{U}(z, t) \quad (34)$$

where

$$\mathbf{A}(z) = \begin{bmatrix} 0 & -1/\hat{g}_l & 0 \\ -\hat{g}_v(z) & 0 & -\hat{g}_v(z) \\ +\hat{g}_v/c_v V & 0 & -\hat{g}_v/c_v V \end{bmatrix}$$

$$\mathbf{B}(z) = \begin{bmatrix} 0 & 0 & 0 \\ -\hat{C}_{Si} & 0 & 0 \\ 0 & 0 & -\kappa(z) \end{bmatrix}, \quad \mathbf{U}(z, t) = \begin{bmatrix} 0 \\ \hat{q}_i \\ 0 \end{bmatrix}. \quad (35)$$

The above partial differential equations can be converted to ordinary differential equations by numerically integrating the equations in time. For this, we choose the backward Euler

method with a sampling time interval h. Hence, at the nth time-point during the simulation, we can write

$$
\frac{d}{dz} \begin{bmatrix} T(z,n) \\ q(z,n) \\ T_C(z,n) \end{bmatrix} = \left(\mathbf{A}(z) + \frac{\mathbf{B}(z)}{h} \right) \begin{bmatrix} T(z,n) \\ q(z,n) \\ T_C(z,n) \end{bmatrix}
$$

$$
- \frac{\mathbf{B}(z)}{h} \begin{bmatrix} T(z,n-1) \\ q(z,n-1) \\ T_C(z,n-1) \end{bmatrix} + \mathbf{U}(z,n). \tag{36}
$$

If the values of the state variables at the previous time-point $n-1$ are known and can be considered as input variables, the above system of equations become similar in form to (4). Theoretically, a solution similar (6) can be derived for these system of equations. However, a closed-form expression for the state variables at any given time point n is extremely difficult to compute as it would require the knowledge of the cumulative state variables at the previous time-point at all points along the length of the test structure (i.e., the state variables $\{T(z,n-1), q(z,n-1), T_C(z,n-1)\}$ integrated from $z = 0$ to any other point z). This is very rarely known, even when the matrices $\mathbf{A}$ and $\mathbf{B}$ are constant matrices that are not a function of z. Hence, only numerical solutions are practically feasible for the transient simulation of the proposed semi-analytical model in (36).

V. VALIDATION RESULTS

In this section, we show the effectiveness and accuracy of the proposed model with respect to the compact thermal model, namely 3D-ICE [1]. We first start by validating the steady-state and transient models. Then, we show the trade-offs between the accuracy and speed-up between the proposed model and 3D-ICE.

A. Steady-State Model Validation

To demonstrate the validity of the proposed semi-analytical model and its closed-form solution, an example with a single track is considered, which has the same structure as in Fig. 5. We use the following values for the material and structure parameters of the individual tracks:

$$
H_{Si} = H_C = W = 100 \ \mu\text{m}, w_C = 50 \ \mu\text{m}, d = 10 \ \text{mm}
$$

$$
k_{Si} = 130 \ \text{W/m} \cdot \text{K}, k_C = 0.6 \ \text{W/m} \cdot \text{K}, c_v = 4.172 \ \text{kJ/m}^3 \cdot \text{K}
$$

$$
V = 0.48 \ \text{ml/min}, T_{C,in} = 300 \ \text{K}, h_{eff} = h\frac{w_C + 2H_C}{W},
$$

$$
h = k_f \frac{Nu}{d_h} \tag{37}
$$

where [23]

$$
Nu = 8.235 \cdot \left[1 - 2.0421\frac{w_C}{H_C} + 3.0853\left(\frac{w_C}{H_C}\right)^2 \right.
$$

$$
\left. -2.4765\left(\frac{w_C}{H_C}\right)^3 + 1.0578\left(\frac{w_C}{H_C}\right)^4 - 0.1861\left(\frac{w_C}{H_C}\right)^5 \right]. \tag{38}
$$

The nusselt number above has been derived for laminar flows in microchannels under fully developed conditions [23]. Integrated microchannels typically encounter liquid velocities of the order of 1 m/s. For microchannel cross-sectional
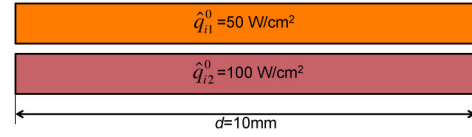

Fig. 10. Input heat flux distributions for the example in Case A.
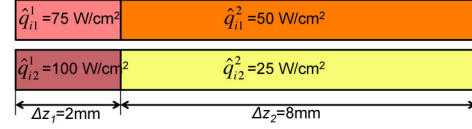

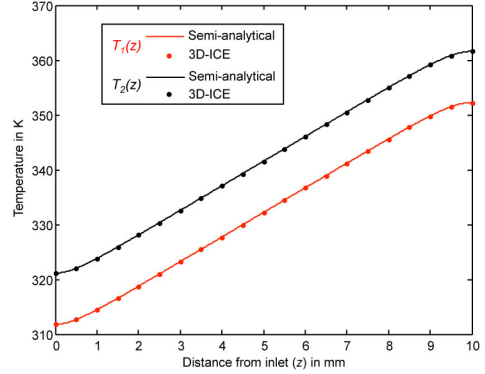Fig. 11. Input heat flux distributions for the example in Case B.

Fig. 12. Comparison of junction temperature distributions for the example of Case A: semi-analytical model versus 3D-ICE.

TABLE I
SAMPLE TEMPERATURE RESULTS AND MAXIMUM ERROR WITH RESPECT TO 3D-ICE FOR CASE A IN SECTION IV-D

Result	Semi-analytical model	3D-ICE
$T_1(0)$	311.7603K	311.7602K
$T_2(0)$	321.1219K	321.1218K
$T_1(d)$	352.2483K	352.2484K
$T_2(d)$	361.6098K	361.6099K
max. error	0.000123K	
max. error percentage	0.00023%	

dimensions of a few 10 s or 100 s of micrometers, this translates to Reynolds numbers of the order of 200–800 resulting in an extremely stable laminar flow justifying the assumption of such conditions for the proposed model [9].

First consider solution for the uniform heat flux distribution considered in Section IV-D (Case A). The heat flux distributions on both layers are uniform and are set to 50 W/cm² and 100 W/cm², respectively, as shown in Fig. 10. The semi-analytical model for this example was constructed and solved using (14) and the junction temperature distributions $\{T_1(z), T_2(z)\}$ were computed. The problem was also solved using 3D-ICE [1] and the corresponding junction temperatures were also computed. The problem size in the 3D-ICE model (number of nodes) was 3003. The comparison of the temperature plots is shown in Fig. 12. The maximum difference in temperatures between the two methodologies was 0.00023% (measured with respect to the temperature deviation from the initial state of 300 K). The results are tabulated in Table I.

The closed-form solution for the nonuniform heat flux distribution (Case B) can also be validated in a similar way. Therefore, we consider an example similar to the one used
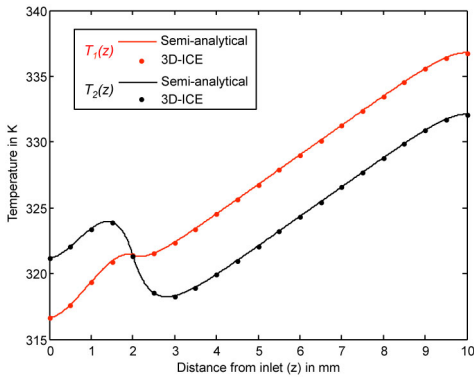
Fig. 13. Comparison of junction temperature distributions for the example in Case B: semi-analytical model versus 3D-ICE.

TABLE II
SAMPLE TEMPERATURE RESULTS AND MAXIMUM ERROR WITH RESPECT TO 3D-ICE FOR CASE B IN SECTION IV-D

Result	Semi-analytical model	3D-ICE
$T_1(0)$	316.6635K	316.6617K
$T_2(0)$	321.1818K	321.1784K
$T_1(d)$	336.7963K	336.7814K
$T_2(d)$	332.1156K	332.1006K
max. error	0.0791K	
max. error percentage	0.3711%	

TABLE III
SAMPLE TEMPERATURE RESULTS AND MAXIMUM ERROR WITH RESPECT TO 3D-ICE FOR THE EXAMPLE IN SECTION IV-E

Result	Semi-analytical model	3D-ICE
$T_{11}(0)$	311.4981K	311.4985K
$T_{12}(0)$	311.3096K	311.3100K
$T_{21}(0)$	315.9758K	315.9741K
$T_{22}(0)$	315.7873K	315.7856K
$T_{11}(d)$	343.6839K	343.6806K
$T_{12}(d)$	343.8364K	343.8332K
$T_{21}(d)$	336.7099K	336.7066K
$T_{21}(d)$	336.7682K	336.7649K
max. error	0.0474K	
max. error percentage	0.2697%	

for Case A. The only difference is the distribution of the heat flux as shown in Fig. 11. Here, there are two regions in both the layers with different heat fluxes. The temperature distributions resulting from these input heat fluxes using both methods, namely, the closed-form solution to the proposed semi-analytical model in (22) and 3D-ICE, are compared in Fig. 13. The maximum difference between temperatures obtained using the two methods in this case was 0.37%. The results are shown in Table II.

As explained in Section IV-D, even though closed-form solutions exist for the proposed semi-analytical model under certain circumstances, it is more practical to use numerical solvers to compute the temperatures in thermal-aware design problems. Hence, an experiment is performed where the proposed semi-analytical model is solved using a numerical solver and then compared against 3D-ICE. For this, consider the case of two tracks of microchannels as shown in Fig. 8 (described in Section IV-E). The material and structural parameters are the same as those given above for the single track case. The heat flux distributions assumed in this case are shown in Fig. 14. The state-space form of the semi-analytical model in (4) lends itself to easy implementation in popular numerical differential equation
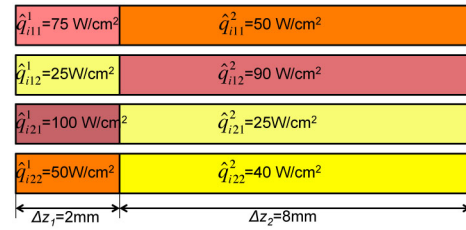

Fig. 14. Input heat flux distributions for the example in Section IV-E.
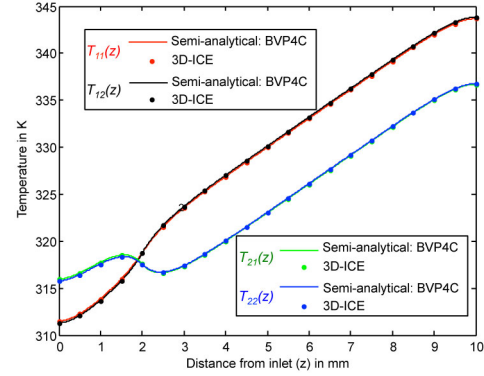

Fig. 15. Comparison of junction temperature distributions for the example in Section IV-E: semi-analytical model (solved using BVP4C [25]) versus 3D-ICE.

solvers. As described in Section IV-B, since the semi-analytical model represents a boundary value problem with the heat flows known to be zero at $z = 0$ and $z = d$ (the adiabatic conditions at the terminals of the structure), boundary value problem solvers, such as the BVP4C package in MATLAB [25], can be used to obtain quick solutions to the temperature distributions for a wide variety of scenarios. The corresponding comparison of temperatures obtained by solving the proposed semi-analytical model in (31) using the BVP4C solver and those obtained from 3D-ICE (problem size 6006) are plotted in Fig. 15. The maximum temperature difference measured in this case was 0.27%. The results are shown in Table III.

B. Transient Model Validation

In addition to the steady-state model validation, the transient thermal model is validated by comparison with 3D-ICE. A case of uniform input heat flux switching between 25 and 50 W/cm² during a 50 ms time interval is applied to the test structure in Fig. 9, with the parameters mentioned before in Section V-A. The total simulation time interval is 50 ms long and the input heat flux starts switching 10 ms after the simulation begins. The proposed semi-analytical model (36) with a time-step of 1 ms was solved using the BVP4C solver, and the transient temperature results were compared with the results from 3D-ICE. Sample comparison of the temperature waveforms obtained from the middle of the junction ($T(z = 5mm, t)$) is plotted in Fig. 16. The maximum difference in the temperatures obtained at this location for all time points, with respect to the maximum temperature deviation from the initial conditions (300 K) was 0.0024%.

C. MPSoC Simulation Validation

After the validation using rather simplistic case-studies, we extend the validation of the proposed model against 3D-ICE by
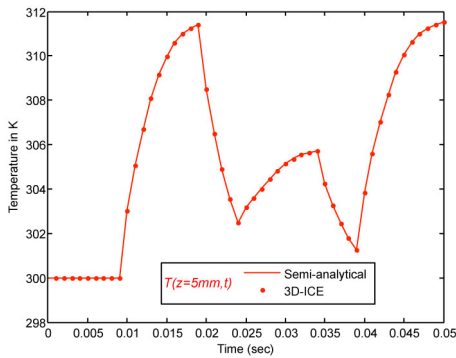
Fig. 16. Comparison of transient temperature waveforms: semi-analytical model (solved using BVP4C) versus 3D-ICE.
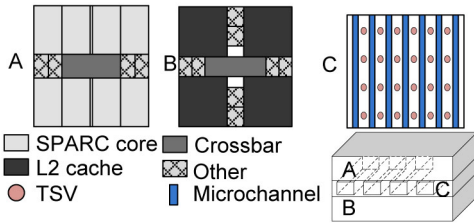

Fig. 17. Schematic diagram of the UltraSPARC T1-based 3-D MPSoC used in this validation [24].

performing steady-state simulations on a complete two-layered 3-D MPSoC with interlayer liquid cooling. The simulated 3-D MPSoC is based on UltraSPARC T1 Niagara MPSoC [26], and the 3-D MPSoC structure adopted in this simulation has been used in several works [1], [11], [24]. Fig. 17 shows the schematic diagram of the targeted 3-D MPSoC. More details on the power figures of this architecture can be found in [26]. All the floorplan elements of this 3-D MPSoC are assumed to be functioning at 100% activity dissipating the maximum possible power. There are 100 microchannels in the channel layer, each of width 100 μm and a pitch of 100 μm. The flow rate of the water coolant through the microchannel cavity is 48 ml/min.

In this validation, we compare between the two models (i.e., proposed and 3D-ICE) by using the following criteria: while the proposed model is continuous in the fluid flow direction, it is discrete in the directions normal to the fluid flow. In this respect, we vary the discretization size in several cases. In each case, we group the microchannels and derive the equivalent cavity media, power consumption, and heat transfer parameters. For the targeted case we split the 100 channels by the following factors {4, 8, 16, 32, 64}. The exact same splits are used in the 3D-ICE splits, in addition to the discretization along the microchannel by using a cell length of 10 μm. We plot the thermal map generated by the proposed model of both layers in Fig. 18.

Fig. 19 shows the simulation time and the error percentage difference between the proposed model and 3D-ICE. From this figure, we can deduce that the proposed model achieves high accuracy, with only 0.18% (or 0.051 K) maximum error, with respect to 3D-ICE. These small errors are due to the fact that the models built in 3D-ICE and the proposed semi-analytical approach are similar in terms of their lateral discretizations and the assumptions of neglecting vertical conduction via microchannel walls. This error does not increase much with
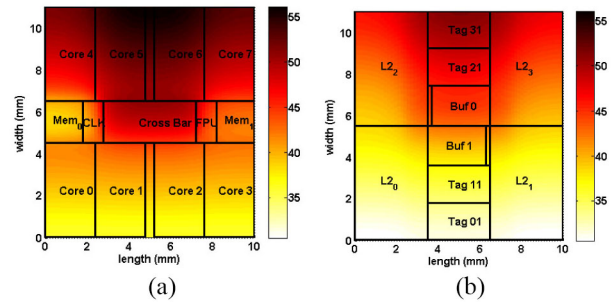

Fig. 18. Temperature maps of the two-die UltraSPARC T1 (Niagara) 3-D MPSoC simulated using the proposed semi-analytical model. (a) Core layer. (b) Cache-memory layer. All temperatures in ^oC.

even finer problem definition. For example, when the 3D-ICE representation is discretized at a much finer level, the error increases to about 2%. The errors for transient simulations also show similar behavior.

D. Observations on Model Performance and Efficacy

Fig. 19 also shows that the proposed model achieves better speedup figures compared to 3D-ICE, with values up to 3X in the illustrated case study. This is mainly caused by treating the heat dissipation along the channel as a continuous domain. By this treatment, no numerical approximations are needed in this direction, hence reducing the formulated thermal problem size. However, it is important to mention that this speed up can be recovered by increasing the cell size. If the cell size is changed from 10 μm to 100 μm, 3D-ICE-based thermal simulation is 50% faster than the proposed model. The claimed speedup (3X) comes at the cost of increased complexity in the solving methodology.

The limitations of the proposed semi-analytical model can be summarized as follows.

1) The proposed model is faster than fully numerical models such as 3D-ICE only when such models are used with very fine discretization as described above.
2) The proposed semi-analytical model requires extensive derivations and preprocessing as is clear from the preceding sections. The derivations of the model and their closed-form solutions become even more complex, when the heterogeneity of the structural and materials (e.g., additional layers, TSVs, conduction via microchannel walls, etc.) in a real 3-D IC are included, since that would imply that the conduction elements of the A matrix in (8) become functions of the distance making the evaluation of matrix exponentials and integrals nontrivial. Including such design complexities in fully numerical models such as 3D-ICE is very straightforward as the parameters only the corresponding discretization units or thermal cells would need to be changed.
3) Moreover, every time any of these design features are changed, this preprocessing must be repeated. Again, note that including these aspects in a purely numerical model like 3D-ICE is very straightforward.

In light of the above limitations, it is clear that extensive thermal simulations for conventional design-space exploration is not the best use of the proposed semi-analytical model when compared to conventional numerical simulators; even though,
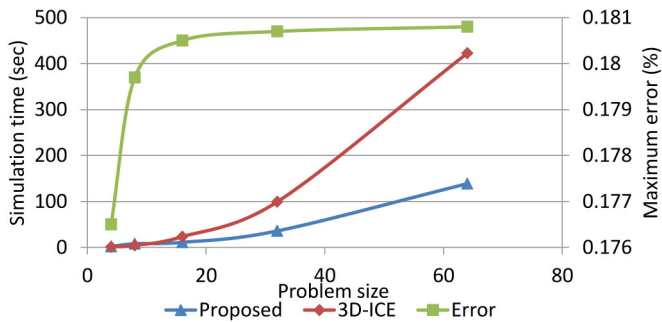
Fig. 19. Thermal simulation time of the proposed semi-analytical model and 3D-ICE, as well as the maximum error percentage between the proposed model and 3D-ICE for different problem sizes.

the proposed semi-analytical model provides a very compact and elegant mathematical representation of heat transfer in a liquid-cooled 3-D MPSoC. Instead, the primary application for this semi-analytical model is in the early-stage optimized design of liquid-cooled ICs as described in the ensuing sections.

VI. APPLICATIONS OF THE PROPOSED SEMI-ANALYTICAL MODEL: THERMAL GRADIENT MINIMIZATION AND ENERGY EFFICIENCY MAXIMIZATION

The state-space form of the semi-analytical model derived in the previous section aids in rapid temperature-aware design-space exploration and optimization of liquid-cooled 3-D-ICs. We briefly present an application that we have implemented based on this model in the ensuing subsections. This application provides different ways of performing channel width modulation, i.e., designing an optimal microchannel width function that can be fabricated on an IC, in order to minimize a specific design cost while respecting other design constraints. In order to accomplish this, optimal control techniques are utilized and combined with the proposed semi-analytical model. By combining these techniques, significant speed-ups are obtained in finding the optimal solution when compared to other thermal simulation frameworks. More detailed information about these novel design algorithms can be found in [11] and [12].

A major challenge in the robust design of ICs is the large thermal gradients that exist on the IC junction (see Section II-B) in a very small area. In liquid-cooled ICs, these thermal gradients arise out of both nonuniform heat flux signatures of multicore processors [26], and the accumulation of heat by the coolant as it flow from inlet to outlet producing a nonuniform cooling of the IC surface [11]. Large thermal gradients can undermine the reliability and lifetime of an IC [27].

This problem can be overcome by carefully designing microchannel heat sinks. Specifically, the cross-sectional aspect ratio $(w_C(z)/H_C)$ of a channel can be fine-tuned at various points along the channel to change local cooling efficiencies. The relationship between convective resistance and local channel width (for a constant channel height) is illustrated in Fig. 20 [23]. Hence, microchannel widths can be modulated in an IC to create more uniform temperatures. However, care must be taken to not exceed design considerations such as minimum spacings for TSVs and maximum pressure drops in the channels. In order to accomplish this, the theory of optimal control [28] was applied to the semi-analytical model in (4) to
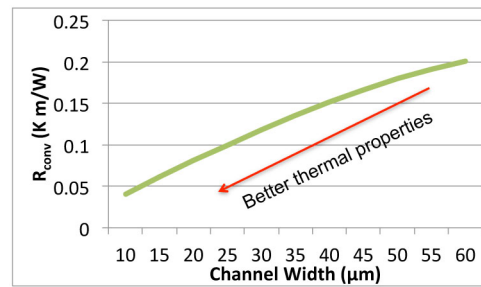

Fig. 20. Convective resistance (inverse of the conductance) versus channel width for a fixed channel height under fully-developed conditions [23].
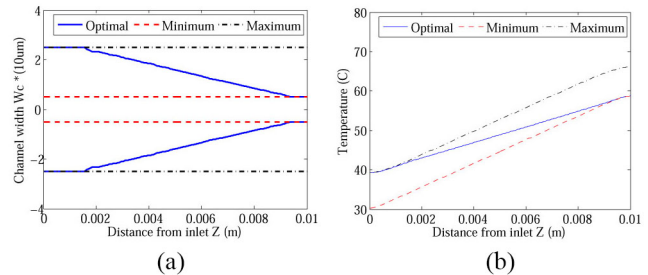

Fig. 21. (a) Channel width function and (b) corresponding temperature distributions obtained using the optimal design algorithm based on channel width modulation. Comparisons against the results from using the minimum- and the maximum-possible uniform channel widths are also shown [11].

find the optimal channel width profile $w_C(z)$ such that thermal gradients in an IC are minimized. Experiments were performed for different test cases with both uniform and nonuniform input heat fluxes. Numerical results confirmed that in comparison to uniformly narrow and wide channels, optimally modulated channels can produce lower—in fact theoretically minimum—thermal gradients in an IC. The results shown for a uniform input heat flux can be seen in Fig. 21 [11].

Note that the mentioned results [11] have been possible using the optimal control theory with relatively small execution time solely because of the state-space form of the proposed semi-analytical model that provides a very concise representation of all the useful variables in the system. To illustrate the effectiveness of our model in reducing the execution time, we run the simulation using both 3D-ICE and the proposed models. Since the optimization algorithm complexity is $O(N^2)$ [28], the optimal control problem achieves the intended solution at least 9X faster compared to deploying 3D-ICE to the optimization loop.

The optimal control-based design of microchannels described above has been modified for another application, namely, to improve the energy efficiency of the cooling systems in a microprocessor [12]. For this, the definition of the cost function was changed to the pumping energy consumed by the coolant inside the microchannel. This application, called GREENCOOL reduces the coolant pumping energy cost up to 80% when compared to conventional straight channels. More details about this application can be found in [12].

VII. CONCLUSION

A new semi-analytical model for forced convective cooling in microchannels has been presented. The proposed semi-analytical model has a transmission line-like structure and

provides concise state-space representation for heat transfer in liquid-cooled microchannels. This new representation can be used in the design and evaluation of advanced liquid-cooled heat sinks for ICs. Both steady-state as well as transient models have been presented for single- or parallel- multiple microchannel cooling systems. Closed-form solutions for the model have been derived for specific cases, while numerical solutions can be used for all other cases. Examples demonstrating the accuracy of the model have been presented for each case. Finally, two applications of the model, which are of practical interest in thermal engineering of ICs, have been discussed.

REFERENCES

[1] A. Sridhar, A. Vincenzi, M. Ruggiero, T. Brunschwiler, and D. Atienza, "3D-ICE: Fast compact transient thermal modeling for 3D ICs with inter-tier liquid cooling," in *Proc. ICCAD*, San Jose, CA, USA, 2010, pp. 463–470.

[2] B. Agostini *et al.*, "State of the art of high heat flux cooling technologies," *Heat Transfer Eng.*, vol. 28, no. 4, pp. 258–281, 2007.

[3] D. B. Tuckerman and R. F. W. Pease, "High-performance heat sinking for VLSI," *IEEE Electron Device Lett.*, vol. 2, no. 5, pp. 126–129, May 1981.

[4] T. Brunschwiler *et al.*, "Interlayer cooling potential in vertically integrated packages," *Microsyst. Technol.*, vol. 15, no. 1, pp. 57–74, 2009.

[5] S. Zimmermann *et al.*, "Aquasar: A hot water cooled data center with direct energy reuse," *Energy*, vol. 43, no. 1, pp. 237–245, 2012.

[6] T. Brunschwiler, B. Smith, E. Ruetsche, and B. Michel, "Toward zero-emission data centers through direct reuse of thermal energy," *IBM J. Res. Develop.*, vol. 53, pp. 11:1–11:13, May 2009.

[7] F. Alfieri *et al.*, "3D integrated water cooling of a composite multilayer stack of chips," *J. Heat Transfer*, vol. 132, no. 12, p. 121402, Sep. 2010.

[8] B. Dang, M. Bakir, D. Sekar, C. King, and J. Meindl, "Integrated microfluidic cooling and interconnects for 2D and 3D chips," *IEEE Trans. Advanced Packag.*, vol. 33, no. 1, pp. 79–87, Feb. 2010.

[9] T. Brunschwiler *et al.*, "Heat-removal performance scaling of interlayer cooled chip stacks," in *Proc. IEEE 12th ITherm*, Las Vegas, NV, USA, Jun. 2010, pp. 1–12.

[10] H. Mizunuma *et al.*, "Thermal modeling and analysis for 3-D ICs with integrated microchannel cooling," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 9, pp. 1293–1306, Sep. 2011.

[11] M. M. Sabry, A. Sridhar, and D. Atienza, "Thermal balancing of liquid-cooled 3D-MPSoCs using channel modulation," in *Proc. DATE*, Dresden, Germany, 2012.

[12] M. M. Sabry, A. Sridhar, J. Meng, A. Coskun, and D. Atienza, "GreenCool: An energy-efficient liquid cooling design technique for 3-D MPSoCs via channel width modulation," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 32, no. 4, pp. 524–537, Apr. 2013.

[13] W. Huang *et al.*, "Hotspot: A compact thermal modeling methodology for early-stage VLSI design," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 5, pp. 501–513, May 2006.

[14] F. Incropera, D. Dewitt, T. Bergman, and A. Lavine, *Fundamentals of Heat and Mass Transfer*. New York, NY, USA: Wiley, 2007.

[15] M. N. Ozisik, *Finite Difference Methods in Heat Transfer*. Boca Raton, FL, USA: CRC Press, 1994.

[16] *ANSYS CFX* [Online]. Available: http://www.ansys.com/products/fluid-dynamics/cfx/

[17] J. Sucec, "Exact solution for unsteady conjugated heat transfer in the thermal entrance region of a duct," *J. Heat Transfer*, vol. 109, no. 2, pp. 295–299, 1987.

[18] W. Khan and M. Yovanovich, "Analytical modeling of fluid flow and heat transfer in microchannel/nanochannel heat sinks," *J. Thermophys. Heat Transfer*, vol. 22, no. 3, pp. 352–359, 2008.

[19] S. Shahsavari, A. Tamayol, E. Kjeang, and M. Bahrami, "Convective heat transfer in microchannels of noncircular cross sections: An analytical approach," *J. Heat Transfer*, vol. 134, no. 9, p. 091701, Jun. 2012.

[20] A. Sridhar, A. Vincenzi, M. Ruggiero, T. Brunschwiler, and D. Atienza, "Compact transient thermal model for 3D ICs with liquid cooling via enhanced heat transfer cavity geometries," in *Proc. THERMINIC*, Barcelona, Spain, 2010, pp. 1–6.

[21] A. Sridhar *et al. 3D-ICE* [Online]. Available: http://esl.epfl.ch/3D-ICE

[22] C. Paul, *Analysis of Multiconductor Transmission Lines*. New York, NY, USA: Wiley, 1994.

[23] R. Shah and A. London, *Laminar Flow Forced Convection in Ducts*. New York, NY, USA: Academic Press, 1978.

[24] M. M. Sabry *et al.*, "Energy-efficient multi-objective thermal control for liquid-cooled 3D stacked architectures," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 12, pp. 1883–1896, Dec. 2011.

[25] *BVP4C MATLAB Solver* [Online]. Available: http://www.mathworks.com/help/matlab/ref/bvp4c.html

[26] A. Leon *et al.*, "A power-efficient high-throughput 32-thread SPARC processor," *ISSCC*, vol. 42, no. 1, pp. 7–16, 2007.

[27] C. J. Lasance, "Thermally driven reliability issues in microelectronic systems: Status-quo and challenges," *Microelectron. Rel.*, vol. 43, pp. 1969–1974, Dec. 2003.

[28] K. L. Teo *et al.*, *A Unified Computational Approach to Optimal Control Problems*. England, U.K.: Longman Scientific and Technical, 1991.

Arvind Sridhar (M'07) received the Ph.D. degree in electrical engineering from École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, 2013.

He is currently a Post-Doctoral Researcher with IBM Research, Zurich. He has authored 3D-ICE, the first compact transient thermal simulator for 2-D/3-D ICs with liquid cooling, which is currently being used by researchers in over 200 universities and laboratories worldwide.

Mohamed M. Sabry (M'12) received the M.Sc. and Ph.D. degrees in electrical and computer engineering from Ain Shams University, Cairo Governorate, Egypt, and from École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, in 2008 and 2013, respectively.

He is currently a postdoctoral research fellow at Stanford University and a visiting scholar in the Embedded Systems Lab, EPFL. His current research interests include system design and resource management methodologies in embedded systems, and multiprocessor system-on-chips (MPSoCs), especially temperature and reliability management of 2-D and 3-D MPSoCs, with particular emphasis on emerging computational and cooling technologies.

Dr. Sabry was the recipient of the Swiss National Science Foundation Early Post-Doctoral Mobility Fellowship in 2013.

David Atienza (M'05–SM'13) received his MSc and PhD degrees in computer science and engineering from UCM, Spain, and IMEC, Belgium, in 2001 and 2005, respectively. He is currently an Associate Professor of Electrical Engineering and Director of the Embedded Systems Laboratory at École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland. His current research interests include system-level design methodologies for high-performance multiprocessor system-on-chip (MPSoC) and low-power embedded systems, including new 2-D/3-D thermal-aware design for MPSoCs, ultralow power system architectures for wireless body sensor nodes, HW/SW reconfigurable systems, dynamic memory optimizations, and network-on-chip design. He has co-authored over 200 publications in peer-reviewed international journals and conferences, several book chapters, and eight U.S. patents in these fields.

Dr. Atienza was the recipient of the IEEE Council on Electronic Design Automation (IEEE CASS) Early Career Award in 2013, the ACM SIGDA Outstanding New Faculty Award in 2012, and the Faculty Award from Sun Labs at Oracle in 2011. He is currently a Distinguished Lecturer of the IEEE CASS. He was also the recipient of the two Best Paper Awards at the IEEE/IFIP VLSI-SoC 2009 and CST-HPCS 2012 conference, and five Best Paper Award nominations at the DAC 2013, DATE 2013, WEHA-HPCS 2010, ICCAD 2006, and DAC 2004 conferences. He serves/served as an Associate Editor of the IEEE TRANSACTIONS ON COMPUTERS PUBLICATION, the IEEE DESIGN AND TEST OF COMPUTERS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, and Elsevier *Integration*.