Design of an Amplifier for Sensor Interfaces

Master Thesis

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Acknowledgments

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Abstract

Sensors are ubiquitous these days, employed to measure a plethora of variables in a multitude of applications. In addition to the sensor, a typical measurement system consists of electronics to perform signal conditioning and data processing which imposes demanding requirements on the electronic interface between the sensor and the processing system. Because the sensors produce low-level signals, pre-amplification of the signals is necessary for further conditioning and processing. Amplifiers thus play an important role in sensor interfaces.

The aim of this project is to design a high-gain, low noise, high PSRR, low-power op-amp for use as a universal pre-amplifier in a generic sensor interface.

This thesis presents the design of a two stage op-amp with 143 dB gain, 8 MHz GBW, 15 nV/$\sqrt{Hz}$ input referred noise consuming 630 μW which can also work in a low-power low-speed mode over a decade range of bias currents. The circuit utilizes a regulated current source load in the first stage to provide gain boosting. The design of the current source load as well as the full op-amp is based on a design methodology which was developed through the course of the project by analyzing the current source and its impact on the gain and stability of the complete amplifier.

Chapter 1

Introduction

1.1 Motivation

Sensors are all around us, employed in a multitude of applications like healthcare monitoring, weather and environment monitoring, agricultural sensing, automobiles, structural monitoring of buildings and many more. Science, engineering, medicine, even economics and commerce, depend on the measurement of a plethora of variables measured by sensors. Past and ongoing research has yielded various types of sensor technologies including resistive, capacitive and inductive sensors, Hall sensors, thermoelectric, photovoltaic and electrochemical sensors, piezoelectric sensors, CCD (charge coupled devices) sensors etc.

A sensor is almost always a part of a measurement system consisting of one or more sensors, electronics to perform signal conditioning and a subsystem to display, transmit, process or store the recorded data. Most often the electronic interface between the sensor and the processing system has demanding requirements on speed, noise, power consumption etc. This is because most of the sensors produce low-level signals which necessitate pre-amplification for further conditioning and processing (which is done mostly in the digital domain). Amplifiers thus play an important role in sensor interfaces.

To meet the requirements on noise, offset, CMRR (common mode rejection ratio) etc. for a pre-amplifier for sensor interfaces several design approaches are possible. The amplifier can be designed as a sampled data system (switched-capacitor system) including *autozeroing* or *correlated double sampling*. However, sampled data systems suffer from clock coupling putting additional constraint on PSRR (power supply rejection ratio), noise folding

and higher noise floor due to thermal noise of resistors. Hence, a continuous time voltage amplifier is suitable to achieve the design requirements for sensor interfaces.

1.2 About This Work

The aim of this project is to design a high-gain, low noise, high PSRR, low-power op-amp for use as a universal pre-amplifier in a generic sensor interface. To be used for generic applications, the amplifier has to be able to work with acceptable performance over a range of at least one decade of current consumption. To this end, multiple candidate circuit architectures were analyzed with an aim to pursue the design of the most suitable one. After choosing the appropriate architecture with the help of theoretical analyses and preliminary simulations, a schematic approach was developed to design the circuit. A design methodology was chalked out and put into action by designing a complete op-amp based on it. This methodology is an important milestone of this project as it gives a step-by-step design procedure to design similar op-amps given a set of specifications. The circuit design was validated with simulations which confirmed that the design goals were met.

1.3 Organization of the thesis

Analog circuit design is an iterative process; to present it in a linear chapter-by-chapter report is not always easy. Still, the work is presented following a conventional circuit design approach starting from the study of the architecture, analyzing the topology to have an intuitive idea of its anticipated behavior followed by actual circuit design and simulation to verify the analysis and design and, ending with the layout of the final circuit.

Chapter 2 gives a background on amplifier by talking about the design of classical miller amplifier emphasizing stability and compensation.

Chapter 3 gives an overview of the state-of-the art in amplifiers for sensor interfaces in both academia and industry.

Chapter 4 starts by listing the initial targeted design specifications for the op-amp to be designed as the goal of the project. A brief overview of the alternative architectures considered for implementation is given followed by a detailed analyses of the regulated current source load which was finally selected for implementation. The design equations for the circuit including conditions for stability are developed.

Chapter 5 lists all the important design equations governing the design of the two-stage op-amp utilizing the regulated current source load. Then, a step-by-step design methodology is developed for the op-amp design which is an important milestone of the project.

Chapter 6 shows the results of the design methodology being put into action. Transistor sizes and results of simulations performed on the final circuit are presented in this chapter.

Chapter 7 shows the final layout of the circuit. This chapter also presents a short discussion about the choice of capacitor type (PIP vs. MOS) that had to be made at the layout stage.

Chapter 8 summarizes the work done and the results achieved.

Appendix A contains the detailed analyses of the alternative architecture as discussed in chapter 4- the cross coupled current mirror- that was analyzed in addition to the regulated current source.

Appendix B presents the detailed step-by-step design calculations for the two-stage op-amp whose summary and results are presented in chapter 6.

Chapter 2

Miller Amplifier Design

2.1 The Operational Amplifier

Operational Amplifier (op-amps) are one of the most versatile analog buildings blocks. They are an integral part of many analog systems. An op-amp can be loosely defined as a "high gain differential amplifier" [1]. Op-amps are typically used in feedback loops and are required to have high gain so that the closed loop gain of the feedback system is practically independent of the op-amp gain. This can be illustrated by considering the negative feedback system shown in Fig.2.1. The overall gain of the system can be easily calculated as:

$$A = \frac{a}{1 + af} \tag{2.1}$$

For af much larger than unity,

$$A \approx \frac{1}{f} \tag{2.2}$$

Moreover, the differential change in A caused by a differential change in a

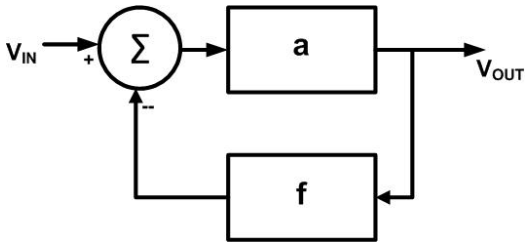

Figure 2.1: Block diagram of a negative feedback system

is given as:

$$\frac{dA}{da} = \frac{d}{da}\left(\frac{a}{1+af}\right) \tag{2.3}$$

$$\frac{dA}{A} = \frac{da}{a}\left(\frac{1}{1+af}\right) \tag{2.4}$$

Here, we observe that the fractional change in A is equal to the fractional change in a attenuated by a factor of $1+af$. Thus, if af is much larger than unity, the feedback system is desensitized to the change in the the amplifier gain a. In typical systems, the gain a would be provided by an op-amp and the feedback gain f would be provided by a passive network and is more precise. Hence, op-amps are designed to have high gains.

A single stage is generally not enough to achieve sufficiently high open-loop gain. Consequently, two or more gain stages are used to that effect. Whereas a single stage op-amp is essentially a single-pole system, a multi-stage amplifier is a multi-pole system which causes the problem of instability and needs to be compensated. This is discussed in next section.

2.2 Stability and Compensation

Consider again the negative feedback system shown in Fig.2.1. Rewriting the transfer function as a function of complex frequency s,

$$A(s) = \frac{a(s)}{1+a(s)f(s)} \tag{2.5}$$

we observe that if $a(s=j\omega_0).f(s=j\omega_0) = -1$ then the gain goes to infinity at frequency ω_0 and the system may start to oscillate. In this scenario, the negative feedback becomes positive and the gain is sufficient to sustain the oscillations. In other words, the feedback contributes 180° of phase shift thus making the total phase shift around the loop 360°. This can be expressed mathematically in the following equations known as Barkhausen Criteria:

$$|a(j\omega_0).f(j\omega_0)| = 1 \tag{2.6a}$$

$$\angle a(j\omega_0).f(j\omega_0) = -180^\circ \tag{2.6b}$$

To avoid instability, the phase shift of the forward amplifier should be minimized so that at unity gain, i.e. $|af| = 1$, $\angle af$ is greater than -180°. The difference of the phase at unity gain from -180° is called the *phase margin* of the amplifier and is a measure of the stability of the system.

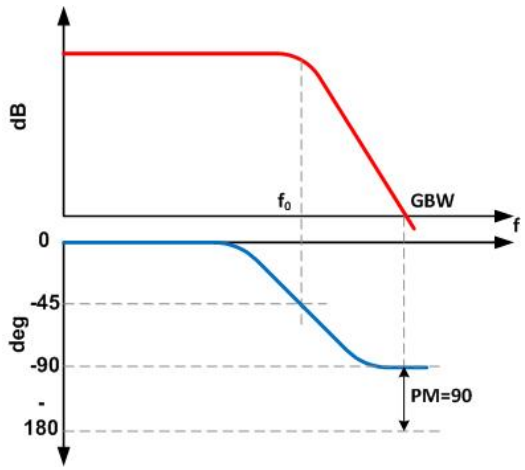

Figure 2.2: Frequency response of a typical single pole system

A single stage op-amp is a single pole system that allows the exchange of gain with bandwidth within a specific GBW (gain bandwidth product) [2]. A single pole contributes a maximum of $-90°$ phase shift, i.e. the phase margin is more than 90°, as shown in Fig.2.2. Thus, a single pole system is unconditionally stable. For a two pole system (like the two stage op-amp) the story is different. As shown in Fig.2.3, each pole causes a phase shift of $-90°$. Hence, at higher frequencies the phase margin can go to 0. To overcome this the system needs to be compensated, with the objective to shift the second pole (called the non-dominant pole) to a much higher frequency such that its phase contribution at unity-gain frequency is minimized. Results from control-theory suggest that if the non-dominant pole lies at about 3 times the GBW, the system is adequately compensated. This is illustrated in Fig.2.4. On shifting the non-dominant pole p_2 to 3*GBW provides a phase margin of 70°.

Miller Compensation A well known compensation method is the *Miller compensation* method. To compensate a two stage op-amp by Miller technique, a capacitance (known as compensation capacitance) is connected between the output of the first stage and the input of the second stage. Fig.2.5 shows the small signal diagram of a generic two-stage op-amp. g_{mI} and g_{mII} represent the transconductances of the two stages and R_I, C_I, R_{II}, C_{II} represent the equivalent output resistance and capacitance, respectively, of the two stages. The capacitor C_c is the compensation capacitor. The transfer

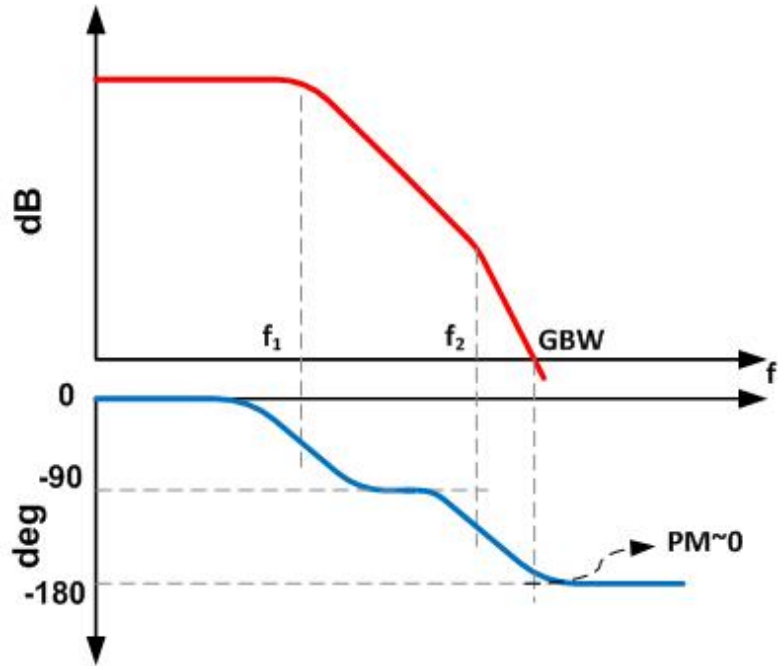

Figure 2.3: Frequency response of a typical two pole system

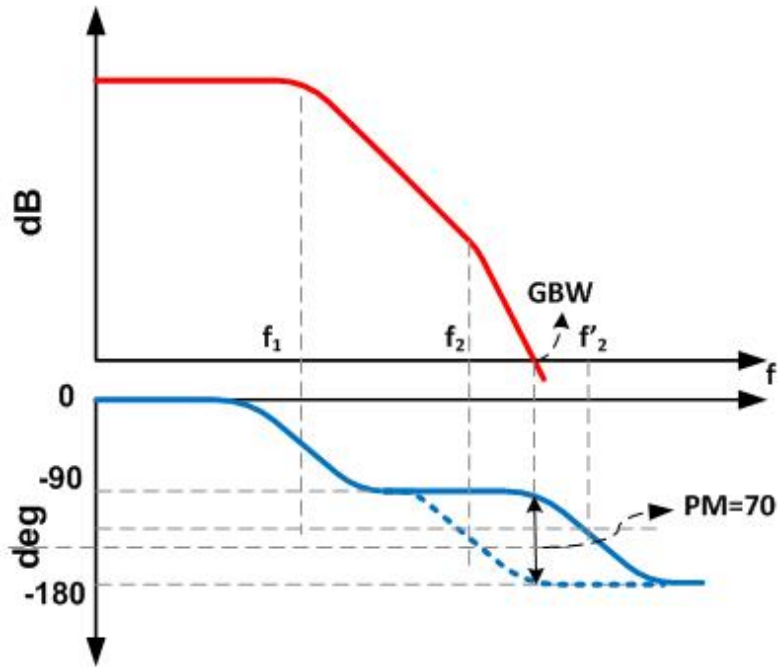

Figure 2.4: Frequency response of a compensated two pole system

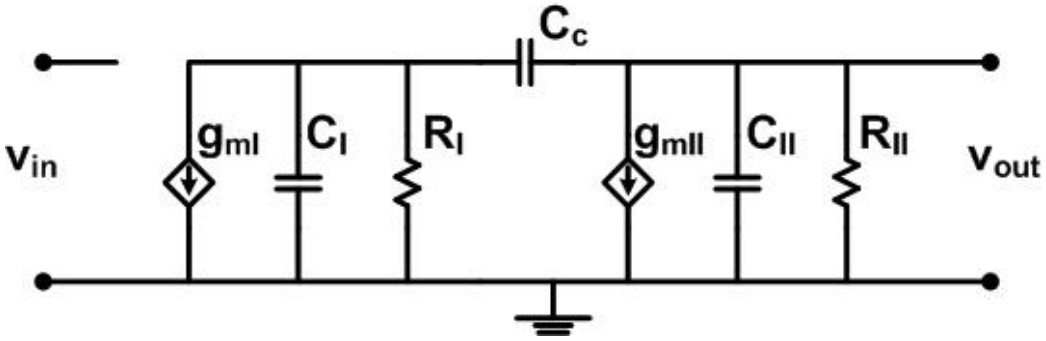

Figure 2.5: Small signal diagram of a generic two-stage op-amp

function $vout/vin$ of the circuit is given as :

$$\frac{g_{mI}g_{mII}R_IR_{II}(1-sC_c/g_{mII})}{1+s[R_I(C_I+C_c)+R_{II}(C_{II}+C_c)+g_{mII}R_IR_{II}C_c]+s^2R_IR_{II}[C_IC_{II}+C_cC_I+C_cC_{II}]} \tag{2.7}$$

A second order polynomial P(s) can be written as

$$\begin{aligned} P(s) &= 1+as+bs^2 \\ &= 1-s\left(\frac{1}{p_1}+\frac{1}{p_2}\right)+\frac{s^2}{p_1p_2} \end{aligned} \tag{2.8}$$

Assuming $p_2 >> p_1$,

$$P(s) \cong 1-\frac{s}{p_1}+\frac{s^2}{p_1p_2} \tag{2.9}$$

Therefore,

$$p_1 = \frac{-1}{a} \tag{2.10a}$$

$$p_2 = \frac{-a}{b} \tag{2.10b}$$

Comparing, (2.7) and (2.10) and assuming the two poles of the two-stage amplifier are widely spaced, we get the following compensated poles:

$$p_1 \cong \frac{-1}{g_{mII}R_IR_{II}C_c} \tag{2.11a}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_IC_{II}+C_{II}C_c+C_IC_c} \tag{2.11b}$$

Generally, C_{II} is greater than C_I and C_c, then

$$p_2 \cong \frac{-g_{mII}}{C_{II}} \tag{2.12}$$

Thus, we see that compensation by the compensation capacitor C_c causes the movement of poles away from their uncompensated values of $p_1 = \frac{1}{R_I C_I}$ and $p_2 = \frac{1}{R_{II} C_{II}}$ which were close together.

The gain of the two-stage amplifier is

$$G = g_{mI} R_I . g_{mII} R_{II} \tag{2.13}$$

Thus, the gain bandwidth product, GBW is

$$GBW = G.p_1 = \frac{g_{mI}}{C_c} \tag{2.14}$$

As stated earlier, stability requirements dictate that the non-dominant pole $p_2 \geq 3 * GBW$, so from (2.12) and (2.14) we get

$$\frac{g_{mII}}{g_{mI}} \geq 3 \frac{C_{II}}{C_c} \tag{2.15}$$

for the amplifier to be stable in unity gain loop. (2.14) and (2.15) are important design equations that we will refer to while designing our amplifier for given specifications.

2.3 The Classical Miller Amplifier

Fig.2.6 shows a classical two stage op-amp, also called the miller amplifier. This op-amp can be seen as a cascade of voltage-to-current and current-to-voltage stages as shown in Fig.2.7 [3]. The first stage is a differential pair that converts the input differential voltage to differential currents applied to the current mirror load which reconverts it to an output voltage. The second stage is a common-source transistor (converting the first stage output voltage to a current) loaded by a current sink. The capacitance C_c between the first and the second stage is the miller compensation capacitance.

2.4 Performance Parameters

Apart from Gain, Bandwidth and Phase Margin which were discussed in the previous sections, there are a number of other performance parameters used to characterize an op-amp. Here we discuss these parameters briefly.

Output Swing The output voltage range over which the gain of the amplifier remains more or less constant. It is desirable to have a high output swing to accommodate a wide range of signal amplitudes.

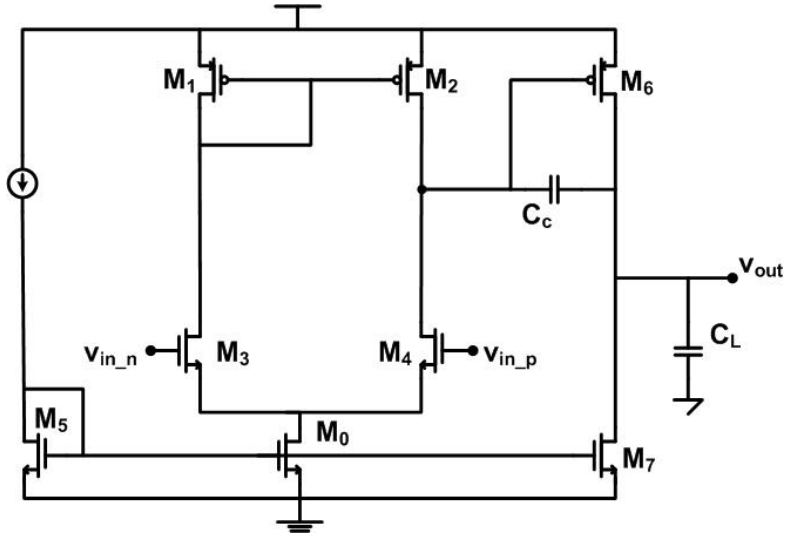

Figure 2.6: The classical miller amplifier

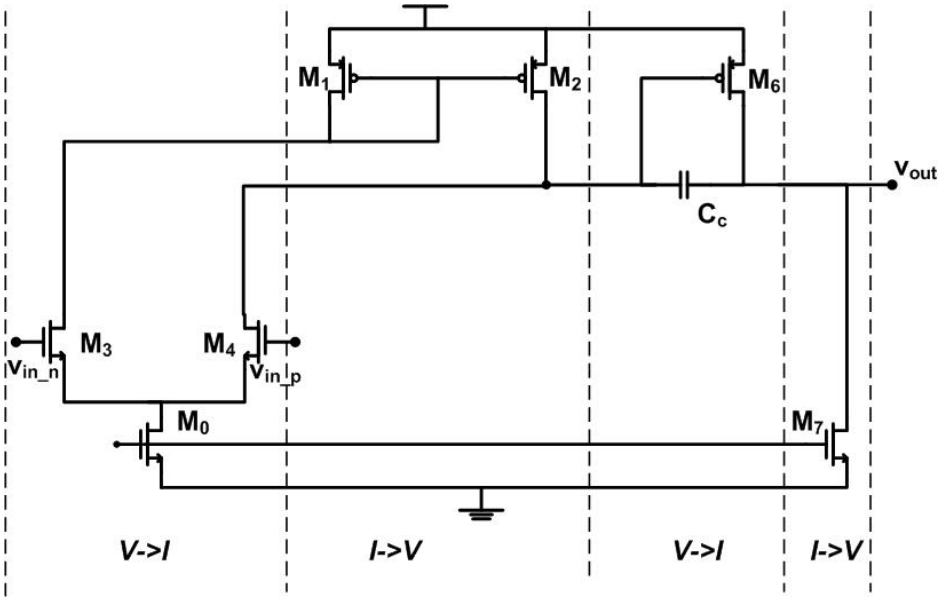

Figure 2.7: The miller amplifier visualized as a cascade of v-i and i-v blocks

Common Mode Range (CMR) The input voltage range over which the amplifier properties are not deteriorated.

Common Mode Rejection (CMRR) The ability of the op-amp to reject common mode signals.

Power Supply Rejection (PSRR) The ability of the op-amp to reject supply noise. This is especially important when the op-amp is employed in mixed-signal environments.

Noise and Offset The input referred noise and offset voltages determine the minimum signal level that can be handled by th op-amp.

Slew Rate It is measure of the speed of operation of the amplifier and is determined by the maximum current which can be delivered to a capacitive load.

Power Dissipation The total power dissipated by the op-amp. The effort is to minimize the power dissipation but this is essentially in a tradeoff with other performance parameters.

Chapter 3

State of the Art in Amplifier Design for Sensor Interfaces

3.1 Design Techniques and Results

A number of op-amp architectures and designs that can be used in sensor interfaces have been published in literature in recent years. Table 3.1 presents a summary of some of the designs reviewed during the course of this work.

	[4]	[5]	[6]	[7]
Technology	0.5μ	0.6μ	0.5μ	0.18μ
DC Gain (dB)	120	114	NA	88.7
CMRR (dB)	100	120	140	NA
PSRR (dB)	90	110	NA	NA
GBW (MHz)	25	2.3	NA	NA
Slew Rate (V/μs)	30	2.2	NA	NA
Noise (nV/$\sqrt{Hz}$)	6 at 100 kHz	17.47 at 1 kHz	27 at DC	46e3 at 4 MHz
Offset (mV)	3	0.05	0.8	4
Supply Voltage (V)	12	3.3	3	1.8
Quiscent Current (mA)	4	0.23	1.7	0.115

Table 3.1: State of the art in op-amp design for sensor interfaces

In [4], the authors present a high gain, high PSRR and high CMRR op-amp with the specific design goal being to achieve a CMRR above 100 dB. The op-amp uses a gain-boosted folded cascode current mirror load along with suppression of impact ionization current in the output stage to obtain

high gain. It also has a circuit to boost the slew rate. Even though the circuit achieves superior performance, its design seems very complex involving thirty local feedback loops. [5] describes a high CMRR, low offset op-amp designed for sensor interfaces. The op-amp incorporates a composite front-end gain stage based on cascading two differential stages. The authors claim to achieve low offset by doing a proper common centroid layout and low noise by choosing an optimum length for input differential pair. A current feedback instrumentation amplifier (CFIA) is presented in [6]. The amplifier has a very low offset and low noise primarily because of the use of ping-pong autozeroing and chopping. Current feedback is used because of their ability to sense differential input voltages in a common-mode voltage range that includes either of the rails thus allowing them to interfaced directly with ground-referenced sensors in single supply systems. [7] presents a configurable multi-sensor interface that includes a two-stage premap with 88 dB gain, 4MHz bandwidth and less than 50 nV/$\sqrt{Hz}$ noise.

3.2 Commercially Available Amplifiers

Several amplifiers for use in sensor applications are available commercially. Table 3.2 lists the reported performance summary of some of them.

	NI LMP2021	Intersil ISL28107	Intersil ICL7611	Maxim MAX9945	Analog Devices AD8506
DC Gain (dB)	160	0	0	130	120
CMRR (dB)	130	145	96	94	105
PSRR (dB)	139	145	94	100	100
GBW (MHz)	5	1	1.4	3	0.095
Slew Rate (V/μs)	2.6	0.32	1.6	2.2	13m
Noise (nV/$\sqrt{Hz}$)	11 at 10 kHz	13 at 10 kHz	100 at 10 kHz	15 at 10 kHz	45 at 1 kHz
Supply Voltage (V)	2.2-5.5	4.5	2	2.4	1.8
Quiscent Current (μA)	1.1e3	0.29e3	10	400	20

Table 3.2: Commercially available amplifiers for sensor interfaces

Chapter 4

Proposed Architecture

4.1 Target Design Specifications

Following the discussion in the previous chapters about the need for high-gain, low noise etc. for the op-amps required for sensor interface applications, the following performance specifications were targeted:

- Gain : $\geq$ 120 dB
- Noise : $\leq$ 10 nV/$\sqrt{Hz}$
- GBW : Configurable for high-speed or low-speed operation
- Power Consumption : Variable depending on speed
- PSRR : As high as possible
- CMRR : As high as possible
- Output Range : Rail to rail

4.2 Amplifier Architecture

The goal here is a high-gain amplifier. It is generally difficult to obtain high gain and high swing with a single stage; we opt to design a two-stage miller amplifier since a classical two stage amplifier architecture is a simple yet robust implementation of an op-amp. However, preliminary simulations suggested that even with a classical two stage architecture it would still be difficult to obtain a gain of as high as 120 dB. Two of the *classical* ways of achieving higher gain are using

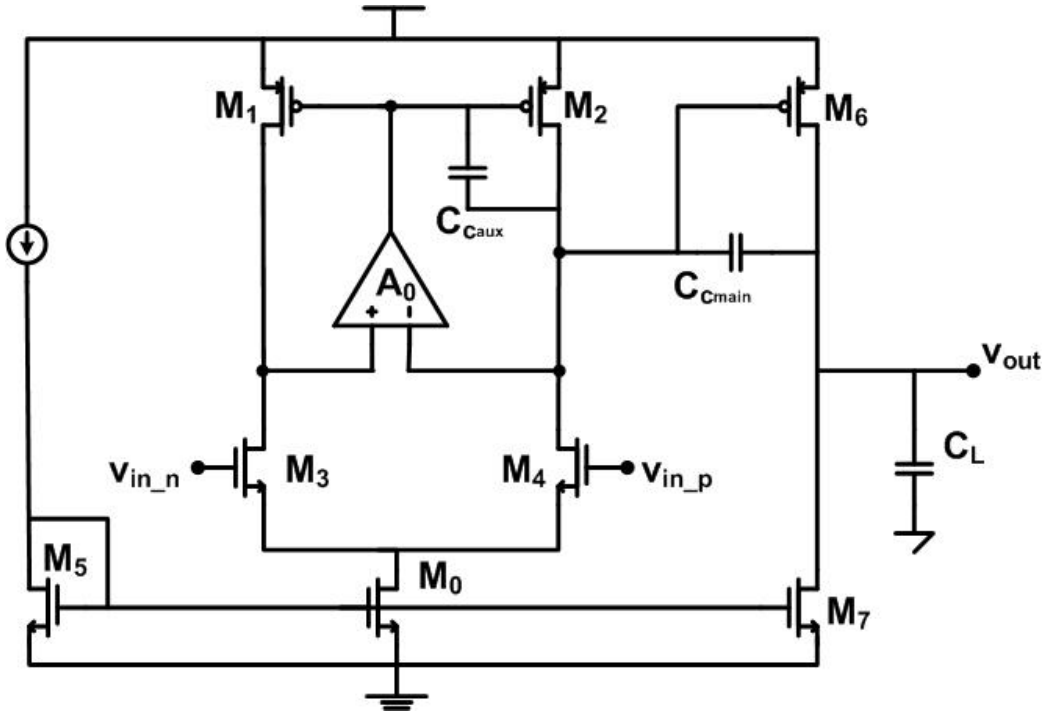

Figure 4.1: Complete two-stage op-amp with regulated current source load

- cascoded current mirror load, or
- folded-cascode current mirror load

in the first stage. The limitation with the cascode approach is that the cascode transistors eat into the voltage headroom. On the other hand, folded-cascode implementation requires a higher quiescent current leading to higher power consumption. To go-around these limitations and yet achieve the design specifications, two alternative loads were considered:

- cross-coupled positive feedback current mirror, and
- regulated current source load with auxiliary amplifier.

The cross-coupled positive feedback load was finally discarded in favor of regulated current source load. This is because even though the cross-coupled load is theoretically capable of providing a very high gain, the inherent positive feedback makes it difficult to stabilize. A detailed analysis of the cross-coupled load is given in Appendix A. Fig.4.1 shows the complete two-stage amplifier with the regulated current source load and compensation capacitors. Analysis of the regulated current source load follows in the next section.

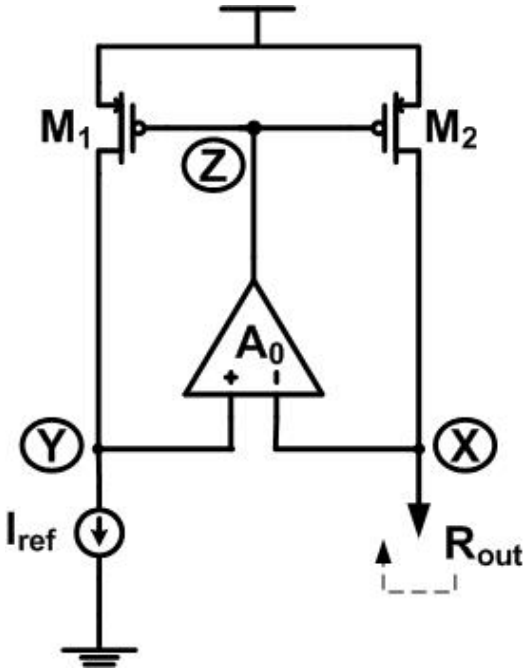

Figure 4.2: Architecture of the regulated current source load

4.3 Regulated Current Source Load

4.3.1 Principle of Operation

The load in a classical operational transconductance amplifier or OTA (the first stage of a classical miller amplifier) is a current mirror. The basic idea behind any modification in the load to improve the stage gain is to increase its output resistance. This is the same goal that the regulated current source structure of Fig.4.2 achieves while still maintaining a low compliance voltage, unlike a cascoded current mirror (or its variants). To understand the principle let us consider the circuit diagram in Fig.4.2 which shows two transistors M_1 and M_2 whose gates are driven by an amplifier A. Amplifier A acts as an error amplifier between the drain voltages of the two transistors. A current I_{ref} is drawn from M_1. The amplifier A implements a virtual ground between nodes X and Y causing the drain-source voltage of M_2 to track that of M_1. The amplifier A needs to adjust the gate voltage accordingly. Thus M_2 mirrors the current through M_1. The drain current through M_2 remains fairly constant effectively implying that the output resistance R_{out} of M_2 has been increased.

To see it rigorously, let us consider the small signal diagram of Fig.4.3.

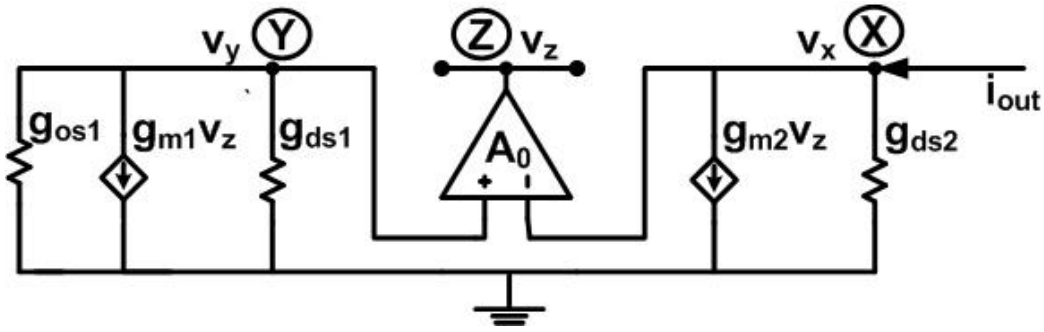

Figure 4.3: Small signal diagram of the regulated current source load

From the small signal diagram,

$$i_{out} = g_{ds2}.v_x + g_{m2}.v_z \tag{4.1}$$

$$v_y = \frac{-g_{m1}.v_z}{g_{os} + g_{ds1}} \tag{4.2}$$

$$v_z = A_o(v_y - v_x) \tag{4.3}$$

From, (4.1), (4.2) and (4.3), we get

$$\begin{aligned} R_{out} &= \frac{v_x}{i_{out}} \\ &= \frac{g_{os} + g_{ds1} + A_0\, g_{m1}}{g_{ds2}\,(g_{os} + g_{ds1} + A_0\, g_{m1}) - A_0\, g_{m2}\,(g_{os} + g_{ds1})} \\ &= \frac{1 + \frac{A_0\, g_{m1}}{(g_{os}+gds1)}}{g_{ds2}\left(1 + \frac{A_0\, g_{m1}}{g_{os}+g_{ds1}} - \frac{A_0\, g_{m2}}{g_{ds2}}\right)} \end{aligned} \tag{4.4}$$

where A_0 is the dc gain of the amplifier A and g_{os} is the output impedance of the current source I_{ref} and g_{m1} (g_{m2}) and g_{ds1} (g_{ds2}) are the small signal transconductance and output conductance respectively, of transistor M_1 (M_2). Assuming M_1 and M_2 are matched and $A_0\, g_{m1}/(g_{os}+g_{ds1}) >> 1$, (4.4) can be simplified to,

$$R_{out} \approx -1/g_{os} \tag{4.5}$$

It is easy to see then, that when a differential pair is loaded with this regulated current source (as shown in Fig.4.4) the output resistance of the gain stage approaches infinity.

$$\frac{1}{R_{out}} = \frac{1}{R_{up}} + \frac{1}{R_{dn}} \tag{4.6}$$

From (4.5),

$$R_{up} \approx -\frac{1}{g_{ds_{M_3}}} \; and \tag{4.7}$$

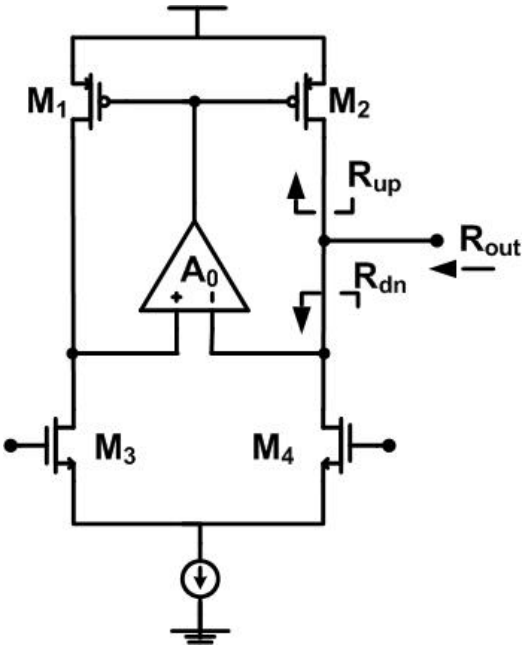

Figure 4.4: Differential pair loaded with the regulated current source

$$R_{dn} = \frac{1}{g_{ds_{M_4}}} \tag{4.8}$$

$$\tag{4.9}$$

Thus, if M_3 and M_4 are matched,

$$R_{out} \rightarrow \infty \tag{4.10}$$

High Frequency Behavior The above analysis describes the dc behavior of the circuit. Instead of doing a rigorous analysis, we present an intuitive approach for its high frequency behavior. First of all it is imperative to note that at higher frequencies the gain of the amplifier A is reduced. So, the node voltage at node X does not track the voltage at node Y anymore. Because of this the output impedance seen at node X becomes independent of the impedance seen at node Y. At high frequencies the capacitive impedance becomes the dominant one. Hence, the impedance seen at node X is now dominated by the parasitic capacitance C_x at that node [8].

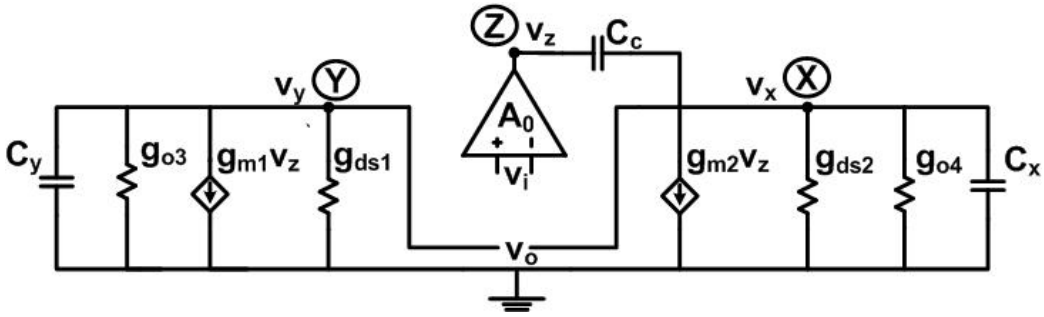

Figure 4.5: Small signal model of regulated current source with feedback loops open

4.3.2 Stability Analysis

The regulated current source consists of two loops. The first loop consisting of amplifier A and transistor M_1 is a negative feedback loop, while the second one with transistor M_2 is a positive feedback loop. This can lead to instability. We present the stability analysis of the circuit which mostly follows the analysis presented in [8].

Consider the small signal circuit in Fig.4.5 in which the loops have been opened at the amplifier inputs, total capacitances at nodes X and Y have been included and a capacitor C_c has been added. The amplifier A would be designed as a simple OTA with a single dominant pole. Its transfer function can then be written as:

$$A(s) = \frac{A_0}{1 + sC_z/g_{oa}} \tag{4.11}$$

where, C_z is the capacitance at node Z and g_{oa} is the output conductance of the amplifier.

Ignoring capacitor C_c, the open loop transfer function, defined as $H_{OL}(s) = v_o(s)/v_i(s)$ is given by

$$H_{OL}(s) = A_L^-(s) - A_L^+(s) \tag{4.12}$$

where A_L^- is the loop gain of the negative loop:

$$A_L^- = \frac{A_0\, g_{m1}/(g_{ds1} + g_{o3})}{(1 + sC_z/g_{oa})(1 + sC_y/(g_{ds1} + g_{o3}))} \tag{4.13}$$

and A_L^+ is the loop gain of the positive loop:

$$A_L^+ = \frac{A_0\, g_{m2}/(g_{ds2} + g_{o4})}{(1 + sC_z/g_{oa})(1 + sC_y/(g_{ds2} + g_{o4}))} \tag{4.14}$$

Assuming $g_{m1} = g_{m2} = g_{m12}$ and $g_{ds1} = g_{ds2} = g_{ds12}$, from (4.12), (4.13) and (4.14) we obtain,

$$H_{OL}(s) = \frac{A_0\, g_{m12}(g_{o4} - g_{o3})}{g_{ds12}(g_{ds12} + g_{o4})} . \frac{1 + s(C_x - C_y)/(g_{o4} - g_{o3})}{(1 + s/p_x)(1 + s/p_y)(1 + s/p_z)} \tag{4.15}$$

where $p_x = (g_{o3} + g_{ds12})/C_x$, $p_y = (g_{ds12} + g_{o3})/C_y$ and $p_z = g_{oa}/C_z$.

The open loop transfer function H_{OL} has three poles. In the context of this circuit being used as a load in a gain stage, the position of pole p_x would largely be governed by capacitance C_x, which could be the output capacitance loading the stage. The relative positions of the three poles would be governed by the values of the conductances and capacitances. With the respective values being comparable, the poles could lie in close proximity leading to instability. That the circuit is indeed unstable has been verified by simulation which will be presented in a later section. Simulations suggest that poles p_x and p_z need to be split to stabilize the loop. This can be done by using a compensation capacitance C_c as shown in Fig.4.5. With C_c in place the open loop transfer function is modified as

$$H_{OL}(s) = \frac{A_0\, g_{m12}(g_{o4} - g_{o3})}{(g_{ds12} + g_{o3})(g_{ds12} + g_{o4})} . \frac{(1 - s/z_1)(1 + s/z_2)}{(1 + s/p_x^{'})(1 + s/p_y)(1 + s/p_z^{'})} \tag{4.16}$$

where $p_x^{'} = g_{m12}/(C_x + C_y)$,
$p_z^{'} = g_{oa}g_{ds12}/g_{m12}C_c$,
$z_1 = (g_{o4} - go3).g_{m12}/C_c\,(g_{m12} + g_{o4})$ and
$z_2 = g_{m12}/C_x$.

Now, for the full two-stage amplifier of Fig.4.1 the pole at node Z is an additional non-dominant pole. Referring to the discussion in chapter 2, for stability, the non-dominant pole must lie farther away from the GBW, i.e. $p_z^{'} >> GBW_{main}$,

$$\frac{g_{oa}g_{ds12}}{g_{m12}C_c} >> GBW_{main} \tag{4.17}$$

where GBW_{main} is the gain bandwidth of the full two-stage amplifier.

Fig.4.6 shows the implementation of the auxiliary (error) amplifier. The compensation capacitance $C_{c_{aux}}$ added for stabilizing the loops in the current source load is also shown (dotted). It can be seen that $C_{c_{aux}}$ is connected

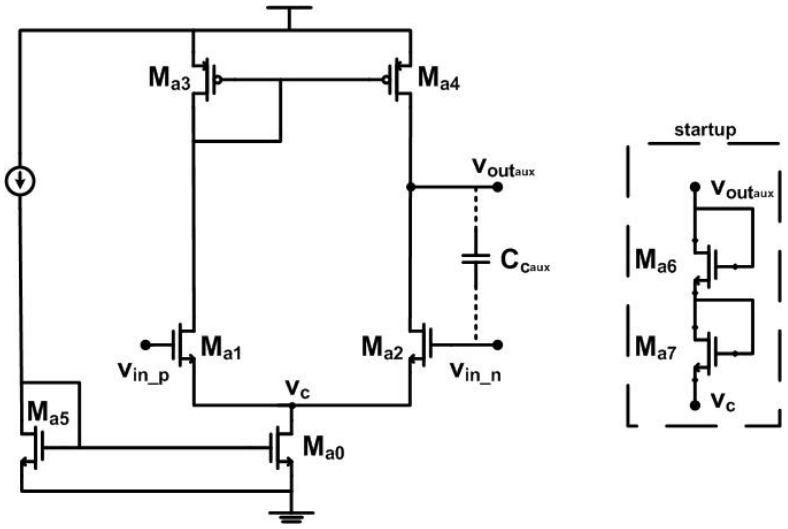

Figure 4.6: The auxiliary (error) amplifier

between the gate and the drain of transistor M_{a2}. This will cause M_{a2} to behave as a diode connected transistor at higher frequencies (around GBW). This implies that at such frequencies the output conductance of the auxiliary amplifier will be

$$g_{oa} = g_{ma12} \tag{4.18}$$

Substituting (4.18) in (4.17) and replacing C_c by $C_{c_{aux}}$,

$$\frac{g_{ma12}g_{ds12}}{g_{m12}C_{c_{aux}}} >> GBW_{main} \tag{4.19}$$

Normally, the ratio $\frac{g_{m12}}{g_{ds12}}$ which is the intrinsic gain of a transistor will be much greater than 10. Thus, to satisfy (4.19), we can safely choose

$$GBW_{aux} \geq 4\,GBW_{main} \tag{4.20}$$

where,

$$GBW_{aux} = \frac{g_{ma12}}{C_{c_{aux}}}$$

is the gain bandwidth of the auxiliary amplifier. (4.20) is another important design equation that we will use to design the complete amplifier.

4.3.3 Simulation Results

The simulated frequency response of the an uncompensated regulated current source load (loading the differential pair of a two stage amplifier) is shown

in Fig.4.7. To obtain the frequency response both the loops of the current source were opened at the inputs of the error amplifier and the differential output was taken at the drains of the pmos transistors that the error amplifier drives. Fig.4.7 shows that the uncompensated circuit is indeed unstable as the phase at unity gain frequency is close to $-400°$. On compensating the circuit with a 2pF compensation capacitor, the frequency response of Fig.4.8 is obtained. The compensation capacitor causes pole splitting as discussed in section 4.3.2 and thus the phase margin of approximately $90°$ is achieved. consequently, these simulation result validate the analysis of section 4.3.2.

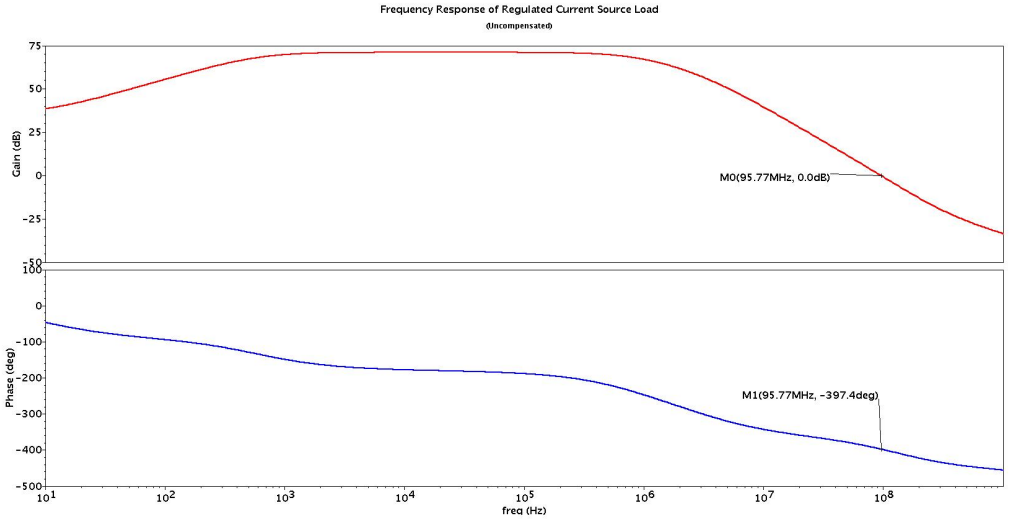

Figure 4.7: Frequency response of the uncompensated regulated current source load

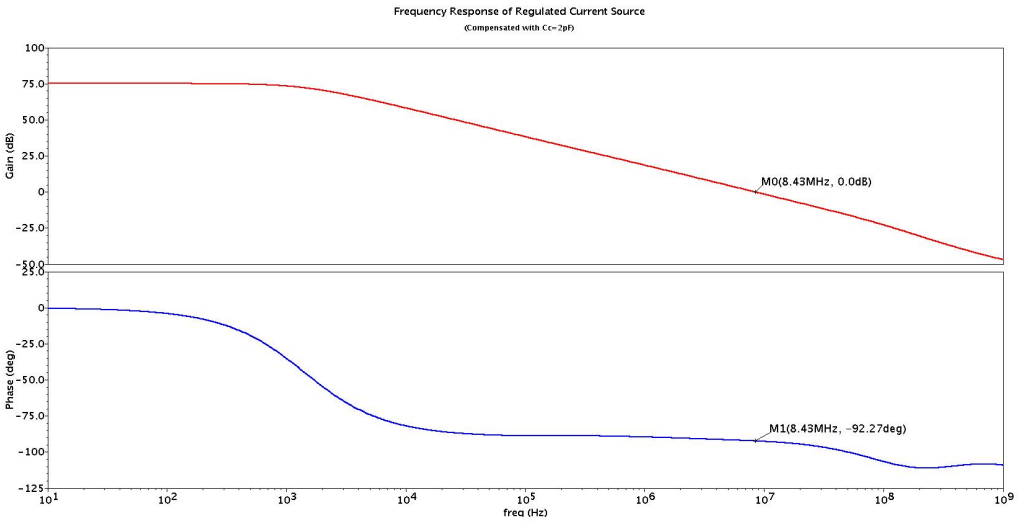

Figure 4.8: Frequency response of the regulated current source load compensated by a 2pF capacitor

Chapter 5

Design Methodology

5.1 Design Equations

In this chapter we will outline the design methodology adopted to design the two-stage amplifier with the regulated current source load. The discussion will draw on the discussions and analysis of the previous chapters. The circuit diagrams of the full amplifier as well as the constituent auxiliary amplifier are reproduced for convenience (Fig5.1 and Fig.5.2). We recap the design goals here:

1. Very high gain
2. Low noise
3. GBW configurable for high-speed or low-speed operation
4. PSRR as high as possible
5. CMRR as high as possible

Once we have selected the circuit architecture, design goals (4) and (5) are essentially equivalent to (1) vis-a-vis circuit design. Good layout is the only additional thing that can be done to have a high PSRR and CMRR.

It was pointed out that equations (2.14), (2.15) and (4.20) are important design equations for the design of this amplifier. We reproduce them here with appropriate notation (referring to Fig5.1 and Fig.5.2).

$$GBW_{total} = \frac{g_{m34}}{C_c} \tag{5.1}$$

$$\frac{g_{m6}}{g_{m34}} \geq 3\frac{C_L}{C_c} \tag{5.2}$$

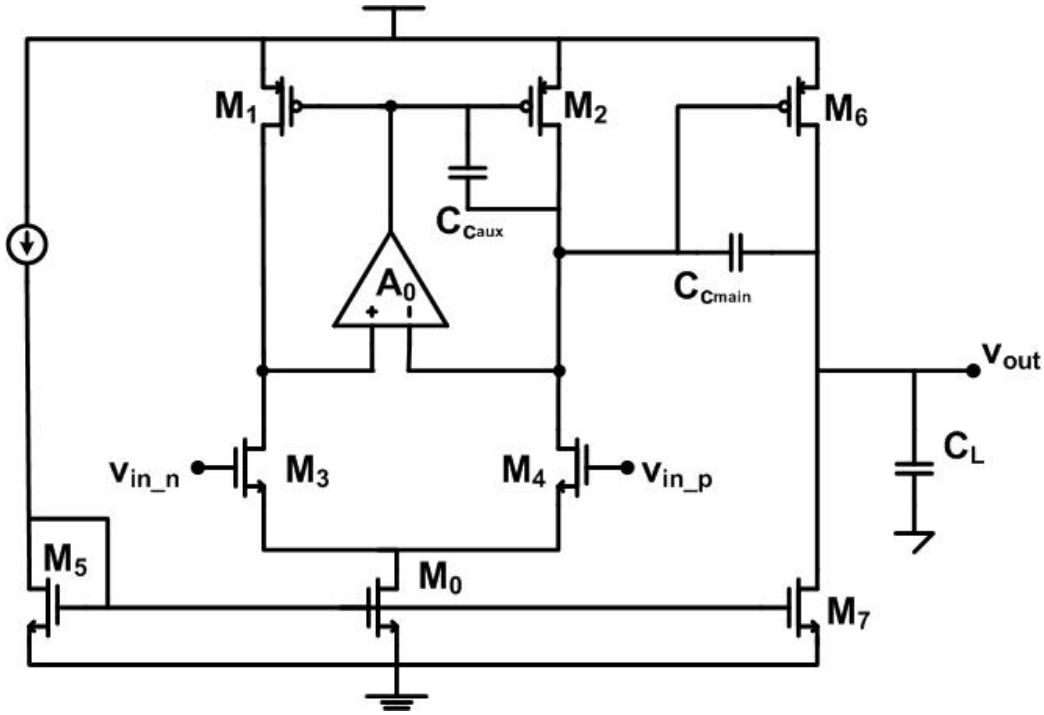

Figure 5.1: Complete two-stage op-amp with regulated current source load

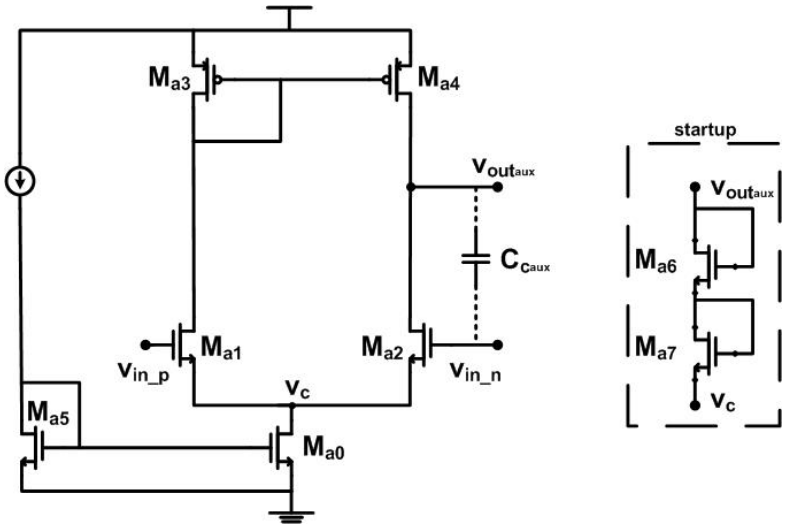

Figure 5.2: The auxiliary amplifier

$$GBW_{aux} \geq 4\,GBW_{total} \tag{5.3}$$

The only missing equation is the one for the gain of the amplifier. Since it is a two-stage cascaded amplifier it is obvious that the total gain will be the product of the gains of the two stages. The gain of the second stage is easily written as

$$A_{II} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} \tag{5.4}$$

To derive the gain of the first stage we note that the output of this stage is taken at the positive feedback loop. From (4.14) we can write the open-loop gain of the loop

$$A_L^+ = \frac{v_{out_1}}{v_{in_{aux}}} = A_0 \frac{g_{m2}}{g_{ds2} + g_{ds4}} \tag{5.5}$$

When the loop is closed, the input signal at the inverting input of the error amplifier provided by the input transistor M_3 is

$$v_{in_{aux}} = \frac{g_{m34}}{g_{ds2} + g_{ds4}} . v_{in} \tag{5.6}$$

So, we can write the first stage gain as

$$\begin{aligned} A_I &= \frac{v_{out_1}}{v_{in_{aux}}} . \frac{v_{in_{aux}}}{v_{in}} \\ &= \frac{A_0\, g_{m2}\, g_{m34}}{(g_{ds2} + g_{ds4})^2} \end{aligned} \tag{5.7}$$

Therefore, total gain of the amplifier is

$$A_{total} = \frac{A_0\, g_{m2}\, g_{m34}}{(g_{ds2} + g_{ds4})^2} . \frac{g_{m6}}{g_{ds6} + g_{ds7}} \tag{5.8}$$

(5.8) completes our set of design equations required to develop a design methodology for this amplifier which we outline in the next section.

5.2 Design Steps

Here we outline one of the possible design sequences for designing the required amplifier. A number of alternative sequences can be adopted depending upon the design goals and constraints on performance specifications. Here, we will list the steps to design an amplifier for a required gain A_{total} within a given power budget (implying a constraint on the bias current I_0, since bias voltage is fixed), and a given bandwidth GBW_{total} with a fixed load capacitance C_L.

1. Given C_L, choose
$$C_c \approx \frac{C_L}{3}$$

2. Determine the g_m of the input differential pair using
$$g_{m34} = 2\pi\, C_c\, GBW_{total}$$
ref.(5.1)

3. Allocate $(1/10)^{th}$ of the total bias current to the input pair. We call it I_{0I}.

4. Size the differential pair using
$$\begin{aligned} \frac{g_m}{I_D} &= \frac{1/nU_T}{0.5 + \sqrt{(0.25 + I_c)}} \; and \\ W/L &= \frac{I_D}{2nU_T^2 K_p I_c} \end{aligned}$$
where U_T is the thermal voltage, n is the slope factor, K_p is the process parameter and $I_D = I_{0I}/2$.

5. Using (5.2) calculate the transconductance g_{m6} of the second stage common source transistor.

6. The ratio g_{m6}/g_{m34} also gives an idea of the current to be allocated to the second stage. (5.2) implies $g_{m6}/g_{m34} \geq 9$. We choose $I_8/I_{0I} = 10$, i.e. 10 times more current in the second stage than in the first stage differential pair.

7. Knowing g_m and I_D size the transistor as in step 4.

8. Using (5.4) and value of g_{m6} obtained in the previous step, determine the gain A_{II} that can be obtained from the second stage. The value of g_{ds} can be calculated using
$$g_{ds} = \frac{I_D}{U_a.L}$$
where U_a is the early voltage and L is the channel length of the transistor. We opt to choose $L_7 = 2$*unit length $(2 * 0.5\mu m)$ for the nmos and $L_6 = (K_n/K_p).L_{12}$ for the pmos.

9. Similarly, calculate g_{ds2} and g_{ds4}.

10. Now, knowing the gain to be obtained from stage I, $A_I = A_{total} - A_{II}$, we can use (5.7) to get

$$A_0.g_{m2} = \frac{A_I.(g_{ds2} + g_{ds4})^2}{g_{m34}}$$

11. We choose to allocate $1/4^{th}$ of the total gain as the gain of auxiliary amplifier (A_0).

12. Thus, g_{m2} is determined. Knowing g_{m12} and I_D, M_2 and M_1 can be sized.

Auxiliary Amplifier We now turn our attention to the design of the auxiliary amplifier.

1. From (5.3) determine GBW_{aux}.

2. A reasonable initial value of $C_{c_{aux}}$ can be chosen and iteratively modified depending on the bias current available and the value of g_m calculated in the next step while ensuring that (5.3) remains satisfied.

3. Calculate $g_{ma12} = 2\pi\, C_{c_{aux}}\, GBW_{aux}$.

4. We allocate the rest of the current to the auxiliary amplifier (current remaining from the bias current constraint after allocating to the differential pair and the common source stage).

5. Knowing g_m and I_D size the differential pair.

6. Knowing the gain and g_m, calculate the output resistance and hence the lengths of the differential pair and load transistors.

7. The current mirror load should work in strong inversion. The load transistors can be sized by choosing an appropriate inversion factor (>10) as the starting point.

Startup transistors Fig.5.2 shows two additional diode connected transistors M_{a6} and M_{a7} which are connected in series between the output node $vout_{aux}$ and the source of the differential pair, node v_c. These act as a startup circuit for the regulated current source load. This startup circuit provides a current path when the two inputs are balanced but cuts off as soon as the a dc voltage develops at $vout_{aux}$. From simulations it was determined that

$V(vout_{aux}) - V(v_c) > 2 * V_T$, where V_T is the threshold voltage. Since, after startup, we want the current to be of the order of nA or smaller, relatively small sized transistors would do the job. We choose to size each transistor as W/L = 8/1 and confirm by simulation.

Current Sources The current source transistors M_0, M_5, M_7, M_{a0} and M_{a5} should be sized keeping the output dynamic in mind. To maximize the output dynamic range we size these transistors such that the saturation voltage across each is around 200 mV. The transistor can be sized using

$$I_D = \frac{K_p}{2n}.\frac{W}{L}V_{Dsat}^2.$$

Note that $W/L(M_0) = W/L(M_5)$, $W/L(M_7) = 10{*}W/L(M_0)$ and $W/L(M_{a0}) = W/L(M_{a5})$.

Chapter 6

Prototype Design

6.1 Design of a 200 μA Amplifier

In this section we present the design of an amplifier starting with the following specifications and constraints:

- Gain, A_{total} = 150 dB
- Gain bandwidth, GBW_{total} = 10 MHz
- Load capacitor, C_L = 10 pF
- Current consumption, I_0 = 200 μA.

The design has been done using the 0.50μm 5 V 2P3M standard CMOS process (Vanguard International Semiconductor Corp.) by following the design methodology developed in chapter 5. The detailed design calculations are given in Appendix B. Table 6.1 lists the dimensions and region of operation of each transistor. Note that transistor sizes listed here are the final values obtained after iterative design procedure including simulation, design optimization and after making modifications for layout considerations.

6.2 Simulation Results

In this section we present the results of simulations performed on the final circuit. Fig.6.1 shows the frequency response of the auxiliary amplifier which is typical of a classical OTA. A GBW of approximately 32 MHz is achieved which is a bit lower than the 40 MHz targeted value. This can primarily be attributed to the lower g_m of its differential pair transistors whose sizes were reduced in the final design. Still, enough gain was achieved to fulfill

Transistor	**W/L**	**Region**
M_1, M_2	3/1.2	SI
M_3, M_4	144/1	edge of WI
M_6	400/1.2	MI
M_{a1}, M_{a2}	16/2	MI
M_{a3}, M_{a4}	6/1.2	SI
M_{a6}, M_{a7}	8/1	cutoff
M_0, M_5	10/1	SI
M_7	100/1	SI
M_{a0}, M_{a5}	12/2	SI

Table 6.1: Transistor sizes for the 200 μA amplifier

the design targets. Fig.6.2 shows the frequency response of the complete amplifier. An overall dc gain of 143 dB and a GBW of 8 Mhz is obtained. The stability requirement that the GBW of the auxiliary amplifier should be 4 times the GBW of the main amplifier is maintained. The difference between the targeted gain of 150 dB and the achieved value of 143 dB can primarily be attributed to the loss in gain of the second stage. The second stage common source transistor is the largest transistor in the circuit and hence contributes substantial parasitic capacitance. To diminish the effect of the parasitic contribution of this transistor (to ensure stability) and to facilitate layout its size (hence gain) was reduced.

Even though the achieved phase margin is 41° (much less than the *textbook requirement* of 60°), the transient response of Fig.6.3 shows that the circuit is practically stable with a very fast settling time as presented in table 6.2. The transient is obtained for a 1 V step applied to the op-amp used in a unity feedback configuration. The output shows a peak ripple of less than 1 mV. When used in a feedback loop with gain=4, the transient output shown in Fig.6.4 shows no ripple albeit slower response. Figs.6.5, 6.6, 6.7 show the frequency behavior of the PSRR+, PSRR- and CMRR respectively of the op-amp. High values are achieved for the three at dc. Even though, ideally the three quantities should retain their high values upto very high frequencies, the architecture of the circuit (single ended output, common-source second stage etc.) does not offer any scope for improvements. Thus the frequency behavior obtained is typical. Fig.6.8 shows the output swing that can be achieved with the circuit. The output swing is limited by the saturation voltage of the second stage current source. Hence it was carefully designed

to have a low saturation voltage of 200 mV.

The circuit has an input referred noise of approximately $15\text{nV}/\sqrt{Hz}$ which, even though is a bit higher than the initial target of $10\text{nV}/\sqrt{Hz}$, yet is very low and is better than or in line with the state-of-the-art. The noise can be reduced further by increasing the size of the input differential pair of the op-amp or pushing more current through it. However, keeping in mind the area and power penalty both of these solutions are undesirable when the circuit's noise performance is already very good.

6.3 Performance Summary

Table 6.2 summarizes the performance parameters for the amplifier. The amplifier can operate in two modes of operation, viz. high-speed and low-speed. The high-speed operation consumes more power than the low-speed operation, which consumes about 10 times less. The performance of the amplifier for both the modes is shown side-by-side for easy comparison.

Parameter	**High-Speed**	**Low-Speed**
Supply Voltage (V)	3.0	3.0
Quiescent Current (μA)	210	23
DC Gain (dB)	143	155.4
GBW (MHZ) (10 pF load)	7.98	0.864
Slew Rate (V/μs)	1.55	0.49
Settling Time (ns)	150	2.7e3
CMRR (dB)	112.3	121.8
PSRR+ (dB)	116.2	126.1
PSRR- (dB)	121.7	130.6
Phase Margin (°)	41	67
Output Swing (V)	2.78	2.78
Noise at 100 KHz (nV/$\sqrt{Hz}$)	15.2	51.7
Offset (mV) (100 run MC simulation)	1.95	4.37

Table 6.2: Summary of the amplifier performance parameters

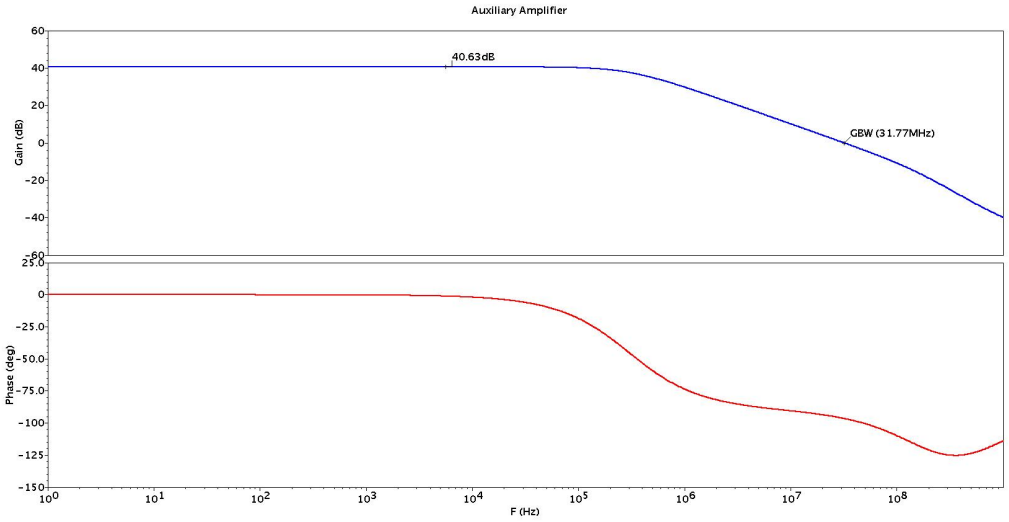

Figure 6.1: Frequency response of the auxiliary amplifier

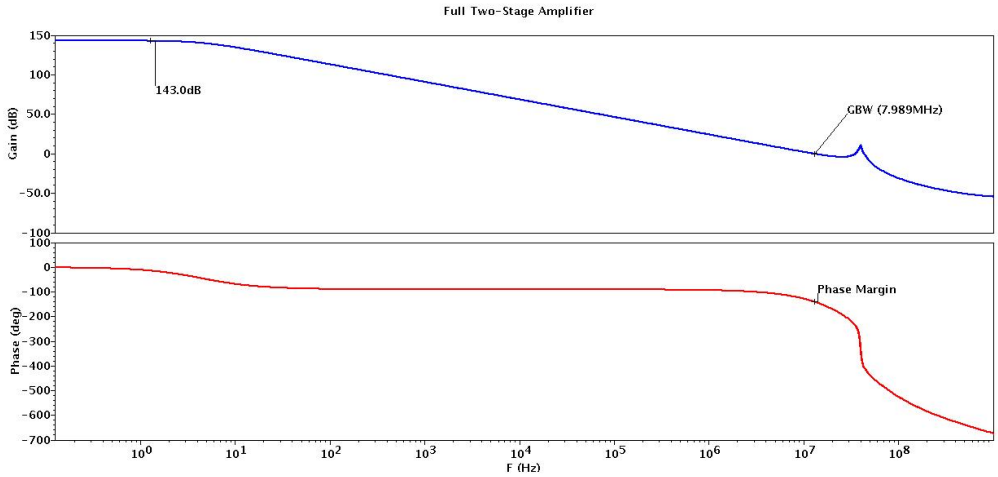

Figure 6.2: Frequency response of the complete op-amp

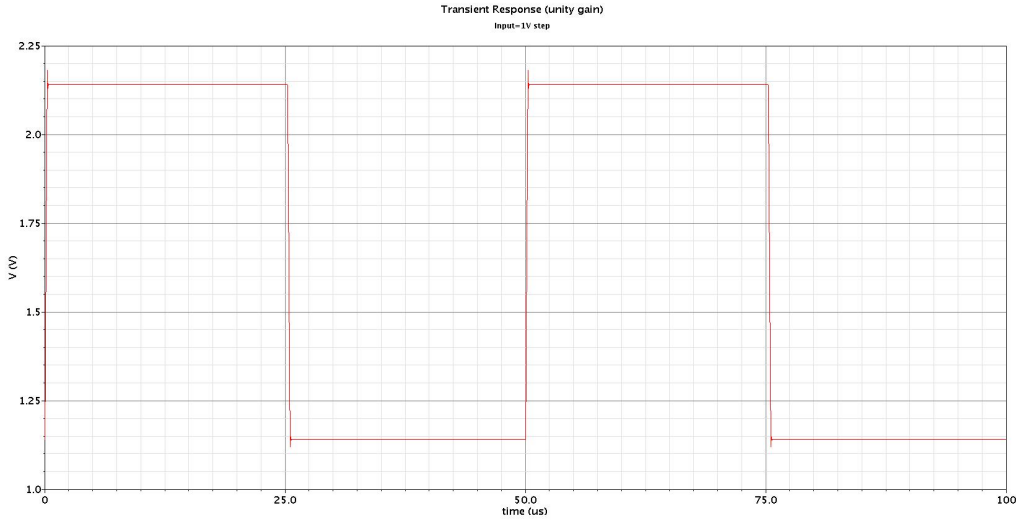

Figure 6.3: Transient response of the op-amp in unity gain feedback loop

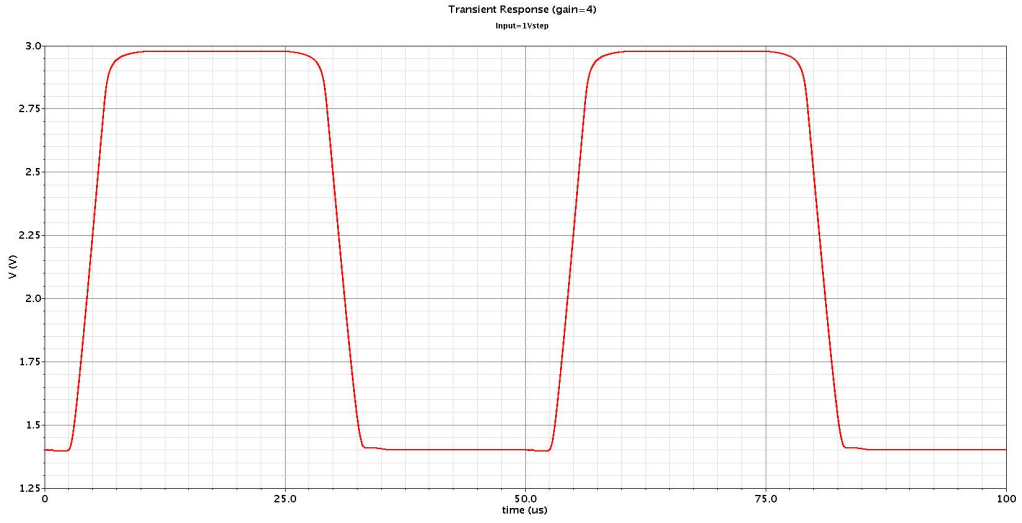

Figure 6.4: Transient response of the op-amp in feedback loop with gain=4

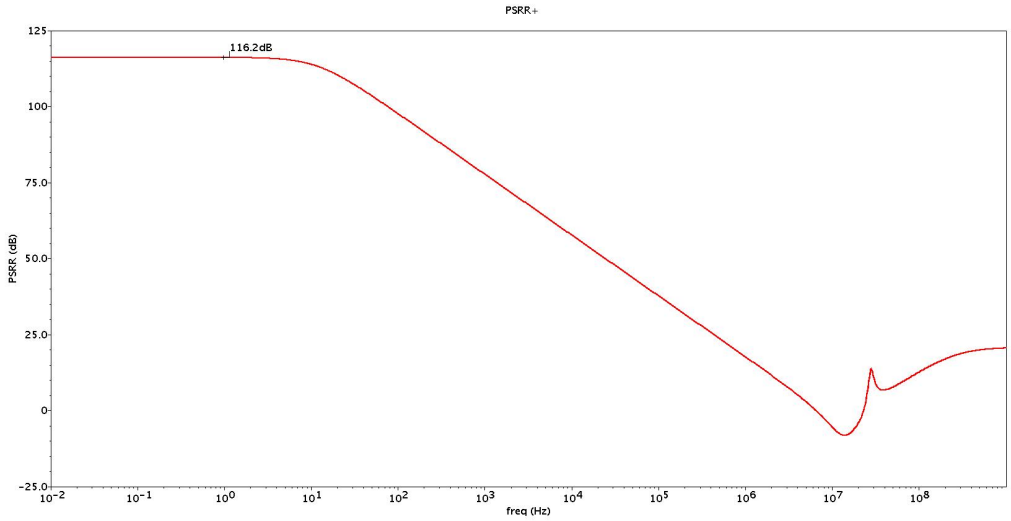

Figure 6.5: PSRR (Vdd rail) response

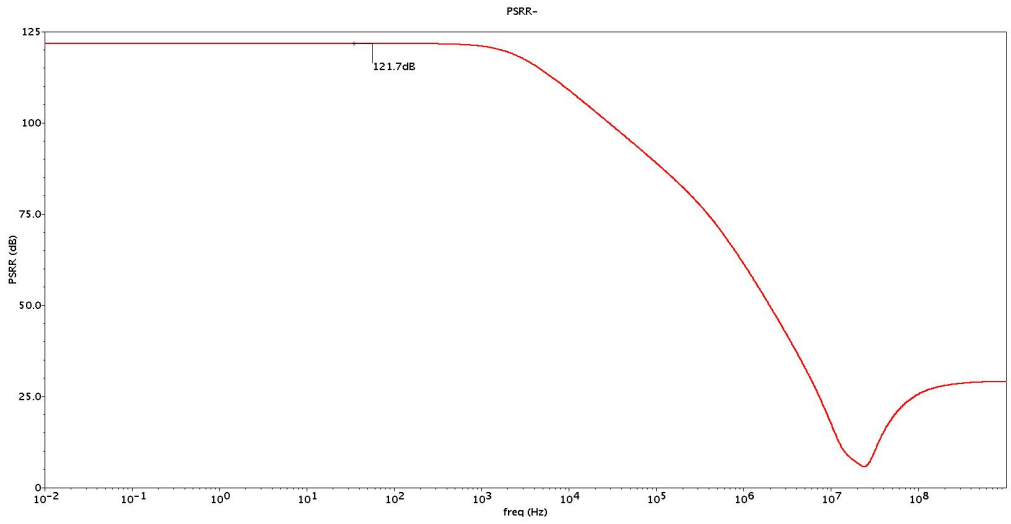

Figure 6.6: PSRR (ground rail) response

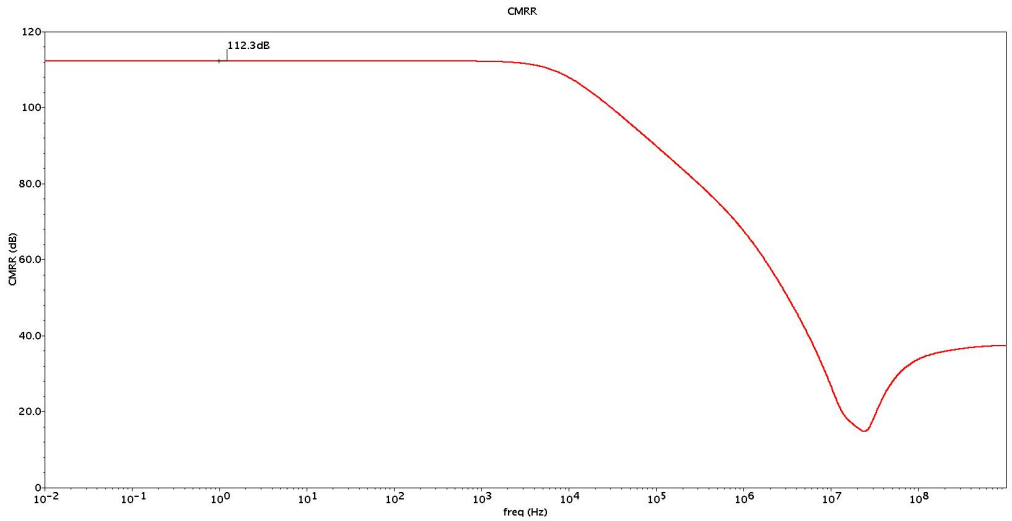

Figure 6.7: CMRR response

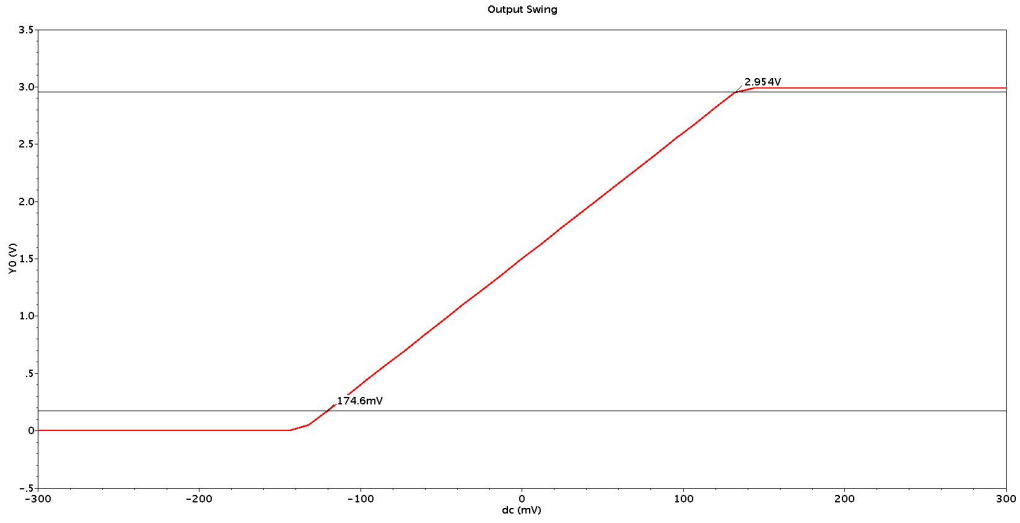

Figure 6.8: Output Swing of the op-amp

Chapter 7

Layout

7.1 General Layout Considerations

Careful layout is important in analog design to improve matching between devices. Matching is important to achieve high CMRR and low offset. Some of the well known analog layout considerations and techniques to minimize mismatch effects are listed below:

- Large device sizes
- Minimum distance between devices
- Symmetrical layout
- Same orientation of devices to be matched
- Same environment of devices to be matched
- Multi-finger transistors
- Common-centroid layout

In the design of this amplifier the differential pairs of both amplifiers- the auxiliary amplifier and the overall amplifier- are laid-out in a quad common-centroid fashion. The common-centroid layout has been done such that the large differential pair transistors are split up into two sub-groups each of which is laid-out in the common centroid manner. The sub-groups are then placed in a common-centroid layout as shown in Fig.7.1. This technique is advantageous in minimizing the mismatch error between transistors and increasing randomness in topological placement [5]. The other transistors are laid-out by splitting them up into fingers and interdigiting wherever possible.

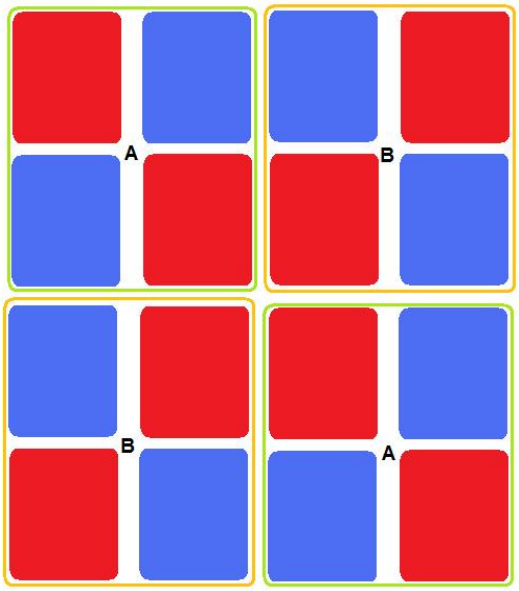

Figure 7.1: Quad common-centroid layout technique

The capacitors have been placed at the outskirts of the circuit to facilitate future design modifications which require values of the compensation capacitors to be changed.

7.2 Capacitor Layout-PIP vs. MOSCap

With the used 2P3M technology, a capacitor can be designed in three alternative ways- Poly-Insulator-Poly (PIP), Metal-Insulator-Metal (MIM) or using a MOS transistor as a capacitor (MOSCap). We decided to make a comparative study between PIP and MOSCap to select one of the two for final implementation (primarily because PIP capacitor is available in standard cell library and and similarly a standard MOS can be easily configured to be used as MOScap).

To compare the relative merits and demerits of PIP and MOSCap, a 1 pF capacitor of each type was designed and simulated. It was found that the MOSCap occupies one-third the area occupied by PIP capacitor for the same capacitance value. Moreover, PIP capacitors require an additional process step during fabrication thereby being costlier. Simulation results showing capacitance vs. the voltage across the capacitor is shown in Fig.7.2 and Fig.7.3. It is seen in Fig.7.2 that the capacitance value drops by nearly 80% between

the voltages marked V_L and V_H. For the MOSCap, the capacitances are nearly constant in the *Inversion Region* (below V_L) and in the *Accumulation Region* (after V_H) but drops in the *Depletion Region* where the channel is depleted of the charges. On the other hand, a PIP is a simple parallel plate capacitor whose capacitance is reasonably constant.

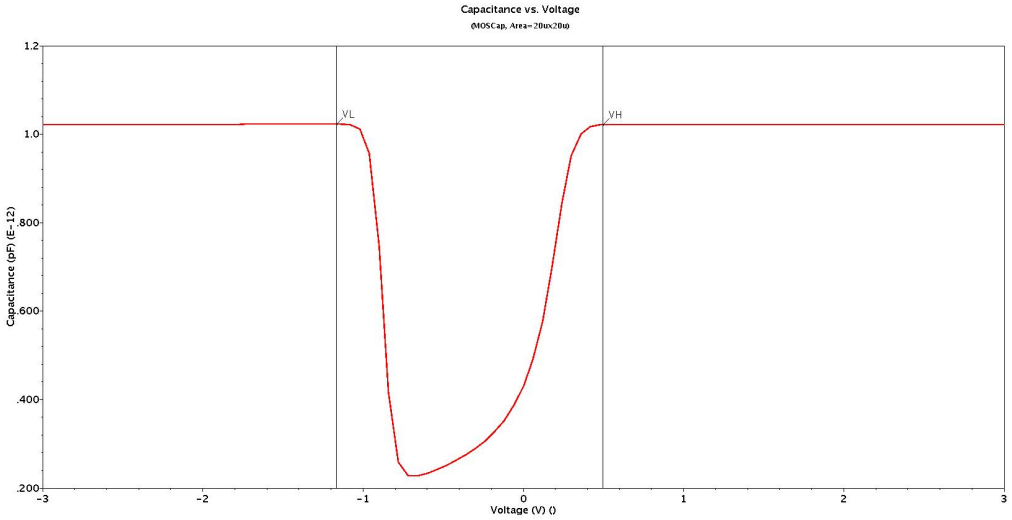

Figure 7.2: Variation of capacitance with voltage for a 1pF MOSCap capacitor

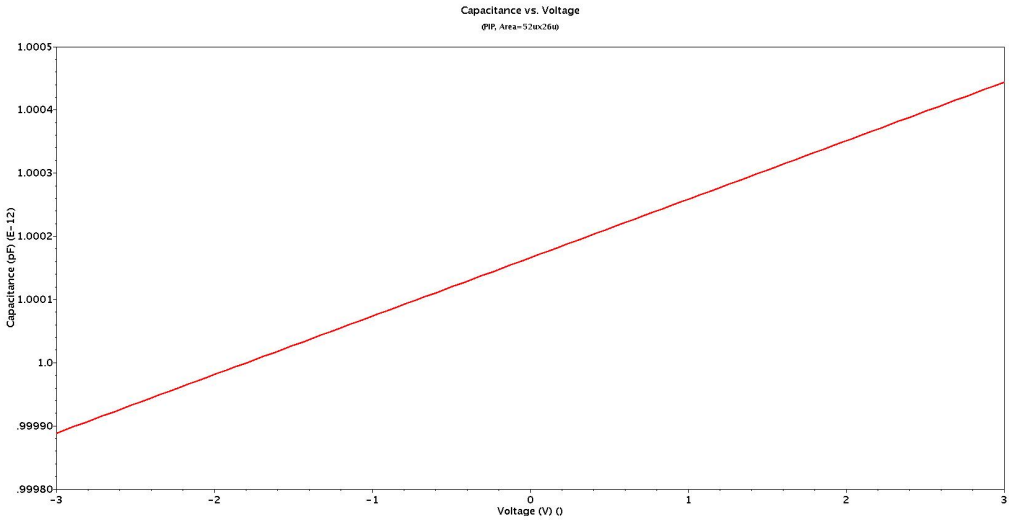

Figure 7.3: Variation of capacitance with voltage for a 1pF PIP capacitor

Even though the PIP capacitors are costlier in terms of area and fabrication cost the capacitance variability of the MOSCap was a deterrent in their use for the amplifier. The amplifier has an almost rail-to-rail dynamic range. The nodes between which the two compensation capacitors connect can swing over a range of voltages wide enough to push the MOSCap into depletion (and hence 80% reduced capacitance) and thereby driving the circuit unstable.

7.3 Final Layout

Fig.7.4 shows the full final layout of the circuit. Fig.7.5 shows the same layout with the various constituents of the amplifier are marked. The circuit occupies a total area of 87.46 μm x 183.31 μm (0.16 mm^2), out of which the compensation capacitors occupy 4788 μm^2.

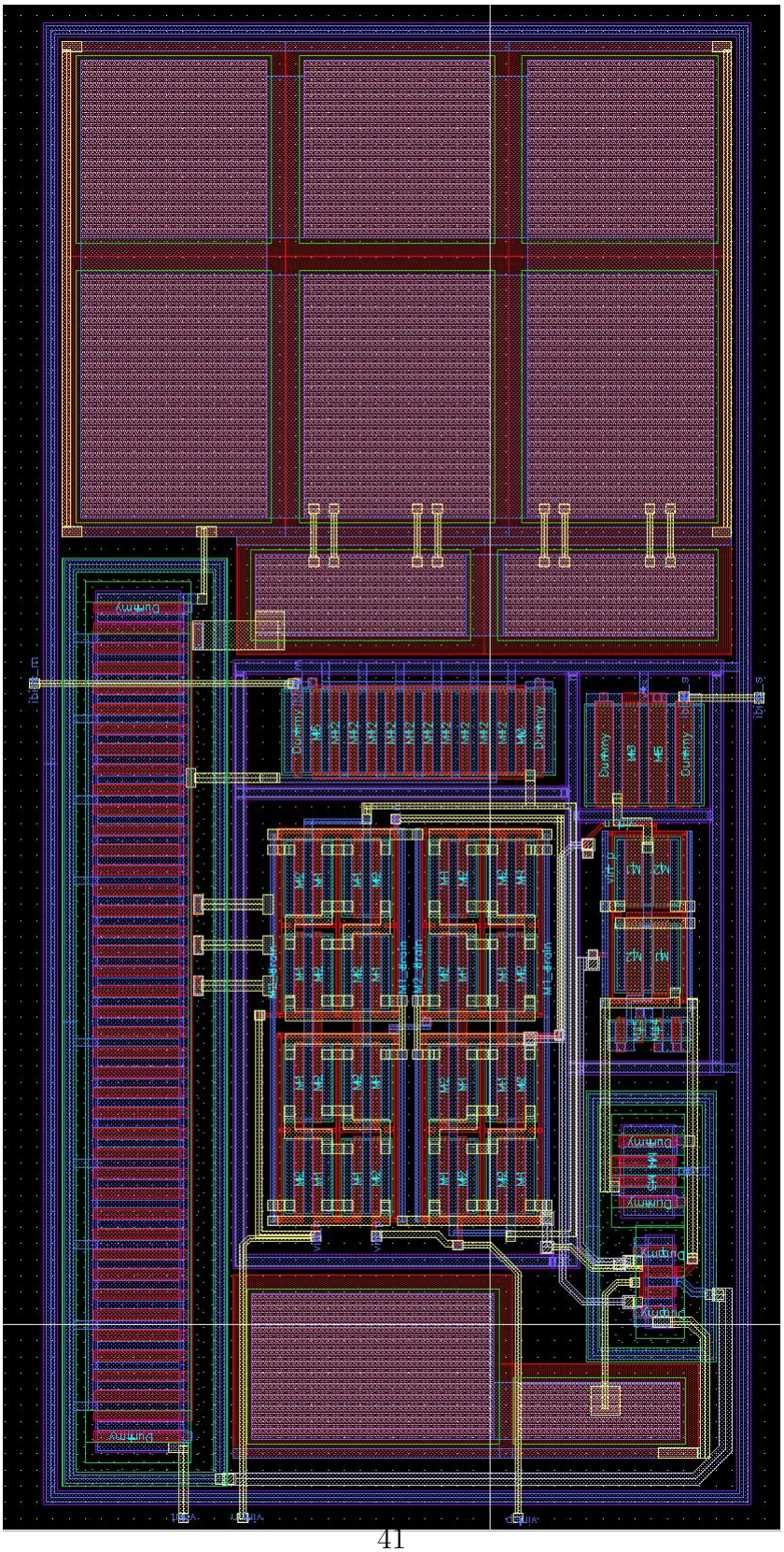

Figure 7.4: Layout of the full two-stage op-amp

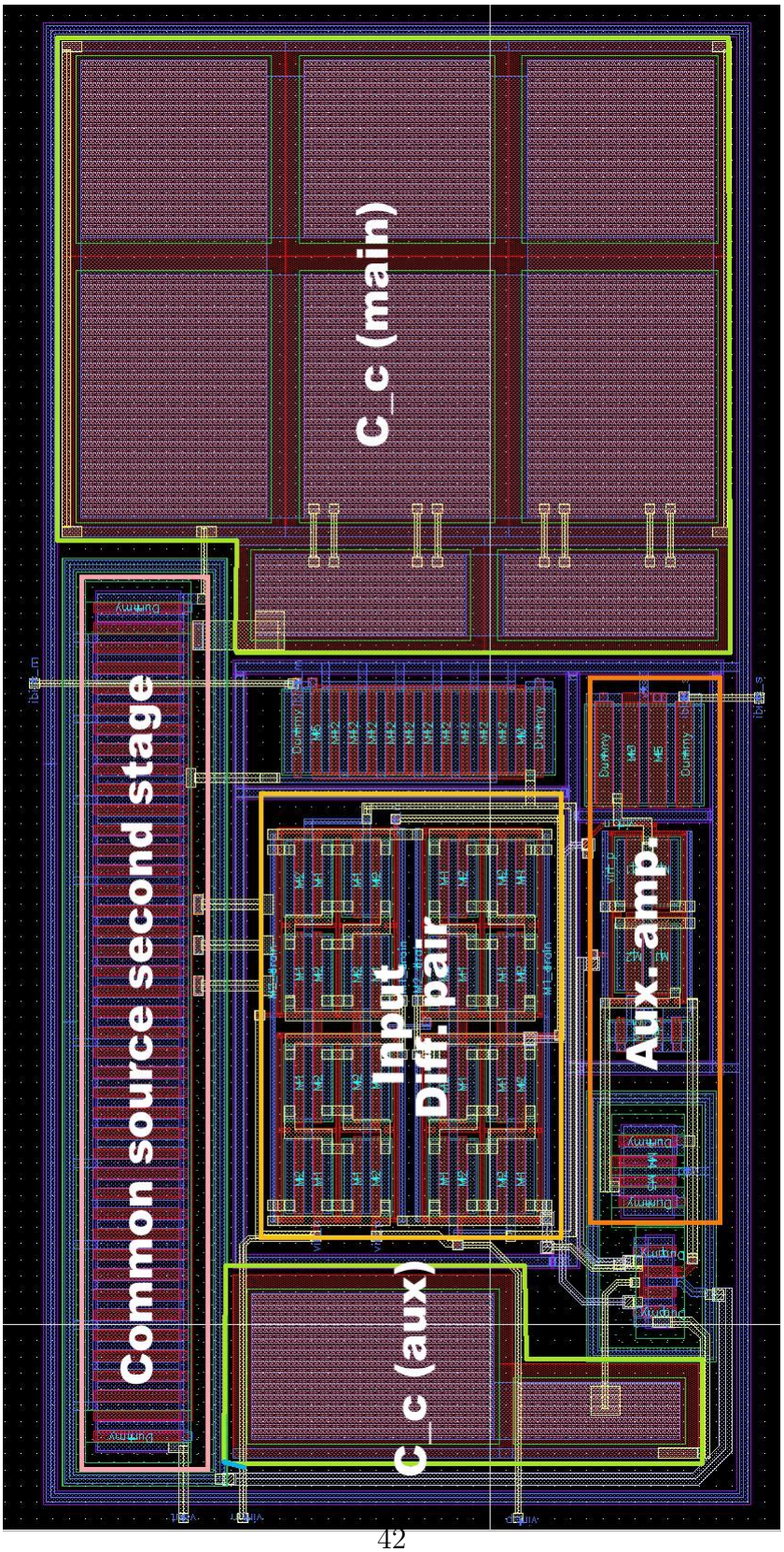

Figure 7.5: Layout showing the constituents of the amplifier

Chapter 8

Conclusion

This thesis presents the design of a very high-gain, low-power, low-noise op-amp intended for use in a generic sensor interface. The classical two-stage miller amplifier was chosen as the starting point of the design because of its simplicity and robustness and a well defined design methodology. It was already conspicuous at the beginning of the project that it will be difficult, if not impossible, to achieve the >120 dB targeted value of gain with just the classical two-stage structure. Cascoding, which is a typical method of increasing the gain, was rejected because of the low-power and high-dynamic requirement. Two other alternative solutions to boost the gain were considered and studied in detail. The first method- to use a cross-coupled current mirror load for the differential pair- seemed to be difficult to stabilize vis.-a-vis. the second method- using a regulated current source as the load. The first method did not seem to provide any obvious advantages over the second one and hence was not pursued further. An analytical approach for the design of the regulated current source was developed to formulate the gain boost provided by it as well as the condition for ensuring stable operation.

As one of the main emphasis of the project, a step-by-step design methodology for the design of the complete two-stage op-amp utilizing the regulated current source for gain-boosting in the first stage was developed. Using the developed methodology an op-amp with 143 dB gain, 8 MHz GBW, 15 nV/$\sqrt{Hz}$ input referred noise was designed in a 0.50 μm 5 V 2P3M standard CMOS process. Most of the performance parameters of the circuit are either better than or comparable to the state-of-art. The complete circuit occupies a total area of $0.16mm^2$ and consumes 630 μW power provided from a 3V supply. The same circuit can operate in low-power mode with upto ten times less power consumption than the high-power mode. Operating in low-power mode, it consumes 69 μW of power and consequently has almost 10 times

lower GBW.

The op-amp thus designed is intended to be used as a pre-amplifier in a sensor interface. Consequently it will always be used in a feedback loop whose gain will be determined externally. Hence, the fact that the transient response of the op-amp in unity gain feedback shows a very small ripple is inconsequential. However, this keeps the scope open for the further detailed study of the circuit to ensure its stability as a buffer too. Alternative design approaches for designing this circuit constraining other parameters like noise (and not just gain) need to be developed. Finally, it would be interesting to study the limits on the performance this circuit architecture can achieve with more advanced process technologies like 0.18μm.

Appendix A

The Cross-Coupled Current Mirror Load

Principle of Operation

The amplifier required in this project targeted for the sensor interfaces needs to have a high gain of the order of 120dB. One of the apparently attractive methods to achieve this gain is to use internal positive feedback in a simple OTA. For a positive feedback structure, the gain G is given as

$$G = A\left(\frac{1}{1-\eta}\right)$$

where A is the forward amplifier gain and η is the loop gain. It can be seen that the positive feedback enhances the gain by the factor $1/(1-\eta)$ if $0 < \eta < 1$.
In the following sections we will first calculate the value of the loop gain and then discuss the consequences of this gain enhancement.

Loop Gain

A simple symmetrical OTA with cross coupled positive feedback load is shown in Fig. A.1. From the circuit,

$$\Delta I_{10} = G_{m10}.\Delta V_{GS10} \tag{A.1}$$

Now, any change in current through transistor M_{10} (ΔI_{10}) will be reflected as the change in current through M_4; the current through M_9 will change

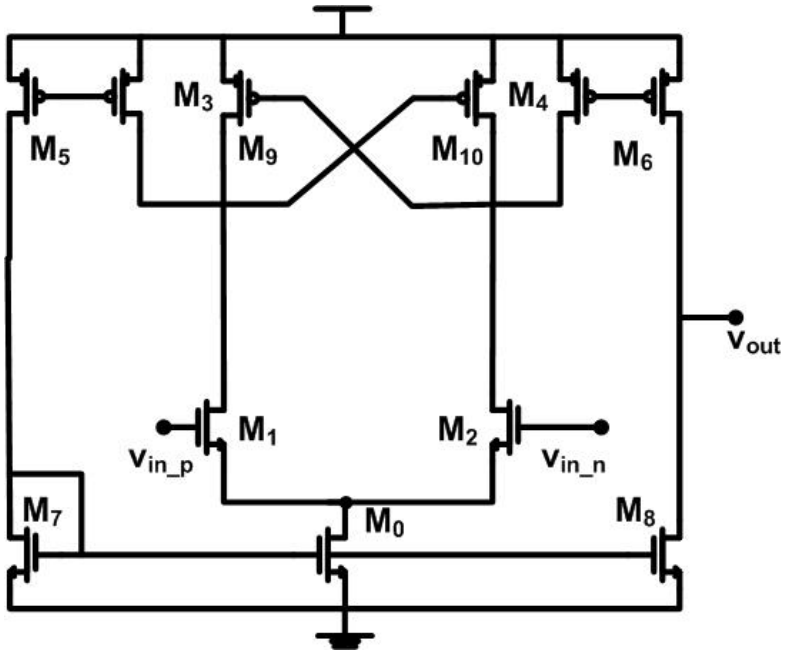

Figure A.1: OTA with cross coupled current mirror load

equally since M_9 forms a current mirror with M_4 and through M_3 which mirrors current through M_{10}. Hence,

$$\Delta I_{10} = \Delta I_4 = \Delta I_9 = \Delta I_3 \tag{A.2}$$

Also,

$$\Delta I_3 = \Delta I_9 = G_{m9}.\Delta V_{GS9} = G_{m9}.\Delta V_{GS4} \tag{A.3}$$

Thus,

$$\Delta I_3 = \frac{G_{m9}}{G_{m4}}.\Delta I_4 = \frac{G_{m9}}{G_{m3}}.\Delta I_{10} \tag{A.4}$$

Therefore, loop gain

$$\eta = \frac{\Delta I_3}{\Delta I_{10}} = \frac{G_{m9}}{G_{m3}} \tag{A.5}$$

Effective Transconductance

For a normal OTA, the gain is given by $G = G_m.R_{load}$. For the OTA with positive feedback, R_{load} remains the same but as already shown in section A, the total gain is enhanced by a factor of $1/(1-\eta)$. This implies that the effective transconductance of the gain stage must be enhanced by the same

factor. Thus, the effective transconductance of the differential gain stage of the OTA with internal positive feedback can be given as

$$G_m = \frac{G_{m1}}{1-\eta} \tag{A.6}$$

where G_{m1} is the transconductance of the input transistor.

Stability Analysis

An undesired consequence of positive feedback is that it can cause instability. As η approaches 1 in equation A.6, the gain of the amplifier approaches infinity and system becomes unstable.
We know that mismatch of transistors causes an offset voltage. Apart from this, the mismatch also causes a mismatch of transconductances, thereby causing a deviation of the effective transconductance. Similarly, the loop gain η which is a ratio of transconducatnces (equation A.5) will also have a deviation. If there is a large variation in η which causes it to approach or exceed 1, the system will become unstable [9]. Thus, for satability
$\sigma_\eta < 1 - \eta$.

The maximum practical gain enhancement using positive feedback is thus limited by the mismatch effect. For a normal distribution and assuming a 3σ criterion, the maximum value of η can be $1 - 3\sigma$. Thus, maximum possible gain enhancement is

$$\frac{1}{1-\eta} = \frac{1}{1-(1-3\sigma)} = \frac{1}{3\sigma} \tag{A.7}$$

From equation A.5

$$\eta = \frac{G_{m9}}{G_{m3}} \approx \sqrt{\frac{I_{F3}}{I_{F9}}} \tag{A.8}$$

assuming M_9 and M_3 are in strong inversion, where I_{Fn} is the inversion factor.
Since $I_F = \frac{I_D}{I_{spec}}$, thus

$${\sigma_\eta}^2 = \frac{1}{4}\eta^2({\sigma_{ID3}}^2 + {\sigma_{ID9}}^2) + {\sigma_{Ispec3}}^2 + {\sigma_{Ispec9}}^2 \tag{A.9}$$

Conclusion

From the above discussion it is clear that the cross-coupled load demands a very careful design and layout to ensure high degree of matching. Even

though the cross-coupled load is an attractive option for obtaining high gain, it falls from favor because of the inherent positive feedback which makes it highly susceptible to instability.

Appendix B

Design Calculations for the 200 μA Amplifier

In this chapter we present the design calculations for the amplifier for the following specifications and constraints by following the design methodology developed in chapter 5:

- Gain, A_{total} = 150 dB
- Gain bandwidth, GBW_{total} = 10 MHz
- Load capacitor, C_L = 10 pF
- Current consumption, I_0 = 200 μA.

We choose a slightly different approach to start the design and begin by choosing the inversion factor (I_c) for the differential pair very close to the edge of weak inversion. We choose

$$I_c = 0.25$$

Thus,

$$\left(\frac{W}{L}\right)_{M_3} = 138.7 \rightarrow 140$$

Now, following the design methodology,

$$C_c = C_L/3 \approx 3pF$$

Being conservative, we allocate I_{0I} = 15μA (<(1/10)*200 μA) bias current to the differential pair. Therefore,

$$g_{m34} = 183.4\mu S$$

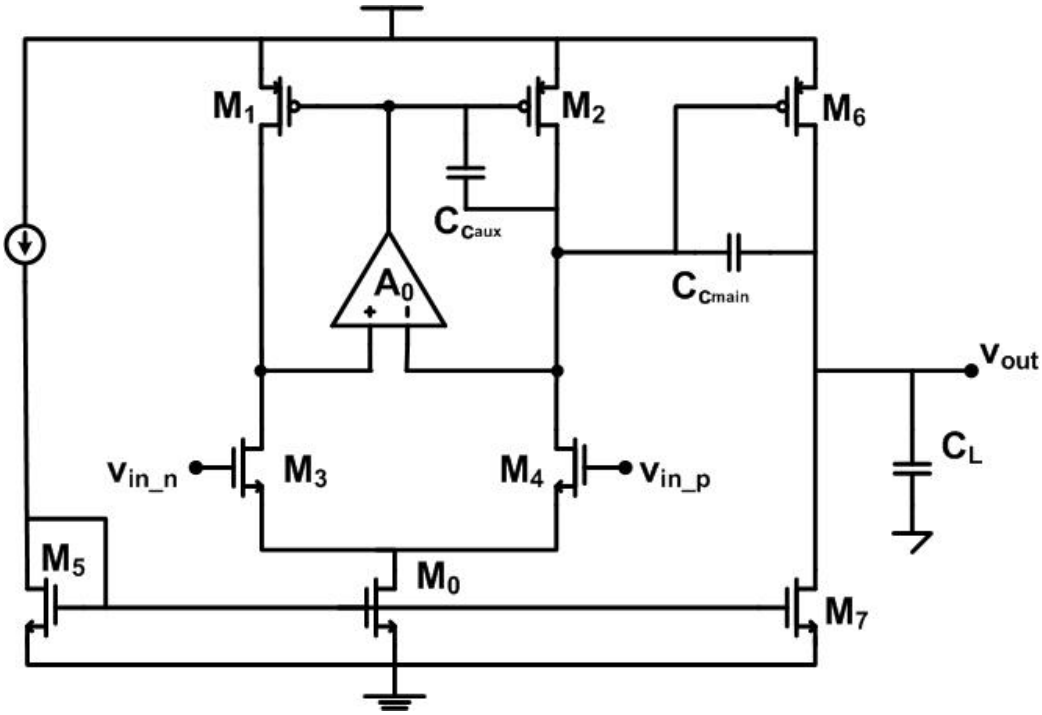

Figure B.1: The complete op-amp

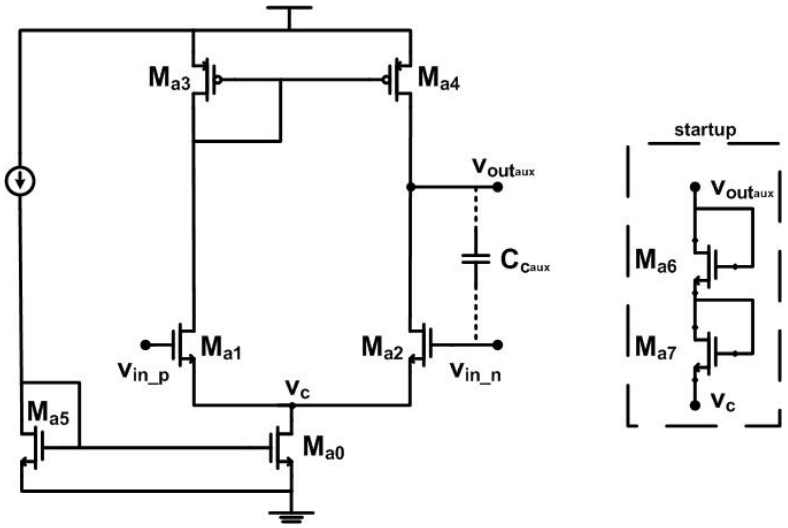

Figure B.2: The auxiliary amplifier

The GBW thus obtained will be

$$GBW_{total} = \frac{g_{m34}}{2\pi\, C_c} = 9.75MHz$$

which is very close to our requirement of 10 MHz. From (5.2)

$$g_{m6} = 1.84mS$$

Referring to step 6 of the design methodology

$$I_6 = 10 * I_{0I} = 150\mu A$$

So,

$$\left(\frac{W}{L}\right)_{M_8} = 491$$

Choosing $L_2 = 1\mu m$ and calculating $L_4 = (K_n/K_p) * L_{12} = 1.2\mu m$, we obtain

$$g_{ds2} = 592.1nS$$

$$g_{ds4} = 643.4nS$$

and the gain provided by the common source second stage as

$$A_{II} = 35.8dB$$

So, we need to obtain approx. 150-35=115 dB from the first stage (A_I). Referring to step 10 of the design methodology

$$A_0.g_{m2} = 4.7mS$$

We allocate 40 dB as the gain of the auxiliary amplifier ($A_0 \approx 150/4$). Thus,

$$g_{m2} = 47\mu S$$

$$\left(\frac{W}{L}\right)_{M_2} \approx 5$$

To design the auxiliary amplifier, we start by calculating the required GBW as

$$GBW_{aux} = 4 * GBW_{total} \approx 40MHz$$

We start by choosing $C_{c_{aux}} = 500fF$ and allocating 20 μA bias current to the amplifier. So,

$$g_{ma12} = 2\pi\, C_{c_{aux}} GBW_{aux} = 125.7\mu S$$

$$\left(\frac{W}{L}\right)_{M_{a1=a2}} = 14.5$$

Using $A_0 = 40dB$ we get

$$g_{ds2} + g_{ds4} = 1.26\mu S$$

Taking $L_2 = 2\mu m$ and $L_4 = 1.2\mu m$ we obtain the required output conductance. We choose the inversion factor for the current mirror load transistors as $I_c = 20$. Thus,

$$\left(\frac{W}{L}\right)_{M_{a3=a4}} = 7.5$$

The current sources are designed for $V_{Dsat} = 200mV$ such that

$$\left(\frac{W}{L}\right)_{M_7} \approx 85$$

Therefore

$$\left(\frac{W}{L}\right)_{M_{0=5}} = 8.5$$

Also,

$$\left(\frac{W}{L}\right)_{M_{a0=a5}} \approx 11$$

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