

A General Purpose FPGA-based Real-Time Simulator for Power Systems Applications

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Abstract-- This paper presents an FPGA-based (field-programmable gate array) real-time digital simulator for power systems and power electronics applications. The proposed approach integrates the Modified Nodal Analysis (MNA) method, the Fixed Admittance Matrix Nodal Method (FAMNM) and multi-conductor transmission line modeling capabilities. In particular, the MNA is used to formulate the electrical circuit equations and the FAMNM for keeping the MNA nodal-matrix constant during switching transitions. The inherent parallel nature of FPGA's computation is exploited by a suitably defined implementation of the simulation approach. The proposed simulator is validated by comparing its results to off-line simulations obtained using the EMTP-RV software. The proposed approach exhibits high computational speed together with excellent accuracy.

Index Terms-- Modified Nodal Analysis, discrete-time switch model, Field-programmable gate arrays (FPGAs), real-time simulation of power system, electromagnetic transients, transmission lines.

I. INTRODUCTION

Real-time digital simulators allow physical imitation of systems behavior by numerically simulating their steady-state and transient conditions. Existing real-time simulators are based on various types of hardware such as: multi-core CPUs, general-purpose processors (GPPS), digital signal processors (DSPs) or computer clusters (e.g. [1]).

The main applications of real-time digital simulators within the field of power systems and power electronics essentially refer to hardware-in-the-loop (HIL) testing applied to: relaying, control of machines and power electronic converters (like Flexible AC Transmission Systems – FACTS, High-Voltage DC converters), or transient studies [2]-[4].

Commercial real-time simulators use parallel simulation of power system networks on PC clusters running QNX or real-time Linux operative systems. These architectures allow the separation of the original model into sub-systems that are solved as parallel tasks [5]. As an example, the RT-LAB platform by Opal-RT utilizes SimPowerSystems (SPS) toolbox of MATLAB to model power system network components whose state-space equations are numerically

integrated with a specific solver (i.e. ARTEMiS [5],[6]). The advantages of this category of solvers are: (i) system separation in tasks solved in parallel, and (ii) pre-calculation of state-space model parameters for different switching states [7]. However, existing real-time simulators are characterized by some drawbacks (e.g. [7], [8]) such as:

- lower-bound limitation of the minimum simulation time-step (i.e., bandwidth upper-bound limitation);
- inherent complexity of the hardware architecture.

Concerning the first point, the main reason limiting the simulation time-step is due to the hardware architecture, mainly based on general-purpose processors or PC clusters. Indeed, general-purpose processors execute instructions essentially in series with a low level of parallelism. As a consequence, the relatively large simulation time steps required by these simulators do not allow to model high frequency phenomena such as electromagnetic transients in power converters or travelling wave transients taking place in short transmission lines.

These limitations have been the main motivation for the introduction of a new category of real-time simulators which makes use of Field Programmable Gate Array (FPGA) hardware (e.g. [1],[8],[9]). Indeed, the use of FPGAs enables parallel implementation methodologies limiting dramatically sequence operations that take place in CPUs. The direct consequence of these advantages is the decrease of the minimum simulation time step to values down to the microsecond range (or even below). Additionally, FPGA-based real-time digital simulators allow the development of portable systems of particular interest for in-situ HIL (e.g., tuning of protections).

Recently, FPGA-based real-time simulators for power system applications have been discussed in the literature. In [1], [10], examples of FPGA-based real-time simulators to study switching electromagnetic transients in three-phase AC electrical machines and power electronics converters have been presented. Classical nodal analysis approach has been used to formulate the electrical network equations whilst switches have been represented by the so-called Associated Discrete Circuit (ADC). Therefore, the system nodal admittance is kept constant during switching transitions

similarly to the FAMNM approach. The proposed methodology has allowed to simulate electrical machines and power electronics converters with a time step in the range of few hundreds of nanoseconds [10].

In [11], an FPGA-based real-time ElectroMagnetic Transient simulator has been proposed for simulating electromagnetic transients in power networks including transmission lines. Employing frequency-dependent line models and the traditional nodal analysis, the proposed simulator allows simulating transmission line transients accurately. However, the proposed approach in [11] does not use FAMNM and, as a result, it has to pre-calculate all the possible values of the system admittance matrix associated with all switch states.

Within this context, this paper proposes an FPGA-based digital real-time simulator based on the combined use of the Modified Nodal Analysis (MNA) applied to networks with multi-conductor transmission lines, together with the FAMNM approach for the switches representation [9],[12]-[13]. The proposed simulator is implemented on the National Instruments Compact-Rio hardware platform where a Xilinx Virtex-5 LX-110 FPGA has been used.

The structure of the paper is as follows: Section 2 describes the theoretical background of the proposed real-time solver. Section 3 describes the implementation into the real-time FPGA-based hardware platform. Section 4 illustrates the validation of the proposed method by means of specific comparison with off-line results obtained using the EMTP-RV simulation environment [14],[15]. The simulated cases refer to electromagnetic transients associated with faults on multiconductor transmission line networks. Conclusions are presented in Section 5.

II. THEORETICAL BACKGROUND FOR POWER SYSTEM TRANSIENTS SIMULATION

A. Network Solutions Methods

Generally, there are two main types of solution methods currently used in the field of power system, power electronics and electronic circuit simulations [16]: (i) MNA and (ii) State-Space (SS) approach. The main advantage of the SS method is its ability of considering variable time-step numerical integration techniques. However, the formation of state matrix is not as straightforward as for the nodal admittance matrix used in MNA-type methods. On the other hands, fixed time-step numerical integration techniques are required in MNA [16]. As the paper deals with the use of FPGA-based hardware platforms, fixed time-step solvers are preferred as FPGAs work with fixed clock speed rates and, usually, elaborate signals which are sampled at a fixed frequency. Therefore, in what follows we will only make reference to the use of the MNA combined with backward Euler numerical integration technique. The MNA formulation is given by equation (1) [17]:

$$[A_n][x_n] = [b_n] \quad (1)$$

where matrix $[A_n]$, in the discrete time domain, is formed by the discrete representation of the network elements; $[x_n]$ is the vector of unknown network's node voltages and branch currents; and $[b_n]$ is a vector composed of the independent sources and current history terms related to the network components. For each iteration, the unknown vector $[x_n]$ is calculated and, then, the vector $[b_n]$ is updated.

B. Numerical integration method

There are several numerical integration methods that can be applied to solve differential equations. Among them, forward Euler, backward Euler and the trapezoidal methods are the most common in power system applications [18]. The trapezoidal integration technique is used for the numerical integrator substitution, due to its simplicity, stability and reasonable accuracy in most circumstances. However, being based on a truncated Taylor's series, the trapezoidal rule can cause numerical oscillations under certain conditions due to the neglected terms [17]. In comparison to the trapezoidal method, backward Euler rule gives better damping to numerical oscillations introduced by switches [12]. In this paper, we have adopted the backward Euler method.

C. Network Components Models

In view of the use of the MNA, all the relevant network components should be discretized to form the so-called nodal equations. In [17],[19], the digital solution of electromagnetic transients in power systems and, more generally, in electrical circuits, has been introduced.

As well-known, while the behavior of power system variables is continuous in time, this approach introduces the concept of "discrete solution". Namely, the solution of the electrical circuits' differential equations is obtained in discrete time steps. Thus, models of system elements should be formulated by means of their discrete representation. To this end, lumped elements (RLC) are represented by their discrete companion model that is composed of an equivalent resistance in parallel with a current source indicating the history terms (e.g., [19],[20]). The values of the equivalent resistance and the current source are determined based on the applied numerical integration method.

Concerning the case of transmission lines, one of the most popular solutions are given by the so-called Bergeron model [21],[22]. It allows a straightforward representation of constant (frequency-independent) transmission line models and, with some adaptations, it can also be applied to the case of frequency-dependent transmission lines [23]. As well known, this approach is based on a circuit representation of the telegraphers' equations where each line termination is replaced by means of a lumped impedance in parallel with a controlled-current or -voltage source.

For the case of multi-conductor transmission lines, by making reference to the modal analysis, it is possible to transform the telegraphers' equations from the phase domain to the modal domain. This allows the decoupling of the multi-

conductor equations so they could be solved in a simple, scalar manner. To this end, transformation matrices $[T_v]$ and $[T_i]$ can be defined in order to transform the phase voltages and currents to the corresponding modal ones [22]:

$$[v_p] = [T_v][v_m] \quad (2)$$

$$[i_p] = [T_i][i_m] \quad (3)$$

where, $[v_m]$ and $[i_m]$ are time-domain modal voltages and currents, and $[T_v]$ and $[T_i]$ are the transformation matrices for phase voltages and currents, respectively [22].

D. Switch model

In order to take advantage of the FAMNM, the adopted method for modeling switches is based on the discrete circuit model presented in [9],[12]. Such a model assumes that the equivalent of the ideal switch is piecewise linear and the relevant model is composed of a constant conductance and a current source (see Fig. 4). As a function of the switch on/off state, the value of the current source is updated at each time step based on the switch current/voltage. The advantage of this method is that the value for the switch conductance G_s is fixed irrespective of the switch on/off state. As a result, the nodal admittance matrix will remain unchanged during switching operations as the switch state only affects the value of the shunt current source. The current source associated with the switch at the simulation step $n+1$ is defined as [12]:

$$J_s^{n+1} = \begin{cases} -i_s^n & \text{for the 'on' state} \\ G_s v_s^n & \text{for the 'off' state} \end{cases} \quad (4)$$

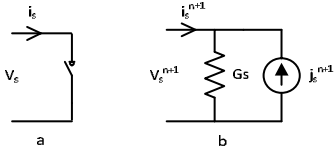


Fig. 1. Ideal switch (a) and discrete-time model (b). Adapted from [12].

Although this method is computationally highly efficient, it introduces artificial parameters (i.e., G_s) into the circuit that do not exist in reality. An example of how the influence of these parameters can be minimized has been discussed in [24].

E. Methodology

After representing all system components by their discrete time models, system nodal equations are formed based on the MNA approach. In other words, a solution of (5) can be written as:

$$[A][x] = [b] \Rightarrow \begin{bmatrix} a_{11} & a_{12} & \dots & a_{1n} \\ a_{21} & a_{22} & \dots & a_{2n} \\ \dots & \dots & \dots & \dots \\ a_{n1} & a_{n2} & \dots & a_{nn} \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \\ \dots \\ x_n(t) \end{bmatrix} = \begin{bmatrix} b_1(t-l\Delta t) \\ b_2(t-l\Delta t) \\ \dots \\ b_n(t-l\Delta t) \end{bmatrix} \quad (5)$$

where, $[x]$ is the vector of unknown nodal voltages (both phase and modal domains) and branch currents (both phase

and modal domains), and $[b]$ is the vector of injected currents including the current sources for history terms of discrete circuit components. For the case of injected currents $l=0$, for lumped elements $l=1$, and for transmission lines $l=p_m\Delta t$ (where $p_m\Delta t$, with $p_m \in \mathbb{N}$, represents the propagation time of the mode m of a given transmission line of the system). It is worth mentioning that for the case of transmission lines where $p_m \notin \mathbb{N}$, the interpolation method based on [25] has been implemented.

In addition, voltage and current transformation matrices ($[T_v]$ and $[T_i]$) are included in Matrix $[A]$. Equation (5) can be separated in two parts: one containing the unknown node voltages and branch currents (k elements), and a second containing the set of phase-to-modal transformations (h elements):

$$\begin{bmatrix} [a_{ii}]_{k \times k} \\ [T_{v,i}]_{h \times n} \end{bmatrix} \begin{bmatrix} [x_i]_{k \times n} \\ [x_j]_{h \times n} \end{bmatrix} = \begin{bmatrix} [b_i]_{k \times n} \\ [0]_{h \times n} \end{bmatrix} \quad (6)$$

In (6), $[a_{ii}]$ is the sub-matrix including admittances and extra rows for additional variables, and $[T_{v,i}]$ is the sub-matrix including phase-to-modal transformation matrices. Basically, the solution of the network variables corresponds to the solution of the linear equation (6) given by:

$$\begin{bmatrix} [x_i]_{k \times 1} \\ [x_j]_{h \times 1} \end{bmatrix} = \begin{bmatrix} [a_{ii}]_{k \times n} \\ [T_{v,i}]_{h \times n} \end{bmatrix}^{-1} \times \begin{bmatrix} [b_i]_{k \times 1} \\ [0]_{h \times 1} \end{bmatrix} \quad (7)$$

It can be seen that h elements of vector $[b]$ are zeroes. Therefore, h columns of $[A]^{-1}$ can be removed and (7) can be reduced to:

$$[x_i]_{n \times 1} = [H]_{n \times (n-h)} \times [b_i]_{(n-h) \times 1} \quad (8)$$

where matrix $[H]$ is the reduced $[A]^{-1}$ matrix by eliminating its h columns.

III. IMPLEMENTATION OF THE MNA INTO AN FPGA-CHIP FOR REAL-TIME SIMULATIONS

A. System Configuration

The hardware chosen to deploy the FPGA real-time simulator is the National Instruments Compact-Rio platform. It is a real-time embedded hardware that couples a microcontroller with a user-programmable FPGA coupled with I/O boards. The adopted Compact-Rio system and its architecture are shown in Fig. 2. Specifically, we are using the NI 9118 FPGA chassis that implements the Xilinx Virtex 5 LX 110 FPGA.

The Compact-Rio microcontroller is used to perform the inversion of matrix $[A]$ and to transfer to the FPGA the simulation parameters, switch states and matrix $[H]$. A high-speed A/D conversion module, with a sampling rate of 1 MHz, has been used to provide real inputs to the FPGA solver. At time step Δt , the FPGA performs the computation of (8) and updates the history terms in $[b]$.

After the computation of (8), all needed network variables

are transferred to memory blocks in order to be monitored by the user-interface.

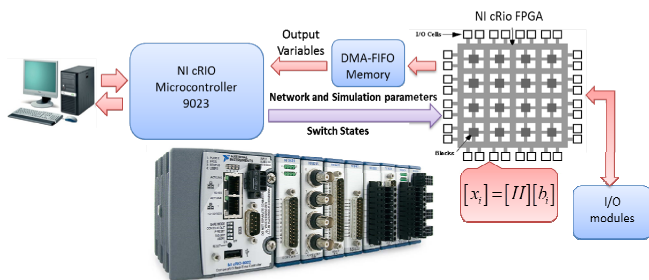


Fig. 2. FPGA-based real-time simulator architecture.

B. FPGA Implementation

As previously mentioned, the FPGA is the computational engine of the developed real-time simulator. In such a system, both sequential and parallel tasks are executed. In particular, the sequential tasks are: (i) injected currents calculation and history terms update, (ii) solution of (8), (iii) data storage into memories implementing different time delays for transmission line variables.

Parallel operations take place at each step. In particular, in the first stage, the vector of injected currents is formed and this operation is done with the update of all the elements by using parallel FPGA blocks.

In the second stage, equation (8) is solved by using the backward-Euler integration method. Each element of $[x]$ in (8) is computed as the sum of dot-products of elements in the corresponding row of matrix $[H]$ times $[b]$, namely:

$$x(i) = \sum_{j=1}^{n-h} H(i, j)b(j) \quad (9)$$

Equations (9) are computed by the FPGA independently and in parallel for each $x(i)$. Additionally, each embedded multiplication and summation in (9) is performed by using a user-defined number of adders and multipliers. As a result, one computational unit (CU in Fig. 3) could be considered for each element of $[x]$ (i.e. $CU(i)$). Each CU is therefore composed of a pre-defined number of parallel multipliers and adders.

In the third step, transmission lines variables are saved in specific memory blocks. These stored variables will be used to update the elements of $[b]_{k \times n}$ that correspond to transmission lines. Concerning the history terms of lumped elements and switches, one time step delay could be applied by using one simulation iteration delay. The flowchart of the implemented algorithm is shown in Fig. 3.

IV. APPLICATION EXAMPLES

In this section, we present a validation of the proposed real-time simulator by making reference to off-line simulations performed within the EMTP-RV simulation environment. For the sake of conciseness, only one case is presented here. It corresponds to fault transients at one end of a 30-km long, three-conductor transmission line. The line is assumed to be terminated at both ends on power transformers

which, for fault-originated traveling waves characterized by a spectrum with high-frequency components, are represented by high input impedances (20 k Ω resistors) associated with their dominant capacitive behavior [26]. The line geometrical parameters correspond to the typical 230 kV transmission lines. A schematic representation of the system is shown in Fig 4 where V_a , V_b , and V_c are voltages on each conductor of the transmission line at its left end.

The same system of Fig. 4 has been simulated in the EMTP-RV where the transmission line has been modeled by means of a constant-parameter (CP) model [22]. To examine the performance of the implemented real-time simulator, a phase-to-ground fault is considered to occur on phase 'a' at the end of the line, represented by the switch S3.

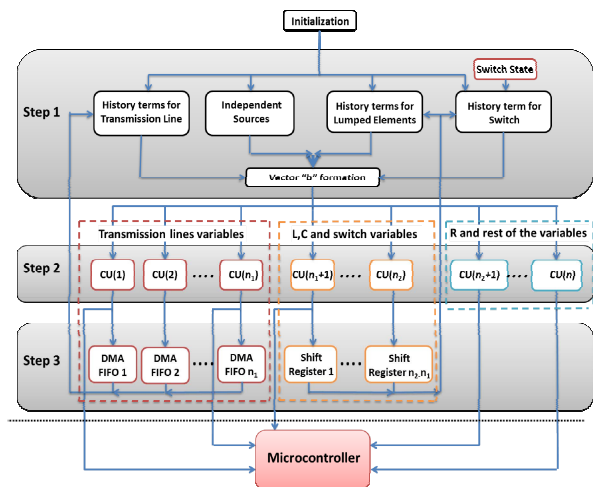


Fig. 3. The flowchart of implemented algorithm in FPGA.

The fault impedance was assumed to be zero. The fault-generated transient signals are recorded at the left-end observation point, on each phase, as shown in Fig. 4.

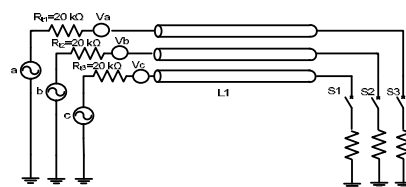


Fig. 4. Schematic representation of system under study.

Fig. 5 shows the computed transients using the proposed approach and their EMTP-RV counterparts. The results provided by the proposed FPGA real-time simulator are in excellent agreement with those obtained by offline simulations. The execution time for simulation of such a system including the reading analog inputs, solving the system nodal equations, and sending the outputs, is 4 μ s.

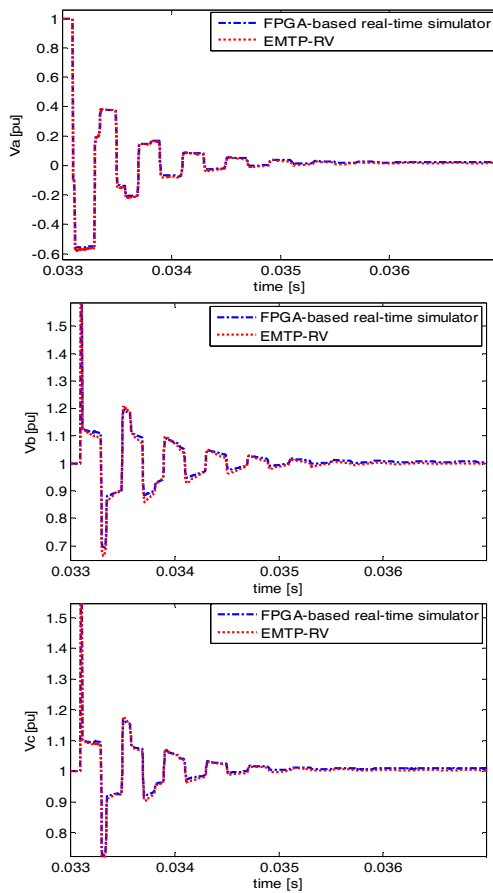


Fig. 5. Comparison of the three-phase voltages obtained by real-time simulations with offline simulation results obtained using EMTP-RV.

V. CONCLUSION

In this paper, an integrated MNA-FAMNM-transmission line FPGA-based real-time simulator was presented. The proposed simulator was implemented in the FPGA of the National Instruments Compact-Rio real-time hardware platform. The main feature of FPGA is exploited by parallelizing the implemented algorithm to solve the MNA-FAMNM equations. The method for modeling switches enabled to keep the MNA matrix constant during switching transitions and, consequently, by skipping the matrix manipulation operations after switching transitions. A comparison with off-line EMTP-RV simulations showed an excellent agreement together with high computation efficiency.

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