24 GHz LNA and Vector Modulator Phase Shifter for Phased-Array Receiver in CMOS Technology

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***Abstract*—With the rapid development of the applications in short range communication, phased-array receiver working at 24 GHz can provide enhanced gain performance at desired transmission direction. Also there is the wide signal bandwidth, i.e. 250 MHz free licensed spectrum at this frequency. In the phased-array front-end, the key component is the phase shifter, which decides the tuning resolution of beam-forming. The challenge of the design work comes from the low-power, low-noise and low-cost requirement. This paper explores the design procedure of a Vector Modulation Phase Shifter (VMPS), consisting of a 90° hybrid, a variable gain amplifier and the Wilkinson combiner. The variable gain amplifier is fabricated in 90nm complementary metal-oxide-semiconductor technology, and the passive hybrid and the Wilkinson combiner are designed on the printed circuit board with RO4003 substrate. After combining the measurement results of each block, the VMPS shows 45° phase shifts with 7° phase error, and 9 mW consumption.**

I. Introduction

The 24 GHz Industrial Scientific Medical (ISM) band is accepted worldwide for Short Range Communication (SRC) and for the radio determination: detection, movement and alert applications [1], [2] and [3]. The Phased-Array (PhA) principle can be applied to add functionalities and improve performances. For example, the beam steering functionality can be exploited by short range devices for interference mitigation and to focus the antenna pointing towards the desired transmitter/receiver. In the radio determination application, the beam steering technique can be used to scan the environment to improve the spatial resolution of the sensor. The relative wide bandwidth, i.e. 250 MHz, allows the relatively high capacities of the data throughput.

Moreover, SRC and sensors often require low power consumption and miniaturization. Therefore, the implementation of Phased-Array Front-End (PhA-FE) using the latest scaled CMOS technologies, ex. 90 nm, is the key point for a low-cost and mass diffusion of these devices.

The challenge of developing such a PhA-FE is related on following aspects: 1) The accuracy of the phase tuning decides the resolution of the system and the pointing direction of the transmission wave. 2) The low-power performance determines the efficiency of the mobile device, which has to be acceptable under the satisfaction of the noise and gain requirements. 3) The parasitic effects are introduced from the circuit and layout design. To avoid or release the potential parasitic effect, the usual way is to optimize the layout design with short RF connections and matched architectures. In our work, we also put ground grids on the first metal layer and also some sensitive parts of other metal layers to decrease the parasitic inductance to the silicon substrate.

In this paper, we report the implementation of two blocks: Low Noise Amplifier (LNA) and Vector Modulation Phase Shifter (VMPS) that are the basic elements of a local oscillator PhA architecture. The single stage LNA is fabricated in 90nm Complementary Metal-Oxide-Semiconductor (CMOS) technology, and it shows 6.5 dB gain, 3.2 dB simulated noise figure, with consumption of 4.3 mW. The VMPS consists of a 90° hybrid, a Variable Gain Amplifier (VGA) and the Wilkinson combiner. The VGA is derived from the LNA design, and also fabricated in 90nm CMOS technology. Passive blocks, i.e. hybrid and combiner are manufactured separately on the Printed Circuit Board (PCB) with hydrocarbon fiber glass (RO4003) substrate. With S-parameter measurement results, the VMPS has been set up in the simulation tool. It shows 45° phase shift resolution with 7° phase error, and 9 mW consumption.

II. Circuit blocks

The local oscillator PhA architecture, shown in Fig. 1, has been selected for its efficiency and versatility as stated in our previous work, [4] and [5].

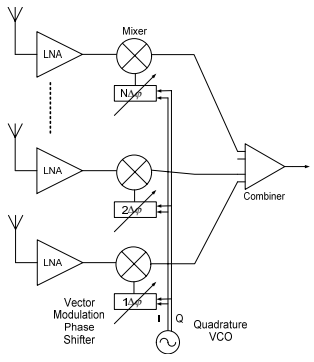


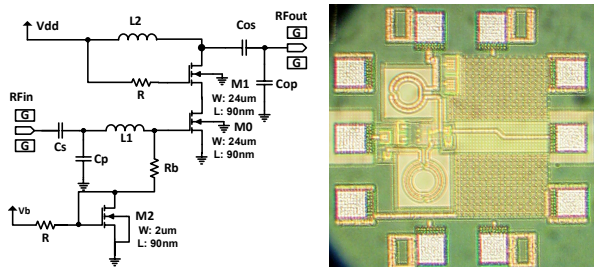
Fig. 1: Local oscillator phased-array architecture

In the receiver architecture, at each signal branch, the LNA is placed following at the receiving antennas. At Local Oscillator (LO) path, the VMPS controls the phase of the carrier frequency signal, in order to compensate phase delay from the receiving signal. After mixing with the RF paths, signals from each branch combine together and flow to the back-end.

The following sections will present the block development of the single stage LNA, the VGA and the VMPS. LNA constitutes the base element of a VGA, which is in turn the basic block of the VMPS. As mentioned in the introduction, VMPS consists two VGAs, a 90° hybrid and a Wilkinson combiner. The last two components are designed and fabricated on PCB. Finally, the performance of the VMPS has been simulated by using the measured S-parameters of all blocks.

A. Low Noise Amplifier

The LNA uses typical cascode structure to carry out the maximum gain from the single stage amplifier, seen in Fig. 2(a). The degenerative inductance on the source is abandoned to preserve gain, and also because a little degeneration is present due to the parasitic inductance in the chip layout. From the measurement, it shows 6.5 dB gain drawing only 3.6 mA at 1.2 V. The input return loss is -15 dB, as shown in Fig. 3. The simulated noise figure is 3.2 dB. Table. I shows the performance comparison with the state of the art. All of the works listed are common-source single-end LNA.



(a) Schematic of 1st-stage LNA (b) Die photo of 1st-stage LNA

Fig. 2: Schematic and the Die photo of the LNA

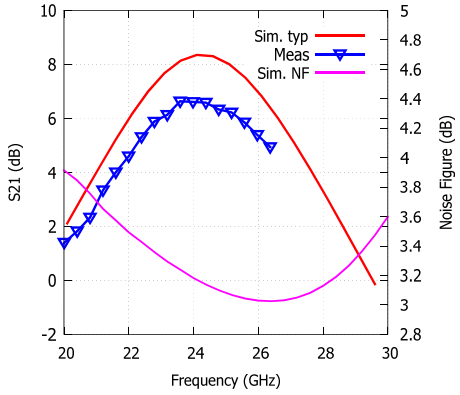
TABLE I: Comparison of the 24 GHz LNA performances.

Reference	[6]	[7]	[8]	This work
Frequency (GHz)	24.0	24.0	24.0	24.0
Technology (nm)	90	130	90	90
Gain (dB)	7.5	19[a]	15.2[a]	6.5
Input matching (dB)	-16	-16	-12	-15
Noise Figure (dB)	3.2	3.8	2.9	3.2[b]
Power Cons. (mW)	10.6	15	9.1	4.3

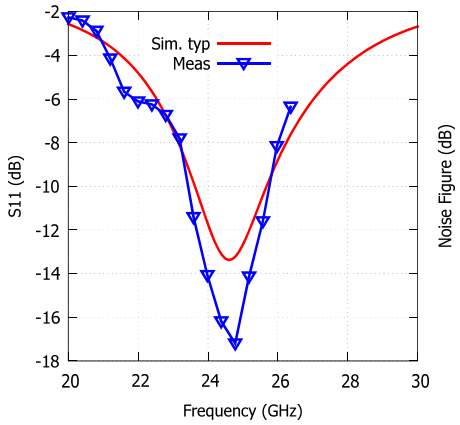
a Two-stage *b* Simulated

B. Variable Gain Amplifier

The design of the VGA has derived from the LNA scheme. Fig. 4(a) shows the modification on the two groups of upper MOSFETs of the cascode: M1 and M3 connected to the resonant load; M2 and M4 connected to the power supply. The amplifier gain is controlled by steering the current between two groups of MOSFETs. In each group, there are two MOSFETs, which can implement 2-bit tuning (three meaningful states), limited by our probe station capabilities. The maximum gain state is obtained when G0 and G1 are low, so that M2 and M4 are biased for the same current as M0, while M1



(a) Simulated and measured LNA gain



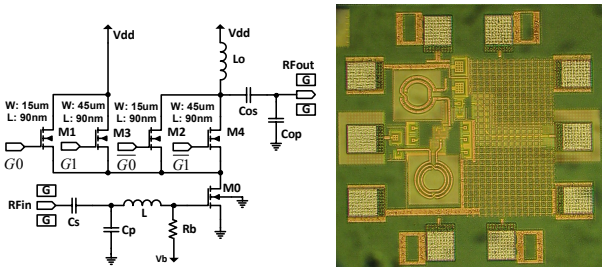
(b) Simulated and measured LNA return loss

Fig. 3: Simulated and measured results of 1-stage LNA.

and M3 are switched off. Half gain state is obtained when G1 is high and G0 is low. When G0 and G1 both are high, the circuit shows the isolation state. In this way the control scheme is scalable over the number of bits. Without considering the measurement limitations, the VGA can be designed for 5-bit phase tuning by splitting the total width of one group (ex. M2+M4) of transistors to 5 pairs, i.e. 30, 15, 7.5, 3.25 and 3.25 um. With this current steering techniques, the input impedance is kept constant over the amplifier gain, contributing to the phase accuracy of the phase shifter. The photo of the VGA chip is shown in Fig. 4(b) and the size of the chip is 0.3 mm×0.15 mm, and 0.6 mm×0.6 mm including the pads. The measured VGA can obtain 5.9 dB of maximum gain and 3.1 dB half gain, illustrated in Fig. 5(a). Thanks to the balanced current steering scheme, at different states, phases are stable, ex. at 24.1 GHz, the phase difference is 5°. The power consumption is 4.5 mW, with the supply voltage 1.2 V. Table. II shows the comparison of our work with the state of the art.

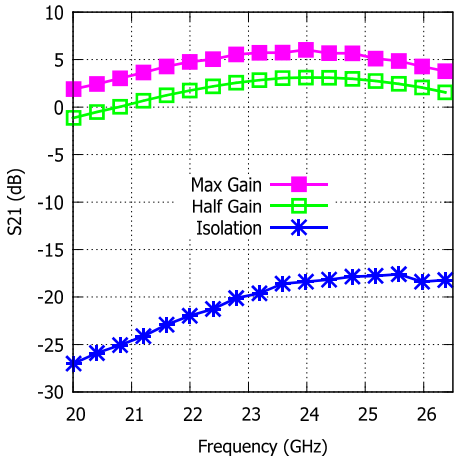
C. Vector Modulator Phase Shifter

The architecture of the VMPS is shown in Fig. 6. The first stage is the 90° hybrid, which generates the quadrant input signals. Hence, the amplitude of the I and Q paths are controlled by the VGA described in Section II-B. And the

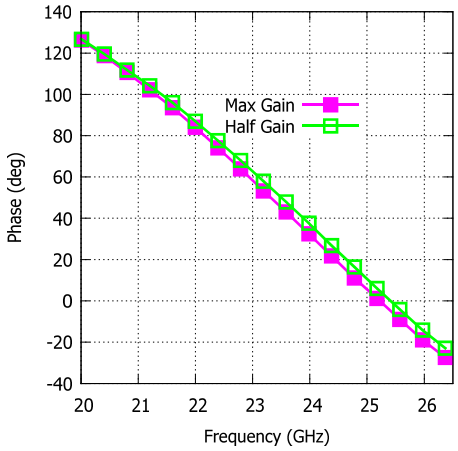


(a) Schematic of VGA (b) Die photo of VGA

Fig. 4: Schematic and the die photo of the VGA.



(a) VGA measured gain for programmed states



(b) VGA measured phase for programmed states

Fig. 5: VGA measurement results.

TABLE II: Comparison of the measured results of the VGA

Reference	[9]	[10]	[11]	This work
Technology (nm)	90	180	130	90
Frequency (GHz)	4.93	21	26	23.8
Max. Gain (dB)	12.2	3	5	5.9
Tuning states (bit)	6	3	4	2
Power Cons. (mW)	28	112	4.5	4.5

weighted components are added by means of a Wilkinson combiner.

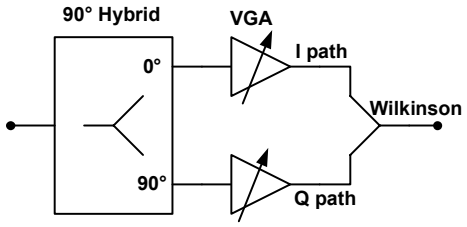


Fig. 6: VMPS scheme used in the simulation

TABLE III: Performance comparison of VMPS

Reference	[12][a]	[13]	[14]	This work
Frequency (GHz)	24	24	60	24.125
Technology (nm)	130	130	90	90[c]
Tuning res. (°)	25	22.5	11.25	45
Gain (dB)	-2	-3	9	-4.2[d]
Phase Imbalance (°)	N/A	11[b]	3	7
Gain Imbalance (dB)	3	1.8[b]	N/A	0.36
Total Power Cons. (mW)	21.36	11.7	60	9

a Simulation results. *b* RMS error.
c Not integrate in one chip. *d* Average gain among three states.

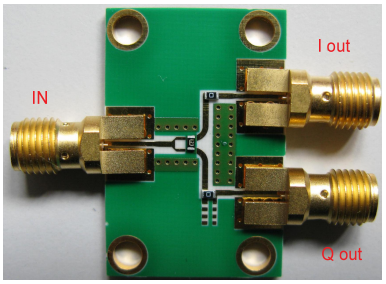
The 90° hybrid, shown in Fig. 7(a), is derived from the Wilkinson combiner adding a 90° length transmission line in one path. The measured S-parameters of this structure are shown in Fig. 7(b). The phase difference between its outputs has been designed as 90° with less than 2° of imbalance. The insertion loss has less than 0.5 dB imbalance. The Wilkinson combiner, after the VGAs, shows 5 dB insertion loss and a perfect phase matching of two branches. Both passive blocks are fabricated on the low-loss Rogers RO4003 substrate.

The state with maximum gain on I path and isolation on Q path is taken as the reference, therefore, when the VGA at I path is set to isolation state, while the VGA at Q path reaches full gain, the combined signal should show 90° phase shift, and if both VGAs are at half gain states, the output signal should get 45° phase shift.

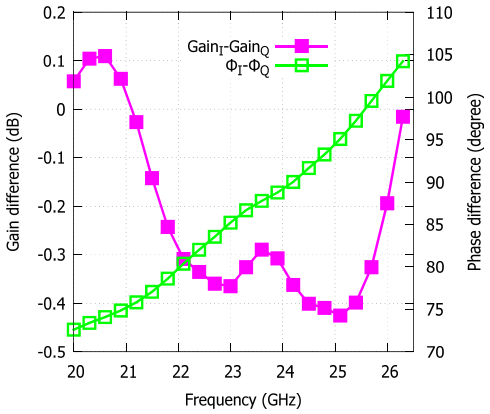
The simulation of the overall VMPS has been implemented in Advanced Design System software environment, based on the measured S-parameters of each block in Fig. 6. In Fig. 8(a) and 8(b), the resulting gain imbalance is within 1 dB at 24.13 GHz over the other two programmed states (45° and 90° phase shift). For the phase difference, it can be distinguished that 45° phase shift has been set between each state, with 6.9° and 3.2° phase error respectively. The comparison of our work with the state of the art is presented in Table. III.

III. Conclusion

The developed blocks are suitable for a low-power implementation of the PhA-FE as shown in the comparison with the state-of-the-art. The evident power saving does not sacrifice much other performances. Indeed, for the LNA, a good noise figure and input return loss are achieved and the gain is within 1 dB with the other single stage LNA reported in Table I. Also the VGA shows the minimum power consumption while keeping good gain, as shown in Table II. Finally, in



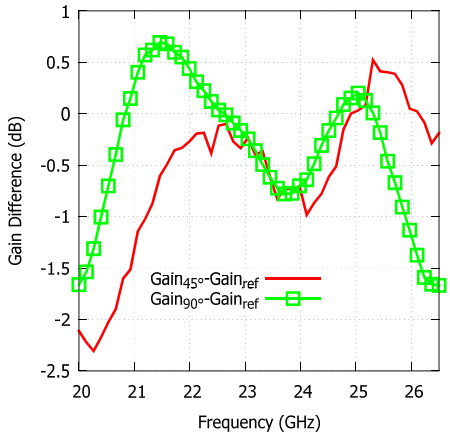
(a) Photo of the 90° hybrid board



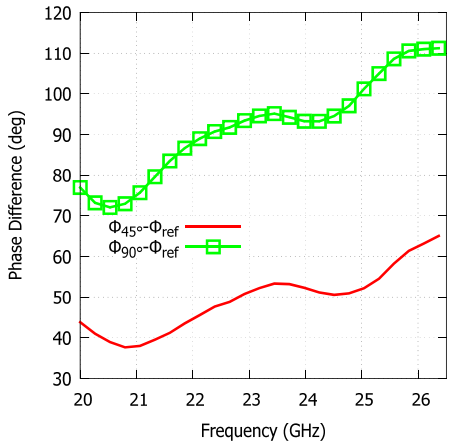
(b) Measured gain and phase imbalance

Fig. 7: 90° hybrid and its imbalance measurement results.

Table. III, our VMPS gets best gain imbalance and profits from the lowest consumption among other three works. As stated above, the number of the tuning bits is limited for test purpose. However, considering the transistor splitting and current steering techniques, with phase accuracy less than 7°, it is sufficient to develop a VMPS more than 5-bit resolution.



(a) Gain difference between programmed states



(b) Phase difference between programmed states

Fig. 8: VMPS simulation performances. Gain and phase variation both relative to the reference state (I max., Q iso.).

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