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# Mobility engineering and a metal–insulator transition in monolayer $MoS_2$

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**Two-dimensional (2D) materials are a new class of materials with interesting physical properties and applications ranging from nanoelectronics to sensing and photonics. In addition to graphene, the most studied 2D material, monolayers of other layered materials such as semiconducting dichalcogenides $MoS_2$ or $WSe_2$ are gaining in importance as promising channel materials for field-effect transistors (FETs). The presence of a direct bandgap in monolayer $MoS_2$ due to quantum-mechanical confinement allows room-temperature FETs with an on/off ratio exceeding $10^8$. The presence of high-κ dielectrics in these devices enhanced their mobility, but the mechanisms are not well understood. Here, we report on electrical transport measurements on $MoS_2$ FETs in different dielectric configurations. The dependence of mobility on temperature shows clear evidence of the strong suppression of charged-impurity scattering in dual-gate devices with a top-gate dielectric. At the same time, phonon scattering shows a weaker than expected temperature dependence. High levels of doping achieved in dual-gate devices also allow the observation of a metal–insulator transition in monolayer $MoS_2$ due to strong electron–electron interactions. Our work opens up the way to further improvements in 2D semiconductor performance and introduces $MoS_2$ as an interesting system for studying correlation effects in mesoscopic systems.**

Molybdenum disulphide ($MoS_2$) is a layered transition-metal dichalcogenide semiconductor[1] with potential applications that could complement those of graphene. As neighbouring layers in transition-metal dichalcogenide crystals are weakly bound through van der Waals interactions, single atomic crystals composed of one or several layers can be extracted using the micromechanical cleavage technique[2] or liquid-phase exfoliation[3,4]. Large-area $MoS_2$ can also be grown using techniques such as chemical vapour deposition[5,6]. The strong covalent bonding between metal and chalcogenide atoms results in a high mechanical strength[7] of $MoS_2$ membranes[8] and electrical breakdown current densities at least 50 times higher than in copper[9]. In contrast to graphene, the presence of a bandgap in monolayer $MoS_2$ and other semiconducting dichalcogenides allows the fabrication of transistors that can be turned off and used as switches[10]. Logic circuits[11] and amplifiers[12] with high gain based on monolayer $MoS_2$ have also been demonstrated, and superconductivity in 20-nm-thick $MoS_2$ was achieved at high electron concentrations using ionic-liquid gating[13].

Monolayer $MoS_2$ has electronic and optical properties that are fundamentally different from those of thicker layers owing to quantum-mechanical confinement[14,15]. Bulk $MoS_2$ is an indirect gap semiconductor whereas single-layer $MoS_2$ has a direct gap[14–17]. The lack of inversion symmetry results in strong coupling of spin and valley degrees of freedom[18–20] and could be used in devices based on the valley Hall effect[21]. The atomic-scale thickness (6.5 Å) of monolayer $MoS_2$, smaller than the screening length, also allows a large degree of electrostatic control over the electrical conductivity. Together with the absence of dangling bonds, this would allow transistors based on monolayer $MoS_2$ to outperform silicon transistors at the scaling limit[22,23].

Previous measurements have shown that the room-temperature mobility of bulk $MoS_2$ is in the 200–500 $cm^2\,V\,s^{-1}$ range and is limited by phonon scattering[24]. Exfoliation of single layers onto $SiO_2$ results in a decrease of mobility down to the 0.1–10 $cm^2\,V\,s^{-1}$ range[2,10]. Charge traps[25] present at the interface between the substrate and the $MoS_2$ layer have recently been proposed as the dominant cause for such low room-temperature mobility in $MoS_2$ devices. Understanding the origin of this mobility degradation and finding a way to restore the mobility to bulk values or even further enhance it would allow us to unlock the full technological potential of this material.

The encapsulation of monolayer $MoS_2$ in a high-κ dielectric environment[26] was shown to result in an increase of the room-temperature mobility[10]. This was tentatively assigned to reduced Coulomb scattering due to the high-κ dielectric environment[26] and possible modification of phonon dispersion in $MoS_2$ monolayers. An increase of mobility with the dielectric deposition, similar to that in monolayers, was also observed in multilayer samples[27,28] and monolayer samples with polymer gating[29]. Previous mobility estimates for monolayer $MoS_2$ are however based on two-contact measurements and lack the information on their temperature dependence. More accurate measurements are needed to gain a better understanding of the various mechanisms that could limit the mobility in monolayer $MoS_2$. In the phonon-limited high-temperature part, the mobility is expected to follow a $\mu \sim T^{-\gamma}$ temperature dependence with $\gamma = 1.69$ and mobility reaching a room-temperature value $\sim$410 $cm^2\,V\,s^{-1}$ according to first-principles calculations[30]. The deposition of a top-gate dielectric is expected to mechanically quench the homopolar phonon mode and reduce the coefficient $\gamma$ to 1.52.

Here, we report on mobility measurements in monolayer $MoS_2$ based on the Hall effect. This allows us to remove the effect of contact resistance and also directly measure the gate-modulated charge density and gate capacitance necessary for the accurate measurements of the field-effect mobility. Our devices are FETs in single- and dual-gate configurations shown in Fig. 1. Degenerately doped Si wafers covered with 270 nm thermally grown $SiO_2$ serve as the substrate and back-gate. $MoS_2$ flakes are shaped into Hall bars using oxygen plasma etching. A 30-nm-thick $HfO_2$ layer deposited

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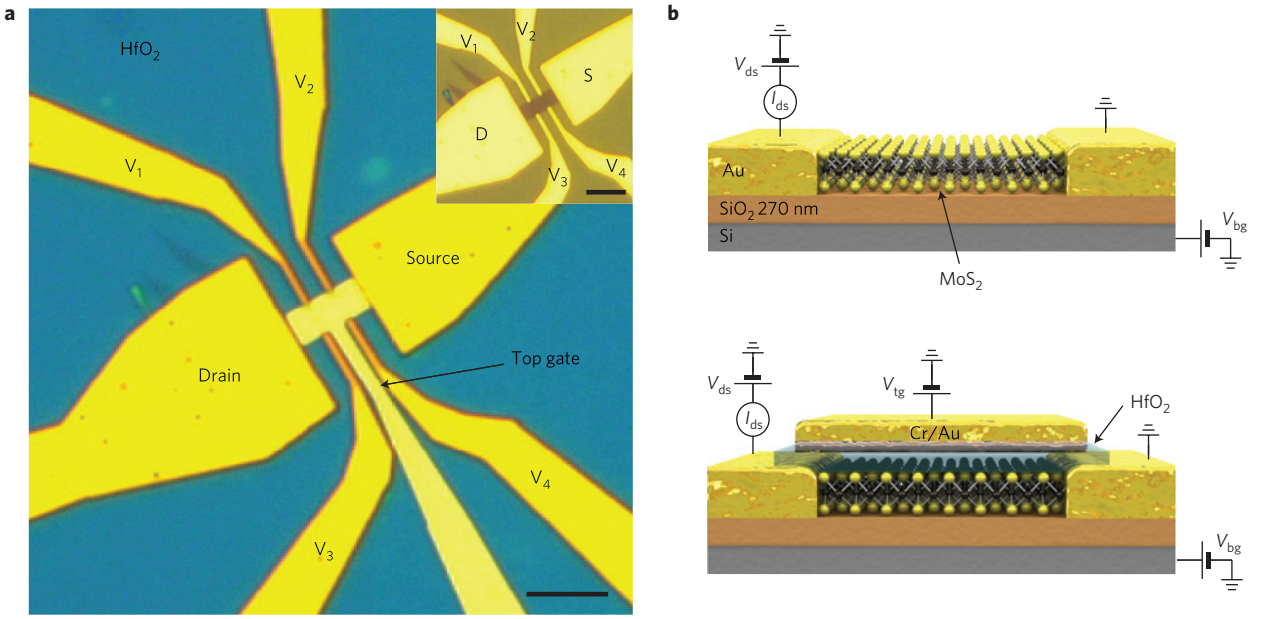


**Figure 1 | Fabrication of single-gated and dual-gated $MoS_2$ devices. a**, Optical image of the $MoS_2$ dual-gated device used in our measurements. The inset shows the single-gate version of the same device before ALD deposition of $HfO_2$ and top-gate electrode fabrication. Scale bars, 5 μm. **b**, Cross-sectional views of devices based on single-layer $MoS_2$ in a single-gate (top) and dual-gate (bottom) configuration. Gold leads are used for the source, drain and voltage probes ($V_1, V_2, V_3$ and $V_4$). Voltage probes have been omitted from the drawing. The silicon substrate, covered with a 270-nm-thick $SiO_2$ layer was used as the back gate. The top-gate dielectric is a 30-nm-thick $HfO_2$ layer.

by atomic layer deposition (ALD) forms the top-gate dielectric. The optical image of one of our top-gated devices is shown in Fig. 1a.

We have performed measurements on multiple devices in single- and dual-gate configurations (Fig. 1b; for more details on devices see Supplementary Table S1). By using the top gate we can induce stronger electrostatic doping of our monolayer $MoS_2$ owing to the higher dielectric constant and smaller thickness of the $HfO_2$ layer ($\varepsilon_{r2} \sim 19$, $d_{ox2}$ ($HfO_2$) = 30 nm) compared with the bottom-gate $SiO_2$ ($\varepsilon_{r1} \sim 3.9$, $d_{ox1}$ ($SiO_2$) = 270 nm). For both types of device, we measure the four-probe conductance defined as $G = I_{ds}/(V_1 - V_2)$, where $I_{ds}$ is the drain current and $V_1 - V_2$ is the measured voltage difference between the voltage probes.

A typical conductance, $G$, dependence on the gate voltage for a single-gate device is shown in Fig. 2a, measured up to the back-gate voltage $V_{bg} = 40$ V that corresponds to a charge concentration of $n_{2D} \sim 3.6 \times 10^{12}$ cm$^{-2}$ calculated using the parallel-plate capacitor model, with $n_{2D} = C_{ox1}\Delta V_{bg}/e$, where $C_{ox1} = \varepsilon_0\varepsilon_{r1}/d_{ox1}$, $\varepsilon_0 = 8.85 \times 10^{-12}$ F m$^{-1}$, $e = 1.602 \times 10^{-19}$ C is the elementary charge and $\Delta V_{bg} = V_{bg} - V_{bg,th}$. The value of threshold voltage $V_{bg,th}$ varies for each device and is close to its pinch-off voltage estimated from the conductance curves. We find that the temperature variation of $G$ in a single-gate monolayer device (Fig. 2b), in the high-temperature regime (80 K ≤ $T$ ≤ 280 K), can be modelled with thermally activated transport:

$$G = G_0(T)e^{-E_a/k_BT}$$

where $E_a$ is the activation energy, $k_B$ is the Boltzmann constant and $G_0(T)$ is the temperature-dependent parameter extracted from the fitting curves. The good agreement of the data with the activation transport model at higher temperatures is suggestive of charge transport that is thermally activated. At temperatures $T \leq 80$ K we observe that the variation of $G$ weakens for almost all $V_{bg}$ values. This can be explained with hopping through localized states becoming dominant at lower temperatures[25], driving the system into a strongly localized regime. The inset of Fig. 2a shows double sweeps of $I_{ds}$–$V_{ds}$ characteristics for several temperatures at $V_{bg} = 30$ V with negligible hysteresis for all temperatures and nonlinear behaviour vanishing completely for temperatures above 40 K, excluding the possibility of the contact resistance or Schottky barrier influencing the mobility extraction. Figure 2c shows the temperature dependence of mobility in this device. Mobility is extracted from the conductance curves in the 30–40 V range of back-gate voltage $V_{bg}$, using the expression for field-effect mobility $\mu = [dG/dV_{bg}] \times [L_{12}/(WC_{ox1})]$. The temperature dependence is characterized by a peak at ~200 K. Below 200 K, we observe a decrease of the mobility as the temperature is lowered down to 4 K. This behaviour is consistent with mobility limited by scattering from charged impurities[31]. Increasing the temperature above 200 K also results in a strong decrease of the mobility from the peak value of 18 cm$^2$ V s$^{-1}$, related to electron–phonon scattering that becomes the dominant scattering mechanism at higher temperatures[30]. We fit this part of the curve with the generic temperature dependence of the mobility $\mu \sim T^{-\gamma}$, where the exponent depends on the dominant phonon scattering mechanism. From the fit we find the value of $\gamma \approx 1.4$, in good agreement with theoretical predictions for monolayer $MoS_2$ ($\gamma \approx 1.69$; ref. 30).

We now examine dual-gated devices. Figure 3a shows a typical top-gating dependence of the four-contact $G$ and sheet conductivity $\sigma$, defined as $\sigma = GL_{12}/W$ with $L_{12} = 1.55$ μm and $W = 1.9$ μm being the distance between the voltage probes and the device width, respectively. The use of the top gate allows a higher degree of doping, up to $n_{2D} \sim 3.6 \times 10^{13}$ cm$^{-2}$ (Supplementary Fig. S1), much higher than typical values for single-gated devices ($n_{2D} \sim 4 \times 10^{12}$ cm$^{-2}$). We observe here an insulating behaviour that persists until $V_{tg} = 2.2$ V. At this point, corresponding to $n_{2D} \sim 1 \times 10^{13}$ cm$^{-2}$ (as measured from the Hall effect), monolayer $MoS_2$ enters a metallic state and the associated metal–insulator transition[32] (MIT) is observed, the first of its kind in a 2D semiconductor (Fig. 3a). This transition manifests itself as a crossing-over between conductance versus gate voltage curves acquired at different temperatures, indicating two different regimes. For gate voltages corresponding to charge densities smaller than $n_{2D} \sim 1 \times 10^{13}$ cm$^{-2}$, monolayer $MoS_2$ behaves as a classical semiconductor with conductance decreasing

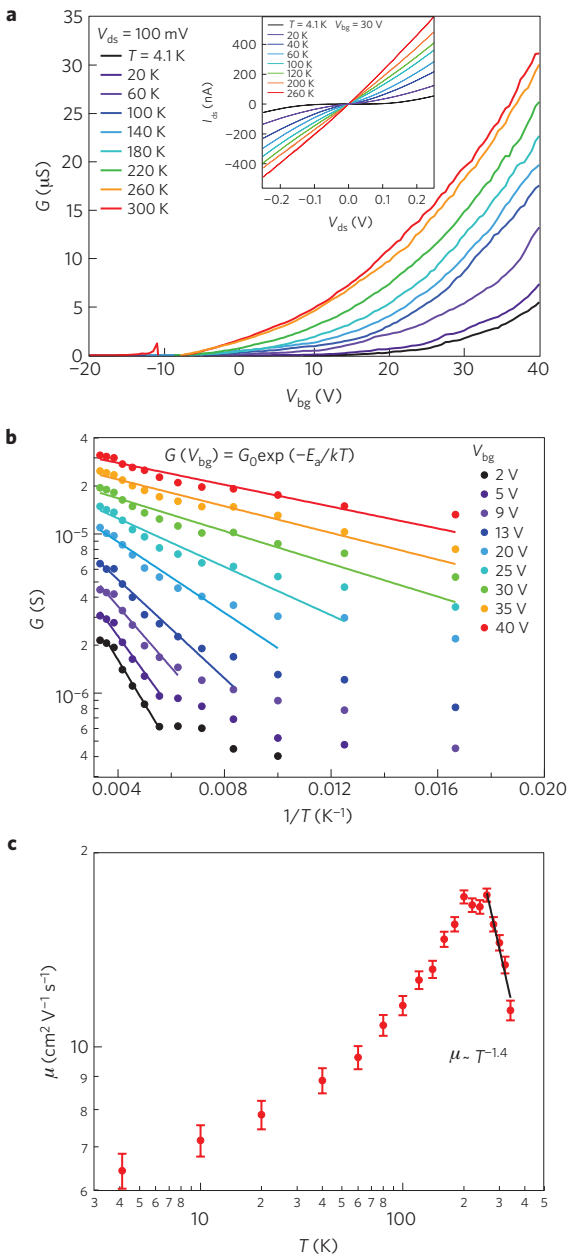


**Figure 2 | Electron transport in single-gate monolayer $MoS_2$ supported on $SiO_2$. a**, $G$ as a function of $V_{bg}$ for a single-gate monolayer $MoS_2$ device acquired at different temperatures. The inset shows double sweeps of $I_{ds}$–$V_{ds}$ characteristics for several temperatures at $V_{bg} = 30$ V with negligible hysteresis for all temperatures. **b**, Arrhenius plot of $G$ for different values of $V_{bg}$. Solid lines are linear fits to the data showing activated behaviour for limited regions of $T$ and $V_{bg}$ (charge density). **c**, The dependence of $\mu$ on $T$ shows a pronounced low-temperature regime consistent with transport dominated by scattering from charged impurities. Above ~200 K, $\mu$ is limited by phonon scattering and follows a $\mu \sim T^{-1.4}$ dependence. Error bars are estimated on the basis of uncertainties in determining the voltage drop across the channel.

as the temperature is decreased, whereas for higher gate voltages, corresponding to charge densities above $n_{2D} \sim 1 \times 10^{13}$ cm$^{-2}$, the conductance increases as the temperature is decreased, which is the hallmark of metallic behaviour. In the inset of Fig. 3a are shown double sweeps of $I_{ds}$–$V_{ds}$ characteristics for several temperatures at $V_{tg} = 0$ V with negligible hysteresis for all temperatures, excluding the possibility of hysteresis influencing our conclusions related to MIT. Fig. 3b shows the temperature dependence of the device conductance for different values of the charge density $n_{2D}$. We can see here more clearly that above the critical charge density of $1 \times 10^{13}$ cm$^{-2}$, the conductance of monolayer $MoS_2$ increases with decreasing temperature, which is the manifestation of metallic behaviour. For charge densities smaller than $1 \times 10^{13}$ cm$^{-2}$, the conductance decreases with the temperature, corresponding to semiconducting behaviour. This striking feature occurs when the conductivity is of the order of the quantum conductance $e^2/h$, the minimum of metallic conductivity, which was considered not to exist in 2D electronic systems according to the scaling theory of localization based on non-interacting electronic gases proposed in 1979[33].

The first step in our analysis is to define the critical point of the MIT. Inspecting Fig. 3a, we can see that each two consecutive isotherms of $G(V_{tg})$ cross each other at some value of $V_{tg}$. These intersections are temperature dependent, so an unambiguous determination of the transition is not possible. Fortunately, at temperatures under 80 K, the crossing point seems to be independent of the temperature and emerges at a well-defined point $V_{tg} = 2.2$ V, clearly separating the metallic and insulating phases. This transition point is the direct consequence of quantum interference effects of weak and strong localization. At lower carrier concentrations ($< n_{2D} \sim 1 \times 10^{13}$ cm$^{-2}$) the system is in the insulating state and strong localization[34] prevails. This charge density is comparable to that recorded for 20-nm-thick $MoS_2$ (ref. 13). As the top-gate bias is increased above $V_{tg} = 2.2$ V (concentration above $n_{2D} \sim 1 \times 10^{13}$ cm$^{-2}$), the system is driven into a metallic phase and weak localization seems to be the dominant effect. The observed quantum critical point of MIT in our devices is the consequence of a strongly correlated 2D electron gas[35]. As the system is confined in two dimensions, strong Coulomb interactions between electrons could cause a large ratio[36] $r_s$ between potential (Coulomb, $E_C$) and kinetic (Fermi, $E_F$) energy:

$$r_s = \frac{E_C}{E_F} = \frac{n_v}{a_B^* \sqrt{\pi n_{2D}}} = \frac{n_v m^* e^2}{4\pi\varepsilon\hbar^2\sqrt{\pi n_{2D}}}$$

where $n_v$ is the number of degenerate valleys in the spectrum, $a_B^* = (4\pi\varepsilon\hbar^2)/(m^* e^2)$ is the effective Bohr radius, with $\varepsilon$ being the dielectric constant and $m^*$ is the effective electron mass. A system with $r_s \gg 1$ cannot be considered as non-interacting and the conclusion of scaling theory of localization[33] is not valid in this regime. In the case of monolayer $MoS_2$ we obtain $r_s \approx 4.2$, considering $m^* = 0.45 m_o$ (ref. 22), $\varepsilon = 7.3\varepsilon_o$ (ref. 37), a double-degenerate conduction band around the $K$ point ($n_v = 2$) and an electron concentration at the transition of $n_{2D} \sim 1 \times 10^{13}$ cm$^{-2}$. This value is similar to those previously measured in the case of GaAs/AlGaAs heterostructures[38] ($r_s \sim 4$–5) and Si metal–oxide–semiconductor FETs[39] ($r_s \sim 8$). This shows that monolayer $MoS_2$ is a very attractive 2D system with strong Coulomb interactions, making the high-$r_s$ regime easier to reach than in cleaner Si metal–oxide–semiconductor FETs or n-GaAs-based devices[40]. The reason for this is the relatively high effective mass (for Si: 0.19 $m_o$; n-GaAs: 0.07 $m_o$) and lower dielectric constant (for Si: 11.7 $\varepsilon_o$; n-GaAs: 12 $\varepsilon_o$) of monolayer $MoS_2$.

We can now also investigate the Ioffe–Regel criterion[41–43] for 2D semiconductors, which predicts the existence of a MIT when the parameter $k_F \cdot l_e$ satisfies the criterion $k_F \cdot l_e \sim 1$, with the Fermi wave vector $k_F = \sqrt{2\pi n_{2D}}$, and mean free path of electrons $l_e = \hbar k_F \sigma / n_{2D} e^2$. According to this criterion, for $k_F \cdot l_e \gg 1$ the phase is metallic whereas for $k_F \cdot l_e \ll 1$, the phase is insulating. For our device, at the crossing point of $V_{tg} = 2.2$ V, we have $k_F \cdot l_e \sim 2.5$, in good agreement with the theory. Our other devices also exhibit $k_F \cdot l_e$ close to 2 (Supplementary Table S1).

The temperature dependence of the mobility is extracted from conductance curves in the $V_{tg} = 1$–5 V range, using the expression

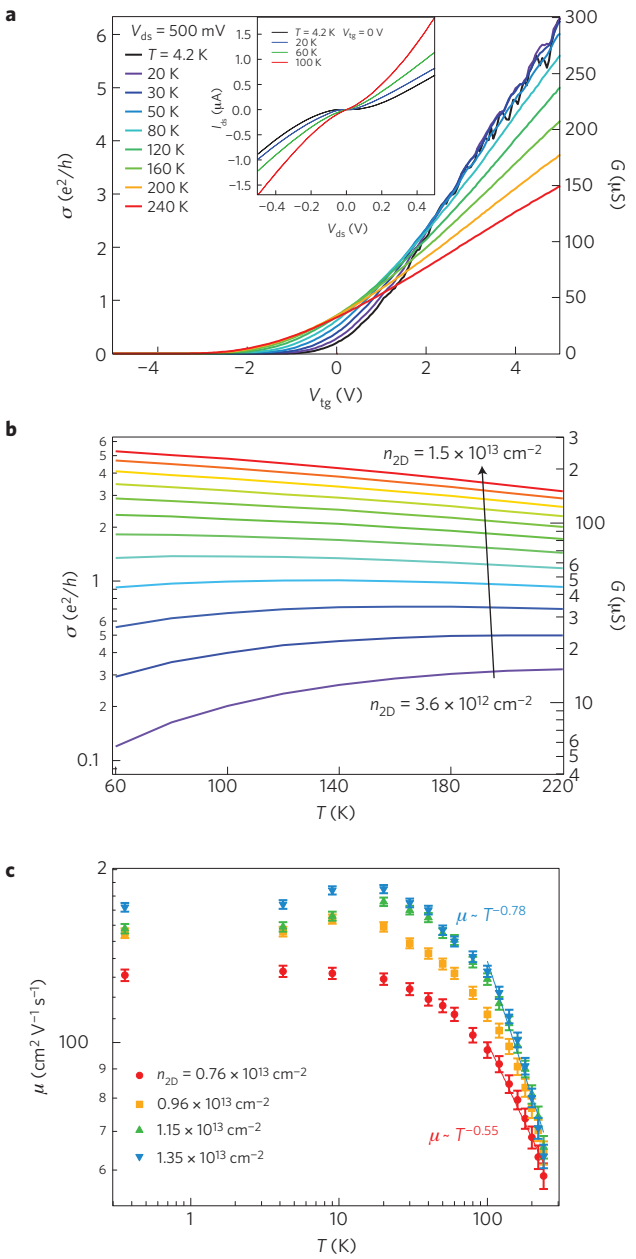


**Figure 3 | Electron transport in dual-gated monolayer $MoS_2$. a**, $G$ and $\sigma$ for different values of $V_{tg}$ and $T$. For low values of $V_{tg}$, $\sigma$ decreases with $T$. Above $V_{tg} \sim 1$–2 V, monolayer $MoS_2$ enters a metallic state, with increasing $\sigma$ as $T$ is decreased. The inset shows double $I_{ds}$–$V_{ds}$ sweeps. **b**, $T$-dependence of $\sigma$ for different values of $n_{2D}$. **c**, $\mu$ is practically independent of $T$ under 30 K, indicating screening of charged impurities due to deposition of the top-gate dielectric. Above ~100 K, $\mu$ decreases owing to phonon scattering and follows a $T^{-\gamma}$ dependence with $\gamma = 0.55$–$0.78$. The strongly reduced value of the exponent $\gamma$ with respect to the single-gated device ($\gamma = 1.4$) is indicative of phonon mode quenching. Error bars are estimated on the basis of uncertainties in determining the voltage drop across the channel.

for field-effect mobility $\mu = [dG/dV_{bg}] \times [L_{12}/(WC_{tg,Hall})]$, with capacitance $C_{tg,Hall}$ extracted from Hall-effect measurements. For all dual-gate devices that we have characterized, we observe a monotonous increase of the mobility as the temperature is decreased with a saturation at low temperatures. Figure 3c shows the temperature dependence of mobility for the main device presented here. The mobility at 4 K is 174 $cm^2 V s^{-1}$, reaching 63 $cm^2 V s^{-1}$ at 240 K for $n_{2D} \sim 1.35 \times 10^{13}$ $cm^{-2}$. This is a distinct difference from devices fabricated in a single-gate configuration (Fig. 2c). We relate this behaviour to effective damping of Coulomb scattering on charged impurities due to the presence of the high-$\kappa$ dielectric and the metallic top gate that changes the dielectric environment of monolayer $MoS_2$ (ref. 27). At low temperatures, the influence of charged impurities on mobility is stronger for lower electron densities. For example, at 10 K for $n_{2D} \sim 0.76 \times 10^{13}$ $cm^{-2}$ we extracted a mobility of 132 $cm^2 V s^{-1}$ whereas for $n_{2D} \sim 1.35 \times 10^{13}$ $cm^{-2}$ we extracted a mobility of 184 $cm^2 V s^{-1}$. In the phonon-limited part between 100 and 300 K, the mobility can be fitted to the expression $\mu \sim T^{-\gamma}$, with the exponent $\gamma$ being in the 0.55–0.78 range for electron concentrations $n_{2D}$ between $\sim 0.76 \times 10^{13}$ $cm^{-2}$ and $1.35 \times 10^{13}$ $cm^{-2}$ (Fig. 3c). For all of our double-gated monolayer devices we find this exponent to be between 0.3 and 0.78, whereas for one double-layer device we find a value of 1.47. These values for monolayer $MoS_2$ are much smaller than the theoretically predicted value of $\gamma \approx 1.52$ (ref. 30) or bulk crystals ($\gamma \approx 2.6$; ref. 24). This indicates that in addition to the quenching of the homopolar phonon mode, other mechanisms might influence the mobility of monolayer $MoS_2$ in dual-gated devices, for example, phonon screening induced by the metallic top gate or a change in the strength of electron–phonon coupling. Further theoretical modelling could shed more light on these mechanisms.

Just as in the case of single-gated devices, we model the temperature dependence of $G$ in the insulating regime of our double-gated devices with thermally activated behaviour (Fig. 4a). Here, we observe that the activated behaviour fits our data very well in the 100–250 K temperature range, with extracted activation energies $E_a$ shown in Fig. 4b.

We have performed Hall-effect measurements on all $MoS_2$ devices covered with a dielectric layer presented here to accurately determine the mobility, density of charge carriers and the capacitive coupling of $MoS_2$ layers to control gate electrodes (bottom or top gates). Figure 5a shows the transverse Hall resistance $R_{xy}$ of our main dual-gated monolayer device, which follows a linear dependence on the magnetic field $B$. From the inverse slope of $R_{xy}$ we can directly determine the electron density $n_{2D}$ in the $MoS_2$ channel. The variation of the electron density extracted from $R_{xy}$ as a function of the top-gate voltage $V_{tg}$ is shown in Fig. 5b. The slope of this dependence gives directly the capacitance $C_{tg,Hall} = 3.17 \times 10^{-7}$ F $cm^{-2}$ used in calculation of the field-effect mobility (Fig. 3c). We also directly measure the capacitive coupling between the channel and the bottom gate in devices where the $MoS_2$ channel is covered with a dielectric layer and in devices with disconnected top gates and compare them with the geometric capacitance per unit area calculated using the parallel-plate capacitance model $C_{geom} = \varepsilon_0 \varepsilon_r / d_{ox,bottom}$, where $d_{ox,bottom}$ is the thickness of the bottom-gate oxide[10]. We find that encapsulation in a dielectric can increase the capacitive coupling from $C_{geom}$ by a factor of 2.4, similarly to graphene devices[45], and disconnecting the top gate increases the capacitive coupling by a factor of 53 (Supplementary Fig. S4). These measurements prove that the capacitance can be underestimated in a complicated dielectric environment, both in the case of disconnected top gates[10–12] and encapsulation[44,46], resulting in mobility values that are probably overestimated. To accurately measure the field-effect mobility of FETs based on 2D materials one needs to measure the actual capacitance using either cyclic voltammetry[28] or Hall-effect measurements as outlined here.

In conclusion, we have performed conductance and mobility measurements on monolayer $MoS_2$ FETs in single- and dual-gate configurations. Using a top gate and solid-state dielectrics, we were able to tune the charge carrier density to more than $n_{2D} \sim 3.6 \times 10^{13}$ $cm^{-2}$, inducing the transition from the insulating to the metallic phase in monolayer $MoS_2$. A quantum critical point, separating the metallic phase, stabilized by electronic interactions,

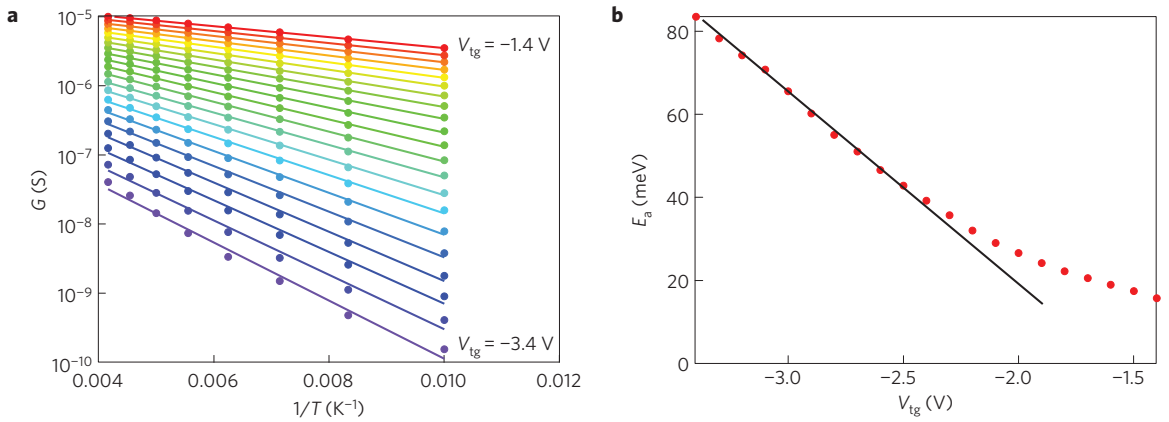


**Figure 4 | $E_a$ for the top-gated monolayer $MoS_2$ in the insulating regime. a**, Arrhenius plot of the conductance of monolayer $MoS_2$ covered with $HfO_2$, in the insulating regime. **b**, Dependence of $E_a$ on $V_{tg}$.

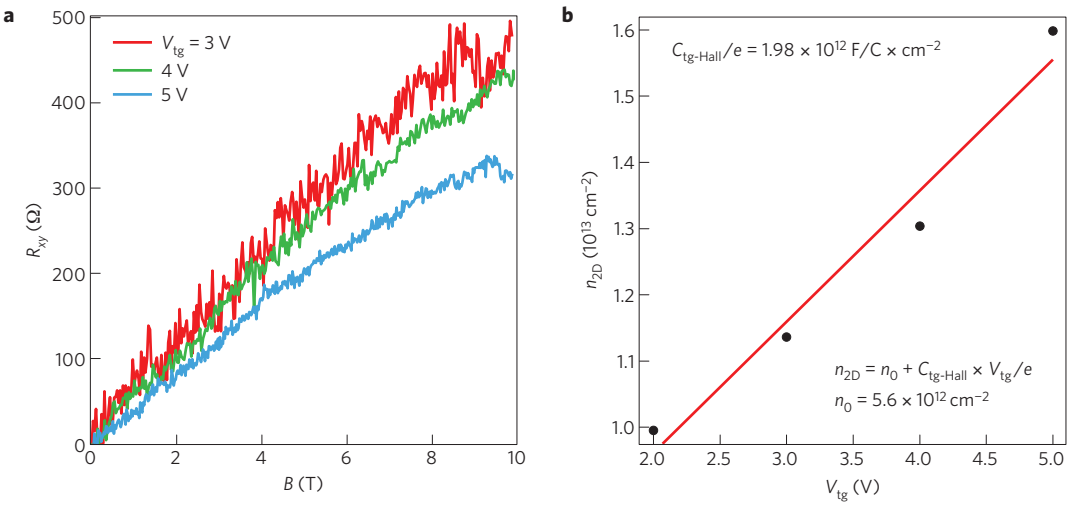


**Figure 5 | Hall-effect measurements in the dual-gated monolayer $MoS_2$ device. a**, Hall resistance $R_{xy}$ versus $B$ for different positive values of $V_{tg}$. **b**, Electron concentration $n_{2D}$ extracted from $R_{xy}$ or different values of $V_{tg}$. From the slope of the red solid line we calculate the capacitance per unit area $C_{tg,Hall}$ of the top-gate $MoS_2$ device. The residual doping of the $MoS_2$ channel is $n_o = 5.6 \times 10^{12}$ cm$^{-2}$. All measurements are performed at $T = 4$ K with a grounded back-gate electrode.

from the insulating phase, where disorder prevails over the electronic interactions, has been identified. This transition point is in good agreement with theory and shows that monolayer $MoS_2$ could be an interesting new material system for investigating low-dimensional correlated electron behaviour. The MIT could also be used for new types of switch, especially fast optoelectronic switches based on differences in optical transmission in metallic and insulating states[47]. In addition to allowing high charge densities, the high-κ $HfO_2$ used as the top-gate dielectric also changes the dielectric environment and effectively screens Coulomb scattering, which results in mobility improvement in dual-gate devices. Furthermore, the presence of the top-gate dielectric and metal electrode results in a quenching of the homopolar mode, which is polarized in the direction normal to the layer, leading to a strong decrease of the mobility exponent $\gamma$ in $\mu \sim T^{-\gamma}$. Our results provide a new picture of the mobility issue in different configurations of $MoS_2$ devices, which should shed new light on the directions for further improvements in device quality and characterization techniques.

## Methods

$MoS_2$ flakes were exfoliated from molybdenite crystals (SPI Supplies Brand Moly Disulphide) by the Scotch-tape micromechanical cleavage technique. ALD was performed in a Beneq system using the reaction of $H_2O$ with tetrakis(ethyl-methylamido)hafnium. Electrical characterization was carried out using National Instruments DAQ cards, SR570 current preamplifiers, SR560 low noise voltage preamplifiers, and an Oxford Instruments Heliox cryo-magnetic system.

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## Author contributions

B.R. worked on device fabrication and performed the measurements. A.K. designed the experiment and initiated the research. B.R. and A.K. analysed the results and wrote the manuscript.

## Additional information

Supplementary information is available in the online version of the paper. Reprints and permissions information is available online at www.nature.com/reprints. Correspondence and requests for materials should be addressed to A.K.

## Competing financial interests

The authors declare no competing financial interests.