Hot Stencils: A New Path for Resistless Nanopatterning

THÈSE N^{O} 5715 (2013)

PRÉSENTÉE LE 5 JUIN 2013
À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE DE MICROSYSTÈMES 1
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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Suisse
2013

Abstract

This thesis describes the developments of nanostencils for improved micro and nano patterning using stencil lithography (SL). A novel stencil concept with an integrated microhotplate on the stencil membrane is introduced and developed for preventing aperture clogging and locally reducing the gap between the stencil and the substrate. The useful life time of the stencil is significantly extended at least one order of magnitude and improved patterning resolution is achieved. In addition, an alternative stencil membrane material, PECVD SiC, is demonstrated to be promising for nanopatterning for both etching and metallization processes. Regarding applications, first results of stenciled nano-gates across high aspect-ratio, vertically stacked silicon nanowire transistors is also presented.

The heated stencil with a microhotplate integrated on the stencil membrane is developed and systematically studied. By locally heating the stencil up to ~850 °C, material condensation on the membrane can be prevented, thus eliminating aperture clogging. Comparison between the heated and non-heated stencils shows clear improvement of using the heated membrane for preventing aperture clogging: after 120 nm Al deposited on both heated and non-heated membranes, no clogging of aperture was found on the heated one, whereas a 300 nm size reduction of the aperture was observed on the non-heated one. The tailored design of the resistive heater allows thermal actuation of the membranes towards the substrate, which locally reduces the gap between the stencil and the substrate. Various membrane geometries are investigated in order to obtain the optimal design for the membrane deformation. FEM simulation is performed to study the heat transfer from the heated membrane through the reduced gap to the substrate. All three operation modes of SL: static mode, quasi-dynamic mode and dynamic mode, have been demonstrated with the heated stencil. In addition, we demonstrate that confining the deposition area on the membrane extends at least one order of magnitude the heated stencil's life time. The combined effects of unclogged aperture and locally reduced gap provided by the heated stencil greatly improve the patterning resolution and prolong the effectiveness of stenciling during deposition, which is especially important for the dynamic mode with sub-micron apertures.

Following the quest for application specific membrane material, we explore the use of PECVD SiC as stencil membrane material. Robust SiC stencils are developed and demonstrated for both micro and nano patterning. Nanodots down to 50 nm wide have been achieved by depositing materials through the SiC nanostencils. Etching through stencil shows that Al coated SiC nanostencil is capable of accurately transferring nanohole arrays to the substrate down to 75 nm wide. The SiC stencil demonstrates a better performance than that made of SiN in terms of robustness to deformation and resistance to etching. The obtained results indicate that SiC stencils provide unique advantages for a potential wider range of SL applications in some critical conditions, such as high temperature and high stress material deposition.

Stencils are successfully used for fabrication of functional sub-μm wide structures on 3D topographies, polysilicon gates on vertically-stacked Si nanowire field effect transistors (FETs) are patterned using nanostencils. A novel approach is developed, by using nanostenciled Al hard mask for structuring gate-all-around (GAA) polysilicon gates on high aspect ratio Si nanowires and Si nanofins transistors. Gate width down to 100 nm is achieved. Electrical measurements confirm the functionality of the fabricated devices with yield larger than 70%. This method provides possibility for achieving high density, large reproducibility and yield for the 3D nanowire transistors while maintaining the performance improvement related to scaling.

The results presented in this thesis are an important development for stencil lithography. Novel stencil concepts with either integrated microhotplate or new stencil membrane material demonstrate the feasibility for further improvement in achieving better resolution in micro and nano patterning. The use of nanostencil in Si nanowire transistors opens a wider path for SL in electronics application.

Keywords:

stencil lithography, micro and nano patterning, heated stencil, microhotplate, microheater, physical vapor deposition, FEM, PECVD SiC, nanofabrication, nanodots, Si nanowire, FET.

Résumé

Cette thèse décrit le développement de pochoirs pour l'amélioration de la micro et nano structuration au moyen de la lithographie par pochoir. Un concept novateur de pochoir muni d'une micro plaque chauffante ayant pour but la prévention de l'obstruction d'ouvertures ainsi que la réduction de la distance au substrat est présenté. Par cette méthode, la durée de vie du pochoir est significativement étendue et une amélioration d'au moins un ordre de grandeur de la résolution des structures crées est atteinte. L'utilisation du carbure de silicium, créé par dépôt chimique en phase vapeur assisté par plasma, comme matériau alternatif pour la réalisation de membranes est également explorée et permet de démontrer de prometteuses propriétés pour la nanostructuration de matériaux. La métallisation ainsi que la gravure au travers des pochoirs en carbure de silicium est étudiée avec succès. Les premiers résultats de la fabrication de nano grilles de transistors à nanofil de silicium superposés au moyen de lithographie par pochoir est également décrite.

Des pochoirs chauffés par une micro plaque chauffante appartenant à la membrane sont développés et systématiquement étudiés. Le pochoir peut être chauffé localement par effet joule jusqu'à 850°C afin de réduire la condensation de matériel sur la membrane permettant ainsi d'éviter l'obstruction des ouvertures. La distribution de la température est étudiée en comparant des simulations par éléments finis avec des mesures infrarouges. Aucune obstruction des ouvertures n'est observée lorsque le pochoir est chauffé alors que sans cela le diamètre de l'ouverture est diminué de 300nm lors d'une évaporation de 120nm d'aluminium. La conception adaptée de la plaque chauffante permet également de déformer la membrane et d'en réduire la distance au substrat. Plusieurs géométries de membranes différentes sont comparées afin d'obtenir une déflection appropriée pour réduire la distance au substrat. Des simulations par éléments finis sont à nouveau utilisées pour étudier le transfert de chaleur au travers de l'espace entre la membrane et le substrat. Le pochoir chauffé est utilisé dans les trois

modes de la lithographie par pochoir à savoir : le mode statique, le mode quasi-dynamique et le mode dynamique. Par ailleurs une amélioration de la méthode est réalisée en confinant la zone de dépôt à la partie chauffée membrane ce qui permet d'en étendre la dure de vie par un facteur d'au moins dix. Les résultats de l'action combinée du pochoir qui ne s'obstrue pas et de la distance au substrat réduite mettent en évidence une grande amélioration des structures réalisées en comparaison avec un pochoir non chauffé. Ceci est particulièrement utile pour le cas du mode dynamique lors de l'utilisation de membranes avec des ouvertures d'un diamètre sub-micrométrique.

Des pochoirs robustes en carbure de silicium créé par dépôt chimique en phase vapeur assisté par plasma sont aussi développés et utilisés pour la fabrication de micro et nano structures. Des points d'un diamètre aussi faible que 50nm sont fabriqués en utilisant de telles membranes. L'étude de la gravure au travers de membranes en carbure protégées par de l'aluminium révèle la capacité de transfert d'ensembles de nano ouvertures d'un diamètre aussi bas que 75nm. Les pochoirs en carbure offrent de meilleures performances que leur équivalent en nitrure aussi bien en matière de résistance aux déformations que d'endurance à la gravure. Les résultats obtenus laissent envisager que les pochoirs en carbure sont des candidats idéaux pour les applications extrêmes de la lithographie par pochoir en conditions de haute température ou fort stress mécanique.

La fabrication de nano-grilles de transistors à nanofil de silicium superposés au moyen de lithographie par pochoir est également décrite. Grâce aux avantages uniques de la lithographie par pochoir, une nouvelle approche utilisant un masque de gravure en aluminium est développée avec succès pour la création de grille en polysilicium pour des transistors à nanofils et nano arrêtes à grand facteur d'aspect. Des grilles d'une jusqu'à 100nm et un rendement de plus de 70 pourcent est atteint. Des mesures électriques confirment la fonctionnalité des transistors fabriqués. Cette méthode offre la possibilité d'atteindre une plus grande densité, une plus grande reproductivité et rendement tout en conservant l'amélioration des performances obtenues avec le facteur d'échelle.

Les résultats présentés dans cette thèse sont importants pour le développement de la lithographie par pochoir. Des concepts de pochoirs novateurs avec des éléments chauffants intégrés ou par l'utilisation de nouveaux matériaux démontrent les capacités d'améliorations futures en achevant une meilleure résolution pour la micro et nano structuration. L'utilisation

de pochoirs pour les transistors à nanofil de silicium ouvre la porte à de vastes applications du pochoir en électronique.

Mots clés:

lithographie par pochoir, micro et nano structuration, pochoir chauffé, micro plaque chauffante, dépôt chimique en phase vapeur, éléments finis, nanofabrication, nanopoints, nanofils de silicium, transistors à effet de champ.

Contents

Acronyms

AFM	Atomic force microscopy
Al	Aluminum
Au	Gold
Cr	Chromium
E-beam	Electron beam
FEM	Finite element method
FET	Field-effect transistor
FIB	Focused ion beam
KOH	Potassium hydroxide
LPCVD	Low-pressure chemical vapor deposition
Ni	Nickel
PECVD	Plasma enhanced chemical vapor deposition
O_2	Oxygen
Pt	Platinum
SEM	Scanning electron microscopy
Si	Silicon
SiC	Slicon carbide
SiN	Silicon nitride
SiNW	Silicon nanowire
SiO_2	Silicon dioxide
Ta	Tantalum
TCR	Temperature coefficient of resistance
Ti	Titanium
W	Tungsten

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1 Introduction

This dissertation focuses on the development and improvement of the stencils for stencil lithography (SL) and its application. This chapter gives the motivation and an overview on the state of the art of stencil lithography. The major technical challenges of SL are described, which limits the further development of SL especially in dynamic mode. Accordingly the objectives of this thesis are given and the outline of the thesis is described.

1.1 Background and Motivation

One of the most important technology innovations in last five decades that fundamentally changed our life is the invention of integrated circuits (IC) and its miniaturization towards very-large-scale integration (VLSI) predicted by Moore's Law. Thanks to the continuous scaling-down of the transistors, more powerful and cheaper devices are able to be applied in all aspects of our lifes. Nowadays, we are rapidly approaching the end of the scaling-down course because of the physical limitation in sub-10 nm domain and the tremendous difficulties in fabrication process. Therefore, novel materials, innovative device architectures and non-planar transistor structures are being studied in order to maintain the technology advancement. Associating with these new research trends are the needs for improvement of current nanopatterning techniques and the complement with new technologies in unconventional nanofabrication, e.g. on 3D structures. In addition, the micro-/nanopatterning and structuring in emerging technologies, such as flexible electronics, organic semiconductors and biomaterial based applications etc., faces many difficulties as well. Thus, the development of a robust, versatile and cost-efficient micro-/nanofabrication toolbox with fast-prototyping capabilities will be a key factor for further miniaturization on complex 3D structures, for new applications based on unconventional nanopatterning as well as for exploration of new phenomenon with nanoscale features on different materials. In recent years, there are few new technologies for miniaturization developed in different fields in science and enginnerning. For examples, *nanoimprint lithography* (NIL) uses a hard stamp to imprint into a resist film with resolution down to sub-50 nm, but it faces difficulties in patterning non-flat surfaces; *scanning probe lithography* is based on the use of scanning probes to modify a surface, however scaling up the size of the patterning surface still needs to be explored; *soft lithography* is based on self-assembly and replica molding, however there are still technical challenges such as alignment and high resolution. Among all such new nanopatterning techniques, stencil lithography provides unique advantages such as fast and simple processing, large compatibility with various materials and high adaptability on topography.

Stencil lithography (SL) is a shadow mask based technique which allows parallel, resistless, micro and nanopatterning of material through apertures in a membrane (stencil) onto a substrate [1, 2, 3, 4], as schematically shown in *Figure* 1.1. The major advantage is its simple and non-resist based process, which allows fabrication on a wide range of materials and substrates that are not compatible with resist based patterning. Besides, it offers important capability of patterning on topography, where conventional spin-coated resist is not able to cover the high aspect ratio step. However, like many other patterning methods, there are also technical challenges which limits the applicability of SL in some aspects. One of the main challenges is that the deposition of material on the sidewalls of apertures leads to the aperture shrinking or even *clogging*, which limits the effective life time of stencil in one deposition. Another important issue is the inevitable *gap* between the stencil and the substrate due to the geometric setup, which results in the enlargement of the pattern comparing with the aperture size, known as *blurring*, the key limiting factor for the resolution in SL. In addition, the stencil membrane becomes unstable in some applications which involve high temperature and stressed material deposited on the membrane, leading to a complicated process for membrane reinforcement. Efforts have already been devoted to find solutions to these issues.

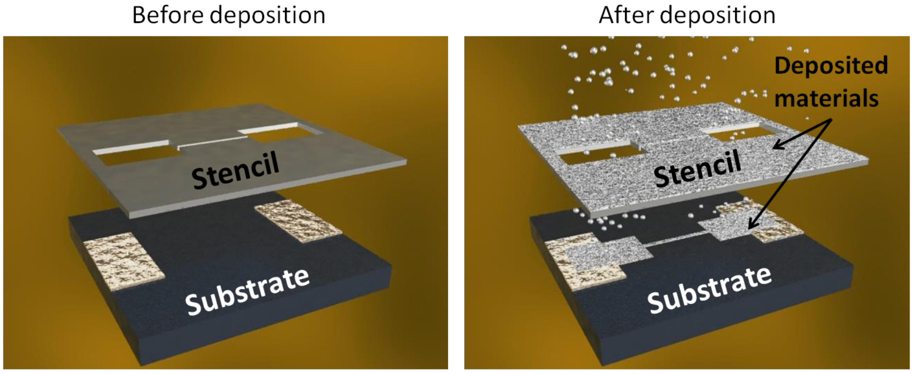


Figure 1.1: Schematic diagram of stencil lithography

However, none of an individual solution can meet all the requirements of these challenges. In order to improve the resolution and exploit the applicability of SL in nanopatterning, it is demanded a further development of this technique for exploring a potential universal solution for all the technical challenges.

1.2 State of the Art: Stencil Lithography

1.2.1 Overview of Stencil

Stenciling or shadow masking is a simple method of repeating a design by means of a cut out shape; the word stencil means the outline of an image. The earliest examples of stenciling to help data storage by transferring the shape of human hands onto the caves were found in Palaeolithic cave paintings dating from as early as 30,000 BC to 9,000 BC. It was the invention of paper by the Chinese in 105 AD that provides a robust and reliable stencil material, which enables the mass production of stenciled symbols and characters. Nowadays, it is still a tradition of making paper cutting stencils in China, especially in the Chinese New year, as shown in *Figure* 1.2a. Currently, stencils have many practical applications in all aspects of our life. *Figure* 1.2b shows the example of stencil in unconventional patterning in our daily life, stenciled cocoa powder pattern on cappuccino. Stencil concept is also used frequently in industrial, commercial, artistic, residential and recreational settings, as well as by military, government and infrastructure management. Stencil templates can be made from any material which will hold its form, ranging from plain paper, cardboard, plastic sheets, metals and wood,

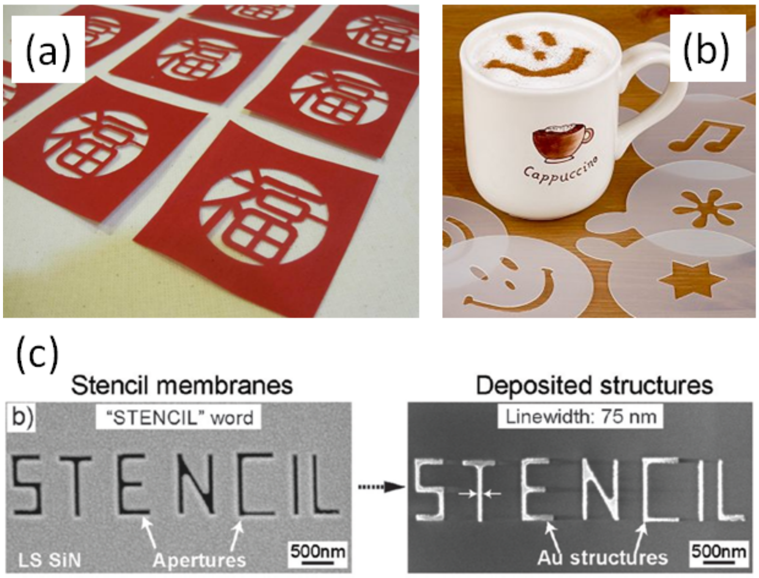


Figure 1.2: Examples of stencils. (a) Chinese New Year stencils by paper cutting. (http://ilikepapercutting.blogspot.ch/2013/01/chinese-new-year-stencils.html) The Chinese character on the stencil means good fortune. . (b) Stenciled pattern with cocoa powder on cappuccino (http://nemavofazia.wordpress.com/2010/08/17/cafe-caliente/). (c) SEM images of word "STENCIL" made of Au with 75 nm line width deposited on SU-8 [6].

etc. The stencil concept has been applied in advanced micro and nanopatterning since the first systematical report in 1959 [5], known as stencil lithography. After decades of development, a large number of new applications have been realized by taking the unique advantages of stencil lithography. *Figure* 1.2d illustrates an example of stenciled nanopatterns on organic substrate [6].

1.2.2 Recent Applications of Stencil Lithography

Stencil lithography (SL) has become a reliable micro-/nanopatterning technique and recently has shown great potential in many unconventional applications [7, 8, 9, 10]. Sub-50 nm patterns on full wafer area have been achieved by SL [11]. Various materials like metals [12], oxides [13], ferroelectric/magnetic materials [14, 15] and organic molecules [16] have been successfully deposited through stencils. In addition to the material deposition, etching [17] and ion implantation [18] to the substrate through a stencil have also been demonstrated, which makes SL a more universal patterning process. Besides the advantage of variety of materials which can be deposited, SL offers unique capabilities in patterning on flexible substrate and on top of three-dimensional (3D) topography. Moreover, its non-resist needed patterning process provides bio-compatible environment for bio-applications. Due to the simple fabrication process and duplicate ability, low cost and high volume production could also be realized by industrial manufactory. Here we selectively show the recent applications by using SL.

Stenciled Structures on Flexible and Unconventional Substrates

Stenciled structures has been recently demonstrated in many applications which involves flexible and unconventional substrates [8, 9, 6]. The realization of structures on flexible, stretchable, nonplanar, and biocompatible substrates as opposed to conventional rigid substrate will direct the path for novel applications. Stencil as a patterning tool has been shown to be capable of creating nanostructures on flexible substrate for biosensing application. Asku *et al* [8] showed the creation of Au bow-tie structures with 40 nm gap on PDMS for plasmonic sensing (*Figure* 1.3) based on the previous work of nanostenciled plasmonic nanoantenna arrays [7]. Active tuning of plasmonic resonances is achieved by applying mechanical strain to a LDPE thin film supporting nanorod structures. Vazquez-Mena et al demonstrated Au nanodots down to 50 nm feature size deposited through nanostencils on different solid [11] and polymer substrates [6], including SiO_2, polyimide, SU-8, parylene and PDMS. Plasmon resonance detection of biotin and streptavidin using the PDMS flexible film with Au nanodots indicates the functionality. Tao *et al* [10] presented the fabrication of metamaterial resonators sprayed on paper substrates with a predefined microstencil for potentially quantitative analysis in biochemical sensing applications. The easily patterned resonant electromagnetic structures on inexpensive paper-based sensing platform enables the dramatically increasing number of diagnostics applicatoins. Engstrom and Savu *et al* [9] showed the high throughput nanofabrication of silicon nanowire and carbon nanotube tips on AFM probes by stencil-deposited catalysts (*Figure* 1.4). The fabricated AFM probes were tested for imaging micrometers-deep trenches, where the SiNW and MWNT tips demonstrated a significantly better performance than commercial high aspect ratio tips. This method demonstrates a reliable and cost-efficient route toward wafer scale manufacturing of SiNW and MWNT AFM probes. Lee *et al* [19] reported a nanocontact printing method that can be used to create large-area arrays of molecular patterns with both high density and high resolution (50 nm) by using nanostencil masks

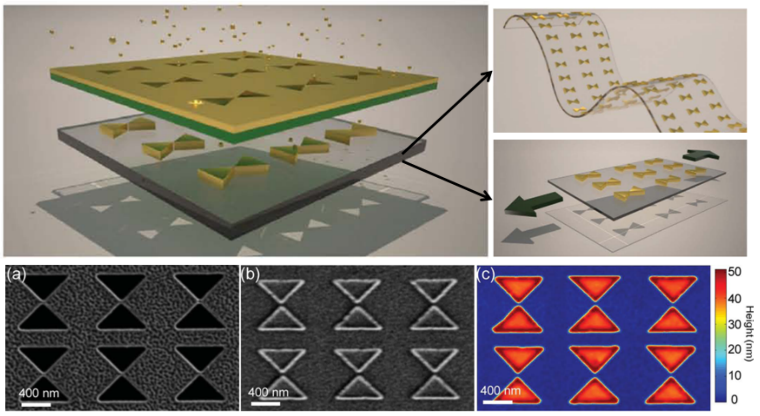


Figure 1.3: Schematics of stencil lithography on flexible and stretchable substrate. (a) SEM image of a bow-tie stencil mask. (b) SEM image of bow-tiw structures on PDMS substrate. (c) AFM image of bow-tie particles shown in (b). The interparticle distance is measured to be 40 nm on average. [8]

consisting of Au films of nanoholes arrays. This method can increase the throughput in the fabrication of biological assays and electronic circuits and can generate model substrates for studies of cell-adhesion and cell-proliferation mechanisms. Huang *et al* [20] demonstrated a reusable nanostencil for creating multiple biofunctional molecular nanopatterns on PDMS substrate. Different types of biomolecules can be covalently patterned on the surface through nanostencils while retaining their biofunctionalities. This approach largely simplifies the bio-nanopatterning process and therefore shows very promising implications in diverse biological and medical applications.

Stenciled Electronics

SL has also been demonstrated in various electronics applications. Zhou et al [21] presented the fabrication of the contacts to molecular circuits by evaporating metal through a nanoscale silicon nitride stencil membrane. In this way, contacts can be fabricated on as-grown molecular wires (λ-DNA networks) that would be contaminated or destroyed by chemicals and heat treatments associated with conventional lithographic techniques. Villanueva *et al* [22] demonstrated the completely resistless all-through-stencil fabrication of transistors (*Figure* 1.5a). It is shown that all the essential fabrication steps (implantation, etching and metallization) can be performed by using stencil lithography on both planar and pre-patterned 3D substrates, thus showing potential for applications in the field of ac-

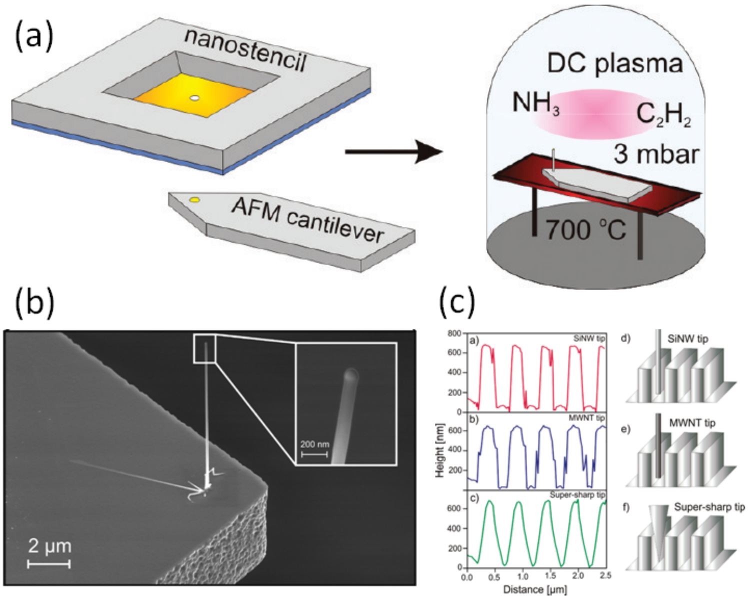


Figure 1.4: (a) Schematics of the formation of carbon nanotubes on the catalyst deposited through nanostencil on AFM cantilever. (b) SEM images of an epitaxially grown SiNW on an AFM cantilever. (c) AFM scans of high aspect ratio silicon trench using a SiNW, MWNT, and Supersharp AFM tip. [9]

celerometers, pressure, gas and radiation sensors. Sidler *et al* [23, 24] showed the fabrication of organic thin film transistors on flexible polyimide substrates (*Figure* 1.5b). Both pentacene and source-drain (S/D) electrodes were directly patterned through stencils with high accuracy on wafer scale. Stretching of the organic transistors is performed by stretching the polymer substrate, which showed a constant mobility after the first stretching cycle. Vazquez-Mena *et al* [12] reported the full wafer stencil lithography on fabrication of metallic nanowires (*Figure* 1.5c). Nanowires down to 70 nm wide and 5 μm long have been achieved showing a resistivity of 10 $\mu\Omega$cm for Al and 5 $\mu\Omega$cm for Au. Lu *et al* [25] presented a novel stenciling method to fabricate silicon nano-conical-frustum array for solar cells application (*Figure* 1.5d). Using planar radioactive β-electron thin film emitters to parallel expose e-beam through a Tungsten coated stencil mask, the resist on the substrate can be selectively exposed to form desired patterns down to 35 nm feature size. This non-vacuum required nanopatterning technique potentially enables large-area massively parallel high throughput electron lithography with high resolution and low cost. Wassei *et al* [26] reported a simple and flexible method of stenciling carbon nanomaterials (graphene, carbon nanotube, C_{60}) that are dispersed in hydrazine using PDMS microstencil (*Figure* 1.6). This method represents a versatile process to selectively register these carbon nanomaterials into configurations suitable for nanoelectronic devices.The stencil technique has also been applied to fabricate commercial consumer electronics. SAMSUNG developed a technique using Fine Metal Mask (FMM) to fabricate high resolution OLED display [27]. The latest flexible display for the mobile phone is believed to be manufactured by using FMM. This technique could enable unlimited applications that potentially would revolutionize the mobile industry.

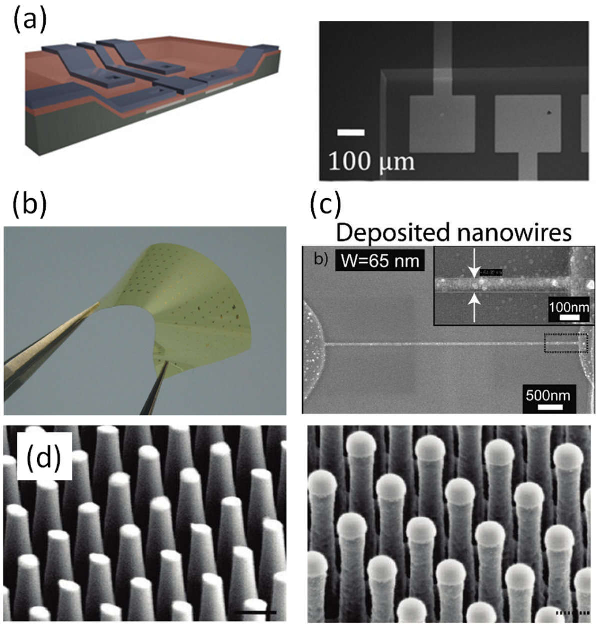


Figure 1.5: (a) Schematics and SEM image of all-stencil transistor [22]. (b) Organic thin film transistors on polyimide substrates [23]. (c) Metallic nanowires deposited through nanostencils [12]. (d) Si nano-conical-frustum arrays and ordered quasi-nanowire arrays made by electron lithography through nanostencils for solar cell application [25].

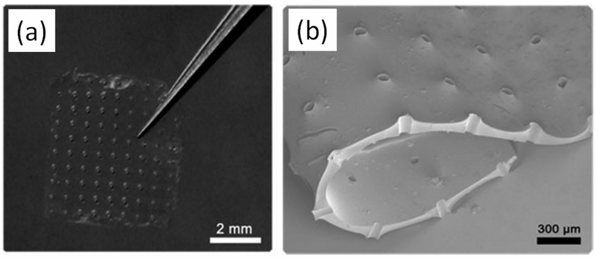


Figure 1.6: (a,b) PDMS microstencil for patterning of carbon materials (graphene, carbon nanotube, C_{60}). [26]

1.2.3 Operation Modes

After decades of development, SL has been developed to have three different operation modes: static mode, quasi dynamic mode and dynamic mode, as illustrated in *Figure* 1.7. Having a stencil remaining static relative to the substrate during patterning (usually with mechanical clamp) is known as static SL (see *Figure* 1.7a), which is the most commonly used mode when standard techniques fail due to either the substrate or the evaporated material's fragility to mechanical, thermal or chemical stress [28, 29, 30]. A step-and-repeat motion of the stencil during the evaporation is called quasi-dynamic mode (see *Figure* 1.7b), which has been developed in applications such as solar cells [31], nanopatterning [32, 33], and organic light emitting devices [34]. A continuous relative motion between the stencil and the substrate during material deposition is known as dynamic mode stenciling (see *Figure* 1.7c) [35, 36, 37, 4]. In this thesis, all three operation modes will be demonstrated by integrating with the heated stencil.

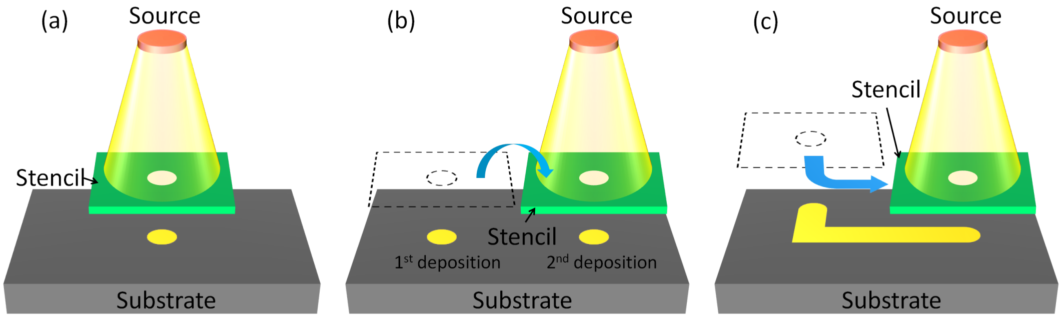


Figure 1.7: Three operation modes for stencil lithography. (a) static mode; (b) quasidynamic mode; (c) dynamic mode.

1.2.4 Dynamic Stencil Lithography Systems

In the static operation of SL, the stencils is fixed on the substrate thus requires no complicated tools. However, a monitoring and controlling system is demanded for the use of quasidynamic and dynamic modes of SL. The first AFM based dynamic stencil lithography (DSL) system was reported in 1999 by Luthi [4], followed by Egger *et al* [35] in 2005. Egger *et al* developed a system where the angle between the stencil and the substrate was measured by laser deflection and corrected by means of a piezo tilting stage (i.e. a non contact method). The development of DSL system was quickly followed by Zahl *et al* in 2005 [38], who used a mechanical auto alignment approach where the stencil and substrate are pressed against each other and mechanically fixed in this position (hard contact method). However, the XYZ actuation is based on a piezo tube, resulting in a rotation of the substrates in the XY displacement. Lateral alignment is achieved by a prealignment of stencil and other tools (STM, AFM) within predefined positions on a carousel type system. Later, Guo *et al* [37] introduced a dynamic nanostencil system based on a movable atomic force microscope (AFM) cantilever borne mask in UHV with outstanding nanopartterning capability as well as *in situ* AFM characterization in large scanning range. However, the metal evaporator is mounted on the AFM vacuum chamber with an angle of 33° between the direction of evaporation beam and the horizontal plane, which means the patterns transferred from the membrane to the substrate have a distortion due to the angle. The aforementioned dynamic stencil systems are all based on conventional SPM, which is limited in chip level. The first full wafer scale dynamic lithography system was reported by Savu and Boogaart *et al* in 2008 [39]. The system allows material deposition in the quasidynamic and dynamic modes. Computer controlled XY and Z positioning stages located inside a high vacuum deposition chamber allow precise 3D movement of micromachined low stress silicon nitride membranes with respect to a static substrate (*Figure* 1.8). Based on the existing system, the full wafer self-cleaning stencil can be integrated into the PVD chamber, with connecting wires to the external power source. In this thesis, the novel stencil is implanted to this DSL system for the use of all three operation modes.

1.3 Challenges: Clogging, Gap and Blurring

There are three major technical challenges in SL that limits the accuracy of pattern transferring and effective life time of the stencil for material passing through the aperture in one deposition. *Figure* 1.9 schematically illustrates the basic principle of stencil lithography and also reveals three major technical challenges: *clogging*, *gap* and *blurring*.

Clogging: The incoming material will deposit on the stencil membrane, but it will also accumulate on the side walls of the stencil aperture, leading to a reduction in the aperture size. It is shown that the clogging size is in the same magnitude range as the deposition thickness. In the case of nanopatterning, it significantly decreases the useful life time of the nanostencil.

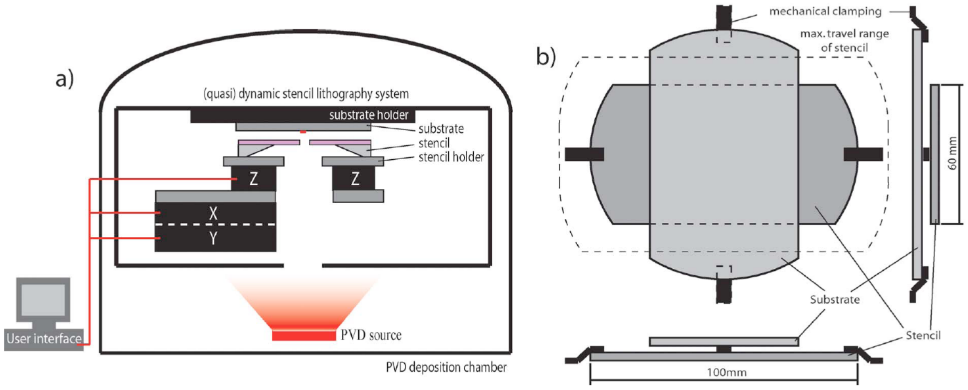


Figure 1.8: Schematics of the full wafer dynamic stencil lithography system. (a) The stencil and the stencil holder are mounted on a high-precision XY stage, while the substrate holder is maintained at a controlled gap from the stencil by three Z actuators, everything controlled by a personal computer user interface, and (b) cleaved stencil and substrate allowing mechanical clamping and full range of XY-stage motion. [39]

In addition, it also largely reduces the reproducibility of the deposited pattern, which presents a more conical shape as shown in *Figure* 1.9. When the deposition thickness is much larger than the aperture size, the complete clogging of aperture will happen, thus no more material can pass through. The clogging of aperture becomes a much severer issue in dynamic SL, as the reduction in aperture size will modulate the width of the trajectory, eventually lose its "writing" function when the aperture is entirely clogged.

Gap: There is usually an inherent gap between the stencil and the substrate due to the curvature of the wafer. Geometrically the gap will produce an enlarged pattern on the substrate, as illustrated in the grey dashed-line in *Figure* 1.9. Systematic study has shown that this enlargement (also known as geometric blurring) can be theoretically extracted by comprehensively considering several parameters: the effective source size, the aperture size and the source-to-substrate distance [40]. The controlling of gap becomes vital if high resolution nanoscale patterning is desired. However, in dynamic mode, a gap (~ 50 μm) has to be advisedly remained in order to allow the free motion between stencil and substrate, leading to the loss of resolution.

Blurring: Due to the gap, the size of the deposited structure is already larger than the size of the corresponding aperture. However, the blurring size also has to take into account the contribution from the diffusion of the deposited material on the surface of the substrate, know as “Halo”. It is demonstrated that the halo size is independent from the temperature of the substrate, but determined by both the gap and the material of the substrate [40]. At nanoscale, this issue dramatically limits the resolution of the deposited patterns.

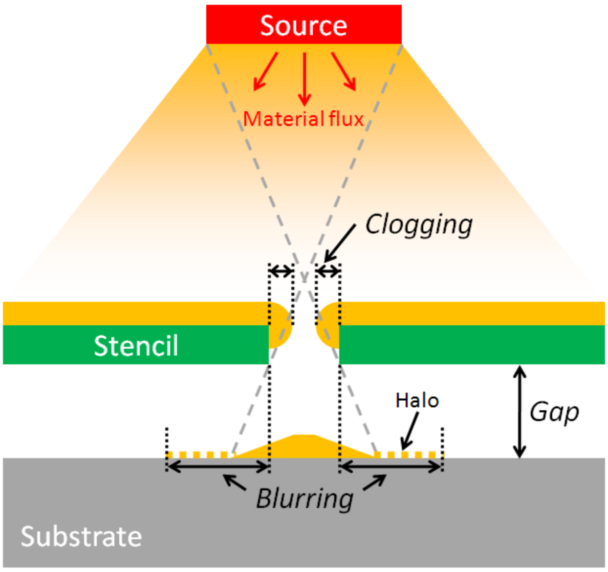


Figure 1.9: Schematics of stencil lithography showing the three major technical challenges: *clogging* of the aperture, inherent *gap* between the stencil and the substrate, *blurring* of the deposited structures.

1.4 Objectives

The general objective of this work is the improvement of resolution in SL, development of full wafer dynamic SL and exploration of the applicability of SL in nanopatterning. In order to achieve this objective, three major aspects will be covered: 1) Exploration of a novel stencil concept as a universal solution to all the technical challenges, which will eventually improve the resolution and extend the useful life time of stencil; 2) Investigation of more robust membrane material as alternative for conventional stencil membrane in order to improve pattern resolution in critical conditions, e.g high temperature and high stress material deposition; 3) Nanopatterning on high aspect ratio topography for electronics application.

To realize the first aspect, a novel stencil concept with integrated microhotplate on the stencil membrane was proposed, namely heated stencil. The goal is to design and fabricate the heated stencil, which will be later used to demonstrate its capability of solving all three technical challenges. The heated membrane has to be characterized to achieve high temperature for eliminating material accumulation on the membrane, an ultimate way to prevent aperture clogging. The heater design needs to be optimized to provide desired bending direction, which is used to locally reduce the gap. This approach is important especially for dynamic SL, as the locally reduced gap still allows free motion of the stencil while improves the resolution.

The investigation of new stencil material will be performed by exploring the feasibility of PECVD SiC membrane in SL application. The excellent chemical and mechanical property of PECVD SiC potentially makes it a great candidate to be used as stencil membrane. Both micro and nano SiC stencils will be fabricated and applied in SL. Comparison has to be made between SiC stencil and SiN stencil. SiC stencil as direct etching mask will also be investigated

The third aspect is the application of nanostenciling in electronics application. Nanostenciled structures on high aspect ratio topography has to be first demonstrated, then applied to the fabrication of functional electronics devices. The target is to create sub-μm wide gate across vertically stacked Si nanowire transistors by using nanostencil lithography. The fabricate process has to be developed and characterization of the fabricated devices has to be carried out in order to demonstrate the functionality.

1.5 Thesis Content and Organization

This thesis is organized in seven chapters. The first chapter has presented the motivation, the state-of-art of stencil lithography, the major technical challenges and the objectives of this work. The overview of the remaining chapters with each a short introduction is shown below:

Chapter 2. Heated Stencils Prevent Aperture Clogging. This chapter presents the heated stencil as a novel stencil concept to prevent clogging of apertures by minimizing material condensation on the membrane, which is achieved by locally heating up the membrane through the integrated microheater.

Chapter 3. Actuated Gap Reduction by Using Heated Stencil. This chapter presents another function of the heated stencil: actuated gap reduction by thermal induced deformation of the membrane. The gap is locally reduced through the bending of the membrane, leading to improved resolution.

Chapter 4. Stencil Lithography with Heated Membrane. This chapter presents the use of heated stencil in all three operation modes of stencil lithography. Comparison between heated and non-heated stencil is described.

Chapter 5. PECVD SiC Membrane Made for Stencil Lithography. This chapter presents the development of robust PECVD SiC membrane for stencil lithography. Both micro and nano SiC stencils are demonstrated as patterning mask in metallization and etching process.

Chapter 6. Nanostencil for Polysilicon Nanowire FETs Application. This chapter presents the application of nanostenciling in the fabrication of polysilicon nanowire FETs. Sub-μm gate is made across vertically stacked Si nanowire arrays by using nanostencils.

Chapter 7. Summary, Conclusions and Outlook. This chapter concludes this work and provides outlook for further research.

2 Heated Stencils Prevent Aperture Clogging

2.1 Introduction

The productivity of SL during one pump-down is limited by the clogging rate of the aperture, which determines the useful lifetime of the stencil [41]. This becomes an even more severe issue in dynamic mode where the stencil moves relative to the substrate during evaporation, translating the gradual size reduction of aperture into a distorted trajectory [42]. Various approaches have been shown to extend the life time of the stencil. The reusability of nanostencils after Al deposition has been proved by using selective wet etching in order to clean the membrane [41]. The nanostencils can be reused several times after each cleaning process. However, the thickness of the total deposited material is still limited when the thickness is comparable to the dimension of the nanoapertures. A different method uses pre-coated self-assembled monolayers on the stencil membrane before deposition [43, 44], which showed a reduced adhesion of gold inside the apertures. However, the clogging still remained an issue in the thick gold layer building up on top of the membrane. Neither of the aforementioned methods can totally prevent clogging as materials still accumulate on the membranes, leading to the inevitable size reduction of the apertures.

In this chapter, we present a novel stencil concept: an integrated microhotplate on the stencil membrane prevents aperture clogging, as shown in *Figure* 2.1. In order to minimize material condensation on the stencil membrane, the stencil is locally heated up by the integrated resistive microheater, an ultimate method to prevent clogging of apertures. At the

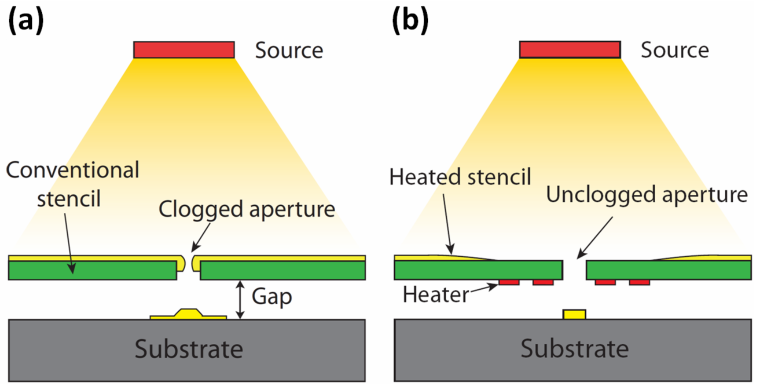


Figure 2.1: The diagrams of (a) conventional stencil lithograph. The pattern on the substrate is distorted, due to the clogging of the stencil aperture and the gap; (b) stencil lithography with heated membrane, which greatly improves the resolution by unclogging the aperture and minimizing the gap.

same time, the material flux can pass through the stencil aperture for substrate patterning. Another advantage of heating the stencil membrane is membrane actuation towards substrate, which minimizes the gap between the stencil and the substrate. Details about minimizing the gap will be introduced in Chapter 3. In section 2.2, the kinetic theory of gases and the classic Hertz-Knudsen equation will be used to theoretically describe the process of minimizing thin film condensation on the substrate or stencil membrane. In section 6.3, design and fabrication process of the heated stencil will be described. Simulation and characterization of the devices will be introduced in section 2.4. Experimental results of heating pre-deposited metal on the membrane will be shown in section 2.5. In section 2.6 the heated and non-heated stencil performance will be compared and the clogging-free apertures in a heated stencil will be demonstrated. Conclusions are presented in section 2.7.

2.2 Thin Film Condensation in Physical Vapor Deposition

Physical vapor deposition (PVD) is the production of a condensible vapor by physical means and subsequent deposition of a thin film from this vapor. The physical means of producing a vapor include heating of a source material with Joule heating (thermal evaporation) or an electron-beam (E-beam evaporation), laser induced vaporization with an intense photon beam (pulsed Laser deposition), and bombarding atoms out of a target with energetic ions (sputtering). Among these different methods, E-beam evaporation is often used in SL applications especially when sub-micron resolution is required, due to the advantages of its small effective source size, the long distance between the source and the targeting substrate, and the directional material flux. These advantages minimize the pattern distortion induced by the geometric setup, leading to better resolution.

The condensation of thin film is a dynamic process. The deposition of material on the substrate depends on the difference between the impingement flux from the source and the reevaporation flux from the substrate. When the impingement flux is larger than the reevaporation flux, which depends on the temperature of the substrate, net condensation of thin film is expected. However, when the temperature of the substrate is high enough that the reevaporation flux becomes larger, condensation will not happen, even the deposited film could be desorbed from the substrate. Therefore, the controlled condensation is achievable by varying the substrate temperature. In this section, the kinetic theory of gases and the classic Hertz-Knudsen equation will be used to theoretically describe the process of minimizing thin film condensation on the substrate or stencil membrane [45].

Condensation of Thin Film from Vapor Phase

The condensation of a vapor to solid or liquid occurs when the partial pressure of the vapor exceeds the equilibrium vapor pressure of the condensed phase at this temperature. That means the vapor is “supersaturated”, which make vapor condense on the substrate to form a solid thin film. The basic science of condensation includes calculating the thermal equilibrium vapor pressure of substances, and determining whether there is a condition of supersaturation at the substrate.

The thermal equilibrium vapor pressure of substance A is given by

$$P_{\mathrm{A}eq} = P^{\circ} exp(\frac{\triangle_{vap} S^{\circ}_{\mathrm{A}}}{R}) exp(\frac{-\triangle_{vap} H^{\circ}_{\mathrm{A}}}{RT}) \tag{2.1}$$

where P° is the ambient pressure (10^5 Pa), $\triangle_{vap} S^{\circ}_{\mathrm{A}}$ is the standard entropy of vaporization, $\triangle_{vap} H^{\circ}_{\mathrm{A}}$ is the standard enthalpy of vaporization, R is the molar gas constant, and T is the temperature. Vapor pressure is estimated with tabulated values of the thermodynamic quantities. The JANAF Thermochemical Tables [46] are an excellent source of standard thermochemical data. *Table* 2.1 presents a selection of thermochemical data of the commonly used evaporation metals [46, 47]. These quantities will be applied to estimate the vapor pressure in section 2.2. Here we only present the values at the melting point of each element. The approximation is made that these quantities are not temperature dependent.

Element	Melting Point (°C)	$\triangle_{vap}H^{\circ}(T_{\mathrm{m}})$ SkJ/mol)	$\triangle_{vap}S^{\circ}(T_{\mathrm{m}})$ $(\mathrm{J}\cdot\mathrm{mo}l^{-1}\cdot{}^{\circ}\mathrm{C}^{-1})$
Aluminum [Al]	660	314	117.8
Chromium [Cr]	1857	349	118.8
Titanium [Ti]	1668	438	124.6
Gold [Au]	1064	349	122
Platinum [Pt]	1768	529	123

Table 2.1: Standard Enthalpies and Entropies of Vaporization for Al, Cr, Ti, Au and Pt at the melting point of each elements.

The impingement rate is the number of collisions per unit area per unit time that a gas makes with a surface, such as a chamber wall or a substrate. Anticipating the ideal gas law, $PV = NkT$, the impingement rate as calculated with the kinetic theory is proportional to the pressure:

$$z = \frac{P}{\sqrt{2\pi mkT}} \tag{2.2}$$

where P is the gas pressure, m is the particle mass, k is Boltzmann's constant, and T is the temperature. By applying the thermal equilibrium vapor pressure P_{eq} to the equation, the impingement rate of a metal material under certain temperature can be calculated. The rate will be then translated to flux to describe the vapor deposition process. *Figure* 2.2 illustrates the key factors of the deposition process, from the temperature of an evaporation source to the film deposition rate, by taking into account the deposition angle.

The beam intensity of an ideal effusion cell is given by

$$J_{\Omega} = \frac{z\delta A\cos\theta}{\pi} \tag{2.3}$$

where δA is the orifice area of the effusion cell and θ is the emission angle.

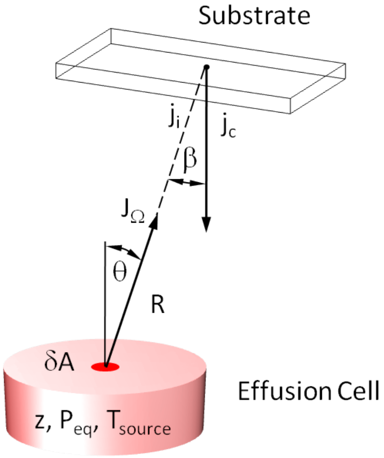


Figure 2.2: Vapor deposition of a thin film. An illustration of the chain of concepts and principles leading from the temperature of an evaporation source to the film deposition rate. T_{source} is the source temperature, P_{eq} is the thermal equilibrium vapor pressure within the source, z is the impingement rate of vapor within the source, J_Ω is the source beam intensity, j_i is the incident flux at the substrate, and j_c is the resulting film deposition rate.

The second item we need to define is the incident flux at the substrate:

$$j_i = \frac{J_\Omega \cos\beta}{R^2} \tag{2.4}$$

This relation gives the particle flux at a point on the substrate, in particles per unit area per unit time. Hear, β is the deposition angle and R is the distance from the orifice to the point of interest on the substrate. To simplify the calculation, we assume the particle flies vertically upwards away from the source and lands perpendicularly to the substrate.

After the definition of the incident flux, the condensation of the film is discussed. A film will condense on a substrate when there exists a supersaturated vapor above the substrate. This fact is described from the equation:

$$j_c = \alpha_c[j_i - z_{eq}(T_{sub})] \tag{2.5}$$

where α_c is the condensation coefficient, which gives the fraction of impinging particles that actually condense. To simplify, here we assume the vaporization coefficient is equal to the condensation coefficient. This equation expresses the condensation flux at the substrate as proportional to the net difference between the impingement flux from the source and the reevaporation flux from the substrate, as illustrated in *Figure* 2.3.

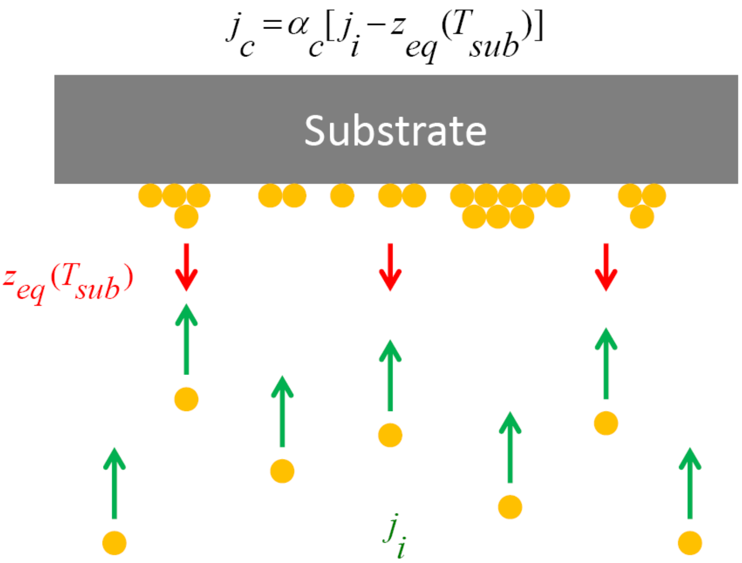


Figure 2.3: The net condensation flux at the substrate depends on the difference between the impingement flux j_i from the source and the reevaporation flux $z_{eq}(T_{sub})$ from the substrate. Their difference is multiplied by the condensation coefficient α_c to get the actual condensation flux.

Therefore, the idealized behavior of condensible vapor is portrayed schematically in *Figure* 2.4, which shows the condensation flux as a function of incident flux. The following principles are illustrated:

- For a given substrate temperature, there is a critical incident flux above which a film will form, but below which no deposit is obtained.
- The greater the substrate temperature, the greater the critical incident flux

In another word, supersaturation is necessary as the condition for accumulation of a thin film. The degree of supersaturation is given by

$$S \equiv \frac{j_i}{z_{eq}(T_{sub})} - 1 \geq 0 \tag{2.6}$$

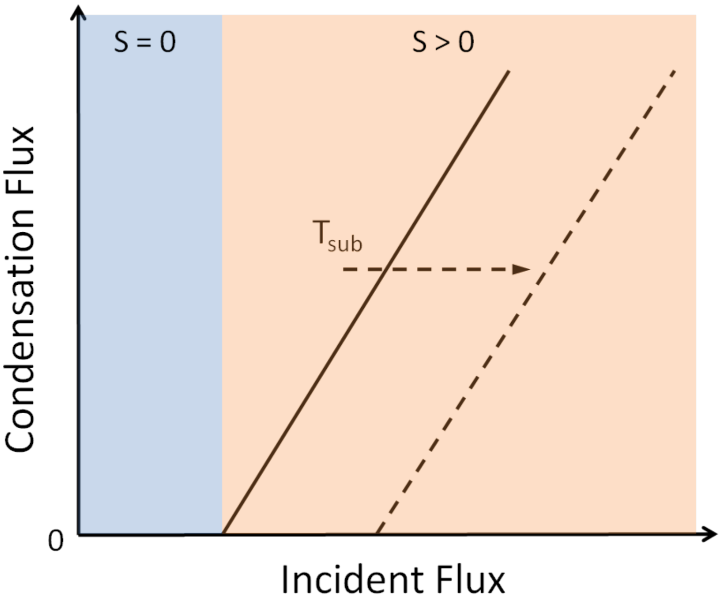


Figure 2.4: Film condensation. For film deposition by condensation from the vapor, there is a critical incident flux at the substrate below which no film accumulates ($S = 0$). The value of this critical flux increases with substrate temperature. The condensation only happens when the incident flux is larger than the reevaporation flux ($S > 0$).

Therefore, j_i must be greater than the impingement rate corresponding to the substrate temperature if a film is to condense on the substrate ($S > 0$). This does not mean merely that the substrate temperature must be below the source temperature, sometimes it must be substantially below the source temperature.

Critical Incident Rate

The critical incident rate is the value that allows us to keep the substrate or stencil membrane clean at certain temperature. Before calculating the critical incident rate, we have to translate the flux j_i [$\text{Å}^{-2} \cdot \text{s}^{-1}$] to rate υ_n [$\text{Å} \cdot \text{s}^{-1}$], in order to adapt the solution to the evaporation system where evaporation rate is often used. The lattice model is applied to estimate this rate. A film deposited on a substrate is shown schematically in *Figure* 2.5.

The total volume of atoms V_{total} deposited on a surface A is given by:

$$V_{total} = A \cdot h = V_{eff} \cdot Number_{atoms} \tag{2.7}$$

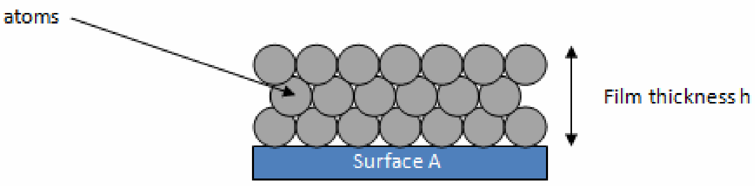


Figure 2.5: Atoms deposited on a surface A

where V_{eff} is the effective volume occupied by an atom inside the lattice, A is the surface area and h is the thickness of a film. In order to estimate V_{eff} the lattice structure of each chosen metal (Al, Au, Pt, Cr and Ti) is investigated and the results are shown in *Table* 2.2.

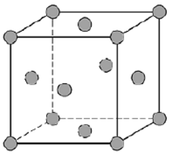
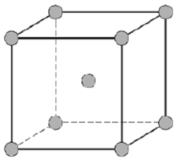
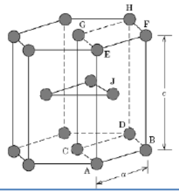
Lattice structure	Lattice volume	Material	V_{eff}
Face-Centered-Cubic (FCC) 	4 atoms per lattice: $V_{eff} = \frac{V_{lattice}}{4}$ $V_{lattice} = a^3$	**Al** (a = 4.05 Å)	16.6 [Å^3]
		Au (a = 4.08 Å)	17 [Å^3]
		Pt (a = 3.92 Å)	15 [Å^3]
Body-Centered-Cubic (BCC) 	2 atoms per lattice: $V_{eff} = \frac{V_{lattice}}{2}$ $V_{lattice} = a^3$	**Cr** (a = 2.88 Å)	11.94 [Å^3]
Hexagonal-Closed-Packed (HCP) 	6 atoms per lattice: $V_{eff} = \frac{V_{lattice}}{6}$ $V_{lattice} = 3.(a^3).sin60°.b$	**Ti** (a = 2.95 Å) (b = 4.68 Å)	17.6 [Å^3]

Table 2.2: Lattice structure of Al, Au, Pt, Cr, Ti and the effective volume of an atom.

Therefore, the rate can be expressed as:

$$v_n = \frac{h}{t} = \frac{V_{eff}\cdot Number_{atoms}}{A\cdot t} = V_{eff}\cdot j_i \tag{2.8}$$

where t is the time during which the substrate is exposed to the incoming flux. By using this method, we can easily translate the flux to rate by only taking into account the effective volume of the atom of each element, with the assumption that the thin film is in crystallization state.

Then by using the thermochemical data from *Table* 2.1, we can calculate the reevaporation rate in order to plot the graph of the condensation rate as function of the incident rate of each element. Here, the critical incident rate is equal to the reevaporation rate at certain temperature, which means the condensation rate is zero ($S = 0$). For example, when the substrate temperature is 900 °C, the reevaporation rate for Al is 3.7 Å/s. This means the critical incident rate must be smaller than 3.7 Å/s in order to make sure no condensation will happen. By using the concept, we will be able to keep the stencil membrane clean when the temperature of the membrane is high enough. *Figure* 2.6 illustrates the Al condensation rate as a function of incident rate for different temperatures. As we can see, when the temperature is at 700 °C, the critical incident rate is very small (0.005 Å/s), which means the substrate is not hot enough to eliminate condensation if the incident rate is in the practical range (>10^{-1} Å/s).

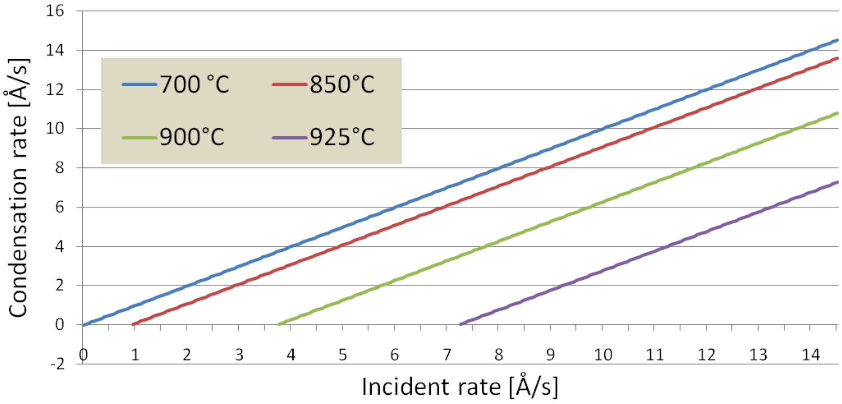


Figure 2.6: Aluminum (Al) condensation rate as a function of incident rate for four temperatures: 700 °C, 850 °C, 900 °C and 925 °C. The critical incident rates under these temperatures are 0.005 Å/s, 1 Å/s, 3.8 Å/s and 7.3 Å/s, respectively.

We also plot the condensation rate as function of incident rate for other commonly used evaporation metals: Cr (*Figure* A.1), Ti (*Figure* A.2), Au (*Figure* A.3) and Pt (*Figure* A.4). Different temperatures are chosen for each element to illustrate the dependence of the critical incident rate on the temperature. Details can be found in Appendix A.

2.2.1 Critical Temperature for Practical Incident Rate

In this section, we estimate the critical temperature of a metal for which the critical incident rate is in the practical range. In E-beam evaporation, the evaporation rate is controlled by the current of the electron beam. A practical rate is usually larger than 10^{-1} Å/s. As we discussed in section 2.2, there is a critical temperature for each metal at which the evaporation rate is larger than 10^{-1} Å/s. This temperature can make sure the deposition rate that passes through the stencil apertures is in the practical range ($> 10^{-1}$ Å/s), at the same time this required temperature is achievable on the membrane for keeping it clean. Details will be discussed in section 2.6. *Table* 2.3 summarizes the critical temperature of different metals for keeping the substrate clean under the deposition rate of 0.3 Å/s, 0.5 Å/s, 1 Å/s and 4 Å/s. *Figure* 2.7 plots the critical incident rate (from 0.01 Å/s to 10 Å/s) as a function of temperature, which shows the practical process window for these metals.

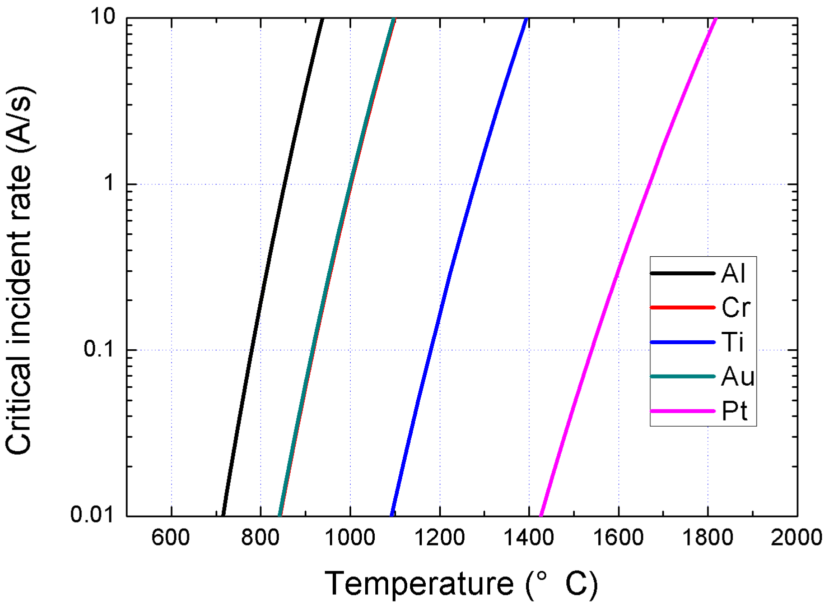


Figure 2.7: Critical incident rate in the practical range (0.1 Å/s to 10 Å/s) as a function of temperature for Al, Cr, Ti, Au and Pt. The curves for Au and Cr are overlapping.

Element / melting point (°C)	Critical temperature (°C) $v_n = 0.3$Å/s	 $v_n = 0.5$Å/s	 $v_n = 1$Å/s	 $v_n = 4$Å/s
Aluminum [Al] / 660	812	830	854	903
Chromium [Cr] / 1857	953	975	1001	1059
Titanium [Ti] / 1668	1225	1249	1277	1358
Gold [Au] / 1064	954	974	1000	1057
Platinum [Pt] / 1768	1598	1626	1674	1752

Table 2.3: Critical temperature of different metals (Al, Cr, Ti Au and Pt) for keeping substrate/membrane clean under practical deposition rates (0.3 Å/s, 0.5 Å/s, 1 Å/s and 4 Å/s)

2.3 Design and Fabrication

The heated stencil is fabricated by integrating membrane based microhotplates [48, 49] with stencils. The resistve heater is either placed on top of or embedded in the LPCVD SiN membrane. Thus it is thermally isolated from the bulk Si in order to achieve a high local temperature. The temperature is not uniformly distributed thus creates a gradient profile across the membrane, with highest temperature in the center area. The metal coils are made of Pt, with Ta serving as an adhesion layer. Ta has the advantage over other adhesion layers, e.g. Ti, to be more compatible with the second deposition of LPCVD SiN, providing more reliable and robust membranes at temperature up to 800 °C [50, 51, 52, 53]. Stencil apertures are placed across the membrane in between the Ta/Pt electrodes for studying clogging behavior under different temperatures. *Figure* 2.8 illustrates the design of the heated stencil. The width of the electrode and the space between the neighbour electrodes are both 30 μm. There are open areas of 40 μm×40 μm embedded in between the electrodes, which serve as windows to place stencil apertures. The membrane area is 1 mm×1 mm. Two shapes of the resistive heater were included, the meander and the coil. As we vary the number of loops, in total 12 different designs were made for optimizing the temperature and the deformation of the membrane. Figure 2.8 shows coil design with 3 loops.

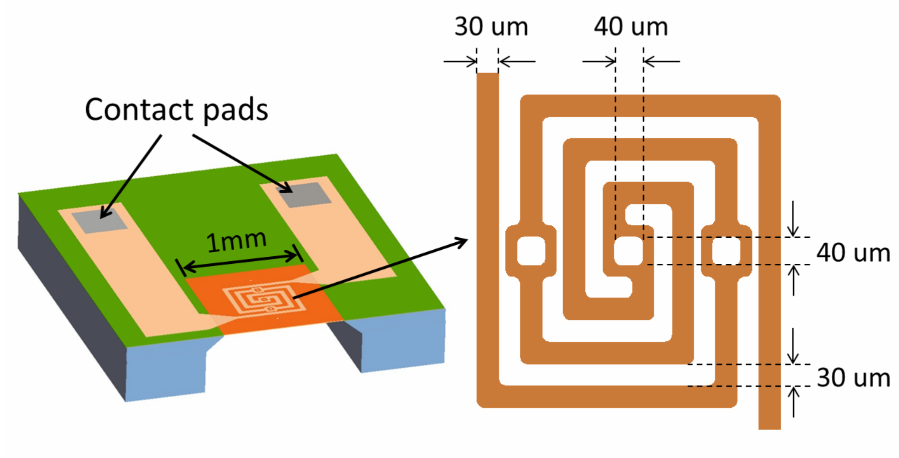


Figure 2.8: Design of the heated stencil. The membrane size is 1 mm×1 mm. The width of the electrode and the space between two electrodes are both 30 μm. The area of 40 μm× 40 μm in between the electrode will be used to place the stencil apertures.

Figure 2.9 illustrates the fabrication process. The heated stencil we developed contains Ta/Pt electrodes patterned on a 500 nm thick SiN membrane, with stencil apertures located in between the coils. The fabrication process started from a Si wafer coated with 500 nm LPCVD SiN on both sides (*Figure* 2.9a). The resistive heating coils were made of 15 nm Ta / 200 nm Pt and defined on the front side of the wafer by lift off process (*Figure* 2.9b). Stencil apertures were then formed by photolithography and SiN dry etching (*Figure* 2.9c). Back side windows were defined by SiN dry etching and consecutively Si deep etching with DRIE process (*Figure* 2.9d). 2 μm thick Parylene was deposited on the front side of the wafer for the protection of the electrode in later KOH process (*Figure* 2.9e). The residual 50 μm thick Si left after the DRIE was etched away by KOH and Parylene was then stripped by O_2 plasma (*Figure* 2.9f).

Figure 2.10 shows optical images of the full wafer heated stencil, the single membrane with integrated microheater, the coils, and a zoomed-in SEM image of the apertures, respectively. The flatness of the membrane after fabrication was measured with an optical profilometer. No deformation due to the induced stress from the metal coils has been observed.

Chip level heated stencils have also been fabricated for characterization, as shown in *Figure* 2.11a. As aforementioned, in total 12 different heater designs are made for investigating the optimal one. *Figure* 2.11b and c selectively show two types of resistive heater designs: coil and meander. All of the heater design is shown in Appendix A (Figure A.5).

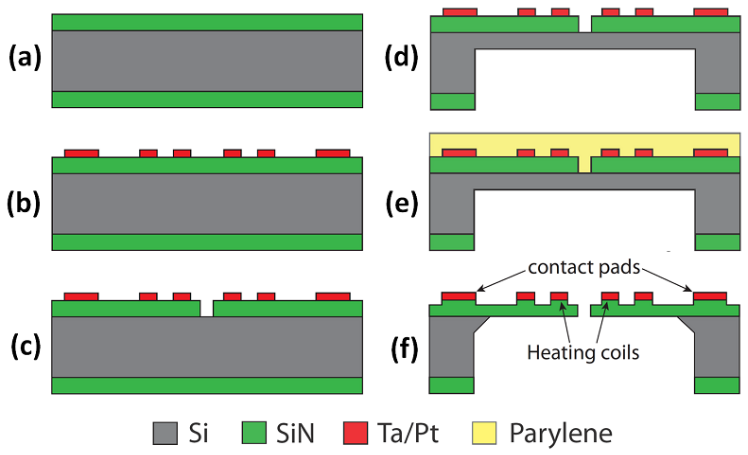


Figure 2.9: Fabrication of the heated stencil. (a) Deposition of 500 nm LPCVD SiN on both side of the Si wafer. (b) Definition of 15 nm Ta / 200 nm Pt resistive heater by lift-off process. (c) Patterning of contact pads and stencil apertures. (d) Definition of backside windows by SiN dry etching and consecutively Si deep etching. (e) Deposition of 2 μm thick Parylene on the front side for protection of electrodes in KOH. (f) Releasing membrane in KOH and stripping Parylene with O_2 plasma.

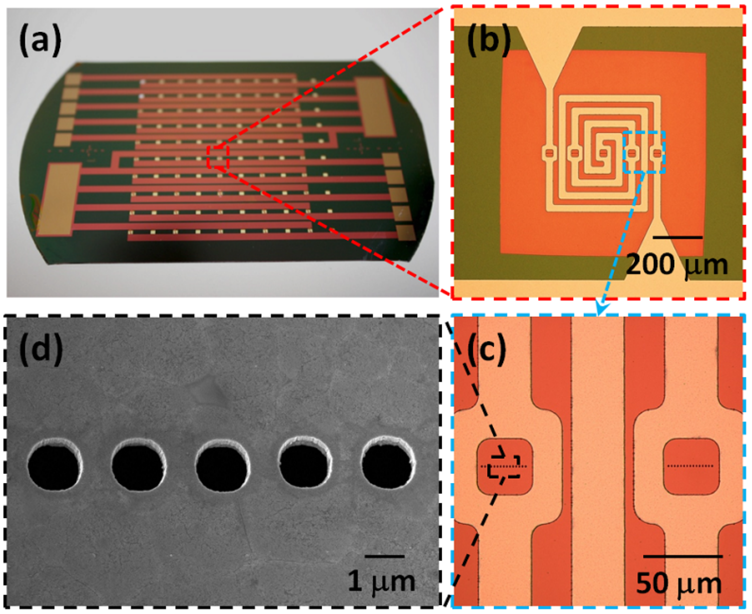


Figure 2.10: Optical micrographs of (a) Full wafer heated stencil, (b) single membrane with integrated microheater with (c) zoom-in and (d) SEM image of the apertures in between the coils.

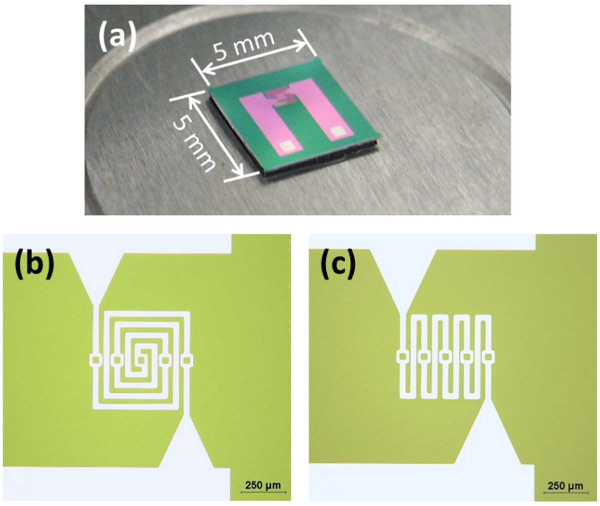


Figure 2.11: Optical images of chip level heated stencil. (a) 5mm × 5mm chip heated stencil. (b) Coil design. (c) meander design.

2.4 Characterization and Simulation

This section presents results of the characterization and the simulation by Comsol. The temperature of the microhotplate (<450 °C) was measured by infrared microscope. When the temperature is higher than the measurable range of the infrared sensor of the microscope, the temperature coefficient of resistance (TCR) is used to estimate the temperature. The distribution of the temperature on the membrane was systematically studied by comparing the results from simulation and IR measurement. The IR measurment was done in collaboration with IEMN, Lille, France. The power applied to the microhotplate is also measured. Different heating materials (Pt, W and Nichrome) were fabricated and compared to find the optimal material for our application. Failure modes at fast and slow ramping speeds were also studied, helping us to evaluate the stability of the device.

2.4.1 Temperature Coefficient of Resistance

The temperature of the heated stencil is calculated from the calibrated temperature coefficient of resistance α (TCR). The temperature dependence of conductors can be described by the approximation below

$$R(T) = R_0[1 + \alpha(T - T_0)] \tag{2.9}$$

where R_0 is the resistance at room temperature T_0 and α is the TCR. As the resistance can be derived from the heating current and the voltage across the heater, the membrane temperature can be calculated from Eq 2.9 based on the resistance.

Platinum (Pt) is a material often used in microheaters due to its resistance to oxidation and its high melting point (T_M ~1768 °C [54]), which offers the capability of high-temperature operation. Furthermore, the resistance of Pt changes linearly with temperature over a wide range (0 ~ 800 °C [55, 56]) and its TCR α is known to be relatively high and stable over this range [52]. The TCR of bulk Pt is 3.9×10^{-3}/°C. As for thin film Pt, the TCR varies from 2.0 ~ 4.3×10^{-3}/°C [57, 58, 59] depending on layer composition of the Pt thin film (application of an adhesion layer or not) and annealing conditions (like temperature and time).

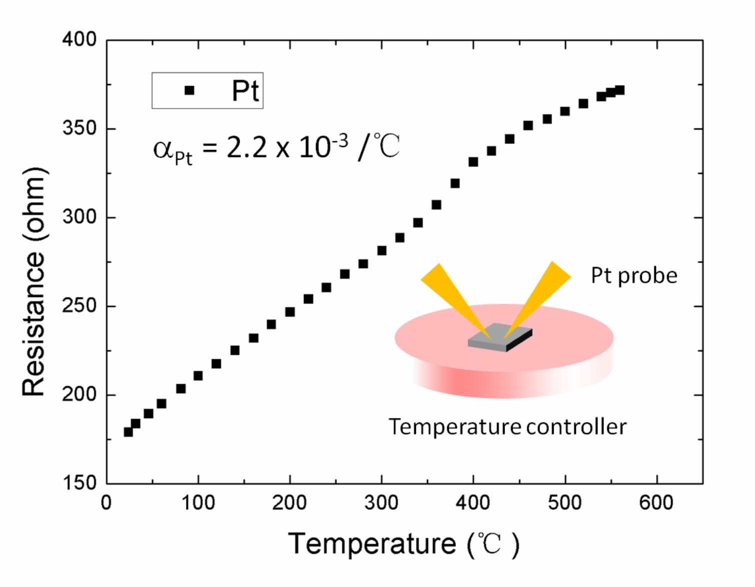


Figure 2.12: Calibration of TCR for heated stencil made by Pt.

For calibrating the device, a temperature controlling stage with max 540 °C was used. A thermocouple was place right beside the device to measure the actual temperature of the device. Pt probe was used for electrically contacting the device in order to eliminate the influence from other metals at high temperature. *Figure* 2.12 shows the calibration of the TCR for Pt (2.2×10^{-3}/°C). The value was derived from the linear fit of resistance vs. temperature. By using this method, the heated stencils with other heater design were also calibrated and the TCR shows slightly different. heated stencil made by other heating materials (W and

Nichrome) have also been calibrated, as shown in *Figure* 2.13. Details will be discussed in section 2.4.4.

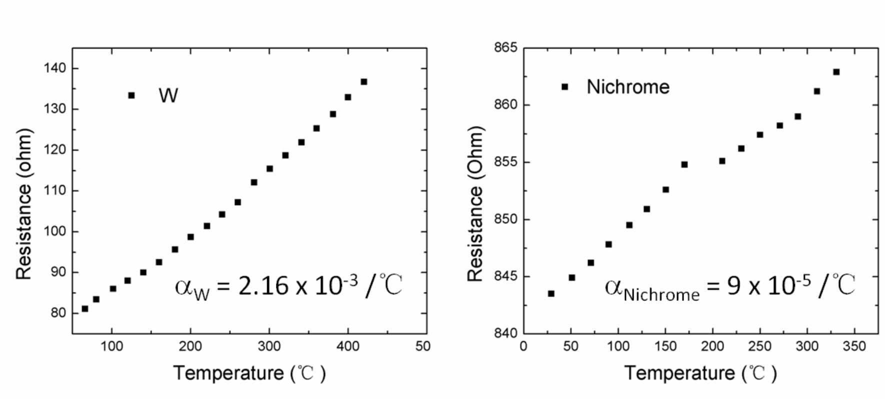


Figure 2.13: Calibration of TCR for heated stencil made by W and Nichrome.

2.4.2 Temperature Distribution on the Membrane

The temperature calculated from TCR is an average value over the heated area, however the actual temperature distribution on the membrane is not uniform. In the design of the resistive heater, we place the windows for stencil apertures in between the electrodes (in an area of 40 μm× 40 μm) . These areas are distributed across the membrane, which provides different temperature for investigating the effectiveness of unclogging. Thus, the temperature mapping of the membrane has to be studied in order to see the temperature difference between these areas.

First, the heated stencil was tested by using HP 4155B Analyzer with an increasing power until its glowing point in order to make the temperature variation visible. *Figure* 2.14a shows the glowing Ta/Pt coil in ambient conditions with an operation power of 130 mW. The brightest area in the center of the coil corresponds to the part with the highest temperature, which must be higher than the measured average value (~650 °C). The optical image validates that the Pt thin film visibly glows starting at around 600 °C [58]. As comparison, simulation with finite element method (FEM) was performed using Comsol 3.5a as the platform. A FEM model was created to simulate the temperature gradient on the membrane (*Figure* 2.14b). In the model, the membrane is modeled as SiN with 1mm×1mm in area and 500 nm thickness. The Pt heater is 200 nm in thickness and is placed on top of the SiN membrane. The boundary conditions fix room temperature on the border of the membrane, which confines the heat generated by the resistive heater on the heated stencil. Bias is applied on the cross-section of the big triangle electrode, which guides the current central heater. The result agrees very well with the optical image. Due the spiral layout of the electrode, a stronger thermal coupling effect must happen in the middle of the membrane, which decreases the temperature gradient in that area. The relatively uniform temperature distribution in the center of the membrane provides a stable thermal environment for the stencil apertures.

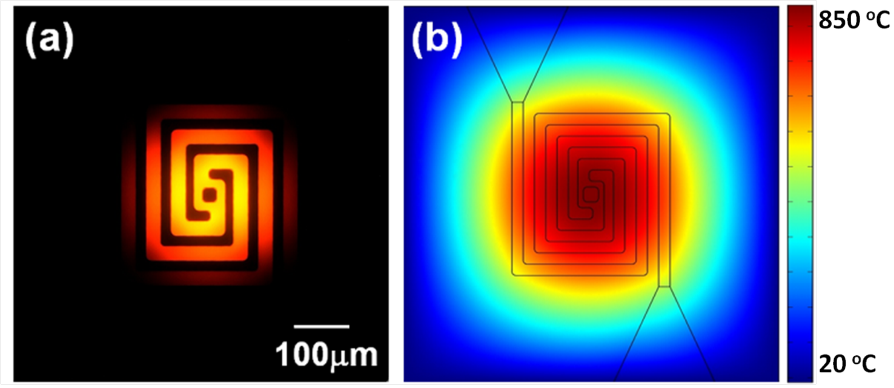


Figure 2.14: (a) Optical image of the glowing Ta/Pt coil in ambient conditions with an operation power of 130 mW. (b) Temperature distribution of the same structure by FEM simulation. The highest temperature is 850 °C in the center of the membrane.

Second, the temperature distribution was observed under an infrared (IR) microscope. From the temperature mapping, the local temperature can be directly read out. The QFI InSb IR FPA Camera (in collaboration with IEMN, Lille, France) was used, which has 0.1 °C step resolution and maximum working temperature at around 400 °C. The spatial resolution is 2.7 μm. Before taking the image, the detector was calibrated. The stage where we place the sample is heated up to ~ 40 °C to reach the sensible range of the detector. A reference image is first taken without applying power to the device. Then, voltage is applied to the device and images are taken. *Figure* 2.15 shows the IR microscope images which were taken for the same device at different applied voltages. Thanks to the high spatial resolution of the detector (2.7 μm), we can visualize the spatial details of the temperature mapping and read out the temperature at the place of interest. The temperature of the aperture windows are collected from the neighbour electrodes, as due to different emissivity of Pt and SiN, the temperature on SiN cannot be properly displaced [60]. Details will be discussed later. In *Figure* 2.15a, at

1.0 V bias, the temperatures of the aperture windows are 64.1 °C (A), 71.1 °C(B) and 74.3 °C(C). The temperature difference between aperture windows becomes larger when a higher voltage is applied, as shown in *Figure* 2.15b, where the temperatures are 313.2 °C(A’), 387.4 °C(B’) and 408.4 °C(C’). The difference between A(A’) and C(C’) increases from 10.2 °C to 95.2 °C. Because the maximum working temperature of the detector is at around 400 °C, we cannot visualize the temperature mapping at higher temperature. In order to understand the difference between aperture windows at high temperature range (>400 °C), we can extract the temperature values of these aperture windows at low range and fit the curve linearly to estimate the difference at high temperature range, which is basically a TCR for the exact point on the membrane, as shown in *Figure* 2.16.

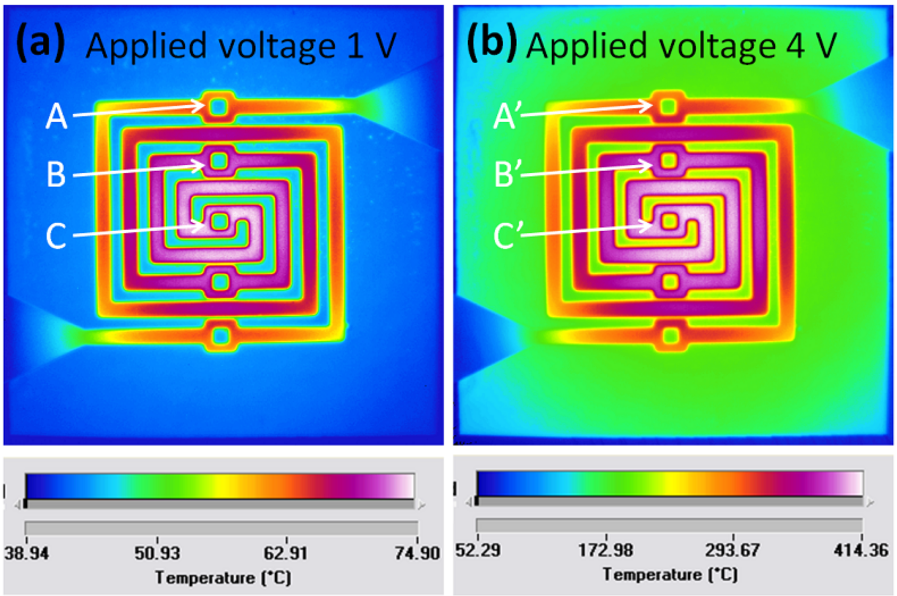


Figure 2.15: IR microscope images of a heated stencil working at different voltage. (a) at 1.0 V, the temperature of different aperture windows are 64.1 °C (A), 71.1 °C(B) and 74.3 °C(C). (b) at 4.0 V, the temperature of different aperture windows are 313.2 °C(A’), 387.4 °C(B’) and 408.4 °C(C’).

The local TCR value at the exact location point can also be extracted by using this method. For comparison, the average value of TCR we measured in section 2.4.1 is 2.2×10^{-3}/°C, while the TCR at the point of the middle aperture window is ~1.95×10^{-3}/°C, as shown in *Figure* 2.17. We selectively show the local TCR value measured for two different heater designs. The meander and coil shape heater showed almost equal TCR, α_A and α_B. The difference between the average TCR and the local TCR clearly demonstrates the nonuniform distribution

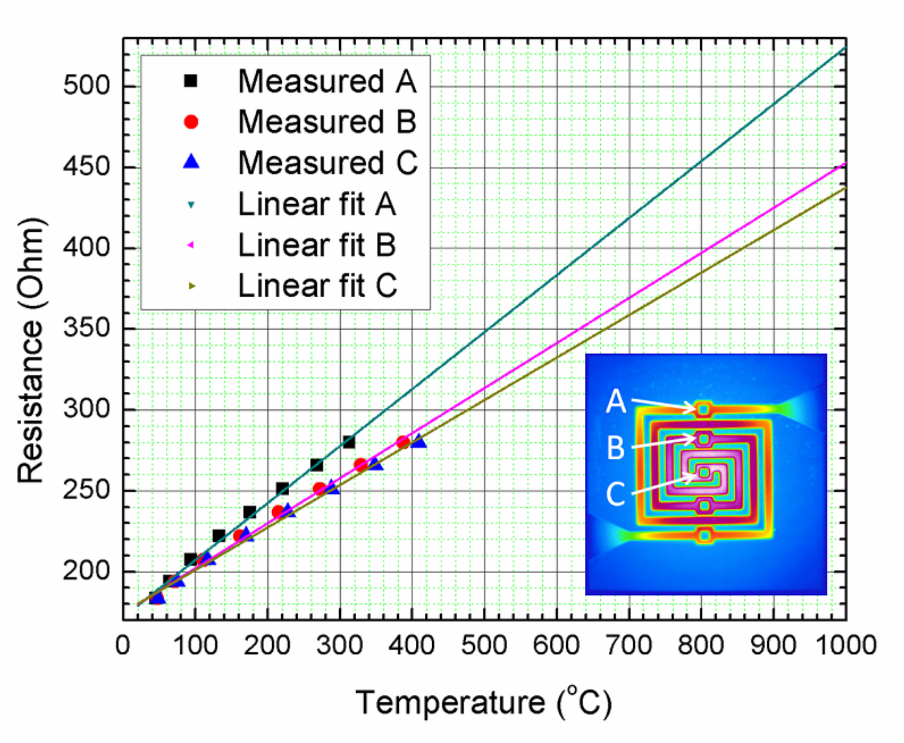


Figure 2.16: The diagram of linear fit to the temperature of each aperture window vs. the resistance, from which we can estimate the window temperature at high temperature range.

of temperature on the membrane. However, in the estimation of the temperature, we still use the average TCR value. As in principle TCR becomes temperature dependent at high temperatures, thus the relation between temperature and resistance becomes less linear. The average TCR would introduce less error in this situation.

As we can see from the IR images in *Figure* 2.15, the color of the SiN membrane is clearly different from that of the Pt heater arm. This is due to the difference in emissivity of the two materials. The value of emissivity is not adjustable locally on the system used for the IR measurements and therefore the graphics in *Figure* 2.15 illustrates a clear noncontinuous temperature profile across the membrane, as shown in *Figure* 2.18. The trenches in the profile represent the aperture window area (A, B and C). The difference between the Pt arm and the SiN aperture window becomes larger when temperature increases. As the temperature of the aperture window affects the effectiveness of unclogging the aperture, it is critical to know the actual temperature profile.

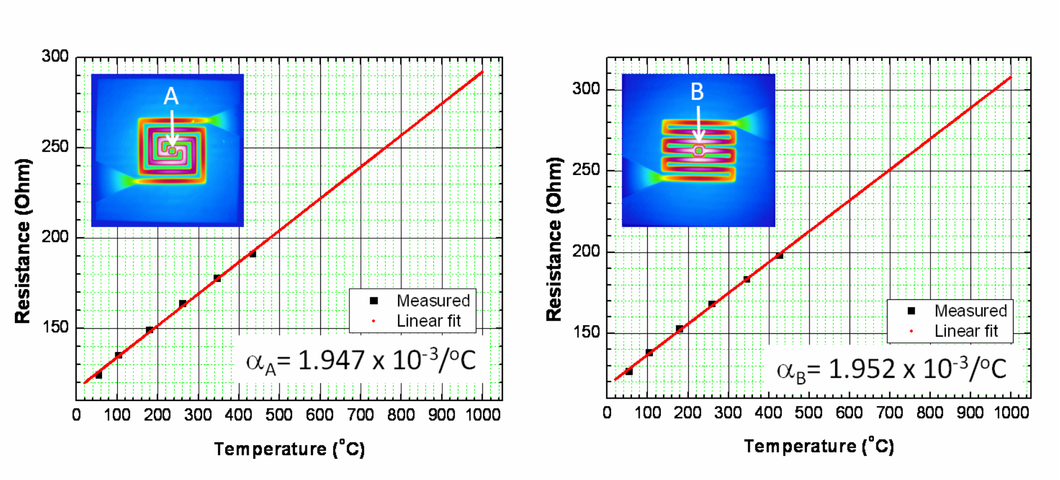


Figure 2.17: TCR measured from the IR images at exact points in the middle aperture window. The TCR for two different designs are showed here. α_A and α_B are almost equal, which is ~1.95×10^{-3}/°C.

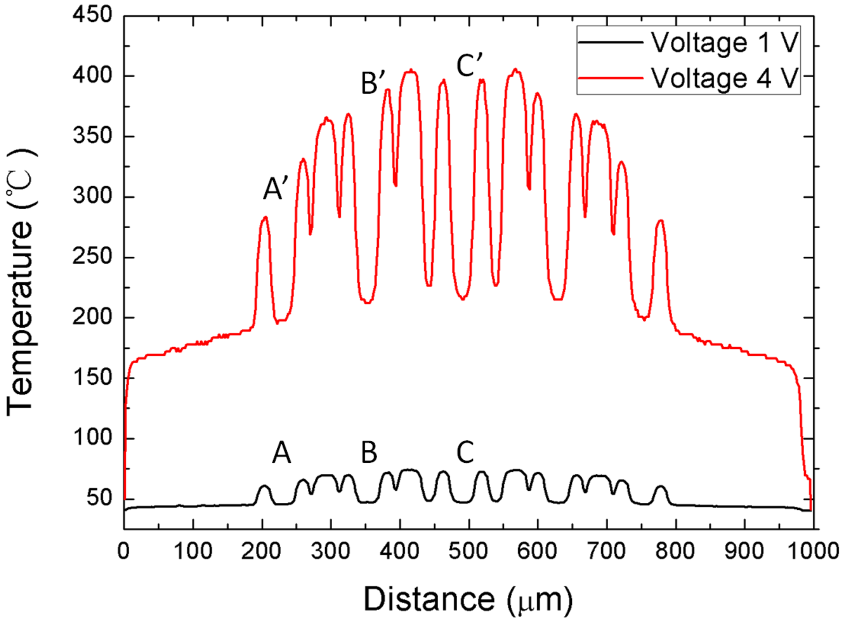


Figure 2.18: Temperature profiles of the heated stencil heated at different voltages. The aperture windows are captioned as A, B and C for 1 V, and A', B' and C' for 4 V. The profile shows that the aperture window has much less temperature than the neighbour electrodes, which is due the different emissivity of Pt and SiN in the IR measurement.

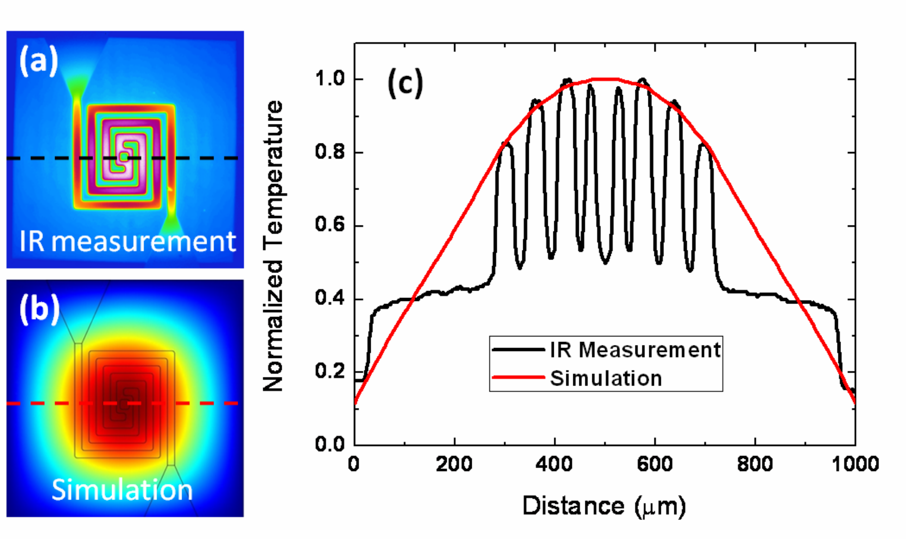


Figure 2.19: The comparison of the temperature profile between measurement and simulation at 1.0 V. A continuous profile is seen from the simulation while the distribution is noncontinuous in the measurement, which is due to the difference in emissivity between Pt and SiN.

To better understand the measured temperature profile, we compare the results with simulation, which shows a continuous temperature profile, as shown in *Figure* 2.19. We normalized the simulated temperature to the measured value with applied power of 1.0 V in order to only compare the profile. The profile of the measured temperature on Pt agrees well with the simulated profile. However, the value on SiN is dramatically lower, which is again due to different emissivity.

In order to visualize the temperature on the aperture window, we deposited 20 nm and 40 nm Pt on two identical devices to create a uniform emissivity area for the detector. The Pt was deposited on the backside of the membrane in order to prevent shortening of the heater. *Figure* 2.20 illustrates the temperature profiles from three devices with identical designs (one without Pt, one with 20 nm Pt and one with 40 nm Pt). The applied voltage is 3.0 V for all three devices. It is clear that more continuous profiles were observed with 20 nm and 40 nm Pt on the membrane, due to the lower emissivity difference between the membrane and the Pt arm. There are still slight steps on the profile from the SiN membrane to Pt arms in the case of 20 nm and 40 nm Pt coated membranes, which should be due to the different Pt thickness between the Pt arm (200 nm + 20/40 nm) and the Pt on the membrane (20/40 nm). The maximum

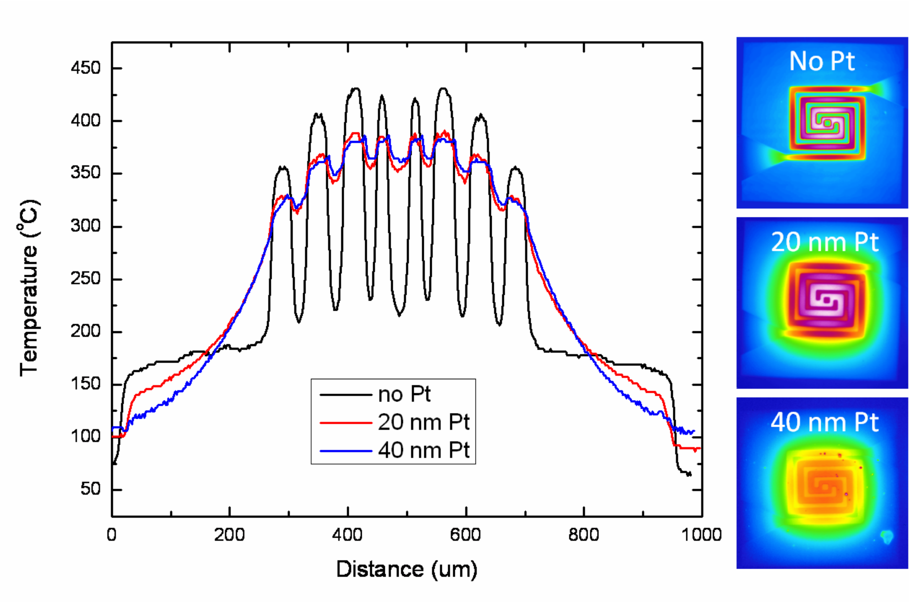


Figure 2.20: Temperature profiles of three heated stencils with identical design, without Pt, with 20 nm Pt and 40 nm Pt on the backside of the membrane, respectively. More continuous profiles were observed with 20 nm and 40 nm Pt on the membrane, due to the less emissivity difference between the membrane and the Pt arm. The applied voltage is 3.0 V for all three devices.

temperature for the Pt coated devices is lower than the non-coated one. It could be explained by the increasing of the thermal conduction through Pt on the membrane, which cools down the membrane. There is no big difference between the temperature profile of 20 nm and 40 nm Pt coated samples, which concludes that 20 nm of Pt coating is already enough for creating a uniform emissivity environment across the membrane. From this experiment, we conclude that the temperature of the aperture window area is within 50 °C from the neighbour Pt arms. Therefore, we can approximate the temperature of the aperture window to that from the Pt arms.

2.4.3 Temperature vs. Power

Using the TCR value of 2.2×10^{-3}/°C calibrated in section 2.4.1, the average temperature of the heated stencil membrane can be derived from the injected current and the corresponding voltage across the coil. This method does not include the thermal loss due to convection from the environment. Therefore, by monitoring the change in resistance, the temperature of the

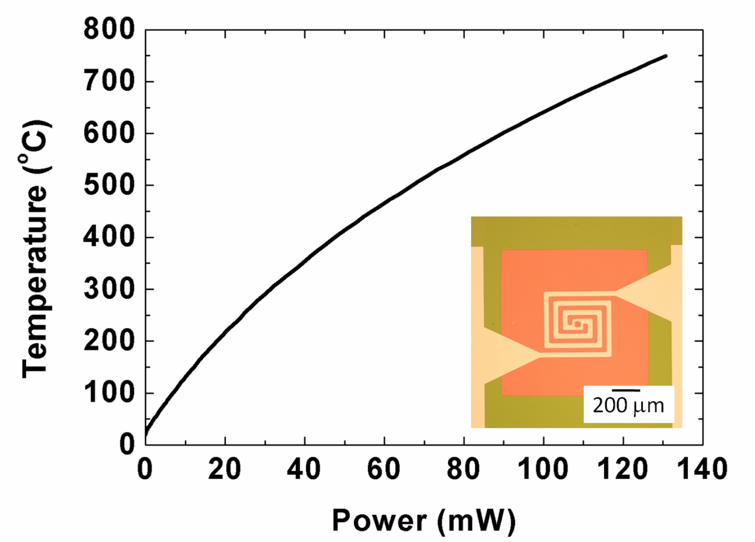


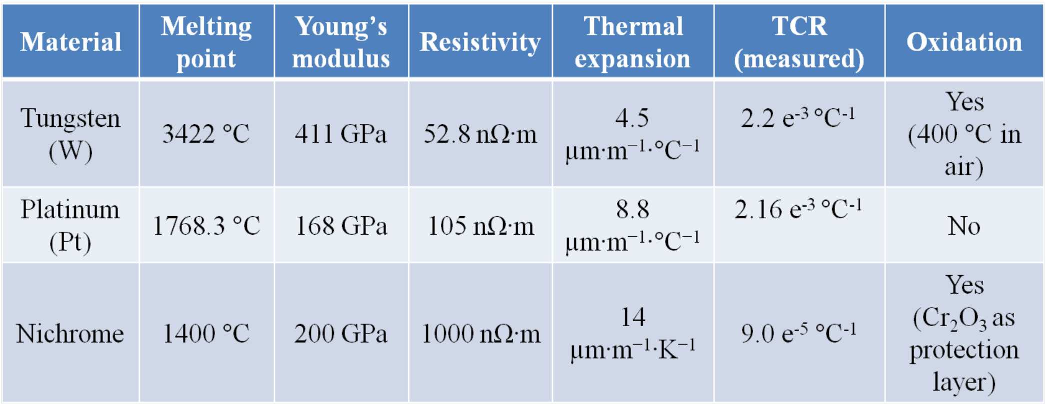
Figure 2.21: The average temperature of the membrane versus the applied power in ambient conditions.

membrane can be inferred both in air and in vacuum. *Figure* 2.21 shows the relationship between the average temperature and applied power for one of the heater designs in ambient conditions.

2.4.4 Different Heating Elements

There are many materials which can be used as the resistive heater, e.g. Pt [53, 61, 59], W [62, 63], TiN [64], Polysilicon [65, 66, 67], SiC [68], etc. The microhotplates made from these different materials have both advantages and disadvantages for the SL application, thus we have to carefully make the choice. The ideal heating element we desire should have these properties:

- High melting point T_m to obtain high temperature that allows high critical incident rate $v_n$of evaporated material
- High current density for a stable functioning at high temperature
- High thermal expansion coefficient to achieve large deformation towards the substrate for locally reducing the gap (introduced in Chapter 3)
- Chemically stable at high temperature, e.g. no oxidation



Material	Melting point	Young's modulus	Resistivity	Thermal expansion	TCR (measured)	Oxidation
Tungsten (W)	3422 °C	411 GPa	52.8 nΩ·m	4.5 $\mu m \cdot m^{-1} \cdot °C^{-1}$	2.2 e^{-3} $°C^{-1}$	Yes (400 °C in air)
Platinum (Pt)	1768.3 °C	168 GPa	105 nΩ·m	8.8 $\mu m \cdot m^{-1} \cdot °C^{-1}$	2.16 e^{-3} $°C^{-1}$	No
Nichrome	1400 °C	200 GPa	1000 nΩ·m	14 $\mu m \cdot m^{-1} \cdot K^{-1}$	9.0 e^{-5} $°C^{-1}$	Yes (Cr_2O_3 as protection layer)

Table 2.4: Material properties of three investigated heating elements, Pt, W and Nichrome

During our investigation, we have tried three different metals (Pt, W and Nichrome) to find the optimal one for our application. Each material has its advantages but also unfortunately has its disadvantages. Detailed comparison is following. *Table* 2.4 lists the typical values of the material property of these three metals.

Tungsten

Tungsten (W) has a very high melting point (T_m= 3422 °C [54]) and can therefore be used at high temperatures. For example, micro lamps with tungsten filaments can be operated up to 1200 °C. However, at these temperatures W oxidizes very fast, therefore vacuum conditions have to be applied [52]. In fact, tungsten is stable in an oxygen environment only for temperatures up to 400 °C [69]. Above 400 °C W starts to oxidize and the formed oxide layer is not protective to the residule W from further oxidation. For temperatures above 700 °C the oxidation rate increases dramatically, and around 900 °C W starts to sublimate, leaving the underlying tungsten even more exposed. These effects cause serious stability problems for thin films of tungsten. Besides, Tungsten has the lowest thermal expansion coefficient among these three metals, which gives the microhotplate made by W the least thermally induced deformation. This will decrease the effectiveness of locally reducing the gap between stencil aperture and the substrate by the thermally actuated membrane. Details will be shown in Chapter 3.

For fabricating the W based heated stencil, the process flow is similar to the Pt based heated stencil which is shown in *Figure* 2.9. 200 nm of W was sputtered and lifted off to form

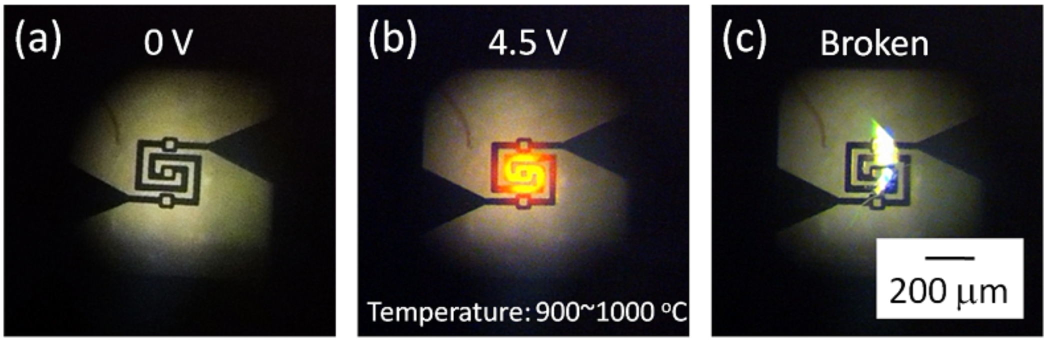


Figure 2.22: Heated stencil made by W resistive heater. The W coil is protected by ALD Al_2O_3 for preventing from oxidation at high temperature. (a) Apply 0 V. (b) W coil glows at 4.5 V, with average temperature of 900~1000 °C. (c) Failure of the W coil due to exceeding the maximum allowed power.

the pattern. The only different step is the annealing of the W after lift-off process for releasing the residual stress from the thin film deposition. The annealing conditions has been optimized for high temperature application [70]. The thermal annealing process was performed in a Centrothem tube. A nitrogen purge of 20 liter/min during 1 hour was performed to establish an oxygen-free environment before ramping up in temperature. In addition a flow of 10 liter/min H_2 was added. The heating and cooling rates were limited to 10 °C/min to prevent thin film delamination caused by high thermal stress. Once the temperature reached 1000 °C, it was maintained during 3 hours at a nitrogen flow of 10 liter/min. The annealing process changes the stress of the W thin film from 600 MPa compressive to 360 MPa tensile, which keeps the membrane flat after KOH releasing.

In our application, although the heated stencil will be operated in the evaporator, oxidation can still be observed, especially at high temperature due to residual oxygen in the chamber. To overcome this drawback, we developed a process that conformally passivates the W electrodes with Al_2O_3 using Atomic Layer Deposition (ALD). This prevents the oxidation of W in both ambient conditions and in vacuum. *Figure* 2.22 shows selected frames from a video which records the process of the heated stencil made by W coil glowing at 4.5 V applied bias in ambient conditions. Due to the protection of ALD Al_2O_3, its failure was caused by too much current and not oxidation.

Platinum

As we discussed before, Pt is an ideal candidate for making microhotplates, due to its high melting point and strong chemical inertness. The thermal expansion coefficient of Pt is in between that of W and Nichrome, which should provide a middle range thermal deformation among these materials. Although Pt is chemically inert, even at high temperatures, it is a good catalyst for numerous reactions, e.g. for Pt-catalyzed oxidation of hydrogen and Pt-catalyzed CPO of ammonia [71, 72]. It is known that on a Pt surface molecular oxygen breaks down into atomic oxygen, which diffuses quickly through the platinum along the grain boundaries [73]. It is clear that heaters should not initiate any catalytic reaction in our application: this can be accomplished by encapsulation the Pt thin films by the second LPCVD SiN layer. However, in order to adjust the orientation of the deformed membrane, it was discovered difficult to passivate the Pt heater and keep the desired orientation at the same time. Besides, the aging of Pt heater at high temperature which eventually leads to failure has been studied [49]. The electro-stress migration of the Pt atoms at high temperature resulted in a discontinuity in the heating element [53], and the degradation of Pt heater at temperature higher than 700 °C has also been reported **(author?)** [74], which is also a reliability issue we encountered in the experiments.

Nichrome

Nichrome is a non-magnetic alloy of nickel, chromium, and often iron, usually used as a resistance wire. The Nichrome we used to fabricate the heated stencil has 75% Ni, 20% Cr and 5% Fe. Due to its relatively high electrical resistivity and resistance to oxidation at high temperatures, it is widely used in electric heating elements, especially in our daily life, such as in hair dryers, electric ovens, soldering irons and toasters. It has a melting point of about 1400 °C. Due to its high resistivity compared to Pt and W, as shown in *Table* 2.4, simulation shows that Nichrome can achieve the highest temperature in comparison to Pt and W at the same power consumption. However, it is not common to see Nichrome used as a microheater, only few papers describe its application [75, 76], probably due to the difficulties in fabrication. One key property of Nichrome that we are interested in is its high thermal expansion coefficient, which provides Nichrome based heated stencil the maximum thermal deformation for reducing the gap between the stencil and the substrate. Comparison will be shown in Chaptor 3. The Nichrome will form a dense oxidation layer Cr_2O_3 at high temperature

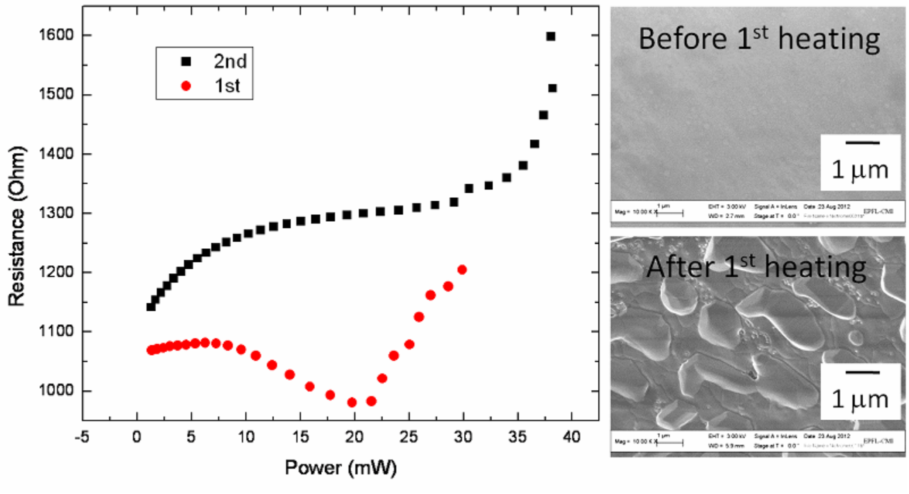


Figure 2.23: The resistance of Nichrome based heated stencil as function of applied power in vacuum. It shows the different behavior of Nichrome based device operated at the same condition for two cycles. During the first operation, self-annealing of Nichrome happened which gives the abnormal resistance vs. power behavior. SEM images show the clear difference before and after the first heating. The second heating shows more reasonable behavior.

that prevents its further oxidation, which means Nichrome is suitable for applications in both air and vacuum.

The fabrication of the Nichrome based heated stencil follows the process flow for W based device. 200 nm of Nichrome was thermally evaporated. The difference here is the annealing temperature after lift-off process, which is 300 °C, for reducing the stress. This annealing temperature is not optimal as we will operate the device at much higher temperature, which creates stability issues. *Figure* 2.23 shows the resistance of Nichrome based heated stencil as function of applied power in vacuum. The first time heating shows strange resistance vs. power behavior, due the self-annealing of Nichrome during the heating. SEM images clearly illustrate the different grain size before and after the first heating. As the heating process was performed in vacuum, there should be no oxidation. Therefore the SEM images we see should be the Nichrome. The second heating shows more reasonable behavior at beginning. When the power is larger than 35 mW, the resistance increases dramatically until the device fails, which is due to the stability issue caused by the electro-migration.

We can conclude the comparison of these three heating materials as following:

- Tungsten is suitable for high temperature application. However, it oxidizes at high temperature, leading to stability issue. The relatively low thermal expansion coefficient limits the functionality of another very important feature of heated stencil, which is the gap reduction by thermally actuating the membrane towards the substrate.
- Platinum is chemically inert at high temperate. The thermal expansion is in the middle range for providing desired membrane deformation. The electro-stress migration at high temperature causes stability issue. For our application, as long as the temperature stays in the safe range, Pt is the optimal choice among these three metals by comprehensive consideration.
- Nichrome has the highest thermal expansion coefficient among three materials, which gives it the best performance in terms of membrane deformation. It oxidizes at high temperature, but the oxidation layer is protective for the residual metal film. However, the self-annealing behavior of Nichrome at high temperature induces repeatability concern. More investigation in the fabrication process would be needed to optimize the performance.

Figure 2.24 shows the comparison of the temperature vs. power in ambient conditions for the heated stencil made by these three materials. The tested devices have identical design, only with different heating materials. It clearly shows that Nichrome gives the highest temperature, but the behavior is strange due to the self-annealing during heating. Pt allows the maximum applied power, with maximum temperature in between Nichrome and W. Therefore, a comprehensive analysis shows that Pt based devices are more suitable for our application.

2.4.5 Failure analysis

There are few failure modes of the heated stencil, depending on how the power is applied. Generally, fast ramping up of the power that is applied to the heated stencil will make the membrane mechanically break, which should be caused by its increasing deformation. Slow ramping rate usually allows higher applied power to the device. The device eventually fails electrically by exceeding the maximum current density. *Figure* 2.25 shows the different failure modes of Pt based device by fast ramping (1 V/sec) and slow ramping (1 V/min).

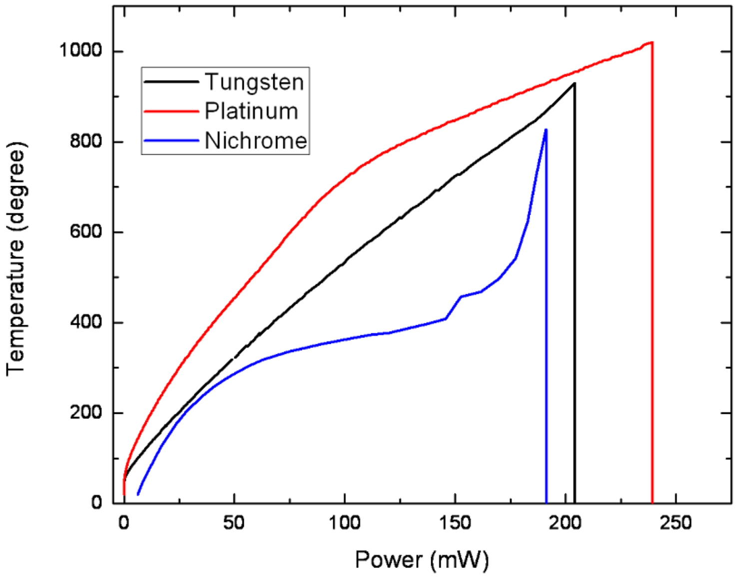


Figure 2.24: The comparison of the temperature vs. power in ambient conditions for the heated stencil made by three materials, W, Pt and Nichrome. The heated stencils have identical design.

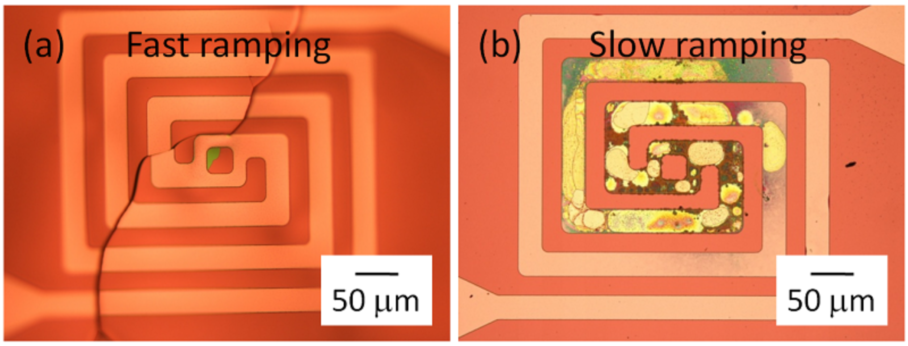


Figure 2.25: The different failure modes for fast ramping and slow ramping. The illustrated device is made of Pt. (a) Fast ramping (1 V/sec) breaks the membrane, due to the deformation of the membrane. (b) Slow ramping (1 V/min) fails the device electrically by electro-stress migration.

We also compare the failure modes with slow ramping between the devices made by different heating materials, as shown in *Figure* 2.26. For Tungsten coil, we can clearly see the oxidation which correlates with the temperature distribution. There is a thickness gradient of the oxidized layer which is illustrated in the image by the coloring effect. The breaking point A happened in the center of the membrane which has the highest temperature. It should be due to both effects, the oxidation and the electro-migration, as the break point A in the back side illuminated image is almost transparent. For the Nichrome coil, we can also see the oxidation effect. However, as Cr_2O_3 forms a protective layer that prevents further oxidizing of the residual metal, we only observe an oxidation layer with uniform thickness. The breaking point B in the back side illuminated image is not transparent, which indicates the failure mechanism should be due to exceeding the maximum current density. For Platinum coil, as aforementioned, the slow ramping creates electro-stress migration at high temperature that eventually fails the device. We can see a large area of degradation of Pt because of this phenomenon.

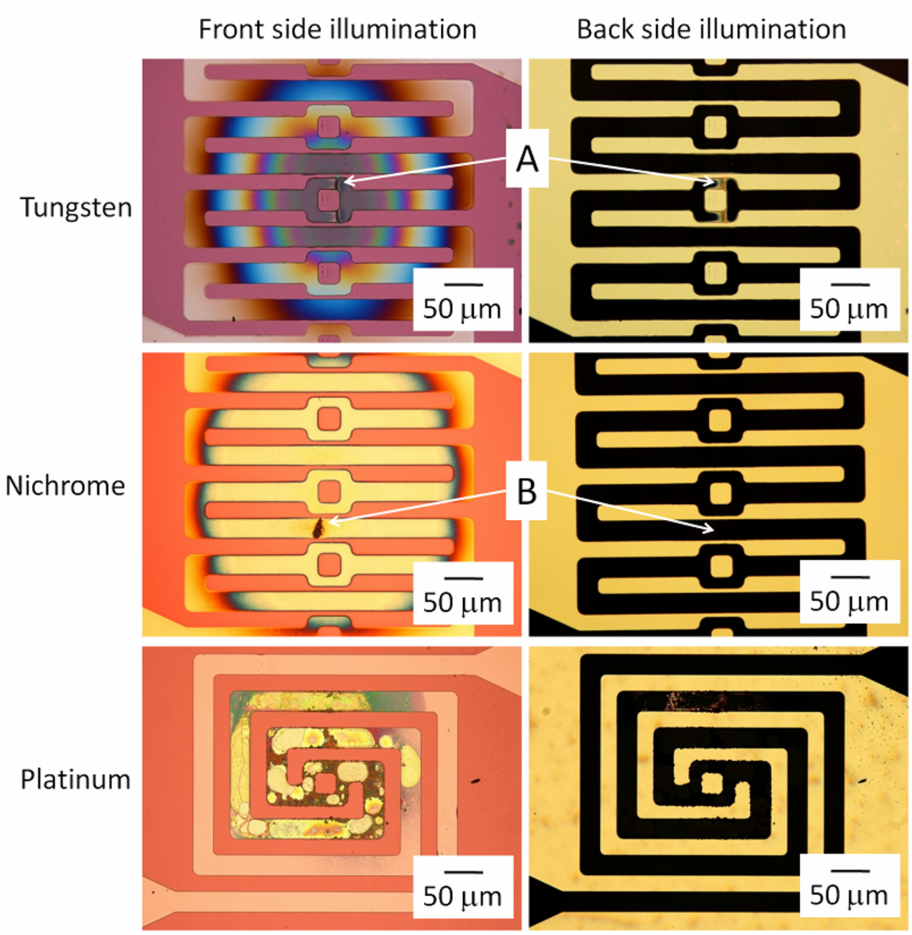


Figure 2.26: Micrographs of failure modes at slow ramping for different heating materials. Images in the left column were taken with front side illumination while images in the right column were taken with back side illumination, where the membran is transparent to light. A is the failing point for Tungsten coil and B is failing point for Nichrome coil.

2.5 Heating Pre-deposited Metals on Pt-based Heated Stencil

Before using the heated stencil for evaporation experiments, we evaluated the device by heating the membrane in vacuum with pre-deposited metal. Both Al and Au were first deposited on the membrane, then the device was heated in ambient conditions or in vacuum. When the device is placed in vacuum, it is electrically connected through feedthroughs into the vacuum chamber. The purpose of this set of experiments is to see the effectiveness of reevaporation of the pre-deposited metal, which provides useful information for later heating the stencil during evaporation. The tested microhotplates in this set of experiments were provided by Dr. Danick Briand from SAMLAB EPFL during the beginning of our exploration.

2.5.1 Investigation on Pre-deposited Al

In ambient conditions

First, as Al has low melting point (660 °C), we investigated the behavior of heating pre-deposited Al on the membrane of microhotplate in ambient conditions to understand the influence of temperature on the metal film. 10 nm of Al was deposited on the front side of microhotplate, which has embedded Pt electrodes in LPCVD SiN. The microhotplate was powered by 0.5 V step voltage till 6.0 V, with each step applied for 10 s. Micrograph images were taken at each step to observe the morphological change on the Al film. *Figure* 2.27 shows selected images to illustrate the transformation. The Al film started to show observable change from 4.0 V applied voltage, which corresponds to average temperature of 430 °C. As the temperature increases with applied voltage, the transformed area becomes larger. When the temperature reaches 611 °C with 6.0 V applied voltage, the Al film on top of the Pt coil completely transformed, as shown in *Figure* 2.27e. The image taken with back side illumination (*Figure* 2.27f) reveals that the transformed area becomes more transparent than the non-transformed Al film. Because the device was heated in air, we consider the transparent area should be due to the oxidation of Al, instead of reevaporation that makes the area transparent. XPS analysis also testified that the transformed area has only Al_2O_3.

In vacuum

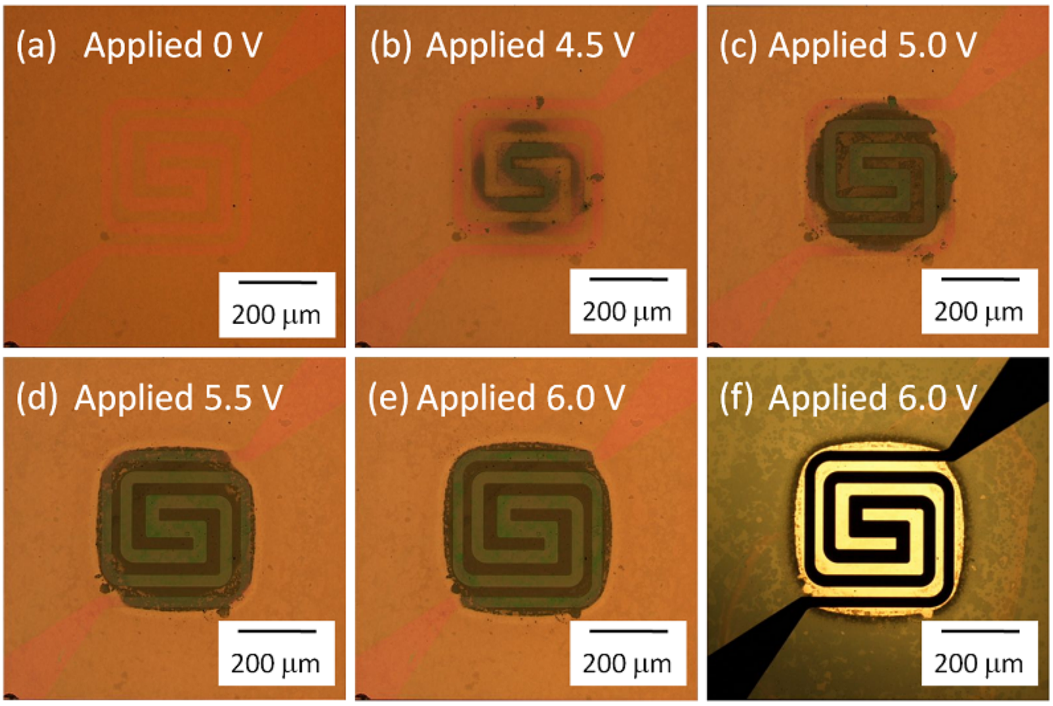


Figure 2.27: Optical images of 10 nm Al coated microhotplate heated in ambient conditions. (a)-(e) Images with front side illumination, applied voltage from 0 V to 6.0 V. The temperature corresponding to each applied voltage are 448 °C (4.5 V), 507 °C (5.0 V), 561 °C (5.5 V), 611 °C (6.0 V). (f) Image with back side illumination, applied 6.0 V.

As our application is used in the evaporation system, the next step is chekcing the behavior of heating metal film in vacuum. 20 nm of Al was deposited on the front side of membrane. The device was then place in a small vacuum chamber which is not designed for high vacuum application. The membrane was heated for 10 s by using 3.5 V with 4.6×10^{-4} mbar vacuum level. The corresponding temperature is 470 °C. *Figure* 2.28a shows the transformed area in the center of the microhotplate. Back side illuminated image (*Figure* 2.28d) reveals again the transparency of this transformed area. The expectation of this experiment is to have the Al in the transformed area reevaporated. However, XPS analysis indicates that the transformed area is still due to the oxidation of Al. *Figure* 2.28b shows the XPS analysis on the transformed area. Only the Al_2O_3 peak was captured. For comparison, two peaks were observed on the non-transformed area, which indicates the existance of both Al and Al_2O_3. The forming of Al_2O_3 in the transformed area could be explained by the low vacuum level, which makes Al oxidize at certain temperature (*Figure* 2.29). Thus higher level of vacuum would be needed in the heated stencil application. The Al_2O_3in the non-transformed area should be contributed from the native oxidation layer of Al.

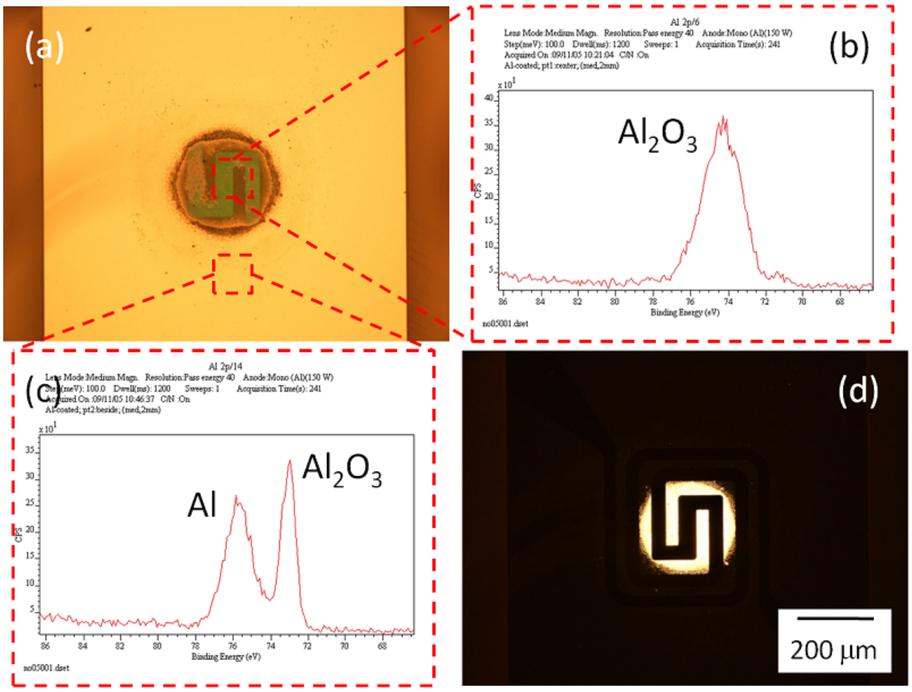


Figure 2.28: (a) Microscope image of the membrane after heating by using 3.5 V with 10 s in vacuum (4.6×10^{-4} mbar). Initially the membrane was covered by 20 nm Al on the backside. The heating temperature is 470 °C. (b) XPS result shows that only oxidized Al exists in the center of the membrane. (c) XPS result shows that the area outside of the centre of the membrane has both metallic Al and oxidized Al. (d) Back side illuminated microscope image indicates that the transparent area on the membrane is corresponding to the area where Al has been oxidized.

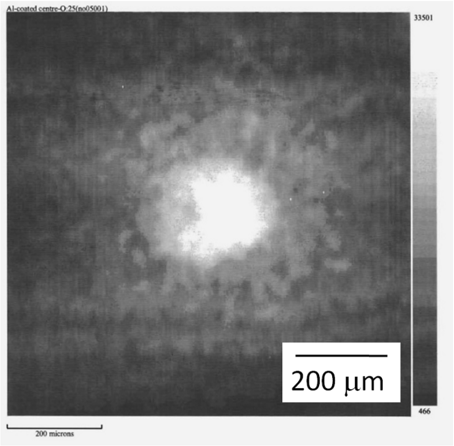


Figure 2.29: XPS mapping of oxygen on the membrane. The high concentration of oxygen in the transparent area indicates the formation of oxidized Al due to high temperature.

2.5.2 Investigation on Pre-deposited Au

The previous investigation on Al indicates that it is not a proper metal for this experiment due to the oxidable property even in vacuum. Au was then selected as the metal for its relative low melting point in the noble metal family. Similar experiments were carried out in both air and vacuum. *Figure* 2.30 shows the SEM images of different thickness of Au thin film after heating in vacuum. The temperature is 700 °C with 3.5 V applied voltage. AFM images were taken afterward, which show that the continuous Au thin film before heating transformed into many isolated Au islands with height much bigger than the initial thickness. From this experiment, we observed the morphology change of the Au film. As we calculated the reevaporation rate for Au at 700 °C is 4.4×10^{-5} Å/s (section 2.2), it is expected that a long heating time would be needed to reevaporate the Au film. As for the sample with 2 nm Au, a much longer heating time (10 min) was performed later with 3.0 V in vacuum. SEM images show that the number of small islands reduces while the big ones remain there.

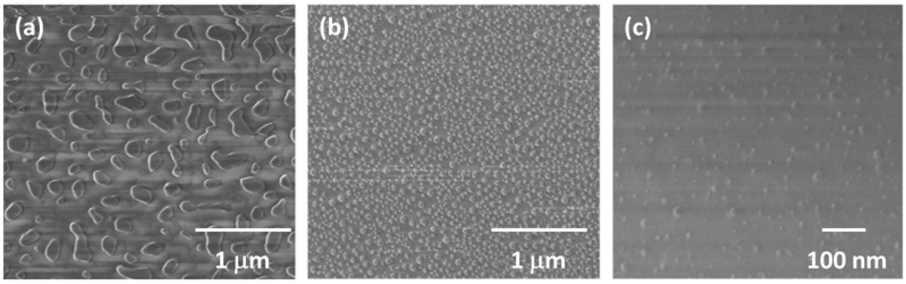


Figure 2.30: SEM images of different initial thickness of Au thin film after heating in vacuum. (a) 10 nm initial thickness, heated by using 3.5 V with 10 s in vacuum (2.5×10^{-4} mbar). (b) 5 nm initial thickness, heated by using 3.5 V with 10 s in vacuum (4×10^{-4} mbar). (c) 2 nm initial thickness, heated by using 3.5 V with 10 s in vacuum (4×10^{-4} mbar). The heating temperature is 700 °C at 3.5 V.

Further data analysis reveals that the applied voltage in order to achieve certain temperature is related to the metal film on the membrane and the environment around (*Figure* 2.31). The same device has different temperature vs. power behavior due to the difference of thermal environment. In our case there are three main mechanisms of thermal loss, the convection through air, the conduction through electrode and the radiation to the environment. In air, more power would be needed to achieve certain temperature due to large contribution of the thermal convection through air. However, in vacuum, the thermal loss is mainly due to the radiation. Thus less power would be needed to achieve the same temperature. Heat conduction through electrode exists in both situation, which is not the cause of the difference. However, when the membrane is coated with metal, the heat conduction through the metal thin film becomes an important factor to the thermal loss, which makes this situation in between the case of vacuum and air. Certainly the thicker the metal thin film is, the more heat conduction will be, thus more power will be needed to reach the same temperature. Potentially this kind of microhotplate is able to be used to monitor both vacuum level and deposited metal thickness in-situ. Pressure sensor made of microhotplate has been reported [63].

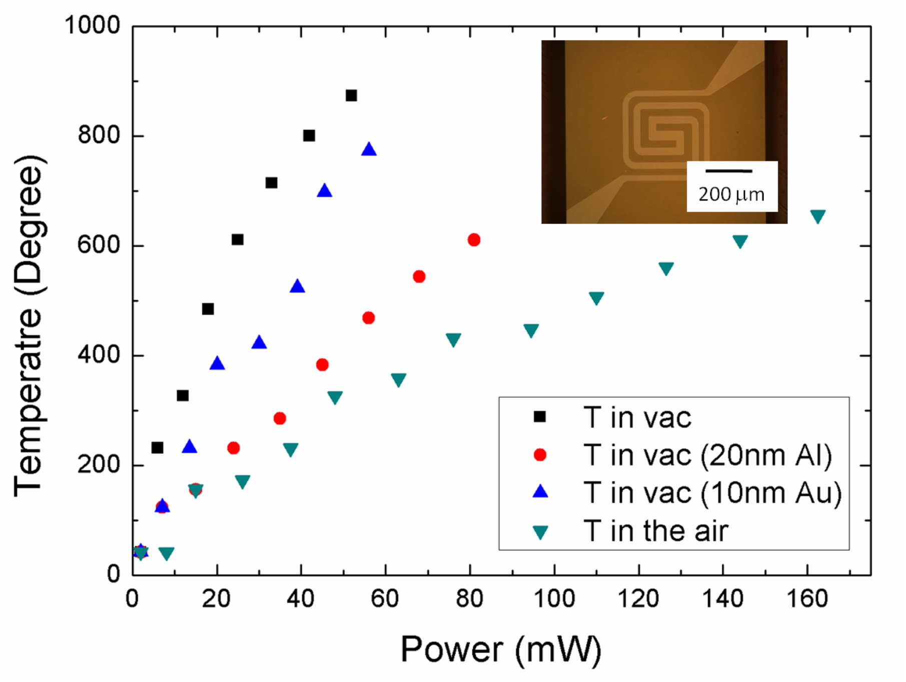


Figure 2.31: Temperature of the microhotplate as function of applied power.

2.6 Clogging-free Apertures by using the Heated Stencil

In this section, we present the results showing the clogging-free apertures by using the heated stencil. The heated stencil was placed on a Si substrate in an E-beam evaporator, as schematically illustrated in *Figure* 2.32. The embedded electrodes were powered by a DC power source. A constant voltage was applied and the current through the heater was monitored during the whole evaporation process. The membrane was heated in vacuum (2.3×10^{-6} mbar) to 67 mW before evaporation to achieve an average temperature of ~800 °C. This temperature indicates that the critical incident rate for Al should not be larger than 0.2 Å/s (*Figure* 2.7) if we intend to eliminate the condensation on the membrane. However, as we learned that the temperature in the center of the membrane is higher than the average, from the local TCR value we can estimate that the it is ~ 890 °C in the center membrane, which corresponds to a critical incident rate that is allowed to be larger than 1.0 Å/s. The optimal evaporation rate is a balance between a maximum required value for minimizing condensation of the material on the heated membrane, and a minimum set by the requirement of having enough material patterned through apertures onto the substrate. In this experiment, an evaporation rate of 0.5 Å/s is chosen for the sake of not pushing to the limit of the device, and this rate can still be used for patterning. Due to the thermal conduction of the metal condensing on the surface of the less hot membrane, the temperature would be continuously decreasing if the power is kept constant during the evaporation. Therefore, a gradually increased input power was applied in order to maintain the variation of the temperature in time as small as possible. *Figure* 2.32a and *Figure* 2.32b show the back side illuminated optical images of the heated stencil before and after the deposition of 120 nm Al. Usually 120 nm of Al should be completely nontransparent in visible light. Therefore, in *Figure* 2.32b, the transparent part in the center of the stencil after deposition indicates the presence of very little Al. The whole process was done in 2.3×10^{-6} mbar vacuum environment, which should avoid the oxidation of Al.

This transparent part corresponds to the hottest area during evaporation. The stencil apertures in this area on the non-heated membrane and the heated one are compared from both sides of the membrane, as shown in *Figure* 2.33. The heated membrane and the non-heated membrane were placed at the same time in the evaporator for comparison. A clear 300 nm shrinkage of the aperture was observed on the non-heated membrane whereas no clogging was found on the heated one. We can even observe the grain boundary of Al entad grows, which reduces the effective size of the aperture (*Figure* 2.33b). A dense Al film can be seen on the back side of the non-heated membrane (*Figure* 2.33a). On the heated one, the back side SiN surface (*Figure* 2.33c) looks different from the front side SiN surface (*Figure* 2.33d), indicating the existence of a very thin condensed Al film. This result validates the functionality of the heated stencil for having clogging-free apertures.

Theoretically, the re-evaporation rate in the center area (~ 1.0 Å/s) is larger than the

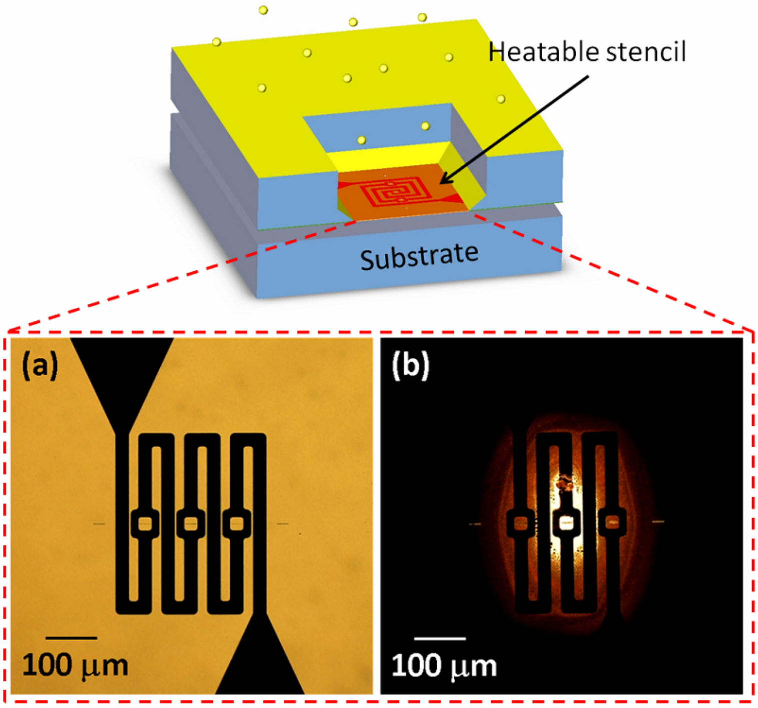


Figure 2.32: Schematics of the heated stencil for SL and optical image with illumination from the back side of the microscope. The heated stencil (a) before and (b) after 120 nm Al deposition with heating power of 67 mW in vacuum. The transparent part in the center of the stencil after deposition indicates the presence of very little Al.

incident rate (0.5 Å/s). Therefore, no condensation should happen in this area, which is proved by *Figure* 2.34a. In the center area, the embedded Pt coil can be clearly observed through the transparent SiN membrane, due to the very little condensation of Al. As the temperature descends from the center to the border, the corresponding reevaporation rate is no longer larger than the incident rate (0.5 Å/s) at certain point, where condensation of Al will be expected. *Figure* 2.34b, c, d show different surface morphology that corresponds to different temperature ($T_A > T_B > T_C$). Isolated Al islands were formed on the surface in T_B area, which indicates that the corresponding re-evaporation rate in this area is smaller than the incident rate. However, the condensed Al still has the mobility obtained from the hot membrane to move around to form big islands. In T_C area, we observe a continuous Al film, implying that the reevaporation rate is much smaller so that a dense film can form. However, this dense film is much thinner than the totally deposited thickness of Al, which is 120 nm. *Figure* 2.34e illustrates the SEM image taken from the front side of the membrane through the aperture, showing a thickness of 70 nm Al film formed in T_C area. This is due to the partial

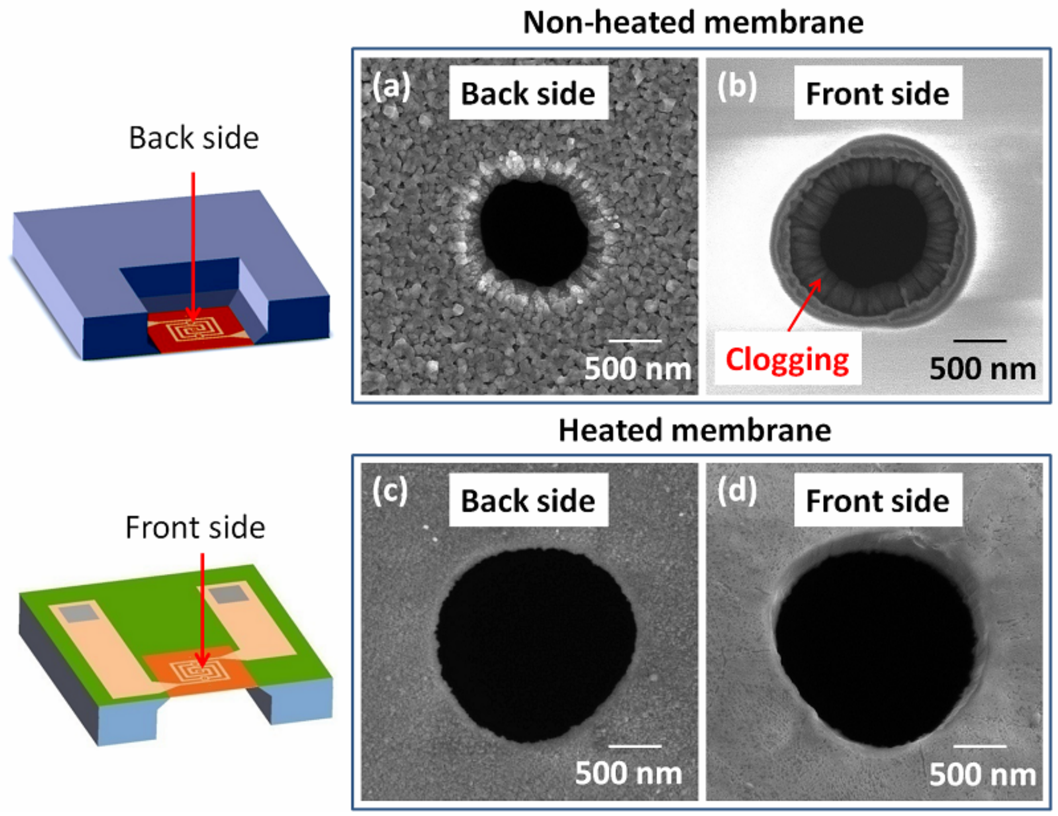


Figure 2.33: SEM images of apertures in the center of the heated and non-heated membrane coated with 120 nm Al. (a) The back side and (b) the front side of aperture on the non-heated membrane, 300 nm size reduction in diameter due to the clogging was observed; (c) The back side and (d) the front side of the aperture on the heated membrane. No clogging was observed. The back side of the heated stencil which is exposed to the Al flux shows very little Al condensed on the surface.

reevaporation of the deposited metal. As comparison, no obvious Al film can be observed through the aperture in T_A area, as shown in *Figure* 2.34f.

This set of experiments indicate that avoiding condensation sensitively relies on the temperature. However, it does not mean that the effectiveness of unclogging the aperture also significantly depends on the temperature. As we see from *Figure* 2.34e, though a layer of 70 nm Al formed on the surface, the aperture was not clogged as the Al did not grow on the side walls of the aperture. That implies the unclogging of aperture could also happen at the temperature that is lower than the incident rate corresponded temperature. On the other hand, as we have pushed the applied power close to maximum value in order to get high temperature (~ 800 °C), the Pt heater gradually degenerated due to the electro-stress migration, which cause stability

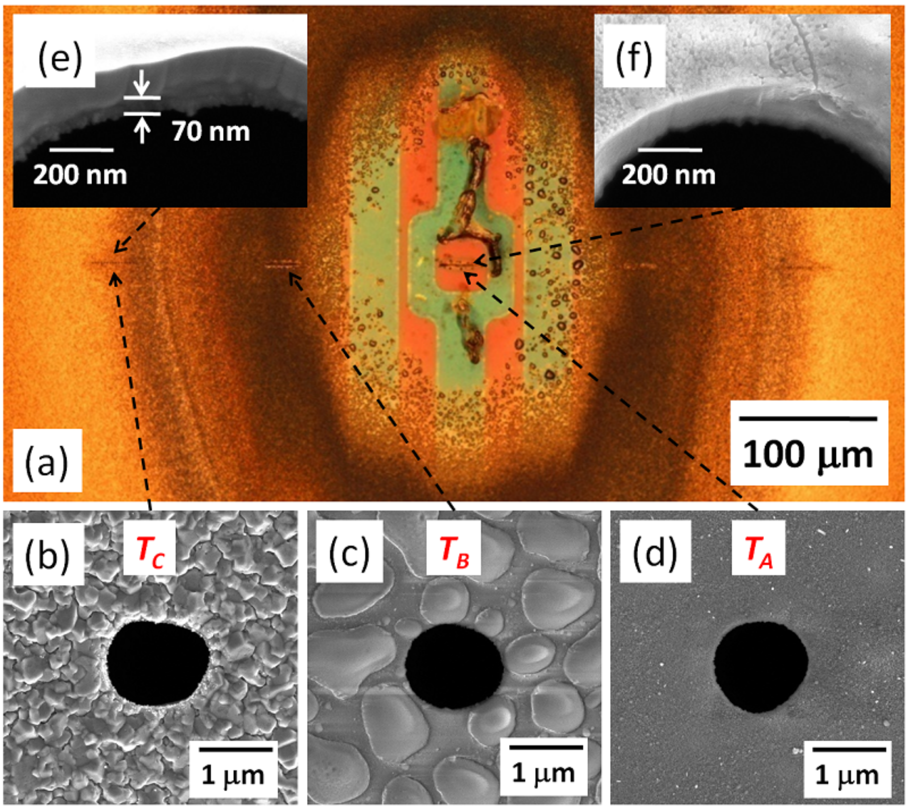


Figure 2.34: Optical and SEM images of the heated stencil after 120 nm Al deposited on the membrane. (a) Optical image of the back side of the membrane. The embedded Pt coil can be clearly observed as very few Al condensed on the surface. (b), (c) and (d) SEM images of the apertures on different temperature area of the membrane. $T_A > T_B > T_C$. (e) Zoom-in of the aperture in T_C area from the front side of the membrane, 70 nm thick Al was observed. It is thinner than the deposited 120 nm Al due to the partial reevaporation of the deposited metal. (f) Zoom-in of the aperture in T_A area from the front side of the membrane. No obvious Al film can be observed.

concern. Therefore, in later experiments, we only create the temperature in the stable range. Though it cannot completely avoid condensation, clogging free aperture can be still achieved.

2.7 Conclusions

In this chapaer, we have presented a novel stencil concept with an integrated microhotplate on the stencil membrane to prevent aperture clogging. We demonstrate that the stencil can be locally heated up by the integrated resistive microheater in order to prevent material condensation on the stencil membrane, which is the ultimate method to prevent clogging of apertures. At the same time, material flux can pass through the stencil aperture for patterning purpose.The kinetic theory of gases and the classic Hertz-Knudsen equation has been used to theoretically describe the process of minimizing thin film condensation on the substrate or stencil membrane. The corresponding temperature for certain critical incident rate of different materials has been calculated, which plots a practical process window for our application. The heated stencils fabricated from three different heating materials (Pt, W and Nichrome) are studied and characterized, revealing that Pt is the optimal heating material among these three materials for our application. However, Pt has its temperature limit at which the stability issue becomes a concern, due to electro-stress migration. Therefore, a better heating material that can work stably at high temperature (> 1000 °C) is required to extend the range of applicable metal. The results of heating pre-deposited metal on the membrane provides us useful information for later heating the stencil during evaporation. By comparing between the heated and non-heated stencil, the concept of unclogging the aperture by heating up the membrane is clearly demonstrated. Due to the limit of the maximum achievable temperature (~ 900 °C), we only present the Al deposition on the heated stencil. Membranes with achievable temperature higher than 1000 °C could enlarge the application range to other metals.

In next chapter, we will introduce another major advantage of heated stencil, which is locally reducing the gap between the stencil membrane and the substrate by thermal actuation of the membrane. The reduced gap provides better resolution in terms of decreasing the blurring of the pattern on the substrate. Systematic investigation of controlling the orientation of membrane deformation will be shown.

3 Actuated Gap Reduction by Using Heated Stencil

3.1 Introduction

In stencil lithography (SL), it is very unlikely that a perfect contact between the stencil membrane and the substrate could happen. There is usually a gap (~μm) between the membrane and the substrate, which is due to several factors, such as the wafer curvature, membrane stress and any topography on the substrate. It is shown that the blurring of the stencil patterned structures on the substrates is associated with the gap [40]. In full wafer scale SL, the gap becomes a more uncontrollable issue due to the the curvature of the wafer, which creates nonuniform gaps across the wafer. Compliant stencil with out of plane membrane has been used to locally reduce the gap in full wafer scale [77]. In this section, we will introduce another method for local gap reduction with the heated stencil by thermally actuating the membrane towards the substrate. This is especially meaningful for full wafer scale dynamic stenciling, as usually a bigger gap (~50 μm) is intentionally left to allow free motion of the stencil. By locally reducing the gap using the thermal actuated membrane, combining with the function of unclogging the aperture which is introduced in Chapter 2, the heated stencil as a platform brings a new concept to SL which is suitable for both static and dynamic stenciling application with better resolution and longer life time, as schematically shown in *Figure* 3.1.

Thermal actuation is one of the fundamental mechanisms that has been widely used in micromechanical system for making micro-membrane based [78] or cantilever based actuators [79, 80]. Comparing to other actuation principles, such as piezoelectric, electrostatic

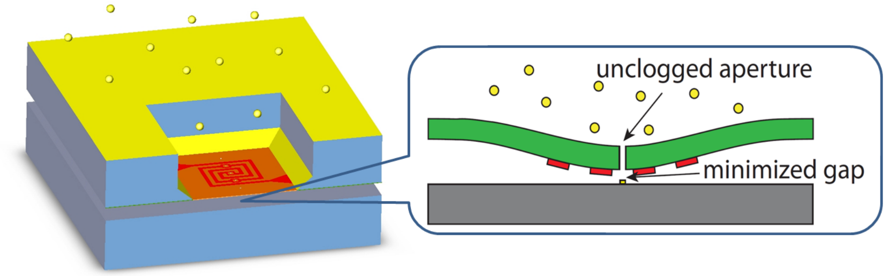


Figure 3.1: Schematics of the heated stencil providing clogging-free aperture and minimized gap by thermal actuation of the membrane.

and electromagnetic, thermal actuation usually provides easier way to construct the actuator. Thermal actuation schemes are generally based on either the linear/volume expansion or phase transformation of the materials. In addition, thermal actuation has been shown to provide significant displacement, force and moderate activation time due to the scale effect [81]. The heated stencil is basically a membrane based microhotplate, which can also be thermally actuated to create out of plane displacement. By controlling the orientation of the deformed membrane towards the substrate, the gap between the stencil aperture and the substrate can be locally reduced, which offers better patterning resolution in terms of reducing the blurring surrounding the main deposited structure. Due to the needs of application, many studies for microhotplate only focuses on the optimization of the temperature distribution on the membrane, e.g. optimizing to have uniform temperature distribution by integrating silicon island on the membrane [60] or by altering geometry of the resistive heater [82]. The membrane deformation is often discussed when reliability becomes a concern [49, 53]. As the membrane based thermal actuator allows the membrane to deform either upwards or downwards, depending on the initial strain and the relative thermal expansion between metal electrode and the SiN membrane, tailored geometry would provide us the control of the deformation direction. Two bending directions of the thermally actuated membrane has been shown by integrating two individual actuators on the membrane [78]. In our application, the heated stencil is desired to bend upwards so that the gap can be reduced.

In this chapter, we present the reduction of the gap by thermal actuation of the membrane. The deformation of the membrane induced by temperature will be introduced in section 3.2.

Tailored geometry of the heated stencil for achieving upwards bending will be presented with both simulation and experimental results in section 3.3. Another important issue concerning the heat transfer to the substrate due to the small gap between the hot membrane and the substrate will be studied in section 3.4. The heated membrane can also be used for gap detection by monitoring the temperature of the membrane. Details will be presented in section 3.5. Conclusion will be made in section 3.6.

3.2 Thermal Induced Deformation

Basic principle

The deformation of the conventional thermal actuator is due to the bending moment generated by the stresses induced from the interface of two components of a composite with different thermal expansion coefficients when temperature changes, known as bimorph effect. The theoretical investigation of a bimorph strip under uniform heating and the consideration in calculating the behavior of bimorph plates were first discussed by Timoshenko [83]. The results obtained by this theory are useful in choosing the material combination and deciding on the layer thickness to maximize the bimorph effect. Theoretical expressions described the behavior of the bimorph membrane subjected to a uniform temperature increase on the annular region under different boundary conditions [84]. This theoretical model is based on a composite membrane with only the annular region being heated, hence it is impractical in actual actuator design. However, it gives comprehensive consideration to the parameters that could affect the bending direction, which provides a guidance to estimate the orientation of the membrane deformation in the case of heated stencil. For example, a simply supported circular bimorph membrane with a material A of a larger thermal expansion coefficient in the center region on top of material B, the deflection is upward, as shown in *Figure* 3.2a. As the thermal expansion coefficient of material A is larger than which of material B, the thermal induced stress $\sigma_{A\triangle T}$ is larger than $\sigma_{B\triangle T}$. The membrane would deflect upwards due to the stress difference generated on the interface between two materials. We consider the behavior of circular bimorph membranes is similar to the square bimorph membranes. Hence, for the heated stencil, we would expect the same bending behavior with similar geometry consideration. The thermal expansion coefficient of Pt is 8.8×10^{-6}/°C, as comparison, it is

2.3×10^{-6}/°C for SiN. Therefore, the upper Pt layer would create more thermal expansion that will deform the membrane upwards. There is a second situation in our experiment that the metal is embedded in two layers of SiN, where the top layer of SiN acts as a passivation layer to protect the metal at high temperature. This situation is schematically described as the model shown in *Figure* 3.2b. In this case, material A of a larger thermal expansion coefficient in the center region is embedded in material B. Both upward and downward deflection are possible, depending on the relative stress induced on both interface between material A and material B. When $\sigma'_{B\triangle T} > \sigma_{A\triangle T} - \sigma_{B\triangle T}$, the membrane would bend upwards. When $\sigma_{B\triangle T} > \sigma_{A\triangle T} - \sigma'_{B\triangle T}$, the membrane would bend downwards. As the relative stress also depends on the thickness of material, the control of bending direction would rely on the thickness ratio between the upper and bottom layer of material B. Detailed experiments will be shown in section 3.3.

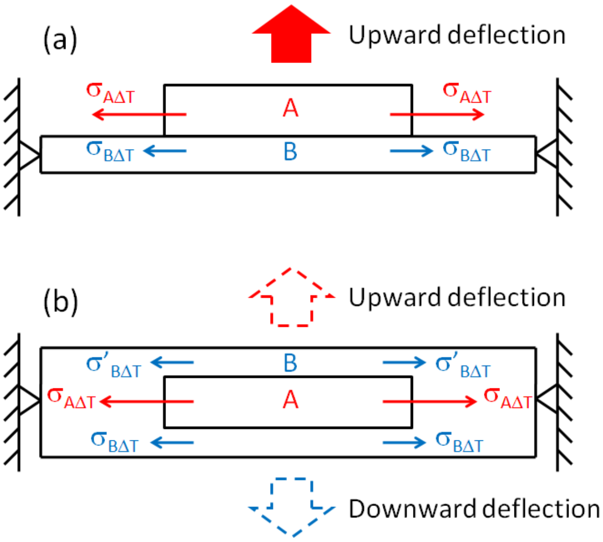


Figure 3.2: Schematics of deflection of clamped circular bimorph membranes. (a) Material A of a larger thermal expansion coefficient in the center region on top of material B. Upward deflection is expected due to that the thermal induced stress $\sigma_{A\triangle T}$ is larger than $\sigma_{B\triangle T}$. (b) Material A of a larger thermal expansion coefficient in the center region embedded in material B. Both upward and downward deflection are possible, depending on the relative stress induced on both interface between material A and material B. When $\sigma'_{B\triangle T} > \sigma_{A\triangle T} - \sigma_{B\triangle T}$, the membrane would bend upwards. When $\sigma_{B\triangle T} > \sigma_{A\triangle T} - \sigma'_{B\triangle T}$, the membrane would bend downwards. As the relative stress also depends on the thickness of material, the control of bending direction would rely on the thickness ratio between the upper and bottom layer of material B.

Inspection tool

To measure the membrane deformation of the heated stencil, a nondestructive method is needed. It is shown that digital holographic microscopy (DMH) can be used to characterize the heated membrane, but the image quality is relatively low [85]. We use an optical profiler system, Veeco Wyko NT1100, which provides three-dimensional surface profile without contact. The vertical shift interference (VSI) mode, based on white light vertical scanning interferometry, was used for heated stencil measurement. With vertical resolution of 3 nm and maximum range of 1 mm of the VSI mode, the bending of the membrane can be visualized and the profile can be precisely plotted.

3.3 Tailored Geometry of Membrane for Upwards Bending

In this section, we will introduce both FEM simulation and the experimental investigation of the proper geometry of the heated stencil to achieve upwards bending. The main variables are the thicknesses of the SiN layer on the top and bottom of the metal layer. The experimental results are compared with simulation results. The bending behaviors of heated stencils made of different heating materials (Pt, W and Nicrhome) are also compared.

3.3.1 FEM Simulation

In order to understand the bending behavior of the heated stencil, Comsol 3.5a is used as the platform for FEM simulation. The heated stencil comprises a 1 mm × 1 mm SiN membrane with 500 nm in thickness. The Pt resistive heater is 200 nm thick and is placed either on top of or embedded in the SiN layer. In the case of embedded electrode, the upper layer of SiN is 200 nm thick and bottom layer is 100 nm. Boundary conditions are applied to the four edges of the membrane, which are mechanically fixed and are given constant room temperature. Electrical bias was applied on the cross section of the two big triangle electrode on the edge of the membrane. *Figure* 3.3 illustrates the simulation results. 5 V bias was applied to the heated stencil in both cases. The maximum temperature in the center of the membrane is ~600 °C. When Pt electrode is placed on the top of the SiN layer, the membrane would bend upwards due to the larger thermal expansion of Pt and the simply-supported boundary condition [84].

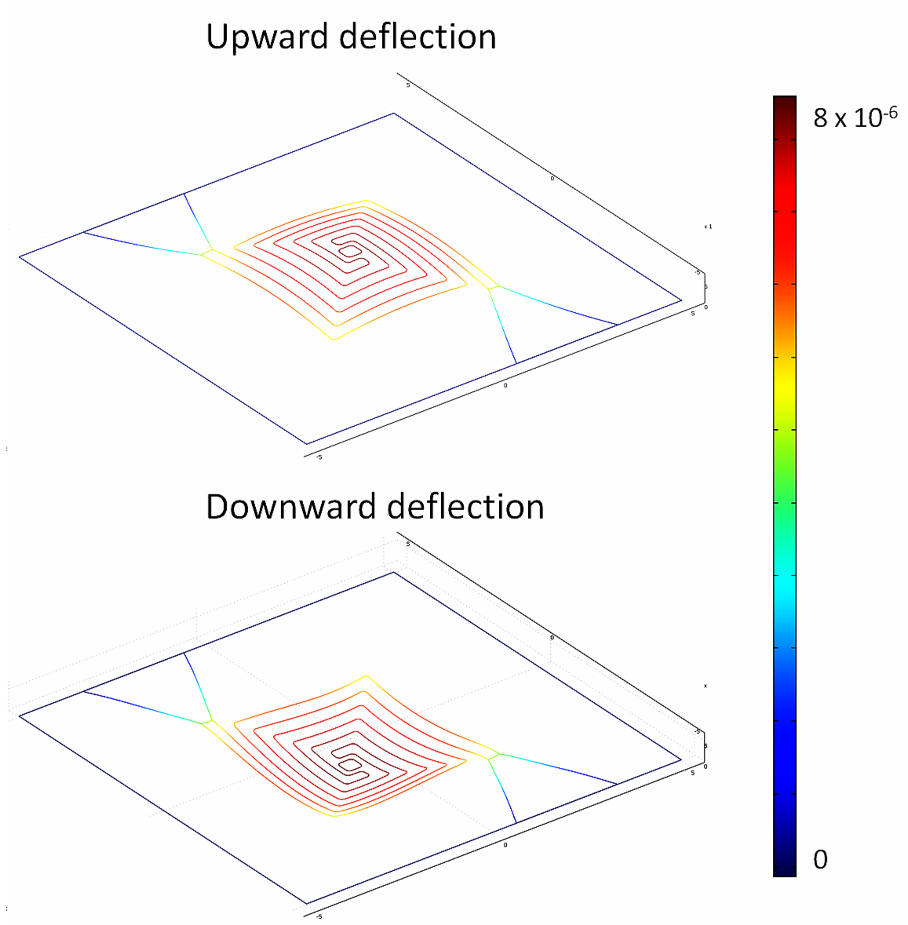


Figure 3.3: FEM simulation of upward and downward deflection of the heated stencil due to different geometry configuration. Upward bending is achieved by placing 200 nm Pt electrode on top of 500 nm SiN. Downward bending is achieved by placing 200 nm Pt electrode embedded in 500 nm SiN. The upper layer of SiN is 200 nm thick and bottom layer is 100 nm thick.

As comparison, when Pt is embedded in the SiN layer, the thermal stress created on both interfaces between Pt and SiN would compete with each other. Because of the thicker SiN of the upper layer, the membrane deflects downwards. The simulation results can help us predict the bending behavior of the heated stencil with different geometry consideration. However, It is a bit more complicated in real case, as Ta is deposited on the bottom as adhesion layer for Pt and the second layer of SiN has topography from the Pt heater. Therefore, different thickness ratio of the SiN film was experimentally attempted to achieve upwards bending, which will be shown in next section.

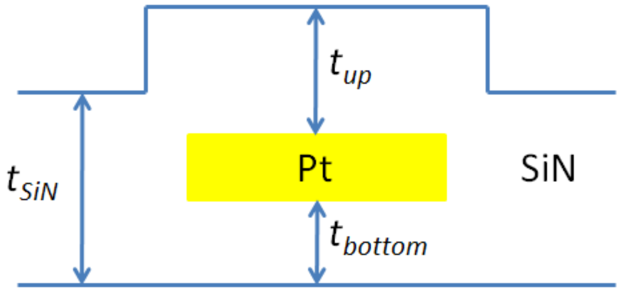


Figure 3.4: Schematics of the cross section of the membrane composition. t_{up} is the thickness of the upper layer SiN. t_{bottom} is the thickness of the bottom layer SiN. t_{SiN} is the total thickness of SiN, which is equal to $t_{up} + t_{bottom}$.

3.3.2 Geometry Study of the Membrane for Upwards Bending

In order to find the optimal geometry to achieve upwards bending, heated stencils with different thicknesses of the top and bottom SiN layer were fabricated. Identical heater design was kept in all cases. *Figure* 3.4 schematically shows the cross section of the membrane composition. t_{up} is the thickness of the upper layer SiN. t_{bottom} is the thickness of the bottom layer SiN. t_{SiN} is the total thickness of SiN, which is equal to $t_{up} + t_{bottom}$. By varying the ratio between t_{up} and t_{bottom}, we attempt to create upwards bending for gap reduction.

t_{up}= 300 nm, t_{bottom} varies

We first keep t_{up}= 300 nm and vary t_{bottom}. *Figure* 3.5 shows the optical images of four heated stencils with t_{up}= 300 nm and different t_{bottom} (90 nm, 140 nm, 200 nm and 500 nm), and corresponding optical profiler images with 5.0 V applied voltage. All the membranes bend downwards at given power. When $t_{bottom} < t_{up}$, which is the case in *Figure* 3.5a, b and c, the membrane bends downwards because of the thermal induced stress on the interface between Ta/Pt and bottom layer SiN is larger than which of on the interface between Pt and top layer SiN, as we discussed in section 3.2. The unique case is shown in *Figure* 3.5d, when $t_{bottom} > t_{up}$, the membrane still bends down. This may be explained by the topography of the upper layer SiN transformed from the Pt heater during the conformal LPCVD process, as the schematic cross section shown in *Figure* 3.5. This topography provides reinforcement that makes the membrane more rigid, which equivalently increases the Young's modulus or increases the thickness of the upper layer SiN, leading to the downward bending. Similar structures have been applied to conventional stencils for improving the stability of the membrane [86, 87].

Figure 3.6 plots the displacement profile of the four heated stencils under 5.0 V applied voltage in ambient conditions. It clearly shows that thinner the bottom layer SiN is, more bending the membrane will have. The power applied to the heated stencil is 100 mW and the corresponding temperature is ~ 620 °C. Maximum downward deformations are 18.3 μm, 18.0 μm, 14.6 μm and 11.5 μm, respectively for the membrane with 390 nm, 440 nm, 500 nm and 800 nm in thickness.

t_{up} *varies,* t_{bottom} *= 200 nm*

It is discovered that the membrane always bends down by fixing t_{up}= 300 nm. Therefore, in this set of experiments, t_{bottom} is fixed to 200 nm and t_{up} varies. *Figure* 3.7 shows the optical images of three heated stencils with t_{bottom}= 200 nm and different t_{up} (100 nm, 300 nm and 300 nm + 25 nm Cr), and corresponding optical profiler images with 5.0 V applied voltage. When t_{up}= 100 nm, as shown in *Figure* 3.7a, the membrane bends upwards. This verifies the theoretical model that when $t_{bottom} > t_{up}$, the deflection is upward. In this case, the reinforcement brought from the topography on the upper SiN layer should be weaker than the case shown in *Figure* 3.5d, as t_{up} is much thinner. Thus the membrane bends up in accordance with the theory. However, wrinkle like topography was observed on the membrane. It should be due to the total thickness (t_{SiN} = 300 nm) that is too thin to support the membrane for achieving smooth deformation. Therefore, thicker SiN layer was used as shown in *Figure* 3.5b, which has been proved in previous experiment that the membrane bends down. In order to understand the bending behavior of thicker SiN membrane, 25 nm Cr was deposited through a paper shadow mask only on the center of the membrane, as shown in *Figure* 3.7c. This simple experiment equivalently increases the thickness of Pt heater or decreases the thickness of upper layer SiN, which should provide larger thermal induced stress and initial strain (Cr has tensile stress) to help the membrane bend upwards. Optical profiler image showing a smooth upwards deformation validates the hypothesize. A brief conclusion can be made that in order to achieve smooth upwards bending, t_{SiN} should be thick enough (≥ 400 nm) and t_{up} should be as thin as possible.

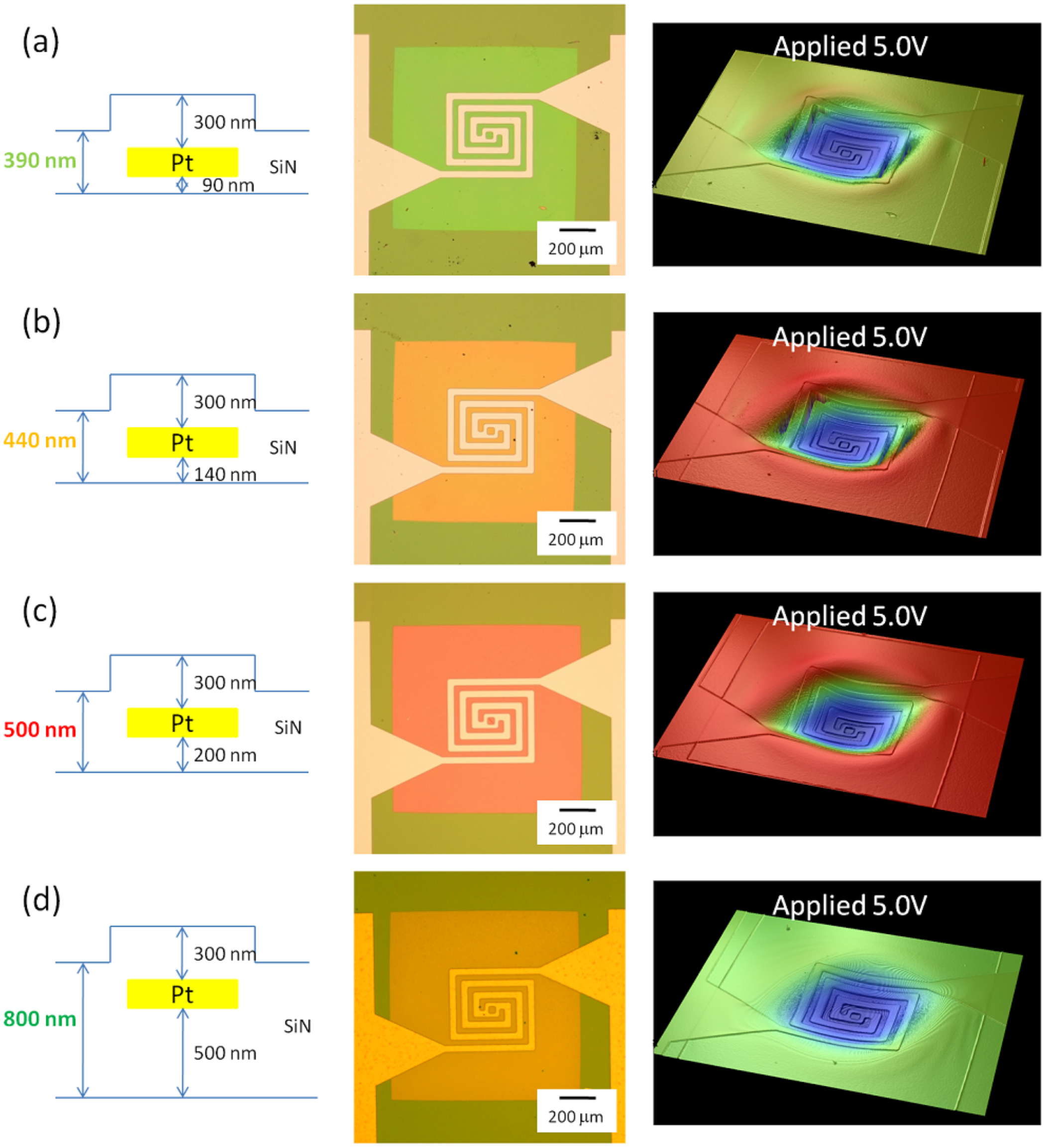


Figure 3.5: Micrograph of heated stencils with fixed thickness (t_{up}= 300 nm) of top SiN layer and different thicknesses of bottom SiN layer, and corresponding optical profiler images with 5.0 V applied voltage. All the membrane bends downwards at given power. (a) t_{bottom}= 90 nm. (b) t_{bottom}= 140 nm. (c) t_{bottom}= 200 nm. (d) t_{bottom}= 500 nm.

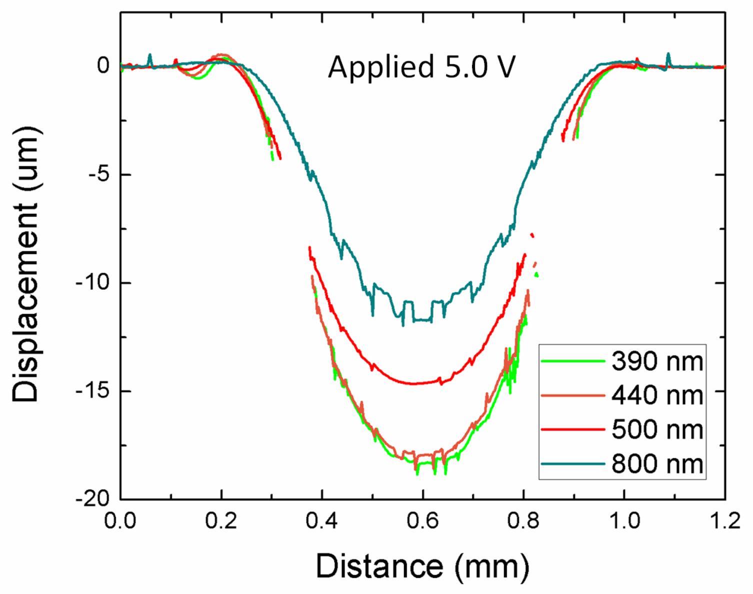


Figure 3.6: Displacement profiles of four heated stencils with with fixed t_{up}= 300 nm and different t_{bottom}(90 nm, 140 nm, 200 nm and 500 nm). Therefore, t_{SiN} is equal to 390 nm, 440 nm, 500 nm and 800 nm, respectively. The power applied to the heated stencil 100 mW and the corresponding temperature is ~ 620 °C.

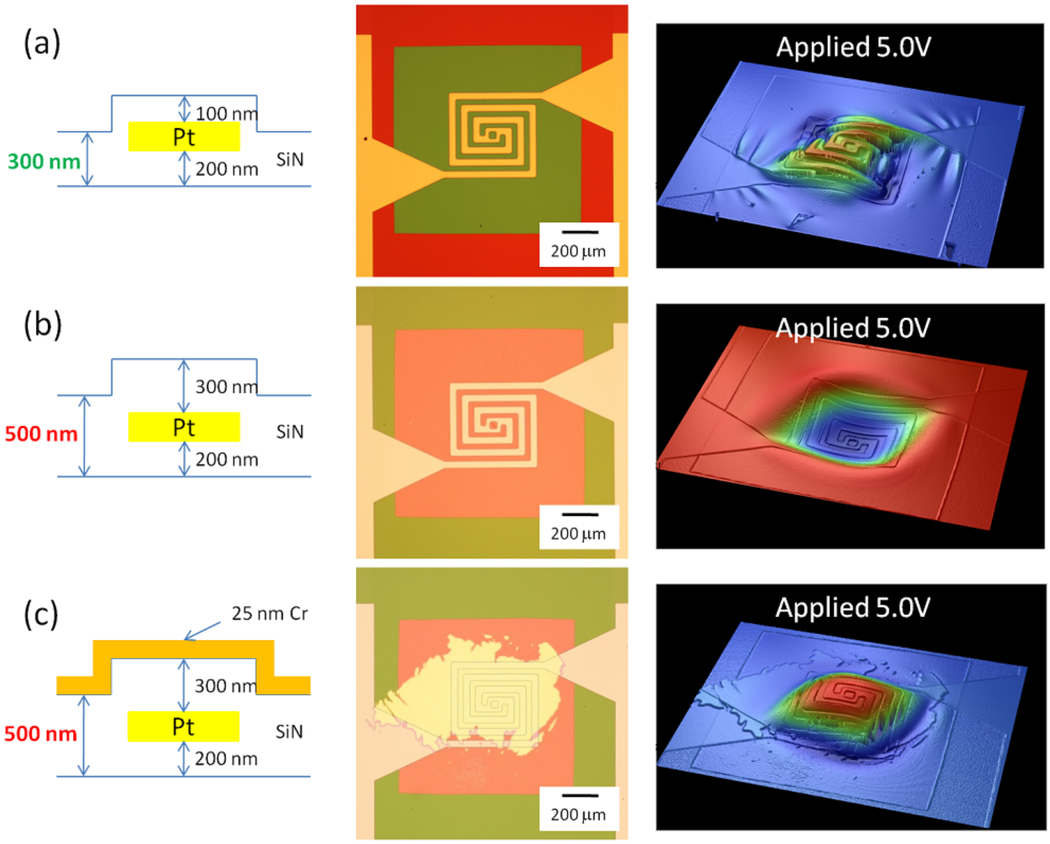


Figure 3.7: Micrograph of heated stencils with fixed thickness (t_{bottom}= 200 nm) of bottom SiN layer and different thicknesses of upper SiN layer, and corresponding optical profiler images with 5.0 V applied voltage. Membrane bends downwards with (a) t_{up}= 100 nm and (c) t_{up}= 300 nm + 25 nm Cr. Membrane bends downwards with (b) t_{up}= 300 nm.

Figure 3.8 shows the displacement profiles of three heated stencils under 5.0 V applied voltage in ambient conditions. The power applied to the heated stencil is 100 mW and the corresponding temperature is ~ 620 °C. Maximum upwards deformations are 11.5 μm for t_{up}= 100 nm and 16.7 μm for t_{up}= 300 nm + 25 nm Cr. Maximum downwards deformation is 14.6 μm for t_{up}= 300 nm. The presence of 25 nm Cr on top of 500 nm SiN completely changes the bending direction. The wrinkle like profile in the case of t_{up} = 100 nm is due to the total thickness t_{SiN} = 300 nm, which is too thin to obtain smooth deformation.

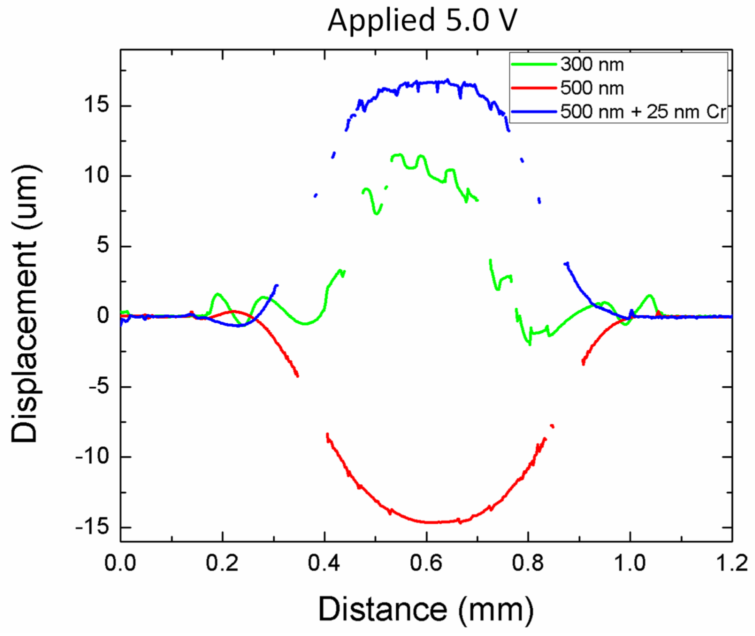


Figure 3.8: Displacement profiles of four heated stencils with with fixed t_{bottom}= 200 nm and different t_{up}(100 nm, 300 nm and 300 nm + 25 nm Cr). Therefore, t_{SiN} is equal to 300 nm, 500 nm and 500 nm + 25 nm Cr, respectively.

t_{up} = 0, t_{bottom} *varies*

In this set of experiments, there is no second layer of SiN covering the Pt electrode. Thus the deflection of membrane is expected to be upward according to the theoretical model. *Figure* 3.9 shows the two heated stencils without the upper layer SiN (t_{up}= 0) and with bottom SiN layer of 200 nm and 500 nm. Both membranes bend up in accordance with theory. As the 200 nm thick SiN membrane is too thin, the bending is not smooth. 500 nm thick SiN shows smooth upwards bending, indicating that it is a good candidate geometry for actuating gap reduction.

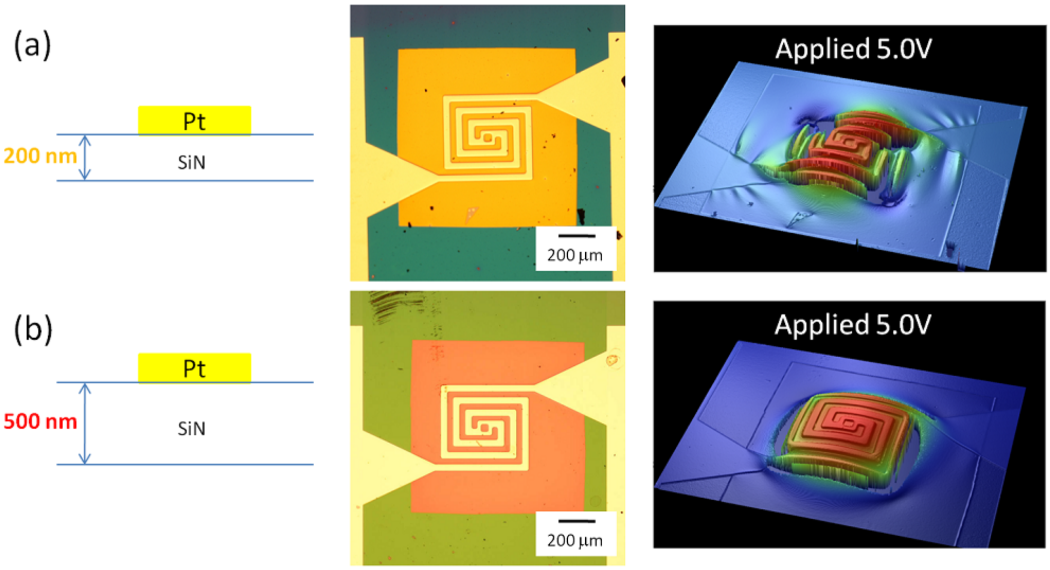


Figure 3.9: Micrograph of heated stencils without upper SiN layer (t_{up}= 0) and different thickness of bottom SiN layer, and corresponding optical profiler images with 5.0 V applied voltage. Both the membrane bends upwards at given power. (a) t_{bottom}= 200 nm. (b) t_{bottom}= 500 nm.

Figure 3.10 plots the displacement profiles of two heated stencils without upper SiN layer (t_{up}= 0) and different thickness of bottom SiN layer (200 nm and 500 nm). The maximum upward deformation is 14.8 μm for t_{bottom}= 200 nm and 20.2 μm for t_{bottom}= 500 nm. Comparing to the profile with $t_{up} \neq 0$, it is noticed that the profile with t_{up}= 0 shows a rougher displacement on top of the heater region. This is due to the different reflectivity between Pt and SiN, which gives the error. As the thickness of Pt is 200 nm, the profile roughness on top of the heater region does not reflect the reality.

We can conclude the geometry study for obtaining upwards deformation as following:

- It is necessary that t_{bottom} is larger than t_{up}. However, due to the topography on upper SiN layer, sometimes even when $t_{bottom} > t_{up}$, membrane still bends down. More investigation would be needed to find the ratio limit.
- When t_{up}= 0, membrane always bends up in accordance with the theory.
- When the total thickness of SiN $t_{SiN} \leq 300$ nm, wrinkle like bending topography was observed. That means the membrane is too thin to obtain smooth deformation.

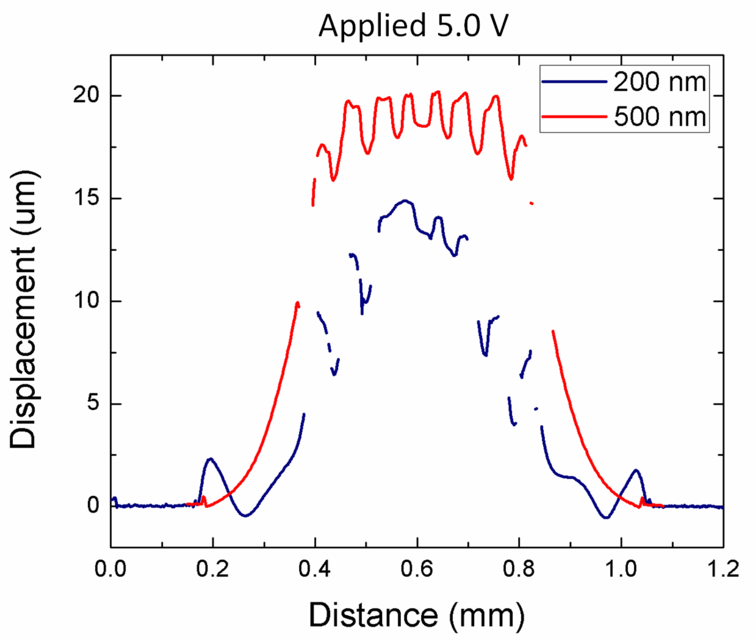


Figure 3.10: Displacement profiles of two heated stencils without upper SiN layer t_{up}= 0 and different t_{bottom} (200 nm and 500 nm).

3.3.3 Deformation vs. Power

The membrane bends more when the applied power increases. *Figure* 3.11a shows the deformation profile at different applied voltage and *Figure* 3.11b shows the maximum Z displacement as function of the power. The sample tested in this experiment has 500 nm SiN on the bottom and no upper layer SiN, thus upward bending is expected. By knowing the deformation at different voltage, controllable membrane actuating can be achieved in order to the control the gap. Another advantage is that, as the stencil window areas are placed on different region across the heater, the deformation profile provides different gaps for study. *Figure* 3.11b plots the relation between maximum Z displacement and the applied power, from which we can see the membrane starts bending only at given power (25 mW for this sample). And then the Z displacement is linear to the applied power. It is practical for our application as we can easily correlate the deformation with temperature, which makes heated stencil controllable in both functions: clogging free aperture and actuating gap reduction. For instance, certain temperature for unclogging is obtained by applying certain power, which can be translated to the Z displacement. Then, initial gap control can be arranged so that this gap can be minimized by actuated membrane.

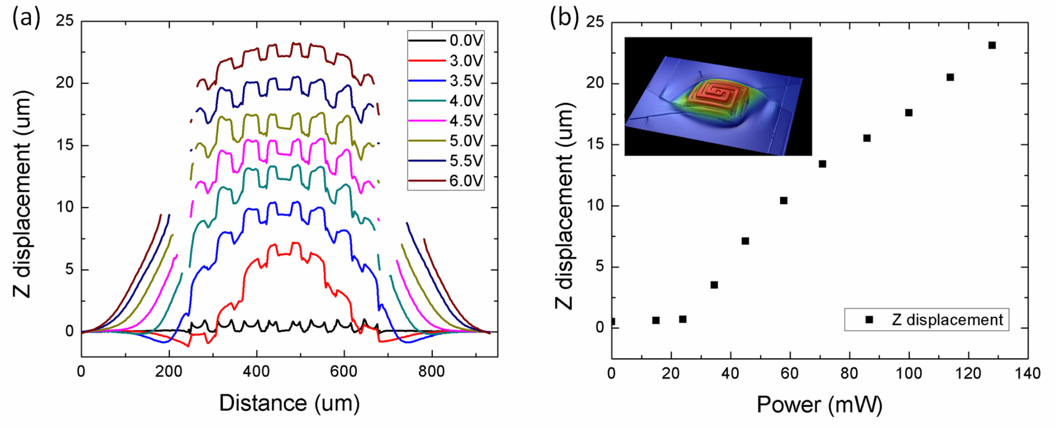


Figure 3.11: (a) Deformation profile of the heated stencil at different applied voltage. (b) Z displacement as function of applied power, indicating that obvious bending of the membrane starts from ~25 mW applied power.

3.3.4 Different Heating Elements

We have introduced in Chapter 2 that heated stencils with different heating elements (Tungsten, Platinum and Nichrome) were made to find the optimal material. Besides the reason for achieving higher temperature, another important factor is to achieve higher Z displacement in order to minimize bigger gap, for example, on a substrate with high topography. Thus, comparison has also been made to see which material gives higher deformation. *Figure* 3.12 illustrates the displacement profile of heated stencil made from three different heating materials, Tungsten, Platinum and Nichrome. All the devices were actuated with maximum power (204 mW for Tungsten, 240 mW for Platinum and 208 mW for Nichrome). Clearly, Nichrome has the highest thermal expansion coefficient (14×10^{-6}/°C) among these three materials, which gives it the largest deformation. Tungsten has the lowest maximum Z displacement due to its low thermal expansion coefficient (4.5×10^{-6}/°C). The deformation with Platinum is in the middle with the thermal expansion coefficient of 8.8×10^{-6}/°C. As usually the gap between a chip stencil and the substrate is within few microns, the displacement provided from all devices should be enough for eliminating the gap. In the full wafer stencil, the gap is usually bigger, in the range of tens of microns. Platinum and Nichrome would provide the possibility to eliminate the gap. Considering Pt has more stable performance at high temperature, this is again the optimal material among these three elements for providing both functions.

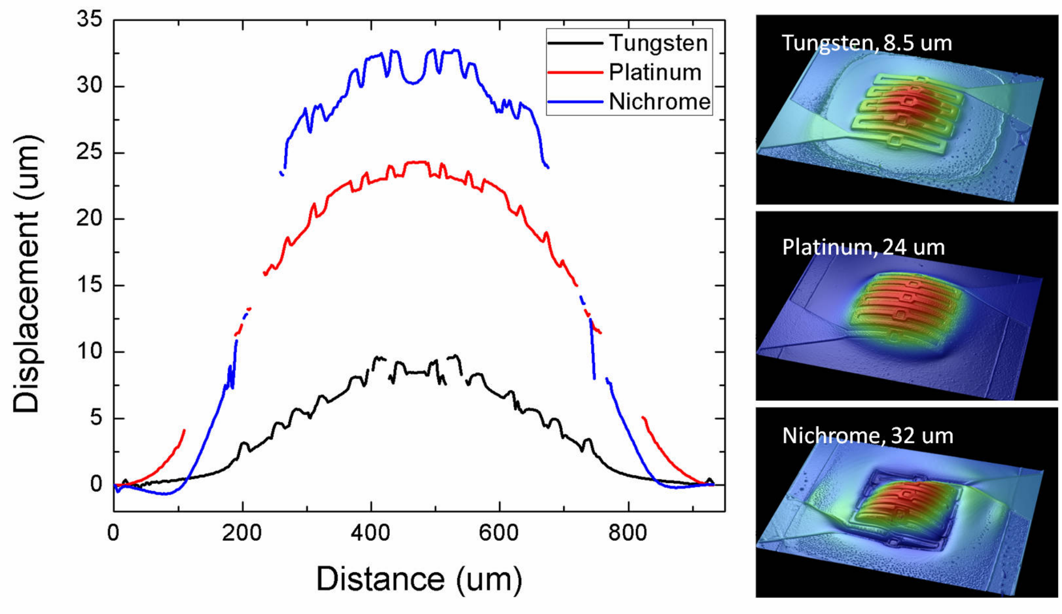


Figure 3.12: Deformation profiles of heated stencil made from different heating elements. The maximum achievable deformation are 8.5 μm, 24 μm and 32 μm for heated stencil made from Tungsten, Platinum and Nichrome, respectively.

3.4 Heat Transfer to the Substrate

The temperature of the substrate is a very important parameter that may cause concern for the actuated gap reduction as well as for the surface diffusion of the deposited materials. As we have discussed, the basic principle for keeping the aperture unclogged is to minimize the condensation of material on the stencil membrane, which would require a high temperature generated by the resistive heater. However, we certainly would like to keep the temperature on the substrate as low as possible to allow material condensing. The gap reduced by the deformation of the membrane would cause a concern of the heat transferred through the narrow gap to the substrate, which could eventually heat up the substrate. In this section, theoretical model was first descrided and then FEM simulation was used to study the heat transferred to the substrate through this narrow gap. Three major factors were considered for the heat transfer in vacuum, the radiation, the convection and the conduction through contact. In all simulations, substrate is Si and the membrane is SiN. The membrane deformation was not taken into account as it complicates the model.

When a hot surface is placed above a substrate with a small gap, the heat flow between these two parallel plates can be described as [88]:

$$Q_{th} = \triangle T \frac{\kappa_{th} A}{d} \tag{3.1}$$

where $\triangle T$ is the temperature difference on the surface of the substrate, κ_{th} is the thermal conductivity of the media in between two plates, A is the area of the hot surface and d is the distance between two plates. κ_{th} should be corrected when the distance d is smaller than the molecular mean free path $\bar{\lambda}$. In our case, the media between two plates is air or vacuum, thus κ_{th} should be modified correspondingly to the air pressure. This equation describes the air in the small gap as an effective heat conduction path between two plates. Besides this effect, radiation is also contributing to the heat transfer between two surfaces, which will is discussed below.

Radiation

In vacuum, radiation seems to be the major source for thermal loss. We first conduct the simulation with a fixed gap of 100 μm between the hot stencil membrane the substrate. Only radiation was considered in the simulation to see the heat transfer from the hot membrane to the substrate. The temperature of the membrane was first set to 825 °C and the simulation result shows that the temperature on the substrate increases 0.26 °C through the 100 μm gap. And the temperature increase is 1.8 °C when the membrane is at 1500 °C. Apparently, this increment is neglectfully small. Simulations were also performed with different gaps. As long as the substrate doesn't touch the substrate, the change of temperature on the substrate is at the neglectable range. Theoretically, it can be explained by the Stefan-Boltzmann law which defines the energy emitted from a perfect object that radiates all the energy from the absorption, know as black body. The energy radiated of a black body per unit time is given by:

$$q = \sigma T^4 A \tag{3.2}$$

where σ is the Stefan-Boltzmann constant, which can be derived from other known constant of nature. T is the black body's temperature and A is the considered surface area.

We could consider the hot membrane as a black body, though in reality the emissivity of the materiel has to be taken into account. However, it only changes the total amount of the energy that radiates from the surface. From this law, we can see that the radiation from the hot membrane at certain temperature is fixed, independently from the gap between itself and a substrate. As the area of the hot membrane is 1 mm^2, comparing to the gap between the hot membrane and the substrate which is smaller than 100 μm, we can assume that the energy absorbed by the substrate is independent from gap between itself and the hot membrane. This could explain the small increment of the temperature we observe on the substrate independently from the gap. The simulation of radiation indicates that it is not a major factor which will increase the temperature on the membrane with a gap of 100 μm. However, it is reported that when the gap is smaller than 1 μm, the radiative heat transfer will be predominant at a pressure lower than the amient one [89]. As we consider that the smallest gap is 10 μm in this simulation study, the contribution of heat transfer from radiation is neglected.

Convection

In ambient conditions, convection is usually the major source for thermal loss. But in vacuum, the convection is often very low due to the thin air. However, in the gap range of sub 100 μm, the convection through the thin air has to be taken into account. Simulation was performed at the vacuum level of 10^{-6} mbar, which is close to the real vacuum when we conduct the evaporation. The membrane-substrate gap is fixed first to 100 μm and the highest temperature in the center of the membrane is 1020 °C. *Figure* 3.13 shows the temperature profile from the simulation results. The highest temperature in the center of the membrane is 1020 °C and the corresponding temperature on the substrate is 32.6 °C. It is also noticed that the temperature drops dramatically along the direction from the membrane to the substrate. Thus the study of varying the gap to see the temperature change on the substrate was conducted.

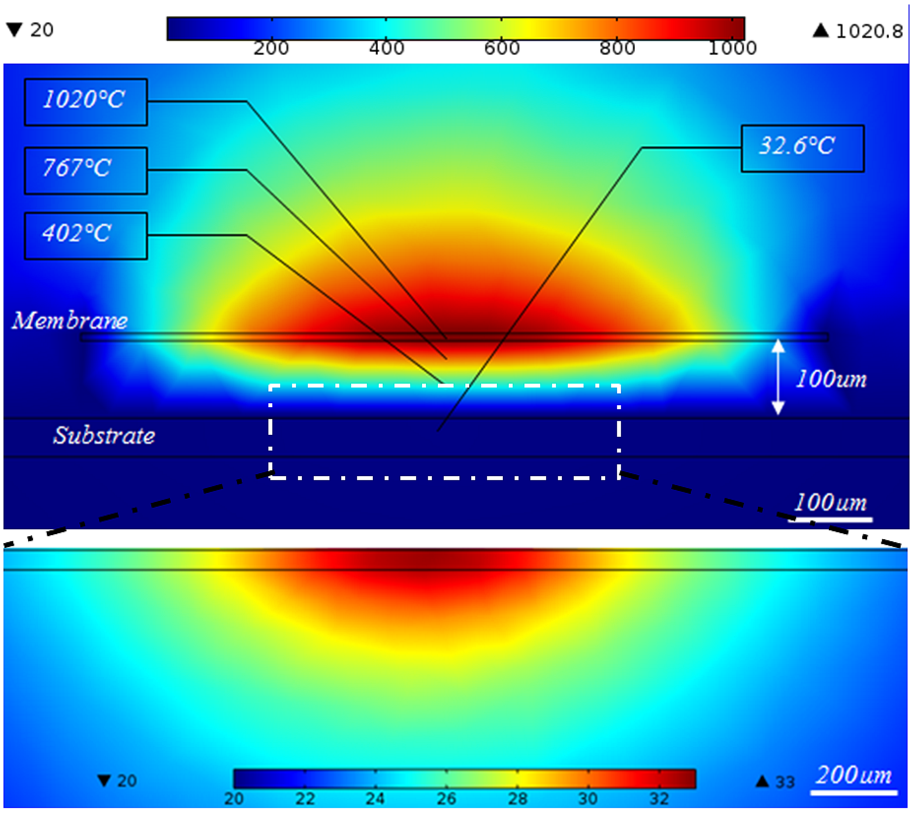


Figure 3.13: FEM simulation result of the temperature profile of a hot membrane on top of a substrate with 100 μm. Only convection through 10^{-6} mbar vacuum was considered. The highest temperature in the center of the membrane is 1020 °C and the corresponding temperature on the substrate is 32.6 °C.

Figure 3.14 plots the temperature profile of the substrate with different gaps between the membrane and the substrate. The temperature in the center of the membrane is fixed to 1000 °C. The temperature on the substrate increases when the gap decreases, which means the smaller air gap provides a stronger convection that transfers the heat to the substrate. When the gap is 10 μm, the corresponding temperature on the substrate is ~ 150 °C. This temperature should not affect the condensation of material as it is still much lower than the necessary temperature for creating a considerable reevaporation flux, as we discussed in Chapter 2. We can expect the temperature increase more when the gap is smaller than 10 μm. However, as long as the membrane does not touch the substrate, the temperature on the substrate stays in the condensible region for the material.

The substrate temperature as function of the membrane temperature with different gaps

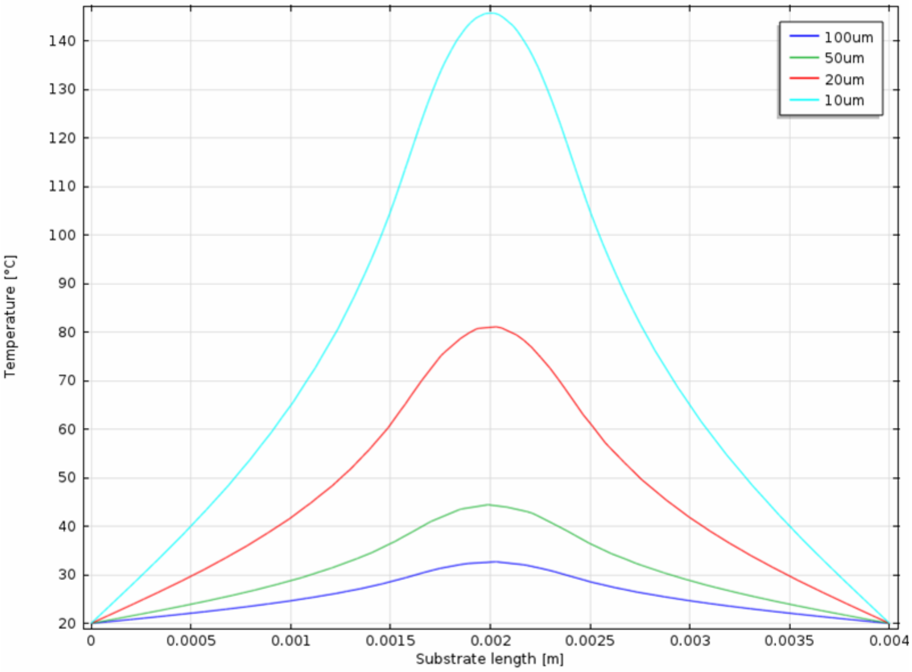


Figure 3.14: Temperature profile on the substrate with different gaps between the membrane and the substrate. The temperature in the center of the membrane is fixed to 1000 °C.

were also simulated, as shown in *Figure* 3.15. It is clearly that the temperature on the substrate increases with smaller gap and higher membrane temperature. The highest temperature given from 10 μm with a membrane temperature of 1500 °C is ~ 250 °C, which is still considered relatively low for preventing the condensation on the substrate.

Conduction through contact

The ultimate situation we should consider is when the membrane touches the substrate. In this case, the heat conduction through the touch point will be major factor that heat transfers from the membrane to the substrate. The temperature of the substrate at the contact point was assumed to be the same as the membrane temperature and the cooling along the substrate will depend on the boundary conditions of the substrate. The temperature remains relatively high in the center region as shown in *Figure* 3.16a. The temperature is over 650 °C at the place 200 μm away from the contact point. This temperature does not ensure reliable condensation of the deposited vapor. Therefore, contact between the substrate and the membrane should be avoided. *Figure* 3.16b compares the temperature profile of the contact situation with which of the non-contact one. When a gap is remained, the temperature is much lower.

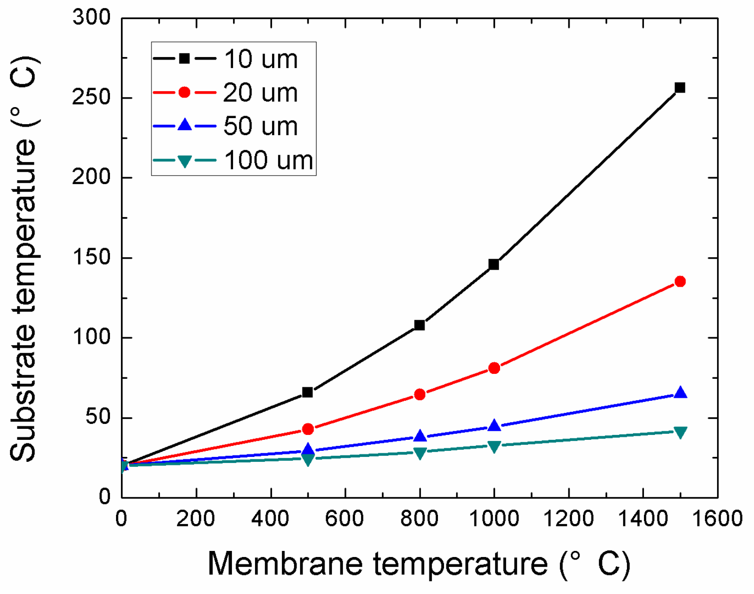


Figure 3.15: The substrate temperature as function of the membrane temperature with different gaps (10 μm, 20 μm, 50 μm and 100 μm).

Conclusions of the FEM simulation study of the heat transferring to the substrate can be made as following:

- Radiation from the hot membrane to the substrate is neglectable for temperature increase on the substrate, which is also independent from the gap.

- Convection through the thin air in vacuum significantly contributes to the temperature increase on the substrate, when a gap is remained. However, the increased temperature is considered relatively low for affecting the condensation on the substrate. Thus it is acceptable. The mean free path of the atoms under this vacuum is not considered for simplifying the simulation process, thus the simulation result cannot represent the real temperature, which could be even lower.

- The conduction happens when the membrane touches the substrate. It heats up the substrate to the temperature which does not ensure a reliable condensation of the deposited vapor. Thus it should be avoided during the evaporation. Gap control will be needed to prevent the contact from the actuated membrane.

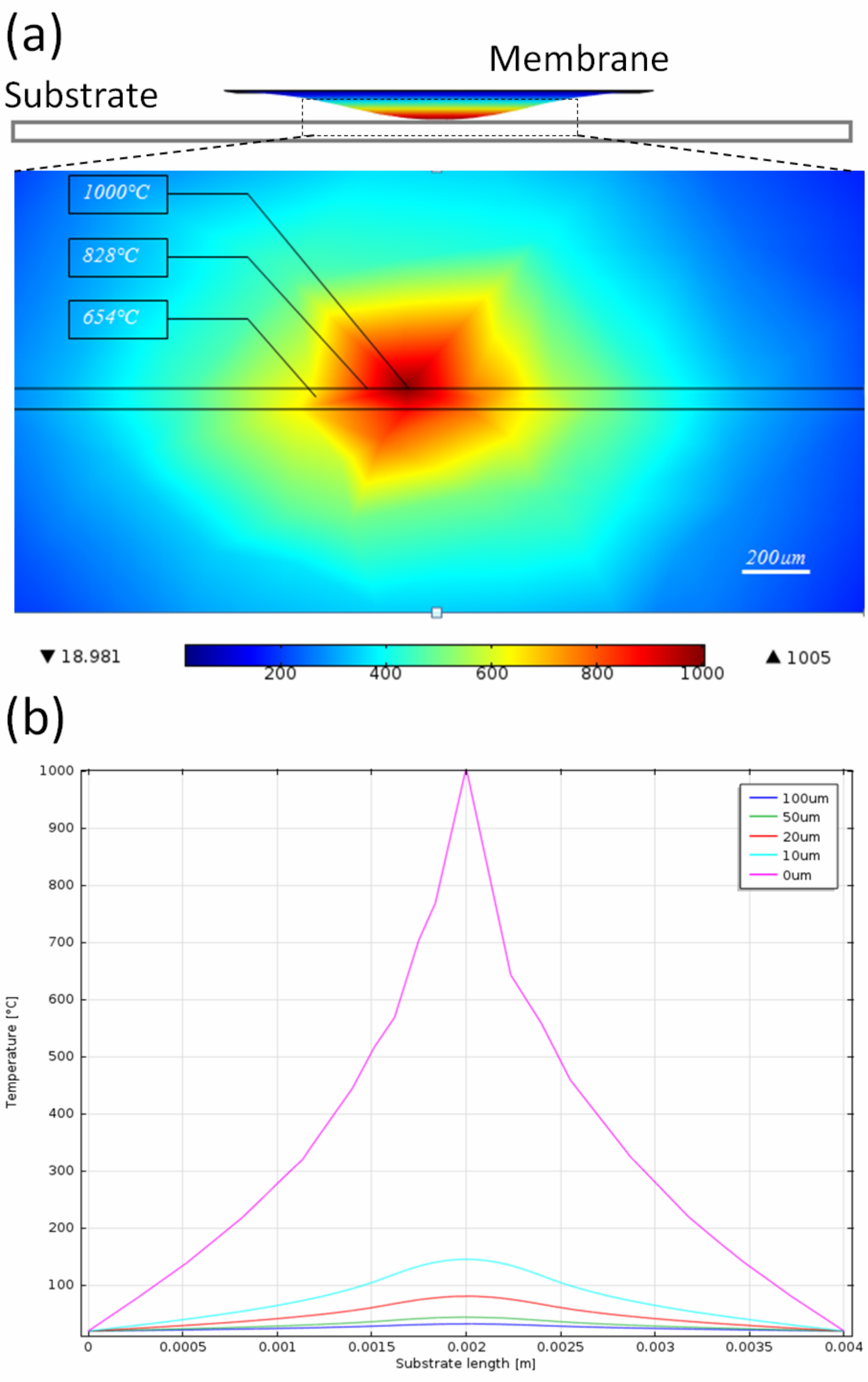


Figure 3.16: Simulation of temperature profile on the substrate when the hot membrane touches the substrate.

3.5 Gap Control

In this section, we show the preliminary results of the in-situ gap control by monitoring the current applied to the heated stencil. We have concluded that the contact between the hot membrane and the substrate should be avoided, thus an intial gap control would be needed when the intrinsic gap is not large enough to compensate the deformation of the membrane. This could be done by monitoring the temperature of the heated membrane when the gap varies. As it is shown that when the gap is below 1 mm, the convection loss through the air would become an equivalent gap to conduct the heat from the hot membrane to the substrate [88]. Therefore, by monitoring the temperature of the membrane which is translated from the applied current, it is feasible to correlate with the gap. On the other hand, when the membrane is in contact with the substrate, the membrane is cooled down by direct conduction from the membrane to the substrate. Therefore, if we lift up a hot membrane from the in contact mode with the substrate, there is a certain point when the direct conduction mode changes to the gap conductin mode, which reflects as an inflection point of the current as the cooling effect of the gap conduction mode is lower.

The experiment was conducted in our dynamic stencil system with a piezo stage to control the Z movement. A full wafer heated stencil was placed on a holder which sits on the piezo stage. Five heated membranes located across the wafer were parallelly connected. A constant voltage with 5.5 V was applied to the heated stencil. There is another fixed holder on which places a Si substrate. The heated stencil was first in close contact with the substrate by moving the piezo stage. Then the piezo stage contracted from the contact position (gap = 0) with a speed of 1 μm/s. Current was monitored during the whole process. *Figure* 3.17 shows the recorded current when the gap increases from 0 to about 150 μm. We can observe that the current does not change at the beginning when the gap increases, which means the membrane was still in contact with the substrate. The inflection point of current indicates the change from the direct conduction mode to the gap conduction mode, which means the deformed membrane was separated from the substrate. Thus the inflection point indicates a gap of 50 μm which should be the non-contacting point at the given power.

By using this method, we can first measure the non-contacting point. Then a corresponding gap is left for preventing the contact by the deformed membrane. It is noticed that 50 μm is larger than the maximum deformation of the Pt heater. It could be caused by the gap nonuniformity across the wafer, which means not every membrane separated from the substrate at the same time.

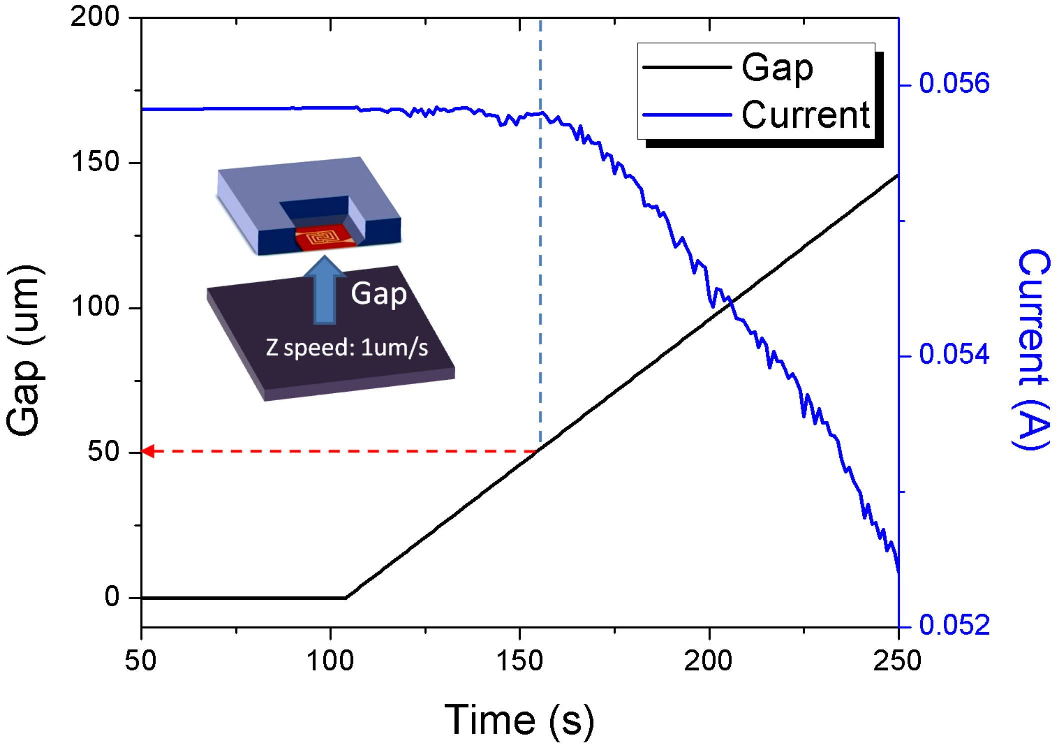


Figure 3.17: Contact detection by monitoring the applied current to the heated stencil. The inflection point of the current indicates a gap of 50 μm which should be the non-contacting point.

3.6 Conclusions

In this chapter, we have presented the reduction of the gap by thermal actuation of the membrane. Geometry study of the membrane was conducted in order to find the optimal design for achieving upwards bending. Particularly, different thicknesses combination of the upper SiN $t_{up}$and the bottom SiN t_{bottom} was tested and the deformation profile of the membrane was measured and compared. It is necessary that t_{bottom} is larger than t_{up}. However, due to the topography on upper SiN layer, sometimes even when $t_{bottom} > t_{up}$, membrane still bends down. More investigation would be needed to find the ratio limit.

When t_{up}= 0, membrane always bends up in accordance with the theory.When the total thickness of SiN $t_{SiN} \leq 300$ nm, wrinkle like bending topography was observed, which means the membrane is too thin to obtain smooth deformation. The Z displacement of the deformed membrane shows a linear relationship with the applied power. Different heating elements were also compared. Tungsten heater exhibits lowest deformation while Nichrome shows the highest. Platinum is in the middle thus is still the optimal heating material by comprehensive consideration. Different heat transfer mechanisms were simulated to see the increment of the temperature on the substrate through the gap. It is concluded that radiation from the hot membrane to the substrate is neglectable for temperature increase on the substrate, which is also independent from the gap. Convection through the thin air in vacuum significantly contributes to the temperature increase on the substrate, when a gap is remained. However, the increased temperature is considered relatively low for affecting the condensation on the substrate. Thus it is acceptable. The conduction happens when the membrane touches the substrate. It heats up the substrate to the temperature which does not ensure a reliable condensation of the deposited vapor. Thus it should be avoided during the evaporation. Gap control will be needed to prevent the contact from the actuated membrane. At last, in-situ gap control capability was shown by the preliminary experimental results.

In next chapter, we will show the experimental results of using the heated membrane in SL. Three different modes of SL, static mode, quasi-dynamic mode and dynamic mode, will be used. Comparison will be made between the heated membrane and the non-heated membrane, on both membrane surfaces and the transferred patterns on the substrate.

4 Stencil Lithography with Heated Membrane

4.1 Introduction

The heated stencil has been demonstrated in Chapter 2 and Chapter 3 to be able to provide solutions for both technical challenges in SL: the membrane can be heated in order to eliminate the material condensation, thus preventing the clogging of aperture; the thermally induced deformation of the membrane minimizes the gap between the aperture and the substrate, which reduces blurring of the pattern on the substrate [77, 40]. In this chapter, we use the heated stencil for improved resolution in patterning with three different operation modes: static mode (section 4.2), quasi-dynamic mode (section 4.3) and dynamic mode (section 4.4). The transferred patterns on the substrate through the apertures on heated and non-heated (conventional) stencils were compared. Clear improvement was observed with the heated stencil in terms of reduced blurring around the main structures and unclogged apertures after the deposition of thick metal film. During the operation of the heated stencil, the metal film condensed on the border area of the membrane where the temperature was not high enough to eliminate condensation. This thick metal film increases the thermal conduction from the hot membrane to the Si frame thus reducing the temperature difference (gradient) between the bulk Si and the heated membrane. As a result, the life time of the heated stencil is limited as more power is required during the evaporation process in order to maintain the effectiveness of unclogging the aperture, eventually leading to break down of the device. In section 4.5, we introduce a second shadow mask to confine the metal deposition only to the

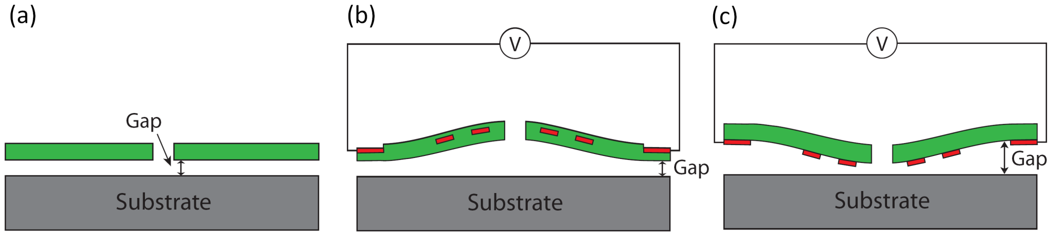


Figure 4.1: Three situations with different gaps in stencil lithography with heated membrane. (a) Static mode, applied voltage V=0. This situation is equivalent to conventional static SL with inherent gap. (b) Static mode, applied voltage V≠0. To avoid the heated membrane touching the substrate, the embedded heater design is chosen to obtain the membrane deformation which enlarges the gap. (c) Quasidynamic and dynamic mode, applied voltage V≠0. An initial gap (30 μm) is left thus the gap in the center of the membrane is minimized by using the heated stencil with non-embedded heater design.

center of the stencil membrane, which significantly extends the life time of the heated stencil.

There are three situations in the heated stencil experiments that give different gaps, as shown in Figure 4.1. In the static mode, the inherent gap is kept when the applied voltage V=0, which is equivalent to the conventional static SL, as shown in Figure 4.1a. In order to avoid touching of the membrane to the substrate through the inherent gap, the embedded heater design was chosen in the static SL experiment when the applied voltage V≠0 (see Figure 4.1b). Thus in this experiment we mainly study the influence of the unclogged aperture on the substrate pattern. In the quasidynamic and dynamic stencil experiments, an initial gap (30 μm) was remained to allow the free motion of the stencil as well as to compensate the z displacement of the membrane. Therefore, we can study both functions of the heated stencil: actuated gap reduction and unclogged aperture, by using the heated membrane with non-embedded heater design (see Figure 4.1c).

4.2 Static mode

In this section, we present the results of heated stencil lithography with static mode to demonstrate the effect of unclogged aperture on the transferred pattern. The heated stencil with Pt heater was placed directly on a Si substrate in an E-beam evaporator. The embedded Pt coil was chosen to create downwards bending when heated. That means the membrane is actuated to increase the gap during evaporation in order to avoid contact between the hot membrane and the substrate. The increased gap may cause more blurring, which is known as “Halo”, a very thin layer of metal surrounding the main deposited structure. Thus in the static SL experiment, we mainly focus on the influence of the unclogged aperture on the substrate pattern.

A DC voltage was applied to the embedded heater and the current through the heater was monitored during the whole evaporation process. The membrane was heated in vacuum (2.3×10^{-6} mbar) to 67 mW before evaporation to achieve an average temperature of ~ 800 °C and an estimated central temperature of ~ 890 °C. As we have discussed in Chapter 2, the central temperature corresponds to a critical incident rate that is allowed to be larger than 1.0 Å/s. In this experiment, an evaporation rate of 0.5 Å/s was chosen to not to push to the limit, at the same time this rate can still be used for patterning. Due to the thermal conduction induced by the condensed metal on the border area of the membrane, the temperature would be continuously decreasing if the power is kept constantly during the evaporation. Therefore, a gradually increased input power was applied in order to maintain the variation of the temperature as small as possible. 120 nm thick Al was deposited through the heated stencil and the non-heated stencil for comparison. As the stencil window areas are distributed across different temperature zones on the membrane, we are able to study the correlation between the temperature and the transferred pattern.

Figure 4.2 first shows the SEM images of the apertures on the non-heated stencil and corresponding structures on the substrate. 120 nm thick Al was deposited through apertures located on different areas of the membrane. Aperture A is in the center of the membrane, B is 120 μm away from A, and C is 120 μm from B, which is on the border of the membrane. Three apertures show the same clogging size (~ 600 nm in diameter) from the front side view. As the aperture size is 1.7 μm in diameter, considering that the clogging size is linear to the thickness of deposited material [41], the aperture will be fully clogged after ~ 340 nm Al deposited on the membrane. 120 nm Al formed a uniform layer across the membrane, which indicates the same grain size of Al around the apertures. The blurring surrounding the main structure on the substrate is a thin layer of metal. It does not give a good contrast on Si substrate in SEM. Thus, in order to visualize the blurring, a 10 s contrast etching was performed. It is a silicon dry anisotropic etching using SF_6 and CF_4 with an Alcatel 601 equipment. The Si etching rate is 400 nm/min, with a selectivity to aluminum of ~ 100. Thus ~ 60 nm Si was etched away. As the membrane is flat, the gap is uniform between apertures and the substrate. Therefore, the same halo was observed on the substrate patterns. The "Halo" sizes are all 1.1 μm for aperture A, B and C. The cause of halo can be explained by both geometric setup and the surface diffusion of the atoms. Thus, it depends on the gap between the membrane and the substrate as well as the type of substrate which gives different surface energy [40].

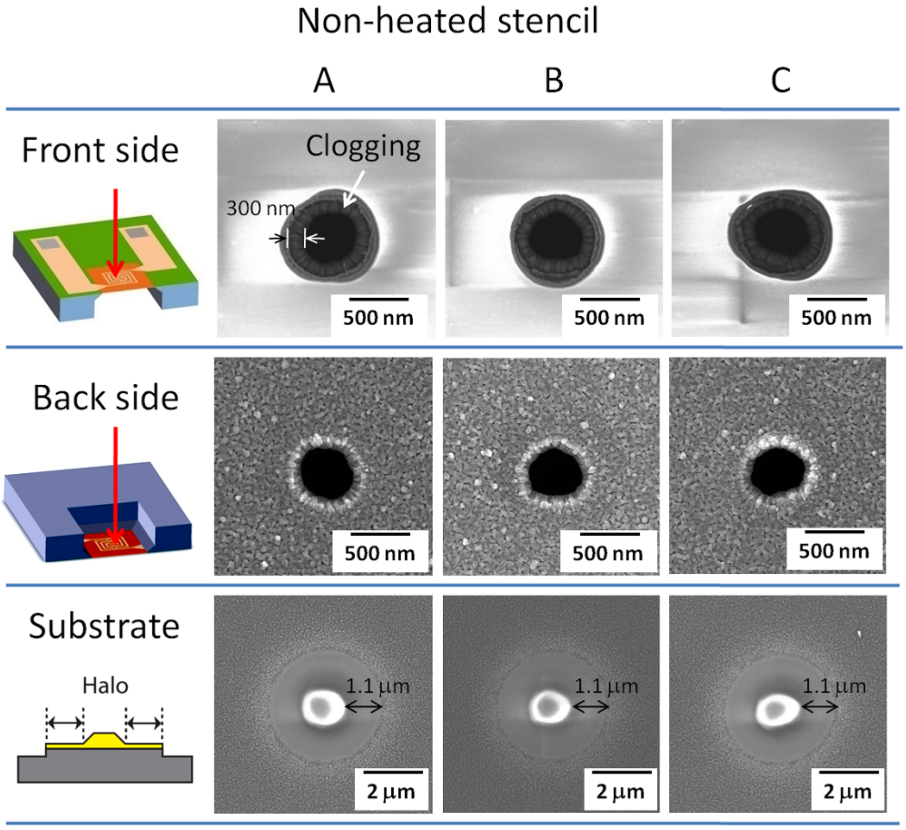


Figure 4.2: SEM images of the apertures on the non-heated stencil and corresponding structures on the substrate. Aperture A is in the center of the membrane, B is 120 μm away from A, and C is 120 μm from B, which is on the border of the membrane. Three apertures show the same clogging size (~ 600 nm in diameter). As the membrane is flat, the gap is uniform between apertures and the substrate. Thus almost the same "Halo" was observed on the substrate patterns. The "Halo" size for aperture A is 1.1 μm, for aperture B is 1.1 μm, and for aperture C is 1.1 μm.

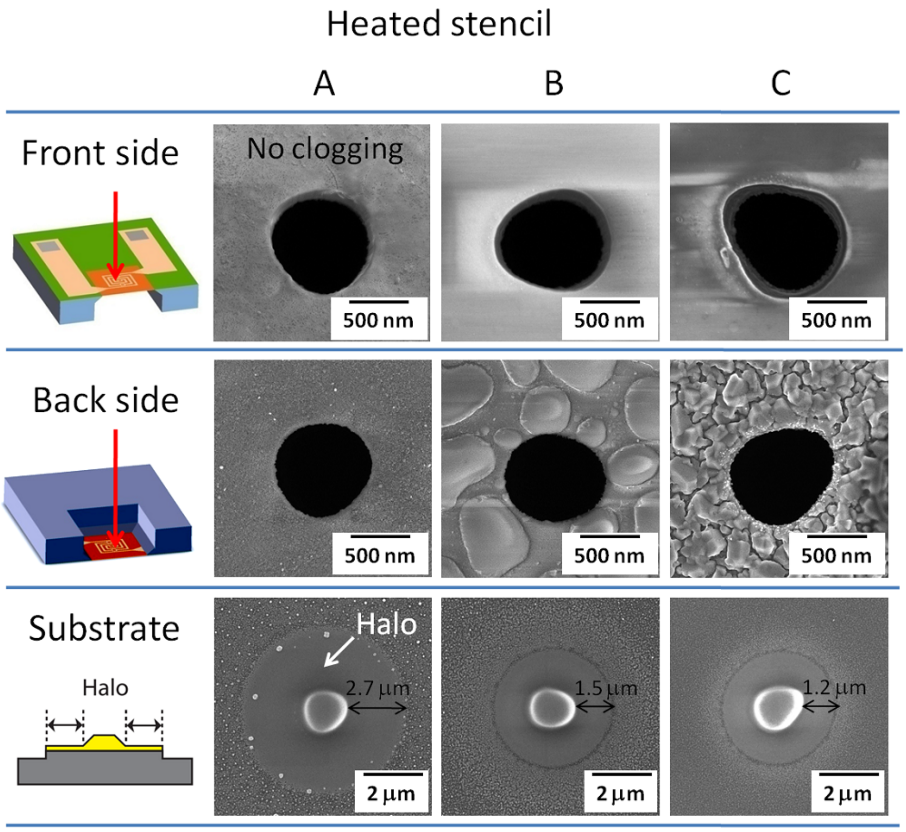


Figure 4.3: SEM images of the apertures on the heated stencil and corresponding structures on the substrate. Aperture A is in the center of the membrane, B is 120 μm away from A, and C is 120 μm from B, which is on the border of the membrane. Thus, the temperature T of the aperture on the membrane is, $T_A > T_B > T_C$. No clogging was observed on three apertures. As the membrane has deformation which increases the gap, the pattern deposited through aperture A shows the biggest "Halo" (2.7 μm) among the three (aperture B (1.5 μm) and C (1.2 μm)).

As comparison, *Figure* 4.3 shows the results from the heated stencil. SEM images of the apertures on the heated stencil and corresponding structures on the substrate are illustrated. Apertures on the same positions as which on the non-heated stencil were chosen for comparison. The front side view demonstrates no clogging from aperture A and B, while a rougher edge can be seen on the side wall of aperture C, which is due to partial clogging from the material on the back side of the membrane. The back side view reveals the formation of Al film on different temperature zones. Aperture A has the highest temperature, which prevents the condensation of Al thus no obvious grain was observed. Aperture B has lower temperature which cannot totally avoid condensation of Al. However, the temperature is still high enough to allow motion of Al atoms forming isolated droplets. The edge of the aperture acts as the boundary which stops the Al droplets from clogging the aperture. Thus, the membrane is partially covered by Al film, but the effectiveness of unclogging still remains in this temperature zone. Aperture *C* has the lowest temperature which cannot stop Al from forming a continuous film, and which is responsible for the rough edge observed from the front side view. The mobility of Al atoms in this temperature zone allows Al to form bigger grains than the case without heating. The rearrangement of Al grains clearly slows down the clogging rate. The substrate was inspected after contrast etching. As we can see from the SEM images, a much bigger haloh with 2.7 μm was observed from the substrate structure which corresponds to aperture A. When the position of the apertures gets further away from the center of the membrane, the size of halo decreases, to 1.5 μm for aperture *B* and to 1.2 μm for aperture *C*. This is due to the downwards bending of the membrane during the deposition, which enlarges the gap between aperture and the substrate. The largest deformation occurred in the center of the membrane where aperture *A* is located, which resulted in a bigger halo. As the gap gets smaller at the places where aperture *B* and *C* are located, the size of halo is also reduced.

The profile of the the substrate structures should provide important information about the effectiveness of unclogging aperture. However, AFM inspection could not be performed in this experiment due to improper handling of the sample. But from the SEM images , we can still try to analyze the profile of the substrate structures, as shown in *Figure* 4.4. SEM images were taken from the top without tilting. Thus a strong contrast on the edge of the main structure from the non-heated stencil experiment indicates a height difference, which can be translated to a side wall with slope, as schematically shown in the profile. The diameter on the top of the main structure d_t is much smaller than that on the bottom d_b, indicating a more conical shape. This is due to the gradually clogged aperture during evaporation. For comparison, a clear edge can be observed on the main structure from the heated stencil experiment, implying a more straight side wall, as illustrated in the schematic profile. Thus, a more columnar shape main structure can be observed on the substrate, as d'_t is close to d'_b.

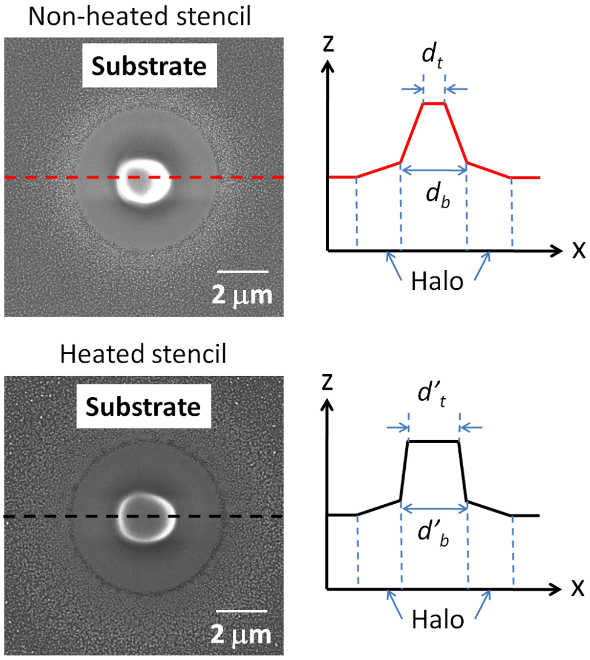


Figure 4.4: Profile of the structures on the substrate deposited through non-heated and heated stencil. SEM image of the structure from non-heated stencil implies a more conical shape main structure, as the diameter on the top d_t is much smaller than of that on the bottom d_b. A more columnar shape main structure can be observed on the substrate with heated stencil, as d'_t is close to d'_b.

There is one issue concerning the stability of the heated stencil we encountered during the experiment. In order to get high enough temperature for avoiding condensation of material, the membrane was heated up close to the maximum power. However, long time operation (120 nm Al with 0.5 Å/s takes ~ 40 min) causes degradation to the Pt electrode due to electro-migration. This limits the life time of the heated stencil in one pump-down as well as the reusability in multiple experiments. Although high temperature can prevent condensation, avoiding clogging of the aperture does not necessarily require zero condensation. As it has been illustrated in *Figure* 4.3, aperture B was kept unclogged despite the forming of Al droplets on the back side of membrane. Thus, temperature can be lower as long as the clogging rate can be significantly reduced. Lower temperature could ensure the long time operation of the heated stencil, at the same time minimize the clogging rate. In later experiment, a lower temperature is adopted for longer operation time purposes.

4.3 Quasi-dynamic mode

In this section, we present the results of heated stencil lithography in quasi-dynamic mode to demonstrate both effects of unclogged aperture and actuated gap reduction on the formation of transferred pattern. The heated stencil used in this experiment has non-embedded heater thus providing upwards bending for reducing the gap. The heated stencil was placed on a piezo stage for moving the stencil in xy plane and controlling the gap in z direction. The substrate was fixed on a non-movable holder and was aligned manually with the heated stencil. A DC voltage with 3.8 V was applied to the heated stencil. The membrane was heated in vacuum (1.5×10^{-6} mbar) to 48 mW before evaporation to achieve an average temperature of ~ 650 °C and an estimated central temperature of ~ 700 °C, corresponding to a critical incident rate of 0.005 Å/s of Al. As we discussed in section 4.2, due to long operation time purposes, a lower power was applied in order to maintain the stability of the device. In this experiment, an evaporation rate of 0.5 Å/s was used. Therefore the temperature on the membrane is not high enough to prevent condensation of material on the surface, but clogging rate can still be significantly reduced. Four consecutive depositions were performed in quasi-dynamic mode (step and repeat), with first three times 50 nm Al and fourth time 80 nm Al deposited. A thicker material deposited on the fourth time was to try to fully clog the aperture on the non-heated stencil. The space between each step is 5 mm to make sure the later deposited structure has no influence on the pre-deposited pattern. 30 μm gap was left for studying the effectiveness of actuated gap reduction on the transferred pattern. *Figure* 4.5 schematically shows the stencil trajectory during the quasi-dynamic stencil lithography experiment. Comparison will be made between the non-heated and heated stencil from two aspects: clogging-free aperture and actuated gap reduction, as following.

Clogging-free aperture

Figure 4.6 shows SEM images of the substrate patterns from the non-heated stencil and the heated stencil in quasi-dynamic mode. Apertures in the center of both non-heated and heated stencil were chosen for comparison. d_{main} is the size of the main structure from non-heated stencil and d'_{main} is the size of the main structure from heated stencil. In the case of non-heated stencil, a clear trend can be observed from the first deposited pattern to the fourth one.

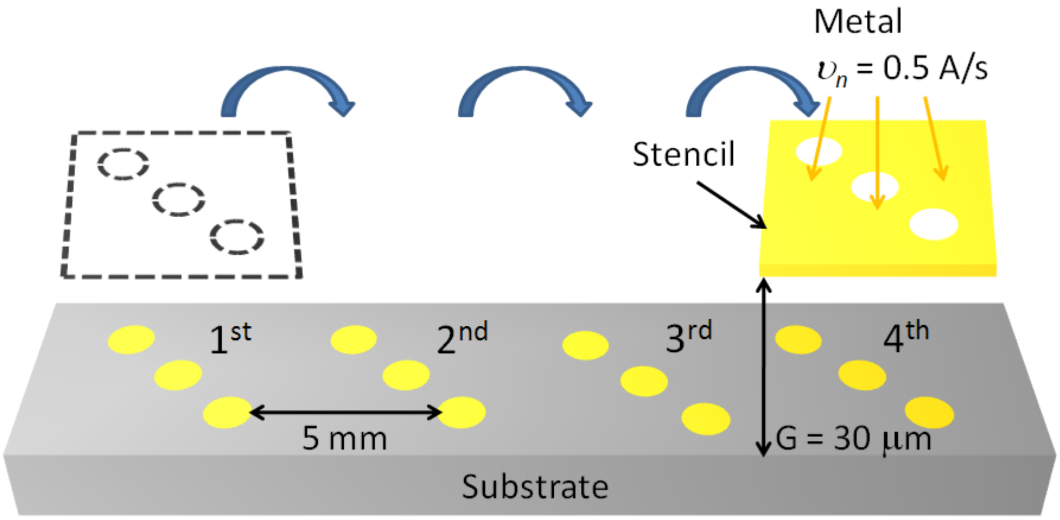
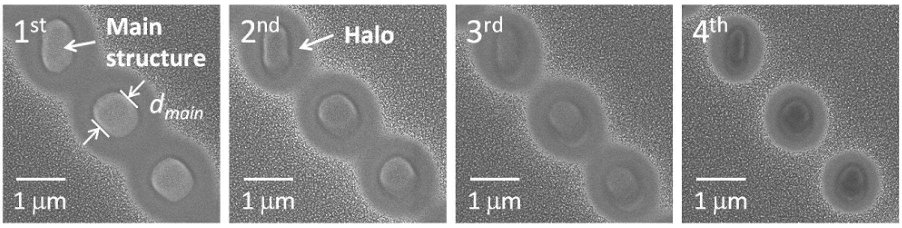


Figure 4.5: Schematics of the quasi-dynamic stencil lithography. Four consecutive depositions were performed in quasi-dynamic mode (step and repeat), with each time 50 nm Al deposited. The deposition rate is 0.5 Å/s. 30 μm gap was left for compensating the upwards bending of the heated membrane.

d_{main} decreases in each step due to the clogging of the aperture by the accumulated material from previous steps, which reduces the effective aperture size in each step. Accordingly, the halo also reduces when the effective aperture size is smaller. Here, the 30 μm gap was remained the same in each step. In the case of heated stencil, d'_{main} remains almost the same, as the heated stencil prevents clogging of aperture. In the first and second deposition, a smaller halo size can be seen compared to the non-heated stencil. This is due to the reduced gap ($< 30\mu$m) induced by the deformation of the membrane, leading to an improvement in the pattern resolution. The halo starts to increase from the third deposition, eventually show the same halo in the fourth deposition as the first deposition by using non-heated stencil. It implies a equal gap (30 μm) in the heated stencil. This is due to the accumulation of material on the back side of the stencil, which changes the mechanical property of the membrane, making it harder to bend. More specifically, as the temperature of 650 °C was remained the same in four depositions, the accumulated material on the membrane diminished the effective thermal expansion coefficient of the membrane, leading to less z displacement. To overcome this issue, a higher temperature should be maintained in order to eliminate condensation of material. However, current device cannot operate at high temperature over a long time. More development would be needed to fabricate more robust devices.

Non-heated stencil



Heated stencil

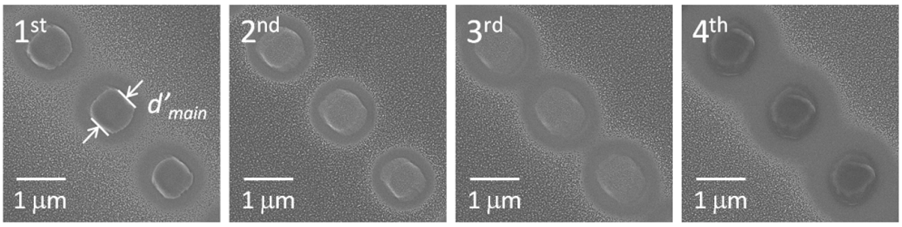


Figure 4.6: SEM images of the substrate patterns from the non-heated stencil and the heated stencil with quasi-dynamic mode. d_{main} is the size of the main structure from non-heated stencil and d'_{main} is the size of the main structure from heated stencil. d_{main} decreases in each step due to clogging of aperture on the non-heated stencil. d'_{main} remains the same as heated stencil prevents clogging of aperture.

In *Figure* 4.7 the size of the main structure on the substrate versus the total thickness of deposited Al is plotted. Comparing the main structure between the first and fourth deposition through the heated stencil, the size reduces from 1 μm to 980 nm with a shrinkage of 2 %. However, it is 40 % shrinkage in the case of the non-heated stencil, the size of the main structure decreasing from 900 nm to 540 nm. SEM images show the apertures from front top view after the fourth deposition. The non-heated aperture has almost been fully clogged while the heated aperture has only few Al droplets formed on the side wall.

AFM inspection was performed to study the profile of the transferred pattern on the substrate. *Figure* 4.8 shows the AFM images of the fourth time deposited structures on substrate through non-heated and heated stencil. Apertures in the center of the membrane were chosen. Non-heated stencil shows a conical shape substrate pattern due to the gradually clogging of aperture during the evaporation. The heated stencil illustrates a more columnar structure on the substrate, indicating no clogging happened during the deposition. The plotted figure compares the profile of the substrate structures. The pattern from non-heated stencil has a tapered profile with a total thickness of ~ 90 nm, which is a bit thicker than the structure

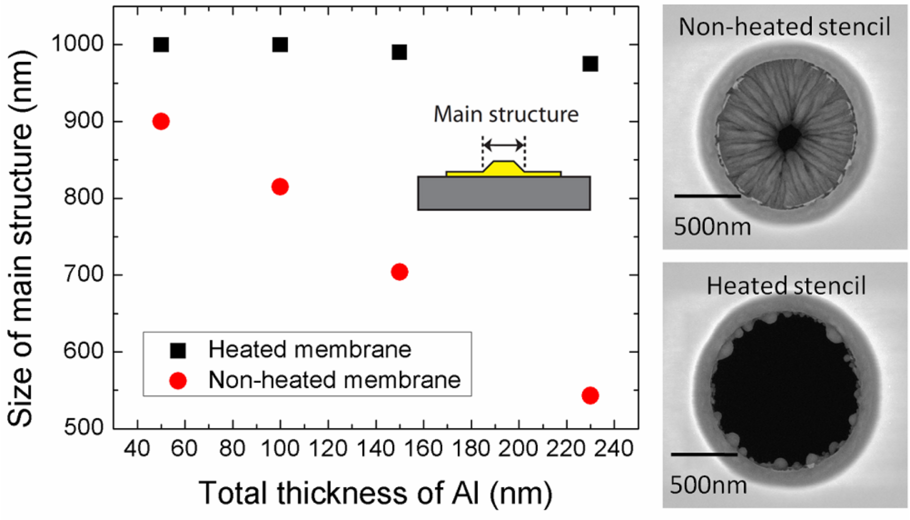


Figure 4.7: The size of the main structure on the substrate versus the total thickness of deposited Al. Comparing the main structure between the first and fourth deposition through the heated stencil, the size reduces from 1 μm to 980 nm with a shrinkage of 2 %. However, it is 40 % shrinkage in the case of the non-heated stencil, the size of the main structure decreases from 900 nm to 540 nm. SEM images show the apertures from front side view after the fourth deposition. The non-heated aperture has almost been fully clogged while the heated aperture has only few Al droplets formed on the side wall.

from the heated stencil (~ 75 nm). We attribute the difference to the small amount of heat transferred to the substrate through the actuated membrane, which slightly decreases the condensation rate. With the heated stencil, the pattern shows a more columnar shape. As the aperture on the non-heated stencil has been almost fully clogged after 230 nm Al deposited on the membrane, no further use of the stencil can be expected unless selectived etching of Al on the membrane is performed. However, the heated stencil can still be used for patterning thus significantly prolongs its life time.

Actuated gap reduction

The gap between the stencil and the substrate can be modulated by thermal actuation of the membrane. The initial gap before each deposition was 30 μm and it was reduced in the center of the membrane to ~ 7μm with 48 mW input power to the heated stencil in vacuum, corresponding to ~ 700 °C. *Figure* 4.9 shows the profiles of the gap reduction by the heated membrane, which was measured in air with 130 mW input power. This power corresponds to the same temperature of ~ 700 °C in the air. Thus we can use this profile to illustrate the

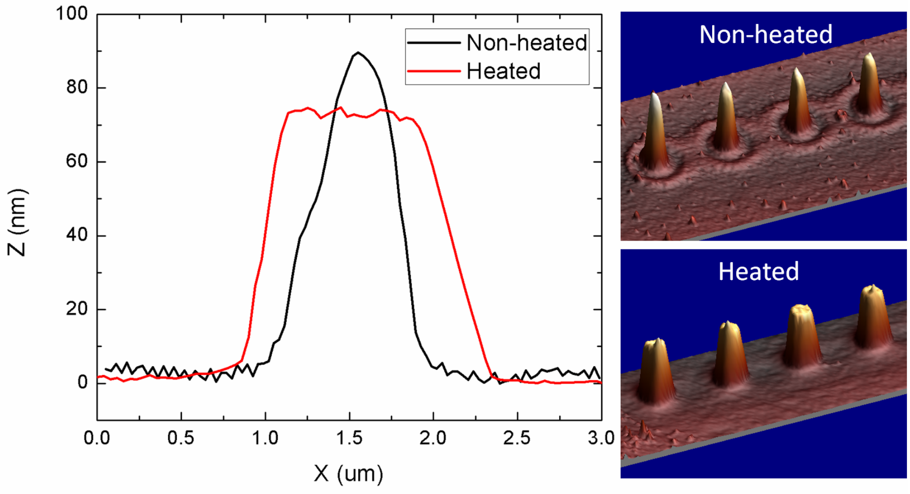


Figure 4.8: AFM images of the fourth time deposited structures on substrate through non-heated and heated stencil. Non-heated stencil shows a conical substrate pattern while heated stencil illustrates a more columned structure on the substrate.

deformation of membrane in vacuum. As apertures are located along the membrane, different gaps are expected as shown in the *Figure* 4.9, $G_A < G_B < G_C$. The reduced gap greatly improves the resolution of the deposited structures on the substrate in terms of decreasing the halo size, as illustrated in the SEM image. The halo sizes are 150 nm, 420 nm and 610 nm for aperture A, B and C, respectively.

To conclude, it is successfully demonstrated that the heated stencil can be operated in quasi-dynamic mode. The clogging-free aperture significantly prolongs the life time of the stencil and improves the quality of the transferred pattern. The gap was reduced by actuating the membrane, leading to an improved resolution in terms of minimized halo. The limits have also been explored. The applied power cannot be close to the maximum power in long time operation, which limits the maximum temperature. The condensed material on the stencil changes the effective thermal expansion coefficient of membrane, which reduces the effectiveness of gap modulation.

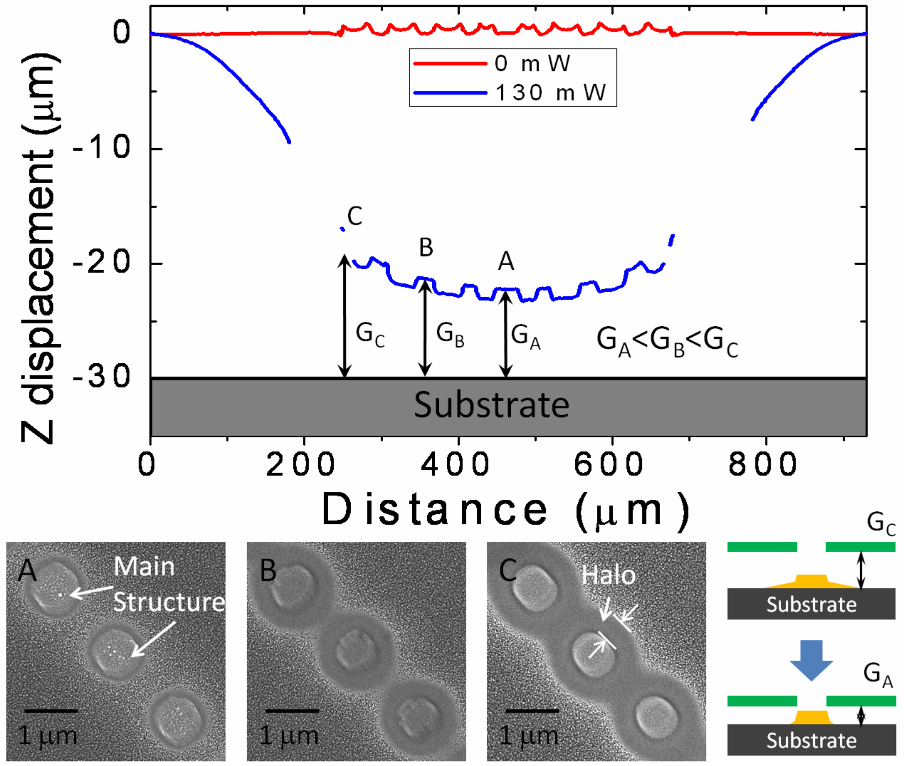


Figure 4.9: SEM images of the patterns on the substrate with different gaps. The initial gap is 30 μm. Due to the deformation of the membrane, $G_A < G_B < G_C$. Thus, the "Halo" increases from A to C as shown in the images of the corresponding structures on the substrate. The "Halo" sizes are 150 nm, 420 nm and 610 nm for aperture A, B and C, respectively.

4.4 Dynamic mode

In this section, we present the preliminary results of heated stencil lithography in dynamic mode. Compared to static and quasi-dynamic mode, dynamic stencil lithography (DSL) allows for the creation of fully customized structures with standardized stencil membrane apertures (e.g. a circular hole), which is very useful as a fast prototyping micro-/nanopatterning technique. However, due to the clogging of the aperture in conventional stencil, pattern transferred on the substrate by DSL becomes tapered, as schematically shown in *Figure* 4.10a. With heated stencil, the life time of the stencil is extended. In the *Figure* 4.10, D and D' are the diameter of the circular apertures on the non-heated and heated stencil, respectively. d is the thickness of deposited structure and w is the width of the pattern with non-heated stencil. Correspondingly, they are d' and w' in the case of heated stencil. As the aperture size gets smaller due to the clogging during the evaporation, the thickness d and the width w of the pattern keep decreasing, leading eventually to no pattern when the aperture is fully clogged. In the case of heated stencil, as the aperture stays open during evaporation, the thickness d' and the width w' are uniform along the trajectory. In the case of heated stencil without clogging, the thickness of deposited pattern can be expressed as:

$$d' = \frac{D'}{v_x} \cdot v_n \tag{4.1}$$

where v_x is the moving speed of the stencil and v_n is the deposition rate. As we have discussed, the deposition rate cannot be much higher than the reevaporation rate for keeping the aperture clean. Based on our current device, the rate v_n is ~ 0.5 Å/s. Thus when the aperture size D' is fixed, in order to get reasonable thickness of the structure, the moving speed of the stencil v_x has to be as small as possible. The lowest limit of the moving speed v_x of the xy stage in our setup is 20 nm/s. Therefore, for instance, a stencil aperture with 400 nm in diameter moving at the lowest speed (20 nm/s) with the evaporation rate of 0.5 Å/s would give a thickness of 1 nm. For some cases, a higher evaporation rate would be preferred, which requires a more robust device that allows higher temperature on the membrane. Then, the aperture with even smaller size can be applied for dynamic mode. For demonstration, we choose bigger apertures to get reasonable thickness of structures on the substrate, which is observable in the SEM.

Figure 4.11 shows SEM images of the structures deposited through non-heated and heated stencil in dynamic mode. The experiment was done in vacuum (2.0×10^{-6} mbar) with 40 mW power applied to the heated stencil. The evaporation rate for Al is 0.5 Å/s. A gap of 50 μm was left between the stencil and the substrate, thus the stencil is able to move in x direction with 20 nm/s during the evaporation. Totally 160 nm Al was deposited and the stencil was moved 65 μm. The original aperture sizes are 4.05 μm for non-heated stencil and 4.9 μm for heated stencil, thus the corresponding thickness of the structure on the substrate is ~ 10 to 12 nm. The width of the main structure decreases from 4.1 μm at the beginning to 3.7 μm at the end of the structure for the non-heated stencil, due to clogging of aperture. For comparison, the size of the main structure in the case of heated stencil remains the same, which is 5.1 μm. This

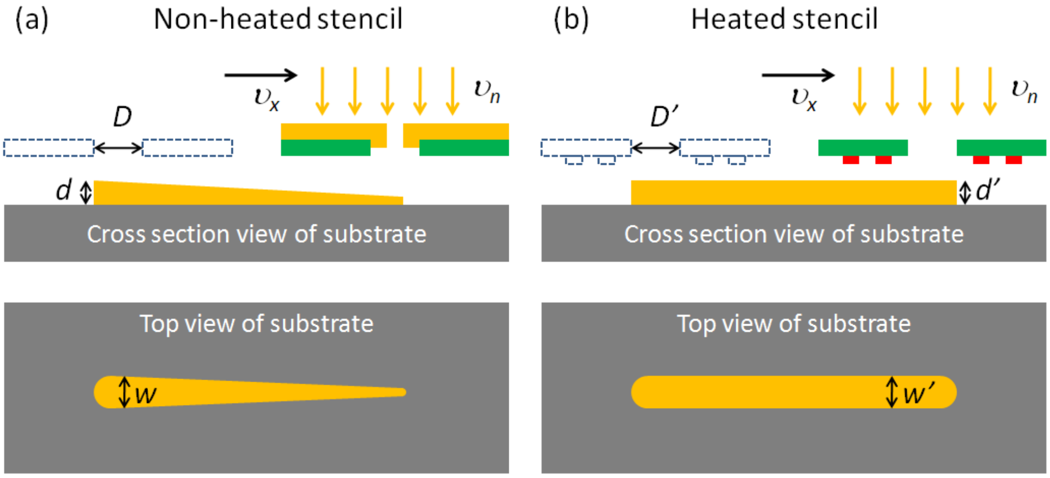


Figure 4.10: Schematics of the dynamic stenciling with non-heated and heated stencil. υ_x is the moving speed of the stencil and υ_n is the deposition rate. D and D' are the diameter of the circular apertures on the non-heated and heated stencil, respectively. d is the thickness of deposited structure and w is the width of the pattern with non-heated stencil. Correspondingly, they are d' and w' in the case of heated stencil. As aperture size gets smaller due to the clogging during the evaporation, the thickness d and the width w of the pattern keep decreasing, eventually no pattern can be observed when the aperture is fully clogged. In the case of heated stencil, as the aperture keeps open during evaporation, the thickness d' and the width w' are uniform along the trajectory.

preliminary result shows a bigger blurring around the pattern from the heated stencil, which is due to the downwards membrane deformation of the selected device. A careful selection of membrane with upwards bending would reduce the blurring.

4.5 Life Time Extension by Thermal Control of the Heated Membrane

So far it has been proven that the heated stencil improves the accuracy of pattern transfer through the aperture by leaving the aperture clogging-free and by reducing the gap through membrane actuation. However, these figures of merit quickly degrade with the accumulation of metal on the periphery of the heated membrane. The effectiveness of heating the stencil is gradually reduced because the evaporated metal layer increases the thermal conductance of the SiN membrane to the bulk Si frame. It occurs especially on the low temperature area on the border of the membrane where metal film is formed. In order to maintain a constant

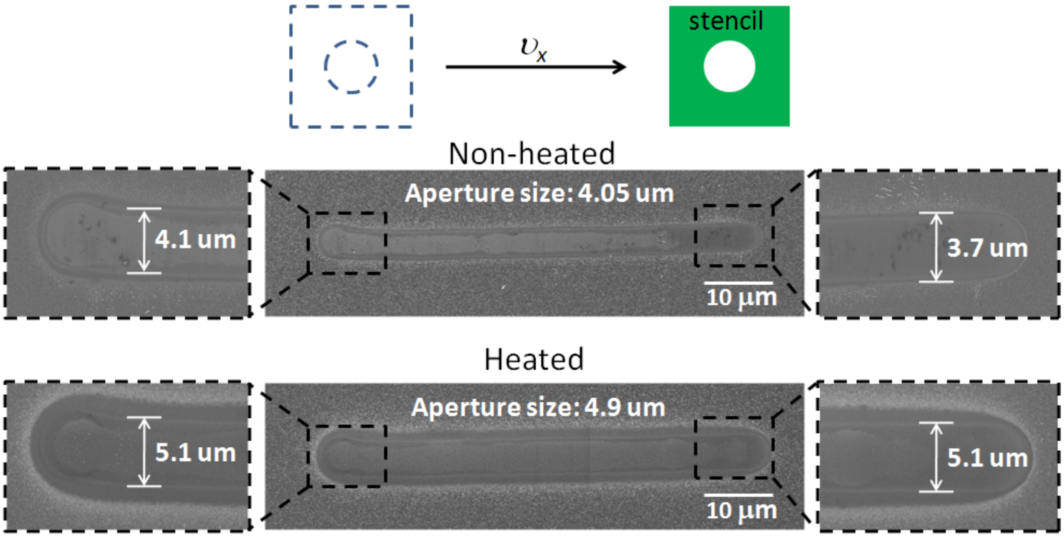


Figure 4.11: SEM images of the structures deposited through non-heated and heated stencil with dynamic mode. The original aperture sizes are 4.05 μm for non-heated stencil and 4.9 μm for heated stencil. The stencil has been moved in x direction for 65 μm. The width of the main structure decreases from 4.1 μm at the beginning to 3.7 μm at the end of the structure for the non-heated stencil, due to clogging of aperture. As comparison, the size of the main structure in the case of heated stencil remains the same, which is 5.1 μm.

membrane temperature, the input power has to compensate for the decrease in thermal resistance to the bulk Si. For example, after 200 nm of evaporated metal, the power necessary to maintain a temperature effective for unclogging is large enough to break the membrane. Therefore, the metal thickness determines now the life time of the heated membrane. In this section, we prolong the life time by using a second shadow mask to confine the deposition area on the membrane. This maintains the temperature by reducing the thermal loss through the deposited metal on the membrane.

4.5.1 Thermal Loss Decreasing the Life Time

As aforementioned, the metal deposited on the border of the membrane where temperature is low will increase the thermal loss, thus cooling the membrane. *Figure* 4.12 shows the front side illuminated images of the heated stencil before (*Figure* 4.12a) and after (*Figure* 4.12b) 100 nm Al deposited on the membrane with an operation power of 20 mW. The relatively thin metal layer condensed in the center of the membrane allows us to clearly see the Pt coil underneath. However, the metal film on the border of the membrane completely blocks the Pt

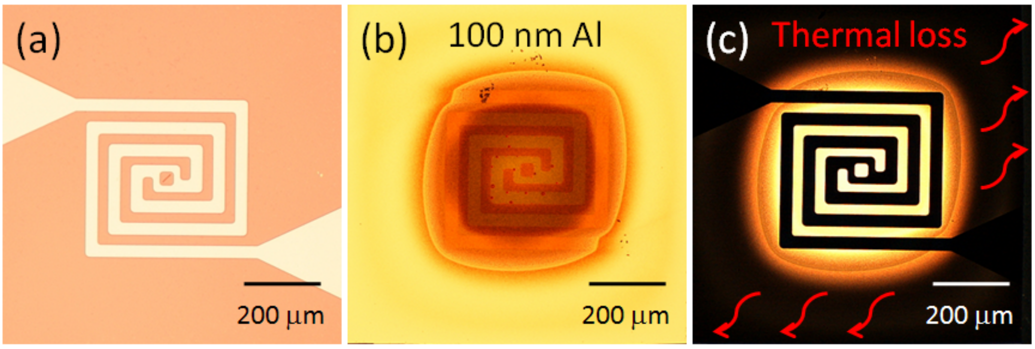


Figure 4.12: Optical images of the heated stencil before and after 100 nm Al deposited on the membrane. (a) Front side illuminated image of the heated stencil before evaporation. (b) Front side illuminated image of the heated stencil after 100 nm Al deposited on the membrane with operation power of 20 mW. (c) Back side illuminated image of the same device. The nontransparent area of the membrane indicates a thick Al film form on the membrane, which significantly increases the thermal loss that cools down the membrane.

electrode, indicating a thick layer of material formed on the membrane which is shown as the nontransparent area in the back side illuminated image (*Figure* 4.12c) of the same device. This nontransparent area significantly increases the thermal loss that cools down the membrane.

Figure 4.13 plots the membrane temperature as a function of the deposited Al thickness. When the applied power is constant (20 mW), due to the thermal loss from the deposited Al, temperature keeps decreasing linearly with the thickness of Al. 100 nm Al deposited on the membrane cools down the membrane to ~ 200 °C. Thus, in order to maintain the membrane temperature, the power has to be slowly increased, which eventually leads to the failure of the device. *Figure* 4.13b shows the temperature as a function of the deposited Al thickness, while gradually increasing the power. The deposition rate in both experiments is 0.3 Å/s. The temperature was maintained in a range of ±50 °C during the evaporation. The voltage was manually increased with a step of 0.1 V. To reduce the variation range, real time compensation loop can be introduced to the current monitoring system, so the applied voltage is automatically increased when the resistance of the heater decreases. However, this would still lead to the failure of the device when the applied power is too high. Thus we can conclude that the allowed thickness of metal is limited at a certain temperature.

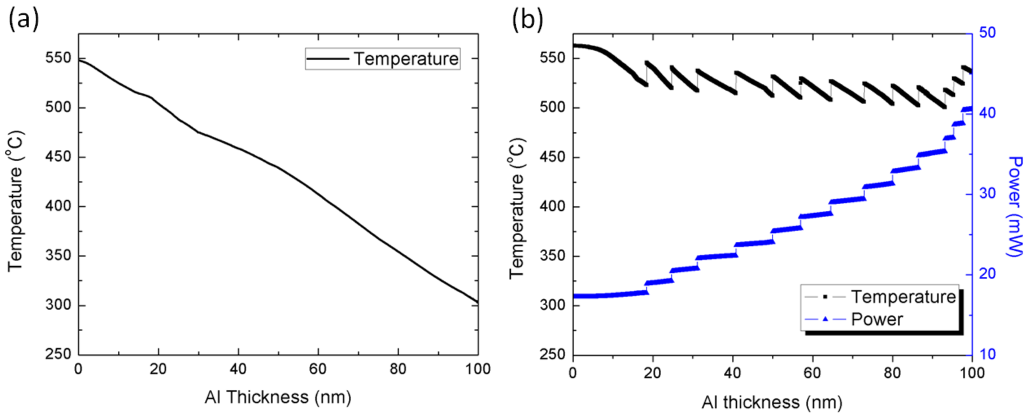


Figure 4.13: Membrane temperature as a function of the deposited Al thickness. (a) When the applied power is constant, due to the thermal loss from the deposited Al, temperature keeps decreasing linearly with the thickness of Al. (b) In order to maintain the membrane temperature, the power has to be slowly increased, which eventually leads to the failure of the device when the power exceeds the maximum value. The deposition rate in both experiments are 0.3 Å/s.

4.5.2 Thermal Control by Using the Second Shadow Mask

To maintain the temperature without increasing the applied power requires thermal control that should significantly reduce the thermal loss. A method using a second shadow mask is proposed. Schematics of the thermal control by using the second shadow mask is shown in *Figure* 4.14. An extra shadow mask is aligned with the heater, blocking the material flux outside the heating area. This confinement cuts off the thermal conduction path from the deposited metal to the bulk Si frame, which keeps the heat in the center of the membrane. The second shadow mask has an open window of 375 μm × 375 μm, which fits the heater area.

Parallel experiments were performed to see the effect of the second shadow mask on the life time of the heated stencil. Three heated stencils with identical designs were heated with the same power (30 mW), but under different conditions, as shown in *Figure* 4.15. The heating power corresponds to an average temperature of ~ 600 °C. *Figure* 4.15a,b show the front and back side illuminated images of heated stencil without 2nd shadow mask, deposition rate is 0.3 Å/s. *Figure* 4.15c,d show the images of heated stencil without 2nd shadow mask, deposition rate is 0.3 Å/s. To verify the heat loss reduction, a third experiment was performed with the deposition rate of 0.6 Å/s, as shown in *Figure* 4.15e,f. In total, 100 nm thick Al was deposited in

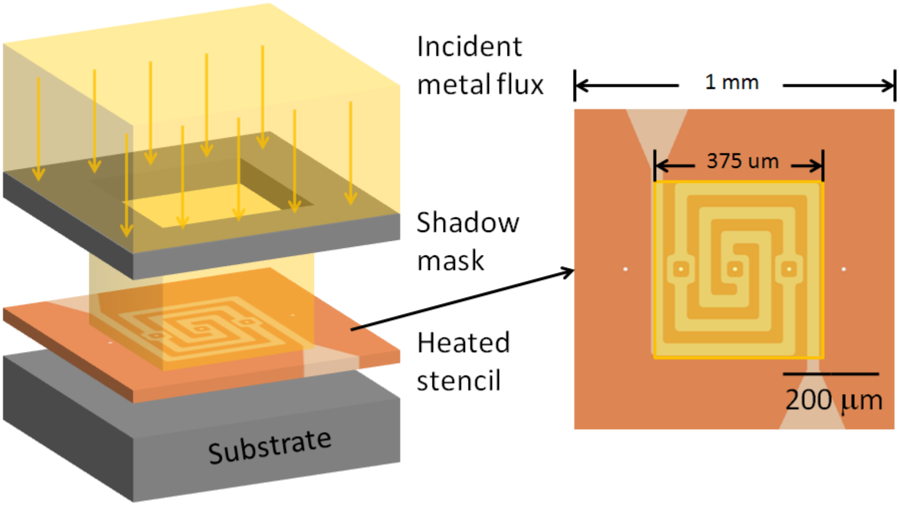


Figure 4.14: Schematics of the thermal control by using the second shadow mask. An extra shadow mask is aligned with the heater which blocks the material flux outside of the heating area. This confines the heat in the center of the membrane and significantly reduces the heat loss.

all experiments.

Figure 4.16 plots the temperature of three heated stencils as a function of the deposited Al thickness. The temperature with localized deposition of 100 nm Al drops by 20 °C, whereas it decreases by 200 °C in the case of deposition without shadow mask. No obvious difference of the temperature in localized deposition was observed between the experiments with 0.3 Å/s and 0.6 Å/s, which validates the effectiveness of the second shadow mask on thermal confinement. The localized deposition extends the life-time of the heated stencil, thus it can be used in-situ 10 times longer without increasing the applied power. There is still a slight drop of temperature (~ 20 °C) after 100 nm Al deposited. This can be compensated by increasing the power, which could extend the life time even much longer.

We also compared the surface morphology of the AL on these three heated stencils. For stability reasons, the chosen applied power is not able to prevent condensation of Al with 0.3 Å/s. In the case without the second shadow mask, Al forms small islands in the center of the membrane. While on the border, because of the thermal loss, it forms continuous film with big grains. When we place a second shadow mask to confine the deposition area with the same experiment condition, Al islands in the center become much bigger, indicating a higher temperature than the case without second shadow mask. The size of Al islands on the border is smaller than that in the center, but it is still larger than that of the center area in the case without second shadow mask, implying a more uniform temperature distribution and better thermal confinement. When the deposition was increased to 0.6 Å/s, the island size reduced in both center and border area. This could be due to the fact that the higher evaporation rate does not give enough time for the mobile Al atoms to relocate, forming therefore smaller islands.

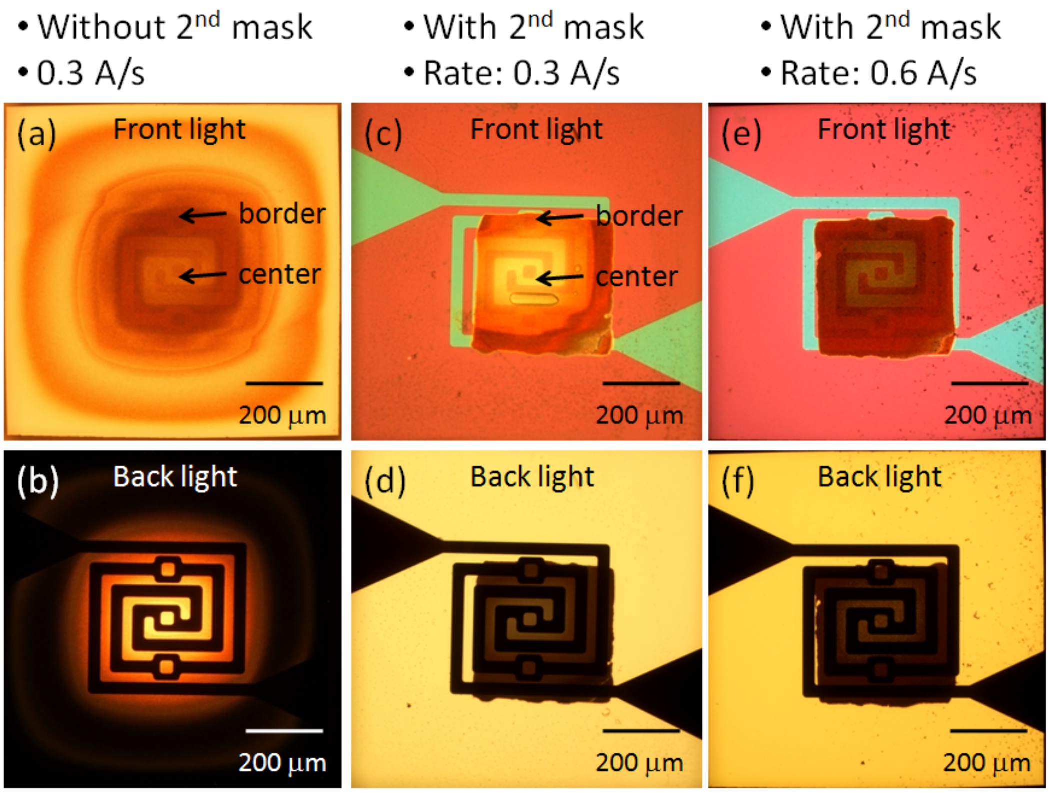


Figure 4.15: Optical images of the heated stencil with and without 2nd shadow mask for blocking the metal flux on the border of the membrane. (a) and (b) Front and back side illuminated images of heated stencil without 2nd shadow mask, deposition rate is 0.3 Å/s. (c) and (d) Front and back side illuminated images of heated stencil with 2nd shadow mask, deposition rate is 0.3 Å/s. (e) and (f) Front and back side illuminated images of heated stencil with 2nd shadow mask, deposition rate is 0.6 Å/s.

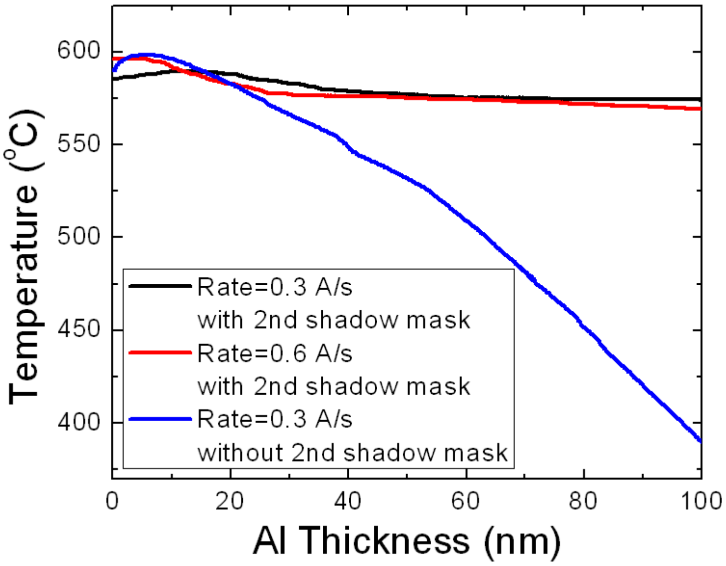


Figure 4.16: Temperature of the membrane as a function of the deposited Al thickness. Power applied to the heated stencil is constant during evaporation. The localized deposition extends the life-time of the heated stencil. The temperature with localized deposition of 100 nm Al drops by 20 °C, whereas it decreases by 200 °C in the case of deposition without shadow mask.

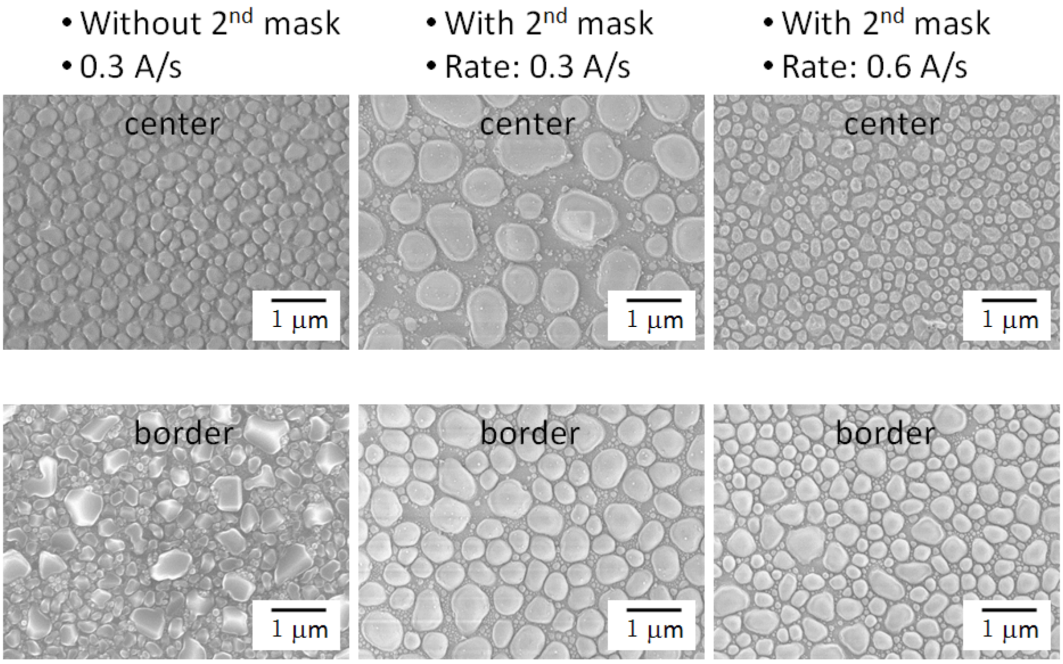


Figure 4.17: SEM images of Al deposited on the heated stencil with and without 2nd shadow mask. The corresponding area are illustrated in *Figure* 4.15.

4.6 Conclusions

To conclude, in this chapter, we have presented the use of heated stencil in SL for improved resolution in patterning with three different operation modes: static mode, quasi-dynamic mode and dynamic mode. In static mode, we demonstrated the effect of unclogged aperture on the transferred pattern. One issue concerning the stability of the heated stencil in long time operation was encountered during the experiment. Thus lower temperature is applied in later experiments without affecting the effectiveness of unclogging aperture. In quasi-dynamic mode, it is demonstrated that the clogging-free aperture significantly prolongs the life time of the stencil and improves the quality of transferred pattern, especially the main structure when thick material is deposited. The gap has been reduced by actuating the membrane, leading to an improved resolution in terms of minimized halo. However, the condensed material on the stencil changes the effective thermal expansion coefficient of membrane, which reduces the effectiveness of gap modulation. Further investigation could be focused on optimizing the performance of the device to stably work at higher temperature. In dynamic mode, preliminary results were presented to show the feasibility of using heated stencil in fast prototyping without distorting the transferred pattern. For the use of nano apertures in dynamic mode, a higher evaporation rate would be preferred as the deposited thickness of the pattern is limited by the lowest moving speed of the stage. That requires a more robust device that allows higher temperature on the membrane. We also showed a method with an aligned second shadow mask to localize the deposition area, which extends the life-time of the heated stencil at least 10 times in-situ, without increasing the applied power.

In the next chapter, we show the study of using PECVD SiC as the membrane material for making nanostencils. Comparing with LPCVD SiN, PECVD SiC arises more interest because of its robustness and cost efficiency. Besides conventional deposition through SiC stencil, we will also use it as a direct dry etching mask for patterning, where it performes better than SiN stencil in terms of resistance to etching.

5 PECVD SiC Membrane Made for Stencil Lithography

5.1 Introduction

In order to accurately transfer patterns by stencil lithography (SL), the membrane material has to be physically and chemically stable and easy to process from micro to nanoscale, which makes SiN an excellent candidate. However, our previous studies found limitations for specific designs, where the membranes could be distorted and therefore the pattern transfer changed. This is usually due to the apertures distorted by the induced stress from deposited materials and by the dynamically enlarged gap between the stencil and the substrate from the deformation of the membrane [86, 90]. To solve this problem, the fabrication process has to become more complex by introducing reinforcement corrugations on the membranes [87]. Thus, we would like to explore new membrane materials which are more robust in some applications without complicating the fabrication process. In this chapter we present the use of PECVD silicon carbide (SiC) thin film for stencil applications. A higher robustness to deformation and a better resistance to etching of the SiC membranes compared to SiN membrane are demonstrated. The SiC stencils allow for a wider choice of the deposited materials, leading themselves to a more precise pattern duplication and less complicated resistless dry etching applications [17].

SiC as a recent material for microsystems applications has received a lot of attention [91]. SiC film in either crystalline or amorphous states has many interesting properties, such as high mechanical strength, high thermal conductivity, stability at high temperature and

Properties	c-SiC	SiN
Melting point (°C)	1800	1900
Young's modulus (GPa)	448	~200
Thermal conductivity (W/cmK)	5.0	~2.0

Table 5.1: Comparison of properties between c-SiC and SiN. Typical values are chosen to show here.

remarkable chemical inertness. These properties make it a very attractive candidate for MEMS applications in harsh environments [92, 93, 94]. Due to the development of micromachining technologies in realizing SiC microstructures, both bulk [95] and surface machining [96] of SiC film are now possible. This provides us an excellent starting point for investigating the possibility of SiC membrane for stencil applications. SiC is a good candidate for stencil membrane material because of its higher Young's modulus that makes it more resistance to bending, its higher thermal conductivity that decreases the thermally induces deformation and its extreme chemical inertness that makes it easier to be used for etching through. Depending on the fabrication process, different types of SiC film can be made, including crystalline SiC (c-SiC) [97, 98], poly-crystalline SiC (Poly-SiC) [93] and amorphous SiC (a-SiC) [99]. Table 5.1 compares the typical value of properties between c-SiC and SiN. SiC demonstrates higher Young's modulus and higher thermal conductivity, which is expected to provide a better performance than SiN for stencil application.

For the preparation of the SiC thin film, chemical vapor deposition (CVD) methods are the main technique used, producing high-quality films on large area, with high volume. Both CVD techniques, LPCVD and PECVD, are applicable in preparing SiC film for bulk and surface machining [100]. LPCVD usually operates at high temperature (800 °C to 1000 °C), which limits the option for substrate material. As comparison, PECVD requires much lower temperature (< 400 °C), which makes it compatible with IC process [101] as well as suitable for post-processing surface micromachining [102]. Another big advantage of PECVD prepared SiC film is that by varying the deposition and annealing parameters, thin film properties such as stress and Young's modulus can be optimized for targeted application. In this work an optimized PECVD process was used to provide low-stress thin film for stencil application.

In this chapter, we present the fabrication and characterize the performance of both microstencils and nanostencils with PECVD SiC membrane. Section 5.2 introduces the fabrication process of SiC stencil with aperture size from 100 μm down to 50 nm. Section 5.3 shows the use of SiC stencils as shadow masks to deposited metal through the apertures. SiC stencils are also used as direct dry etching masks to pattern the substrate, as shown in section 5.4. Comparison between SiC and SiN stencils is made in section 5.5. Section 5.6 concludes this work.

5.2 Fabrication of SiC Stencils

5.2.1 Preparation of PECVD SiC film

PECVD SiC thin film was prepared in collaboration with Prof. Haixia Zhang's group in Peking University. SiC film was deposited on the front side of double-side polished Si wafer by PECVD (STS, UK). During the PECVD process, SiH_4 (silane gas) and CH_4 (methane gas), respectively, served as the silicon source and the carbon source. Typical temperature for the reaction in PECVD was 300 °C. The flow rate of CH_4 was carefully chosen in order to make a dense SiC thin film which is neither too silicon-rich, which would induce low mechanical performances, nor too sparse, which would cause nanosize pinholes in the membrane [103]. The as-deposited amorphous SiC film has a large compressive stress, for example -450 MPa for a 1 μm thick thin film. Consequently, a thermal annealing process at temperatures from 400 to 500 °C is essential for adjusting the stress to the adaptable range (0–200 MPa) for SL applications. The intrinsic stress of the SiC can be tuned from compressive to tensile by varying the annealing time. The annealing temperature used in this experiment was 450 °C for 50 min, resulting in a tensile stress of 130 MPa for 200 nm thick film and 110 MPa for 540 nm thick film. SiC stencils with both thicknesses were fabricated with details shown in section 5.2.2. During the annealing process, the amorphous SiC is starting to crystallize and thus enhance its robustness, which translates into a higher Young's modulus [99]. The film we used has a measured Young's modulus of ~ 300 GPa. In principle, zero stress PECVD SiC thin films with various thicknesses can be fabricated to minimize the influence of the membrane material on the performance in SL application. The annealing process is also very helpful to densify the SiC thin film, which improves the chemical inertness in etching processes.

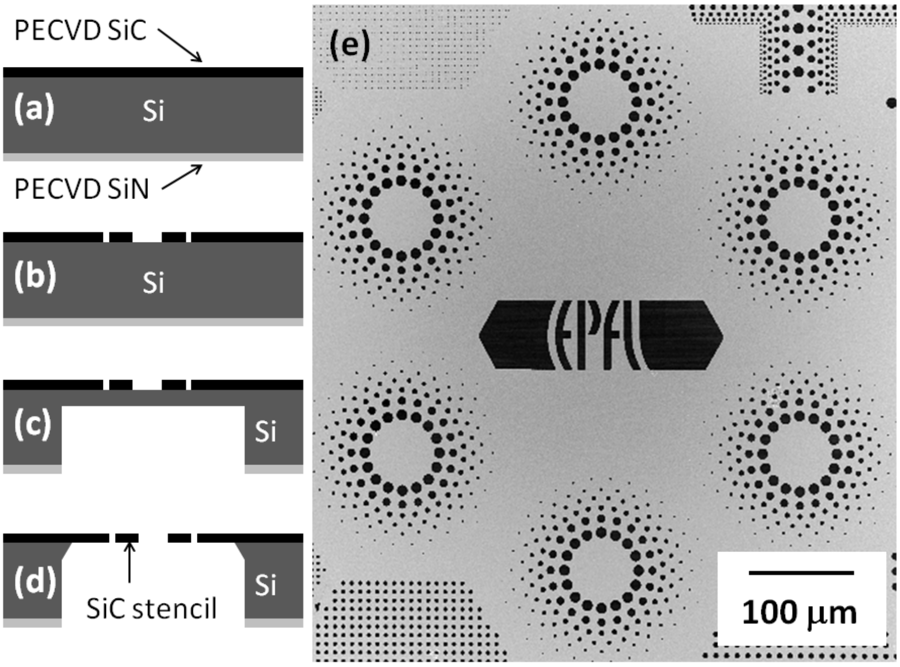


Figure 5.1: Schematics of the fabrication process and SEM image of SiC microstencil. (a) Deposition of PECVD SiC and PECVD SiN; (b) SiC dry etching by using the patterned photoresist as etching mask; (c) SiN and Si deep dry etching to open the back side window; (d) KOH wet etching to release the membrane; and (e) SEM image of the membrane with 1 mm×1 mm in area. The minimum aperture size is 2 μm.

5.2.2 Fabrication Process

We developed the fabrication process for both microstencil and nanostencil with SiC membrane. The fabrication of the microstencil (Figure 5.1a-d) started from a Si wafer with 540 nm thick PECVD SiC on the front side and 200 nm thick PECVD SiN on the backside. Front side SiC was patterned by conventional photolithography with minimum aperture size of 2 μm. Using photoresist (2 μm AZ92xx) as etching mask, the pattern was transferred to SiC by dry etching with the recipe of SF_6/O_2 (130 sccm / 20 sccm) in AMS 200 DSE. The etching rate of SiC is about 200 nm/min. A following DRIE process was performed to open the membrane windows on the backside by sequentially etching SiN and Si. The residual 50 μm thick Si left after the DRIE process was then etched away by KOH to release the membrane. Figure 5.1e shows the SEM image of a patterned 1 mm×1 mm area free standing SiC membrane.

The fabrication of nanostencil employs E-beam lithography for nano-patterning. As the E-beam resist is too thin to stand the SiC dry etching process, an extra Al hard mask is added

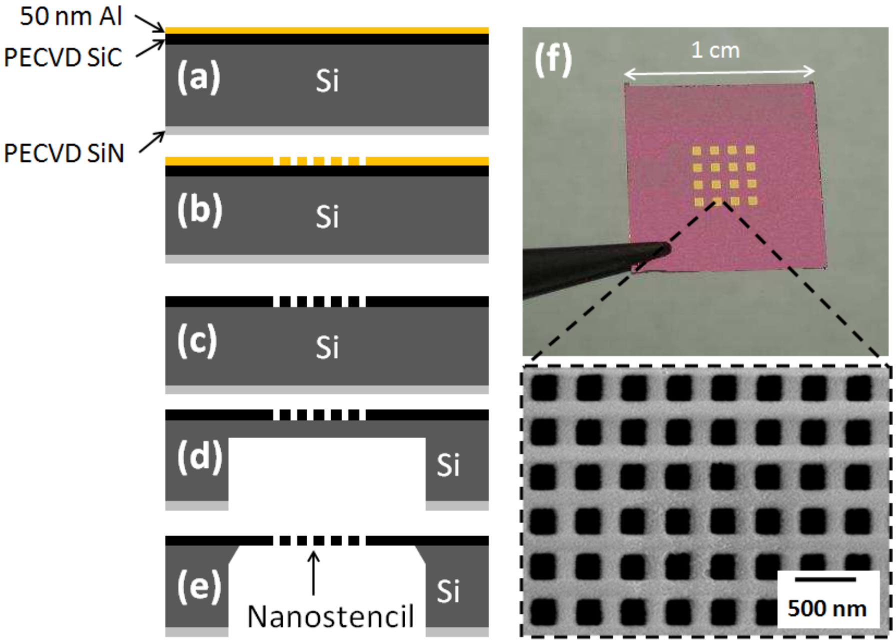


Figure 5.2: Schematics of the fabrication process and optical/SEM images of SiC nanostencil. (a) 50 nm thick Al coated on PECVD SiC; (b) E-beam lithography to pattern nano-apertures and then transfer to Al by dry etching; (c) Using Al as hard mask to pattern SiC by dry etching; (d) SiN and Si deep dry etching to open the back side window; (e) KOH wet etching to release the membrane; and (f) optical image of fabricated SiC nanostencil and zoom-in SEM image of the nano-apertures. The chip size is 1 cm × 1 cm with in total 16 membranes. Apertures with different sizes and spaces are arranged on each membrane, which is 300 μm × 300 μm in size. SEM image shows square aperture array with 200 nm in size and 200 nm in space.

to transfer the pattern from E-beam resist to SiC film. Here we aim at sub 100 nm aperture size, thus a 200 nm thick SiC thin film was used to reduce the aspect ratio. Figure 5.2a-e schematically show the fabrication process. First, 50 nm Al was deposited on top of 200 nm SiC. Then the substrate was patterned by E-beam lithography (Vistec EBPG5000ES) with a spin-coated 160 nm thick ZEP resist. The patterns were transferred to Al by fluoride based dry etching in STS Multiplex ICP with an etching rate of 200 nm/min. Using Al as hard mask, SiC etching was performed using the same recipe as the microstencil with less etching time. After the definition and deep etching for the back side window, the membrane was released by KOH wet etching. Figure 5.2f shows the optical image of the chip level SiC nanostencil. The chip size is 1 cm × 1 cm with in total 16 membranes. Apertures with different sizes and spaces are arranged on each membrane, which is 300 μm × 300 μm in size. The SEM image shows a square aperture array with 200 nm in size, and 200 nm apart.

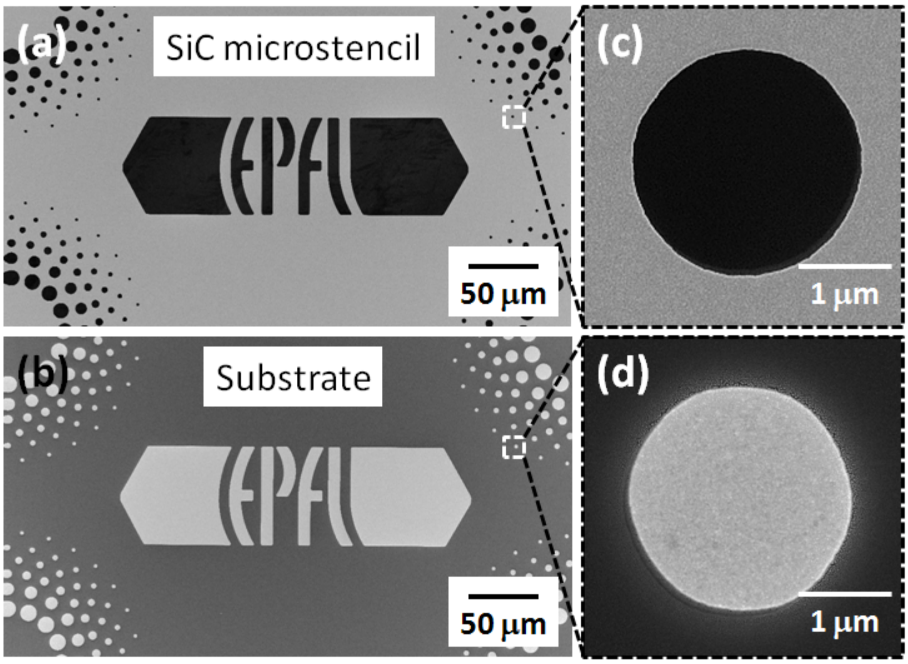


Figure 5.3: SEM images of Au deposition through SiC stencil. (a) SiC microstencil; (b) 5 nm Ti / 50 nm Au deposited on Si substrate through the stencil; (c) Aperture on SiC stencil with 2 μm in diameter and (d) corresponding pattern on the substrate.

5.3 Deposition of Metals through SiC Stencils

The SiC stencils were first used for metal deposition to demonstrate their capability for micro-/nano-patterning. The SiC stencils were placed on Si substrates for metal deposition in an e-beam evaporator. Figure 5.3 shows the SEM images of apertures on SiC microstencil and the corresponding patterns on the substrate after depositing 5 nm Ti / 50 nm Au through the stencil. The accurately duplicated patterns demonstrate the feasibility for SiC stencil in SL applications. The results are comparable to those from SiN stencil deposition, where the main challenge is the blurring of the pattern. Since Au is not compatible with our dry etching system, contrast etching like what can be performed to deposited Al structure for visualizing the halo area cannot be done. However, we can still qualitatively compare the blurring from the SEM images. Figure 5.4 presents the SEM images for comparison between the Ti/Au dots with 2 μm in diameter deposited through SiN stencil and SiC stencil. Zoom-in images show similar blurring size between SiN and SiC, indicating similar gaps during deposition.

As SiC microstencil demonstrates excellent performance in transferring micropatterns

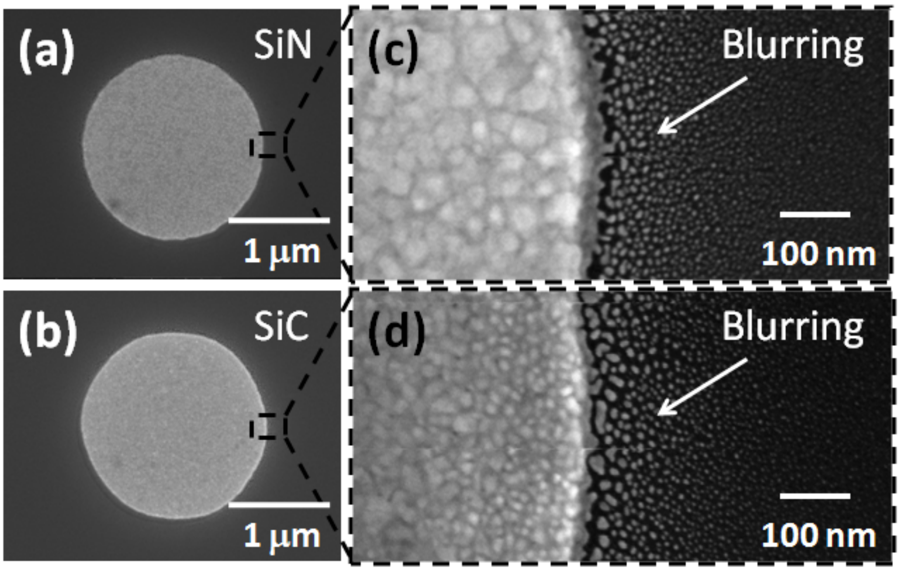


Figure 5.4: SEM images of comparison between the Ti/Au dots with 2 μm in diameter deposited through SiN stencil (a) and SiC stencil (b). Zoom-in images show similar blurring size between SiN (c) and SiC (d), indicating similar gaps during deposition.

to substrate, more investigation of patterning through SiC nanostencils was performed to explore the nano-patterning capability. Stenciled metallic nanodots have been successfully demonstrated for plasmonic biosensing applications which show great interest [104, 6]. Thus we explored the feasibility of using SiC nanostencil for creating metallic nanodots. *Figure* 5.5 shows the SiC nanoholes and deposited nanodots with different size and spacing on Si substrate. The deposited dot arrays have a periodicity corresponding to the hole array in the stencil membrane. 45 nm of Au and 40 nm of Al were deposited. Nanodots down to ~ 50 nm were achieved by using SiC nanostencil. The stencil holes ≥200 nm present a squared shape, as they were designed. The square shape is also transferred to the deposited nanodots. However, for 100 nm and 50 nm wide holes, the squared shape is rounded in the stencil, which also produced rounded dots on the substrate. The precise shape and size of the structures is also affected by the blurring and mobility of the atoms on the substrate. As Au has shown higher mobility than Al [6], the patterns are more blurred in the Au nanodots.

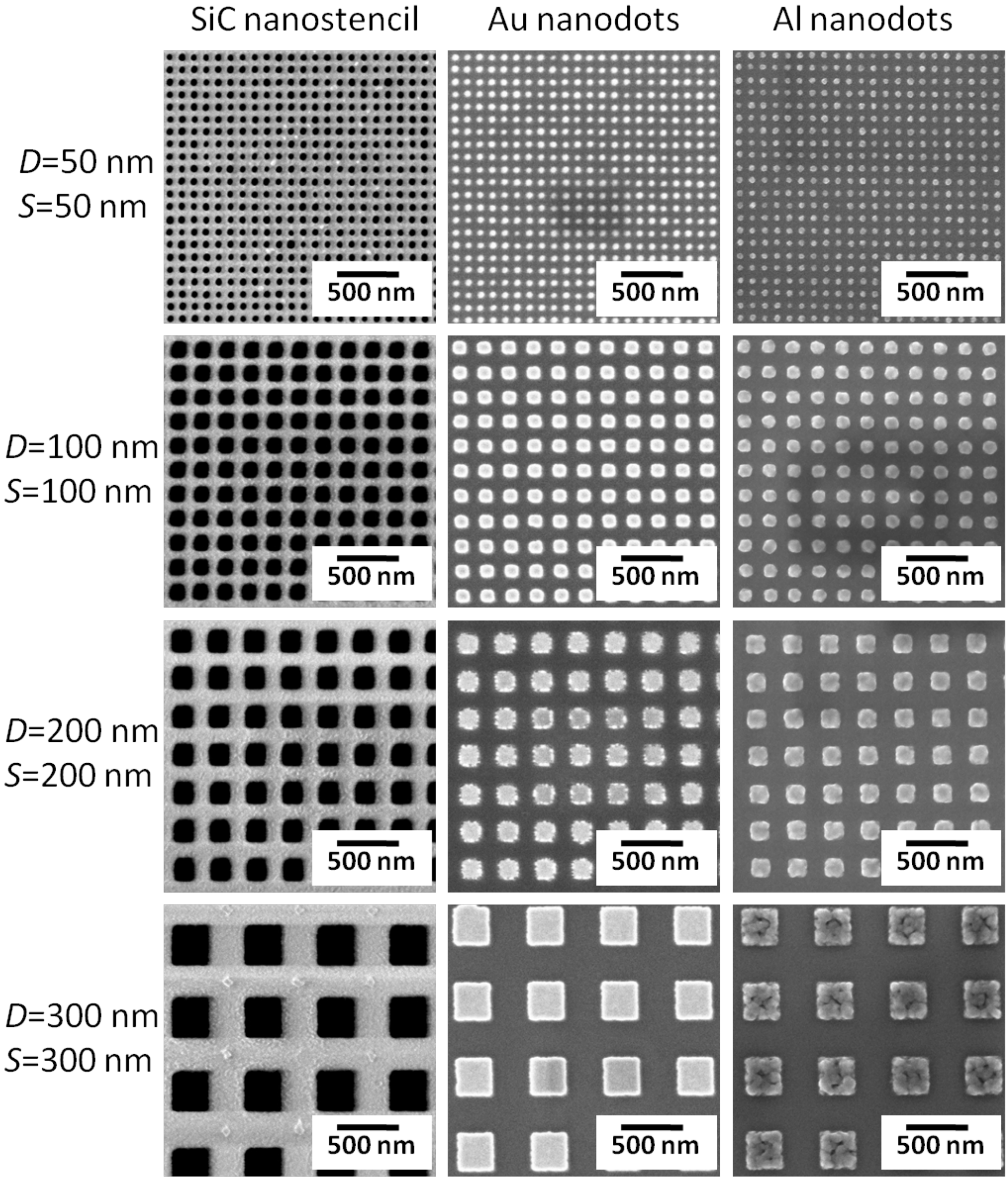


Figure 5.5: SiC nanoholes and their corresponding deposited nanodots with different size and spacing on silicon substrate. 45 nm of Au and 40 nm of Al were deposited. Nanodots down to ~ 50 nm were achieved by using SiC nanostencil.

5.4 Dry Etching through SiC Stencils

Another resistless patterning process by using stencil besides deposition is direct etching of structures on the substrate through the stencil. Here stencil acts as hard mask for etching. It's been shown that stencil as hard shadow mask can be used for direct machining of different materials (Si, poly-Si, LS-SiN, SiO_2 and polyimide) [105]. It is also possible to create high aspect ratio structures by etching through stencil [106]. As the conventional stencil membrane is made of LPCVD SiN, it is not possible to etch substrate materials such as Si, SiN or SiO_2 due to the low etching selectivity. Thus a metal hard mask for protecting the SiN membrane during the etching is necessary. In addition, the metal layer on the membrane improves the thermal conduction during etching, which prevents the failure of membrane from over heating.

The SiC is highly chemically inert, enables it to be a good mask for both dry and wet etching. The etching selectivity between SiC and Si, SiN or SiO_2 is much higher than which between SiN and these materials. Besides, SiC has higher thermal conductivity then SiN, enabling a better heat conduction. Based on the aforementioned advantages, SiC stencil was used as the etching mask without any metal coating. A 540 nm thick SiC stencilwas placed on 500 nm thick SiO_2 for the etching experiment, as illustrated in Figure 5.6a. No metal protection layer was coated on the membrane. 500 nm SiO_2 was completely etched away from the stencil aperture within 30 s by using C_4F_8/CH_4 plasma in AMS 200. The transferred patterns (Figure 5.6b) show a sub 100 nm loss in diameter for a 3.2 μm diameter aperture, as shown in Figure 5.6c and d. Close-up observation on the edge of aperture shows the enlargement of roughness which increases the size of aperture. This indicates that the selectivity between SiC and SiO_2 is not large enough for a long time protection of the SiC membrane in this aggressive etching process. The reusability of the stencil and repeatability of the experiment cannot be assured neither. Thus, in later etching experiments with even thinner membranes (200 nm) on SiC nanostencil, a metal layer was coated for improving the selectivity.

Two sets of experiments were performed by using Al-coated SiC nanostencil as dry etching mask to transfer nanoholes to Si substrate for the potential investigation in photonic crystal waveguides application [107, 108]. 40 nm Al was coated on the back side of 200 nm thick SiC nanostencil. Figure 5.7 illustrates the etching process. First set of experiments aimed at

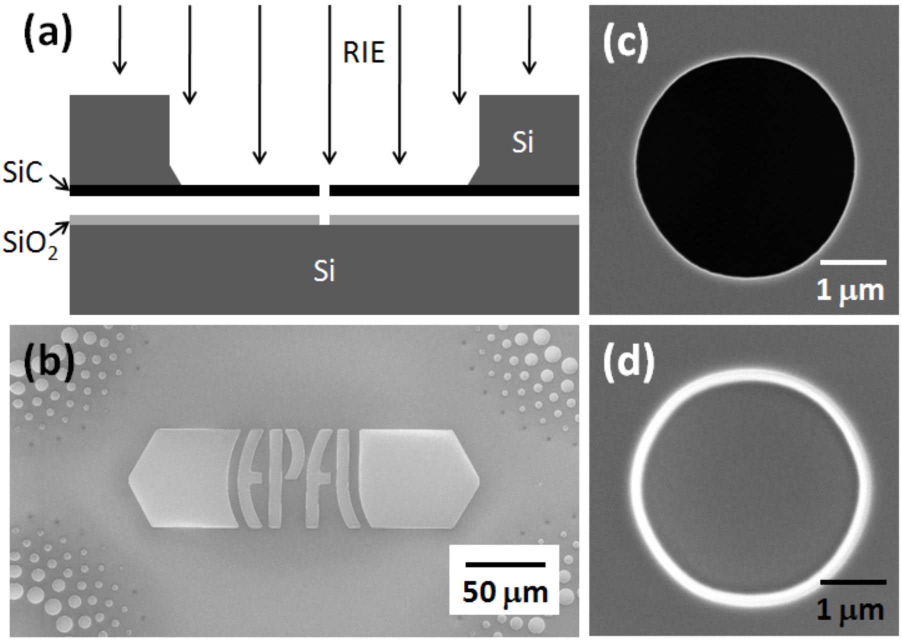


Figure 5.6: SiO_2etched through SiC stencil with no need for metal protection layer on the SiC membrane. (a) Schematic; (b) 500 nm deep etched patterns in SiO_2; (c) Aperture with 3.2 μm in diameter on SiC stencil and (d) the etched pattern on SiO_2 with 3.1 μm in diameter.

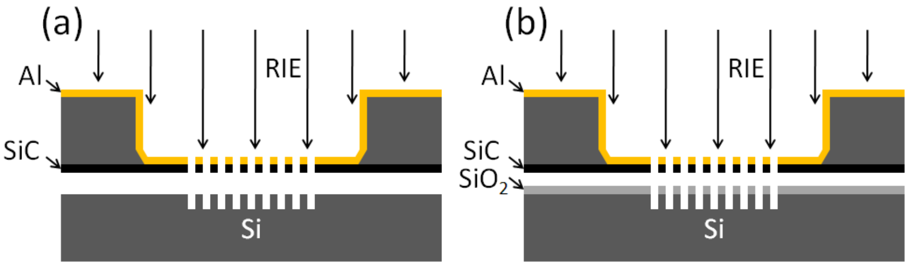


Figure 5.7: Schematics of dry etching through Al coated SiC nanostencil. (a) Direct etching Si substrate; (b) Direct etching SiO_2, then using it as a mask to etch Si.

transferring nanoholes by direct etching of a Si substrate (Figure 5.7a). An optimized etching recipe with SF_6 / C_4F_8 was found in our dry etching machine Alcatel 601E for the Si etch. After 30 s etching, ~ 500 nm deep Si was etched. Figure 5.8 shows the etching results. Due to the clogging of aperture from the 40 nm Al protection layer, nanoholes with 50 nm size on the SiC nanostencil were not visible thus no pattern was transferred. Nanoholes down to 75 nm were etched into the Si substrate. Compared to the original aperture size, a ~ 35% enlargement of the hole size on the substrate can be observed. The sizes of nanoholes on the Si substrate are 106 nm, 125 nm, 265 nm and 401 nm for D =75 nm, D =100 nm, D =200 nm and D =300 nm, respectively. The enlargement is due to the isotropic etching of this continuous Si etching process. It gradually produces the loss of dimension of the etched structures, thus slope on the sidewalls of the nanoholes are expected. We can see the formation of slope on the sidewalls on nanoholes ≥200 nm wide. Nanoholes <200 nm present nonregular hole shapes, which is also due to the isotropic etching. Rough surface between nanoholes is due to the damage from the etching plasma, which presents in the gap between the stencil and the substrate. The etching gases diffuse under the membrane and reacts with the substrate to cause rough surfaces. One solution is to reduce the gap. However, unless there is a physical barrier, it is very unlikely to have zero gap thus the lateral gas diffusion is inevitable.

In a second set of experiments, we applied another strategy by introducing an intermediate protection layer for the substrate, as shown in Figure 5.7b. A Si wafer with 50 nm grown SiO_2 was used as substrate, thus the oxide is used as protection layer to avoid unwanted effects (size enlargement and surface roughness). We first pattern the oxide layer through the nanoholes on stencil. The etched oxide layer is then used as a mask to transfer the pattern into Si. In the end the oxide will be removed by wet etching, thus the Si surface can be protected. Another advantage of having SiO_2 as the intermediate layer is because of its highly directional etching under plasma, which can accurately transfer the hole size without enlargement. Figure 5.9 shows the etching results. The nanoholes on SiO_2 were achieved by etching through an Al coated SiC nanostencil with C_4F_8 plasma in AMS 200. 50 nm oxide was removed after 15 s etching. Comparing with direct Si etching, SiO_2 presents accurate pattern transfer without size enlargement. The openings of the oxide are well defined, with sharp edges and corners until D =100 n. Actually in the case of D =75nm, the circular shape of the holes comes from the

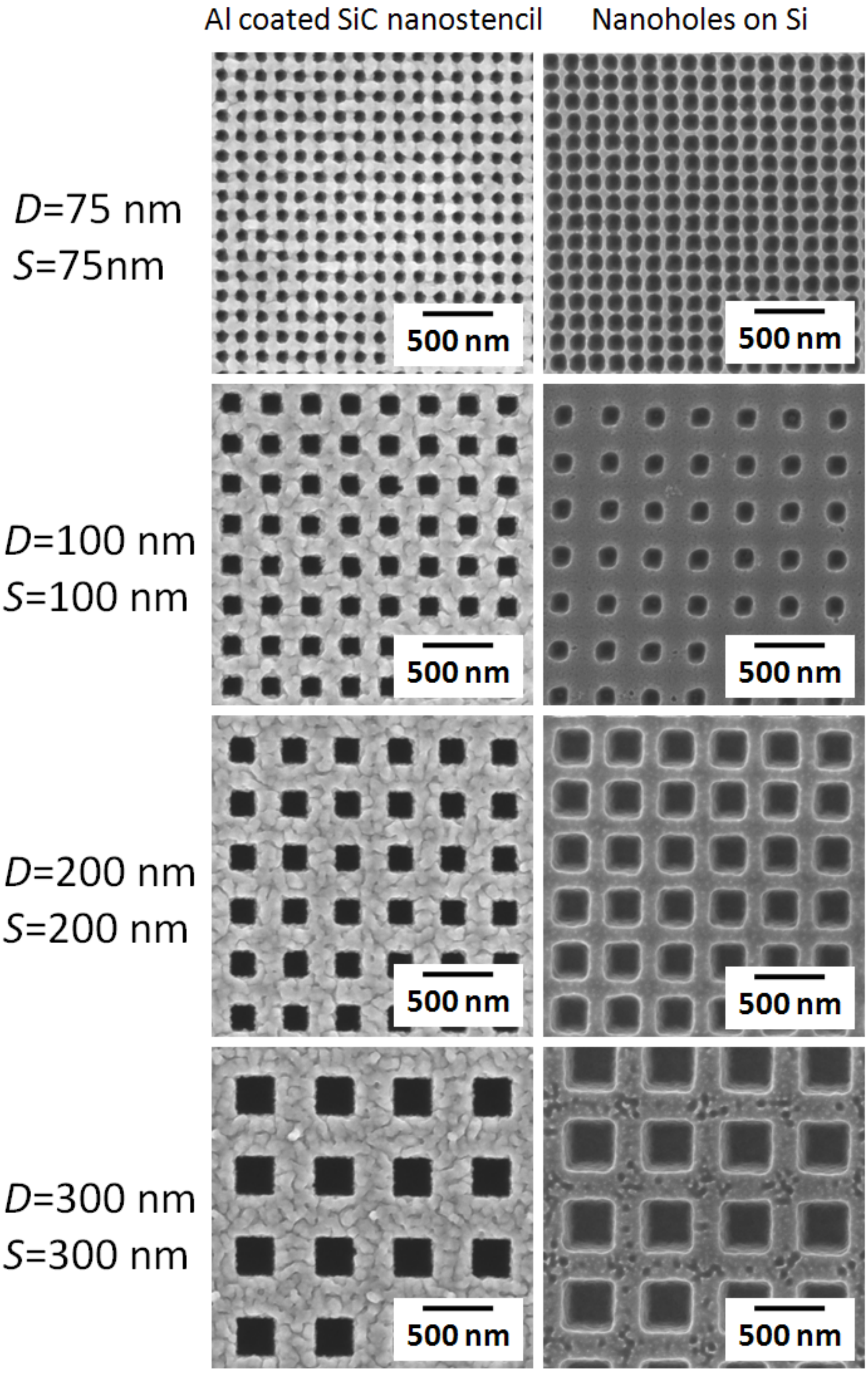


Figure 5.8: 40 nm Al coated SiC nanostencils and their corresponding transferred nanoholes with different size and spacing on silicon substrate. ~500 nm deep Si was etched. Comparing with original aperture size, ~ 35% enlargement of the hole size on the substrate can be observed thus decreases the spacing. Rough surface between nanoholes indicate the etching process is not anisotropic.

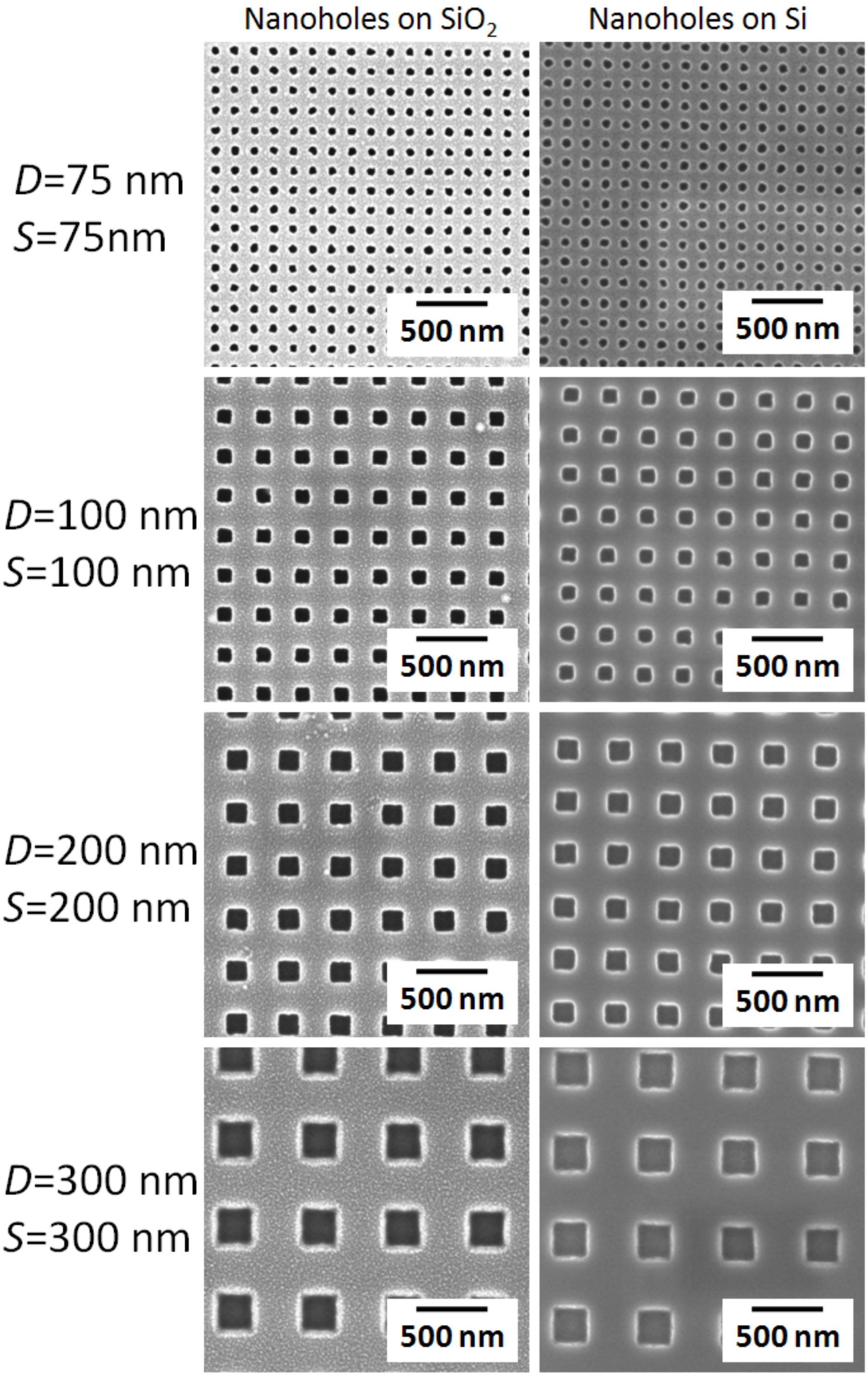


Figure 5.9: Nanoholes on SiO_2 and corresponding nanoholes on Si. The nanoholes on SiO_2 were achieved by etching through Al coated SiC nanostencil. The nanoholes on Si was etched by using the SiO_2 as etching mask. Oxide layer was then removed in BHF. A smooth surface on Si was obtained with no size enlargement of the square.

nanostencil, which again proves the accurate transfer of the hole shape. The surface roughness of the oxide is the same for different hole sizes, implying no damage to the oxide surface under the membrane. The following process is to etch Si by using the patterned oxide as mask, which will be later removed by wet etching in BHF (NH_4F 40%:HF 50% 7:1). The dry etching of Si was performed with SF_6/C_4F_8 plasma in AMS 200 and ~ 100 nm thick Si was etched away. SEM images of nanoholes on Si present accurate shape transfer from the oxide mask, which means an accurate transfer from the nanostencil. There is a slight size reduction between the stencil apertures and the final silicon nanoholes, which is ~3%. This can be improved by extending the etching time of the oxide layer. To conclude, due to the protection layer, there is no surface roughness from the aggressive etching process. In addition, smooth and vertical sidewalls can be achieved by this method.

5.5 Discussion

5.5.1 Resistance to Bending

In this section, we compare the different behaviors when stress material is deposited on SiC and SiN membrane. When cantilever-like structures are part of a stencil membrane, the deposition of high-stress materials through the stencil can induce a bending of the cantilevers. This causes a higher gap between stencil and substrate, which leads to undesired blurring. The robustness was compared between the low-stress (110 MPa) SiC and the low-stress (200 MPa) SiN by depositing 25 nm Cr film, which is a high tensile stress material. Figure 5.10 shows the different bending behaviors of cantilever structures in the membranes when coated with 25 nm Cr. The SiC cantilevers bend 75% less than the SiN ones by measuring the maximum deformation. This provides a wider choice for the deposited material, allowing less blurred pattern transfer for high-stress material. The higher robustness to deformation of the SiC membrane indicates the possibility of having in general a more accurate pattern duplication from the stencil to the substrate.

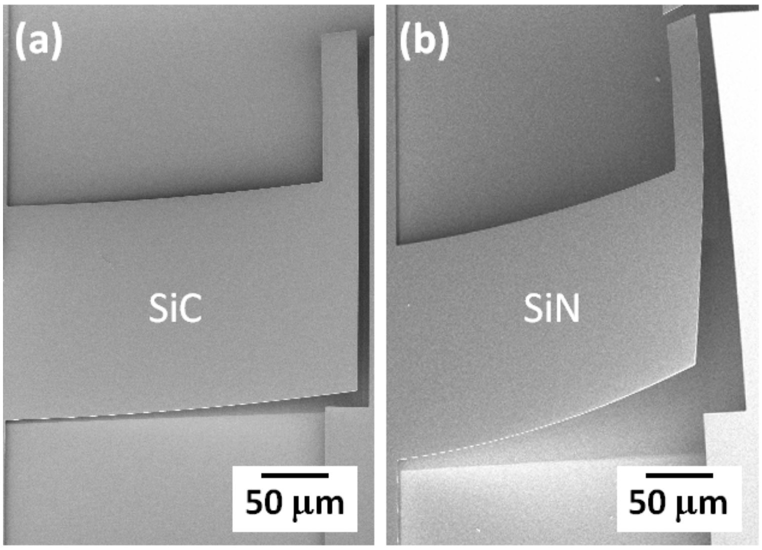


Figure 5.10: SEM images of cantilever structures on SiC and SiN stencil with different bending behaviors after 25 nm Cr deposition. (a) 540 nm thick low-stress SiC with 110 MPa intrinsic tensile stress; and (b) 500 nm thick low-stress SiN with 200 MPa intrinsic tensile stress.

5.5.2 Blurring

Contrast etching was performed on Al nanodots (40 nm thick) in order to analyze the blurring. It was found that the blurring size varies with respect to the location of the nanodots in the array. Further investigation reveals the localized downward deformation of the nanoholes array on the SiC membrane, as shown in the optical profiler image of Figure 5.11a. The localized deformation is due to the densely patterned area which lowers the mechanical strength of the membrane. Figure 5.11b plots the profile of cross section S-S'. The maximum downward deformation in the center of the array area is 1.1 μm, which locally reduces the gap. Nanoholes located in position A, B and C has different gaps, which is $G_A < G_B < G_C$. The difference in gaps translates into different blurring size around the nanodots as shown in Figure 5.11c-e. The blurring size of nanodots in location A is not measurable in the SEM image. In location B, due to a slightly larger gap, 28 nm of blurring can be observed. In location C where has an even larger gap, 45 nm of blurring can be seen. Though the bending due to the dense pattern is a side effect, it provides a locally reduced gap which improves the resolution. Thus, in principle, we can take advantage of this side effect to create locally minimized gap by optimizing the design.

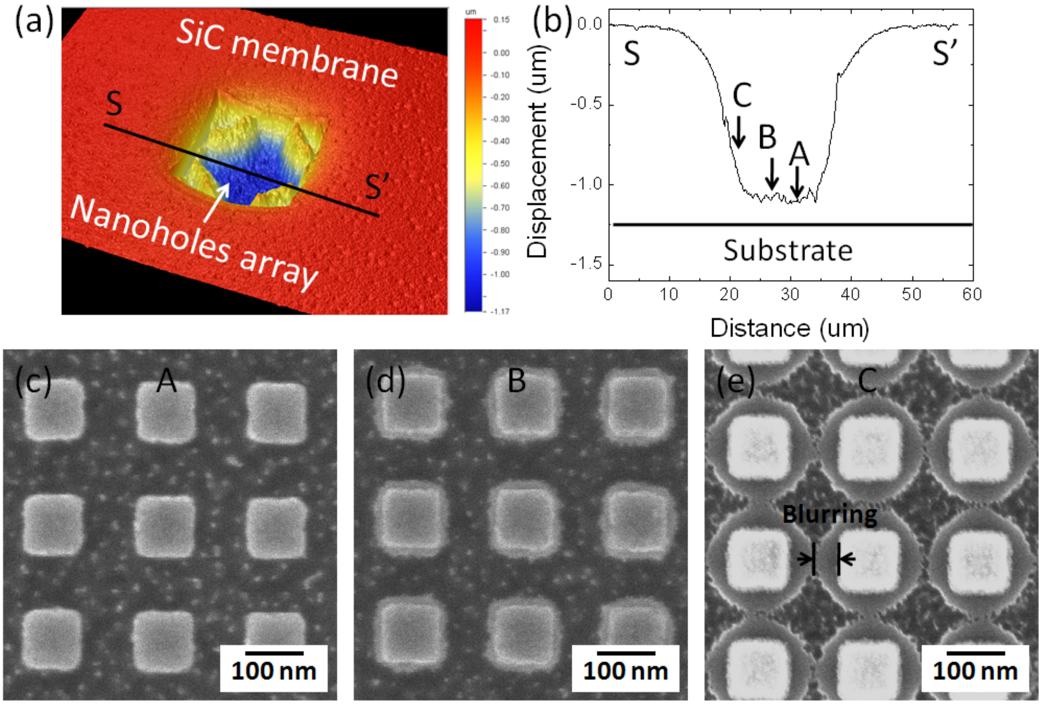


Figure 5.11: The blurring of Al nanodots on the substrate with respect to the localized gap. (a) Optical profiler image showing membrane deformation due to the densely patterned nanoholes array; (b) Profile of cross section S-S', the maximum downward deformation is 1.1 μm. Nanoholes located in position A, B and C has different gaps. $G_A < G_B < G_C$; (c-e) SEM images of corresponding nanodots on substrate. Contrast etching was performed in order to see the blurring. The blurring sizes are 0 (not measurable), 28 nm and 45 nm for position A, B and C, respectively.

5.6 Conclusions

We have successfully developed robust PECVD SiC stencils with both micro- and nano-apertures for stencil applications. Nanodots down to 50 nm wide have been achieved by deposition through the SiC nanostencil. The investigation of etching through stencil demonstrates that Al coated SiC nanostencil is capable of accurately transferring nanoholes array to the substrate down to 75 nm wide. With a thinner membrane and protection layer, it should be possible to push down to even smaller feature size. The SiC stencil demonstrated a better performance than that made of SiN in terms of robustness to deformation and resistance to etching. In conclusion, SiC stencils provide unique advantages for a wider range of SL applications. The PECVD SiC could be potentially used to replace the LPCVD SiN for the stencil membrane material in some critical conditions, such as high temperature, high stress material deposition.

In the next chapter, we will apply the nanostencil to make vertically-stacked gate-all-around polysilicon nanowire FETs. The nanostencil will be used to pattern high aspect ratio polysilicon gate around the vertically-stacked silicon nanowires, which cannot be achieved by conventional E-beam lithography due to the topography on the substrate.

6 Nanostencil for Polysilicon Nanowire FETs Application

6.1 Introduction

The conventional planar transistor design is facing considerable challenges following the ever higher circuit density predicted by Moore's Law. Thus novel materials, innovative device structures, as well as significant modifications of the planar transistor design are being studied in order to meet more demanding requirements [109]. Among all the novel device structures, the multiple-gated nanowire (NW) channel transistor with FinFET construction has been demonstrated to be one of the best in terms of electrostatic control, thus enabling further device scaling [110]. In fact, double-gated and FinFET structures are the first non-planar 3D gate constructions being successfully employed in commercial products by Intel. Currently, an increasing research effort is devoted to gate-all-around constructions with sub-10 nm diameter NW channels. Multiple NW channels are also being studied for enabling even higher driving current of the transistor [111, 112]. Compared to the horizontally-arranged multiple NWs, the vertically-stacked NWs provide a higher density footprint, which is more promising for scaling down [113, 114]. In addition, SiNW FETs can be used to build new logic architectures [115, 116]. Nevertheless, as the dimensions reduce and 3D structures are introduced, major fabrication difficulties arise due to the need of creating nano-features across high aspect ratio topography while keeping high fabrication yields.

One of the advantages of stencil lithography (SL) is the capability of resistless micro-/nano-patterning regardless of the material or topography of the substrate. This unique strength

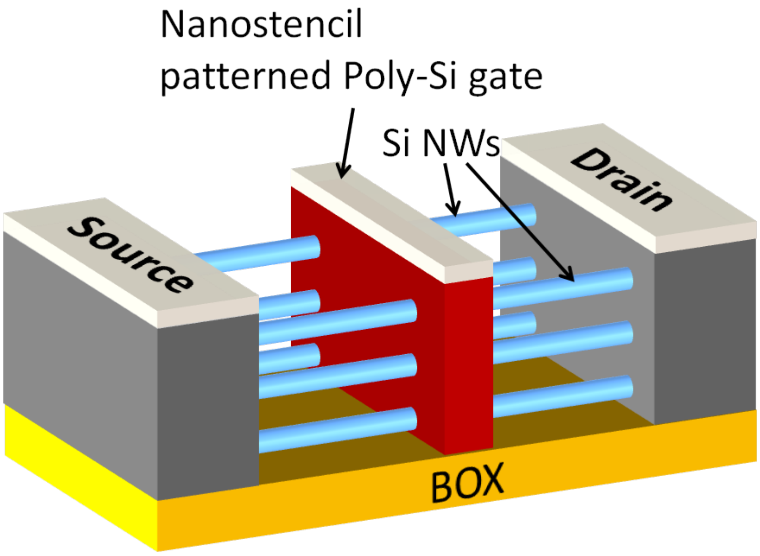


Figure 6.1: Schematics of the vertically-stacked gate-all-around Si nanowires (SiNWs) FETs with nanostencil patterned poly-Si gate.

provides the possibility to create micro-/nano-patterns on top of non-planar substrates with three dimensional (3D) features, especially when the aspect ratio of the substrate structure becomes a serious issue for conventional resist-based lithography techniques. In a previous work, SL has been demonstrated as a key fabrication step able to pattern micro size metallic gates on single Si NW transistor [117]. However, the channel length is limited by the width of stenciled gate and the yield is not satisfactory. In this chapter, we present the application of nanostencil lithography (nSL) in a fully CMOS-compatible top-down fabrication method for making vertically-stacked gate-all-around (GAA) Si nanowires (SiNWs) field effect transistors (FETs) with sub-μm gates [118], as schematically shown in *Figure* 6.1. The use of nanostencil allows us to create sub-μm polysilicon gates around the vertically-stacked Si nanowires, which is not trival for E-beam lithography to pattern nanoscale features having high aspect ratio (the spin-coated ebeam resist is not able to cover high steps). In addition, a high fabrication yield of ≥70 % is obtained with optimized mask design, which makes this method promising for achieving even higher density with good reproducibility and yield. This work was done in close collaboration with Davide Sacchetto from the Microelectronic Systems Laboratory in EPFL, Lausanne, Switzerland.

The content organization of this chapter is as follows. Section 6.2 will introduce the feasibility test on fabricating metallic gates and silicon gates by using SL. Based on the investigated process, the design and fabrication of the SiNW FETs will be presented in section 6.3. Characterization results will be seen in section 6.4, showing the functionality of the fabricated devices. At last, conclusion will be drawn in section 6.5.

6.2 Process Development

Early investigation of the process was focused on the feasibility study of fabricating both metallic and poly-Si nanogates by using SL. Metallic gate provides better electrostatic control on the channel than poly-Si gates. Thus, the priority was given to the investigation of stencil patterned metallic gates (both micro and nano) across the high aspect ratio Si NWs / nanofins. Due to clogging, the thickness of a metallic gate deposited through a stencil cannot be larger than the gate length. Thus for higher-stacks of released NWs, the width of the metal gate has to be at least the heigh of the stack. Later, we used therefore conformal poly-Si and used stencil to pattern the hard masks for defining the gates.

Metallic Gates

Initial exploration of defining metallic gates through stencil was performed with a microstencil aperture placed perpendicularly to the nanofins, as shown in the schematics of *Figure* 6.2. 200 nm thick Al was vertically deposited through the stencil opening onto the pre-fabricated high aspect ratio Si nanofins. *Figure* 6.2 shows the tilted SEM images of the deposited Al wire across the nanofins with different aspect ratios. In the case of nanofin with width W =100 nm and height H =200nm (aspect ratio 2:1), the height is the same as the deposited Al, which was expected to cover both side walls of the nanofin to form electrical connection through the Al on the top of the nanofin. However, we can observe a small gap between the Al on the top and on the bottom, which intercepts the current path through the Al wire. Later electrical measurement confirmed that there was no electrical connection along the Al wire. This separation is due to the accumulation of Al on the top of the nanofin during deposition, which creates a “mushroom” head. This “mushroom” acts as a shadow mask that prevents the vertical metal flux to reach the side wall of the nanofin. Higher aspect ratio nanofins with the same thickness of Al show a clearer separation (see *Figure* 6.2d). The aspect ratio here is 6:1. An obvious gap can be seen between the side wall and the bottom Al. Thus no electrical connection is achieved by using this method.

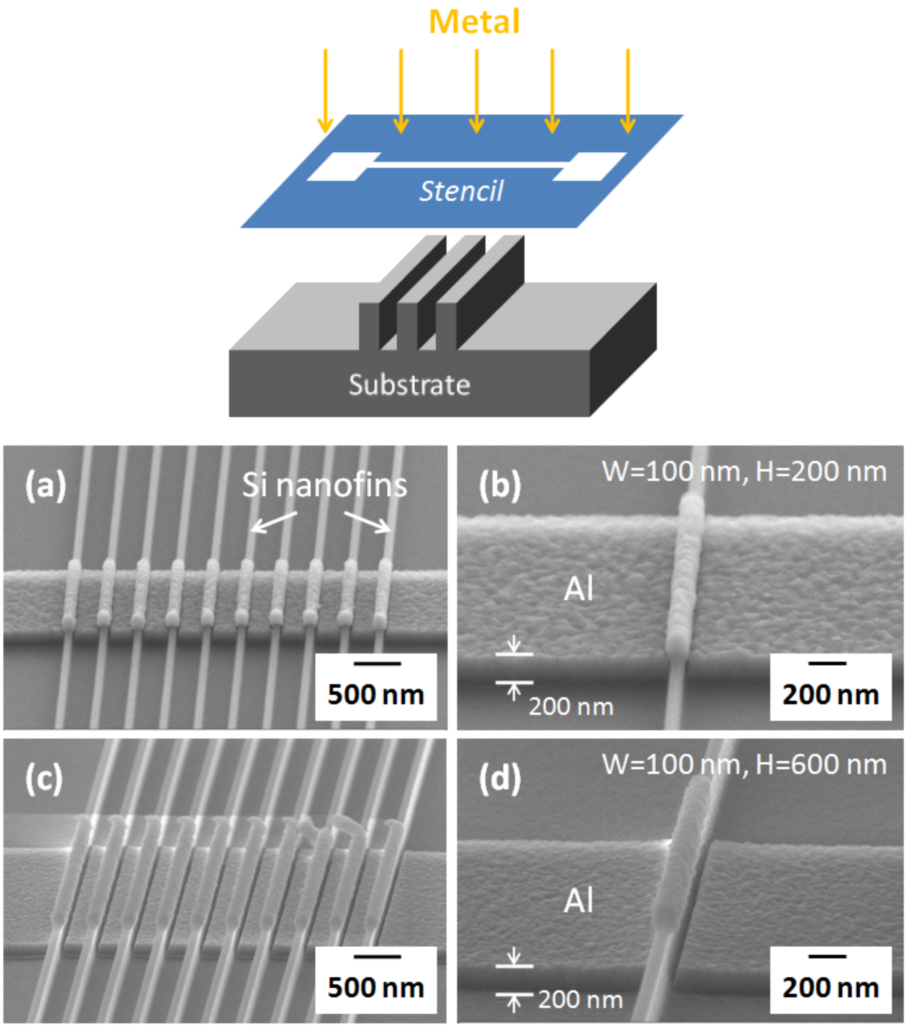


Figure 6.2: Vertical deposition of 200 nm Al through microstencil on top of high aspect ratio Si nanofins. (a) Si nanofins array and (b) single nanofin with width W =100 nm and height H =200nm. Aspect ratio is 2:1. (c) Si nanofins array and (d) single nanofin with width W =100 nm and height H =600nm. Aspect ratio is 6:1.

The ideal gate should conformally cover both side walls of the nanofin in order to create the best electrostatic control on the channel, which is not achievable by the vertical deposition. Thus we next emploied angle modulation of the incident metal flux in order to cover the side walls. Two-angle deposition was used with ±60° incident angle, as shown in *Figure* 6.3a. The Si nanofin has width W =40 nm and height H =200nm, thus the aspect ratio is

5:1. A nanostencil was used with 300 nm wide opening. SEM images show both side walls after 100 nm Al deposited each time with the titled angle. Therefore, in total 200 nm Al was deposited. Because of the misalignment between the two depositions, the deposited Al nanowire is much wider than the opening size. A clear shadow effect can be seen on both side of the nanofin due to the incident angle. The Al accumulated on the top of the nanofin is thinner than the total deposited thickness, which should also be related to the angle modulation. A very thin layer of Al can be observed on both side walls, indicating a potential electrical connection. However, electrical measurement shows a poor connection with very high resistance (~Mohm). This is probably due to the formation of native AlO between the first and second metal deposition. Thus, further improvement is needed by means of integrating angle modulation platform in the evaporator to eliminate the dielectric layer in between two metal layers in this approach. Another reason to have the automated modulation platform is to control the accuracy of the transferred metal nanowire, which in this experiment was affected by the misalignment between two deposition. The feasibility test of the metallic gate indicates that SL is applicable in making metallic micro/nanowires on top of high aspect ratio nanofins with further improvement needed in the angle modulation of the incident metal flux.

Poly-silicon Gates

As we encountered difficulties in defining metallic gate on high aspect ratio 3D substrate by SL, an alternative approach was found to define a poly-Si gate with conformal coverage on the side wall by using stencil. By taking the advantage of the conformal deposition of poly-Si, a nanostencil-defined metallic nanowire was used as the etching mask to create poly-Si gate on high aspect ratio nanofins/nanowires. Fabrication details will be introduced in section 6.3. To investigate the feasibility of this process, we first apply the nanostencil on flat Si substrate for the study of lateral dimension control. *Figure* 6.4 illustrates the process set up, showing Si nanofin made by nanostencil defined metallic etching mask and sequential Si etch. The lateral dimension of the metallic etching mask is determined by the halo, which is caused by the gap between stencil and the substrate. Since a full wafer nanostencil is needed in this experiment due to the requirement of alignment, the gap is larger and more uncontrollable than at chip level. In order to locally minimize the gap, we used magnetic tape and magnets. The magnetic tape was placed on the back side of the substrate and the magnets were put on

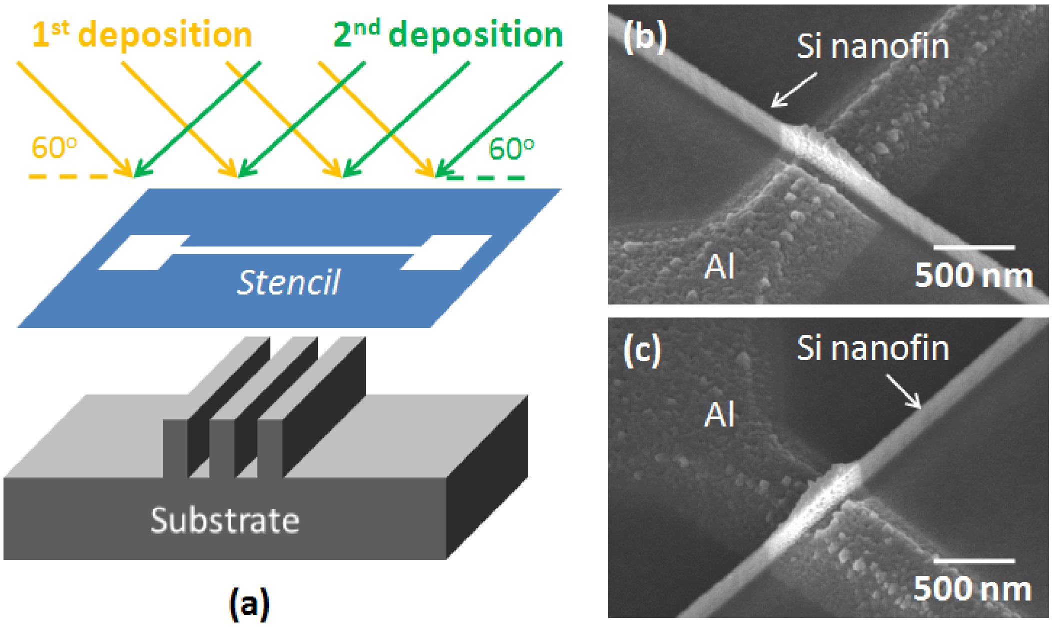


Figure 6.3: Two-angle deposition of 200 nm Al through nanostencil on top of high aspect ratio Si nanofin. (a) Schematics; (b) and (c) SEM images showing two sides of the Si nanofins after each side 100 nm Al deposited through a nanoslit on stencil. The nanofin has width W =40 nm and hight H =200nm. Aspect ratio is 5:1. The deposition angle is 60°.

top of the stencil. The generated magnetic force locally pulls the stencil membrane and the substrate closer for gap reduction. The reduced gap can remarkably decrease the halo, thus narrower gates can be achieved. This practical approach was also used in later fabrication of the poly-Si gated SiNW FETs.

Figure 6.5 shows the SEM images of the nanostencil patterned metallic etching masks after the anisotropic Si etching process. 100 nm Al was deposited and 200 nm deep Si was etched away. The nanostencil-defined metallic nanowires present obvious difference in lateral dimension between the results with and without magnets. The original aperture width is W_A. The patterned main structure is defined as gate width W_G. Halo is labeled in the image. Thus the total lateral dimension of the metallic etching mask is $W_G + 2 \times halo$. In the case with magnets, W_G is larger than W_A due to the blurring caused by geometric setup, for instance, when W_A= 50 nm, W_G= 114 nm. This difference becomes much bigger (W_A= 50 nm, W_G= 238 nm) in the case without magnets, which is related to the bigger gap. Comparing with the increment of W_G, the halo size is even more affected by the gap. For example, when W_A = 100 nm, halo size dramatically increases from 40 nm (with magnets) to 225 nm (without magnets).

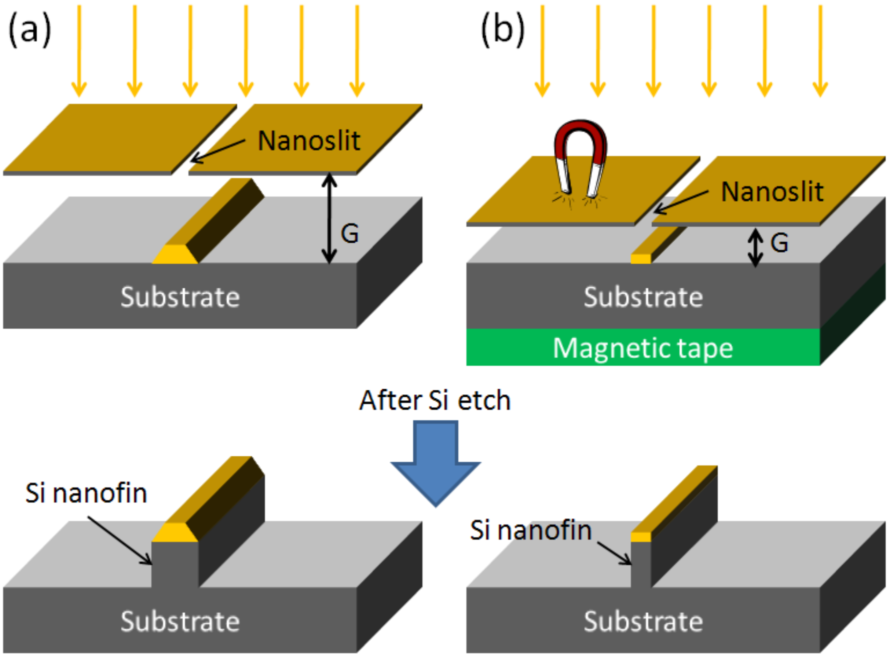


Figure 6.4: Schematics showing Si nanofin made by nanostencil defined metallic etching mask and sequential Si etch. (a) Gap induced blurring enlarges the width of the nanofin. (b) Gap reduction by introducing magnets in full wafer stenciling. A magnetic tape was placed on the back side of the substrate and magnets were put on the stencil.

It is also noticed that a smaller gap gives a better edge define on the main structure, which agrees with the observations from previous work [40].

Figure 6.6 plots the halo size as a function of gate width W_G. Without magnets, the halo is dramatically increased comparing with the case with magnets, which has a smaller gap. A linear relationship between halo and W_G can be seen from the graph in both cases, which indicates that both halo and W_G are related to the gap. Thus the reduction of gap plays a significantly role in creating narrower structures. *Figure* 6.7 shows the tilted view of the Si NW etched by using the nanostencil defined metallic NW mask. The nanoslit on the stencil has W_A= 100 nm. Again, without magnets, a much bigger halo was observed which enlarges the lateral dimension. The metallic NW etching mask present in the case without magnets presents a trapeziform cross section, which is due to the clogging of aperture during Al deposition.

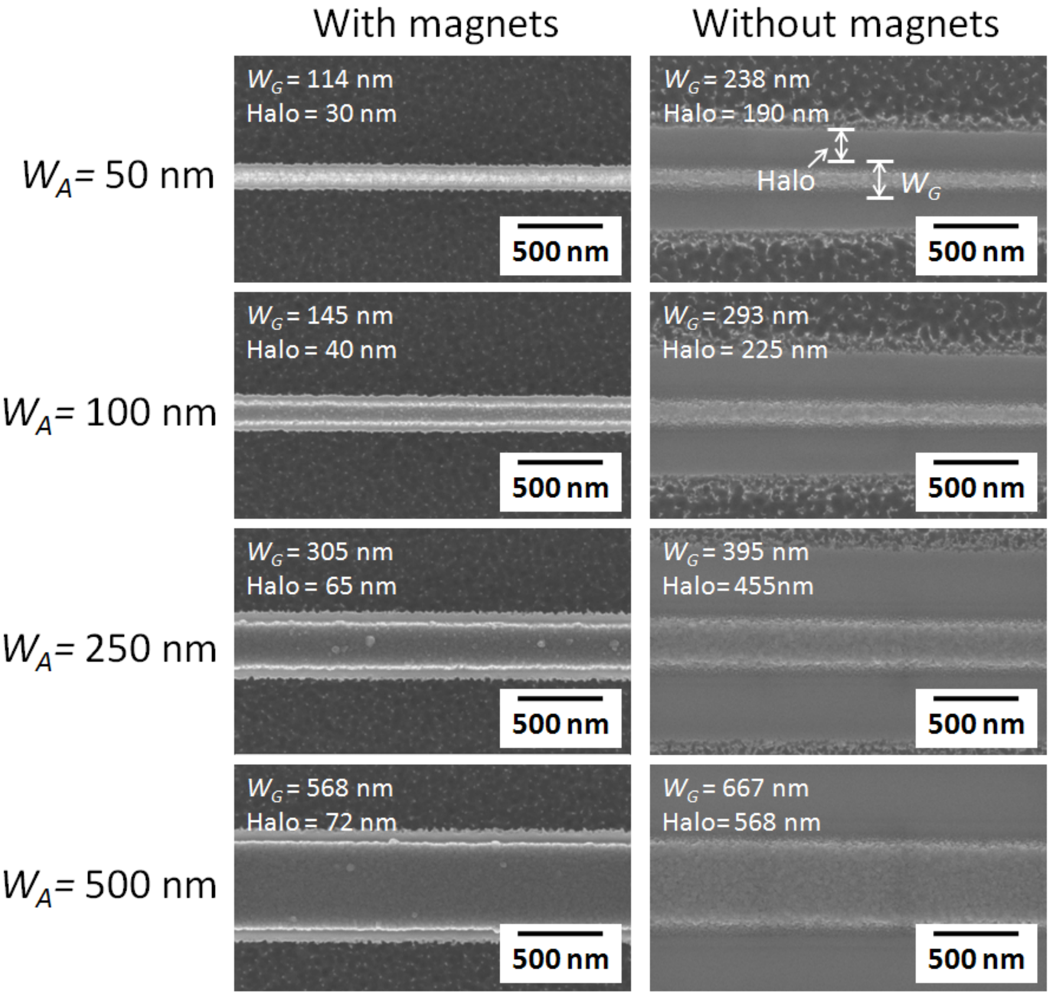


Figure 6.5: SEM images of the nanostencil patterned metal etching mask (with and without magnets configuration) after the anisotropic Si etching process. 200 nm deep Si was etched away. The original aperture width is W_A. The patterned main structure is defined as gate width W_G. Halo is labeled in the image.

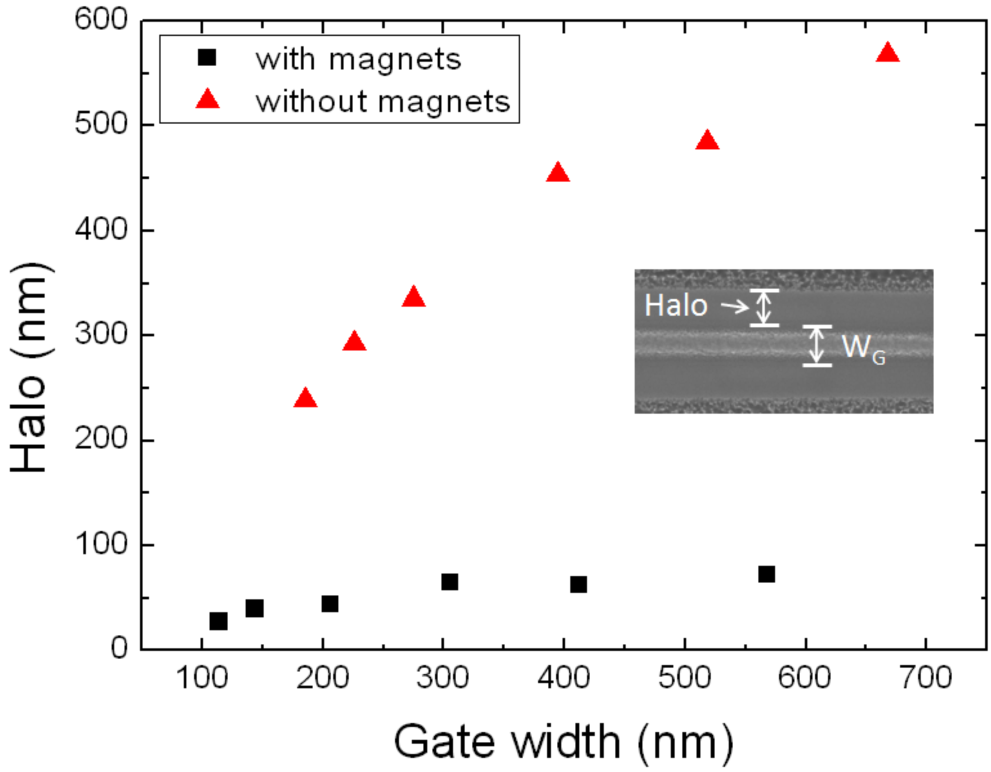


Figure 6.6: The halo size as a function of gate width. Without magnet, the halo is dramatically increased comparing with the case with magnet for reducing the gap.

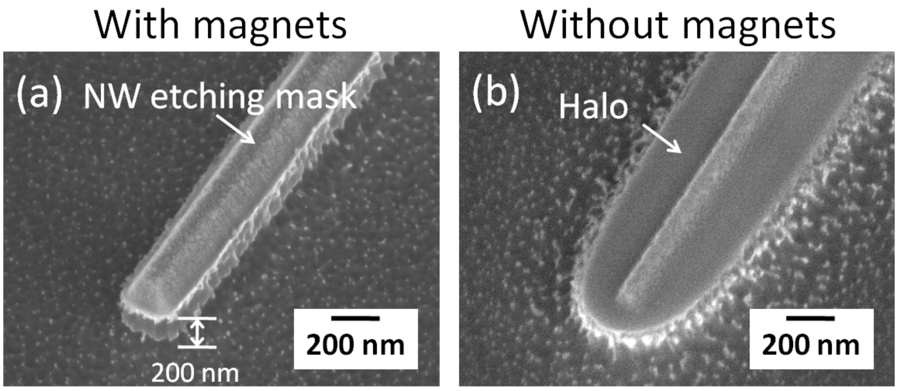


Figure 6.7: Tilted SEM images of the Si NW etched by using the nanostencil defined metallic NW mask. (a) With magnets, the etching mask is well defined with small halo size. (b) Without magnets, a big halo was observed which enlarges the lateral dimension. Both experiments used nanoslit with W_A= 100 nm. 100 nm Al was deposited and sequentially 200 nm Si was etched.

6.3 Design and Fabrication

After the process feasibility study, we integrated the optimal process of making poly-Si gates into the fabrication of SiNW FETs.

Design

The devices can be sorted into two categories: finFETs and vertically-stacked SiNW FETs. In the first case, FETs or inverters having either 1 to 11 fin channels and tri-gate construction are built. In the second case, FETs or inverters with 1 to 11 parallel strands consisting of 3 vertically-stacked SiNWs and GAA construction are built. Apart from the fabrication of non-planar channels in such devices, the lithography definition of tri-gate or all-around gate structures above 3D channel regions is considered to be a significant challenge.

Process Flow

The fabrication [118] starts with the substrate preparation for the two separate wafer batches. Bulk-Si wafers are oxidized in wet atmosphere to form 500 nm thermal oxide. Then either 50 nm or 350 nm thick LPCVD polysilicon is deposited as the device layer to build finFETs or vertically-stacked SiNW FETs, respectively. Individual or arrays of lines of widths of 50 nm and length of 8 μm are patterned with diluted hydrogen silsesquioxane (HSQ) using E-beam lithography (EBL) (see *Figure* 6.8a). The HSQ is then used as hard mask for the fins and the vertically-stacked SiNWs etching (*Figure* 6.8b). For the fin formation, a Cl_2 based plasma etching is used to obtain vertical sidewalls, whereas for the vertically-stacked SiNWs the etching consists of 3 cycles of passivation and etching steps, alternating low frequency pulses of C_4F_8 and SF_6 plasmas. The etching technique used for the stacked SiNW formation has been calibrated from the recipes previously described for the formation of vertically-stacked SiNWs in crystalline Si substrates [119]. Next, a 10 nm dry oxidation followed by a 100 nm LPCVD polysilicon deposition form the gate stack (see *Figure* 6.8c). The following step is to pattern the metallic etching mask by using a nanostencil made of 100 nm thick LPCVD SiN. The nano-apertures for gate and contact pads are defined by EBL, followed by consecutive etching steps to open the apertures and back side windows. Then the nanostencil mask is aligned with a dedicated optical alignment tool and mechanically clamped with the device substrates. After loading the substrates with the nanostencil into a commercial E-beam evaporator (LAB600), 40 nm Al are deposited, leaving an Al hard mask reproducing the gate design on top of the polysilicon layer (*Figure* 6.8d). The Al mask gives better selectivity than SiO_2 hard mask for dry Si etching, thus enabling the patterning of higher aspect ratio structure. Hence, polysilicon gates are etched and SiN spacers are formed to provide good isolation barrier between the gate and the source/drain regions (*Figure* 6.8e). This step is thus used to form pad areas for electrical characterization as well as polysilicon gates with lengths between 100 nm and 500 nm. Finally, a 30 nm thick Ni layer is deposited on the substrates, and a thermal annealing process at 400 °C is utilized to form a stoichiometric 1:1 NiSi phase on top of the gates and to metallized source/drain regions. The unreacted Ni that was lying either on top of SiO_2 BOX layer or onto the spacers has been removed with a selective Piranha solution. Thanks to the self-alignment of the SiN spacers with the gates, self-aligned source/drain regions are formed and the devices are ready for electrical characterization.

The fabricated devices included FETs or inverters designed with different number of channels, having either 1 to 11 parallel SiNWs for the finFETs. For the vertically-stacked SiNWs the same design is used, but due to stacking 3 levels, the same devices have 3 to 33 parallel SiNW channels. Another difference between finFETs and vertically-stacked FETs is notably the gate structure, which are tri-gates and GAA, respectively. In *Figure* 6.9a, a finFET with 11 parallel SiNWs and tri-gate construction is shown. The SiNWs are interconnected every 500 nm in order to improve the mechanical stiffness and avoid bending. In *Figure* 6.9b, a vertically-stacked FET with 3 stacked SiNWs of 30 nm diameter and GAA construction is shown. In the inset, conformal coverage of 10 nm thick SiO_2 dielectric and LPCVD polysilicon gate is shown.

6.4 Characterization

Electrical characterization was carried out by Davide Sacchetto with a manual probe station connected to a Agilent B1500 semiconductor parameter analyzer. Tungsten tips are put in contact with the polysilicon source/drain pads and on the Al/polysilicon gate pad. Typical I_{ds}-V_{gs} curves are first measured for finFETs which show large inverse subthreshold slopes of about 1500 mV/dec and average I_{ON}-I_{OFF} ratio of 3 orders of magnitude. These results are then

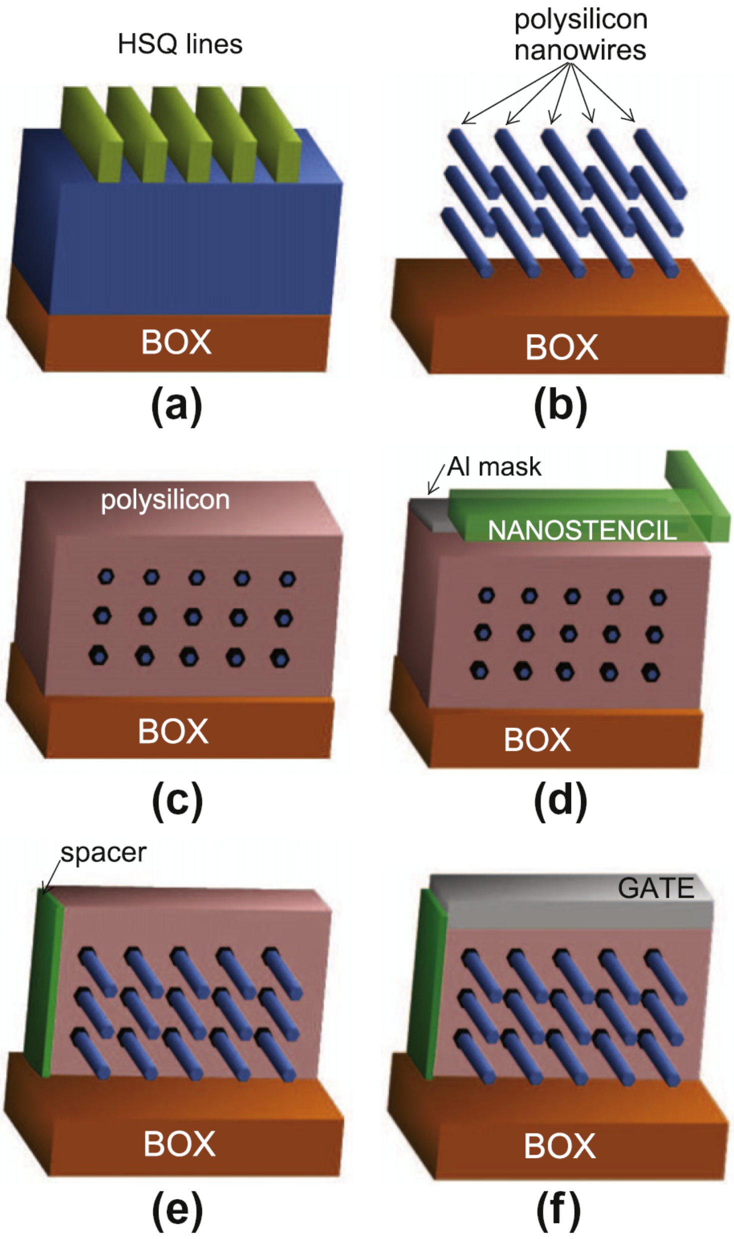


Figure 6.8: Fabrication flow of the vertically-stacked GAA FETs. (a) HSQ lines are patterned with EBL. (b) A DRIE etching process is tuned to form 3 levels of stacked SiNWs. The nanowires are attached to polysilicon pillars at their extremes (not shown). (c) 10 nm dry oxide and 100 nm LPCVD polysilicon are deposited to form the gate stack. (d) A nanostencil mask is aligned and mechanically clamped with the substrate, serving as evaporation mask for Al deposition. The Al is then used as mask to pattern the gate.(e) After gate patterning a SiN spacer is formed on vertical sidewalls. (f) After Ni blanket deposition and a thermal annealing at 400 °C, a Piranha wet etching is used to remove unreacted Ni from either BOX and spacer regions, thus forming self-aligned NiSi source/drain and gate areas.

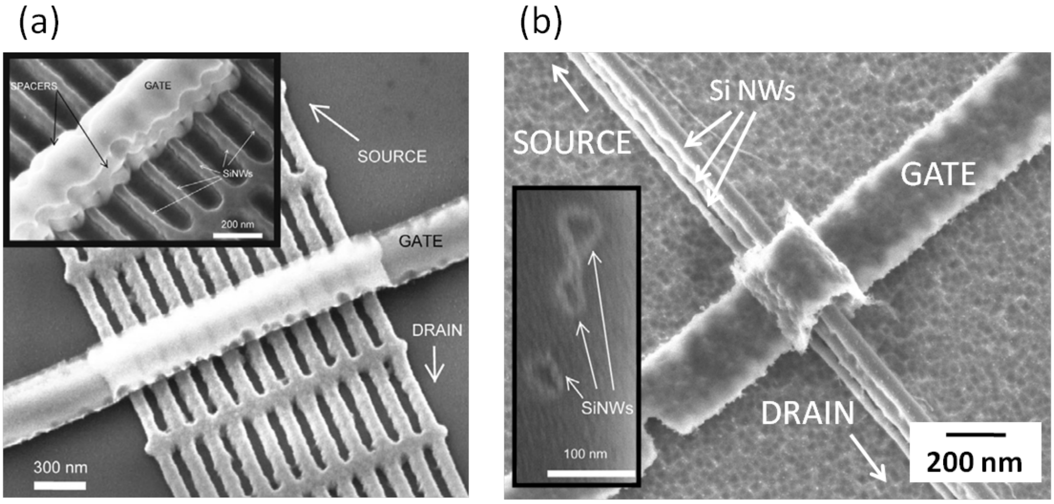


Figure 6.9: SiNW FET with nanostencil patterned gate. (a) FinFET with 11 channels with 50 nm×50 nm channel cross section, 350 nm wide polysilicon gate. The nanowires are connected at regular intervals of 500 nm in order to improve the stiffness of the structure. In the inset a magnified and tilted SEM view shows the nitride spacers and the SiNWs around the gate structure. (b) Vertically-stacked FET with 3 stacked SiNWs of 30 nm diameter channels. In the inset, a Focused Ion Beam (FIB) cross-section of the gate shows 3 SiNWs surrounded by 10 nm SiO_2 dielectric and 100 nm LPCVD polysilicon. Gate width is 350 nm.

compared with the electrical performance measured for the vertically-stacked GAA NW FETs. The I_{ds}-V_{gs}curves (*Figure* 6.10a) for the vertically- stacked FETs with 3 stacked SiNWs show typical device ambipolarity with inverse subthreshold slopes for n- and p-branches up to 300 mV/dec and up to 1300 mV/dec, respectively. Notice the strong dependence of the p-branch with applied V_{ds}. This undesired behavior is largely compensated for, in the devices with 3 times 11 parallel fingers, as shown in *Figure* 6.10b. The apparent robustness with respect to short channel effects is attributed to the different geometry of the 3D mesh with respect to the single stranded stacked SiNWs. The electrical measurement shows that yield of functional devices on one wafer is more than 70%.

Inverter and logic NAND operation have also been performed using a current biasing scheme. In *Figure* 6.11, a current bias from 5 pA to 15 pA in 5 pA steps has been utilized. As shown in the graph, the inversion voltage saturates at $V_{in} \approx 1.2V$ with a gain $\triangle V_{out}/\triangle V_{in} \approx 14$. Moreover, by using two vertically-stacked FETs in series connection, NAND functionality can be achieved by measuring the voltage drop across while sweeping the gate voltages of the two devices. With this method, typical NAND functionality is obtained, as shown in *Figure* 6.12.

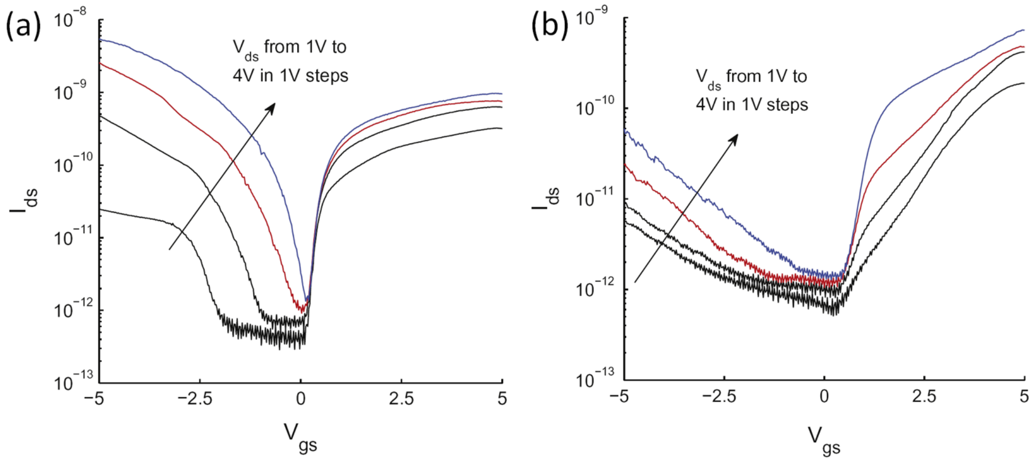


Figure 6.10: (a) I_{ds}-V_{gs} curve for vertically-stacked SiNW GAA FET with 3 stacked channels. Measured minimum inverse subthreshold slopes for electrons (n-branch) and holes (p-branch) are 300 mV/dec and 1300 mV/dec at V_{ds}= 4 V. (b) I_{ds}-V_{gs} curve for vertically-stacked SiNW GAA FET with 3 times 11 channels. Measured minimum inverse subthreshold slope for electrons is 350 mV/dec. Notice that the holes conduction is effectively suppressed due to the 3D nanowire mesh.

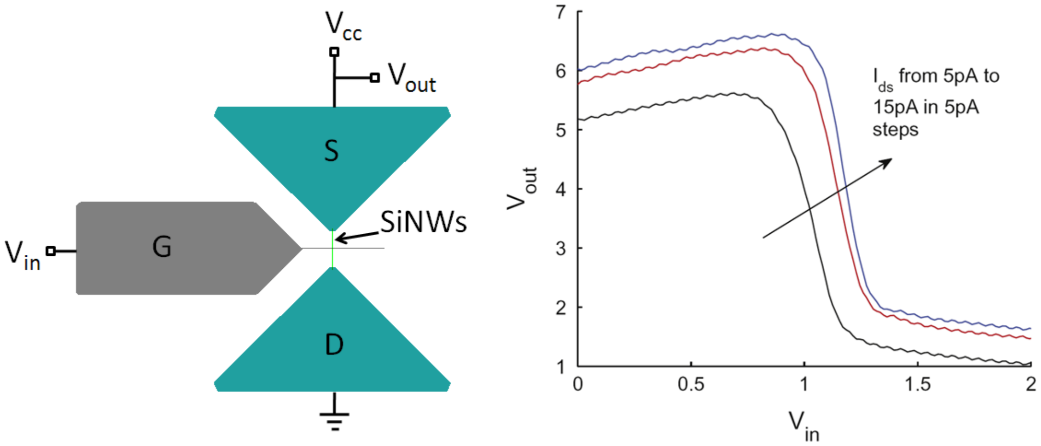
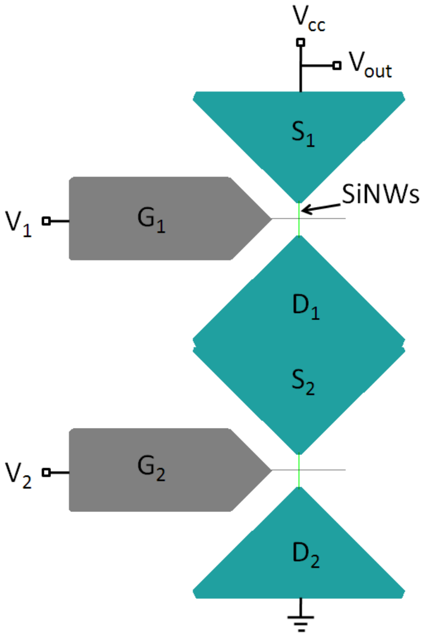


Figure 6.11: Inverter operation obtained by biasing a FET with constant current. The V_{in}-V_{out} characteristics switched from high to low V_{out} at V_{in}=1 V.



V_1 [V]	V_2 [V]	V_{out} [V]
0 (logic 0)	0 (logic 0)	≈4 (logic 1)
0 (logic 0)	2 (logic 1)	≈3 (logic 1)
2 (logic 1)	0 (logic 0)	≈5 (logic 1)
2 (logic 1)	2 (logic 1)	≈0.5 (logic 0)

Figure 6.12: Typical NAND functionality obtained by using two vertically-stacked FETs in series connection.

6.5 Conclusions

In conclusion, we demonstrated for the first time vertically-stacked Si nanowire FETs with polysilicon GAA having gate width down to 100 nm and yield larger than 70%. The reported ambipolar behavior for vertically-stacked FETs achieves I_{ON}-I_{OFF} ratio up to 4 orders of magnitude and inverse subthreshold slopes (SS) up to 300 mV/dec. The method provides excellent step coverage on either finFETs and vertically-stacked SiNW FETs with strongly non-planar topography, thanks to the use of an Al etch mask deposited through nanostencil. The electrical behavior confirms the results obtained from similar devices fabricated with a standard lithography while achieving higher density, larger reproducibility and yield, maintaining the performance improvement related with scaling. Finally, functional inverter and logic NAND operations are obtained, confirming the developed fabrication flow as a valuable tool for building logic circuits in 3D.

7 Summary, Conclusions and Outlook

7.1 Summary of the Results

This section summarizes the chief results achieved in the thesis. The presented achievements (No.1 to No. 6) focus on the development of heated stencil. No. 7 and No. 8 summarize the exploration of PECVD SiC stencils and the application of nanostenciling to 3D SiNW transistors, respectively.

1. The critical material incident rate under certain temperature is theoretically calculated for five different metals (Al, Cr, Ti, Au and Pt). The process window for the practical incident rate vs. membrane temperature is plotted (*Figure* 2.7), which is a very useful reference in the use of heated stencil.

2. The heated stencil is developed and fabricated. Temperature distribution of the heated membrane is systematically studied by comparing the results from simulation and IR measurements. The temperature profile provides reference values for each stencil window which can be correlated to the effectiveness of preventing aperture clogging.

3. Metals pre-deposited on the heated membranes have been heated in both ambient conditions and in vacuum. Pre-deposited Al oxidizes due to the high temperature, while reevaporation of 2 um pre-deposited Au is observed after 10 minutes at 700 °C in vacuum.

4. Heating the stencil during metal evaporation prevents aperture clogging. Comparison between the heated and non-heated stencil reveals the significant improvement of the heated membrane on preventing aperture clogging.

5. Local gap reduction between stencil and substrate is achieved by thermally actuating the heated stencil, with an optimized heater design. Heat transfer from the stencil through the gap to the substrate is studied by simulation, showing that the increase of the substrate temperature does not affect the condensation of the material on the substrate. Dynamic gap control by monitoring the variation of the applied current has also been demonstrated.

6. Heated stencil is used in three operation modes of stencil lithography. Improved pattern resolution and extended stencil life time have been achieved. The effective life time of the heated stencil is significantly prolonged by introducing a second shadow mask, which contributes to maintaining the correct temperature profile on the heated stencil during deposition of thermally-conductive materials.

7. Novel stencils made of robust PECVD SiC membrane have been exploited. Both micro and nano SiC stencils are successfully fabricated and demonstrated their excellent performance in two stencil lithography processes: metallization and etching.

8. Nanostencils are used to pattern functional sub-μm gates across vertically stacked Si nanowire FETs is achieved. Gate width down to 100 nm across high aspect ratio Si nanowires/nanofins is successfully demonstrated. Electrical characterization shows the functionality of the devices. The potential of further miniaturization of the 3D nanowire transistors by using SL is proved.

7.2 Conclusions

The achieved results of this work present a significant advancement for stencil lithography in terms of the improvement for pattern resolution, the extension of stencil life time, the exploration of new stencil membrane material and the application of SL in nanowire transistors. The contributions of this thesis to SL include: a novel stencil concept using heated membrane as a universal solution to three major technical challenges of SL; the exploration of PECVD

SiC as alternative stencil membrane material for applications in critical conditions; and the application of nanostencilling in high aspect ratio nanowire transistors.

The developed heated stencil has shown the capability of being a universal solution to three major technical challenges of SL: *clogging*, *gap* and *blurring*. The membrane can be heated up during material deposition to prevent clogging of the aperture by minimizing the material condensation on the stencil membrane. The inherent gap can be locally reduced by thermal actuation of the membrane towards the substrate, which results in the decreasing of the blurring size. The heated stencil is successfully demonstrated in all three stencil operation modes: static, quasidynamic and dynamic modes. The presented results show significant improvement of preventing aperture clogging, advance of pattern resolution and prolongation of stencil life time comparing with conventional stencil lithography. This development is important for dynamic SL as it enables the possibility of unlimited “writing” through the moving aperture in high resolution.

PECVD SiC stencils with both micro and nanoapertures for stencil application has been demonstrated. Nanodots down to 50 nm wide have been achieved by deposition through SiC nanostencil. The investigation of etching through stencil demonstrates that Al coated SiC nanostencil is capable of accurately transferring nanoholes (down to 75 nm) array to Si and SiO_2 substrates. The SiC stencil shows a better performance than that made of SiN in terms of robustness to deformation and resistance to etching, which provides SiC stencil more advantages for a wider range of SL applications. The PECVD SiC could be potentially used to replace the LPCVD SiN for the stencil membrane material in some critical conditions, such as high temperature, high stress material deposition.

By taking the unique advantage of SL in nanopatterning on high aspect ratio topography, it is first time demonstrated the vertically-stacked Si nanowire FETs with polysilicon gate-all-around having gate width down to 100 nm and yield larger than 70%. The developed process using nanostenciled Al etching mask provides excellent step coverage on either finFETs or vertically-stacked Si nanowire FETs with strongly non-planar topography. The electrical measurement confirms the functionality of the devices, indicating that this process can potentially enable higher density, larger reproducibility and yield while maintain the performance improvement related with scaling. Functional inverter and logic NAND are also demonstrated.

In conclusion, the heated stencil as universal solution to the major technical challenges of SL, the exploration of PECVD SiC as alternative stencil membrane material, and the application of nanostenciling in fabricating nanowire transistors have been presented. Looking back to the initial motivation and objectives for this thesis, the outcome of this work meets the expectation and also provides a new path for resistless nanopatterning.

7.3 Outlook

The results of this thesis also bring new challenges and point out the direction for further development. As the temperature on the heated stencil determines the allowed incident rate of the material flux, it is important to achieve a temperature as high as possible in order to enlarge the practical process window, which is especially critical for dynamic SL. The Pt-based heated stencil developed in this work can stably work up to 800 °C, which would allow unclogging at higher incident rate. Further development of the heated stencil should focus on using other heating elements and new heater design to obtain higher temperature (>1000 °C). Tungsten could be a candidate due to its higher melting point, but proper passivation should be developed in order to prevent its oxidation at high temperature. Doped SiC could be another interesting candidate by taking advantage of both mechanical and electrical properties. The stability of the heated stencil for extended operation time has to be improved. Current devices are limited by several degradation factors, such as electro-migration. Changing from DC to AC voltage should decrease this phenomenon, leading to a better stability. However more investigations are needed as the applied AC voltage should avoid making the heated membrane vibrate under the resonant frequency, which could decreases the pattern resolution by modulating the gap. The deformation of the membrane is directly related to its temperature. The variation of the membrane temperature is currently controlled manually within 50 °C. The development of an automatic loop for adjusting the applied power based on the variation of the monitored temperature could improve the precision of the gap control. The successful development of the heated stencil opens new paths for nanopatterning in many applications, which has to be explored in the future. Fabrication of PECVD SiC stencil shows a relatively low yield compared to SiN stencils, probably due to the remaining pinholes in the SiC membrane. The yeild could be higher by using pinhole-free PECVD SiC thin film.

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A Appendix

A: Condensation Rate vs. Incident Rate

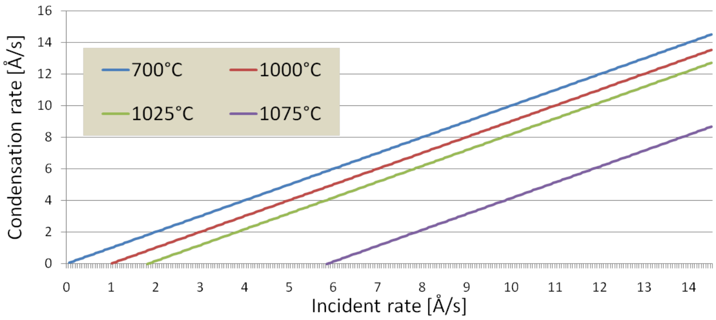

Figure A.1: Chromium (Cr) condensation rate as a function of incident rate for four temperatures: 700 °C, 1000 °C, 1025 °C and 1075 °C. The critical incident rates under these temperatures are 4E-5 Å/s, 1 Å/s, 1.8 Å/s and 5.8 Å/s, respectively.

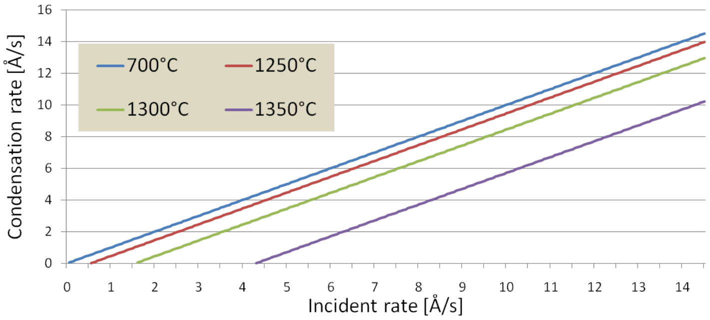

Figure A.2: Titanium (Ti) condensation rate as a function of incident rate for four temperatures: 700 °C, 1250 °C, 1300 °C and 1350 °C. The critical incident rates under these temperatures are 2E-9 Å/s, 0.55 Å/s, 1.6 Å/s and 4.3 Å/s, respectively.

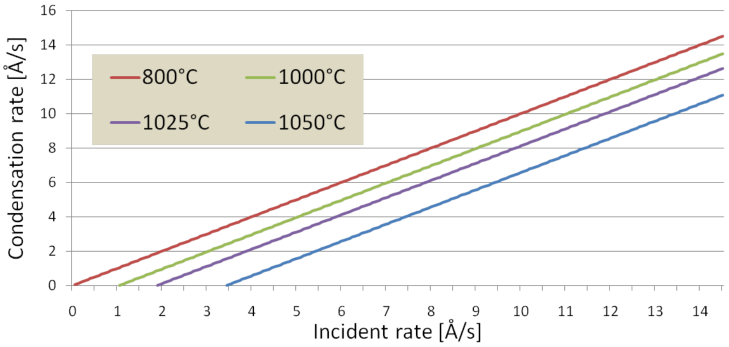

Figure A.3: Gold (Au) condensation rate as a function of incident rate for four temperatures: 800 °C, 1000 °C, 1025 °C and 1050 °C. The critical incident rates under these temperatures are 2.4E-3 Å/s, 1 Å/s, 1.9 Å/s and 3.4 Å/s, respectively.

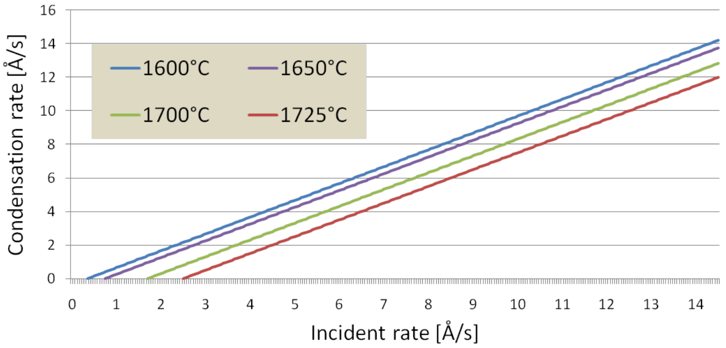

Figure A.4: Platinum (Pt) condensation rate as a function of incident rate for four temperatures: 1600 °C, 1650 °C, 1700 °C and 1725 °C. The critical incident rates under these temperatures are 0.4 Å/s, 0.7 Å/s, 1.6 Å/s and 2.5 Å/s, respectively.

B: 12 Heater Designs for Heated Stencils

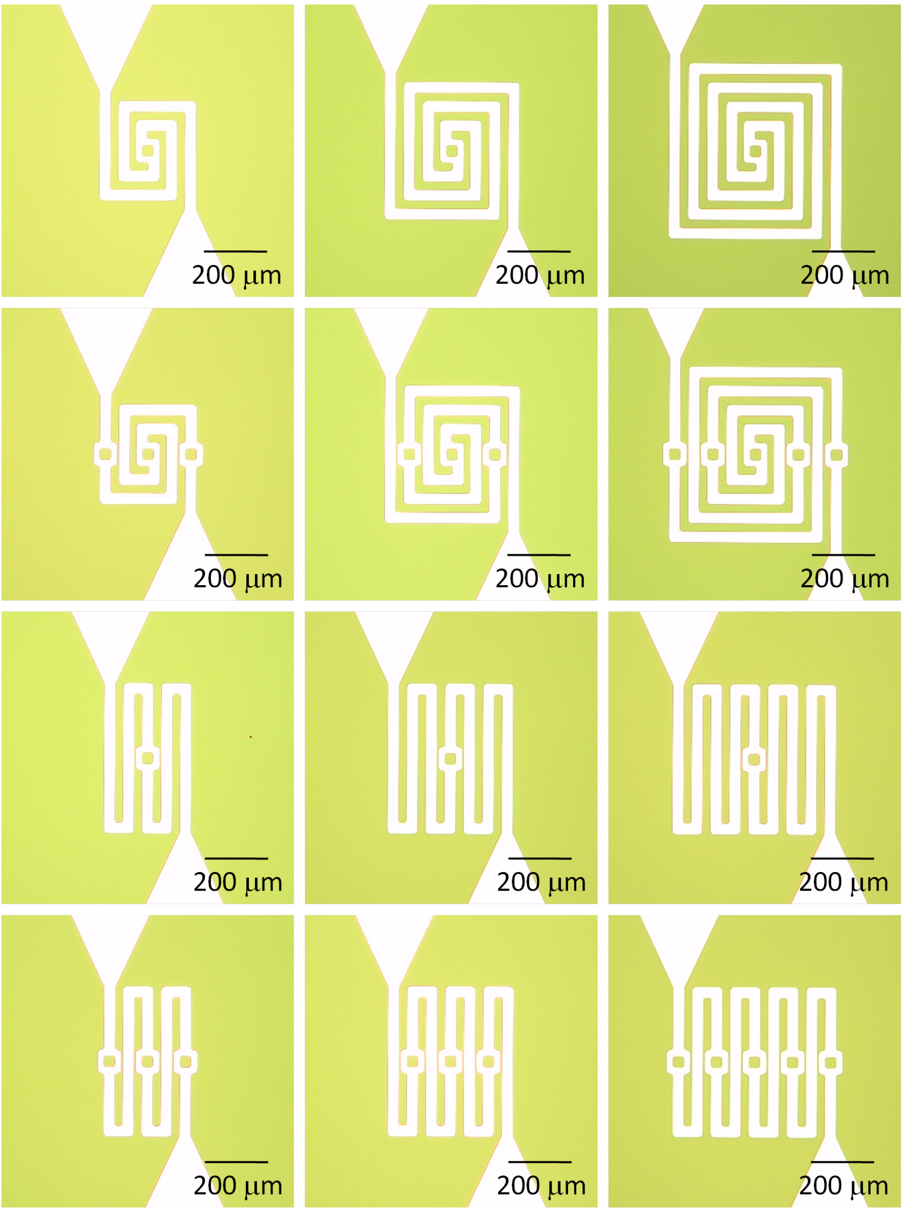

Figure A.5: 12 heater designs in coil and meander shapes with different numbers of loops.

B Curriculum Vitae

• Personal data

Name: Shenqi Xie
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• Education

2009 ~ 2013	PhD thesis in Microsystems laboratory (LMIS1), EPFL, Switzerland
2005 ~ 2008	Master of Science in Microelectronics, Dept. of Microelectronics Fudan University, Shanghai, P.R.China
2001 ~ 2005	Bachelor of Science in Microelectronics, Dept. of Microelectronics Fudan University, Shanghai, P.R.China

• Professional experience

2009 ~ 2013	Reaserch and techaing assistant in Microsystems laboratory (LMIS1) EPFL, Switzerland
2008 ~ 2009	Product development engineer, Intel Shanghai Product Ltd.

2005 ~ 2008	Reaserch assistant on “ Fabrication of large scale and high density gratings based on nanoimprint lithography”, Dept. of Microelectronics Fudan University, Shanghai, P.R.China

• Honors & Awards

2011	Chinese government award for outstanding self-financed students abroad
2008	First-class graduate of Shanghai city, China
2007	Qimonda Technologies (XIAN) Co., Ltd Scholarship
2007	First prize of Graduate’s scholarship (NXP scholarship), Fudan University

• Language skills

Chinese (Mandarine):	Mother tongue
English:	Advanced
French:	Beginner

C Publication list

Peer Reviewed Journals

1. **S. Xie**, V. Savu, W. Tang, O. Vazquez-Mena, K. Sidler, H. Zhang, J. Brugger, "Robust PECVD SiC membrane made for stencil lithography", *Microelectronics Engineering* 88 (2011) 2790-2793.

2. V. Savu*, **S. Xie***, J. Brugger, "100 mm dynamic stencils pattern sub-micrometer structures", *Nanoscale* 2011, 3, 2719. (*shared first author, published on cover page)

3. **S. Xie**, V. Savu, J. Brugger, "Heated stencils for improved nanopatterning in stencil lithography", in preparation.

4. **S. Xie**, C. O. Simonin, W. Tang, V. Savu, H. Zhang, J. Brugger, "Fabrication of stenciled patterns by using PECVD SiC nanostencils", in preparation.

5. D. Sacchetto, **S. Xie**, V. Savu, M. Zervas, G. D. Micheli, J. Brugger, Y. Leblebici, "Vertically-stacked gate-all-around polysilicon nanowire FETs with sub-μm gates patterned by nanostencil lithography", *Microelectronic Engineering* 98 (2012) 355–358.

6. M. Frantlović, I. Jokić, V. Savu, **S. Xie**, J. Brugger, "Effects of tensile stress on electrical parameters of thin film conductive wires fabricated on a flexible substrate using stencil lithography", *Microelectronic Engineering* 98 (2012) 230–233.

Peer Reviewed Conferences

1. **S. Xie**. V. Savu, J. Brugger, “Thermal control extends heated stencil’s life-time”, *EIPBN* 2012, Waikoloa, Hawaii, USA, poster presentation.
2. **S. Xie**, V. Savu, J. Brugger, “Heated membranes with actuated gap reduction and clogging-free apertures for quasi-dynamic stencil lithography”, S. Xie, et al., *IEEE-NEMS 2012*, Kyoto, Japan, oral presentation.
3. **S. Xie**, V. Savu, J. Brugger, “Heated membranes prevent clogging of apertures in nanostencil lithography”, *Transducers’11*, 2011, Beijing, China, oral presentation.
4. **S. Xie**, V. Savu, W. Tang, O. Vazquez-Mena, K. Sidler, H. Zhang, J. Brugger, “Robust PECVD SiC membrane made for stencil lithography”, *MNE 2010*, Genoa, Italy, oral presentation.
5. D. Sacchetto, **S. Xie**, V. Savu, M. Zervas, G. D. Micheli, J. Brugger, Y. Leblebici, “Vertically-stacked gate-all-around polysilicon nanowire FETs with sub-μm gates patterned by nanostencil lithography”, *MNE 2011*, Berlin, Germany, invited oral presentation.
6. M. Frantlović, I. Jokić, V. Savu, **S. Xie**, J. Brugger, “Effects of tensile stress on electrical parameters of thin film conductive wires fabricated on a flexible substrate using stencil lithography”, *MNE 2011*, Berlin, Germany, poster presentation.

Patent

1. **S. Xie**, V. Savu, J. Brugger, “MICROHEATER BASED IN SITU SELF-CLEANING DYNAMIC STENCIL LITHOGRAPHY”, International Patent Application n° PCT/IB2012/052806 filed June 4, 2012

Peer Reviewed Journal Publications during Master Study

1. **S. Xie**, J. Wan, BR. Lu, Y. Sun, Y. Chen, XP. Qu, R. Liu, “A nanoimprint lithography for fabricating SU-8 gratings for near-infrared to deep-UV application”, *Microelectronic Engineering* 85 (5), 914-917.

2. **S. Xie**, BR. Lu, Y. Sun, Y. Chen, XP. Qu, R. Liu, “Fabrication of 150 nm Half-Pitch Grating Templates for Nanoimprint Lithography”, *Journal of Nanoscience and Nanotechnology* 9 (2), 1437-1440.
3. ZC. Xu, **S. Xie**, Z. Shu, BR. Lu, J. Wan, Y. Chen, E. Huq, XP. Qu, R. Liu, “Fabrication and characterization of high extinction ratio transmission polarizers”, *Microelectronic Engineering* 87 (5-8), 1005-1007.
4. B. Lu, **S. Xie**, J. Wan, R. Yang, Z. Shu, XP. Qu, R. Liu, Y. Chen, E. Huq, “Applications of Nanoimprint Lithography for Biochemical and Nanophotonic Structures Using SU-8”, *International Journal of Nanoscience* 8 (1), 151.

D Acknowledgments

This thesis would not have been accomplished without great support from many people. I would like to express my deepest appreciation to everyone who has helped me during the past four years.

I would like to give my greatest gratitude to my supervisor Prof. Juergen Brugger for offering me the possibility of carrying out this interesting research project in LMIS1, where I truly learned knowledge, developed my skills, met friends and experienced different cultures in a very international environment. Thank you very much for all your professional and personal supports, for which I could not forget forever.

I wish I have better words than my deepest gratefulness to my co-supervisor, Dr. Veronica Savu, who is my mentor in daily scientific discussion, who is my model of being an outstanding researcher, and who is also my friend sharing happy moments. I feel very fortunate to start this adventure with Veronica's help from the beginning.

I would also like to thank the jury members for my oral thesis examination: Prof. Alfred Ludwig, Prof. Pasqualina M. Sarro, Prof. Herb Shea and Prof. Martinus Gijs as the jury president. I want to thank Severine Eggli, Mme. Modoux and Marie Halm for all the administrative support during my doctoral study.

I am very grateful to Prof. Lionel Buchaillot, Dr. Damien Ducatteau and Dr. Bernard Legrand all from Institut d'Electronique de Microélectronique et de Nanotechnologie (IEMN), France, for the fruitful collaboration and the great opportunity to stay as short term exchange in IEMN, where I used the nice facilities and received valuable suggestion about IR measurement for my devices.

I want to thank Prof. Adrian Ionescu and Prof. Yusuf Leblebici for the collaboration and discussion in the joint project. Especially I want to thank Davide Sacchetto for our fruitful collaboration on exploring the application of nanostenciling in 3D transistors. I also want to thank Matthias Bopp for the collaboration on early investigation of this project.

I also give my greatest acknowledgment to the Center of Micro-Nanotechnology of EPFL (CMi) and its staff. Without their valuable experience and technical support, I could not imagine having the devices fabricated for my experiments. I want to thank specially to Dr. Philippe Langlet, Dr. Kevin Lister and Dr. Cyrille Hibert for their support on developing new fabrication processes for my experiments.

My biggest thank to all the present and former LMIS1 colleagues, who make our group a big sweet family. I really enjoyed the atmosphere in the group as well as the bear in Satellite and barbeque on the lake side. Especially I would like to acknowledge Dr. Oscar Vasquez-Mena and Dr. Katrin Sidler for transferring the invaluable know-how about stencil lithography in the beginning of my study. I thank Valentin Flauraud for helping me translate the French abstract of my thesis. I also thank Jonas Henriksson for the inspiring discussion and his help on wire bonding. I acknowledge Jonas Grossenbacher for helping me bind the thesis. I am very happy to have had several great master students for their excellent works which also contribute to my research, for which I thank Coralie Ougier Simonin, Sahbi Boujnah and Sebastien Vaneberg.

Last but not least, I give all my heart to thank my dear parents, Jianzhong Xie and Qingzhen Li, who always believe in me and unconditionally understand and love me. I feel sorry that I did not spend so much time together with you and I have not been there for the Chinese New Year in the past four years. No words can express my regret and my love to you! This accomplishment is a gift for you!

Shenqi Xie
Lausanne, April 25, 2013