SILICON HETEROJUNCTION SOLAR CELLS ON N- AND P-TYPE WAFERS WITH EFFICIENCIES ABOVE 20%

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ABSTRACT: A systematic comparison of front- and rear-emitter silicon heterojunction solar cells produced on *n*- and *p*-type wafers was performed, in order to investigate their potential and limitations for high efficiencies. Cells on *p*-type wafers suffer from reduced minority carrier lifetime in the low-carrier-injection range, mainly due to the asymmetry in interface defect capture cross sections. This leads to slightly lower fill factors than for *n*-type cells. However, these losses can be minimized by using high-quality passivation layers. High V_{oc}s were obtained on both types of FZ wafers: up to 735 mV on *n*- and 726 mV on *p*-type. The best V_{oc} measured on CZ *p*-type wafers was only 692 mV, whereas it reached 732 mV on CZ *n*-type. The highest aperture-area certified efficiencies obtained on 4 cm^2 cells were 22.14% (V_{oc}=727 mV, FF=78.4%) and 21.38% (V_{oc}=722 mV, FF=77.1%) on *n*- and *p*-type FZ wafers, respectively, demonstrating that heterojunction schemes can perform almost as well on high-quality *p*-type as on *n*-type wafers. To our knowledge, this is the highest efficiency for a full silicon heterojunction solar cell on a *p*-type wafer, and the highest V_{oc} on any *p*-type crystalline silicon device with reasonable FF.
Keywords: Heterojunction, High-Efficiency, Silicon Solar Cell, c-Si

1 INTRODUCTION

Silicon heterojunction solar cells are interesting candidates for low-cost high-efficiency solar cells. Conversion efficiencies above 23% have indeed already been demonstrated by Sanyo [1], and the production costs of such devices are potentially low. No high-temperature or photolithographic processes are required, since passivation of the crystalline silicon (c-Si) wafer surfaces and formation of the emitter and back surface field are all performed with thin intrinsic and doped hydrogenated amorphous silicon (a-Si:H) layers, usually deposited by plasma-enhanced chemical vapor deposition (PECVD). PECVD fabrication steps are presently well controlled at the industrial scale, benefiting from the knowledge gained in the last decades in the fabrication of large-area thin-film devices.

So far, the highest efficiency silicon heterojunction solar cells were obtained using *n*-doped, rather than *p*-doped, c-Si wafers [2]. Fundamental issues with the band structure, such as the asymmetry between the conduction and valence band offsets (see Fig. 1), are often assumed to reduce performance of *p*-type heterojunction solar cells [3]. Nevertheless, *n*-type wafers are less readily available on the market than *p*-type wafers, which are widely used for the production of conventional (diffused-emitter) silicon solar cells. The possibility to produce high-efficiency heterojunction solar cells from *p*-type wafers is thus of great practical interest. Such cells have already been demonstrated by several groups [4-9], but with efficiencies significantly lower than those achieved on *n*-type wafers.

In this work, by means of minority carrier lifetime, current-voltage and quantum-efficiency measurements, a systematic comparison of silicon heterojunction solar cells produced on *n*- and *p*-type wafers is performed in order to investigate their potential and limitations for high efficiencies. In particular, since charge transport in the cell is one of the major differences when using *n*- or *p*-type substrates (different types of minority carriers and different band structures, as shown in Fig. 1), cells with front and back emitters are experimentally analyzed. In this way, insights into transport are provided. Finally, the best efficiencies obtained on different wafer types (doping type and material quality) are presented.

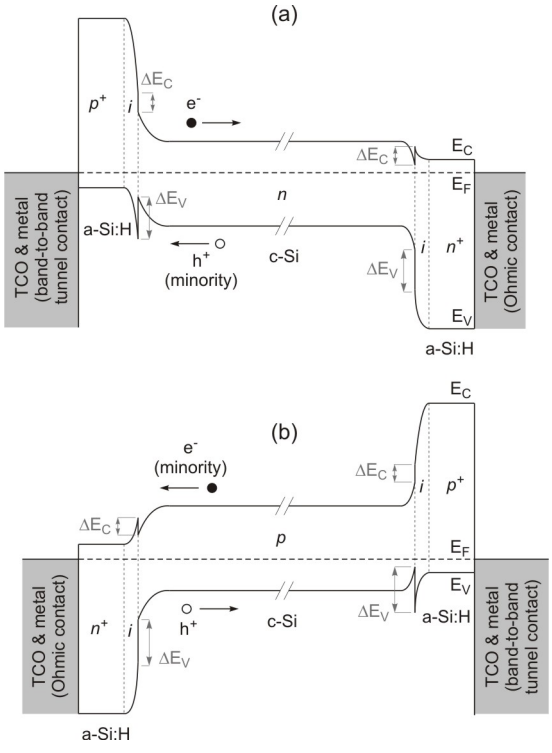

Figure 1: Schematic band diagram of a silicon heterojunction cell based on: (a) an *n*-type c-Si wafer; (b) a *p*-type c-Si wafer. E_C denotes the conduction band edge, E_V the valence band edge, E_F the Fermi level, e^- electrons, and h^+ holes. Band offsets (ΔE_C, ΔE_V) are present at each a-Si:H/c-Si interface, in both bands, and band bending is likely induced at the a-Si:H/TCO interface as well (not drawn, for simplicity). For front-emitter cells, light is incident from the left; for rear-emitter cells, from the right.

2 HETEROJUNCTION SOLAR CELL FABRICATION

Unless otherwise stated, *n*- and *p*-doped (4 Ω·cm) float zone (FZ) c-Si(100) wafers were used as substrates. As-cut wafers were textured in a potassium hydroxide (KOH) solution (final wafer thickness: 230 µm), wet-chemically cleaned, and dipped in hydrofluoric acid (HF) just before PECVD. Intrinsic and doped a-Si:H layers were deposited on the whole wafer surfaces at 200 °C using mixtures of silane (SiH_4), hydrogen (H_2), phosphine (PH_3) and trimethylboron ($B(CH_3)_3$) in an automated, large-area (electrode size: 50 cm x 60 cm), narrow-gap (13 mm), parallel-plate industrial PECVD reactor powered at very high frequency (VHF, 40.68 MHz). The large area of this reactor allowed us to co-deposit identical a-Si:H layers on several wafers in the same run, with excellent uniformity.

Transparent conductive oxide (TCO), typically indium tin oxide (ITO), was then deposited on the front and back of the wafers by DC magnetron sputtering. The size of the cell on the wafer was defined by using a shadow mask during deposition of the front and back ITO layers. The ITO properties required for the front and the back layers differ from each other. At the front, the ITO refractive index and the layer thickness were chosen in order to create an anti-reflection coating with a minimum in reflectivity at approximately 600 nm. The carrier density is also an important parameter for the front ITO layer, since there is a trade-off between low parasitic free-carrier absorption and low resistivity [10]. The back ITO layer was optimized for transparency alone since lateral transport is not required, as it is covered by a silver back reflector. This back reflector was deposited by sputtering immediately after the back ITO, using the same shadow mask. A front grid was screen-printed with a low temperature silver paste, and the cell was cured at around 200 °C for several minutes. Note that all of these fabrication steps are fully compatible with cell production at an industrial scale.

3 RESULTS AND DISCUSSION

3.1 Effect of the wafer doping type and emitter position on silicon heterojunction solar cell performance

Heterojunction solar cells were produced on *n*- and *p*-type wafers, with the emitter located either at the front side (front-emitter cell) or at the back side of the cell (rear-emitter cell). In this way, potential differences in charge carrier transport through the wafer are highlighted. All four possible cell structures were tested and are schematically shown in Fig. 2. All wafers were batch-processed together during the wet-chemical treatments and the a-Si:H, ITO and back Ag layer depositions. Only the screen-printed front grid was applied on one cell at a time, but consecutively, and with the same Ag paste and screen. Therefore, every individual layer can be considered as strictly identical on all cells, although each cell has its own particular structure. The size of each cell is 2 cm x 2 cm.

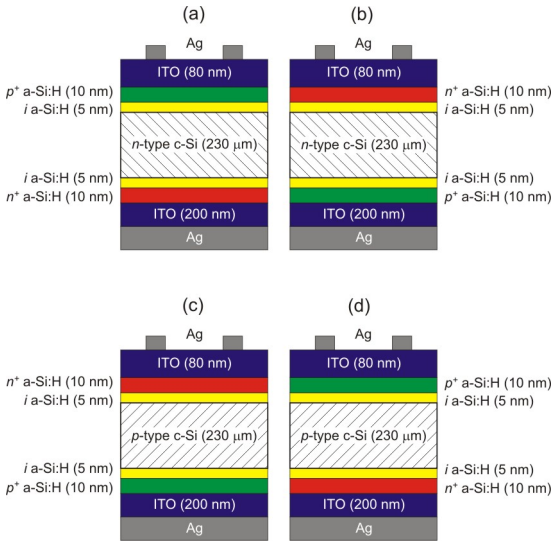

Figure 2: Schematic drawings of the different heterojunction solar cell structures tested (not to scale): (a) *n*-type wafer with front emitter; (b) *n*-type wafer with rear emitter; (c) *p*-type wafer with front emitter; (d) *p*-type wafer with rear emitter.

After deposition of the in^+ and ip^+ a-Si:H stacks by PECVD, the minority carrier lifetimes of the solar cell precursors were measured with a quasi-steady-state photoconductance system. Since infrared light is used to generate carriers homogeneously in the wafer, no difference is observed when illuminating from the in^+ or the ip^+ side. Samples on *n*-type and *p*-type wafers exhibit different behavior, especially in the low-injection range (see example in Fig. 3). On the one hand, at high injection levels, the lifetime values are relatively similar: 1.9 ms on *n*-type and 1.6 ms on *p*-type at a minority carrier density of 10^{16} cm^{-3}, for example (lifetimes are limited by unavoidable Auger recombination in this range). Therefore there is the potential for high open-circuit voltages (V_{oc}) on both types of wafers, since these high-lifetime cells reach high injection at open circuit. The 1-sun implied V_{oc} values given in Fig. 3 confirm this high V_{oc} potential and show no significant difference between *n*- and *p*-type. On the other hand, a dramatic drop is observed on *p*-type at injection levels below $3 \cdot 10^{15}$ cm^{-3}: 5.6 ms is measured on *n*-type and 2.1 ms on *p*-type at 10^{15} cm^{-3}, for example. As with c-Si passivated by thermally grown silicon dioxide (SiO_2) [11], the larger capture cross section of interface defects for electrons than for holes explains this difference in the injection-dependent lifetimes of *n*- and *p*-doped samples. Since electrons (minority carriers in *p*-doped c-Si) are more easily lost at the interface than holes, *p*-type samples suffer more from surface defect-assisted minority carrier recombination than *n*-type samples, especially at low injection. Even if the asymmetry in the respective cross sections is much less pronounced for defects at the a-Si:H/c-Si interface than for defects at the SiO_2/c-Si interface [12], it is nevertheless sufficient to reduce the low-injection lifetime on *p*-type samples. The behavior cannot be attributed to bulk defects: high-quality FZ wafers were used here and longer low-injection lifetimes are observed when similar wafers are passsivated with the negative fixed-charge dielectric aluminum oxide (Al_2O_3) [13, 14]. Note that the behavior at low injection is also seen with *p*-doped wafers passivated with ip^+ a-

Si:H stacks on both sides (data shown in [15]). This suggests that the small additional field-effect passivation created by the p^+ doped layers is not sufficiently strong to screen the interface defects and avoid surface recombination at low injection levels. In addition, *p*-doped samples passivated with in^+ a-Si:H stacks on both sides or with only *i* a-Si:H layers on both sides exhibit also the same behavior (data shown in [15]). Thus, the drop in lifetime at low injection is not dominated by the band bending configuration at the interface.

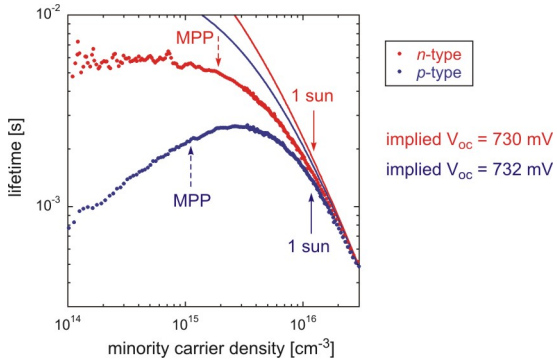

Figure 3: Minority carrier effective lifetimes of solar cell precursors (textured wafers passivated with co-deposited in^+ and ip^+ a-Si:H stacks) on *n*- and *p*-type FZ wafers. The injection levels corresponding to 1-sun illumination are marked by solid arrows, and the corresponding implied V_{oc} values are given. The injection levels corresponding to the maximum power points of the finished devices (under 1 sun illumination) are marked by dashed arrows. Combined radiative and Auger recombination limits are shown by solid lines.

Since the minority carrier density changes from high to low values during an illuminated current-voltage (IV) measurement as we move from open-circuit to short-circuit conditions, a reduced fill factor (FF) can be expected for completed solar cells when *p*-type wafers are used. This drop in the lifetime will indeed cause a reduction in the cell performance at the maximum power point (MPP) compared to a cell for which the lifetime stays flat for decreasing injection (*n*-type case). This effect can be clearly seen and quantified by calculating "implied IV curves" from the solar cell precursor lifetime data, similar to Suns-V_{oc} measurements. In a standard Suns-V_{oc} measurement, the V_{oc} of a finished device is measured at illumination intensities (I_L) between 0 and >1 sun. A "pseudo IV curve" is then obtained by plotting pseudo current density (pJ) against the measured illumination-dependent $V_{oc}(I_L)$. This pseudo current density is defined by $pJ(I_L) = J_{sc}\cdot(1\text{-}I_L)$, where J_{sc} is the short-circuit current density of the finished device measured in a standard IV measurement (at 1 sun), and I_L is expressed in number of suns. In our implied IV measurements, however, the device is not finished (the emitter is present but without terminals) and $V_{oc}(I_L)$ is thus replaced by the implied voltage determined from the excess minority carrier densities, which is also measured at different illumination intensities during an injection-dependent lifetime measurement. The implied current density is calculated in the same way as pJ in a Suns-V_{oc} measurement, namely implied $J(I_L) = J_{sc}\cdot(1\text{-}I_L)$. Since both pseudo IV and implied IV measurements are done at open circuit, the pseudo fill factor (pFF) and implied FF values obtained from these curves exclude series resistance and possible issues related to transport and extraction of carriers through the contacts. Fig. 4 shows the implied IV curves of the two solar cell precursors of Fig. 3, and also of a virtual *p*-type sample with a constant lifetime at low injection and the same behavior at high injection as the actual *p*-type sample. Implied FF values obtained from these curves show clearly that an absolute loss of around 1% in the real FF of the finished device can be attributed to the drop in lifetime at low injection for the *p*-type sample, compared to the virtual flat-lifetime case ("*p*-type" curve compared to "*p*-type flat" curve). A total absolute loss of around 2% in real FF is estimated compared to the *n*-type sample, due solely to this difference in lifetime at low injection ("*p*-type" curve compared to "*n*-type" curve). From this, we conclude that high V_{oc} values are not a sufficient criterion to obtain high FF values and, despite comparable V_{oc}s, cells on *p*-type wafers are expected to be less efficient than those on *n*-type wafers. High voltage at maximum power point (V_{MPP}) is of greater importance. As the lifetime at MPP is determined here by surface recombination, FF depends thus fundamentally on the a-Si:H/c-Si interface properties. Note that in *p*-type multicrystalline silicon solar cells, bulk defects (rather than surface defects) create also a strong injection-level dependence of the lifetime, resulting similarly in a limitation of FF values [16].

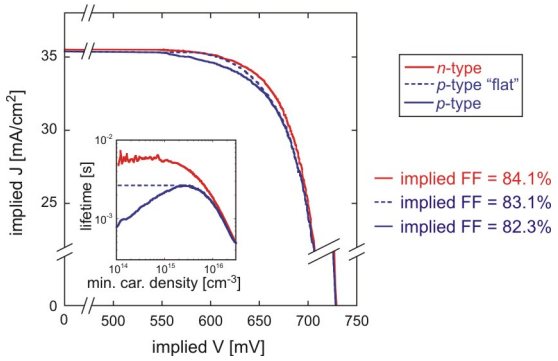

Figure 4: Detail of the "implied IV curves" around the maximum power point and implied FF values calculated from the lifetime data of the *n*- and *p*-type solar cell precursors of Fig. 3. The calculated implied IV curve of a modified *p*-type case is also shown, in which we assumed a constant ("flat") lifetime at low injection (see corresponding curves in the inset). The J_{sc} values taken for the calculations of implied J are the actual values obtained from the finished cells (see Table I below).

The detailed parameters of the finished cells are given in Table I. The cells were measured under standard test conditions (25 °C, AM 1.5 G) with a shadow mask that has an opening that is the same size as the cells (defined by the front ITO layer and back metallization). pFF values obtained from standard Suns-V_{oc} measurements done with the same shadow mask are also given in Table I.

For standard front-emitter cells, similar V_{oc} values are obtained on *n*- and *p*-type wafers, as expected from the carrier lifetime measurements (Figs. 3 and 4), whereas FF and pFF are slightly lower on *p*-type. Measured FF and pFF values are consistent with implied FF values predicted in Fig. 4, showing an absolute loss of

between 1 and 2% on *p*-type compared to *n*-type. pFF is consistently slightly lower than implied FF, likely due to additional passivation losses induced by the processes required to finish the cells (ITO and Ag sputtering, front grid screen-printing and curing). The J_{sc} values are very similar on both types of wafers because light absorption in the cells is comparable. The wafer thicknesses and front ITO layers are identical, and our *n*- and *p*-doped a-Si:H layers have similar optical absorption properties [10] and thicknesses.

Table I: IV parameters of 4 cm^2 cells (average of 6 cells)

doping type	emitter position	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	pFF [%]	η [%]
n-type	front	718	35.6	76.5	83.2	19.6
n-type	rear	713	35.6	75.0	80.7	19.0
p-type	front	718	35.7	75.5	81.6	19.4
p-type	rear	716	35.6	71.8	77.5	18.3

With regards to carrier transport, it was shown by both experiment and simulation that band offsets influence the transport mechanisms at low bias, where tunneling of carriers through band offsets can take place [17-19]. This will result in different carrier transport in *n*- and *p*-type heterojunction solar cells due to the different band structure seen by minority carriers [18, 19]. In device-operating conditions (similar to a high-bias regime), however, the a-Si:H/c-Si interface defect density was shown to be the limiting factor for solar cell performance [3, 17-20]. Suppressing the defect states at the interfaces is indeed the key to efficient transport and high V_{oc} and FF values, whereas band structures may play only a minor role [19]. Therefore, the slightly lower FF of *p*-type cells is probably not caused only by pure transport problems linked to band offsets, e.g. band offset tunneling. The asymmetry in capture cross sections is rather the dominant effect responsible for the lower FF of *p*-type cells, as discussed above.

When the emitter is put at the back of the cell, losses in FF and pFF are observed on both types of wafers, especially in the *p*-type case. The pFF values indicate that the FF ranking of the different cells is not dictated only by series resistance losses, but also by something intrinsically related to the cell structure (pFF excludes series resistance). V_{oc} values are slightly reduced as well, but to a lesser extent. This reduction in performance of rear-emitter cells may result from the decreased illumination of the a-Si:H layers at the emitter side. The properties of the emitter and the transport through the a-Si:H layers may improve under increased illumination, resulting in higher FF for front-emitter devices. The relatively similar J_{sc} values of the four different kinds of cells are again explained by comparable absorption coefficients and thicknesses of the *n*- and *p*-doped a-Si:H layers. Overall, despite these slight differences, the performance of rear-emitter cells is not dramatically lower than that of front-emitter cells, underlining the potential to fabricate high-efficiency back-contacted heterojunction solar cells.

After specific optimization of the a-Si:H and TCO layers for rear-emitter cells, the best FF that we obtained on an *n*-type wafer was 78.1% (82.8% pFF), giving an efficiency of 20.3%.

No significant difference is observed in spectral response (external and internal quantum efficiencies) between *n*- and *p*-type cells and between front- and rear-emitter cells (data shown in [15]). This is in good agreement with the similar J_{sc} values obtained from illuminated IV measurements (Table I).

3.2 Best efficiencies obtained on *n*- and *p*-type wafers

Finally, we present in this section the results of optimized front-emitter heterojunction solar cells produced on different types of wafers (*n*- or *p*-doped, FZ or Czochralski (CZ)) and of different sizes (4, 100 and 149 cm^2, aperture areas). It should be noted that more optimization has been done on 4 cm^2 cells. All wafers have the same resistivity (4 Ω·cm). Specific optimization has been done differently for *n*- and *p*-type wafer-based cells. Since parasitic light absorption in the front stack of layers is of particular importance for heterojunction solar cells [10], the properties and thicknesses of the *n*- and *p*-doped a-Si:H layers and TCO layers have been adjusted differently according to the cell structure, aiming for high transparency at the front. This optimization explains the higher efficiencies obtained compared to the cells described in the previous section, where simple co-depositions of standard layers were done. The electrical properties of these optimized cells are given in Table II.

Table II: IV parameters of the best heterojunction solar cells (all cells have screen-printed contacts)

wafer type	cell area [cm^2]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
FZ *n*-type	4	727	38.9	78.4	22.14*
FZ *n*-type	100	727	36.5	78.9	20.95
FZ *n*-type	149	732	36.3	75.2	19.95
CZ *n*-type	4	731	36.9	77.1	20.80
CZ *n*-type	100	730	36.5	77.7	20.71
CZ *n*-type	149	728	35.0	73.4	18.74
FZ *p*-type	4	722	38.4	77.1	21.38*
CZ *p*-type	4	679	36.2	70.6	17.33
CZ *p*-type	100	692	35.1	70.1	17.04
CZ *p*-type	149	689	36.3	67.7	16.92

* certified by Fraunhofer ISE CalLab

Thanks to well-controlled wafer cleaning and to high-quality passivating a-Si:H layers [21, 22], the V_{oc}s on *n*-type wafers are similar on FZ and CZ material. Values as high as 733 mV and 732 mV were obtained on FZ and CZ material, respectively (160 µm thick wafers). The slightly lower value for the best 4 cm^2 cell on FZ is due to a greater wafer thickness (230 µm). In this study, the highest V_{oc} value was obtained using a 96 µm thick FZ *n*-type wafer, yielding 735 mV (20.8% cell efficiency, limited by J_{sc}). Differences in wafer thickness also explain the higher J_{sc} of the 4 cm^2 cell on FZ, as more light is absorbed in the thicker wafer. Although cell performance slightly decreases when cell area increases (mainly due to some inhomogeneities, slightly increased shadow losses and electrical losses in the front grid), efficiencies well above 20% can be maintained on 100 cm^2 cells, and close to 20% on full-5-inch cells. The highest aperture-area efficiencies obtained on CZ and FZ *n*-type material are 20.8% and 22.1%, respectively.

Conversely, on the *p*-type wafers used in this work, a difference of more than 30 mV in V_{oc} is clearly visible between FZ and CZ material. This large difference is likely due to the relatively low quality of the CZ *p*-type wafers used in this study (numerous bulk defects with large electron capture cross section). Wang et al. showed that a loss of less than 10 mV can be maintained when

changing from FZ to CZ *p*-type wafers [4], using CZ *p*-type material that was probably of better quality than that used here. The low FF values of the CZ *p*-type cells are also attributed in part to the lifetime dependence at low injection described previously, which become even more critical if the implied V_{oc} is reduced (MPP is at an even lower injection level and therefore V_{MPP} is strongly reduced). It should also be noted that, contrary to *n*-type c-Si, CZ *p*-type material additionally suffers from severe light-induced degradation caused by the boron-oxygen complex (non-degraded cells presented here). Thus, the use of thinner wafers should be especially beneficial in the *p*-type case. Then, light-induced degradation is reduced, and the minority carrier density is increased at MPP, leading to higher FF values.

As discussed earlier, the FF and V_{oc} values are generally lower on *p*-type than on *n*-type wafers, limiting cell performance. Nevertheless, a cell with a V_{oc} of 722 mV, a FF of 77.1% and an efficiency of 21.38% has been produced on FZ *p*-doped material, and the highest V_{oc} measured on a *p*-type cell reached 726 mV (230 µm thick wafers). To our knowledge, these are the first V_{oc}s significantly above 700 mV and the highest efficiency for a full silicon heterojunction solar cell on a *p*-type wafer. Silicon heterojunction solar cells can thus perform almost as well on high-quality *p*-type as on *n*-type wafers, with efficiencies over 21% demonstrated for both doping types (Fig. 5).

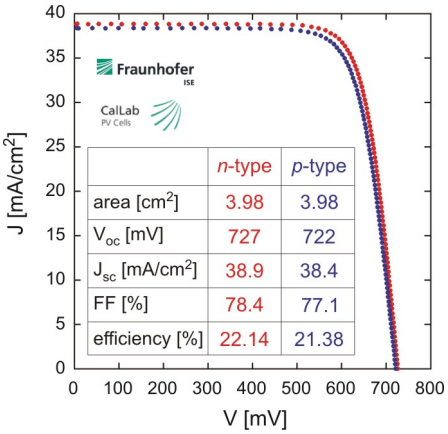

Figure 5: Illuminated IV curves of the best 2 cm x 2 cm cells on *n*- and *p*-type FZ wafers (certified by Fraunhofer ISE CalLab).

4 CONCLUSION AND OUTLOOK

Mainly due to the asymmetry in interface defect capture cross sections but also due to the band structure seen by minority carriers, silicon heterojunction solar cells generally perform better on *n*-type than on *p*-type wafers. A major difference is observed in the minority carrier lifetime, especially at low injection, leading to reduced FF values for *p*-type cells. Nevertheless, devices with efficiencies above 21% and V_{oc} values above 720 mV have been demonstrated on both types of FZ wafers. This key feature of heterojunction solar cells is thus preserved independent of the wafer doping type, proving that high efficiencies are also possible on *p*-type material. However, for mass scale production, the use of CZ material is obviously the only possible option due to economic considerations. In this case, *n*-type wafers are probably preferable, as we achieved comparable efficiencies on *n*-type FZ and CZ material. Nevertheless, if the quality of commercially available *p*-type CZ material is improved or if the wafer thickness is sufficiently reduced, the use of *p*-type CZ wafers could be a possible alternative for the industrial production of silicon heterojunction solar cells.

5 ACKNOWLEDGMENTS

The authors are indebted to Mr. Y. Andrault for his dedication and excellent work in wafer preparation.

This work was supported by Roth & Rau Switzerland, by Axpo Naturstrom Fonds, by the European Commission (FP7 project 20plµs, Grant No. 256695), and by the Swiss Commission for Technology and Innovation.

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