Analog microelectronic emulation for dynamic power system computation

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To you, dear reader.
Thank you for your interest.

Abstract

Power system dynamic simulators can be classified according to multiple criteria, including speed, precision, cost and modularity (topology, characteristics and model). Existing simulators are based on time-consuming numeric algorithms, which provide very precise results. But the evolution of the power grid constantly changes the requirements for simulators. In fact, power consumption is steadily increasing; therefore, the power system is always operating closer to its limits. Moreover, focus is put on decentralized and stochastic green energy sources, leading to a much more complex and less predictable power system. In order to guarantee security of supply under these conditions, real-time control and online security assessment are of the utmost importance. The main requirement for power system simulators in this context thus becomes the simulation time. The simulator has to be able to reproduce power system phenomena much faster than their real-time duration.

An effective way to accelerate computation time of power system stability simulators is based on analog emulation of the power system grid. The idea is to avoid the heavy, time-consuming numerical matrix calculations of the grid by using an instantaneous analog Kirchhoff grid, with which computation becomes intrinsically parallel and the simulation time independent of the power system topology size.

An overview of the power system computation history and the evolution of microelectronics highlights that the renaissance of dedicated analog computation is justified. Modern VLSI technologies can overcome the drawbacks which caused the disappearance of analog computation units in the 1960s.

This work addresses therefore the development of a power system emulation approach from its theoretical principles to the behavioral design and the microelectronic implementation of a first demonstrator.

The approach used in this research is called AC emulation approach and is based on a one-to-one mapping of components of the real power system (generator, load and transmission line) by emulating their behavior on a CMOS microelectronic integrated circuit (ASIC). The signals propagating on the emulated grid are the shrunk and downscaled current and voltage waves of the real power system. The uniqueness of this emulation approach is that frequency dependence of the signals is preserved. Therefore, the range of phenomena that can be emulated with an AC emulator depends only on the implemented models. Within the framework of this thesis, we restrict our developments to transient stability analysis, as our main focus is put on emulation speed.

We provide behavioral AC emulation models for the three main power system components. Thereby, special attention is paid to the generator model, which is shown to introduce a systematic error. This error is analyzed and reduced by model adaptation. Behavioral simulation results validate the developed models.

Moreover, we suggest custom programmable analog building blocks for the implementation of the proposed behavioral models. During their design, application specific requirements, as well as imperfections, calibration, mismatch and process-variation aspects, are taken into account. In particular, the design of the tunable floating inductance used in all three AC emulation models is discussed in detail. In fact, major design challenges have to be addressed in order to achieve an inductance suitable for our application.

Finally, a first AC emulation demonstrator is presented. A benchmark using a fixed two-machine topology has been implemented using a 0.35μm 3.3V CMOS technology. The characteristics of the emulated components (i.e. generators and transmission lines) are reprogrammable, allowing short circuits to be emulated at different distances from the generator. The emulated phenomena are shown to be $10'000$ times faster than real time, therefore proving the high-speed capabilities of AC emulation.

Keywords: active tunable inductance, analog CMOS design, analog computation, analog emulation, analog integrated circuit, application specific integrated circuit (ASIC), high-speed simulation, power system simulation, power system stability, VLSI technology

Résumé

Les réseaux électriques sont de plus en plus amenés à opérer proche de leur limite de fonctionnement, en raison de l'accroissement de la demande des consommateurs, ainsi que par la mise en place de nouvelles sources d'énergies stochastiques et décentralisées. Il devient indispensable de disposer d'un diagnostic en temps réel de l'état de stabilité du réseau, afin de pouvoir au mieux prévenir et s'écarter de l'état d'instabilité du réseau. Cette prospection fait appel à l'étude des phénomènes dynamiques inhérents aux réseaux électriques à l'aide de simulateurs dédiés. Les points d'intérêt de tels simulateurs sont la vitesse de calcul, la précision des résultats, le coût ainsi que la flexibilité. Les solutions existantes requièrent cependant la résolution d'équations complexes, extrêmement onéreuses en temps de calcul. La constante évolution des caractéristiques du réseau électrique ne peut de ce fait que difficilement être prise en compte. Dès lors, leur utilisation à des fins de sécurisation de l'approvisionnement en ressources électriques reste limitée.

Afin d'adresser les problèmes liés à l'évaluation de la sécurité d'approvisionnement et au contrôle du réseau en temps réel, de nouveaux outils de simulation centrés sur la rapidité d'exécution doivent être développés. Ces calculateurs à vitesse de résolution accrue doivent être en mesure de reproduire le comportement dynamique d'un réseau électrique en temps réel, voir même plus rapidement que le temps réel.

Une méthode intéressante permettant de réduire le temps de calcul est basée sur le concept de l'émulation analogique des lignes de transmission du réseau. L'idée est de s'affranchir des lourds calculs matriciels nécessaires à l'évaluation de l'état des noeuds d'un réseau (équations de Kirchhoff) à l'aide d'un modèle analogique dédié dont la résolution est quasiment instantanée. L'opération devient donc intrinsèquement parallèle et son temps d'exécution indépendant de la taille du réseau. Ce travail se consacre au développement d'une nouvelle approche d'émulation, partant de l'élaboration de ses principes théoriques et allant jusqu'à la conception et l'implémentation d'un premier démonstrateur microélectronique.

L'approche sur laquelle repose ce travail de thèse est appelée approche d'émulation AC et est basée sur l'idée d'émuler le comportement de chaque composant physique du réseau électrique (ligne de transmission, générateur et charge) à l'aide d'électronique active. Les signaux qui se propagent sur le réseau émulé sont alors les signaux de tension et courant du réseau réel miniaturisés et transposés en fréquence.

La particularité d'une telle approche est la conservation de la dépendance fréquentielle des éléments constituant le réseau. La gamme des phénomènes qui peuvent être considérés

dépend donc uniquement des modèles mis en oeuvre. Dans le cadre de cette thèse, les développements sont limités à l'analyse de la stabilité transitoire du réseau. Cette analyse permettra d'illustrer la réduction du temps de calcul inhérente à l'émulation AC.

Afin de valider les concepts évoqués précédemment, des modèles comportementaux des trois principaux composants du réseau électrique adaptés à l'utilisation dans l'émulation AC sont présentés. Une attention particulière a été portée au modèle du générateur qui, par sa construction, souffre d'une erreur systématique. Cette erreur est analysée et réduite par l'adaptation de ce même modèle. Des résultats obtenus à l'aide de simulations permettent de valider les développements.

La réalisation de l'émulateur comprend ensuite la conception de blocs analogiques programmables dédiés à l'implémentation des modèles développés dans ce projet. Tout au long de leur conception, les aspects spécifiques à cette application, ainsi que les aspects liés à la microélectronique (imperfections et disparité des composants, variations du procédé, calibration) ont été pris en compte. Une attention particulière est portée à la conception de l'inductance flottante programmable utilisée dans chacun des trois modèles. En résumé, des défis majeurs doivent être abordés afin de parvenir à la conception d'une inductance adaptée à l'application décrite dans ce projet.

Dans l'ultime partie de ce document, un démonstrateur d'émulation AC est présenté. Une topologie fixe de réseau électrique, composée de deux machines, a été implémentée en utilisant une technologie 0.35μm 3.3V CMOS. Les caractéristiques des composants émulés (i.e. générateurs et lignes de transmission) sont reprogrammables. Des courts-circuits, peuvent être représentés à des distances programmables sur la branche reliant les deux machines. Les phénomènes émulés s'avèrent 10'000 fois plus rapide que le temps réel. La réduction du temps de calcul intrinsèque à l'émulation AC a ainsi pu être vérifiée.

Mots-clés: calcul analogique, circuit integré analogique, circuit intégré propre à une application (ASIC), conception des circuits analogiques CMOS, émulation analogique, inductance active variable, simulation à haute vitesse, simulation des réseaux électriques, stabilité des réseaux électriques, technologie VLSI

Zusammenfassung

Simulatoren der dynamischen Stabilität des Höchstspannungsübertragungsnetzes (kurz: Netzsimulatoren) können nach mehreren Kritierien beurteilt werden. Dazu gehören Geschwindigkeit, Präzision, Preis und Flexibilität (Topologie, Eigenschaften, Modelle). Existierende Simulatoren basieren auf zeitintensiven numerischen Algorithmen, welche sehr präzise Resultate liefern. Durch die Evolution des Übertragungsnetzes ändern sich die Anforderungen an die Simulatoren fortlaufend. In der Tat, steigt zum Beispiel der Stromverbrauch stetig an. Dies führt dazu, dass das Übertragungsnetz immer näher an seinen technischen Grenzen arbeitet. Zusätzlich dazu, verschiebt sich der energiepolitische Schwerpunkt auf die Integration von dezentralisierten und stochasitischen erneuerbaren Energiequellen. Dies führt zu einem viel komplizierteren und weniger vorhersehbaren Stromnetz. Um unter diesen Voraussetzungen die Versorgungssicherheit zu gewährleisten, sind Echtzeit-Regelung und Online Sicherheitsbeurteilungen des Stromnetzes von zentraler Bedeutung. Die Hauptanforderung an Netzsimulatoren in diesem Zusammenhang ist die Simulationszeit. Solche Simulatoren müssen fähig sein die dynamischen Phänomene des Stromnetzes viel schneller als ihre Echtzeitdauer zu reproduzieren. Die bisher existierenden numerischen Simulatoren sind zu langsam für diese Aufgabe.

Eine effiziente Methode die Simulationszeit von Netzsimulatoren zu reduzieren basiert auf dem Prinzip die Übertragungslinien zu emulieren. Die Idee dahinter ist die komplexen, zeitintensiven Matrizenberechnungen der numerischen Simulatoren durch eine instantan funktionierende Kirchhoff Schaltung zu ersetzen. Die Berechnungen werden dadurch höchstmöglichst parallelisiert und die Simulationszeit wird somit völlig unabhängig von der Grösse des zu simulierenden Stromnetzes.

Diese Forschungsarbeit befasst sich mit der Entwicklung eines Stromnetzemulationsansatzes von seinen theoretischen Grundlagen über die Entwicklung von Verhaltensmodellen und derer mikroeletronischer Umsetzung bis hin zur Erstellung eines Prototypen.

Der Emulations-Ansatz, der im Rahmen dieser Arbeit entwickelt wurde heisst AC Emulation und basiert auf einer Eins-zu-Eins Abbildung des Verhaltens der Stromnetzkomponenten (Generatoren, Lasten und Übertragungslinien) auf einen Mikrochip durch dazu eigens entwickelte analoge CMOS Schaltungen. Die Signale auf dem emulierten Stromnetz sind daher die geschrumpften und frequenzverschobenen Strom- und Spannungssignale, welche auch auf dem realen Stromnetz exisitieren.

Dieser Emulationsansatz zeichnet sich dadurch aus, dass die Freqeunzabhängigkeit der Signale erhalten bleibt. Daher ist die Reihe der Phänomene, welche mit einem AC Em-

ulator abgebildet werden können, ausschliesslich von den gewählten Komponentenmodellen abhängig. Im Rahmen dieser Arbeit setzten wir uns das Ziel einen AC Emulator für die Analyse der transienten Stabilität des Stromnetzes zu erstellen und dadurch das Hochgeschwindigkeitspotential dieses Ansatzes zu beweisen.

Verhaltensmodelle für die drei Hauptnetzkomponenten wurden entwickelt. Dabei wurde das Hauptaugenmerk auf das Generatorenmodell gelegt, da gezeigt werden konnte, dass dieses einen systematische Abweichung aufweist. Dieser Fehler wurde analysiert und durch eine Modellanpassung reduziert. Die Gültigkeit der Modelle wurde durch Simulationen überprüft.

Für die Realisierung der entwickelten Verhaltensmodelle wurden massgeschneiderte, programmierbare analoge CMOS Schaltugen entwickelt. Während ihrem Design wurden anwendungsspezifische Anforderungen, sowie auch Imperfektions-, Kalibrations-, Diskrepanz- und Prozessvariationsaspekte berücksichtig. Insbesondere während der Entwicklung der programmierbaren, erdfreien Induktanz, welche in allen drei Netzkomponenten vorkommt, mussten grössere Design-Herausforderungen gelöst werden.

Der AC Emulation Prototyp ist ein Benchmark, bestehend aus einer 2-Generatoren-Architektur, das in einer 0.35μm 3.3V CMOS Technologie implementiert wurde. Die Charakteristiken der emulierten Komponenten (Generatoren und Übertragungslinien) sind programmierbar und Kurzschlüsse in verschiedenen Abständen von den Generatoren können reproduziert werden. Mit diesem ersten AC Emulations Prototypen konnte das Hochgeschwindigkeitspotential von AC-Emulationsansätzen vollumfänglich bewiesen werden: Die emulierten Phänomene sind 10′000 mal schneller als Echtzeit.

Schlüsselwörter: Aktive variable Induktanz, analog CMOS Schaltungen, analoge Berechnungen, analoge Emulation, analoge integrierte Schaltungen, ASIC Schaltungen, Stromnetzsimulation, Hochgeschwindigkeitssimulation, Stromnetzstabilität, VLSI Technik

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List of Acronyms

ASIC Application Specific Integrated Circuit

CCT Critical Clearing Time

CM Common Mode

CMIR Common Mode Input Range

CMOS Complementary Metal Oxide Semiconductor

CQFP Ceramic Quad Flat Pack

DAE Differential Algebraic Equation

FPAA Field Programmable Analog Array

FPGA Field Programmable Gate Array

FPPNS Field Programmable Power Network System

GBW Unity Gain Bandwidth

GPU Graphical Processing Unit

HF High Frequency

MCU Microcontroller Unit

OP Operating Point

OTA Operational Transconductance Amplifier

PC Personal Computer

PCB Printed Circuit Board

PDA Personal Digital Assistant

PM Phase Margin

PSA Power System Atom

RF Radio Frequency

SNR Signal-to-Noise Ratioĺ

THD Total Harmonic Distortion

UI User Interface

VCO Voltage Controlled Oscillator

VHF Very High Frequency

VLSI Very-large-scale integration

Chapter 1.

1 Introduction

1.1. Context

A stable power system[1], which delivers electric energy safely, reliably, economically and in a timely fashion, is of the utmost importance. Indeed, modern life as we know it is highly dependent on electricity. Most of our daily activities need, to a greater or lesser extent, electricity. An adequate supply of electricity is therefore necessary for satisfying basic needs, for economic development and hence for the stability of a country. In this context, it is important to note that Switzerland estimates the costs of power outages to be around CHF 3 million per minute. And it is even harder to imagine the consequences an insecure supply would have on everyday life. [1, 2]

Most of today's European power system was built in the post-war period. In the past, reliability was ensured by having excess capacity in the system, with globally unidirectional electricity flow to consumers from centrally dispatched power plants. While innovation and technology have dramatically transformed other industrial sectors, the electric system, for the most part, has continued to operate in the same way for decades. There is a popular comparison that emphasizes this lack of change:

> If Alexander Graham Bell were somehow transported to the 21st century, he would not begin to recognize the components of modern telephony - cell phones, texting, cell towers, PDAs, etc. - while Thomas Edison, one of the grid's key early architects, would be totally familiar with the grid. [3]

Slowly, different circumstances and evolutions pushing the classical power system to operate in a way for which it was not designed, lead to a change in the mindset of stakeholders.

- The above-described lack of investment, combined with an asset life of 40 or more years, the difficulty of obtaining rights for expanding the transmission system and

[1] In this thesis "power system", as long as nothing else is stated, refers only to the transmission and sub-transmission level of the power system.

the ever-increasing consumption of energy has resulted in an inefficient power system, working always closer to its operating limits. The following background information underlines this point:

1. Over the past ten years, European electricity consumption has further increased by more than 20%. And in the future, European electricity consumption is predicted to increase by a further 1.2% per year until 2035 [4, 5]. There are numerous reasons for this. There is, of course, the ever increasing population; but there are also such factors as economic growth, rising traffic performance and the expansion of building area. Moreover, the broadening digitalization of Europe and the transition from fossil fuels to new technologies also create additional electricity demand.

2. The legal approval process for getting the rights to construct transmission lines takes, in Switzerland, an average of between 9 and 12 years. Often it takes even more than 20 years. Additionally, today, two thirds of the lines of the transmission grid have reached the end of their lifespan of 40 years. [2]

- A growing environmental awareness gives rise to the integration of decentralized and stochastic green energy sources on all voltage levels. On the one hand, this leads to bidirectional power flow between the different voltage levels, and hence to a much more complex power system. And on the other hand, power generation becomes less predictable.

- The energy turnaround in different European countries [6, 7] schedules the substitution of major generation centers by multiple ideally sustainable distributed production units. The overall inertia of the power system, and hence the dynamic stability of the power system, will decrease.

All these facts and changes require a new, more intelligent system that can manage the increasingly complex and unstable power system. The energy community is therefore starting to marry information and communication technology with the electric infrastructure, leading to a two-way flow of electricity and information [8]. Real-time monitoring of everything, from power plants to customer preferences to individual appliances, becomes possible.

Real-time analysis of this huge amount of data is necessary to improve grid reliability and utilization, and hence to guarantee uninterrupted supply. A crucial part of this is therefore the transient stability evaluation, also referred to as dynamic security assessment, of the power system. The main requirement for dynamic stability simulators in this context becomes the simulation time. The simulators have to be able to reproduce power system phenomena much faster than their real-time duration. Currently, such a simulator does not exist. And this is where the present research work comes in. The detailed objectives of this thesis are outlined in the following section.

1.2. Contributions

In this thesis, we develop a power system emulation approach from the theoretical principles to the design and the realization of a first demonstrator. This approach is called the AC emulation approach, and is based on analog emulation of the power grid. Its main objective is to overcome the speed limits of commonly used numerical simulators.

The contributions of this thesis include:

- The development of a method to guarantee the flexibility of analogically implemented power system simulators.

- The proposition of AC emulation, a power system emulation approach which keeps the frequency dependence of the power system signals, and the elaboration of the theoretical background of this approach.

- The development of behavioral AC emulation component models, including their error analysis and their behavioral validation.

- The design of programmable analog building blocks for the implementation of the developed AC emulation component models in a conventional CMOS 0.35μm technology. The foundation of these are blocks laying on classical microelectronic building blocks, but also two blocks specially developed for power system AC emulation:

    1. A tunable floating active inductance. This inductance is able to operate properly despite unsymmetrical operating conditions at its terminals, and includes a special mechanism for emulating short circuits.

    2. A custom miller amplifier containing a supplementary stage in order to duplicate the current at its output.

- The fabrication and testing of the first AC emulation demonstrator dedicated to transient stability analysis being 10'000 times faster than real-time, therefore proving the high-speed capabilities of AC emulation.

1.3. Thesis organization

After the introduction, which sets the general context of this thesis and highlights its contributions, 6 more chapters follow.

We start with **Chapter 2: Power grid emulation**. This chapter presents the principle of power system emulation and highlights its interest by comparison to numerical simulation and by application examples. Furthermore, the modularity issue of power system

emulators is addressed.

Based on this, **Chapter 3**, introduces the **AC emulation approach**. First, we present the basic principle and ultimate scope of this novel power system emulation approach. Second, we outline the specifications of the first demonstrator, and third, we compare our approach and our demonstrator to the state of the art.

Then, the following chapters are dedicated to modeling, implementation and measurement of the first AC emulation demonstrator. The behavioral AC emulation component models are developed in **Chapter 4: Behavioral modeling**. Thereby, the power system theory, which laid the foundation for the development of the AC emulation component models, is also summarized. Systematic errors are analyzed and reduced, before the models are finally validated by behavioral simulations.

Chapter 5, focuses on the microelectronic **implementation** of the developed behavioral models. We start by identifying the application-specific requirements. This leads to adequate topology choices and, where necessary, to the development of dedicated solutions. The design of the different blocks is described from system level to transistor level providing design guidelines. Transistor level simulations validate the developments.

Finally, **Chapter 6** provides and investigates **measurement results** of the realized Application Specific Integrated Circuit (ASIC), which contains the first AC emulation demonstrator. In this way, the theoretical developments, the behavioral modeling and the microelectronic implementation are validated. Moreover, the functionality of each newly developed microelectronic block is verified separately.

The last chapter, **Chapter 7**, summarizes the main findings of this work and provides an outlook on potential follow-up work.

Chapter 2.
2 Power grid emulation

Chapter overview

This chapter introduces the principle of power system emulation. It shows that power system emulation overcomes the speed bottleneck of current numerical power system simulators by bypassing heavy matrix calculations through a quasi-instantaneous analog grid. Moreover, a concept called FPPNS is presented, aiming to keep the flexibility of emulators comparable to the flexibility of numerical simulators. Finally, some applications for faster-than-real-time simulators, based on power grid emulation, are proposed.

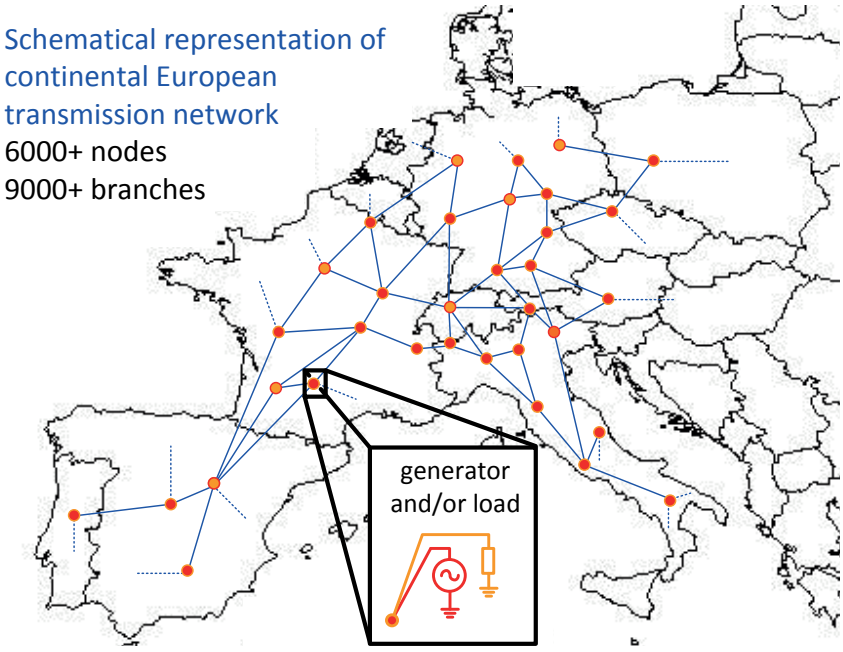


Figure 2.1.: Schematical illustration of continental European Transmission network (numerical values from [9])

2.1. Background and principle

Fig. 2.1 illustrates schematically the main challenge of power system simulators: they have to be able to simulate the behavior of thousands of loads and generators, all interconnected with each other.

Common power system simulators are based on time-consuming numerical algorithms. Indeed, numerical simulation uses the admittance matrix of the power grid in order to link the node voltages to the injected currents that flow in the grid through Kirchhoff equations [10]. Thus, for each time step, heavy matrix calculations have to be completed, i.e. the inversion of the matrix. For a one core processor, the computation time is therefore proportional to the square of the number of nodes of the power system [11]. Moreover, for transient stability simulation in the same time span and for every node, differential algebraic equations (DAE) describing the behavior of the generators and loads have to be computed, further decreasing the computation speed.

In a more abstract way, a power system transient stability simulator can be seen as a solver of multiple sets of Differential Algebraic Equations (DAEs) linked to each other through a huge set of Kirchhoff equations. In terms of speed, a parallel computation architecture is therefore more appropriate than the sequential architecture of conventional computers.

Since the 1960s, extensive and ever continuing research has been done to overcome the

speed bottleneck of numerical simulators using parallel computing hardware. This research has shown that the communication time between the different computers or clusters is the most important limitation in terms of speed [12,13]. Similarly, modern massive parallel hardware architectures, such as multi-core processors and computation platforms on Graphical Processing Units (GPUs) or Field Programmable Gate Arrays (FPGAs), which allow the association of an independent processor or process with each power system component, set of components or bus, additionally suffer from memory access time limitations, due to shared resources. Hence, even if the computation is highly parallelized, the simulation time remains dependent on the number of nodes of the power system [14,15]. However, these parallelization efforts, which were assisted by rapid hardware evolution, have resulted in the release of commercial real-time simulators from, among others, Siemens [16], RTDS Technologies [17] and OPAL-RT [18].

The aim of power system emulation is to further overcome these speed limitations of numerical simulators by avoiding the heavy matrix calculation of the grid. The idea is to use an instantaneous analog Kirchhoff grid and to connect the generator model equation solvers, as well as the load model equation solvers, through this grid. This has the advantage that all the DAE solvers, whether they are implemented analogically or numerically, instantaneously discern the results of the others. The simulation or emulation time becomes independent of the number of nodes, due to this intrinsic parallelism. Faster-than-real-time simulation is easily achieved. Fig. 2.2 illustrates the emulation principle first introduced by R. Fried et al. in [19].

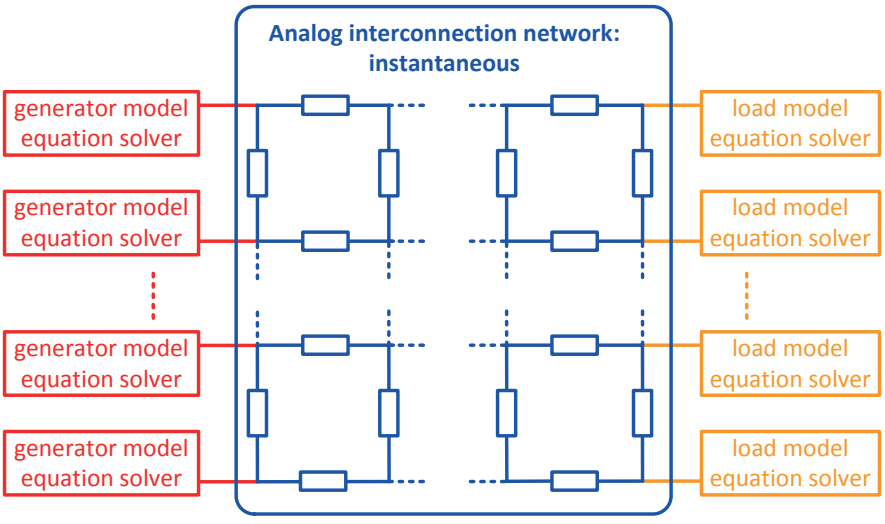


Figure 2.2.: Emulation principle

2.2. Field programmable power network system (FPPNS)

Besides speed, another main consideration for simulators is their modularity. Analog implementations are often seen as too rigid compared to numerical ones. Indeed, in numerical simulators, the topologies, the characteristic of the elements and the models used to characterize the different power system components can simply be changed through the software. No hardware changes are needed.

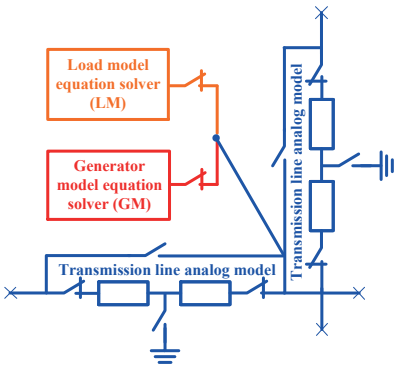
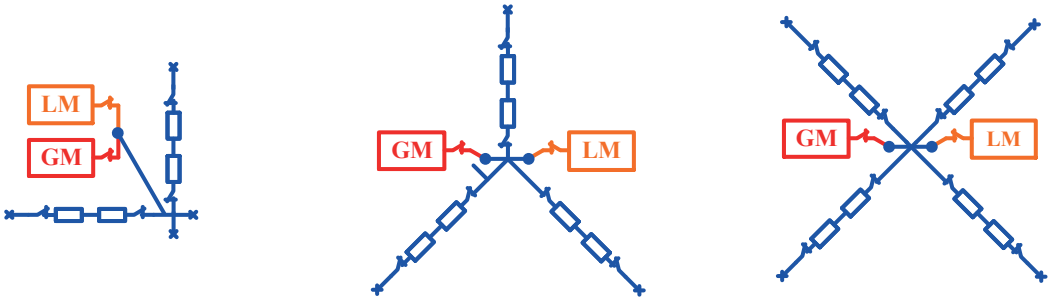


Figure 2.3.: Power System Atom (PSA): the repeatable and reconfigurable FPPNS basic block

In order to enhance the flexibility of analog emulation approaches, we developed and patented a concept called Field Programmable Power Network System (FPPNS) [20, 21]. The concept is based on an array of multiple, repeatable and reconfigurable basic blocks called Power System Atoms (PSAs). Each PSA is composed of the basic elements of a power system. Hence, it contains at least a generator model (GM), a load model (LM) and some analog transmission line models. The analog transmission lines are used to interconnect the atoms. Fig. 2.3 shows in detail a possible PSA topology. Other possible PSA topologies are schematically illustrated in Fig. 2.4. Whereas 2.4(a) offers analog interconnections to 4 neighboring atoms, 2.4(b) offers connections to 6 and 2.4(c) to 8 adjacent atoms.

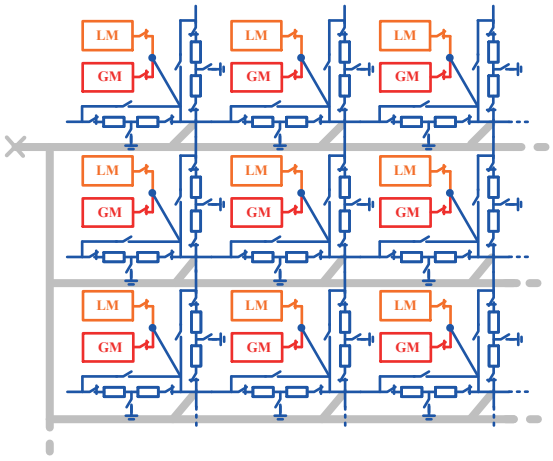


(a) 4 atoms (b) 6 atoms (c) 8 atoms

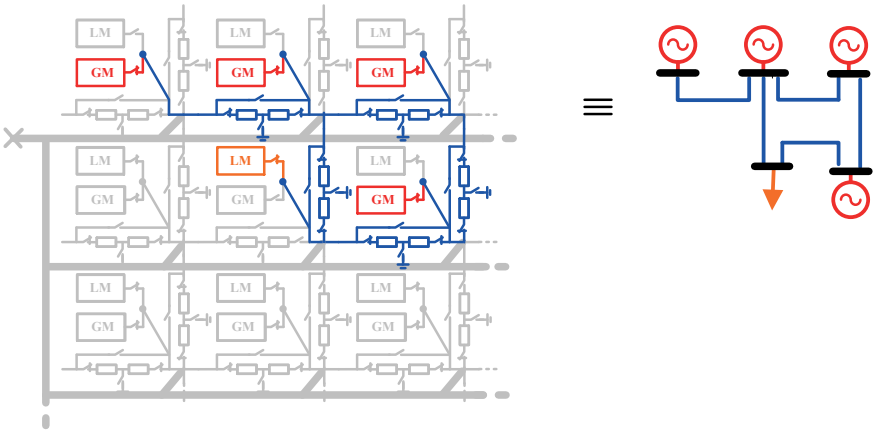
Figure 2.4.: Schematical illustration of possible PSA topologies offering analog interconnections to a different number of neighboring atoms

Each element of a PSA is not only reprogrammable but also equipped with switches. Therefore, it becomes possible to map any power system topology on the array of PSAs as is illustrated in Fig. 2.5. Once the topology is mapped and the element characteristics are programmed, different scenarios can be applied. A digital communication bus is needed to set the topology, to program the component characteristics and to transmit results to the user.

FPPNS makes it possible for the flexibility of analog emulation approaches to become comparable to the flexibility of numerical simulators in terms of the topology and reconfigurability of the elements. The flexibility in terms of models, however, depends entirely on the implementation of the generator and load models. Pure analog implementations are thus more rigid, in terms of models, than mixed-signal implementations.



(a) Unprogrammed FPPNS



(b) Programmed FPPNS

Figure 2.5.: Illustration of reprogrammability through FPPNS: unprogrammed and programmed FPPNS with the digital communication bus indicated in gray

2.3. Emulation vs. simulation

Power system simulators can be classified regarding multiple criteria including **speed**, **precision**, **cost** and **flexibility**. As highlighted in the introduction, speed becomes one of the most important parameters of power system dynamic simulators in the context of real-time control. Section 2.1 explained why numerical simulators are limited in terms of speed, as well as how emulation is overcoming this bottleneck, enabling faster than real-time simulation. The subsequent section, Section 2.2, proposed a concept called FPPNS, to enhance the flexibility of analog emulation approaches. In the past, one of the reasons why analog computation methods were judged inappropriate for power system computation was the lack of flexibility [22]. Finally, in this section, we aim to summarize the strengths and weaknesses of both analog emulation and numerical simulation with respect to the aforementioned criteria. Thereby, two different analog emulation implementations are considered: the purely analog and the mixed-mode implementation.

Numerical power system simulation methods are technologically mature and therefore offer high programmability (in terms of models, topology and component characteristics) and easy operation. Due to the robust computation theory behind numerical simulators, these simulators are very precise (especially compared to analog computation methods). But numerical computation methods run into problems with large non-linear systems. These systems require time-intensive iterative computation methods, such as Newton-Raphson or Gauss-Seidel, and therefore numerical instability and convergence problems can appear, leading to a slow-down of computation and, in the worst case, to no solution. [22,23] The simulation time of numerical simulators is dependent on system size (number of nodes) and model complexity. Even if highly parallelized algorithms and hardware are used, this dependency persists [24].

On the other hand, the emulation time of analog emulators is independent of the system size, due to the intrinsic parallelism of the computation. Faster-than-real-time reproduction of dynamic power system phenomena becomes possible. The high precision of numerical simulators is not reached, as a result of microelectronic imperfections. Nevertheless, accurate results are achieved using calibration techniques.

Purely analog implementations do not suffer from numerical stability issues. The presence of any instability in analog computation signifies inherent instability of the system being studied [23]. Applying the FPPNS concept enables flexibility in terms of topology and component characteristics. Load and generator model modifications, however, are less easy to achieve. In the worst case, a hardware change is necessary to alter these models. Other possibilities include providing PSAs containing more than one generator and load model, or creating FPPNSs containing different PSA-topologies.

Mixed-signal implementations are more flexible than the pure analog implementations. Additionally to the modularity provided by the FPPNS-concept, they allow changing the generator and the load models similarly to a numerical simulator due to the numerical implementation of the generator and load model equation solvers. Computation time

remains, nonetheless, independent of the number of nodes.

On the whole, it can be stated that the main advantage of analog emulators is speed, whereas the main advantage of numerical simulators is precision.

2.4. Applications

In the introduction, we described the recent evolution of power systems, as well as the new challenges that power system operators are confronted with. This section provides further motivation for the development of a high-speed power system emulator by describing their possible applications.

In this scope, let us suppose that a multi-node, faster-than-real-time power system emulator for dynamic phenomena exists.

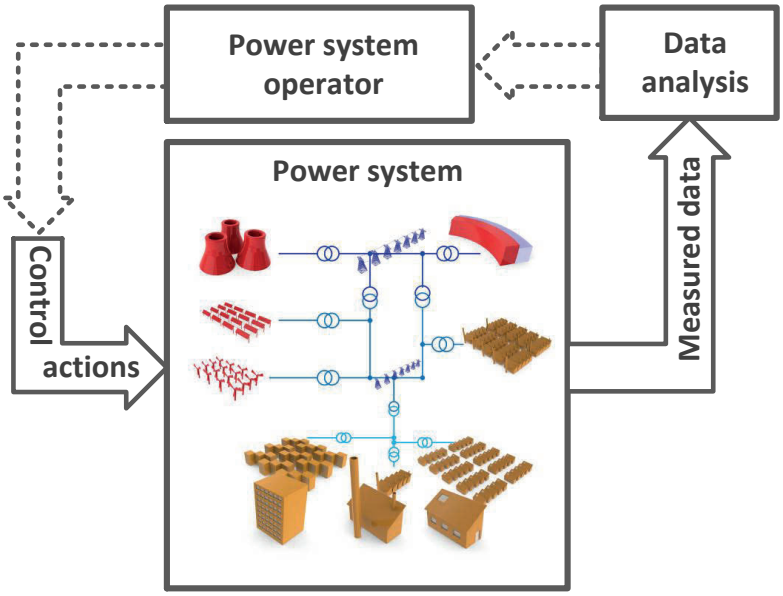


Figure 2.6.: Schematical overview of power system operation

Different applications are possible in the context of **power system operation and control**. Currently, system operators dispatch generation and control circuit breakers and switches. Thereby, they want to reach maximal profitability, guaranteeing at each moment uninterrupted supply for everyone. Conceptually, power system operation is a closed loop process with human intervention (system operators), as illustrated in Fig. 2.6. The information on which the system operators found their decisions is provided by system measurement and analysis. This analysis is currently done by numerical simulators. Due to their speed limits, they can not furnish information during critical moments. The information which is furnished is typically incomplete or, in the worst case, absent.

An example of this is the blackout which occurred in August 2003 in North America. The failure of a state estimator, one of the pieces of information the numerical simulators are able to provide to the system operator in a reasonable amount of time, is one of the leading causes for the outage [23, 25].

Due to their speed advantage, emulators are able to absorb the massive computational efforts specifically related to contingency analysis and dynamic stability, enabling multiple analyses to run while operating the system. For this reason, they can provide more robust power system security analysis, supplying power system operators with better information to control the system.

One can imagine the following analyses:

- **Online security assessment:** Emulators can be employed constantly to screen the overall dynamic security level (robustness to contingencies) of the power system and to prevent critical situations. Thousands of dynamic scenarios can be analyzed constantly and during real-time operation to identify critical states. When the overall state is too insecure, emulators can warn the system operators and propose solutions to reach a more secure, steady state.

- **Real-time problem solving:** If a contingency happens somewhere, the emulators are able to identify immediately whether the fault is critical or not and to indicate how to remediate it.

- **Optimization:** The emulators could help to find the most economical or/and ecological power system state, which still guarantees an acceptable security level. Therefore, online security assessment emulations can be combined with economical and ecological criteria for multi-objective optimization.

Properly applied, this increase of system analyses for real-time operations would allow better power system operation and greater reliability. The integration of green energy sources would be much more secure.

Finally, also in the context of **power system planning**, where simulation time is not of the utmost importance, emulators could be used to improve the efficiency of the precise numerical simulators. Indeed, emulators could be used to determine critical scenarios. These are fully analyzed subsequently, using numerical simulators. In this way, wasting precious computation resources for uncritical scenarios is avoided.

With all these applications, high-speed power system emulators do not aim to replace today's powerful numerical simulators, but rather to complete them.

⋆ ⋆ ⋆ ⋆ ⋆ ⋆

To close this chapter, a very ambitious vision:

As human errors were recognized to be at the origin of the most wide area blackouts [1], it would be even better to aim for closed loop observation and controlling, without the intervention of humans. A very ambitious idea is to distribute emulators in each power system device, and on each power system node to create a system of distributed intelligence, directly acting on the parameters of power system components, devices and switches. Self-control and self-healing of the power system would become reality.

⋆ ⋆ ⋆ ⋆ ⋆ ⋆

3 Chapter 3. AC emulation approach

Chapter overview

This chapter introduces the AC emulation approach, which is based on a one-to-one mapping of the real power system components on an Application Specific Integrated Circuit (ASIC). The ultimate scope, as well as the specifications of the first demonstrator, are outlined. Additionally, the scaling factors are introduced and the speed interest of such fully analog approaches is highlighted. Finally, we compare both the AC emulation approach and its first realization to the state of the art.

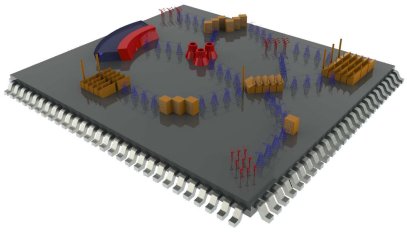


Figure 3.1.: Schematical illustration of the AC emulation idea

3.1. Principle: back to purely analog computation

AC emulation is based on the idea of downscaling the real power system on a microelectronic integrated circuit, as illustrated in Fig. 3.1. The components of the real power system are one-to-one mapped on microelectronics. Corresponding to the principle of emulation introduced in Section 3.1 and illustrated in Fig. 2.2, this means that not only the power grid is emulated but also the loads. Thus, frequency dependence is preserved as the signals propagating on the emulated grid are the shrunk and downscaled current and voltage waves (AC signals) of the real power system. This is the reason why this approach is termed AC emulation.

Theoretically, it becomes possible to simultaneously analyze various types of stabilities with different time constants (dynamic and electromagnetic) after the occurrence of a contingency. Practically of course, this also depends on the models that are implemented, as well as on the limits of microelectronic imperfections such as noise, parasitic elements and nonlinearities.

In order to retain the full advantage gained by conserving the frequency dependence of the signals without restricting speed, purely analog implementation is necessary. A power system simulator based on AC emulation is therefore a custom analog computer.

A brief look at the history of power system stability simulation shows that analog simulation techniques are not a new invention. Indeed, before the emergence of numerical simulation methods in the 1960s, analog simulation methods were predominant [26]. The timeline in Fig. 3.4 illustrates that from about 1920, when the stability of power systems was first recognized as an important problem [27], the methods of power system analysis and the models used were dictated by developments in the art of computation, and by the theory of dynamic systems [28].

The first two entries that appear in the upper-left of the timeline are milestones of the period between 1920 and the early 1930s: it was at this time that theoretical work led to the basic understanding of power system stability phenomena. In 1925 a general approach for solving power system transients involving integration of the system differential

equation was proposed, recognizing the need for machine-aided computation [29]. The right side of the time line shows the computation tools used for power system stability analysis. In the early days, before 1940, simulation was mainly done using mechanical devices able to solve analogically differential equations. Besides these general purpose tools, Vannevaar Bush also developed the network analyzer. Fig. 3.2 shows a part of the MIT network analyzer. In [28], such an analyzer is described as a scaled model of an AC power system with adjustable resistors, reactors and capacitors, used to represent the transmission network and loads. Generators are represented using voltage sources whose magnitude and angle were adjustable. Anywhere in the network there were meters to measure voltages, currents, and power.

Around the 1940s, mechanical analog computers were superseded by analog computers based on vacuum tubes. Before the era of general purpose reliable precision electronic analog computers, there existed dedicated analog computers, which solved specific power system transients [30]. The reign of electronic analog computers was comparably short. Indeed, the interest in analog computers decreased in the 1960s and 1970s as numerical computation became more advanced. With the developments of analog to digital and digital to analog conversion techniques in the second half of the 1960s, there was a period where hybrid computers, making use of the benefits of the analog and numerical computers of that time, were developed. With advances in microelectronics, numerical simulation almost completely supplanted analog and hybrid simulation [26]. Only a few analog or hybrid power system simulators based on the network analyzer and combined with the advances in technology have been developed since then [31, 32]. Even if they are more precise than their precursors, they remain huge and are essentially only used for research and educational purposes.

Figure 3.2.: 3 out of 5 blocks of the MIT network analyzer. Photo reproduced from [33]

The timeline in Fig. 3.4 illustrates that the era of analog computation ended before modern CMOS microelectronic technologies were developed. This evolution brought always more precise modeling of the physical parameters of the Complementary Metal Oxide Semiconductor (CMOS) technology, always smaller feature-size and always less power per circuit, as well as very powerful microelectronic design tools. Moreover, with the reduction of the feature size, the cost also decreased significantly. It became possible to continually realize more complex electronic functions at an ever lower price. On the one hand, this

evolution has strongly influenced the development of numerical computation, which became more and more powerful (i.e. performance improvement and cost reduction). On the other hand, the technical community has hardly considered what advantages modern Very-large-scale integration (VLSI) techniques could pass on to analog computers. Indeed, many of the stated disadvantages in the heyday of analog computers are simply overcome by using VLSI technologies, as outlined below (see also [22]):

Reconfigurability: Classical analog computers were hand-wired through the plugging and unplugging of patch cords and by turning potentiometers to tune gains and time constants. This was tedious and took a considerable amount of time. But this problem does not apply to VLSI analog computers, since programming operations can be controlled automatically through a User Interface (UI) that both sets the states of electronic switches to control the connectivity of the blocks and programs gains and time constants.

User Expertise: Hand-wiring and scaling the parameters in order to match them to the analog computers dynamic ranges required a good user expertise. Today, these operations are automated through the UI, hence less user expertise is needed to handle a VLSI analog computer.

Size: Fig. 3.3 shows an analog computer (the TRIDAC) of 1954 composed of 2000 amplifiers made out of 8'000 vacuum tubes. It is hosted in a special-purpose facility. The same quantity of transistors is nowadays implemented on a few square millimeters. It is hence possible to integrate a large density of functions on one chip substrate. The size of the networks that can be simulated can thus be considerably enhanced.

Cost: Classical analog computers tended to be expensive due to their large number of parts and the significant mechanical assembly needed (see Fig.3.3). VLSI circuits are inexpensive when produced in quantity and electronic assembly costs are low.

Furthermore, the advantages that classical analog computers possessed are also kept by VLSI analog computers:

Speed: Analog computers are inherently parallel and independent of the complexity of the system being simulated. Their speed is determined by the bandwidth of the elements and the time constants of the technology.

Interactivity: Analog simulators are highly interactive because parameters can be changed during the operation.

Mathematical aspects: The presence of any instability in analog computation signifies inherent instability of the system being studied.

Two bottlenecks persist: accuracy and dynamic range limitations. The accuracy of analog computers has been considerably improved since the 1950s. The fact that CMOS models became very precise and that they now use modern calibration techniques, further improve

precision. Nevertheless, numerical computation precision cannot be reached by these improvements alone. This has already been discussed in Chapter 2, where it is shown that the high-speed capabilities of such simulators lead to very promising applications, despite the limited accuracy. The dynamic range of analog computers is limited by noise for small signals and by distortion for big signals. For general purpose analog computers, this aspect is indeed a limiting factor. For dedicated analog computers, as this aspect can be included in the design, it is a minor problem.

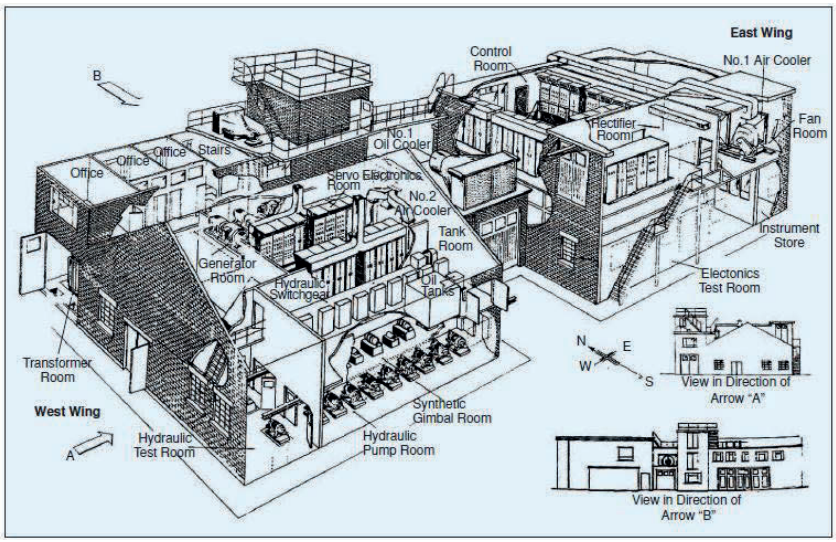


Figure 3.3.: TRIDAC general purpose analog computer housing in its special-purpose facility. Photo reproduced from [30].

All these aspects justify why a renaissance of dedicated analog computation using VLSI technologies is promising for power system stability analysis. The ultimate scope of AC emulation is therefore to create a custom analog computer for high-speed multiple-phenomena-in-one power system analysis. It can be seen as the successor of Vandevaar Bush's network analyzer, miniaturized thanks to modern VLSI technologies and upgraded by the inclusion of analogically solved generator model equations. This new approach allows not only load flows, but also power system dynamics to be solved.

The ultimate AC emulator consists of an ASIC containing a FPPNS composed of a large number of PSAs, which contain the AC emulated power system components. The idea is to set the power system topology under investigation and the system parameters through a UI, which can be a dedicated one or simply a Personal Computer (PC). This information is then converted into the corresponding emulated network parameters and transmitted to the ASIC. Once the initial values are set, the operating point of the network (known as steady state of the power system) is reached automatically and the system is ready to emulate the response of the network to a particular perturbation. Relevant data is then extracted and transmitted to the UI or directly evaluated on chip and communicated to the UI or to power system equipment. Fig. 3.5 shows the working principle of the ultimate AC emulator.

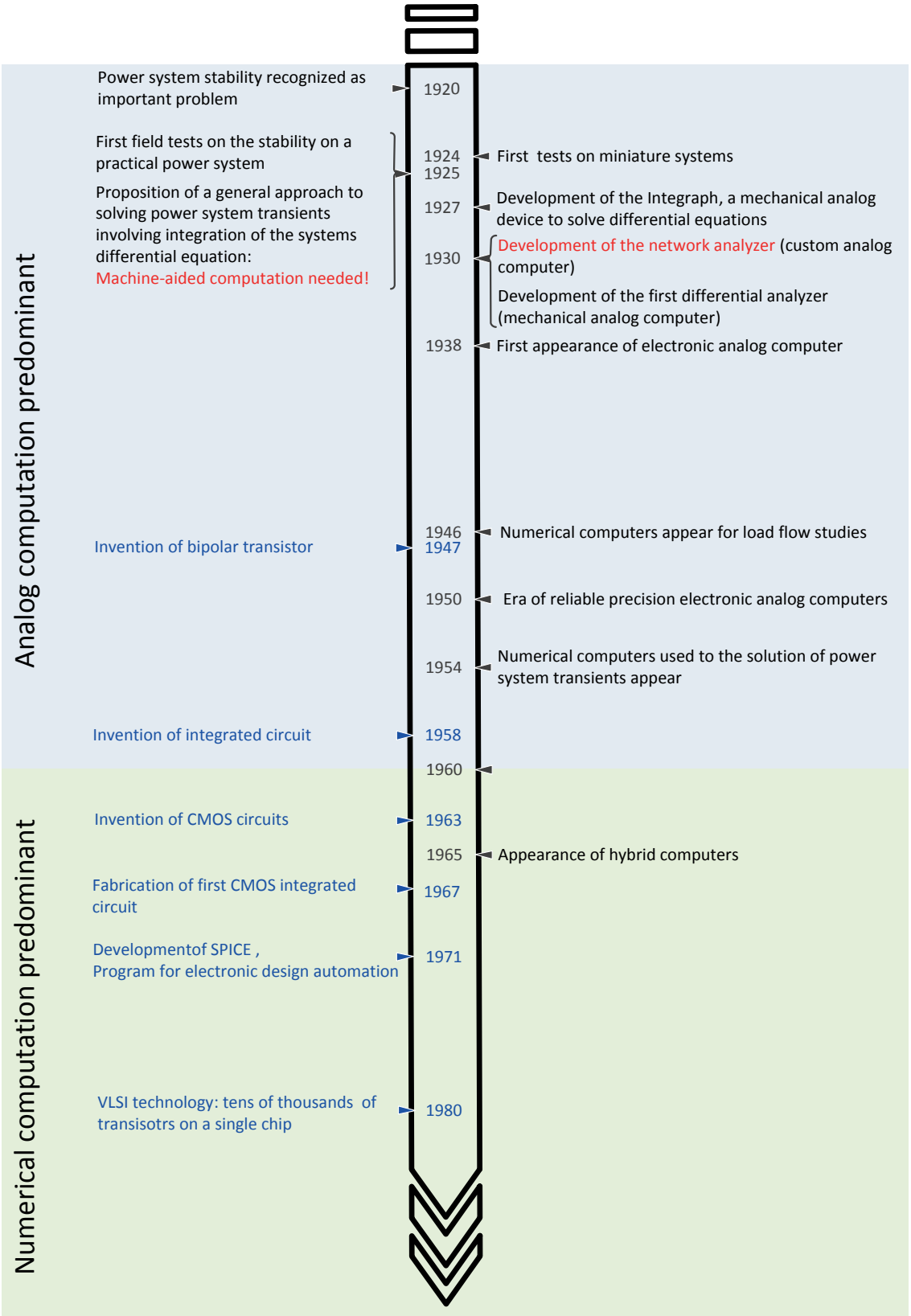


Figure 3.4.: The evolution of power system simulation which goes with the development of the art of computation. In blue the milestones of the evolution of microelectronics.

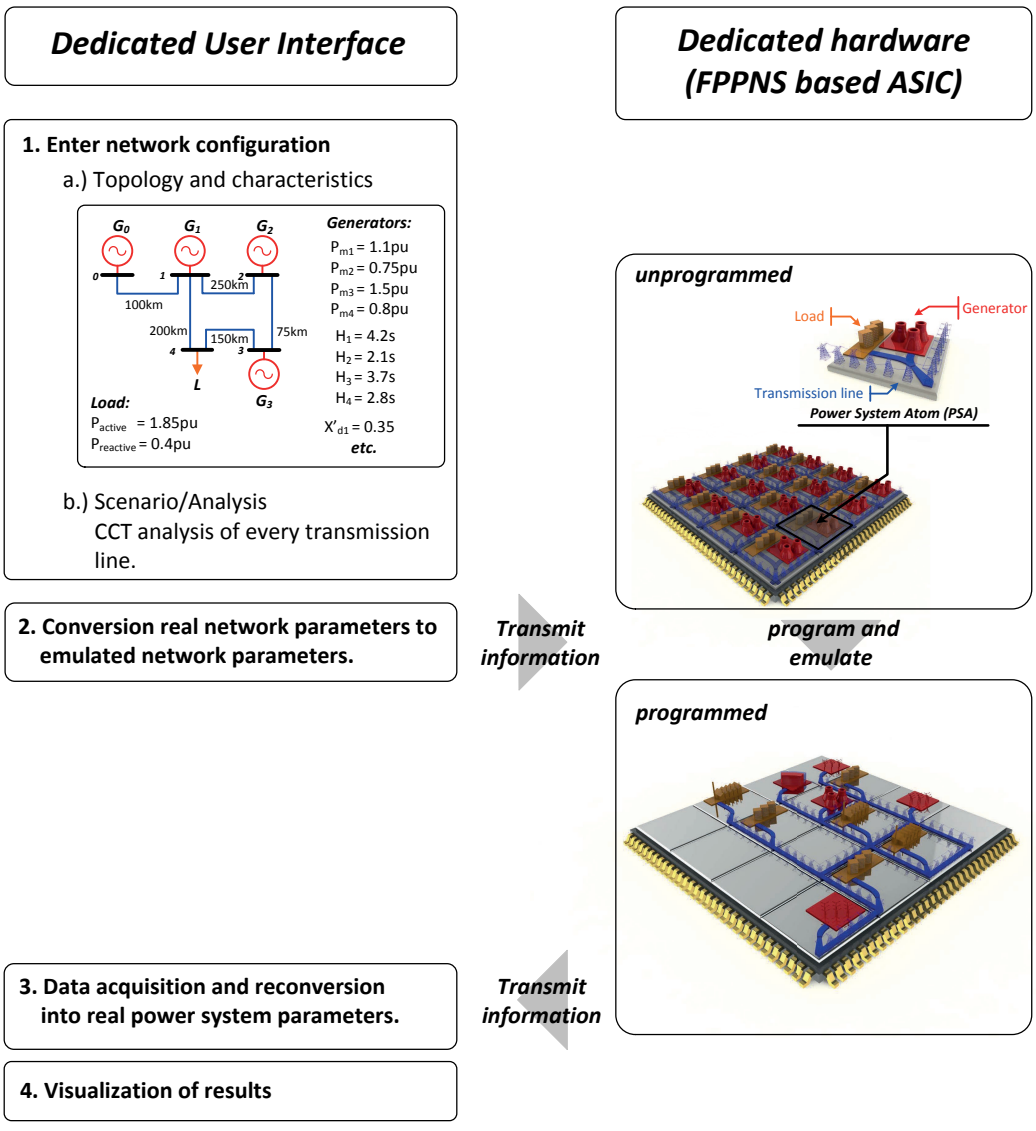


Figure 3.5.: Block diagram of the ultimate AC emulator

3.2. Speed

As explained in Chapter 2, the main interest of power system emulation is the enhanced speed, as compared to current numerical simulators. Speed of AC emulation is determined by the frequency f_{tr} of the AC signals propagating on the emulated grid. Indeed, the emulated power system is working at a much higher frequency f_{tr} than the real power system f_{rps}[1], thus ensuring that the emulated phenomena will be much faster than their real duration. The time scaling factor Ψ, connecting real and emulated time, is defined as follows:

$$\Psi = \frac{f_{tr}}{f_{rps}} \tag{3.1}$$

The higher the operating frequency f_{tr}, the shorter is the emulation time. f_{tr} is determined by the bandwidth of the emulated elements. The speed of AC emulation is therefore limited by the capacitive parasitic effects of the microelectronic technology used.

Note that Ψ describes only the speed-up of emulated phenomenon compared to the real phenomenon. The absolute speed of the emulator compared to real time has to be computed, taking into account setup time and result evaluation time. Eq. (3.2) illustrates the total emulation time. Contrary to the emulation time, the setup time depends on the number of nodes. The results evaluation time also varies, depending on the way the results are evaluated (visually, on-chip etc.).

$$t_{total} = t_{setup}(\#\text{of nodes}) + t_{emulation} + t_{evaluation}(\text{evaluation manner}) \tag{3.2}$$

3.3. Scaling parameters

In addition to the time shrink Ψ, a downscaling also has to be introduced to map the real power system on the emulated microelectronics world. Therefore, the parameters for the voltage, current, impedance and power scaling are defined in Table 3.1 by means of defining the base quantities of the emulated world. As a comparison, typical real-world base quantities are given in the same table.

These parameters are determined by the characteristics of microelectronic implementation, which are, among other characteristics, the chosen CMOS technology, the microelectronic modeling and the imperfections. Moreover, the wished component tuning ranges also influence these values. For the first demonstrator, all these figures are defined in Chapter 5.

[1] Two different frequencies are used all over the world: 50Hz (Europe, Russia, etc.) or 60Hz (Northern America, etc.).

Table 3.1.: Definition of downscaling and time shrink factors

	[p.u.]	real world[a]			emulated world		
$\boldsymbol{U}$	1	U_n	380	kV	k_v	[V]	voltage scaling
$\boldsymbol{I}$	1	I_n	263	A	k_i	[A]	current scaling
$\boldsymbol{S}$	1	S_n	100	MVA	$k_S = k_i \cdot k_v$	[VA]	power scaling
$\boldsymbol{Z}$	1	Z_n	1'444	Ω	$k_Z = \frac{k_v}{k_i}$	[Ω]	impedance scaling
$\boldsymbol{f}$	–	f_{rps}	50	Hz	f_{tr}	[Hz]	transposed frequency

[a] European transmission network figures

3.4. Demonstrator specifications

The first AC emulation demonstrator aims to confirm the high-speed capabilities and the feasibility of this approach. In its first instance, this prototype is restricted only to the study of transient stability. The topology of this first demonstrator is shown in Fig. 3.6. It is a single-machine infinite bus system, thus a fixed topology with reconfigurable component characteristics.

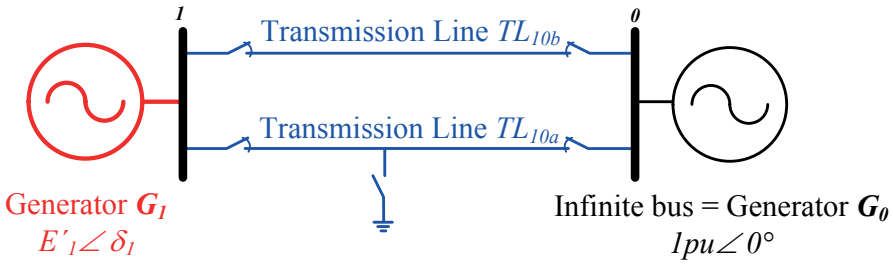


Figure 3.6.: Topology of the first AC emulation demonstrator

This topology allows the emulation of the following scenarios:

- Short circuits at different distances on transmission line TL_{10a}
- The disconnection of transmission line TL_{10a} and/or TL_{10b}

In addition to the feasibility study, this first demonstrator allows the confirmation of the developed models and the investigation of the precision of the microelectronic implementation. In this scope, an attempt is also made to maximize the tuning ranges of the implemented power system components. Note that the topology and the possible phenomena to be emulated are intentionally kept restricted. This allows the confirmation of the feasibility and high-speed capabilities of AC emulation, in the first instance by restricting the analog design challenges. Moreover all other currently developed emulation prototypes are also transient stability emulators. Comparison to other emulation approaches therefore becomes more significant. Readers can refer to Section 3.5 for detailed

information about the state of the art.

Once the feasibility is confirmed, the development can go further in two different ways:

1. Model improvement to allow analyzing several phenomena within the same emulator.

2. Apply the FPPNS concept to AC emulation.

3.5. State of the art

3.5.1. Emulation approaches

Two different emulation approaches exist in literature. On the one hand, there is the AC emulation approach, the subject of this work, which is based on the downscaling and shrinking of the real power system on chip [34]. On the other hand, there is the so-called Phasor emulation approach, formerly also known as DC emulation approach.

Phasor emulation is based on a mathematical abstraction of the grid. It uses the complex representation of electrical variables (i.e. voltage, current and power), which allows a grid composed of π-line models to be mathematically described by multiple, separated resistive networks. Therefore, the Phasor emulation approach is solely dedicated to dynamic phenomena analysis. This includes transient stability, long-term stability and voltage stability analysis. Practically of course, this is for Phasor emulation as well, dependent on the implemented models.

Table 3.2 provides an overview of the two approaches and highlights their differences. The main interest of AC emulation is the kept frequency dependence of the grid signals, which potentially allows the emulation of electromagnetic and dynamic phenomena.

3.5.2. Demonstrators

Different implementations of the two existing power system emulation approaches are currently under development. In addition to the AC emulation demonstrator presented in this work, two different teams, one in Switzerland at the EPFL (L. Fabre et al.) and one in the U.S. at Drexel University (A. Deese, C. O. Nwankpa et al.) are working on Phasor emulation demonstrators.

The very first power system emulator, also a Phasor emulation demonstrator, was presented in 1997 by R. Fried et al., who introduced the principle of power grid emulation. No further improvements are known of this first demonstrator.

Table 3.2.: Phasor emulation approach vs. AC emulation approach

	Phasor emulation approach	AC emulation approach
Principle	Analog implementation of power grid's mathematical abstraction	Downscaling of the real power system on chip
Reason for speed enhancement	Replacing time consuming matrix computation of the grid by instantaneous analog computation	Frequency transposition
Implementations	Purely analog or mixed signal	Purely analog
Phenomena	Dynamic phenomena	Electromagnetic and dynamic phenomena
Signals on emulated grid	Downscaled envelopes of the real power system signals	Downscaled AC signals of the real power system signals

Tables 3.3 and 3.4 summarize the different emulation demonstrators that exist in literature and provide references for more information.

All these demonstrators highlight the high-speed capabilities of power system emulation. The work of L. Fabre et al. is the most advanced. With the first fixed-topology demonstrator, the feasibility of Phasor emulation and the high-speed capabilities of power system emulation have been confirmed. Moreover, it has been shown that the loss in precision compared to purely numerical simulators can be greatly reduced by using advanced calibration techniques [38]. In order to improve the flexibility in terms of topology, a second demonstrator was created. A modular 16-node topology confirming the FPPNS-concept was realized in two versions: a discrete electronics version and an ASIC-based version [39]. At the same time, the feasibility of mixed-signal Phasor emulation implementations was confirmed. Finally, with the 96-node demonstrator, the demonstrator size has been considerably extended. For the first time, it was successfully proven that the accurateness of emulation approaches can be maintained despite a large number of nodes. Aiming to further extend the number of nodes, an ASIC containing 6 analog-grid nodes was realized. This allows the Signal-to-Noise Ratio (SNR) to be further increased, and thus permits a greater possible number of nodes. Results of this ASIC based, 96-node demonstrator will be published in [44]. Changing from a purely analog implementation of Phasor emulation, such as Fried et al. proposed, to a mixed-signal implementation, allowed a high modularity in terms of models to be achieved, but limited the possible speed enhancement.

Deese et al. work with commercially-available Field Programmable Analog Arrays (FPAAs).

Table 3.3.: State of the art of the different analog emulation demonstrators that appear in literature

	Approach	Generator		Grid		Load		Analysis	#-buses	Topology	Speed	Ref
		Models	Impl.	Model	Impl.	Models	Impl.					
L. Fabre et al.	Phasor emulation	Classical model	Mixed-signal, discrete electronics and micro-controller	π-Model, L only	Analog, discrete compo-nents	Constant current model	Analog, discrete electronics	Transient stability	3	Fixed	100x faster[c]	[35–38]
	Phasor emulation	Recon-figurable[a]	Numerical, microcon-troller	π-model, L only	Analog, discrete compo-nents	Recon-figurable	Numerical, microcon-troller	Transient stability	up to 16	Modular	100x faster[d]	[38, 39]
	Phasor emulation	Recon-figurable[a]	Numerical, microcon-troller	π-model, L only	Analog, dedicated integrated hardware	Recon-figurable	Numerical, microcon-troller	Transient stability	up to 16	Modular	100x faster[d]	[40]
	Phasor emulation	Recon-figurable[a]	Numerical, FPGA[b]	π-model, L and C	Analog, discrete compo-nents	Recon-figurable	Numerical, FPGA[b]	Transient stability	up to 96	Modular	1'000x faster[d]	[41]
	Phasor emulation	Recon-figurable[a]	Numerical, FPGA[b]	π-model, L and C	Analog, dedicated integrated hardware	Recon-figurable	Numerical, FPGA[b]	Transient stability	up to 96	Modular	1'000x faster[d]	[41]

[a] Classical model, Park equations, etc.
[b] Field Programmable Gate Array (FPGA)
[c] Emulation time $t_{emulation}$ compared to real time.
[d] Emulation time step compared to a time step of 1ms in real time.

Table 3.4.: State of the art of the different analog emulation demonstrators that appear in literature (cont'd)

	Approach	Generator		Grid		Load		Analysis	#-buses	Topology	Speed[c]	Ref
		Models	Impl.	Model	Impl.	Models	Impl.					
R. Fried et al.	Phasor emulation	Classical model	Analog, dedicated integrated hardware	π-Model, L only	Analog, dedicated integrated hardware	*Not implemented*		Transient stability	2	Fixed topology	10'000x faster	[19]
A. Deese et al.	Phasor emulation	Classical model	Analog, FPAA[b]	π-Model, L only	Analog, FPAA[b]	Exponential recovery model	Analog, FPAA[b]	Transient stability	3	Fixed topology	Real time	[42]
I. Nagel et al.	AC emulation	Classical model	Analog, dedicated partly integrated partly discrete hardware	π-Model, $R(fix)$, $L(var)$, $C(fix)$	Analog, dedicated integrated hardware	*Not implemented*		Transient stability	2	Fixed topology	10'000x faster	[43]

[a] Classical model, Park equations, etc.
[b] Field Programmable Analog Array (FPAA)
[c] Emulation time $t_{emulation}$ compared to real time.

The implementation is therefore purely analog. A 3-bus demonstrator, implemented using 11 FPAA development boards, confirmed the developed models and the promising approach to use FPAA technology. A second demonstrator is under development where the same 3-bus topology is implemented using one Printed Circuit Board (PCB) containing 17 FPAAs. More details can be found in [45]. Using FPAA has the advantage that the development time decreases drastically, as no dedicated microelectronic hardware has to be designed and realized.

Finally, the first AC emulation demonstrator is compared to the state of the art. The main advantage compared to other demonstrators is the speed. Indeed, the developed demonstrator is 10'000 times faster than real time. This is 10 times faster than the most advanced currently developed demonstrators, and this without special speed optimization. All developed demonstrators are limited to transient stability analysis. The current and first AC emulation demonstrator is a fixed-topology demonstrator. The most recent Phasor demonstrators of L. Fabre et al. are much more advanced in terms of modularity. As the FPPNS-concept can also be applied to purely analog AC emulation, this limitation is not a disadvantage of purely analog AC emulation implementation compared to mixed-signal Phasor emulation implementations. It merely highlights a development advance of the Phasor emulation approach.

Nevertheless, it is possible to determine the general advantages and disadvantages of mixed-signal Phasor emulation implementations, as compared to purely analog AC emulation implementations. On the one hand there are the differences between the two emulation approaches, which were already presented in Table 3.2. And on the other hand, there are the distinctions caused by the different implementations, which are listed in Table 3.5.

The table highlights the main advantages of the two implementations. Analog implementations are faster, mixed-signal implementations are more flexible in terms of models. Indeed, the numerical generator and load computation blocks can simply be reprogrammed without any hardware changes. Analog implementations have to deal with the models implemented on the hardware.

Table 3.5.: Mixed-signal Phasor emulation implementation vs. purely analog AC emulation implementation

	Phasor emulation approach Mixed-signal implementation	**AC emulation approach** Purely analog implementation
Speed limiting factor	Loop containing AD conversion, numerical computation stage, DA conversion and the analog emulation time response [46]	Parasitic elements of used microelectronic technology determining the bandwidths
Topology	Modular, if FPPNS-concept is used	Modular, if FPPNS-concept is used
Models	Modular, as generator and load models are implemented by means of easily reprogrammable numerical computation units	Reduced modularity, only models implemented on hardware can be used

Chapter 4.
4 Behavioral modeling

Chapter overview

This chapter is dedicated to AC emulation component modeling. Models of the main power system components, i.e. generator, load and transmission line, are presented. For every component, a short insight into the classical power system modeling is given, which lays the foundation for AC emulation models. The models were developed having microelectronic implementation in mind. Finally, the validity of AC models is confirmed by behavioral simulations.

4.1. Preliminaries

There are many models in power system theory. They differ in their level of abstraction and they also differ based on the phenomena that one wants to analyze. However, all models have in common that they are based on a certain number of assumptions and simplifications. The following development of the AC emulation models for the three main power system components is based on classical power system modeling. Therefore, it is useful to state here the following general assumptions:

- The models are developed with the scope to use them for **transient stability** analysis.

- We suppose **symmetrical three-phase operation** of the power system. Hence, single-phase equivalent circuits can be used, limiting the type of short circuits that can be emulated to symmetrical three-phase short circuits.

The models include the analytical shrink and downscaling factors presented in Table 3.1. In this way, the models remain as general as possible, and are directly customizable to different microelectronic technologies. For their behavioral validation, numerical values for the shrink and downscaling factors have been introduced corresponding to an implementation in a conventional 0.35μm 3.3V CMOS technology. These values are justified and derived in Chapter 5.

4.2. Generator modeling

In this section, the AC generator model development is presented. Downscaling and time shrink parameters are not taken into account until subsection 4.2.4, which introduces them explicitly. Therefore, all variables introduced before this subsection refer to real-world power system values or their equivalent per-unit values.

4.2.1. Theoretical background [28, 47, 48]

Synchronous generators, i.e. practically all generators, are the most important power system components in the analysis of electro-mechanical oscillations in power systems. These oscillations appear when the rotor of the machine does not rotate with constant angular frequency corresponding to the system frequency, but rather is superimposed by low frequency oscillations, typically between 0.1 - 2Hz. If these superimposed oscillations are too large, the stability of the power system can be endangered.

In the following, we give a short insight into the operating principle of a synchronous machine to get a basic understanding of the physical phenomena to be modeled. Going into more detail would go beyond the scope of this thesis. Nevertheless, a lot of literature exists in which a deeper understanding of synchronous machines can be acquired: [28], [47] and [48].

In the synchronous machine, a magnetized rotor creates a rotating magnetic field in the air gap. If the rotor field is ideally sinusoidal, and if the rotor rotates at constant speed, this will induce ideally sinusoidal voltages in the stator windings. If the machine terminals are connected to the grid, the currents flowing in the stator windings create a second rotating magnetic field which causes a torque on the rotor. In a synchronous generator, the magnetic torque opposes the mechanical driving torque of the prime mover.

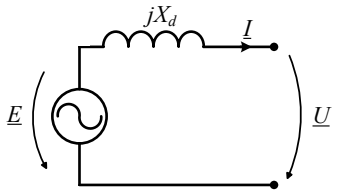


Figure 4.1.: Classical generator model under stationary conditions

In **stationary operation**, i.e. under steady-state conditions, the magnetic torque is equal to the mechanical torque, and so the rotor continues to rotate at a constant speed. The rotor field thus induces sinusoidal voltages in the stator windings that are shifted by 120° with respect to each other. The frequency of the voltages is proportional to the rotor frequency. The magnitude of the voltages depends on both the rotor speed and the magnitude of the rotor field; it can therefore be controlled via the rotor field current.

Assuming the symmetry described above, the generator can be represented by the single-phase equivalent circuit shown in Fig. 4.1. This model is generally known as the Classical Model, the simplest model to represent generators. The induced voltages are modeled by a voltage source $\underline{E}$, $\underline{I}$ is the stator current and $\underline{U}$ is the terminal voltage of the generator. If the losses are neglected, the total impedance of the generator, as seen from the stator, can be modeled with a single lumped inductance X_d. This is strictly only valid for round rotor machines.

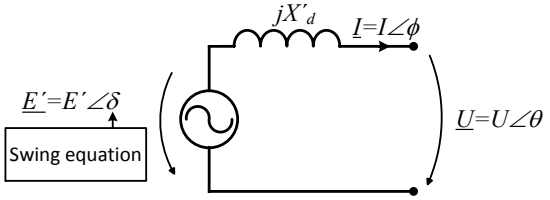


Figure 4.2.: Classical generator model during network transients

During **network transients**, the reactance of the synchronous generator is not constant. For symmetrical transients, the machine reactance itself undergoes transient changes, as the machine passes through the sub-transient, transient and steady-state stages. Due to the fact that electro-mechanical oscillations are quite slow, as mentioned before between 0.1 and 2Hz, the sub-transient state can be ignored and the generator modeled with the transient reactance X'_d. Similarly, during transients, the magnitude of the induced voltage drops to the value E' and can be assumed constant in the first few seconds after a fault, due to a relatively long time constant for changes in the magnetic flux. The generator in transient state is therefore represented as a sinusoidal voltage source $E'\angle\delta$ with a constant magnitude E' behind a reactance X'_d. This model is depicted in Fig. 4.2. The electrical angle δ is governed by a second order ordinary differential equation called a swing equation, which describes the rotor dynamics in the transient state, i.e. when an imbalance between mechanical power P_m fed into the machine and the electrical power P_e extracted from it exists. This equation is as follows:

$$M\frac{d^2\delta}{dt^2} = P_m - P_e \tag{4.1}$$

with M, the inertia factor given by

$$M = \frac{2H}{\omega_0}. \tag{4.2}$$

H is the inertia coefficient and ω_0, the synchronous rotor speed. The mechanical power P_m, i.e. the power from the prime mover, can be considered constant during this transient study, which lasts for only a few seconds. The electric power instead depends on the currents and voltages on the grid, and therefore varies once there are changes.

By introducing $\omega = \dot{\delta}$, the second order differential equation (4.1) can be written as a system of two first order differential equations:

$$\frac{d\delta}{dt} = \omega \tag{4.3}$$

$$\frac{d\omega}{dt} = \frac{\omega_0}{2H}(P_m - P_e) \tag{4.4}$$

This form of the swing equation will be used in the following section to develop the AC emulation generator model. The angular frequency ω introduced in equations 4.3 and 4.4 denotes the relative variation of the rotor speed with respect to ω_0 (i.e. typically $2\pi \cdot$ 50Hz in Europe).

Note that the dynamic model presented here is very simple and neglects a number of features; nevertheless it captures the most important properties needed to model electromechanical oscillations in power systems. Indeed, this model allows the studying of the transient stability of a power system through the observation of the electrical angles δ_i of each generator G_i of the system. The information about the stability of the system is included in the first oscillation after a fault, as the validity of the model is limited to the first 5s after the fault, in which both the internal voltage magnitude E' and the mechanical power P_m can be approximated to be constant.

4.2.2. Adaptation to AC emulation

The centerpiece of the AC emulation approach is the downscaled grid. The AC generator model can therefore be built up on the electronic circuit diagram of the classical generator model shown in Fig. 4.2, which generates a voltage sine waveform to be injected into the grid. The sinusoidal voltage source is implemented as Voltage Controlled Oscillator (VCO). A VCO is a circuit that creates a varying signal (sinusoidal or other) whose angular frequency ω_{out} changes in direct proportion to an input voltage v_{in}. This characteristic permits the electrical angle δ to be governed by the swing equation.

The characteristic of a VCO is illustrated in Fig. 4.3.

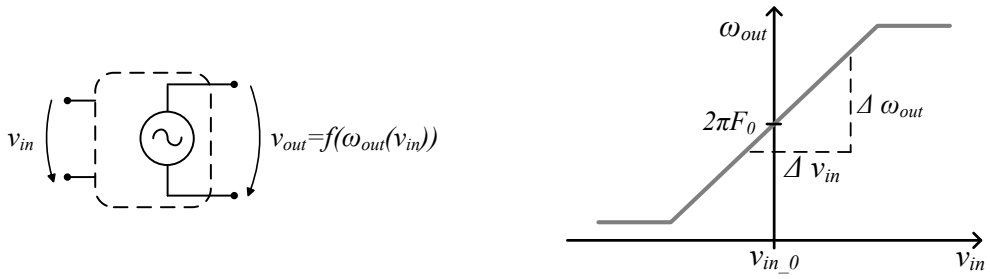
Analytically, its behavior is described by the following equations:

$$\omega_{out}(t) = 2\pi f_{out} = \omega_0 + \omega(t), \tag{4.5}$$

where

$$\omega_0 = 2\pi F_0, \tag{4.6}$$

$$\omega(t) = K_0 v_{in}(t). \tag{4.7}$$



(a) VCO symbol

(b) VCO transfer function

Figure 4.3.: VCO symbol and relationship between input voltage v_{in} and output frequency ω_{out} of the signal generated by the VCO

F_0 is called the center-operating frequency (or free-running frequency) and K_0 the sensitivity of the VCO which is defined as

$$K_0 = \frac{\Delta\omega_{out}}{\Delta v_{in}}. \tag{4.8}$$

Both parameters are illustrated in Fig. 4.3(b).

For modeling, within the scope of this section, we set

$$K_0 = 1 \quad \text{and} \tag{4.9}$$
$$v_{in\_0} = 0. \tag{4.10}$$

v_{in_0} is the VCO input voltage, which leads to the center frequency F_0, as illustrated in Fig. 4.3(b). This choice has no impact on the validity of the modeling, but allows scaling factors to be omitted from this section.

The phase δ_{out} of the varying output signal v_{out} is the integral over time of its angular frequency ω_{out} and can therefore be expressed as

$$\delta_{out}(t) = \int_0^t \omega_{out}(t)\,\mathrm{d}t = \omega_0 t + \underbrace{\int_0^t \omega(t)\,\mathrm{d}t}_{=\delta(t)} = \omega_0 t + \delta(t). \tag{4.11}$$

This equation shows that a VCO solves intrinsically equation (4.3), one of the two equations forming the swing equation. Solving the second equation of the swing equation (4.4) determines the input of the VCO:

$$\omega(t) = \frac{\omega_0}{2H} \int_0^t (P_m - P_e)\,\mathrm{d}t. \tag{4.12}$$

Let us call this equation the reduced swing equation. Contrary to the mechanical power P_m, which is constant and known (as explained in Section 4.2.1), the electrical power P_e is dependent on the grid. Hence, the input needed to solve the reduced swing equation is the electric power P_e, i.e. the active power at the terminal of the generator. Because the signals propagating on the emulated grid of the AC emulation approach are the shrunk and downscaled current and voltage waves of the real power network, and because we are working with a single-phase equivalent circuit, we have direct access only to these instantaneous waveforms at the terminal of the generator.

The sinusoidal voltage generated by the voltage source and the voltage at the terminal of the generator can be described as follows:

$$e'(t) = E' \sin(\omega_0 t + \delta), \tag{4.13}$$
$$u(t) = U \sin(\omega_0 t + \theta). \tag{4.14}$$

Similarly, the sinusoidal current injected in the grid at the terminal of the generator is defined as

$$i(t) = I \sin(\omega_0 t + \phi). \tag{4.15}$$

Hence, only the instantaneous power $p(t)$ at the terminal of the generator, defined as

$$p(t) = i(t)u(t) = i(t)e'(t) = E'I\cos(\delta - \phi) + E'I\cos(2\omega_0 t + \delta + \phi), \tag{4.16}$$

is available quasi-instantaneously by multiplying the current and the voltage sine wave. An additional computation step is needed to get the electric power P_e out of the instantaneous power $p(t)$. Knowing that $i(t)$ and $e'(t)$ are both sine waveforms, the following relationship between P_e ant $p(t)$ holds:

$$P_e = \frac{1}{T} \int_{t-T}^{t} p(t)\,\mathrm{d}t = E'I\cos(\delta - \phi), \tag{4.17}$$

with T, the period of both, the current and the voltage sine wave adequately approximated as

$$T = \frac{2\pi}{\omega_0}. \tag{4.18}$$

Out of this reasoning, the AC generator model shown in Fig. 4.4 was developed. The reduced swing equation solving block is preceded by an electric power computation block, which uses as input the instantaneous current and voltage waveforms, $i(t)$ and $e'(t)$. The output of the reduced swing equation solving block, $\omega(t)$, is the input signal of the VCO. Together, the P_e-computation block and the reduced swing equation block form the feedback loop of the AC emulation generator model. From a microelectronic point of view, damping has to be added to the model for attenuating the oscillations created at power-on of the system. This allows the steady state of the system to be found as fast as possible after the initialization of all parameters.

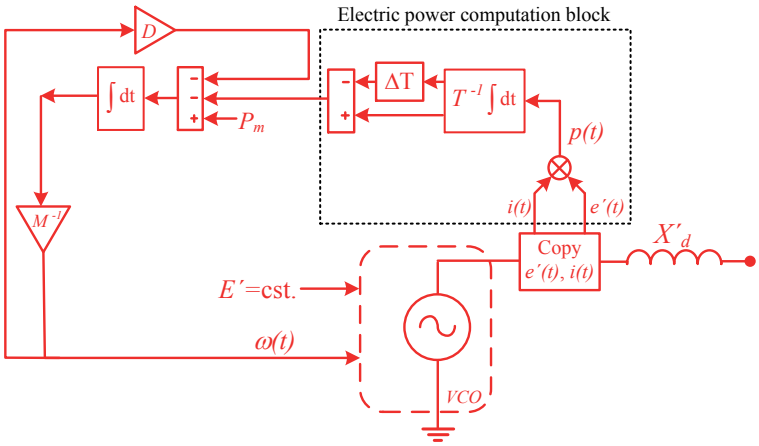


Figure 4.4.: Original AC emulation generator model: The classical generator model as presented in Section 4.2.1 adapted to AC emulation

The analytical analysis of this model shows that instead of solving the swing equation as presented in (4.1), the following equation is solved by the emulated generator model:

$$M\frac{\mathrm{d}^2\delta}{\mathrm{d}t^2} = P_m - \underbrace{\frac{1}{T}\int_{t-T}^{t} p(t)\,\mathrm{d}t}_{=P_e} - P_D. \tag{4.19}$$

Two supplementary elements appear compared to (4.1).

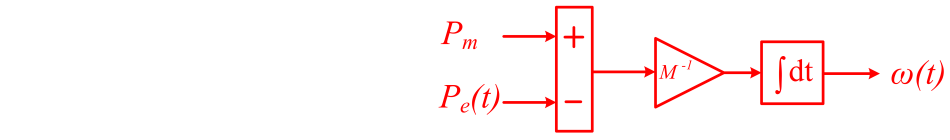
1. The factor P_D represents the damping power. It is proportional to $\omega(t)$ according to the following equation:

$$P_D = D\frac{\mathrm{d}\delta}{\mathrm{d}t} = D\omega(t), \tag{4.20}$$

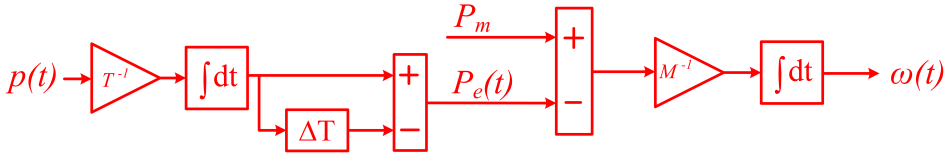
D is called the damping coefficient and is ideally set to zero during emulation, thereby not influencing the emulation results, nor falsifying the model.

2. The second element that appears is the supplementary integration needed to extract P_e, which introduces most notably a delay of at least one period in the feedback loop. The corresponding part is highlighted in Fig. 4.4. This delay does not reflect any reality, and consequently has to be considered as a systematic error.

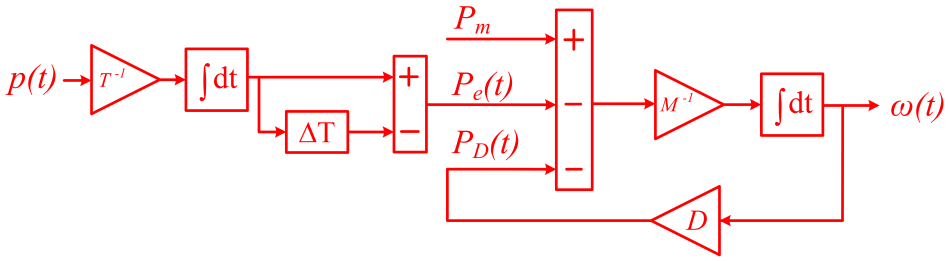
In order to quantify the error introduced by the P_e-computation block, an open-loop characterization of the feedback loop, the ideal and the emulated one has to be performed. As the non-linear sine wave generating unit is the same in all models, it is omitted in the analysis. For analytical calculations, the feedback loops are quantified in the Laplace domain and only the output function is then retranslated back to the time domain. Details of the Laplace domain calculations can be found in Appendix A.



(a) Ideal



(b) Emulated without damping



(c) Emulated with damping

Figure 4.5.: System level of the different opened feedback loops

Therefore, the output of the ideal feedback loop as shown in 4.5(a) is:

$$\omega(t) = \frac{1}{M} \int_0^t (P_m - P_e(\tau)) \mathrm{d}\tau. \tag{4.21}$$

Thus, ideally, the temporal weighting is uniform.

In the original emulated model, where no damping is used, the present moment in time has no influence on the result:

$$\omega(t) = \frac{1}{M}\int_0^t (P_m - \frac{1}{T}(p(t-\tau) - p(t-\tau-T))\tau)\mathrm{d}\tau. \tag{4.22}$$

Indeed, the weighting is linearly increasing towards the past. This unsatisfying behavior is illustrated in Fig. 4.6. A considerable systematic error appears. Mathematically, this error can be reduced by adding damping as illustrated in Fig. 4.5(c):

$$\omega(t) = \frac{1}{MD}P_m(1 - \mathrm{e}^{-\frac{D}{M}t}) - \frac{1}{TD}\int_0^t ((p(t-\tau) - p(t-\tau-T))(1 - \mathrm{e}^{-\frac{D}{M}\tau})\mathrm{d}\tau. \tag{4.23}$$

In this case, the weighting also increases towards the past, but as opposed to the previous case without damping, the error tends towards a constant value. Fig. 4.6 illustrates the weighting toward the past for all three cases.

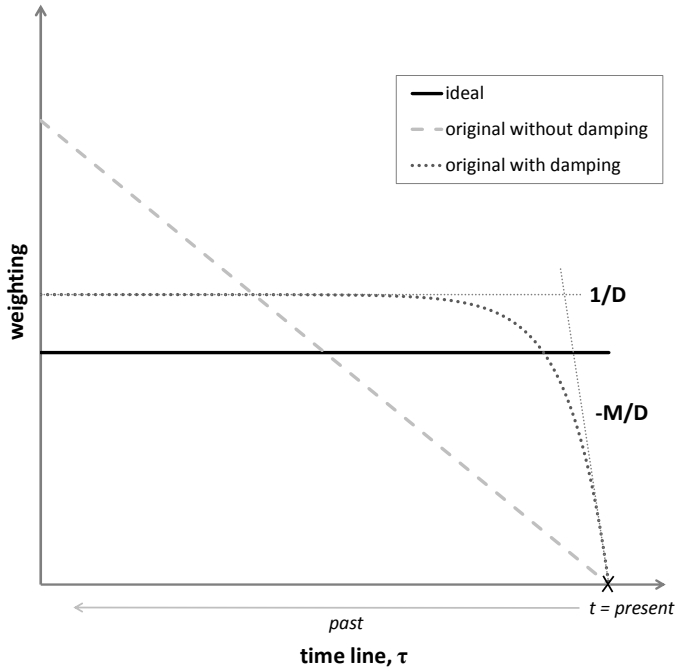


Figure 4.6.: Weighting as calculated in 4.21, 4.22 and 4.23

This analytical analysis emphasizes that keeping a damping factor after a power system fault considerably reduces the systematic error introduced by the P_e-computation block.

An optimal value for D, for which the systematic error is minimal, exists. Nevertheless, with these formulas only an approximate optimal numerical value is obtained, because in a power system, multiple generators are interconnected, thus sharing their errors mutually. Only a qualitative minimization of the error is thus possible, which has to be repeated whenever topology or parameter changes occur. The next section is therefore dedicated to optimizing the error of the original model.

4.2.3. Error optimization

Eq. (4.16) shows that the instantaneous power $p(t)$ is composed by the electric power superposed by a signal that oscillates at twice the frequency of the voltage and current signal. The integration over one period in (4.17) suppresses the oscillating part. The remaining part is the DC component of the instantaneous power. Hence, the instantaneous power already contains the active power as information. Omitting the supplementary integration in the feedback loop would suppress the systematic error described in the previous section. Consequently, the equation that is solved by the emulated generator becomes

$$M\frac{\mathrm{d}^2\delta}{\mathrm{d}t^2} = P_m - p(t) - P_D \tag{4.24}$$

with all the parameters as defined before. Replacing $p(t)$ by (4.16) and supposing no damping, the equation becomes:

$$M\frac{\mathrm{d}\omega(t)}{\mathrm{d}t} = P_m - \underbrace{E'I\cos(\delta-\phi)}_{=P_e} - \underbrace{E'I\cos(2\omega t+\delta+\phi)}_{=\text{ systematic error } e}. \tag{4.25}$$

Obviously a systematic error exists here as well. In order to be coherent, the influence of this error has to be expressed on the output function $\omega(t)$, as done for the original model. In this scope, the systematic error found in (4.25) is integrated, obtaining:

$$\mathrm{e}_{\omega(t)} = \frac{E'I}{M}\frac{1}{2\omega}(\underbrace{\sin(\delta+\phi)}_{\text{constant}} - \underbrace{\sin(2\omega t+\delta+\phi)}_{\text{oscillating}}). \tag{4.26}$$

Both the amplitude of the oscillating part of the error, as well as the frequency independent part of the error, are negligible compared to the useful signal $\omega(t)$, as their values are attenuated by the factor $\frac{1}{2\omega}$ compared to the useful signal.

The optimized model is depicted in Fig. 4.7.

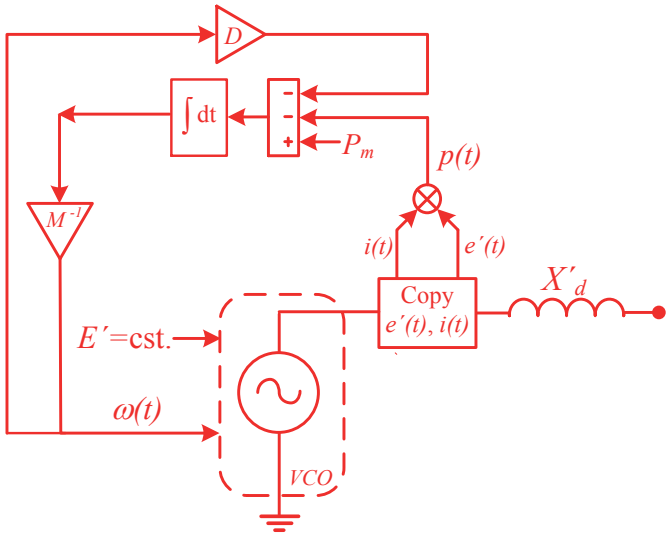


Figure 4.7.: Optimized AC emulation generator model

The following advantages of the optimized model can be stated compared to the full implementation presented in the last section:

- No additional blocks not corresponding to a physical reality are added in the feedback loop.
- The damping power does not have to be used to qualitatively minimize the systematic error caused by the added P_e-computation block. Results become more reliable.
- The systematic error is quantified.
- The solution is certainly stable on the system level. Indeed, as there is only one single integrator, the maximum phase shift at unity gain is $-\frac{\pi}{2}$.

4.2.4. Introducing the scaling parameters and the time shrink into the AC generator model

Sections 3.2 and 3.3 introduce the time shrink Ψ and the downscaling parameters k_v, k_i, k_S and k_Z. These parameters allow miniaturizing the real world on the AC emulated world. Therefore, the current and voltage waves characterizing the generator are:

$$e'_{em}(t) = k_v \cdot E' \sin(\Psi \cdot \omega_0 t + \delta) \tag{4.27}$$

$$i_{em}(t) = k_i \cdot I \sin(\Psi \cdot \omega_0 t + \phi) \tag{4.28}$$

where k_v, k_i and Ψ are the scaling parameters and E', I, ω_0, δ, ϕ are the parameters of the real world sine wave forms as presented in (4.13) and (4.15).

Using these parameters, the emulated swing equation becomes:

$$M \cdot \frac{k_s}{\Psi^2} \frac{\mathrm{d}^2\delta}{\mathrm{d}t^2} = k_s \cdot P_m - i_{em}(t)e'_{em}(t) - P_D. \tag{4.29}$$

Breaking the complete emulated swing equation down to the reduced swing equation and considering all VCO parameters, the optimized model, including all scaling and time shrink factors, can be derived. It is graphically illustrated in Fig. 4.8.

It is obvious that all elements need to be reprogrammable. Moreover, switches are needed for two different reasons:

1. Switch S_G is needed for topology configurations, i.e. to connect or not the generator to a node.

2. Switches S_{SL} permit the feedback loop of the generator to be disconnected in order to configure the generator as slack. Slack generators are modeled as voltage sources with fixed voltage magnitude and phase:

$$E'_{slack} = E'_0$$
$$\delta_{slack} = \delta_0$$

The phase δ_0 is assumed to be the reference angle of the system. Normally, only one slack generator is defined per system.

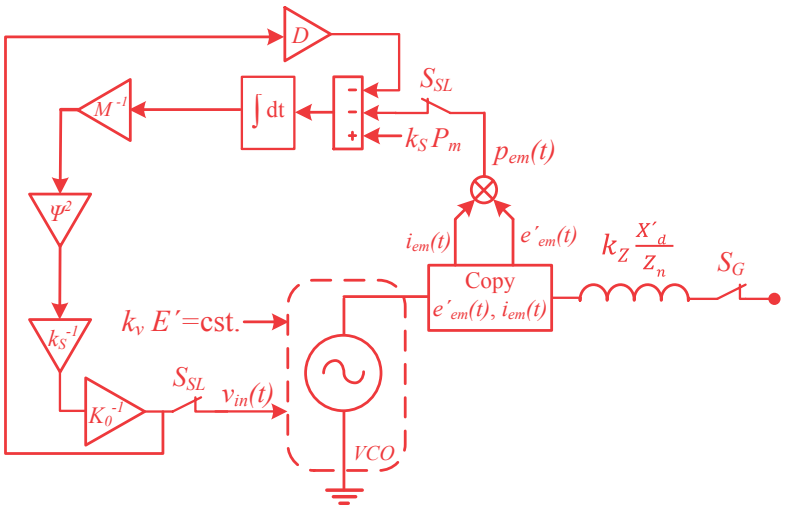


Figure 4.8.: AC generator model with introduced scaling parameters

4.3. Transmission line

4.3.1. Theoretical background [28, 47, 48]

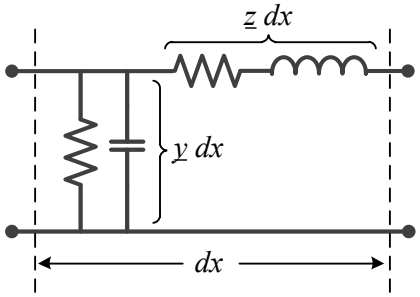


Figure 4.9.: Equivalent circuit of a line element of length dx

A transmission line is characterized by four parameters: series resistances R due to the conductor resistivity, shunt conductance G due to leakage currents between the phase and ground, series inductance L due to magnetic field surrounding the conductor, and shunt capacitance C due to the electric field between the conductors.

Fig. 4.9 shows a single-phase equivalent circuit of an infinitesimal section dx of a transmission line suitable for analyzing its symmetrical three-phase operation. It contains all of the line parameters described above. They are assumed to be uniformly distributed over the line length. Therefore, the parameters describing the circuit are:

$$\begin{aligned} \underline{z} &= R' + j\omega L' = \text{series impedance per unit length per phase} \quad [\Omega/km] \\ \underline{y} &= G' + j\omega C' = \text{shunt conductance per unit length per phase} \quad [S/km] \\ l &= \text{line length} \quad [km] \\ \omega &= 2\pi f \quad [rad/s] \end{aligned}$$

where f is the frequency and R', L', G' and C' the parameters linked to the transmission line behavior as described at the beginning of this section.

Based on the equivalent circuit of Fig. 4.9, the telegraph equations, which consist of a pair of partial differential equations, are obtained. They describe the voltage and the current along the line, dependent on distance and time. By assuming stationary sinusoidal conditions, the long line equations, ordinary differential equations, were obtained. By solving these equations and restricting the interest to the conditions at the ends of the lines, the lumped-circuit line model (π-model), as shown in Fig. 4.10, is obtained. The elements of the equivalent circuit are given by the following expressions:

$$\underline{Z}_{tl} = \underline{Z}_C \sinh(\gamma l) \tag{4.30}$$

$$\frac{\underline{Y}_{tl}}{2} = \frac{1}{\underline{Z}_C} \tanh\left(\frac{\gamma l}{2}\right) \tag{4.31}$$

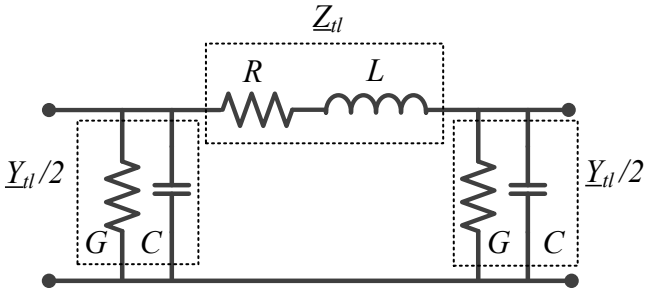


Figure 4.10.: Equivalent π-circuit of a transmission line

where $\underline{Z}_C$ is the characteristic impedance defined as

$$\underline{Z}_C = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \quad [\Omega] \tag{4.32}$$

and γ is the propagation constant specified as

$$\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} \quad \left[\frac{1}{m}\right] \tag{4.33}$$

All parameters where explained before.

If $\gamma l \ll 1$, the expressions for $\underline{Z}_{tl}$ and $\underline{Y}_{tl}$ may be approximated as follows:

$$\underline{Z}_{tl} \approx \underline{z} l \tag{4.34}$$

$$\frac{\underline{Y}_{tl}}{2} \approx \frac{\underline{y} l}{2} \tag{4.35}$$

This approximated model is called a nominal π-equivalent model. Generally, this approximation is good for $l < 300km$ for overhead transmission lines and $l < 100km$ for underground cables, supposing a frequency of 50Hz. Indeed, underground cables are represented by the same equivalent circuit as overhead lines. However, the values of the elements, and hence the characteristics of the cables, differ significantly from those of overhead lines. Table 4.1 lists some typical parameters. Moreover, for typical power lines from about 130kV on, G' is practically 0. The shunt conductance can therefore be approximated by a simple capacitor: $G' + j\omega C' \approx j\omega C'$.

Table 4.1.: Typical overhead transmission line and cable parameters for any nominal voltage

type	overhead lines [49]		cables [28]	
R'	0.01 - 2	[Ω/km]	0.01- 0.06	[Ω/km]
$\omega L'$	0.3 - 0.7	[Ω/km]	0.06 - 0.35	[Ω/km]
$\omega C'$	1.8 - 4.5	[μS/km]	9 - 300	[μS/km]

Finally, overhead line models can be classified according to the line length, based on the approximations justified in their modeling.

Short lines Lines shorter than 100km have negligible shunt capacitance, and may therefore be represented by their series impedance $\underline{Z}_{tl} = R'l + j\omega L'l = R + j\omega L$.

Medium-length lines Lines with lengths in the range of 100km to about 300km may be represented by the nominal π-model and the corresponding equations (4.34) and (4.35).

Long Lines In the case of lines longer than 300km, the distributed effects of the parameters are significant. They need to be represented by the normal π-model described by equations (4.30) and (4.31). Alternatively, they may be represented by cascaded sections of shorter line lengths, with each section represented by a nominal π-equivalent model.

Detailed derivations from the telegraph equations to the π-model can be found in standard books on power systems such as [28].

4.3.2. Adaptation to AC emulation

As the base of the AC transmission line model, the π-equivalent model (see Fig. 4.10), neglecting the shunt conductance G, is taken. According to the theoretical explanations given in the previous section, care has to be taken in the way of computing the element values of the model. In order to be able to create short-circuits at any distance from a node, two of these π-models are connected in series, with a switch S_{sc} to ground in their middle. Fig. 4.11 shows this configuration. The switches S_{tl} have two functions:

1. Together with nS_{tl}, they are used to configure the topology, i.e. to connect or not the corresponding transmission line.

2. They are used to emulate line dis- and re- connections.

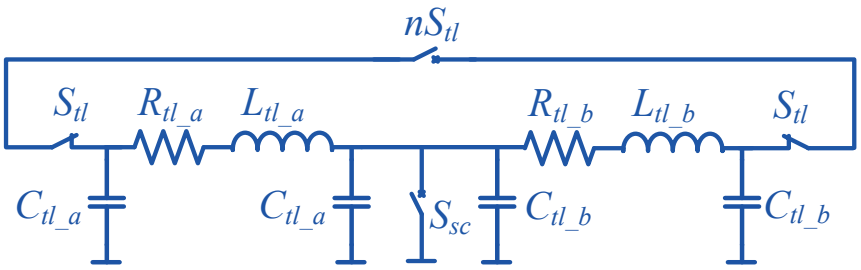


Figure 4.11.: Transmission line model adapted to AC emulation

All element values are programmable. Supposing a short-circuit at x% of the transmission line, the element values R_{tl_a}, L_{tl_a}, C_{tl_a}, R_{tl_b}, L_{tl_b} and C_{tl_a} of the AC transmisison line are computed according to the following equations:

$$R_{tl\_a} = \frac{x}{100}\ k_Z\ \frac{R'\,l}{Z_n} \tag{4.36}$$

$$L_{tl\_a} = \frac{x}{100}\ \frac{k_Z}{2\pi f_{tr}}\ \frac{\omega L'\,l}{Z_n} \tag{4.37}$$

$$C_{tl\_}a = \frac{x}{100}\ \frac{1}{2\pi f_{tr}\,k_Z}\ (2\,\omega C'\,l\,Z_n) \tag{4.38}$$

$$R_{tl\_b} = \left(1 - \frac{x}{100}\right)\ k_Z \frac{R'\,l}{Z_n} \tag{4.39}$$

$$L_{tl\_b} = \left(1 - \frac{x}{100}\right)\ \frac{k_Z}{2\pi f_{tr}}\ \frac{\omega L'\,l}{Z_n} \tag{4.40}$$

$$C_{tl\_}b = \left(1 - \frac{x}{100}\right)\ \frac{1}{2\pi f_{tr}\,k_Z}\ (2\,\omega C'\,l\,Z_n) \tag{4.41}$$

K_Z and f_{tr} are emulated-world parameters, as defined in Table 3.1. Z_n is the real-world impedance base value quantity defined in the same table. R', $\omega L'$ and $\omega C'$ are the real distributed line parameters per unit length and phase, as defined in the previous section.

4.4. Load

4.4.1. Theoretical background [28, 47, 49–51]

Each aggregated load represents a relatively large fragment of the system, typically comprising low and medium voltage distribution networks, small power sources operating at distribution levels, reactive power compensators, distribution voltage regulators etc. and including a large number of different component loads such as motors, lighting, heaters, and electrical appliances. The exact composition of an aggregated load is difficult to estimate. Also, the composition changes depending on many factors, including time (hour, day, season), weather conditions and the state of the economy. Determining simple and valid aggregated load models is therefore not an easy problem, and is still the subject of intensive research.

Component load characteristics can traditionally be divided into two broad categories:

Static load The active and the reactive power drawn by the load are, at any moment in time, an algebraic function of the bus voltage magnitude and frequency at the same instant.

Lighting and heating are examples of this.

Dynamic load Loads whose responses to voltage or frequency disturbances do not occur instantaneously, but require some time. They tend to recover to, or close to, their original level, following changes in voltage and frequency within a certain range. Instantaneously, they behave as static loads; the recovery is governed by the overall time constants, depending on the type of load. Mathematically, such behavior is described by differential equations.

Motor loads are an example.

Most commonly, an aggregated load contains both types of component loads. For modest amplitudes of voltage/frequency changes, the response of most aggregated loads is fast, and the steady state of the response is reached very quickly. Hence, the use of static load models is justified. This is the case for conventional rotor angle (large and small disturbance) stability analyses, in which the frequency variations rarely overstep ± 1 Hz. Hence, traditionally static load models were taken.

However, there are many cases where it is necessary to account for the dynamics of load components. Studies of inter-area oscillations, voltages stability and long-term stability often require load dynamics to be modeled. Moreover, the study of systems with large concentrations of motors also requires the representation of load dynamics. Typically, motors consume 60 to 70% of the total energy supplied by a power system [28]. Therefore, the dynamics attributable to motors are usually the most significant aspects of dynamic

characteristics of system loads.

A load model is a mathematical representation of the relationship between a bus voltage (magnitude and frequency) and the power (active (P) and reactive (Q)) or current flowing into the bus load. The simplest load models are static load models:

Constant current load model The power varies directly with the voltage magnitude. This is a reasonable representation of the real power demand of a mix of resistive and motor devices.

Constant power load model The power remains constant, independent of the voltage magnitude variation. This model allows loads with a stiff voltage characteristic to be represented, and is often used in load-flow calculations.

Constant impedance load model The power varies directly with the square of the voltage magnitude. With this model, some lighting loads are well-represented.

To obtain more general voltage characteristics, the benefit of each of the models presented above can be combined by using the so-called **polynomial or ZIP model**, consisting of the weighted sum of constant impedance (Z), constant current (I) and constant power (P), multiplied by a frequency dependent term. However, this model has no physical correspondence.

Another general static load model where the frequency dependence is also included is called the **exponential load model** and is described as follows:

$$P = P_0 \left(\frac{U}{U_0}\right)^{\alpha} \left(\frac{f}{f_0}\right)^{\beta} \tag{4.42}$$

$$Q = Q_0 \left(\frac{U}{U_0}\right)^{\lambda} \left(\frac{f}{f_0}\right)^{\tau} \tag{4.43}$$

where P and Q are active and reactive components of the load when the bus voltage magnitude is U and the frequency is f. The subscript $_0$ identifies the values of the respective variables at the initial operating condition. The parameters of this model are the exponents α, β, λ and τ. Note that by setting the exponents to the corresponding values, the constant impedance ($\alpha = 2$, $\beta = 0$, $\lambda = 2$, $\tau = 0$), constant power ($\alpha = 0$, $\beta = 0$, $\lambda = 0$, $\tau = 0$) and constant current ($\alpha = 1$, $\beta = 0$, $\lambda = 1$, $\tau = 0$) models are obtained.

In the absence of any detailed information on the aggregated load composition, the real power part is usually represented by the constant current model, while the reactive power is represented by a constant impedance [47]. In the case that the bus voltages drop too low, the static model in use is replaced by a constant impedance model.

As mentioned before, in a typical power system, up to 70% of the loads served may be motor loads, and of these, the majority would be induction motors. Detailed developments, similar to the generator model development, can be found in basic power system

books [28, 47, 50]. The equivalent circuit representing the transient behavior of an induction motor is equal to the generator model shown in Fig. 4.2 with an obvious sign change.

In [50] it is pointed out that the induction motor model, with appropriate parameter values, can faithfully represent any aggregated dynamic load, for both angle and voltage stability studies. The selection of the right parameter values may, however, present some challenges.

4.4.2. Adaptation to AC emulation

Within numerical simulation, the frequency information is often approximated by using the average system frequency. Otherwise it must be computed through the voltage angle on the bus. AC emulation instead contains this information in the AC signals on the grid. It is therefore straight-forward to implement a frequency dependent **dynamic** model composed of passive elements. Fig. 4.12 illustrates the AC emulation load model, also containing all switches to keep maximum possible modularity.

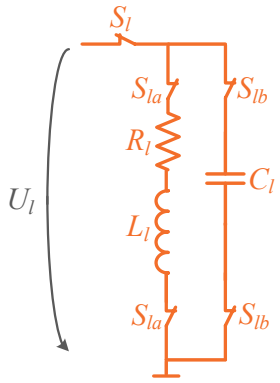


Figure 4.12.: Load model adapted to AC emulation

The switches S_{la} and S_{lb} allow the load to be configured as follows:

- As RL-impedance inspired by the inductive motor load model. The AC model parameter values are set using the following formulas:

$$P_l = \frac{1}{k_S} \frac{R_l}{R_l^2 + (\omega L_l)^2} \cdot U_l^2 \tag{4.44}$$

$$Q_l = \frac{1}{k_S} \frac{\omega L_l}{R_l^2 + (\omega L_l)^2} \cdot U_l^2 \tag{4.45}$$

  The active and reactive power, P_l and Q_l, of the load are expressed in p.u., k_S is the emulated-world power base quantity (see Table 3.1) and U_l is the magnitude of the load bus voltage.

- As $RL//C$-impedance. Active and reactive power parts depend on the values of R_l, L_l and C_l. Capacitive, resistive and inductive effects can be emulated. There is an additional degree of freedom as compared to the simple RL-series load. The AC model parameter values are set through the following formulas:

$$P_l = \frac{1}{k_S} \frac{R_l}{R_l^2 + (\omega L_l)^2} \cdot U_l^2 \tag{4.46}$$

$$Q_l = \frac{1}{k_S} \frac{\omega L_l - \omega C_l R^2 - \omega^3 L_l^2 C}{R_l^2 + (\omega L_l)^2} \cdot U_l^2 \tag{4.47}$$

  P_l and Q_l are expressed in p.u..

- As C. Then the load is used to compensate the reactive power in the system and the AC element value is set by

$$P_l = 0 \tag{4.48}$$

$$Q_l = -\frac{1}{k_S} \omega C_l \cdot U_l^2 \tag{4.49}$$

  P_l and Q_l are expressed in p.u..

The switch S_l is used to configure the topology (connect or not connect the load to the corresponding bus), and to emulate load disconnections or shedding. Moreover, the analog type of simulation permits continuous and discontinuous variation of the load value during an analysis. Dynamic or discontinuous behavior of the aggregated load can therefore also be represented using this straight-forward model.

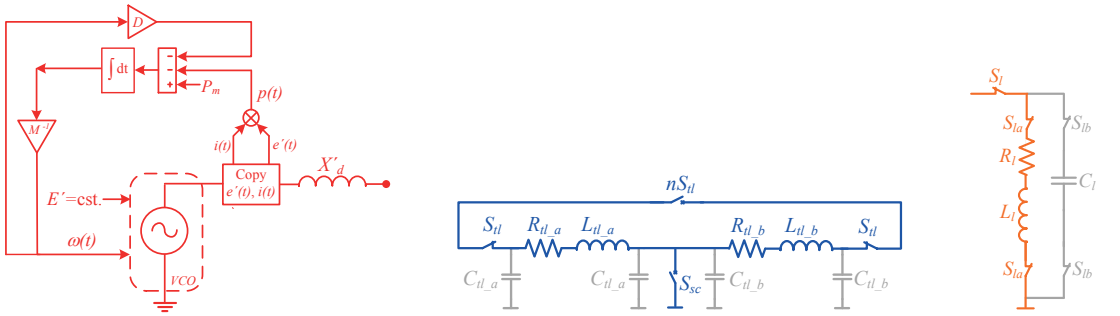
4.5. Behavioral validation

4.5.1. Description of the simulation method

All behavioral simulations are performed in the Cadence IC-Virtuoso environment. The simulator used is Spectre [52]. This allows the simulation of power system topologies with the electronic models of the transmission lines and the load in combination with the purely behavioral optimized generator model. These models are remembered and referenced in Fig. 4.13. Table 4.2 gives the shrink and downscaling factors used for the behavioral emulation. The distributed line parameters used are:

$$\begin{aligned} R' &= 0.03 \quad [\Omega/\text{km}] \\ \omega L' &= 0.7 \quad [\Omega/\text{km}] \\ \omega C' &= 3.14 \quad [\mu S/\text{km}] \end{aligned}$$

The obtained results are compared to the results of a numerical simulator implemented in LabView. The validation of this numerical reference simulator by comparison, on the one hand, to an example presented in [10], and on the other hand, to EUROSTAG [53] can be found in Appendix B. Note that the results are presented either in real-world values or in emulated-world values. The abbreviations (rw) and (ew) respectively are used to indicate in which world the results are given. The speed enhancement of AC emulation is therefore not visible when the obtained results are converted into real-world values for comparison.



(a) AC generator model

(b) AC transmission line model

(c) AC load model

Figure 4.13.: Reminder of the AC models validated in this section and developed in the previous sections: generator in Section 4.2.2, transmission line in Section 4.3.2 and load in Section 4.4.2. The gray parts of the models are omitted.

4.5.2. 4-bus topology reference scenario

We have chosen a 4-bus topology to validate the behavioral models developed throughout this chapter. This topology contains the three main power system components, and is

Table 4.2.: Time shrink and scaling factors used for behavioral validation of the models

	[p.u.]	real world			emulated world		
$\boldsymbol{U}$	1	U_n	380	kV	k_v	80	mV
$\boldsymbol{I}$	1	I_n	263	A	k_i	4	μA
$\boldsymbol{S}$	1	S_n	100	MVA	k_S	320	nVA
$\boldsymbol{Z}$	1	Z_n	1'444	Ω	k_Z	20	kΩ
$\boldsymbol{f}$	–	f_{rps}	50	Hz	f_{tr}	500	kHz

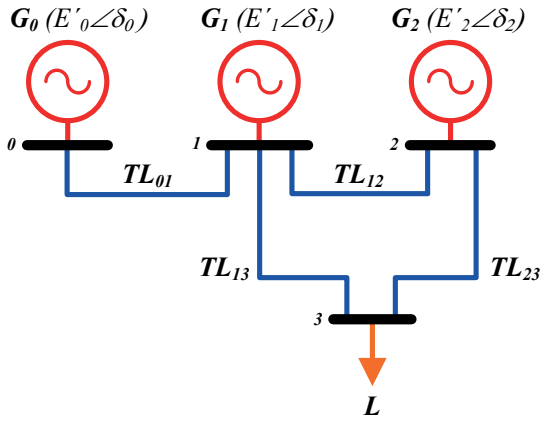


Figure 4.14.: Reference topology used for validating the behavioral AC models

depicted in Fig. 4.14. The used real-world characteristics of its elements are listed in Table 4.3. The emulated-world parameters are obtained by means of Table 4.2 and the formulas given in Sections 4.4.2, 4.3.2 and 4.2.4. We use relatively long transmission lines so as to have significant oscillations for comparison. However, this does not necessarily correspond to real transmission systems.

The reference scenario selected for the validation is as shown in Fig. 4.15. A time t_{sc} after setting off the emulator, a short circuit is applied at x% of transmission line TL_{23} between Generator G_2 and Load L. A certain time t_{clr} later, the whole line is disconnected.

Note the following parameter definitions:

t_{sc} : moment in time where the short circuit starts
t_{dsc} : short circuit duration
t_{clr} : moment in time where the short circuit is cleared by reconnection or disconnection of the concerned transmission line
CCT : Critical Clearing Time is defined as the longest possible short circuit on a transmission line before the power system loses its stability.

Table 4.3.: Real-world characteristics of the reference topology

	Parameter		Value	Unit
Generator 0	E'_0	Internal voltage	1	[p.u.]
G_0	δ_0	Electrical angle	0	[deg]
Generator 1	P_1	Active power	0.7	[p.u.]
G_1	Q_1	Reactive power	0.25	[p.u.]
	H_1	Inertia	4.2	[s]
	X'_{d1}	Internal impedance	0.35	[p.u.]
	E'_1	Internal voltage	1.114	[p.u.]
Generator 2	P_2	Active power	1.1	[p.u.]
G_2	Q_2	Reactive power	0.4	[p.u.]
	H_2	Inertia	2.1	[s]
	X'_{d2}	Internal impedance	0.3	[p.u.]
	E'_2	Internal voltage	1.164	[p.u.]
Load	P_l	Active power	1.85	[p.u.]
L	Q_l	Reactive power	0.4	[p.u.]
Line TL_{01}	L_{01}	Reactance	0.1	[p.u.]
200km	R_{01}	Resistance	0.004	[p.u.]
Line TL_{12}	L_{12}	Reactance	0.18	[p.u.]
370km	R_{12}	Resistance	0.0077	[p.u.]
Line TL_{13}	L_{13}	Reactance	0.2	[p.u.]
400km	R_{13}	Resistance	0.0083	[p.u.]
Line TL_{23}	L_{23}	Reactance	0.1	[p.u.]
200km	R_{23}	Resistance	0.004	[p.u.]

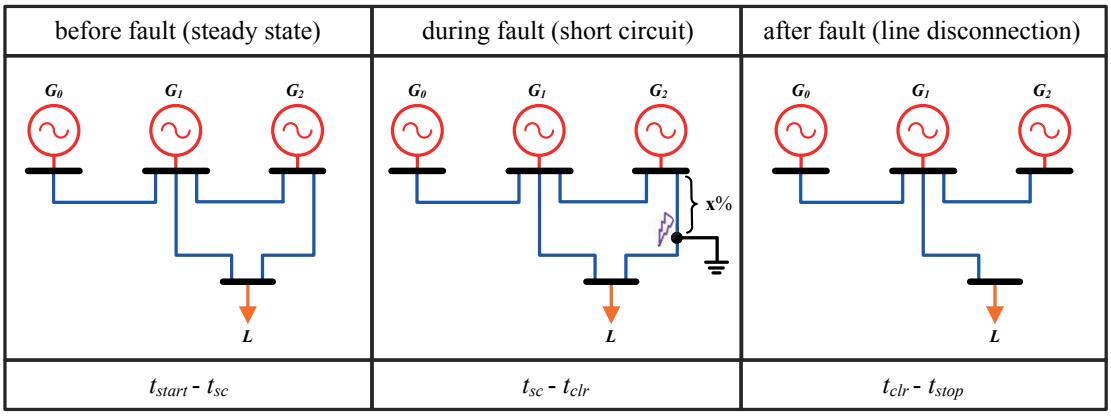


Figure 4.15.: Reference scenario

Three different aspects are validated:

Emulation vs. simulation The behavioral emulation results are compared to numerical simulation results by comparing the behavior of the electrical angles δ_1 and δ_2.

Generator models The original generator model with and without damping is compared to the optimized model. The developments made in Section 4.2 are validated.

Critical Clearing Time The CCT simulation and emulation results are compared at different short-circuit locations on line TL_{23}. Thereby, the influence of the moment in time of the short circuit is discussed.

1st comparison: emulation vs. simulation

Before comparing emulated results to simulated results, the signals propagating in the emulator are analyzed. As such, they are not retransposed to real-world values. Fig. 4.16 and 4.18 show the emulated generator signals after a short circuit at t_{sc}=1.5052s of t_{dsc}=70ms and at 50% of line TL_{23} in the scenario described above. At the beginning of the emulation, a certain time is necessary to converge to the steady state values of the system. In order to force fast convergence, damping is used. The damping factor D of the optimized generator model (see Fig. 4.7) is set to a high value until the steady state is reached. Then, its value is set to 0 and the emulation of the scenario can start.

A zoom on the emulated generator signals (see Fig. 4.17 and 4.19) shows the particularity of AC emulation: the sinusoidal current and voltage AC signals. Moreover, the negligible systematic error of the generator model also becomes partially visible in the ω_1 and ω_2 curves. Indeed, the offset during the steady state is too small to be seen, but the oscillating part of the systematic error is clearly visible.

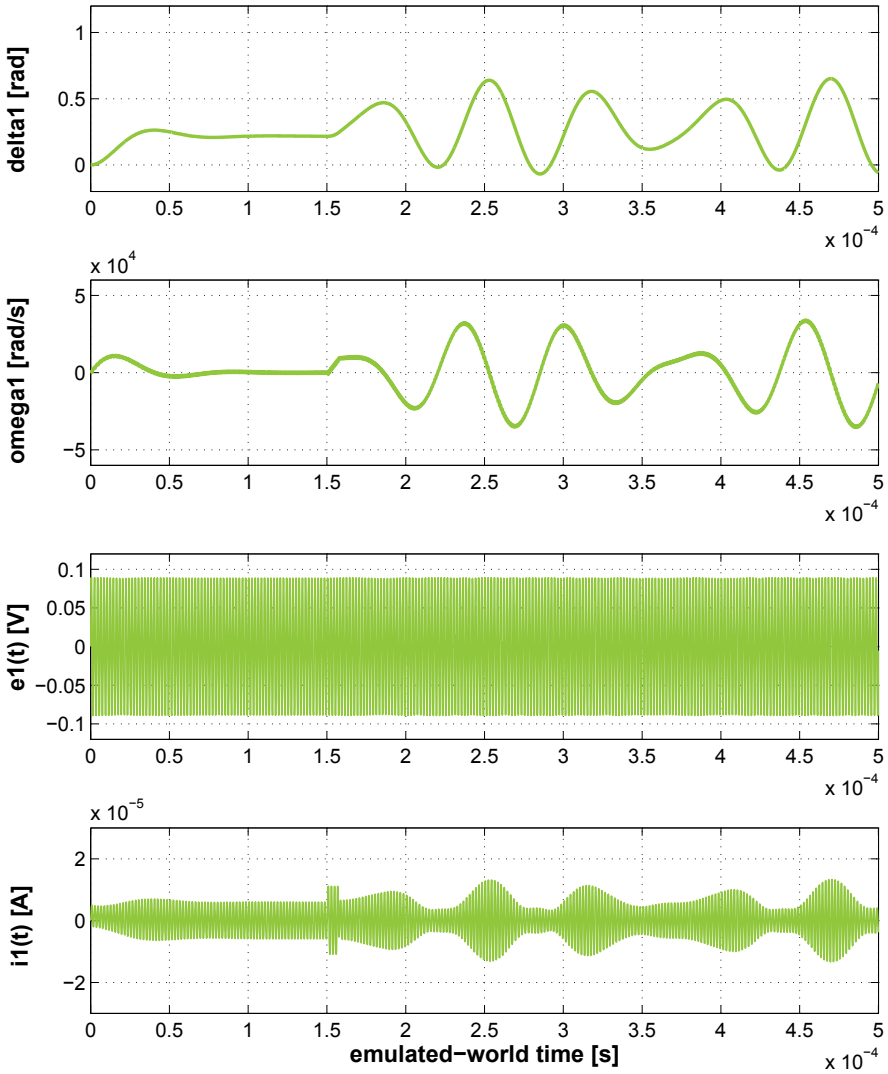


Figure 4.16.: $\omega_1(t)$, $\delta_1(t)$, $e'_1(t)$ and $i_1(t)$ of G_1 for $t_{sc} = 150.52\mu$s, $t_{dsc} = 7\mu$s and x = 50%. (ew)

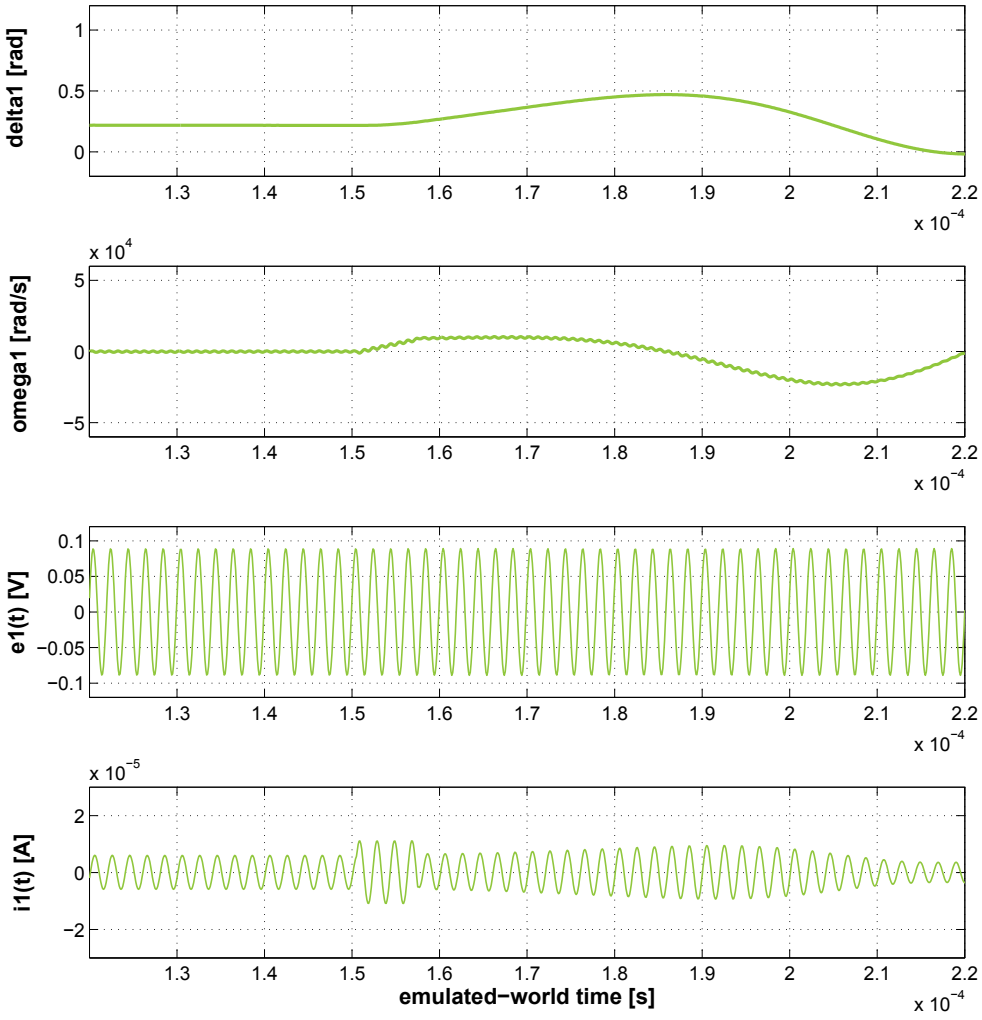


Figure 4.17.: Zoom on Fig. 4.16 around t_{sc}, i.e. from 1.2μs to 2.2μs. (*ew*)

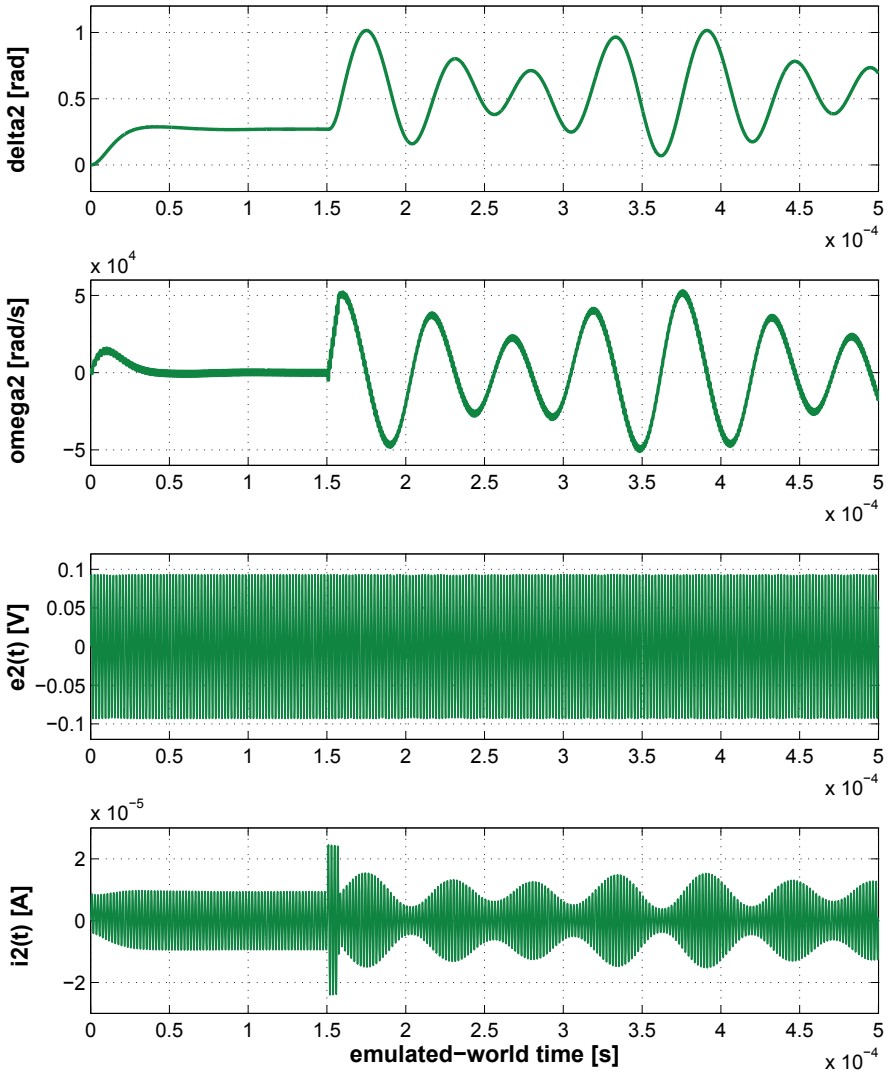


Figure 4.18.: $\omega_2(t)$, $\delta_2(t)$, $e_2'(t)$ and $i_2(t)$ of G_2 for $t_{sc} = 150.52\mu$s, $t_{dsc} = 7\mu$s and x = 50%. (ew)

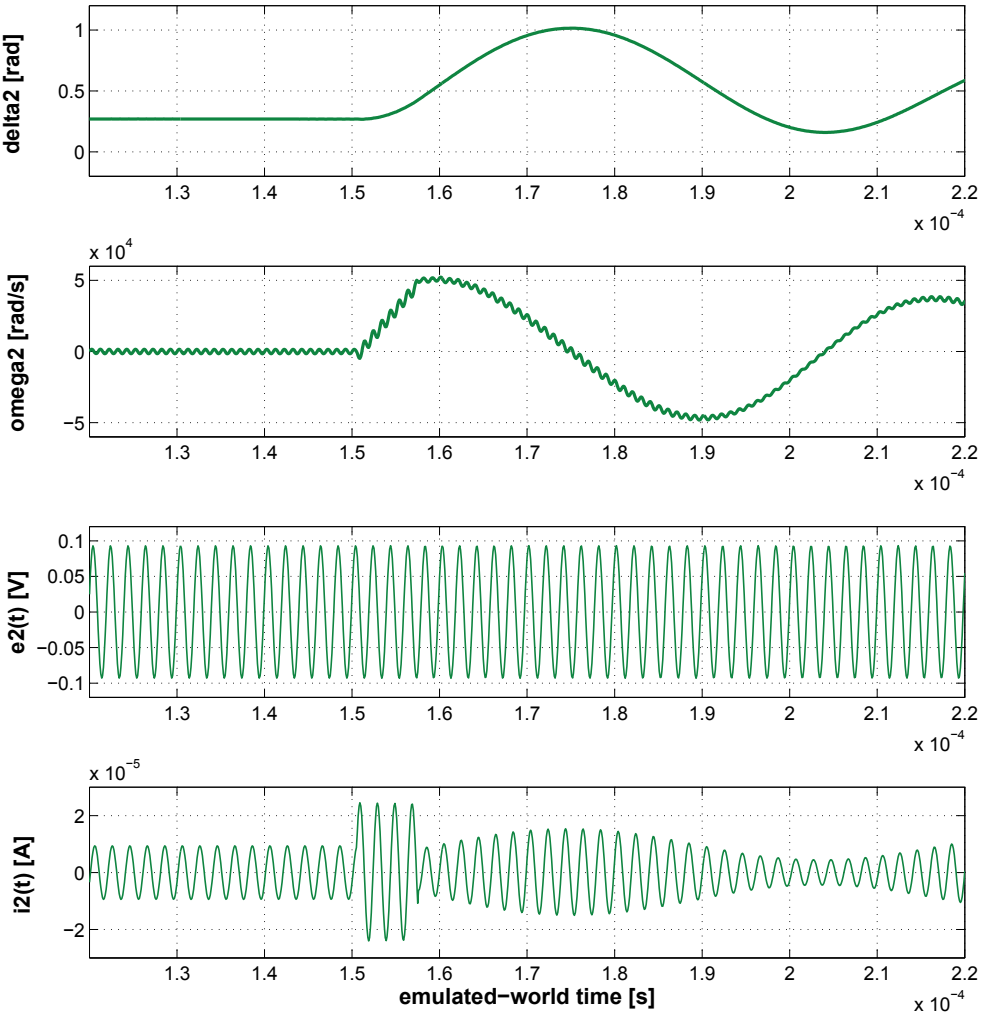


Figure 4.19.: Zoom on Fig. 4.18 around t_{sc}, i.e. from 1.2μs to 2.2μs. (*ew*)

The signals in the transmission line TL_{23} are plotted in Fig. 4.20. The moment of short circuit t_{sc} was chosen in order to avoid a DC offset in the current of the transmission line. Indeed, Fig. 4.21 shows the current in TL_{23} for different t_{sc}. The DC component of the current wave appears, due to the RL-impedance of the transmission line model. For the best possible emulation results, no DC component should appear. This is due to the fact that we are working with a single-phase equivalent of a symmetrical three phase system. In a three-phase system the DC components of the signals are also present in each phase, but the sum of these DC components is always equal to 0.

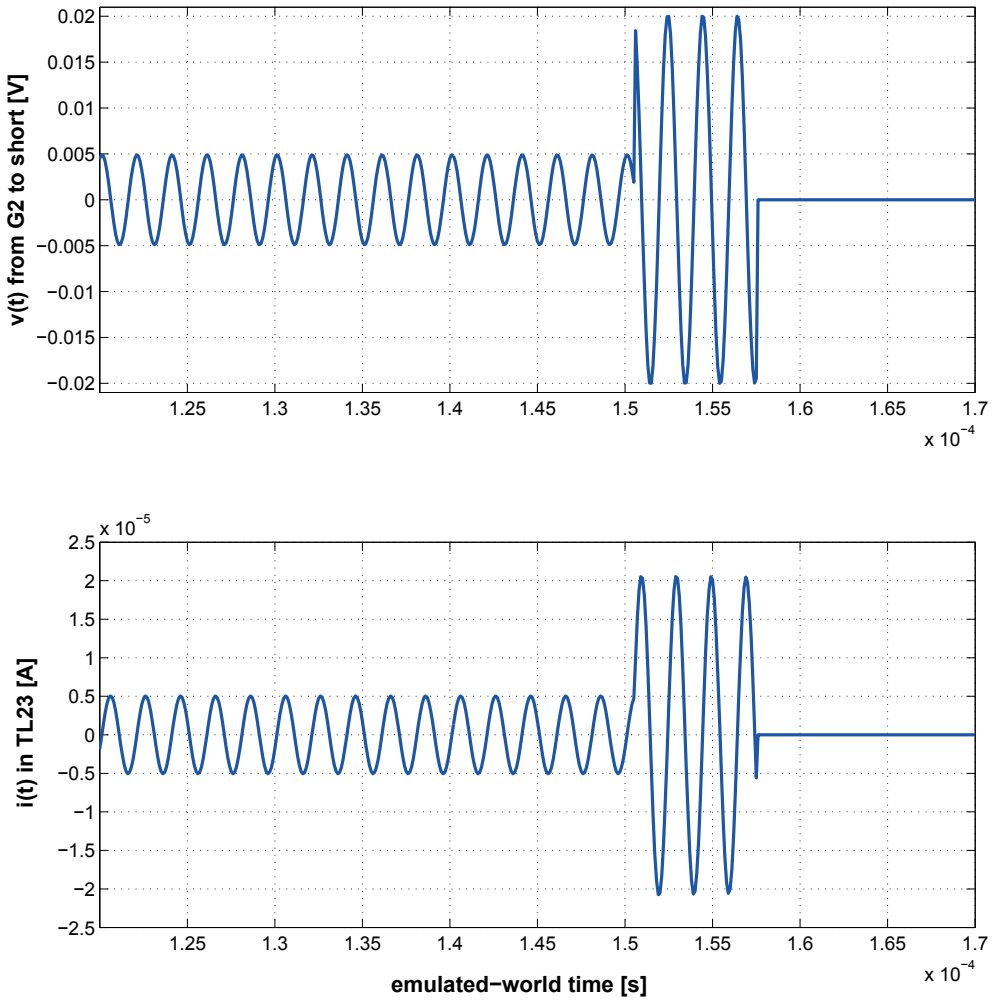


Figure 4.20.: Transient signals in transmission line TL_{23} for $t_{sc} = 150.52\mu$s, $t_{dsc} = 7\mu$s and x = 50%. (ew)

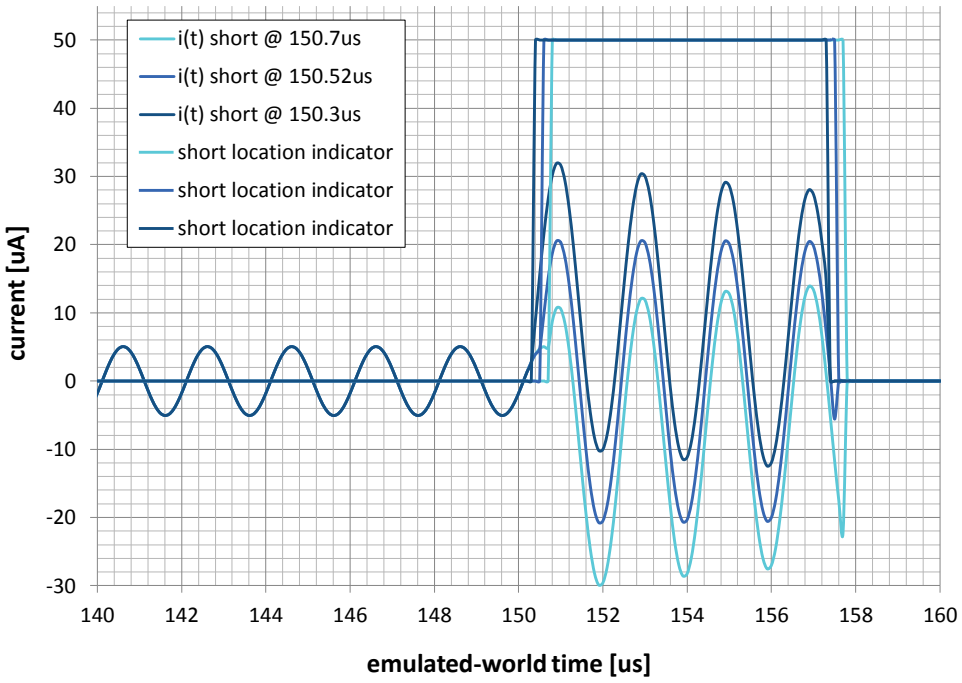


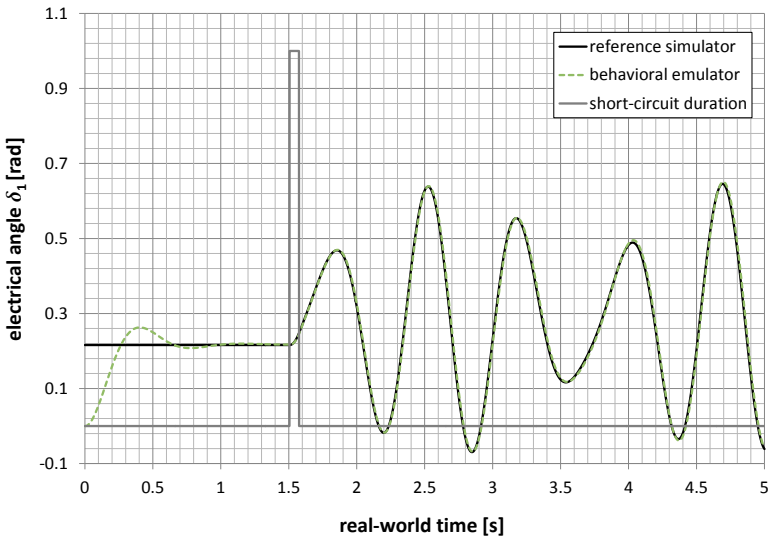
Figure 4.21.: Illustration of the current behavior in TL_{23} depending on the moment of short circuit for $t_{dsc} = 7\mu$s and x = 50%. (ew)

Finally, Fig. 4.22 compares the behavior of the electrical angles δ_1 and δ_2 of the behavioral emulation with the results of the numerical reference simulator. These results clearly validate the developed models. Again, it can be seen that the emulator needs some time to convert to the steady state value. Table 4.4 shows the absolute error of the emulation compared to the numerical simulation within 3.5s after the fault.

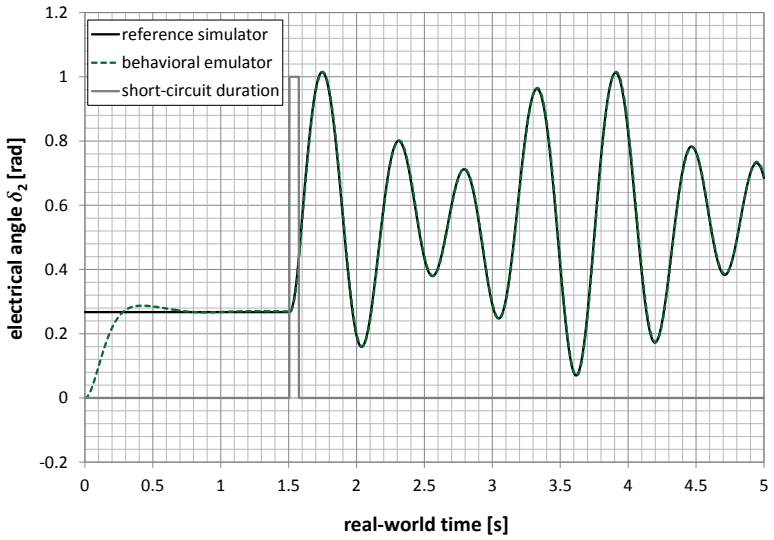
Table 4.4.: Absolute error within 3.5s after fault

	Δ_{min} [deg]	Δ_{max} [deg]
δ_1	-0.89	1.18
δ_2	-0.89	1.01

To illustrate the time scaling between the real-world and the emulated-world, Fig. 4.23 depicts the same electrical angles as Fig. 4.22, without transposing the emulation results into real-world values. Considering the time axis of the two charts, the time scaling becomes visible. As predicted, as the emulator is working at 500kHz, its phenomenon is 10'000 times faster than the duration of the real phenomenon shown by the numerical reference simulator.

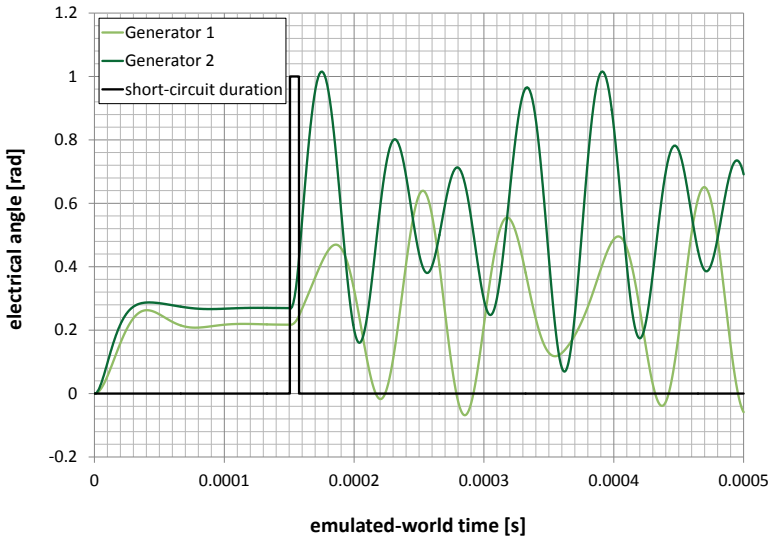


(a) Comparison of the electrical angle δ_1 of G_1 emulated and simulated

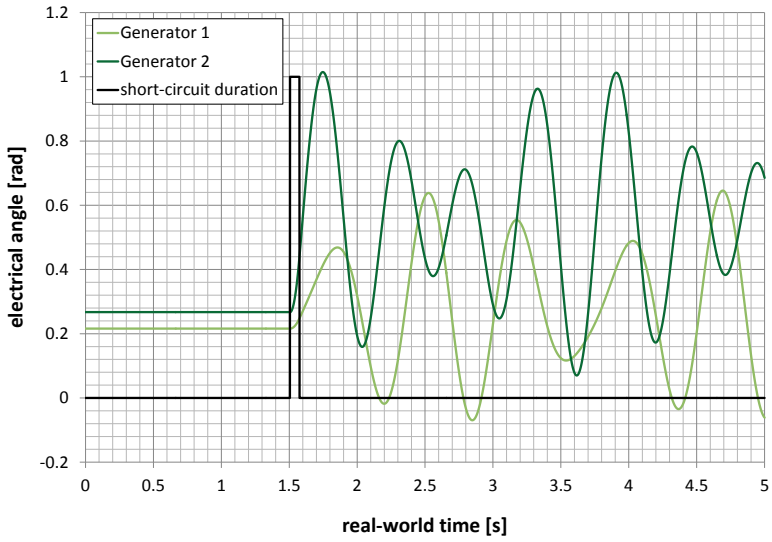


(b) Comparison of the electrical angle δ_2 of G_2 emulated and simulated

Figure 4.22.: Comparison of the electrical angles δ_1 and δ_2 simulated and emulated for t_{sc} = 1.5052s, t_{dsc} = 70ms and x = 50%. (rw)



(a) Emulated electrical angles δ_1 and δ_2 for $t_{sc} = 150.52\mu$s, $t_{dsc} = 7\mu$s and x = 50%. (ew)

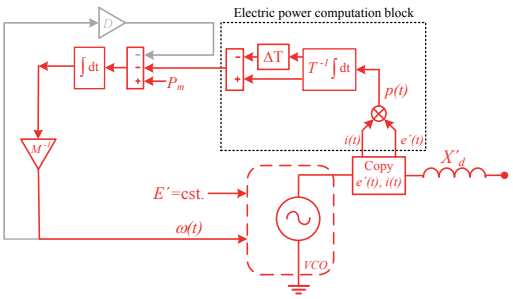


(b) Simulated electrical angles δ_1 and δ_2 for $t_{sc} = 1.5052$ms, $t_{dsc} = 70$ms and $x = 50\%$. (rw)

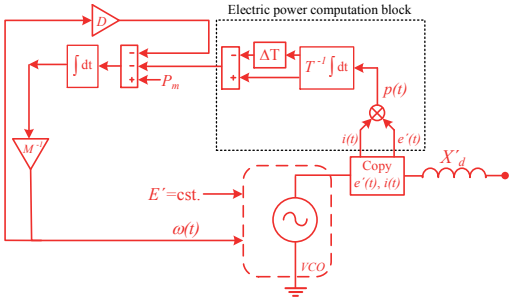
Figure 4.23.: Emulated-world time scale vs. real-world time scale to illustrate the speed-up: $\Psi = 10'000$.

2nd comparison: Generator models

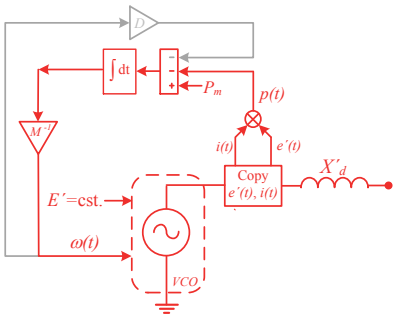
The same emulation as already described is done with the original generator model with and without damping. All generator models are remembered in Fig. 4.24. The results are presented in Fig. 4.25, where they are compared to the results of the optimized generator model, as well as to the results of the numerical reference simulator. As theoretically demonstrated in Section 4.2.2, the systematic error of the original model without damping constantly increases with time. Using damping to reduce this error works, but the optimal damping factor can only be found experimentally, knowing already the final result, as illustrated in Fig. 4.26. Therefore this model becomes useless.



(a) Original AC generator model without damping

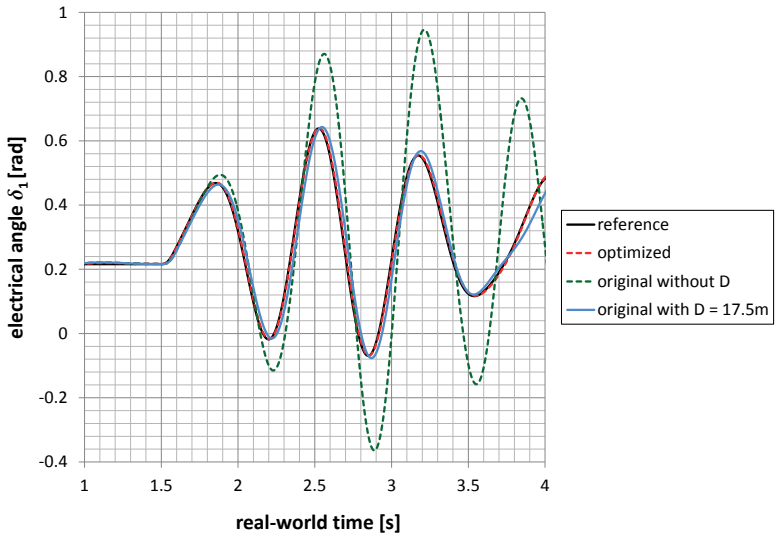


(b) original AC generator model with damping

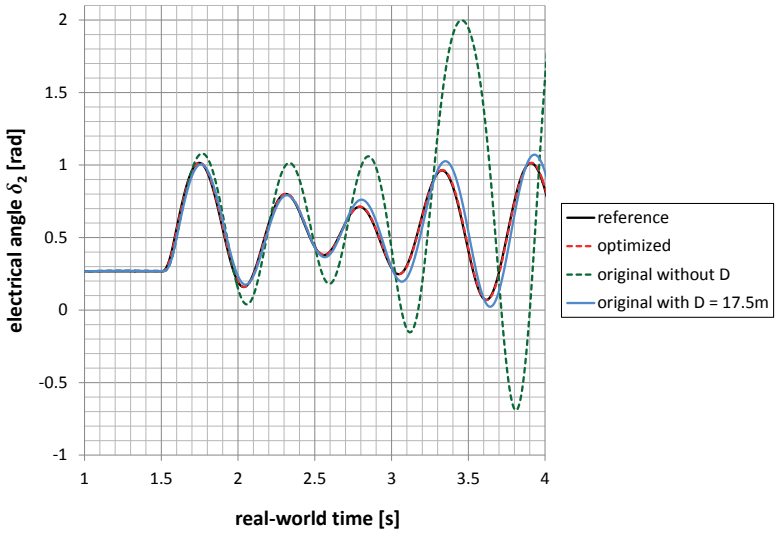


(c) Optimized AC generator model

Figure 4.24.: Reminder of the AC generator models developed in Section 4.2.2.Where the damping is in gray, it is not used during the emulation of the scenario, but only at the beginning for finding the steady state of the system.

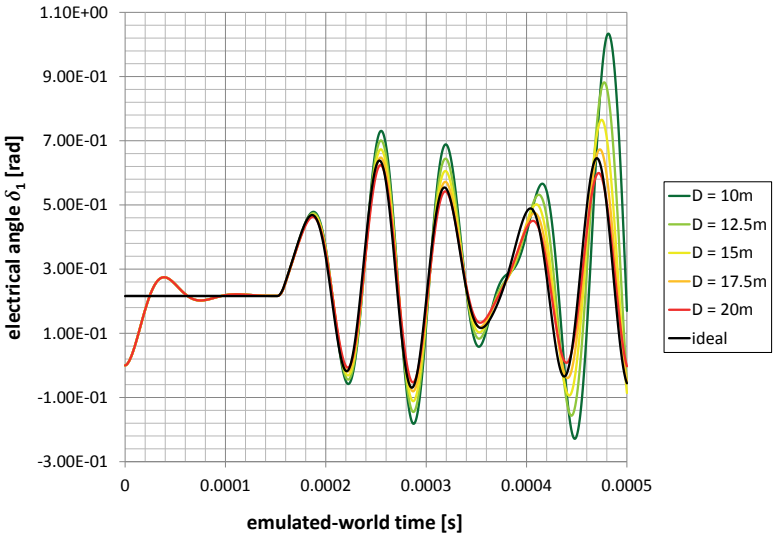


(a) Comparison of the electrical angle δ_1 of G_1 for the 3 different generator models

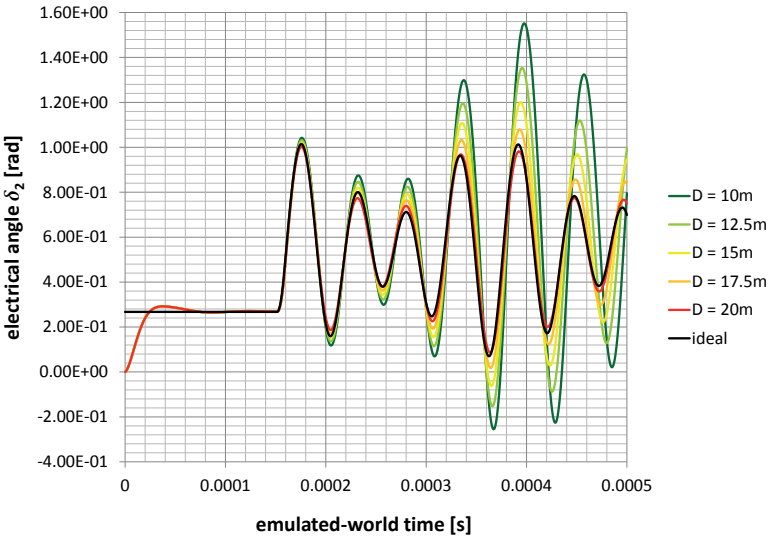


(b) Comparison of the electrical angles δ_2 of G_2 for the 3 different generator models

Figure 4.25.: Comparison of the original generator model with ($D = 17.5m$) and without damping with the optimized generator model for $t_{sc} = 1.5052$ms, $t_{dsc} = 70$ms and $x = 50\%$. (rw)



(a) δ_1 of G_1 for the 3 different generator models



(b) δ_2 of G_2 for the original generator model with different damping values D

Figure 4.26.: Comparison of the electrical angles for the original generator model with different damping values D for for $t_{sc} = 1.5052$ms, $t_{dsc} = 70$ms and $x = 50\%$. (rw)

3rd comparison: Critical Clearing Time (CCT)

The main function of a transient stability power system simulator is to determine the Critical Clearing Time (CCT) of a transmission line. As defined above, CCT, is the longest possible short circuit on a transmission line before the power system loses its stability. Fig. 4.27 shows an example of Generator G_2 being out of step, hence a case of instability of the 4-bus power system under test.

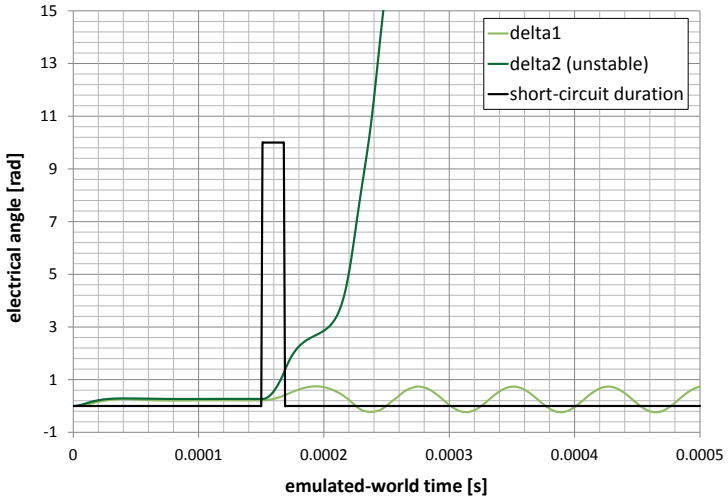


Figure 4.27.: Example of instability (G_2 out of step): Emulated electrical angles δ_1 and δ_2 for $t_{sc} = 150.5\mu$s, $t_{dsc} = 18.5\mu$s and $x = 50\%$. (ew)

In order to definitively prove the validity of the developed AC emulation models, CCT was determined for different short-circuit locations on TL_{23} and compared to the results of the numerical reference simulator. Therefore, the results are indicated in real-world time. The resolution chosen to determine CCT is 1ms, i.e. the twentieth part of the period of the signals propagating on the power grid. The short-circuit location varies form 5% to 95% of the total length of TL_{23} seen from generator G_2 with a step of 5%.

These results are very accurate and confirm the validity of the developed models. The difference between the emulated CCT-results and the corresponding simulated results, is never larger than 7ms, which is just a fraction of the period of the signals propagating along the transmission line (T=20ms). As such, it must be noted that the dependence on t_{sc} appears here as well. Fig. 4.29 illustrates this fact. CCT is determined for t_{sc} varying over one period with a step and a resolution of 100ns (the twentieth part of the period of the AC signals propagating along the transmission line). Depending on the value of the current at the moment of short circuit, CCT varies. As explained before, this is due to the changing initial conditions for the current in a RL-impedance, subject to a sudden voltage change.

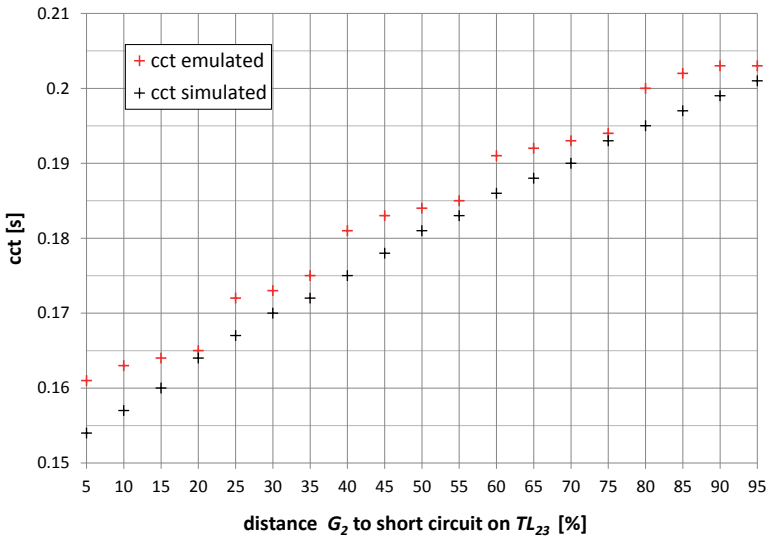


Figure 4.28.: CCT in dependence of the short-circuit location. (rw)

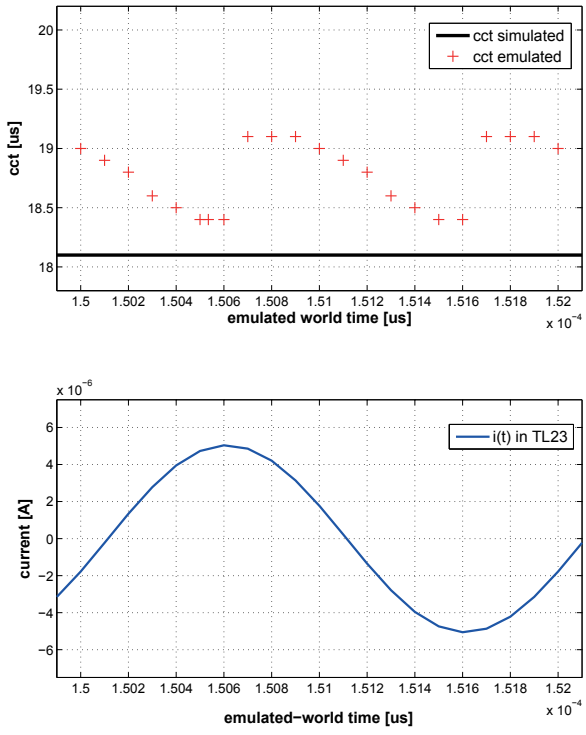


Figure 4.29.: CCT in dependence of the moment of short circuit t_{sc}. (ew)

5 Chapter 5. Implementation

Chapter overview

This chapter is dedicated to the design and implementation of the first AC emulation demonstrator. We propose custom programmable analog building blocks for the implementation of the proposed behavioral models. During their design, application-specific requirements, as well as imperfections, calibration, mismatch and process-variation aspects, are taken into account. In particular, the design of the tunable floating inductance used in all three AC emulation models is discussed in detail. In fact, major design challenges have to be addressed in order to achieve an inductance suitable for our application. The other designed blocks are portrayed in broad strokes, describing their working principle and discussing critical issues. The functionality and adequacy of the blocks are confirmed by transistor-level simulations.

5.1. Preliminaries

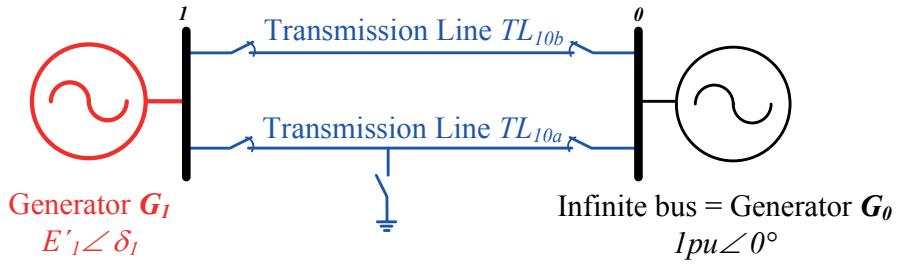


Figure 5.1.: Topology of the first AC emulation demonstrator: fixed topology with reconfigurable component characteristics

Before presenting the design of the different components, some general considerations are necessary. The general specifications and the scope of the first AC emulation demonstrator are outlined in Section 3.4; its topology was already presented in Fig. 3.6, which is now portrayed in Fig. 5.1.

This topology is composed of a generator, two transmission lines and an infinite bus (= slack generator). Transmission lines TL_{10a} and TL_{10b} can be disconnected, and transmission line TL_{10a} is additionally equipped with short circuit capabilities.

According to the behavioral models developed in the previous chapter, the topology to be implemented becomes as illustrated in Fig. 5.2. We identify three main components: the tunable floating inductance, the VCO and the reduced swing equation solver. The inductance is used in both the transmission line and the generator model; and, from a microelectronic point of view, it is the most challenging component to design. The VCO, including current and voltage copy and the reduced swing equation solver, belongs to the generator model.

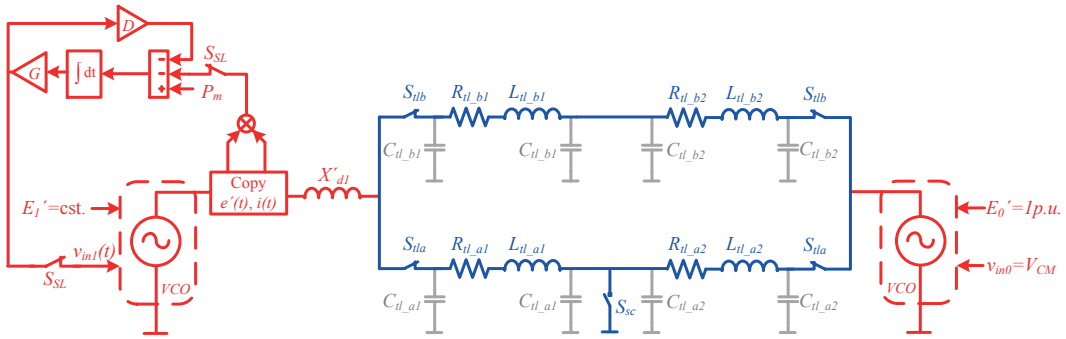


Figure 5.2.: Schematic view of the demonstrator

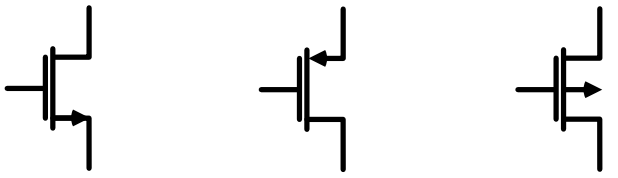
The technology that is used to realize this first AC emulation demonstrator is a conventional 0.35μm 3.3V CMOS technology. The common mode voltage V_{CM} is chosen so as to be in the middle of the power supply range. As such, the positive supply voltage V_{DD},

the common mode voltage V_{CM} and the negative supply voltage V_{SS} are as follows:

$$V_{DD} = 3.3V$$
$$V_{CM} = 1.65V$$
$$V_{SS} = 0V$$

A conventional technology with rather high supply voltage is preferable for purely analog implementations for two reasons. On the one hand, it does not restrict the microelectronic topology choices as a result of low-voltage constraints. And on the other hand, more voltage headroom is available for the operating signals and, therefore, noise is less critical. Moreover, the circuit should be designed for testability. In this scope, test circuitry is included in the different components, meaning that the power consumption and the area of the complete system are higher than strictly necessary.

In the following, the transistor-level design procedures presented are based on the EKV modeling approach and rely on the device inversion level I_F as a fundamental design variable [54]. Simulations were done in the Cadence Virtuoso environment using Spectre [52]. For the NMOS and PMOS transistors, the symbols illustrated in Fig. 5.3 are used. It is important to note that, due to the chosen technology, which does not allow separate p-wells, the bulk of the NMOS is imperatively connected to V_{SS}.



(a) (b) (c)

Figure 5.3.: Transistor symbols used in this section: (a) NMOS with bulk connected to V_{SS}, (b) PMOS with bulk connected to V_{DD} and (c) PMOS.

5.2. Inductance design

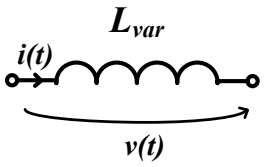


Figure 5.4.: Ideal tunable inductance

The purpose of this section is to develop a reprogrammable, floating and fully integrated inductance. This element is used as an internal inductance of the generator model, emulating the transmission line, and as part of the impedance load. In literature, integrated

inductor topologies exist; but, as is shown in the following, none of them is suitable for the application conditions of power system AC emulation. The proper microelectronic design of this element is therefore a key challenge of this thesis.

5.2.1. Topology development

Application specific considerations

Table 5.1.: Inductance value range

		range	$2\pi f_{tr} \cdot L_{min}$	$2\pi f_{tr} \cdot L_{max}$
1/2 transmission line	ωL_{tl}	25-450km	$25 \cdot \omega L' \cdot \frac{k_Z}{Z_n}$	$450 \cdot \omega L' \cdot \frac{k_Z}{Z_n}$
Internal inductance	X'_d	0.2 - 0.4p.u.	$0.2 \cdot k_Z$	$0.4 \cdot k_Z$
Load element	ωL_l	0.02 -0.4p.u.	$0.02 \cdot k_Z$	$0.4 \cdot k_Z$

Table 5.1 specifies the emulated inductance ranges of the different power system components. Obviously, these ranges depend on the shrink and downscaling factors introduced in Section 3.3 and the distributed line parameters defined in Section 4.3.1. Without setting concrete numerical values, the above values show already that, between the largest and the smallest desired inductance value, a factor of 20 exists.

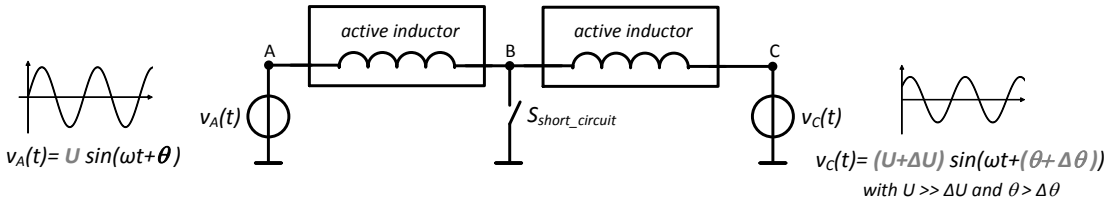


Figure 5.5.: Typical application of the active inductance in power system emulation

The typical application environment can be abstracted, as shown in Fig. 5.5. On the one hand, there will be inductance terminals where the voltages and their Operating Points (OPs) are imposed. This is typically the case at nodes where generators are connected. And on the other hand, there are also terminals where the inductance needs to be able to set voltages and OPs by themselves. The voltage amplitude at the terminals of the inductances is within $0.9 \cdot k_v$ and $1.1 \cdot k_v$. Hence, the swing is considerable on both terminals, but the voltage difference between the terminals is small. As such, the inductances have to handle different OPs at their terminals, and they have to accommodate large common-mode variations. Moreover, a fixed frequency operating range has to be guaranteed for all possible inductance values.

Out of this reasoning, the following specifications can be defined:

1. Maximum inductance tuning range

2. Frequency operating range constant for all possible inductance values

3. Able to work under unbalanced DC conditions

4. Large Common Mode Input Range (CMIR)

Existing topologies

Floating integrated inductors exist in CMOS fabrication technologies. They can be separated into two categories [55]:

- CMOS spiral inductors (passive) [56]

- CMOS active inductors [57–60]

Passive inductors are not suitable for our application, as they need a prohibitively large silicon area. Moreover, their inductance value is non-tunable. On the other hand, inductors synthesized using active devices are promising, as they need little area compared to their passive counterparts. In addition to this, reprogrammable inductances with large tuning ranges can be obtained. [61, 62]

Most of the floating active inductance topologies presented in literature have been designed for Radio Frequency (RF) applications, in which there is a critical need for inductive characteristics. Indeed, inductances are used in *LC* oscillators, RF phase shifters, RF bandpass filters, etc. Even if, initially, the topologies all appear different, they are usually based on the classical and well known gyrator-C networks.

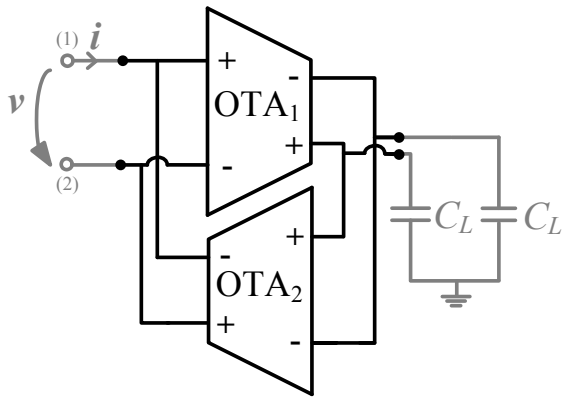


Figure 5.6.: Classical floating active inductor topology (between terminals (1) and (2)) based on a gyrator (in black) connected to capacitances

A top-level view of a floating active inductor created using a gyrator-C network is illustrated in Fig. 5.6. A gyrator consists of two back-to-back connected Operational Transconductance Amplifiers (OTAs) and acts as an impedance inverter. Hence, the

gyrator converts the capacitive behavior seen at its output into an inductive behavior.

Due to the nature of synthesized devices, the frequency range of active inductors is limited. For analyzing the frequency behavior of gyrator-C based inductors, we replace the OTAs of the gyrator with their one-pole equivalent model, as is shown in Fig. 5.7. An OTA is thereby represented using an ideal voltage-controlled current source with a transconductance G_m and its output conductances and capacitances, g_o and C_o, respectively. The subfix 1 or 2 indicates to which OTA of the gyrator the element belongs.

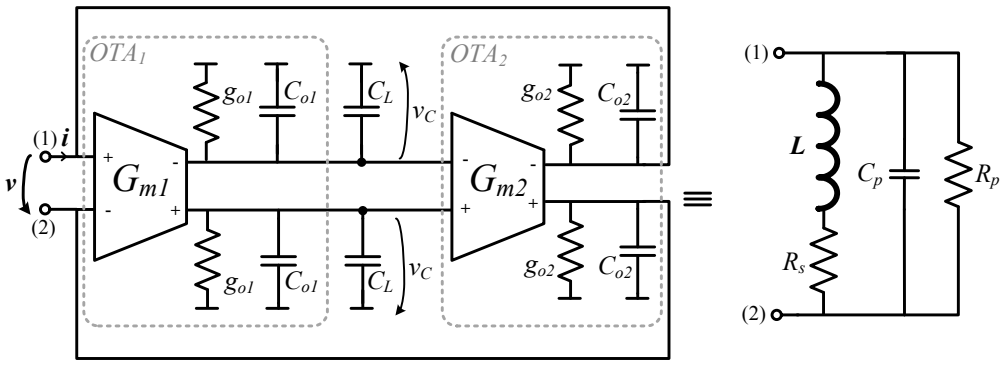


Figure 5.7.: System level of the active inductance model with its equivalent impedance model

Using this one-pole model of the OTA, the equivalent impedance of the gyrator-C topology can be determined. It is also depicted in Fig. 5.7. The equivalent impedance of the active inductance consists of several additional parasitic elements. The values of the elements correspond to:

$$L = \frac{C}{G_{m1}G_{m2}} \qquad C_p = \frac{C_{o2}}{2}$$

$$R_s = \frac{g_{o1}}{G_{m1}G_{m2}} \qquad R_p = \frac{2}{g_{o2}}$$

The inductance value is directly proportional to the conversion capacitor C and inversely proportional to the product of the transconductances of the OTAs of the gyrator. The conversion capacitor, C is composed of the sum of all capacitors at the output node of the gyrator:

$$C = C_L + C_{o1}. \tag{5.1}$$

The asymptotes of the impedance Bode plots, which are plotted in Fig. 5.8, show the influence of the parasitic elements. The inductance operating range is limited between the zero frequency ω_z and the resonance frequency ω_n.

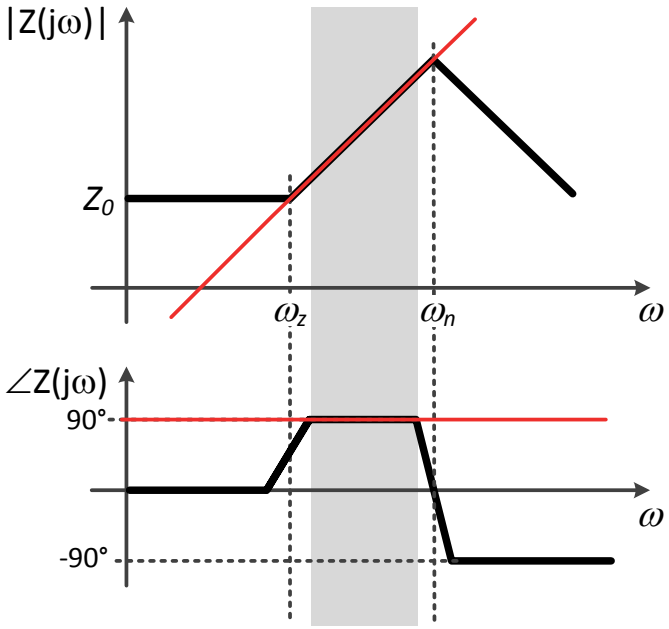


Figure 5.8.: Impedance Bode plots (asymptotes) magnitude and phase of the classical gyrator-C inductance topology (black) and the corresponding ideal inductance (red)

The zero and resonance frequencies and the impedance Z_0 are defined as follows:

$$Z_0 = \frac{R_p R_s}{R_s + R_p}, \tag{5.2}$$

$$\omega_z = \frac{R_s}{L}, \tag{5.3}$$

$$\omega_n = \sqrt{\frac{R_s + R_p}{L C_p R_p}}. \tag{5.4}$$

The developed impedance model fully characterizes the small signal behavior of a classical gyrator-C inductor. However, this model cannot be used to quantify the large signal-behavior. For this reason, the dependence of the inductance on the DC OP conditions, as well as the maximum signal swings, have to be investigated apart. Notably, a DC OP analysis reveals that this topology is not suited for application in power system emulation.

The problem appears at the output nodes of the gyrator. Their operating points V_C are highly sensitive to unsymmetrical DC conditions at the terminals of the inductance. Indeed, a voltage drop ΔV over the inductance, corresponds to a voltage difference at the input of OTA_1, and is therefore amplified by its voltage gain A_{v0_1}:

$$V_C = A_{v0\_1}\, \Delta V = \frac{G_{m1}}{g_{o1}}\, \Delta V. \tag{5.5}$$

This obviously leads to the risk that the inductance will saturate at these nodes, making operation impossible.

Custom topology

Additional circuitry is needed in order to control the OPs of the active inductor under unbalanced DC conditions. The solution is to create a custom inductance topology based on the classical gyrator-C topology, to which is added an offset reduction block [63, 64]. This topology is illustrated in Fig. 5.9. As the application conditions are not fully differential, there is no need to keep both OTAs fully differential. Replacing OTA_1 by a single-ended OTA does not change the method of operation, but has the advantage that only one offset reduction block has to be implemented.

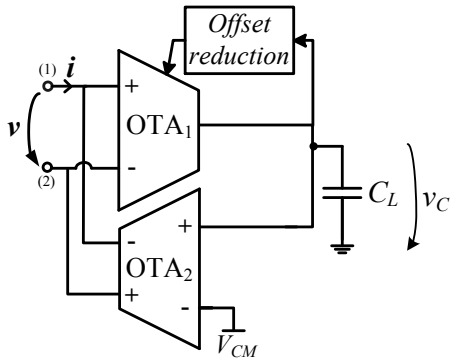


Figure 5.9.: Custom floating active inductance topology based on the classical gyrator-C topology

The operating principle can be described as follows. The offset reduction block senses the DC voltage component at the output of the gyrator, compares it to the ideal value, which corresponds to no offset, and then calibrates the DC current output of OTA_1. In this way, the offset currents are reduced.

5.2.2. System level analysis

Fig. 5.10 shows the system level of the custom topology using, as before, the one-pole equivalent model for the two OTAs. The offset reduction block adds two more parasitic elements to the equivalent impedance. The values of the elements correspond to:

$$L = \frac{C}{G_{m1}G_{m2}} \qquad R_p = \frac{2}{g_{o2}} \qquad R_{red} = \frac{1}{G_{m2}}$$

$$R_s = \frac{g_{o1}}{G_{m1}G_{m2}} \qquad C_p = \frac{C_{o2}}{2} \qquad C_{red} = \frac{G_{m2}}{\omega_{LP}}$$

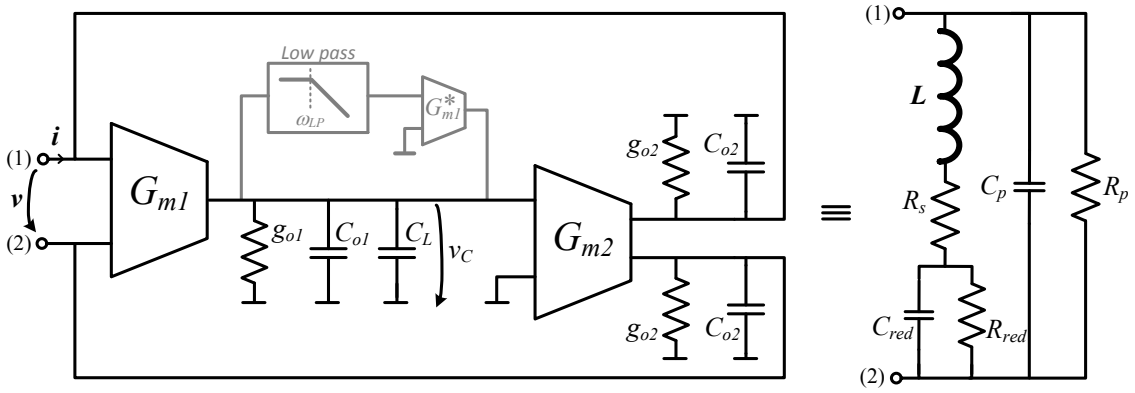


Figure 5.10.: System level of the custom inductance with its equivalent impedance model

The capacitor named C includes the conversion capacitor C_L, C_{o1} and all parasitic capacitance introduced by the blocks connected to the output of the gyrator.

The equivalent impedance shows that the customized gyrator-C network continues to behave like a lossy inductor. The inductance value is not affected by the offset reduction block, and remains independent of the output conductances of the two OTAs. In order to see the influence of the offset reduction block and to define the frequency operating range, we analytically express the equivalent impedance, obtaining:

$$\underline{Z} = Z_0 \frac{1 + j\omega n_1 + (j\omega)^2 n_2}{1 + j\omega d_1 + (j\omega)^2 d_2 + (j\omega)^3 d_3}, \tag{5.6}$$

where

$$Z_0 = \frac{R_p(R_{red} + R_s)}{R_p + R_{red} + R_s},$$

$$n_1 = \frac{L + C_{red}R_{red}R_s}{R_{red} + R_s},$$
$$n_2 = \frac{LC_{red}R_{red}}{R_{red} + R_s},$$

$$d_1 = \frac{C_{red}R_{red}R_p + L + C_{red}R_{red}R_s + C_pR_pR_{red} + C_pR_pR_s}{R_p + R_{red} + R_s},$$
$$d_2 = \frac{C_{red}R_{red}R_pC_pR_s + LC_pR_p + C_{red}R_{red}L}{R_p + R_{red} + R_s},$$
$$d_3 = \frac{C_{red}R_{red}LC_pR_p}{R_p + R_{red} + R_s}.$$

It appears that this impedance is composed of a complex conjugate zero and three poles, a single pole and a complex conjugate pole. Because $R_s \ll R_p$ and $R_s \ll R_{red}$, the dip frequency of the complex conjugate zero ω_{n1} and the peak frequency of the complex

conjugate pole ω_{n2} can be expressed as

$$\omega_{n1} = \sqrt{\frac{1}{LC_{red}}}, \tag{5.7}$$

$$\omega_{n2} = \sqrt{\frac{1}{LC_p}}. \tag{5.8}$$

In the same way, ω_p, the single pole frequency and Z_0 are

$$\omega_p = \frac{1}{R_{red}C_{red}}, \tag{5.9}$$

$$Z_0 = \frac{R_p R_{red}}{R_p + R_{red}}. \tag{5.10}$$

The frequency behavior of the customized topology becomes, therefore, as depicted in Fig. 5.11. Its analysis shows that the offset reduction block adds a pole and a zero, thereby increasing the value of the DC impedance Z_0, and influencing the lower border of the frequency operating range.

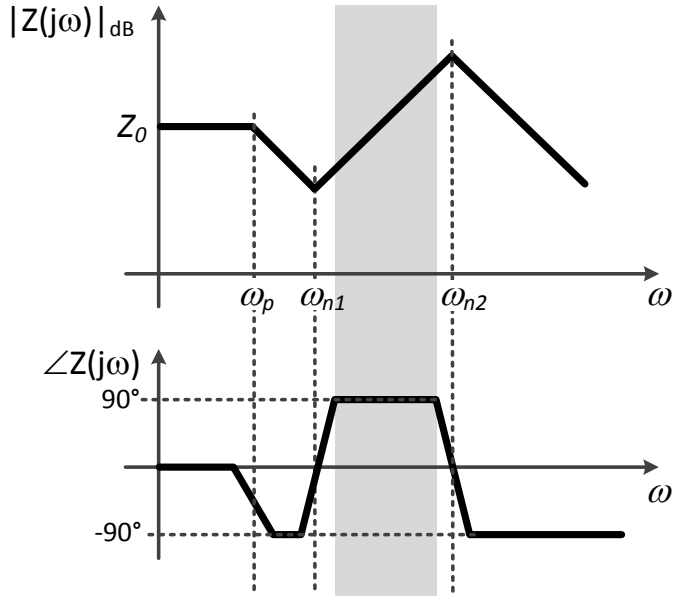


Figure 5.11.: Impedance Bode plots (asymptotes) magnitude and phase of the custom inductance topology

The inductive frequency range is delimitated by ω_{n1} and ω_{n2}. The upper boundary of the frequency range is typically known as a self-resonant frequency of an inductance. Finally, the quality factor of the complex conjugate pole, Q_{n1}, and complex conjugate zero, Q_{n2}, can be approximated as

$$Q_{n1}^2 \approx \frac{L}{C_{red}R_s^2}, \tag{5.11}$$

$$Q_{n2}^2 \approx \frac{R_p^2 C_p}{L}. \tag{5.12}$$

These factors are important when considering the phase error of the inductance in the operating frequency range. The phase of the impedance of active inductors should be made constant and as close as possible to $\pi/2$ over the whole operating range. Hence, the higher the quality factors, the more ideal is the inductance. As such, R_s should be minimized and R_p maximized. Note that the frequency boundaries, as well as the inductance value, are independent of the output conductances of the two OTAs. This means that the quality factors can be tuned independently of the operating frequency range.

Table 5.2 summarizes the obtained results, by describing optimization strategies for the frequency range and the phase error of the inductance, depending on the OTA design parameters.

Table 5.2.: Parameters which optimize the tuning range and phase error of the inductance

characteristic to optimize		**design parameter** to increase	to decrease
ω_{n1}	decrease	C	G_{m1}, ω_{LP}
ω_{n2}	increase	G_{m1}, G_{m2}	C, C_{02}
Q_{n1}	increase	G_{m1}, C, ω_{LP}	g_{o1}
Q_{n2}	increase	C_{o2}, G_{m1}, G_{m2}	C, g_{o2}

Another significant design parameter is the stability of the inductance. In this scope, we determine the open-loop transfer function v_{out}/v_{in} of the inductance. Fig. 5.12 illustrates the approach. Analytically, we obtain

$$\frac{v_{out}}{v_{in}} = A_{v0} \frac{1 + j\frac{\omega}{\omega_{LP}}}{\left(1 + j\omega\frac{C_{o2}}{g_{o2}}\right)\left(1 + j\omega\frac{g_{o1}+\omega_{LP}C}{\omega_{LP}(g_{o1}+G_{m1})} + (j\omega)^2\frac{C}{\omega_{LP}(g_{o1}+G_{m1})}\right)} \tag{5.13}$$

$$A_{v0} = \frac{2G_{m1}G_{m2}}{g_{o2}(g_{o1} + G_{m1})} \tag{5.14}$$

This transfer function contains a zero and three poles. The zero frequency is set by the offset reduction block and corresponds therefore to ω_{LP}. The resonance frequency of the complex conjugate pole coincides with ω_{n1}, the lower boundary of the inductance operating range, and finally, the single pole is set by the dominant pole of OTA_2. Fig. 5.13 illustrates the described behavior.

Stability (Phase Margin (PM) $\geq>$ 60°) can only be achieved if the dominant pole frequency of OTA_2 is higher than the Unity Gain Bandwidth (GBW) frequency:

$$\omega_{GBW} < \omega_{pd2} \tag{5.15}$$

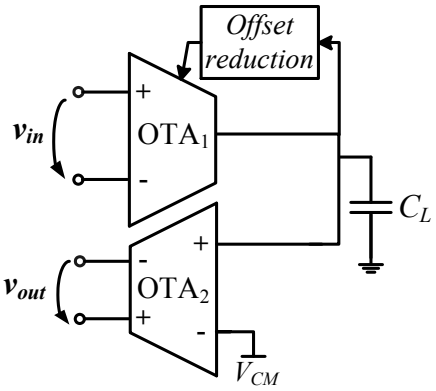


Figure 5.12.: Open-loop configuration for stability analysis of the inductance

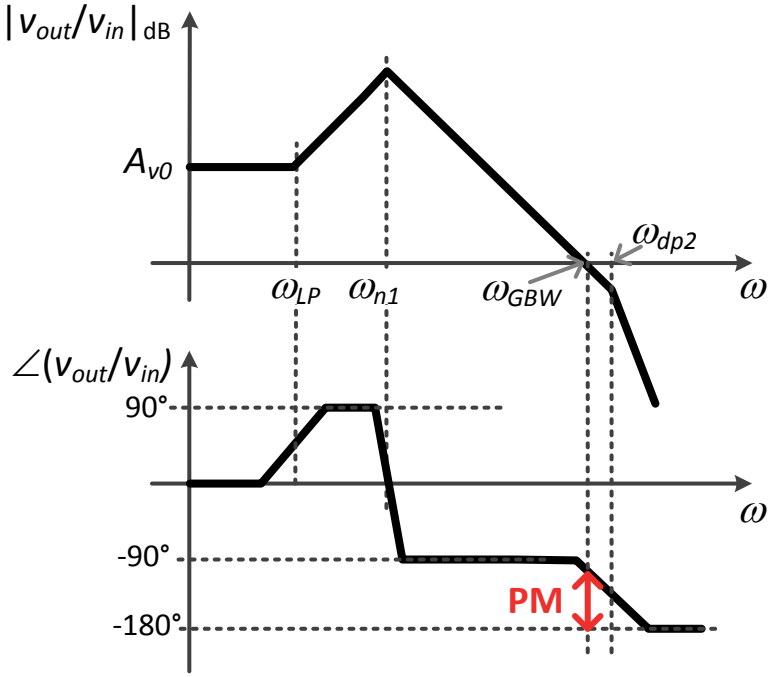


Figure 5.13.: Bode plot (v_{out}/v_{in} as illustrated in Fig. 5.12)

If this is the case, ω_{GBW} equals

$$\omega_{GBW} = \omega_{n1}^2 \frac{A_{v0}}{\omega_{LP}} = \frac{G_{m1} G_{m2}}{g_{o2}\, C} = \frac{1}{L\, g_{o2}}. \tag{5.16}$$

As the dominant pole frequency of OTA_2 is defined as

$$\omega_{dp2} = \frac{g_{o2}}{C_{o2}}, \tag{5.17}$$

there are two ways to optimize the PM for a given L value: to decrease C_{o2} or to increase g_{o2}. The latter acts on ω_{GBW} and ω_{dp2}, and is therefore more efficient.

Finally, within the operating range of the inductance, the amplitude of the voltage v_c at the output of the gyrator can be quantified as:

$$|v_C| = \frac{2G_{m1}}{\omega C} |v| . \tag{5.18}$$

This equation characterizes the input voltage of OTA_2, giving a design constraint for its linearity range.

5.2.3. Inductance tunability

The system analysis has shown that the inductance value is dependent on the transconductances of the OTAs and the conversion capacitor C, according to the following equation

$$L = \frac{C}{G_{m1}G_{m2}}. \tag{5.19}$$

Therefore, the value of the inductance can be tuned by varying G_{m1}, G_{m2} or C_L. The latter should be avoided, due to the huge silicon area needed to implement a programmable array of capacitances.

The transconductance G_m of an OTA is typically set by the g_m of the differential pair transistors at the input of the OTA. This transconductance g_m depends on the current I_D flowing through it, and on the ratio width over length (W/L) of the transistor:

$$g_m = \frac{1}{nU_T} \frac{I_D}{\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{I_D}{2nU_T^2 K_P \frac{W}{L}}}}, \tag{5.20}$$

where n, U_T, and K_P are technology-dependent parameters [54]. After integration, only the current can be varied: the dimensions are fixed. Fig. 5.14 illustrates these relations. Two main reasons lead to the decision to vary only G_{m1}:

1. Varying the current in an OTA also affects its poles. Therefore, as illustrated in Fig. 5.13, in order to guarantee stability, the dominant pole of OTA_2 has to be at the highest possible frequency.

2. As we want to emulate short circuits on transmission lines, OTA_2 has to be able to sink and source a lot of current. Therefore, it is best to keep this current constant for every inductance value.

G_{m1} is therefore the only parameter to be varied and, keeping C_L and G_{m2} constant, G_{m1} has to be tunable by a factor of around 20 (see Section 5.2.1). This variation is purely theoretical as a process, and mismatch variations were ignored. Indeed, a passive integrated poly capacitor can vary up to ±30%, while the transconductance differs up to ±20%. These variation ranges have to be compensated by using an even larger G_{m1} tuning range.

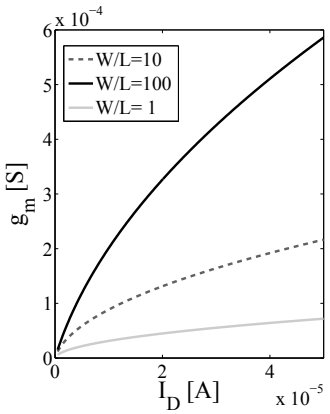


Figure 5.14.: Relation between transconductances, current and width over length ratio (W/L) of a PMOS transistor

5.2.4. Choice of the shrink and downscaling factors

Table 5.3.: Shrink and downscaling factors

	[p.u.]	real world		emulated world	
$\boldsymbol{U}$	1	380	kV	80	mV
$\boldsymbol{I}$	1	263	A	4	μA
$\boldsymbol{S}$	1	100	MVA	320	nVA
$\boldsymbol{Z}$	1	1'444	Ω	20	kΩ
$\boldsymbol{f}$	–	50	Hz	500	kHz

All the aforementioned design constraints extracted from the system level analysis and the application specific considerations permit the shrink and downscaling factors to be chosen. First, we set the transposed frequency to f_{tr}=500kHz and the operating range to $f_{tr} \pm 250$kHz. This ensures that no HF and VHF design challenges are added to the design, and that enough GBW could be obtained with commonly used amplifier topologies, nevertheless keeping a maximal speed enhancement. The voltage and current downscaling factors were chosen with care, in order to minimize the influence of imperfections. The per-unit voltage was kept as small as possible in order to minimize the necessary linearity ranges over the large inductance biasing current range. At the same time, the per-unit current was maximized, keeping reasonably high per-unit impedance: the higher the impedance, the more stable the inductance. The trade-off between inductance stability and linearity is a key challenge of the following transistor-level design.

The choices are summarized in Table 5.3.

5.2.5. Transistor level design

The transistor-level implementation is depicted in Fig. 5.15. Only the main structure is shown. The current and voltage biasing structure is omitted, as these factors have no influence on the presented design parameters.

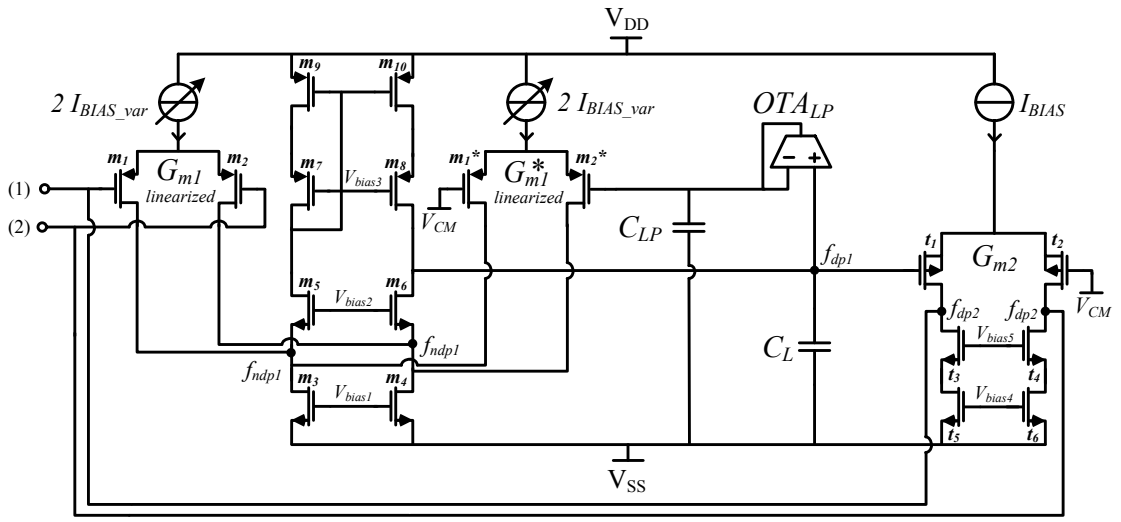


Figure 5.15.: Transistor-level schematic of the inductance (main structure)

In the following, we provide the grounds for the topology choice of each component and we break down the system-level and the application specific design constraints to transistor-level design constraints.

In addition to the constraints that are introduced by the inductance requirements, each component has to be stable on its own in order to guarantee its functionality within the inductance.

$\mathbf{OTA_1}$

OTA_1 is implemented as a folded cascode amplifier with two matched input differential pairs. The added differential pair G^*_{m1} is used as part of the offset reduction block. Its inputs are the filtered DC value V_C at the output of the gyrator on one side, and the ideal DC value (=V_{CM}), which corresponds to no offset on the other side. This reduction loop regulates V_C until it equals V_{CM} + ΔV, where ΔV is the constant voltage drop over the inductance. If, additionally, the input referred offset voltage of each block is considered, V_C equals

$$V_C = V_{CM} + \Delta V + V_{offset\_G_{m1}} - V_{offset\_G^*_{m1}} - V_{offset\_LP} \tag{5.21}$$

and still avoids, therefore, the internal saturation of the inductance. Nevertheless, a side effect of the offset compensation exist: A constant offset current ΔI is generated:

$$\Delta I = G_{m2}(V_C - V_{CM} + V_{offset\_G_{m2}}). \tag{5.22}$$

The equivalent impedance of the inductance, including its OP behavior, is illustrated in Fig. 5.16.

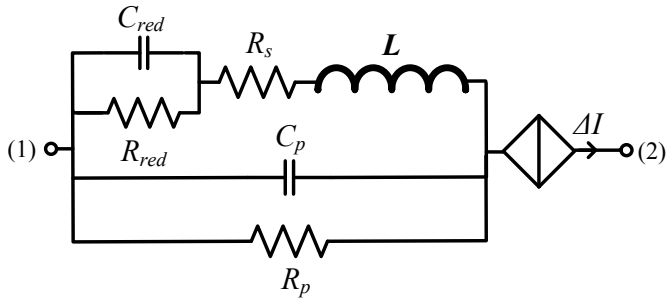


Figure 5.16.: Equivalent impedance of the active inductor including its OP behavior

We have chosen a folded cascode topology because a simple OTA topology, as used for the OTA_2, does not guarantee enough output swing for the whole biasing current range. An additional design constraint is added by this choice, as a non-dominant pole f_{ndp1} appears (see Fig. 5.15). So as not to disturb the functionality of the inductance and endanger its stability, we have to guarantee that this pole frequency is at least one decade away from ω_{GBW} of the inductance.

Out of all the previous considerations, the following specifications for OTA_1 can be extracted:

G_{m1}	:	$G_{m1\_max}/G_{m1\_min} = 20$
differential input signal	:	$\pm$15mV
common mode swing	:	$\pm$80mV
inductance stability	:	$f_{ndp1} \geq 10 \cdot f_{GBW}$
OTA_1 stability	:	$60° = 180° - \arctan\left(\frac{f_{GBW1}}{f_{dp1}}\right) - \arctan\left(\frac{f_{GBW1}}{f_{ndp1}}\right)$
output swing	:	$V_{CM} \pm 0.6$V
g_{o1}	:	permits to optimize Q_{n1}

And from these specifications, design constraints for the different transistors of the topology can be derived, knowing:

$$g_{o1} = \frac{g_{ds\_m8} g_{ds\_m10}}{g_{m\_m8}} + \frac{g_{ds\_m6}(g_{ds\_m4} + g_{ds\_m2})}{g_{m\_m6}} \tag{5.23}$$

$$f_{GBW} = \frac{g_{m\_m1}}{2\pi(C_L + C_{o1})} \tag{5.24}$$

$$f_{dp1} = \frac{g_{o1}}{2\pi(C_L + C_{o1})} \tag{5.25}$$

$$f_{ndp1} = \frac{g_{m\_m6}}{2\pi(C_{gs\_m6} + C_{gd\_m4} + C_{gd\_m2})} \tag{5.26}$$

$$C_{o1} = C_{gd\_m6} + C_{gd\_m8} \tag{5.27}$$

Equation 5.20, associating g_m of a transistor to its bias current I_D, shows that considerable bias current variation is needed in order to cover this large G_{m1} tuning range. Therefore, to improve the linearity for low bias currents, the differential pairs are linearized using the method presented in [65]. Two transistors, designed to work in triode region, are added to the differential pairs, as illustrated in Fig. 5.17. The drawback of this linearization is the reduction of the G_{m1} tuning range, as is illustrated in Fig. 5.18. This implies the need for an even larger bias current range.

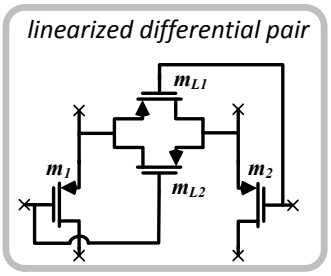


Figure 5.17.: Differential pair linearization as introduced in [65]

OTA$_2$

OTA_2 is a fully differential OTA. A common mode feedback loop is not necessary, because of the fact that the OPs of the inductance are externally imposed or indirectly controlled by the offset reduction block. The critical design parameter of this OTA is the inductance stability. A topology able to provide a dominant pole at high frequency is needed. A simple OTA topology is therefore convenient.

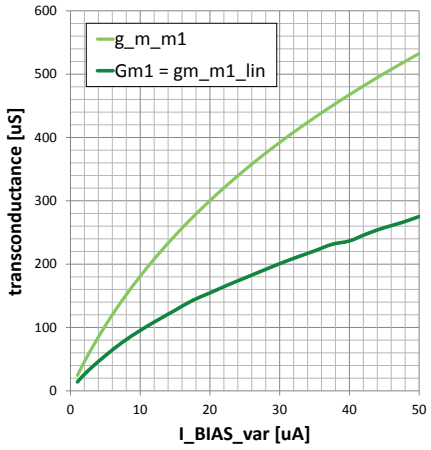


Figure 5.18.: Transconductance of transistor m_1 (g_{m_m1}) compared to the linearized equivalent transconductance G_{m1}

Similar to OTA_1, we are able to extract the following specifications concerning OTA_2:

I_{BIAS}	:	15 p.u.
differential input signal	:	$\pm$ 0.6V
output swing	:	$\pm$80mV
inductance stability	:	$f_{GBW} \ll f_{dp2}$
C_{o2}	:	permits to optimize ω_{n2} and Q_{n2}
g_{o2}	:	permits to optimize Q_{n2}

The corresponding transistor-level equations are:

$$g_{o2} = g_{ds\_t2} + \frac{g_{ds\_t4} g_{ds\_t6}}{g_{m\_t4}} \tag{5.28}$$

$$C_{o2} = C_{ds\_t1} + C_{gd\_t3} + C_{eq} \tag{5.29}$$

$$f_{dp2} = \frac{g_{o2}}{2\pi C_{o2}} \tag{5.30}$$

$$G_{m2} = \frac{g_{m\_t1}}{2} \tag{5.31}$$

C_{o2} is the equivalent capacitance seen at the output node of OTA_2. Obviously, this capacitance depends on the parasitic capacitances of the output transistors of OTA_2 ($C_{ds\_t1} + C_{gd\_t3}$) and on the parasitic capacitances of all blocks that are connected to this node ($= C_{eq}$). First, there is the parasitic capacitance of the differential pair of OTA_1,

C_{gs_m1}, as seen in Fig. 5.15. Second, if the environment in which the inductance will be used (see Fig. 5.2) is considered, there are switches. In order to minimize the parasitic capacitances that these switches add to the output node of the inductance, a dedicated mechanism to create short circuits and line disconnections is implemented.

The short circuit mechanism is illustrated in Fig. 5.19. The output and the input of the different OTAs are isolated from each other during the short circuit. Therefore, the requirements for the switches to ground are relaxed. As there is no current in SW_{1a}, the differential pairs see an ideal short circuit. All the short-circuit current is flowing through SW_{1b}, which is allowed to be resistive, as the voltage level at the output of OTA_2 is allowed to differ from the ideal value. Indeed, this does not influence the quality of the short circuit. During normal operation, switch SW_2 establishes the connection between OTA_1 and OTA_2. But, as there is no current flowing through this switch, it can be optimized for small parasitic capacitance.

The line disconnection is emulated by putting off the current biasing and the active load of OTA_2. Therefore, this action no longer has an impact on the output node of OTA_2.

Moreover, still working to guarantee the stability of the inductance, we make use of the fact that the transmission line model contains a low resistance in series with the inductance. This resistance can consequently be used to further decrease the output conductance of OTA_2, thereby improving the stability of the inductances used in the transmission line model.

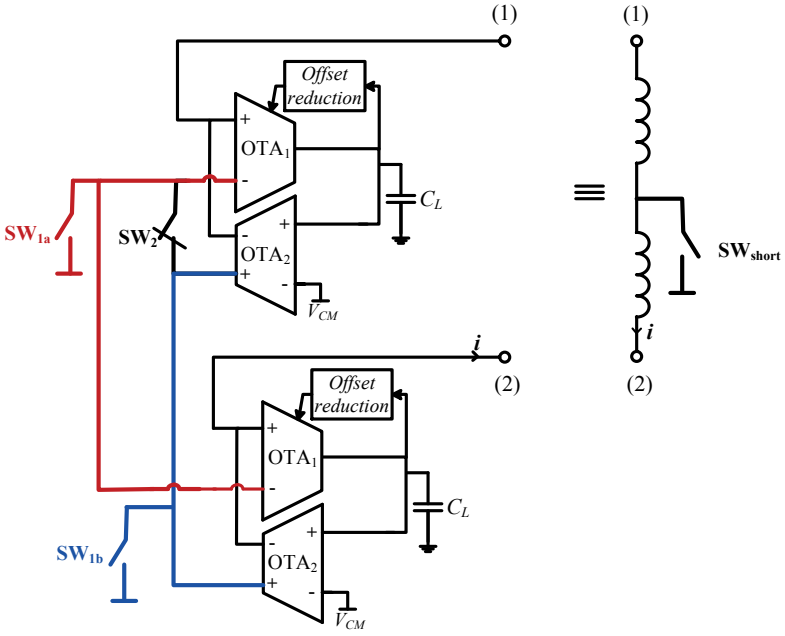


Figure 5.19.: Schematic illustration of the dedicated short-circuit mechanism

$\mathbf{OTA}_{LP}$

The low-pass filter is implemented as a first order RC-filter. In order to save area, the resistance is implemented as a lowly-biased simple OTA, mounted as follower.

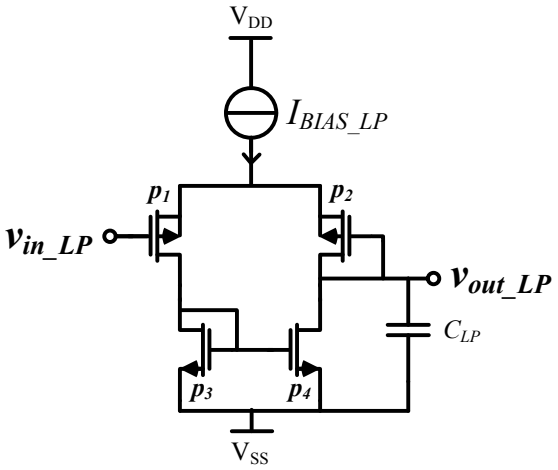


Figure 5.20.: Transistor-level schematic of the low-pass filter (main structure)

The design specifications are:

ω_{LP}	:	$\omega_{LP} \ll \omega_{n1}$
area	:	$C_{LP} \leq 20\text{pF}$
ω_{LP}	:	permits to optimize ω_{n1} and Q_{n1} (trade-off)

And the cutoff frequency of the filter is defined as

$$\omega_{LP} = \frac{g_{m\_p1}}{C_{LP}}. \tag{5.32}$$

Complete inductance

The bottom line of the inductance design is to specify G_{m1_min}, G_{m1_max}, G_{m2} and C_L. This is due to the fact that almost all inductance characteristics depend on these parameters (remember Table 5.4). Several optimization loops are necessary in order to be able to find an optimal solution for each of these parameters. Indeed, as shown by means of the transistor-level design constraints presented before, g_{o1}, g_{o2}, C_{p1} and C_{p2} are also influenced by the choice of G_{m1} and G_{m2}, respectively. Table 5.4 summarizes the findings of this section.

Table 5.4.: Transistor-level parameters which optimize the frequency range, the phase error and the stability of the inductance

characteristic to optimize		**design parameter** to increase	to decrease
ω_{n1}	decrease	C_L, C_{gd_m6}, C_{gd_m8}, C_{LP}	g_{m_p1}, $g_{m\_m1\_lin}$
ω_{n2}	increase	g_{m_t1}, $g_{m\_m1\_lin}$	C_{ds_t1}, C_{gd_t3}, C_{eq}, C_L, C_{gd_m6}, C_{gd_m8}
Q_{n1}	increase	C_L, C_{gd_m6}, C_{gd_m8}, g_{m_p1}, $g_{m\_m1\_lin}$, g_{m_m8}, g_{m_m6}	g_{ds_m8}, g_{ds_m10}, g_{ds_m6}, g_{ds_m4}, g_{ds_m2}, C_{LP}
Q_{n2}	increase	$g_{m\_m1\_lin}$, g_{m_t4}, C_{ds_t1}, C_{gd_t3}, C_{eq} , g_{m_t1}	g_{ds_t2}, g_{ds_t4}, g_{ds_t6}, C_L, C_{gd_m6}, C_{gd_m8}
PM	increase	g_{ds_t4}, g_{ds_t6}, g_{ds_t2}	C_{ds_t1}, C_{gd_t3}, C_{eq}, g_{m_t4}

By means of this table and several iterations, the design of the inductance can be accomplished. It is recommended that the initial stage of design is to specify G_{m2}, as the stability of the inductance is the most critical design parameter.

The transistor dimensions and bias current choices of the inductance designed to be part of the first demonstrator are listed in the following tables for each component separately. They are followed by tables containing their simulated characteristics. All transistor-level simulations are performed in the Cadence IC-Virtuoso environment. The simulator used is Spectre [52]. This allows to perform DC, transient and AC simulations of the transistor level of the designed inductance and its components. Moreover, the analysis of the influence of process variations and mismatch is also possible; this is done either by doing corner analysis (worst-case approach) or by Monte Carlo simulations (statistical variations of the device parameters).

Table 5.5.: Dimensions of OTA_1

Parameter		**Value**	**Unit**
$I_{BIAS\_var\_min}$		1	[μA]
$I_{BIAS\_var\_max}$		50	[μA]
C_L		15	[pF]
$m_1 = m_2$	W	64	[μm]
	L	1	[μm]
$m_1^* = m_2^*$	W	64	[μm]
	L	1	[μm]
$m_{L1} = m_{L2}$	W	24	[μm]
	L	1	[μm]
$m_3 = m_4$	W	151.2	[μm]
	L	2	[μm]
$m_5 = m_6$	W	28	[μm]
	L	0.35	[μm]
$m_7 = m_8$	W	32	[μm]
	L	0.35	[μm]
$m_9 = m_{10}$	W	96	[μm]
	L	1	[μm]

Table 5.6.: Characteristics of OTA_1 with C_L=15pF

Parameter	**Unit**	$I_{BIAS\_var\_min}$	$I_{BIAS\_var\_max}$
g_{m_m1}	[μS]	24.5	533
G_{m1}	[μS]	14	275
g_{o1}	[nS]	7.45	1'100
f_{dp1}	[Hz]	79	11'600
f_{ndp1}	[MHz]	18.4	202
A_{v0_1}	[dB]	65.5	48
PM	[°]	90	90
CMIR	[V]	0.7 - 2.65	0.62 - 1.95
linearity	[%]	0.1	0.1
Δv_{in}	[mV]	$\pm$100	$\pm$40
linearity	[%]	1	2

Table 5.7.: Dimensions of OTA_2

Parameter		Value	Unit
I_{BIAS}		60	[μA]
$t_1 = t_2$	W	6	[μm]
	L	0.35	[μm]
$t_3 = t_4$	W	8	[μm]
	L	0.35	[μm]
$t_5 = t_6$	W	64	[μm]
	L	4	[μm]

Table 5.8.: Characteristics of OTA_2 with C_L=500fF

Parameter	Value	Unit
g_{m_m2}	190	[μS]
G_{m2}	95	[μS]
g_{o2}	6.8	[μS]
f_{dp2}	2.1	[MHz]
A_{v0_2}	29	[dB]
PM	92	[°]

Table 5.9.: Dimensions and characteristics of the low-pass filter

Parameter		Value	Unit
I_{BIAS_LP}		10	[nA]
C_{LP}		20	[pF]
$p_1 = p_2$	W	1	[μm]
	L	24	[μm]
$p_3 = p_4$	W	1	[μm]
	L	20	[μm]
f_{LP}		685	[Hz]

After the separate verification of each inductance component, three simulations show the behavior of the designed inductance. First, in Fig. 5.21, the inductance variation range at f_{tr}=500kHz is shown for different corner simulations (typical case *(tm)*, worst speed case *(ws)* and worst power case *(wp)*). Note the big value differences between the two extreme cases *wp* and *ws*. Moreover, it has to be stated that the targeted range from L_{min}=0.15mH to L_{max}=3mH is not respected. We nevertheless decided to implement this solution in the first demonstrator: instead of using an inductance for each component, the internal inductance X'_d is merged with the transmission line inductance L_{tl}. Details can be found in Section 5.5.

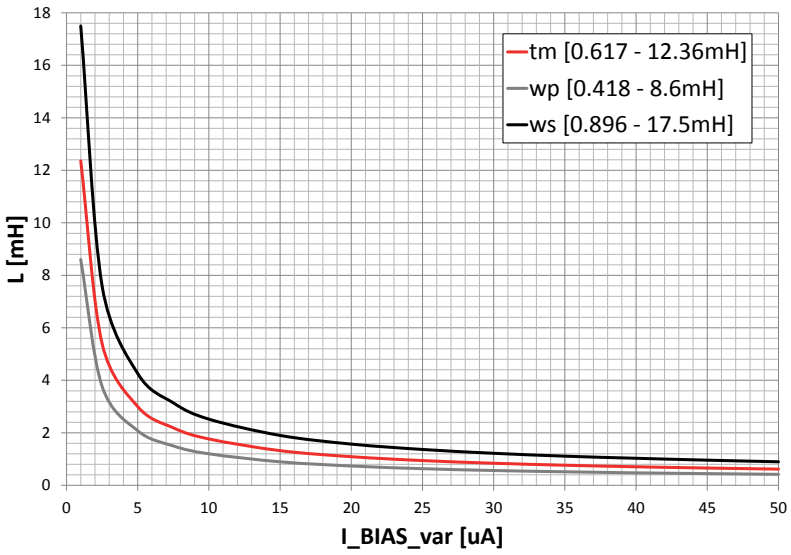


Figure 5.21.: Simulated inductance value variation at 500kHz ($tm/ws/wp$)

Fig. 5.22 illustrates the Bode plot of the equivalent impedance for a 1.5mH inductance and also for different corner simulations. The targeted operating range of the emulator is highlighted. The current is calibrated in order to obtain in each simulation case an inductance of 1.5mH. Doing the same simulation for L_{min} and L_{max} shows that, in the most unfavorable situation, the phase error can reach 5° at 500kHz.

The stability of the designed inductance is tested applying a small and a big voltage step at the terminals of L_{min}. The results also confirm stability for worst case simulations. Note that *(ws)*-cases are at the edge of stability.

The third simulation is to check that the designed inductance is able to find appropriate OPs in each possible case. Therefore, two inductances were connected together and the OP at their connection point V_B was observed. Fig. 5.24 illustrates the test configuration. A Monte Carlo analysis shows that the implemented offset reduction block fixes an accurate OP for each possible offset (see results in Fig. 5.23). At the same time, the generated offset currents (I_A, I_B and I_C) are also depicted.

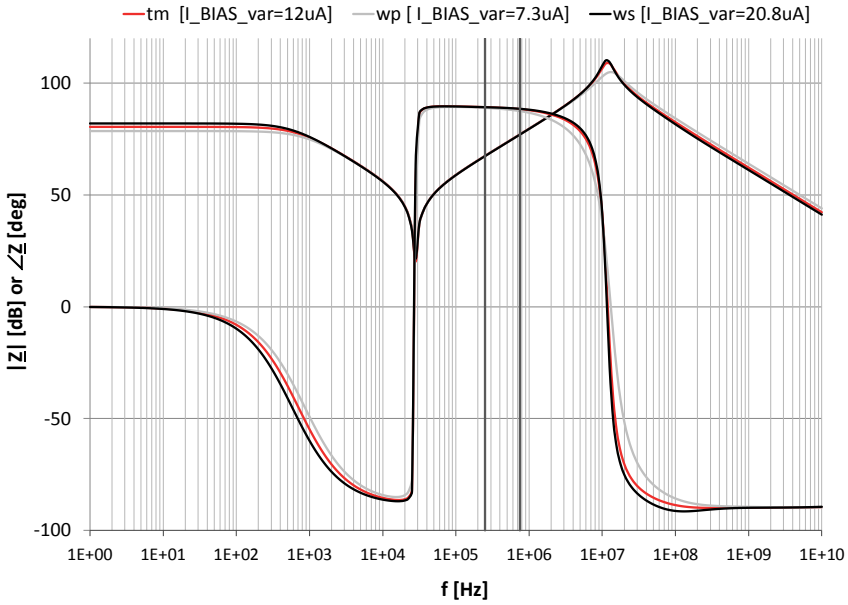


Figure 5.22.: Equivalent impedance (magnitude and phase) for an inductance ($tm/ws/wp$) of 1.5mH with highlighted operating range

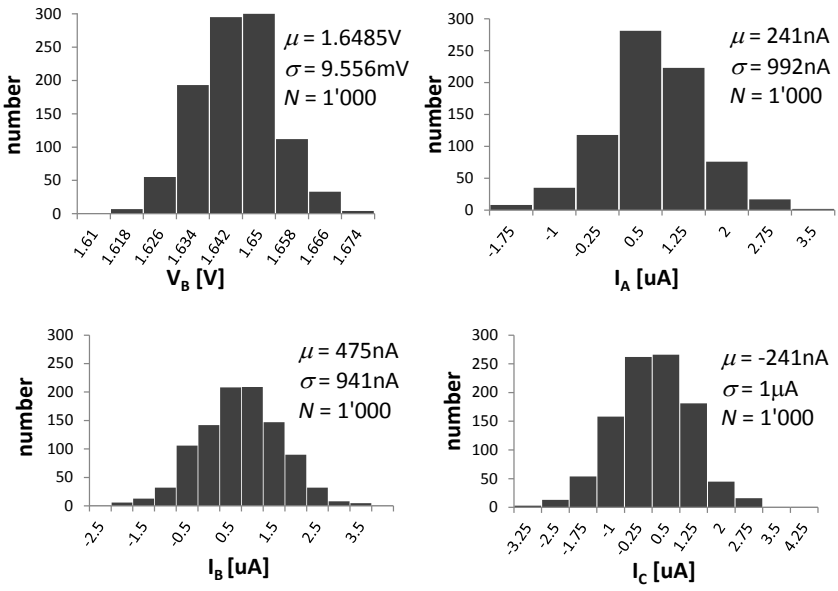


Figure 5.23.: Monte Carlo OP analysis results for 1'000 runs

Finally, we simulate the inductance in its normal application environment: the first AC emulation demonstrator topology. Thereby, the inductances and the output stage of the generators are simulated using their transistor-level implementation. All other blocks are

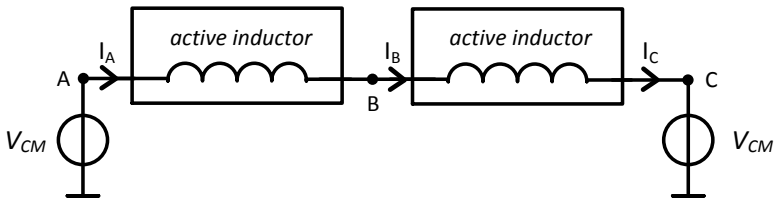


Figure 5.24.: Test configuration for operating point verification

kept behavioral. The topology and the applied scenario are illustrated in Fig. 5.25. Of particular interest, in terms of stability studies, is a topology using the smallest possible inductance value. Therefore, the real-world characteristics of its elements are chosen as listed in Table 5.10.

A time t_{sc} after setting off the emulator, a short circuit is applied at 0% of transmission line TL_{10a}. A certain time t_{clr} later, the line is reconnected. Transmission line TL_{10b} remains disconnected during the whole emulation and damping is applied only to reach the steady-state condition.

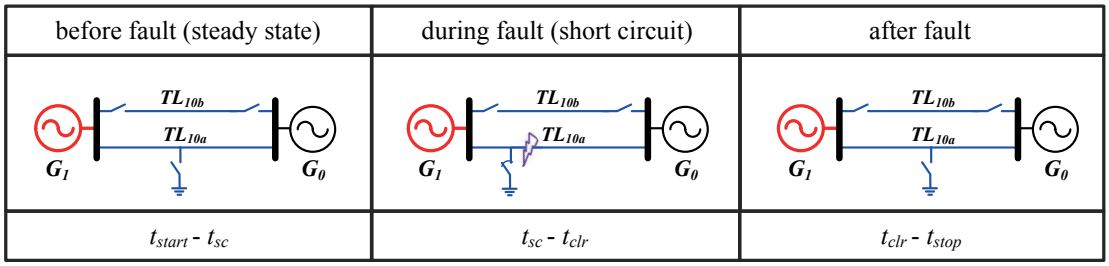


Figure 5.25.: Emulated scenario

Table 5.10.: Real-world characteristics of the reference topology

	Parameter		Value	Unit
Generator 0	E'_0	Internal voltage	1	[p.u.]
G_0	δ_0	Electrical angle	0	[deg]
Generator 1	P_1	Active power	1.15	[p.u.]
G_1	Q_1	Reactive power	0.9	[p.u.]
	M_1	Inertia factor	0.0265	$[s^2\omega_0^{-1}]$
	X'_{d1}	Internal impedance	0.265	[p.u.]
	E'_1	Internal voltage	1.36	[p.u.]
Line TL_{10a}	L_{01}	Reactance	0.11	[p.u.]
225km	R_{01}	Resistance	0.005	[p.u.]
Line TL_{10b}		disconnected		

Fig. 5.26 shows the electrical angle δ_1 for the different corner simulations compared to a behavioral simulation. Additionally, the CCT results are indicated. This example very accurately shows the impact of process variations on the designed blocks. Moreover, Fig. 5.27 illustrates the current for the same simulation. This permits the analysis of the dependence between stability of the inductance and CM-variation of the current. It is as was expected: the CM-variation is the most important in the least stable case. Note that the CM-variation does not affect the accuracy of the CCT results. Indeed, taking into account the worst possible cases analyzed, they are within an acceptable range of ±10%, and therefore validate the transistor-level design of the inductance.

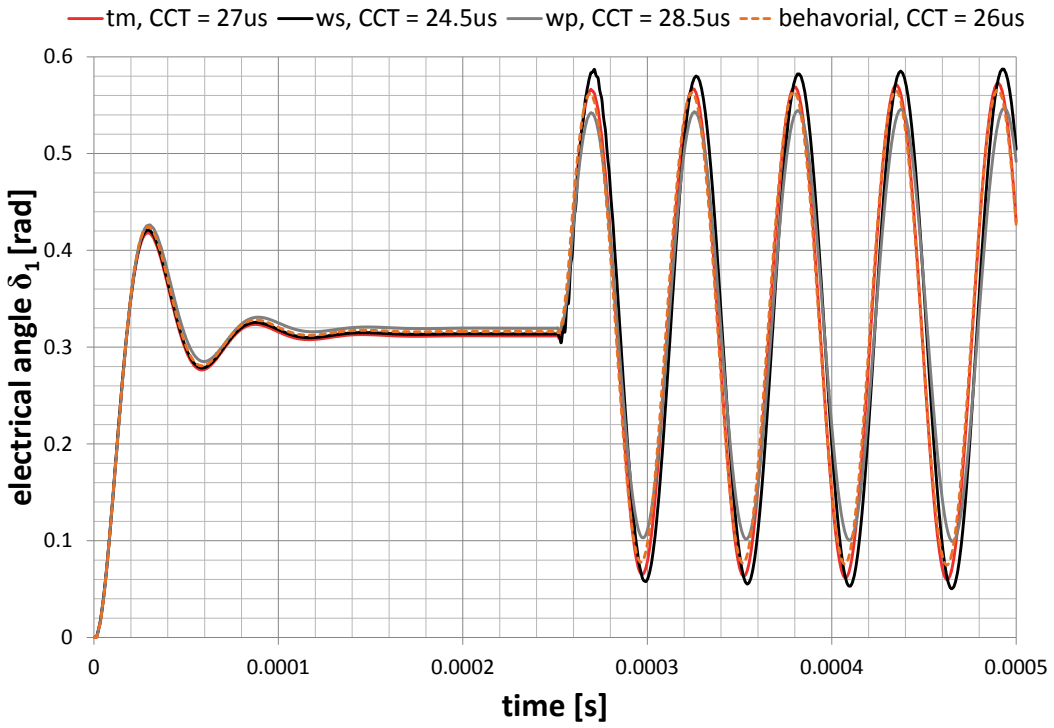


Figure 5.26.: Emulated electrical angle δ_1 (*ws, wp, tm and behavioral*) for $t_{sc} = 250.5\mu$s, $t_{dsc} = 7\mu$s. (*ew*)

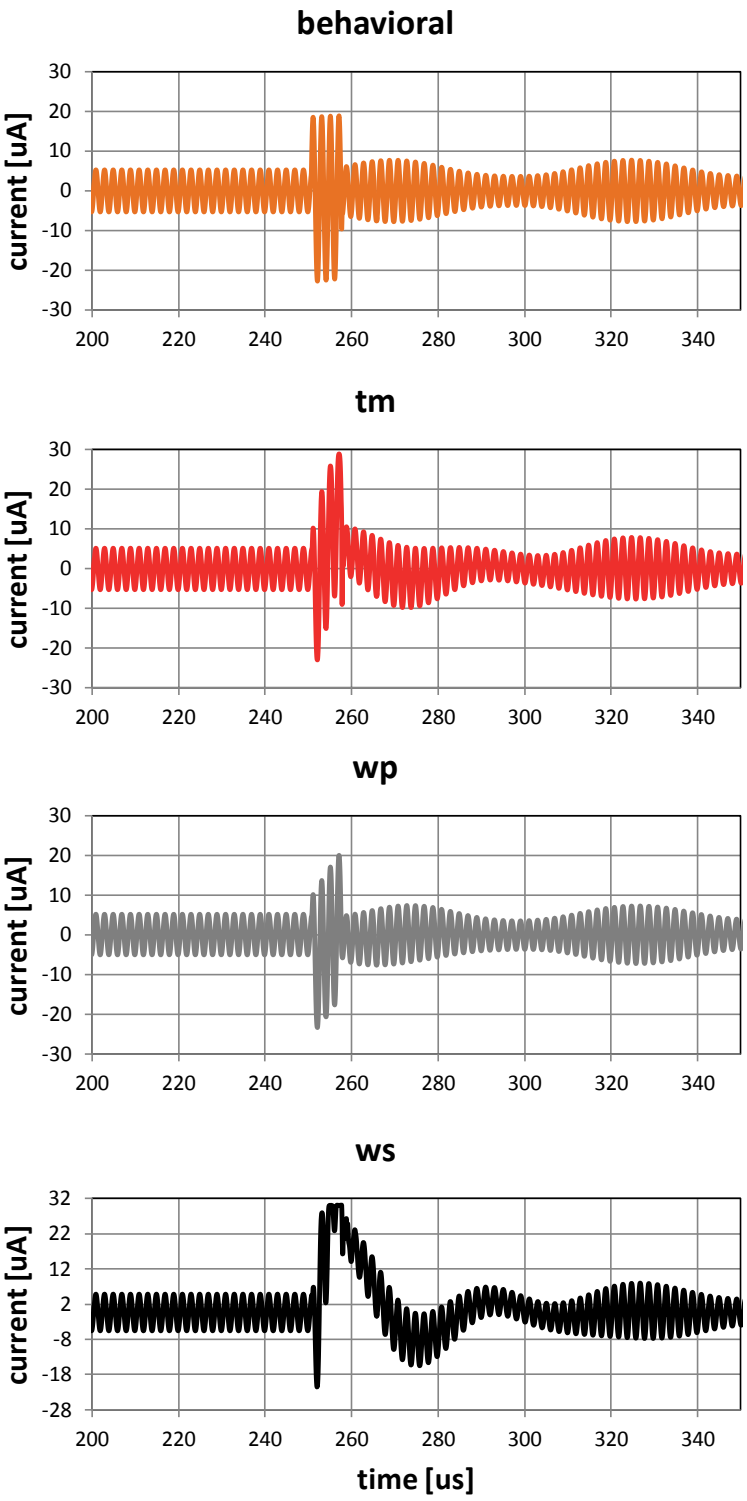


Figure 5.27.: Emulated current (*ws, wp, tm and behavioral*) for $t_{sc} = 250.5\mu$s, $t_{dsc} = 7\mu$s. (*ew*)

5.3. Voltage controlled oscillator design

The overall generator can be seen in Fig 5.2. It is composed of a VCO, including a voltage and a current copy structure, presented in this section, and a reduced swing equation computation solver, presented subsequently in a separate section. The former is implemented in microelectronics, and the latter using discrete electronics on Printed Circuit Board (PCB).

5.3.1. Specification and topology choice

Using the shrink and downscaling factors defined in Section 5.2.4, and the application specific considerations of Section 5.2.1, the following specifications can be extracted.

F_0	:	f_{tr}= 500kHz
Δf_{out_min}	:	F_0 ±100kHz
v_{in0}	:	V_{CM}=1.65V
E'	:	$k_v \pm 10\% = 80\text{mV} \pm 8\text{mV}$

F_0, v_{in0} and E' are characteristics of the VCO as defined in Section 4.2.2. Δf_{out_min} defines the minimal necessary frequency variation range. Moreover, the relationship between the control voltage and the output frequency has to be linear and has to contain a possibility to synchronize the generators.

A classical way to implement linear sine-wave VCOs is to use untuned oscillator topologies, which typically create a triangular output signal. This triangular output is then connected to a sine-shaping circuit [66]. We have applied this principle: The block diagram of our VCO is as illustrated in 5.28. The VCO structure can be divided into three blocks: a triangular waveform VCO, a triangular to sine waveform converter and an output stage containing the voltage and current copy structures.

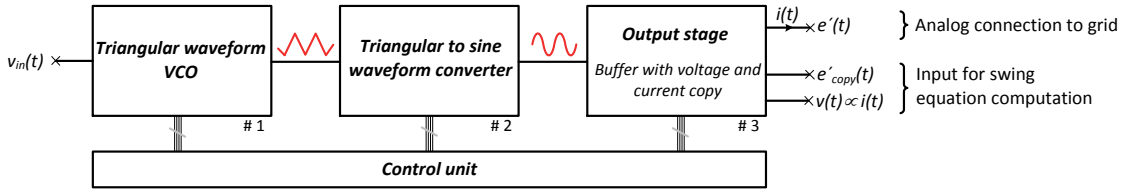


Figure 5.28.: Block diagram of the VCO including an output stage copying the current and the voltage at its terminal

Before presenting the implementation of the three blocks separately, the influence of a generator creating a distorted sine waveform has to be analyzed. As such, the behavioral simulations conducted in Section 4.5.2 are repeated using a highly distorted sine wave

(THD=11%):

$$e'_{dist}(t) = E' \sin(\omega t + \delta) + 0.1E' \sin(2\omega t + \delta) + 0.05E' \sin(3\omega t + \delta) + 0.01E' \sin(4\omega t + \delta) + 0.007E' \sin(5\omega t + \delta) \quad (5.33)$$

Comparing the results obtained by the ideal and the distorted simulation shows that the error on the electrical angles (δ_1 and δ_2) is never bigger than 0.4°. Fig. 5.29 depicts this absolute difference between the ideal result and the result obtained with the distorted signal.

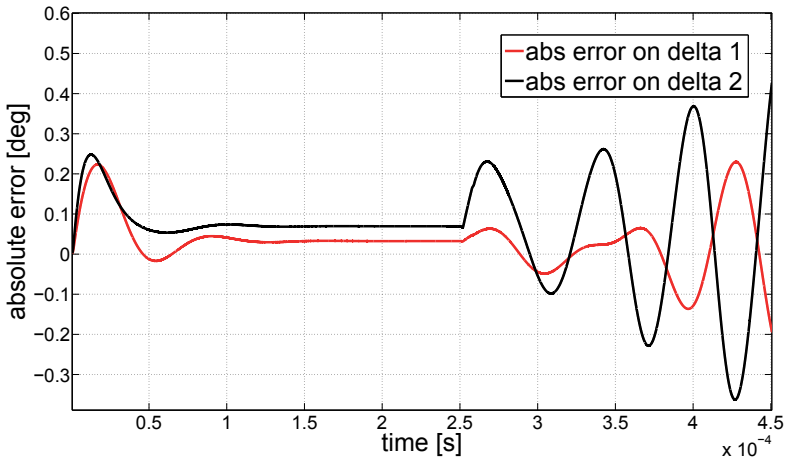


Figure 5.29.: Absolute error on the emulated electrical angles (δ_1 and δ_2) between the results obtained using a distorted VCO and an ideal VCO for $t_{sc} = 250.52\mu$s, $t_{dsc} = 7\mu$s and x = 50%. (ew)

As these good results are obtained from an extreme case, i.e. a very high distortion, the use of such VCO topology is justified.

5.3.2. Triangular waveform Voltage Controlled Oscillator

Fig. 5.30 shows the implementation of the triangular waveform VCO. Basically, it consists of an integrator cascaded with a bistable circuit. The bistable circuit is implemented with 2 comparators and 2 NAND-cells. The operating principle of the VCO is as follows. First, the input voltage v_{in} is transformed into a current, using R_{var_8bit}. This current is integrated by the capacitance $C_{fix} + C_{var\_4bit}$ until the voltage over the capacitance reaches $V_{CM} + h_{var}$ or $V_{CM} - h_{var}$. At this moment, the bistable circuit switches the state, causing the differential pair to change the direction of the current in the capacitance, creating a triangular voltage waveform with amplitude h_{var}. Its frequency is varied by

changing the amount of current in the capacitances and is defined as:

$$f_{out} = \frac{i_{in}}{4h_{var}(C_{fix} + C_{var\_4bit})} \tag{5.34}$$

$$i_{in} = \frac{v_{in}}{R_{var\_8bit}} \tag{5.35}$$

Hence, the relation between input voltage v_{in} and output frequency f_{out} is linear. The switch S_{sync} in parallel with C_{fix} and C_{var_4bit} is implemented to synchronize the VCOs. All elements described with the subfix var are programmable. h_{var} is thereby used to calibrate the amplitude of the triangular waveform in order to have an optimal input for the triangular to sine waveform converter, despite possible process variations. R_{var_8bit} and C_{var_4bit} are used to adjust F_0 for the defined v_{in_0}. This is necessary, as the integrated passive elements can vary up to 30%. The voltage to current converter stage is designed to guarantee Δv_{in} up to 2.2V for a current i_{in_max} not exceeding 4μA. A summary of the characteristics of the implemented VCO can be found in Table 5.11.

Table 5.11.: Characteristics of the triangular waveform VCO

Parameter	**Value**	**Unit**
C_{fix}	3.6	[pF]
C_{var_4bit}	2.4	[pF]
R_{var_8bit}	1	[MΩ]
K_0	303'030	[-]
v_{in_max}	2.2	[V]
f_{out_max}	666.5	[kHz]

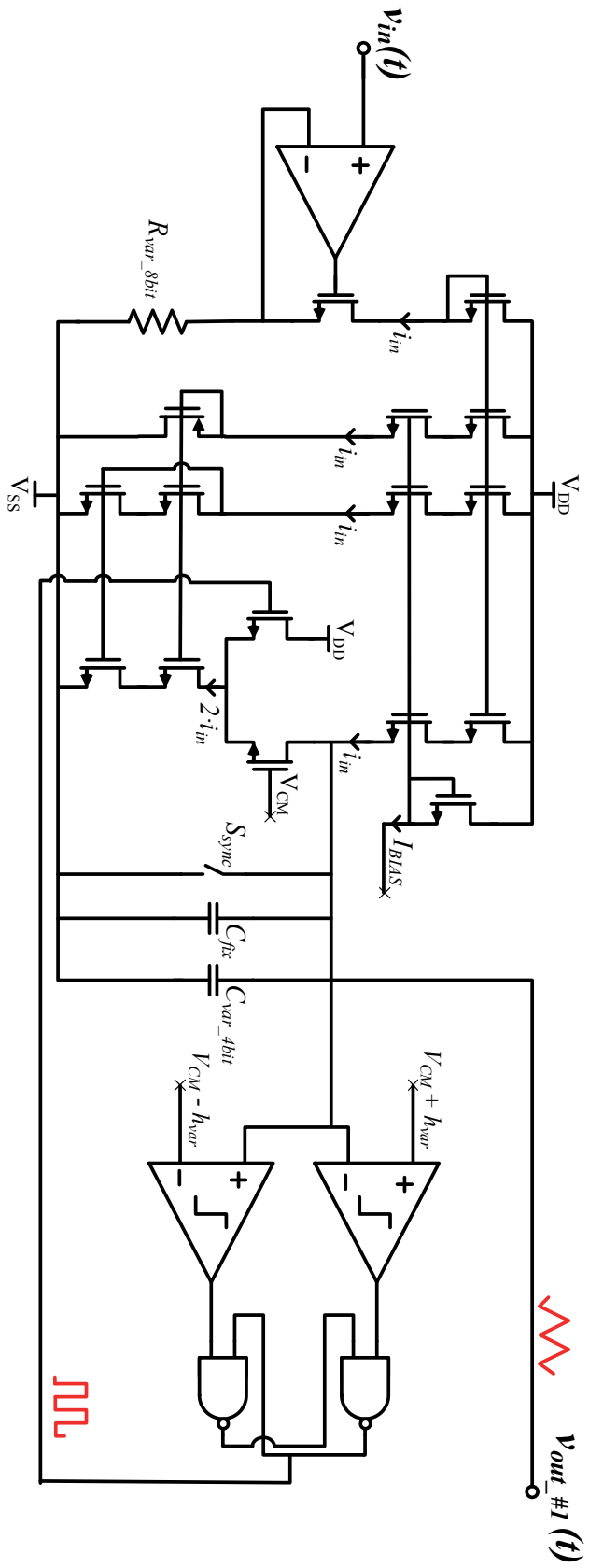


Figure 5.30.: Triangular waveform VCO

5.3.3. Triangular to sine waveform converter

We use the non-linear characteristics between the input voltage difference Δv and the output current i_{out} of a differential pair in strong inversion as the triangular to sine waveform converter. This method was proposed by J. Fattaruso et al. in [67]. Fig. 5.31 illustrates the transfer characteristic of such a differential pair.

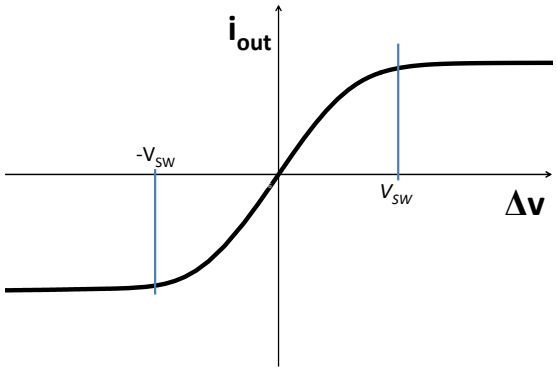


Figure 5.31.: Typical transfer characteristic of a differential pair

$\pm V_{SW}$ is the differential input voltage required to completely switch the pair. Beyond this input voltage, the differential output current saturates to the bias current, I_{BIAS}, applied to the differential pair. Analytically, it is shown in [67] that this characteristic can be expressed as

$$i_{out} = \begin{cases} -I_{BIAS} & v_{in} < -V_{SW} \\ \left(\frac{v_{in}}{V_{SW}}\right)\left(2 - \left(\frac{v_{in}}{V_{SW}}\right)^2\right)^{1/2} & -V_{SW} < v_{in} < V_{SW} \\ I_{BIAS} & V_{SW} < v_{in} \end{cases}$$

where v_{in} is normalized to V_{SW}.

We have chosen to implement this converter as shown in Fig. 5.32 using a simple OTA topology in open loop configuration.

The added output resistor R_{var_7bits} therefore has two tasks:

1. Decrease the output resistance of the converter, in order to achieve an attenuation instead of a gain ($A_{v0} < 1$). This guarantees that the converter never saturates and that sufficient bandwidth ($> f_{out\_max}$) is provided.

2. The 7-bit programmable resistance, R_{var_7bits}, is connected as potentiometer, allowing E', the amplitude of the sine waveform, to be adjusted.

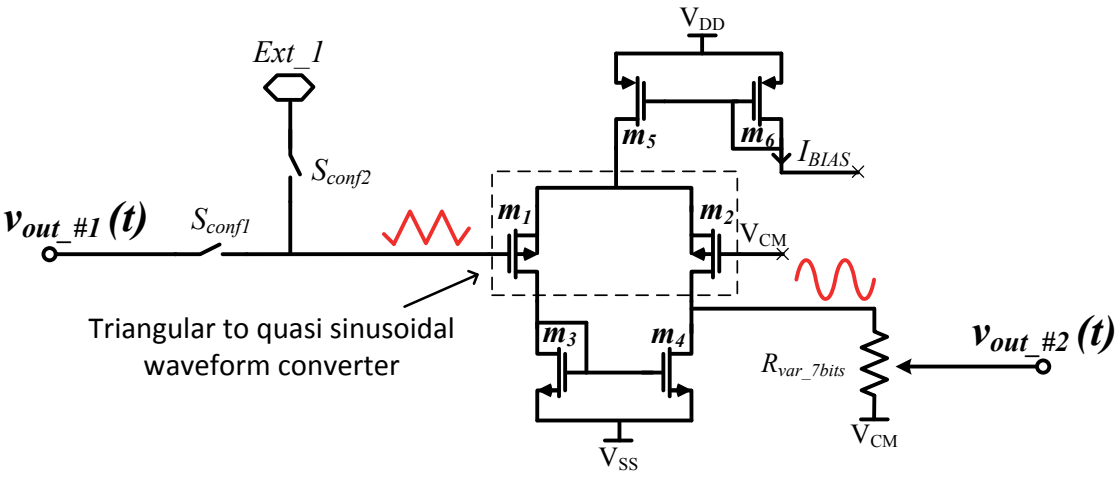


Figure 5.32.: Transistor level of the triangular to sine waveform converter

The differential pair is designed for a proper conversion of a triangular signal with amplitude ±300mV.

Table 5.12.: Characteristics of the triangular waveform VCO

Parameter		Value	Unit
I_{BIAS}		10	[μA]
R_{var_7bits}		10	[kΩ]
$m_1 = m_2$	W	7	[μm]
	L	1	[μm]
$m_3 = m_4$	W	4	[μm]
	L	1	[μm]
$m_5 = m_6$	W	12	[μm]
	L	1	[μm]
THD (worst case)		1.5	[%]
A_{v0}		-5.5	[dB]
f_{dp}		190	[MHz]

5.3.4. Current and voltage copy

The output stage of the VCO is illustrated in Fig. 5.33. The scope of this output stage is, firstly, to interface the VCO with the transmission lines. This function is fulfilled by a conventional buffer stage. Its second task is to provide the inputs of the reduced swing equation solver, i.e. a copy of the current $i(t)$ and the voltage $e'(t)$.

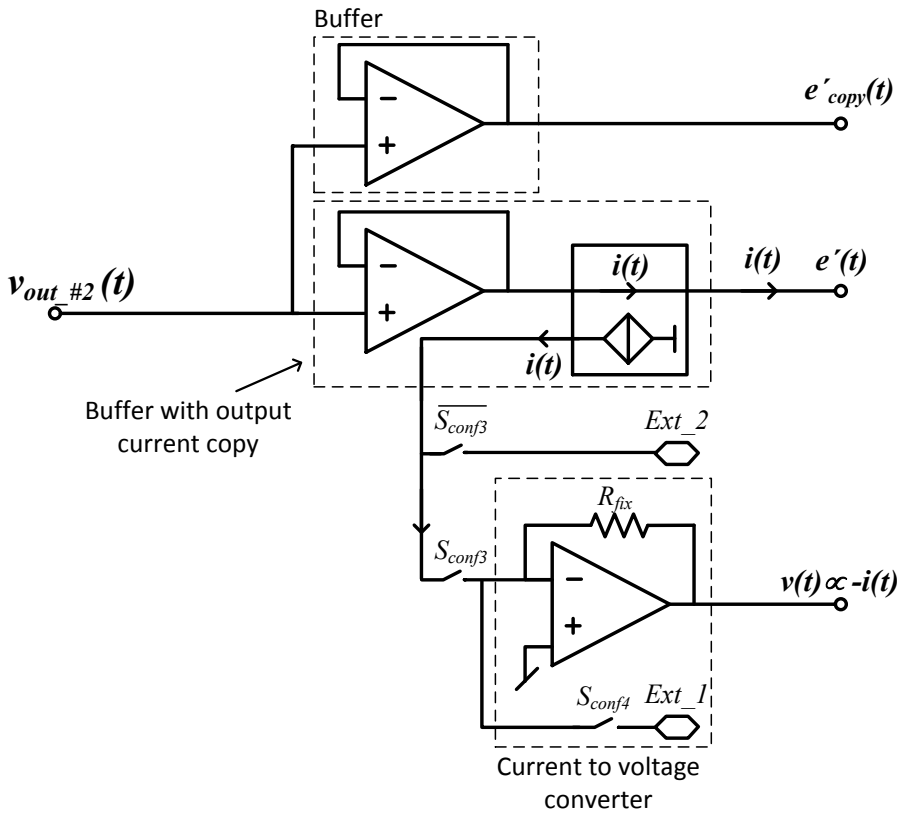


Figure 5.33.: VCO output stage

The voltage is copied by adding a voltage follower. It is implemented using a Miller amplifier, which is designed to tolerate up to $C_L = 50pF$ at its output. This is necessary because this stage is connected to a pad.

The current is copied by adding a dedicated output stage to a conventional Miller amplifier. This stage permits the reproduction of the current in a third stage using cascoded current mirrors. The entire transistor level of this amplifier is illustrated in Fig. 5.34, and the transistor dimensions and bias currents are shown in Table 5.14. Note the huge current in the Miller stage (I_2=200μA) necessary to guarantee stability. Finally, since the current also needs to be externally available, a current to voltage converter, which tolerates up to $C_L = 50pF$ at its output, is implemented on chip. Its operation can be described as follows:

$$v(t) = -i(t)R_{fix}. \tag{5.36}$$

Consider that the integrated resistance R_{fix} can vary up to 30% due to process variations. Therefore, it has to be possible to determine the effective value of R_{fix} after integration and its variation has to be compensated by a tunable gain in the reduced swing equation solver.

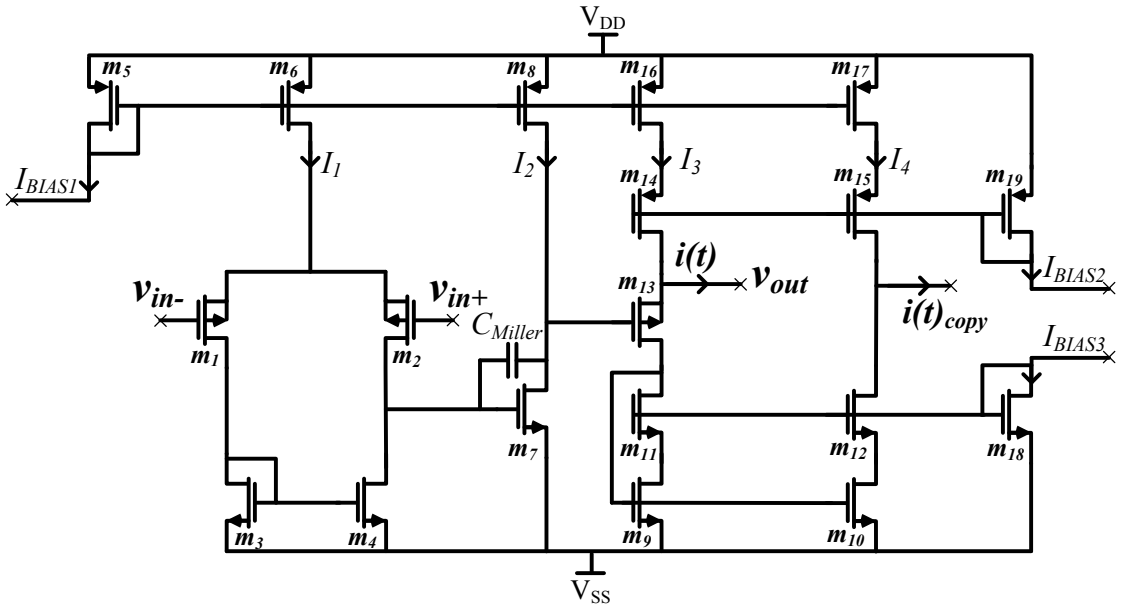


Figure 5.34.: Transistor level of the buffer with integrated current copy stage

The main characteristics of the three amplifiers are listed in Table 5.13.

Table 5.13.: Characteristics of the three amplifiers composing the output stage

Buffer containing a current copy stage (C_L=2pF, C_{Miller}=2.5pF)		
Parameter	Value	Unit
A_{v0}	84.9	[dB]
f_{GBW}	19.5	[MHz]
PM	56	[°]
Voltage copy (C_L=50pF, C_{Miller}=5pF)		
Parameter	Value	Unit
A_{v0}	73	[dB]
f_{GBW}	16.4	[MHz]
PM	61	[°]
Current to voltage converter (C_L=50pF, C_{Miller}=5pF, R_{fix}=50kΩ)		
Parameter	Value	Unit
A_{v0}	71.5	[dB]
f_{GBW}	16.4	[MHz]
PM	61	[°]

Table 5.14.: Dimensions of the buffer containing a current copy stage

Parameter		**Value**	**Unit**
I_{BIAS1}		10	[μA]
I_{BIAS2}		10	[μA]
I_{BIAS3}		10	[μA]
C		2.5	[pF]
$m_1 = m_2$	W	80	[μm]
	L	0.5	[μm]
$m_3 = m_4$	W	16	[μm]
	L	1	[μm]
m_5	W	16	[μm]
	L	2	[μm]
$m_6 = m_{16} = m_{17}$	W	64	[μm]
	L	2	[μm]
m_7	W	160	[μm]
	L	20	[μm]
m_8	W	320	[μm]
	L	2	[μm]
$m_9 = m_{10}$	W	20	[μm]
	L	2	[μm]
$m_{11} = m_{12}$	W	24	[μm]
	L	0.7	[μm]
m_{13}	W	100	[μm]
	L	0.35	[μm]
$m_{14} = m_{15}$	W	72	[μm]
	L	9	[μm]
m_{18}	W	2	[μm]
	L	3	[μm]
m_{19}	W	7	[μm]
	L	3	[μm]

5.4. Reduced swing equation solver implementation

Within the framework of this thesis, the reduced swing equation solver is realized on PCB with discrete components. Details are visible in Fig. 5.35.

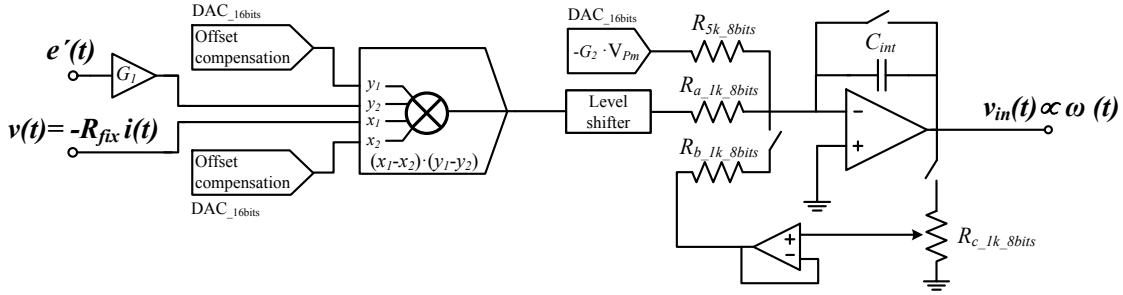


Figure 5.35.: Detailed system level of the realized reduced swing equation solver

Consequently, the implemented reduced swing equation can be expressed as follows:

$$v_{in}(t) = \underbrace{\frac{G_2}{R_{5k\_8bits}C_{int}}V_{P_m}}_{\frac{\Psi^2}{MK_SK_0}P_m} - \underbrace{\frac{R_{fix}G_1}{R_{a\_1k\_8bits}C_{int}}e'(t)i(t)}_{\frac{\Psi^2}{MK_0k_S}p(t)} - \underbrace{\frac{k}{R_{b\_1k\_8bits}C_{int}}\int v_{in}}_{\frac{\Psi^2}{Mk_SK_0}P_D}, \quad (5.37)$$

where k is the attenuation factor set by the potentiometer $R_{c\_1k\_8bits}$. It corresponds to the emulated reduced swing equation presented in Section 4.2.4 and Fig. 4.8.

Several calibration possibilities are provided. The offset voltages of $e'(t)$ and $v(t)$ are compensated at the input of the integrator. Gain G_1 compensates the variation of the on-chip resistor R_{fix} used in the current to voltage converter. The level shifter contains the possibility of compensating the offset of the multiplier.

5.5. Effective demonstrator topology

The microelectronic developments in this chapter lead to the effective implementation of the demonstrator as shown in Fig. 5.36. The active inductance includes the series resistance, which is, for this first implementation, kept constant. Moreover, the switches are also directly included in the active inductance topology. In order to be able to emulate realistic topologies and scenarios, the internal inductance X'_{d1} of Generator G_1 is part of the transmission line inductance (see also Fig. 5.2). This is a consequence of the inductance value tuning range.

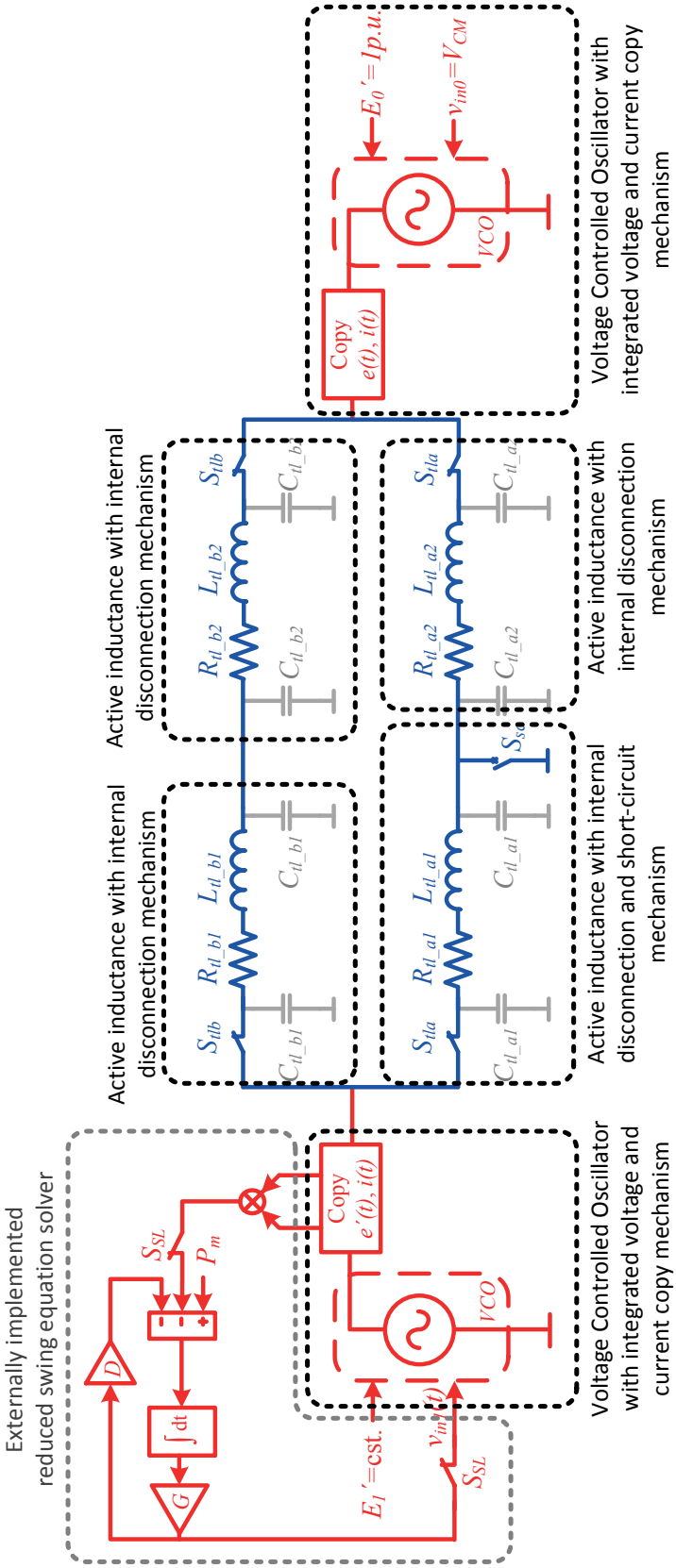


Figure 5.36.: Effectively implemented demonstrator topology

5.6. Integrated circuit

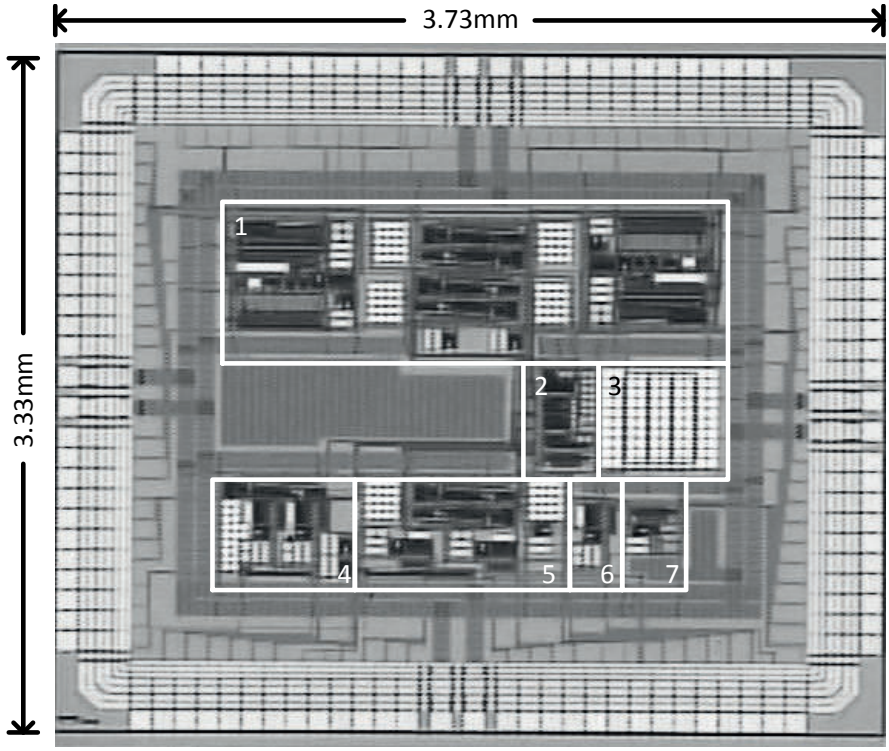


Figure 5.37.: Micrograph of the implemented integrated circuit

An integrated circuit has been fabricated in a conventional 0.35μm 3.3V CMOS technology and encapsulated in a standard 120-pin Ceramic Quad Flat Pack (CQFP) package. The complete ASIC, including the padring, occupies 12,42mm^2. Fig. 5.37 shows a micrograph of the implemented circuit. In addition to the first AC emulation demonstrator, the following blocks are implemented on it:

Block 1 The first AC emulation demonstrator, as illustrated in the previous section in Fig. 5.36 and with I/O interface to the swing equation solver, which is implemented externally on PCB.

Block 2 A current biasing block, which locally creates all constant currents needed to bias the other blocks, except the generators.

Block 3 An array of eight matched 15pF-capacitors needed as conversion capacitors C_L of the implemented inductances.

Block 4 A single inductor to be tested and characterized separately, including the necessary buffers to connect external voltage sources and to measure the current at the terminals of the inductor.

Block 5 Two inductors connected in series in order to test the offset reduction mechanism, including the necessary buffers to connect external voltage sources, as well as to measure the current at the terminals and the voltage in the middle of the two inductors.

Block 6 A current copy amplifier to be tested separately.

Block 7 A capacitance measurement circuit for determining the precise value of the conversion capacitors C_L by determining the value of one of the capacitors of block 3.

The area of each block is listed in Table 5.15.

Table 5.15.: Areas of the different blocks implemented on the first ASIC

Block	1	2	3	4	5	6	7	complete
Area [mm^2]	1.440	0.137	0.288	0.310	0.447	0.076	0.068	12,42

An inductance alone including the complete biasing structure covers 0.17mm^2. The conversion capacitor C_L and the low-pass filter capacitor C_{LP} occupy together 40% of this area.

6 Chapter 6. Measurement results

Chapter overview

This chapter presents experimental data of the developed ASIC. First, the test environment is briefly described, explaining its main blocks. Then, the inductance and the VCO are characterized separately. Their frequency ranges and programmability are investigated, and the functionality of the offset reduction block of the inductance is analyzed. Finally, the last section presents results of the AC emulation demonstrator. Its operating principle is presented step-by-step and illustrated with signal captures. Critical Clearing Time (CCT) measurements for different topologies are compared to simulated results, underlining the accuracy of the results.

6.1. Test environment

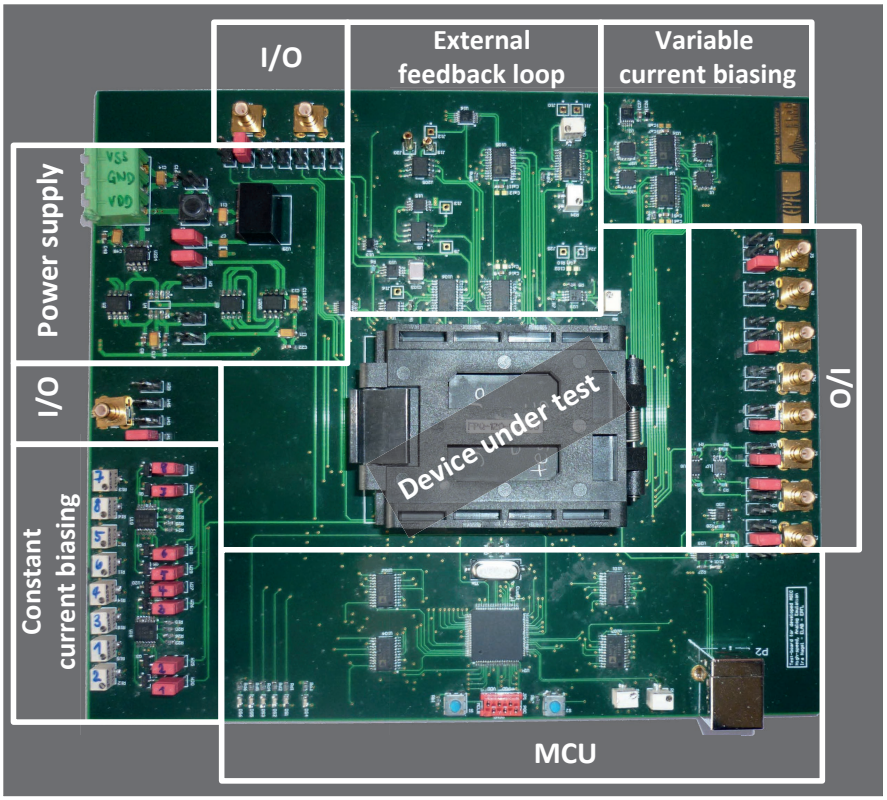


Figure 6.1.: Photo of the test environment (17cm x 15cm)

Fig. 6.1 shows the environment used to validate and characterize the created ASIC. It is a 6-layer PCB, which generates all necessary supply voltages and biasing currents to feed the ASIC. Moreover, it contains the reduced swing equation solver (= external feedback loop), which is implemented using discrete components.

Focus was put on testability; hence, compactness was ignored. A socket, which permits the testing of different ASIC-samples, is the centerpiece of the PCB. A Microcontroller Unit (MCU) is used to configure the different blocks contained in the integrated circuit and on the PCB. Therefore, digital and analog parts of the PCB are supplied separately. I/O connectors are used to visualize signals and to input test signals. The acquisition of the signals can either be done using these I/O interfaces or through the MCU. Furthermore, the test environment previews calibration possibilities, mainly for manual calibration of the elements. This has to be considered during the evaluation of the results.

6.2. Inductance characterization

The inductance is characterized using block 4 of the ASIC (refer to Fig. 5.37 in Section 5.6). This block contains a single inductor, including the necessary buffers to connect external voltage sources and to measure the current at the terminals of the inductor. Fig. 6.2 shows the described topology. The value of the inductance L is tuned through the biasing current I_{BIAS_var}.

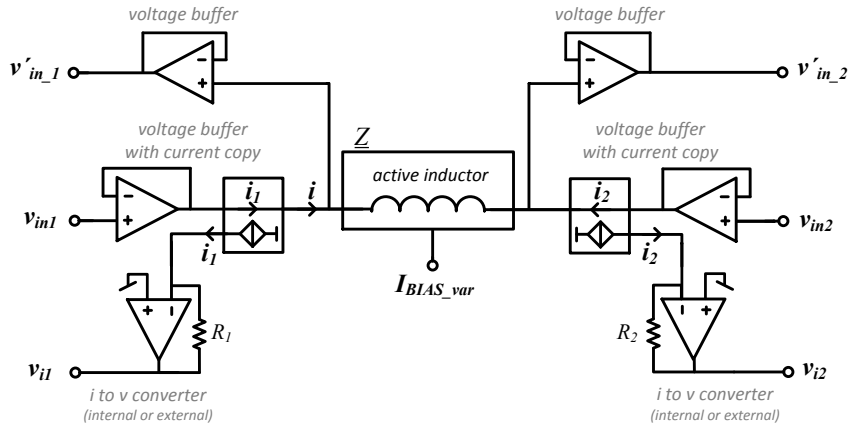


Figure 6.2.: Topology of block 4

Applying two sinusoidal voltage signals v_{in1} and v_{in2} with equal frequency and phase but different amplitudes and observing the resulting current $v_{i1} = i \cdot R_1$, permits the magnitude of the impedance to be characterized as follows:

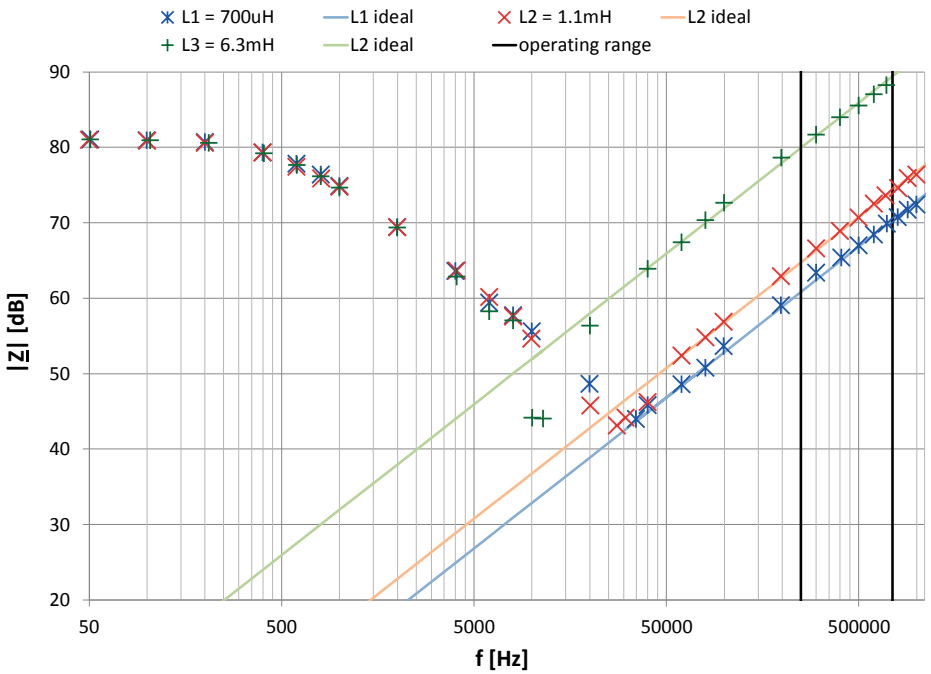
$$|\underline{Z}| = \frac{\hat{V}'_{in\_1} - \hat{V}'_{in\_2}}{\hat{V}_{i1}/R_1}. \tag{6.1}$$

The phase $\angle\underline{Z}$ is determined by measuring the phase shift between v_{i1} and v'_{in_1}. Obviously, the same developments can be made for $|\underline{Z}|$ and the phase shift using v'_{in_2} and $-v_{i2}$.

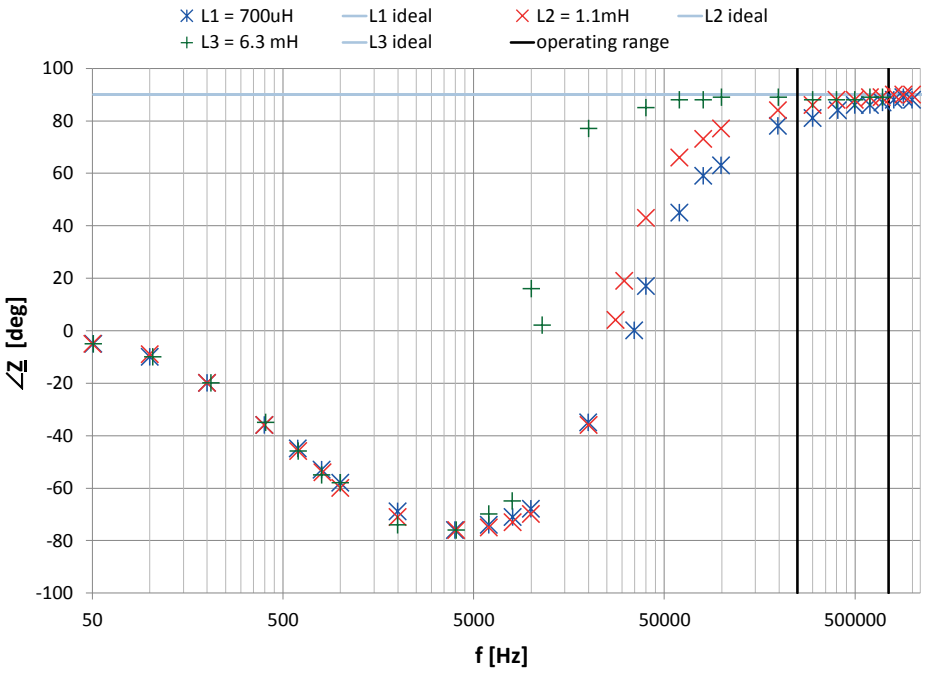
Fig. 6.3 shows the frequency characterization between 50Hz and 1MHz of the inductance for three different inductance values: L_1=700μH, L_2 = 1.1mH and L_3=6.3mH.

Fig. 6.4(a) depicts the tuning range of L varying I_{BIAS_var} from 1μA to 50μA at 500kHz and, therefore, in the middle of the frequency operating range. Fig. 6.4(b) illustrates the corresponding phase shift between the current and the voltage wave. Fig. 6.5 shows the same measurements for different ASIC-samples. No significant differences appear. All inductances can at least be varied between 750μH and 10mH for a variation of I_{BIAS_var} from 1μA to 50μA.

The results confirm the theoretical development made in the previous chapter.

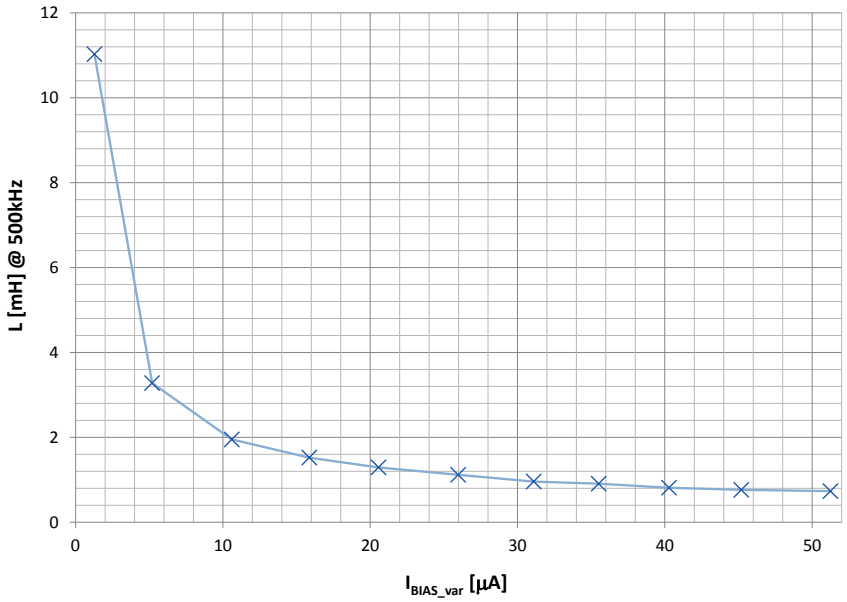


(a) Bode plot of the magnitude of the equivalent impedance

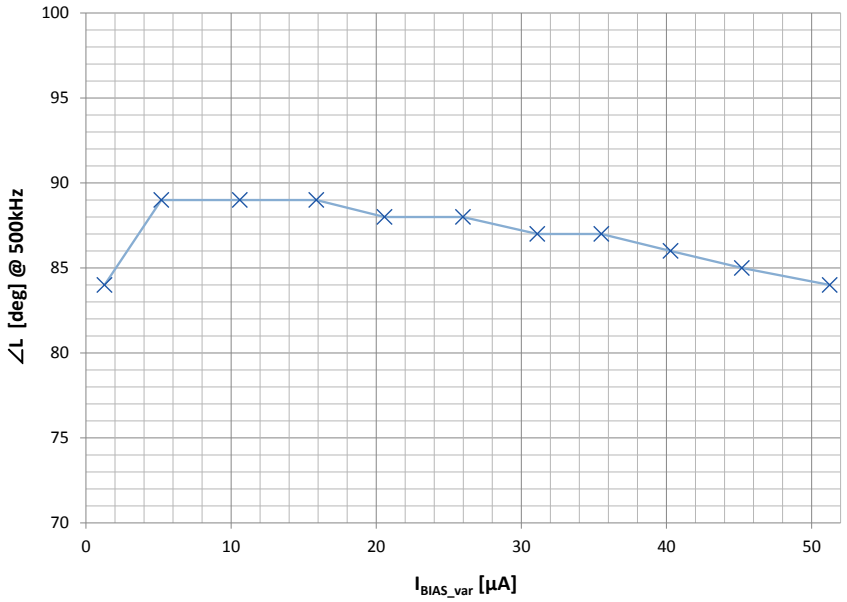


(b) Bode plot of the phase of the equivalent impedance

Figure 6.3.: Measured frequency behavior of the inductance illustrated by the impedance Bode plots of magnitude $|\underline{Z}|$ and phase $\angle\underline{Z}$. The targeted operating range from 250kHz to 750kHz is highlighted.

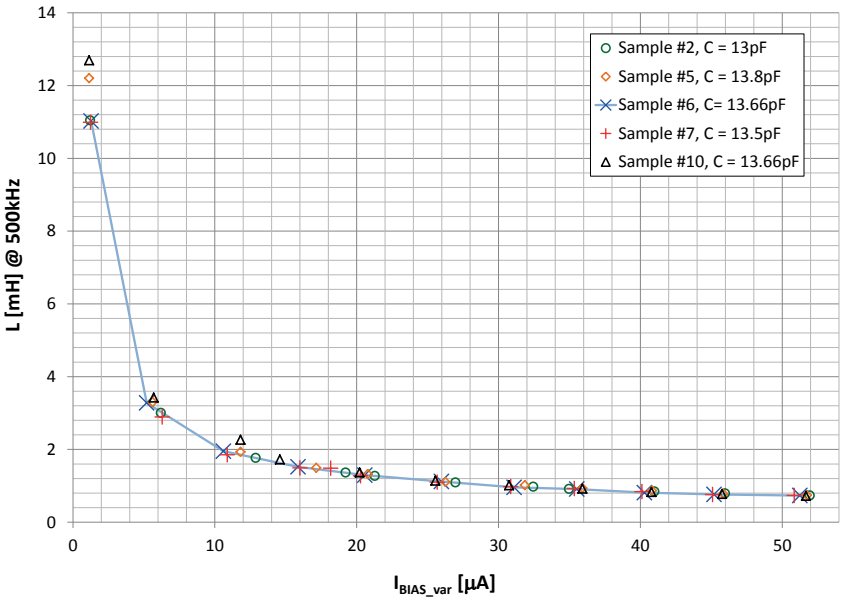


(a) Inductance magnitude variation

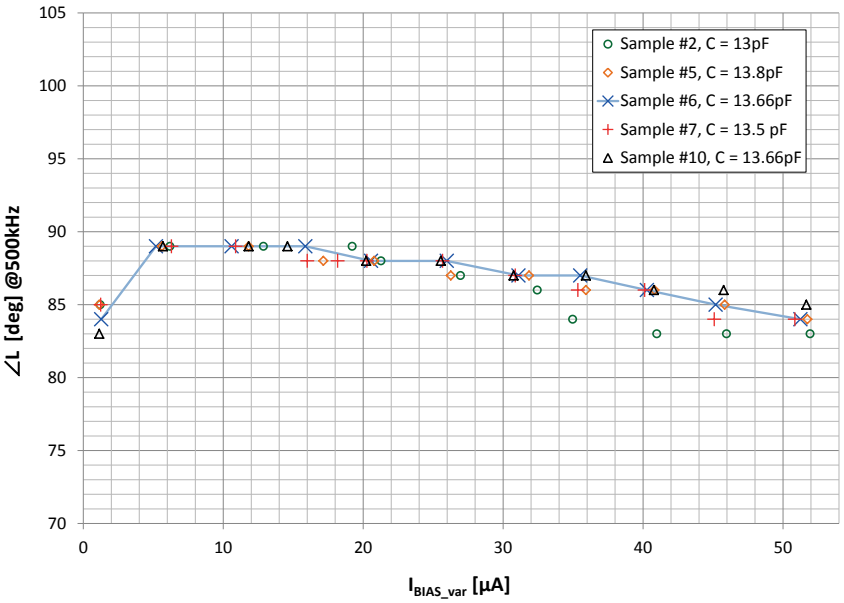


(b) Phase shift between current and voltage for the different inductance values, measured with a resolution of 1°.

Figure 6.4.: Inductance tuning range characterization at 500kHz for different biasing currents I_{BIAS_var}



(a) Inductance magnitude variation



(b) Phase shift between current and voltage for the different inductance values, measured with a resolution of 1°.

Figure 6.5.: Inductance tuning range characterization at 500kHz for different biasing currents I_{BIAS_var} and different ASIC-samples. For each sample the measured value of the conversion capacitor is indicated.

Besides the tuning and the frequency range of the inductance, also the functionality of the offset reduction mechanism is of interest. This is the reason for block 5 of the ASIC (see Fig. 5.37 in Section 5.6). It is made up of two inductors connected in series, including the necessary buffers to connect external voltage sources and to measure the current at the terminals and the voltage in the middle of the two inductors. Fig. 6.6 illustrates this topology. As before, two sinusoidal voltage signals v_{ina} and v_{inb} with equal frequencies but

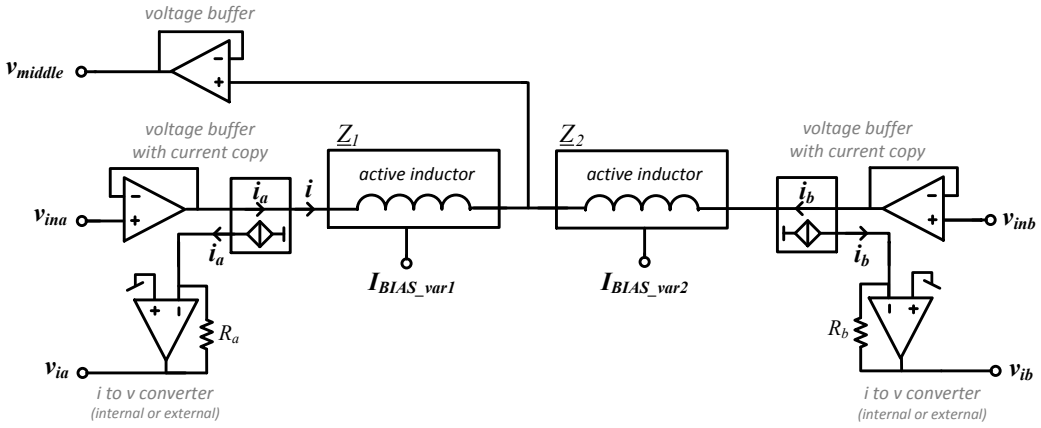


Figure 6.6.: Topology of block 5

different amplitudes are applied. These input signals are shown in Fig. 6.7(a). Fig. 6.7(b) and Fig. 6.7(c) depict v_{ia}, v_{ib} and v_{middle} for $L_1 = L_2 = 1.85$mH and for $L_1 = 718\mu$H & $L_2 = 1.85$mH, respectively. The Common Mode (CM) voltage set for the integrated circuit is indicated in gray. This allows the offset of the signals to be seen at a glance. Different observations have to be commented.

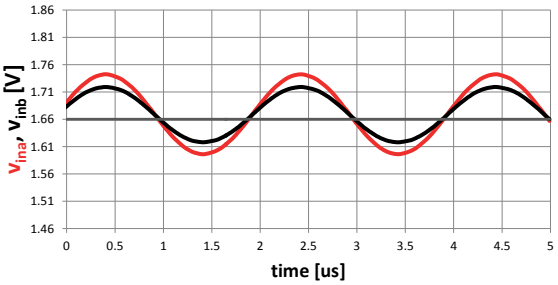
- The signals v_{middle} illustrated in Fig. 6.7(b) and Fig. 6.7(c) confirm that the offset mechanism works properly. No saturation appears. Table 6.1 shows further results. The CM voltage of the input signals shown in Fig. 6.7(a) is changed to different values, observing the behavior of the CM voltage of v_{middle}. Even for 600mV of input CM voltage difference, the offset reduction mechanism keeps the inductances operating. The limiting factor becomes, in this case, the current to voltage conversion block, which is not able to handle this significant offset.

- The observation of v_{ia} and v_{ib}, which are proportional to the current i propagating in the circuit, permits to confirm the theoretical developments regarding the current copy and the current to voltage conversion block in Section 5.3.4. Indeed, it is confirmed that
$$\frac{v_{ia}}{R_a} = -\frac{v_{ib}}{R_b}, \tag{6.2}$$
as long as the CM-components of the signals are not taken into account.

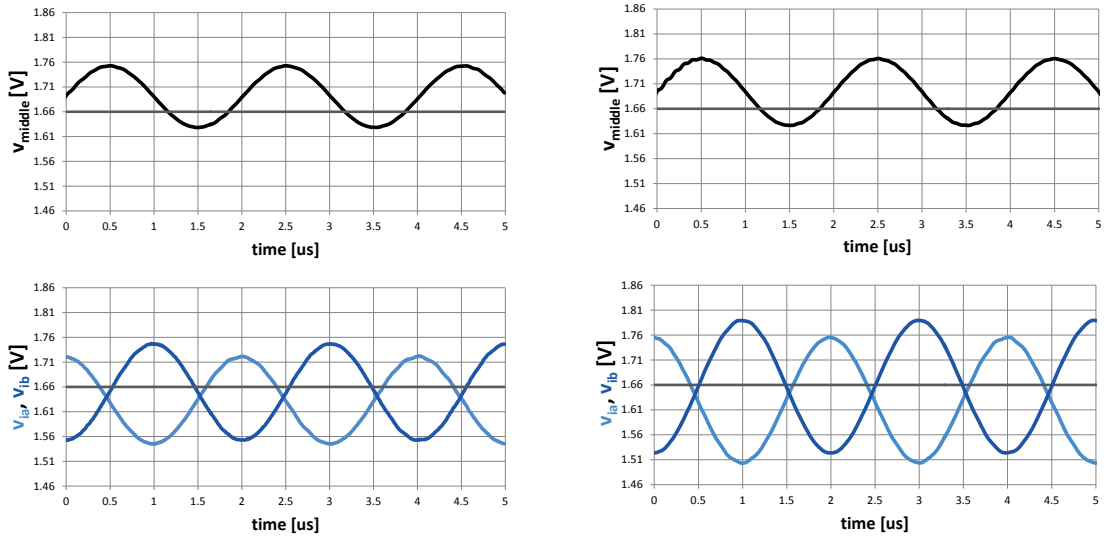
- It is observed that there is a mismatch between R_a and R_b. Measurements confirm this mismatch: R_a=44.1kΩ and R_b=46.58kΩ.

Table 6.1.: Offset reduction mechanism test results for $L_1 = 718\mu\text{H}$ and $L_2 = 1.85\text{mH}$

ΔCM	[V]	0.07	0.20	0.60	0.10	0.10
CM of v_{ina}	[V]	1.67	1.67	1.95	1.35	1.91
CM of v_{inb}	[V]	1.60	1.47	1.35	1.45	2.05
CM of v_{middle}	[V]	1.66	1.60	1.68	1.43	2.00



(a) Input voltages v_{ina} and v_{inb}



(b) $L_1 = L_2 = 1.85\text{mH}$

(c) $L_1 = 718\mu\text{H}$ and $L_2 = 1.85\text{mH}$

Figure 6.7.: Observed signals during the offset reduction mechanism test using block 5. Different L values are applied keeping the same input voltages v_{ina} and v_{inb}. V_{CM} is indicated in gray.

6.3. VCO characterization

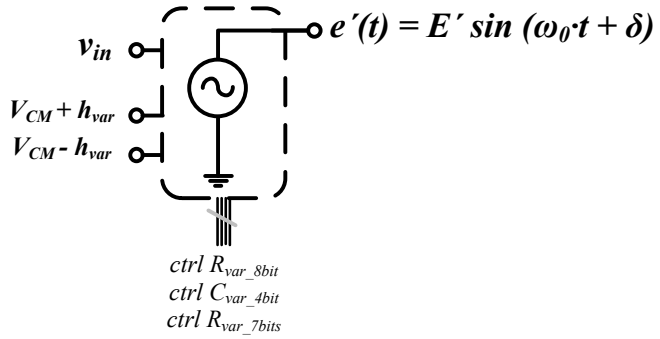


Figure 6.8.: Schematic view of the VCO, including all necessary input signals and defining the output signal $e'(t)$

The VCO is characterized using the first AC emulation demonstrator, which is included in block 1 of the ASIC (refer to Fig. 5.37 in Section 5.6). This block contains two VCOs, one emulating the slack generator, and the other as part of generator G_1. Both can be tested separately. Fig. 6.8 reminds all necessary input signals of the VCO. Please refer to Section 5.3.1 for explanations of the working principle, and to Fig. 5.30 and Fig. 5.32 for the detailed implementation of the VCO. First, a calibration cycle has to be executed as follows:

1. Set v_{in} to v_{in_0}. R_{var_8bits} to midscale, C_{var_4bits} to 0 and R_{var_7bits} to fullscale.

2. Adjust h_{var} to optimize the amplitude of the triangular waveform in order to reduce the distortion.

3. Calibrate R_{var_8bits}, C_{var_4bits} in order to obtain F_0.

4. Set the amplitude E' through R_{var_7bits}.

According to the use of the VCO in the first AC emulation demonstrator, we set:

$$\begin{aligned} v_{in\_0} &= V_{CM} \\ F_0 &= 500\text{kHz} \\ E' &= 1p.u. = 80\text{mV} \end{aligned}$$

The obtained AC signal and its spectrum can be seen in Fig. 6.9. The variation of the amplitude E' using R_{var_7bits} is illustrated in Fig. 6.11. The amplitude can be varied between 10mV and 110mV. Furthermore, by varying v_{in}, the frequency of $e'(t)$ is changed, as shown in Fig. 6.12. The slowest and fastest signals are obtained for v_{in_min}=30mV and v_{in_max}= 2.25V, and correspond to a frequency of 10kHz and 645kHz respectively. Both signals are depicted in Fig. 6.10. Please note the different time scales.

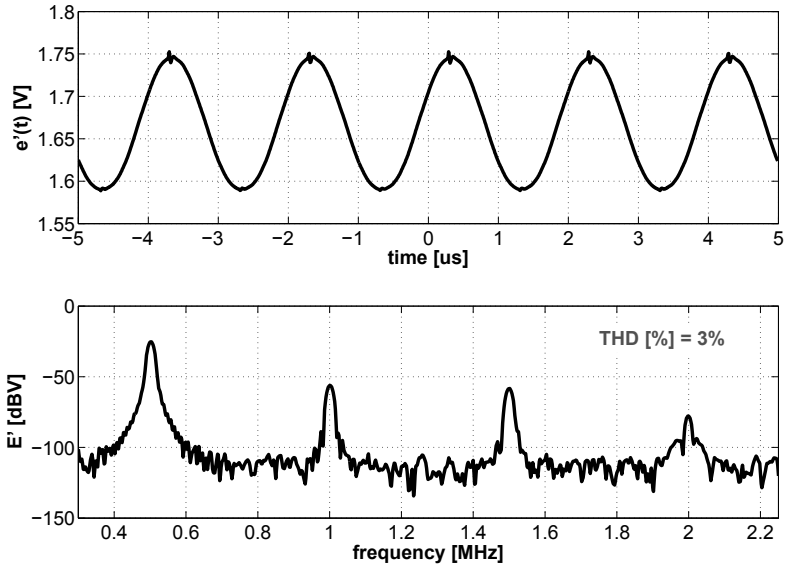


Figure 6.9.: VCO output signal $e'(t)$ for $v_{in} = V_{CM} = v_{in\_0}$, F_0=500kHz and E'=80mV with the corresponding spectrum obtained by Fast Fourier Transform of the time domain signal

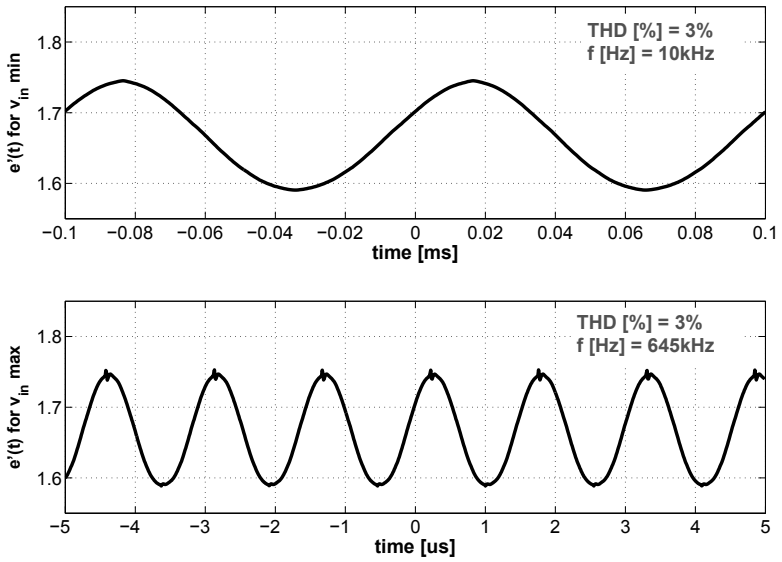


Figure 6.10.: VCO output signals $e'(t)$ for $v_{in} = v_{in\_max}$ and $v_{in} = v_{in\_min}$ both with E'=80mV

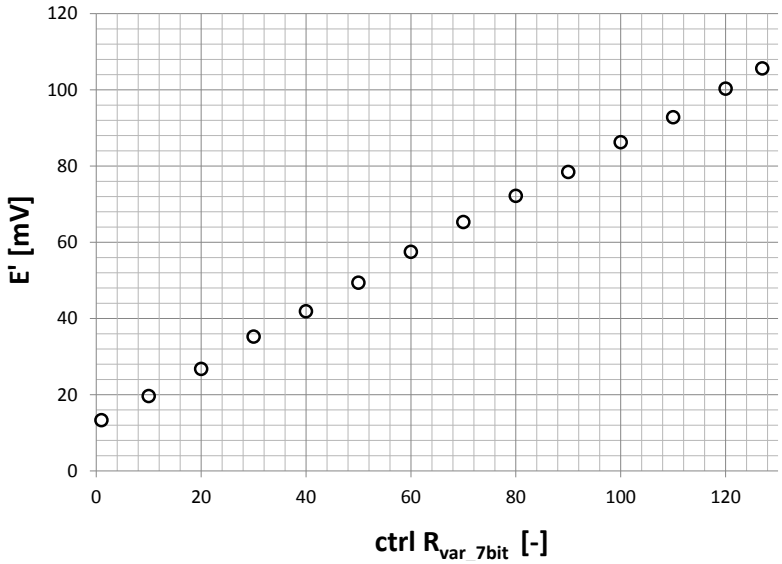


Figure 6.11.: Amplitude E' tuning range varying R_{var_7bits}

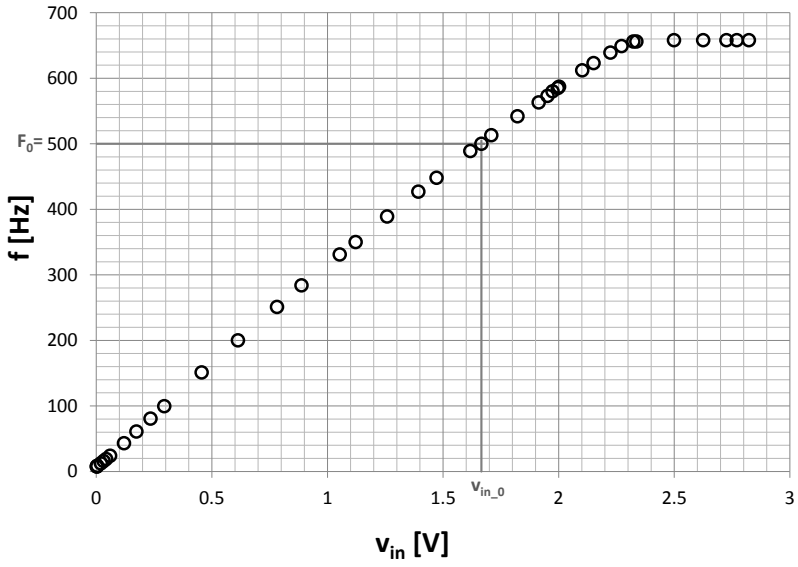


Figure 6.12.: Frequency f of the VCO output signal with respect to the input signal v_{in}

The Total Harmonic Distortion (THD) is computed for these three signals on the basis of their spectra, and using the following formula:

$$THD = \frac{\sqrt{{E'_2}^2 + {E'_3}^2 + {E'_4}^2 + \ldots + {E'_n}^2}}{E'_1}, \tag{6.3}$$

where E'_1 is the amplitude of the fundamental, and E'_2 to E'_n are the amplitudes of the harmonics. A THD of about 3% was obtained for all three signals, considering the harmonics within 2MHz.

These results confirm the theoretical development made in the previous chapter.

6.4. AC emulation demonstrator

This section presents experimental data from the first AC emulation demonstrator. The applied scenario is illustrated in Fig. 6.13. The used real-world characteristics of its elements are listed in Table 6.2. A time t_{sc} after setting off the emulator, a short circuit is applied at 0% of transmission line TL_{10a}. A certain time t_{clr} later, the line is reconnected. Transmission line TL_{10b} remains disconnected during the whole emulation. Damping is applied only to reach the steady state condition. After that, all parameters are set up. Then the damping is removed.

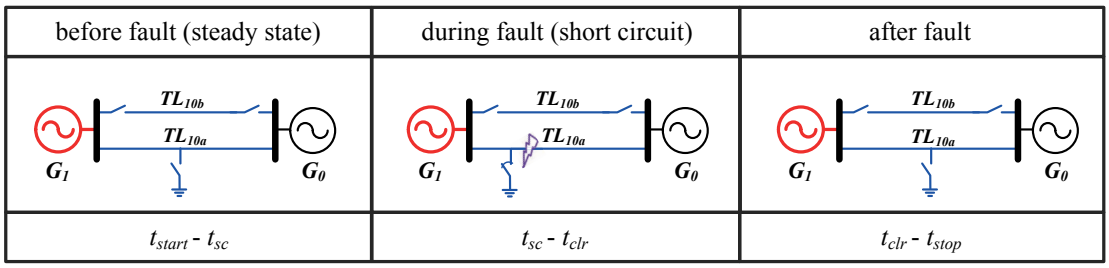


Figure 6.13.: Emulated scenario

Using the described scenario three different aspects are presented:

Emulation flow The operating principle of the emulator is presented step-by-step and illustrated with signal captures.

AC signals The behavior of the AC signals during a short circuit is analyzed for a stable and an unstable case.

Validation The demonstrator is validated by comparing, on the one hand, the steady state and, on the other hand, CCT measurements of the emulator to behavioral simulation results. This is done for different P_m-values.

Table 6.2.: Real-world characteristics of the reference topology

	Parameter		Value	Unit
Generator 0	E'_0	Internal voltage	1	[p.u.]
G_0	δ_0	Electrical angle	0	[deg]
Generator 1	P_1	Active power	1.15	[p.u.]
G_1	Q_1	Reactive power	0.9	[p.u.]
	M_1	Inertia factor	0.0265	$[s^2\omega_0^{-1}]$
	X'_{d1}	Internal impedance	0.265	[p.u.]
	E'_1	Internal voltage	1.36	[p.u.]
Line TL_{10a}	L_{01}	Reactance	0.11	[p.u.]
225km	R_{01}	Resistance	0.005	[p.u.]
Line TL_{10b}		disconnected		

1st aspect: emulation flow

The necessary steps for a successful emulation are listed in Fig. 6.14. After calibration of the external feedback loop, the VCOs and the inductances, the parameters and the topology can be set. Then, once the generators are synchronized, the swing equation loop can be launched, keeping some damping to reach the steady state of the system. Finally, the emulator is ready to analyze the stability impact of a given scenario.

In Fig. 6.14, the different steps are illustrated with signal captures of the scenario described at the beginning of this section. Step 2 shows the synchronized generator voltage signals, and step 3 the AC signals at steady state. Thereby, the upper figure depicts the current and the voltage at the input of the reduced swing equation computation block. Therefore, and as explained in Section 5.3.4, the current is not measured as current, but as voltage proportional to the current. The lower figure shows again the generator voltage signals. The phase shift between the two generator signals is the electrical angle δ_{1_0} of Generator G_1 at steady state. Finally, step 4 contains a figure illustrating a stable and an unstable case by means of the behavior of the input voltage of G_1. This input voltage corresponds to the emulated ω_1.

Obviously steps 0, 1 and 2 don't have to be repeated before every emulation.

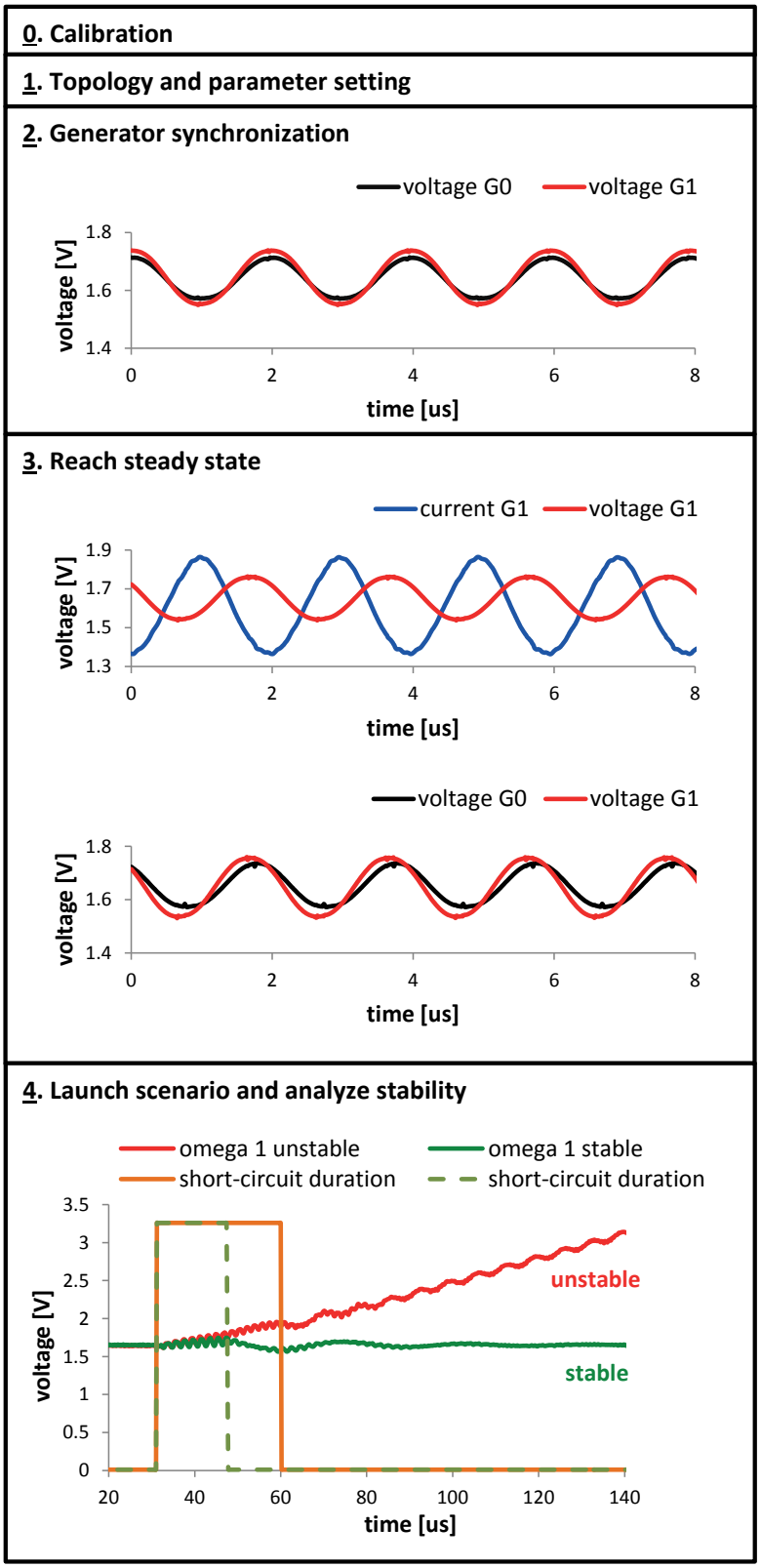
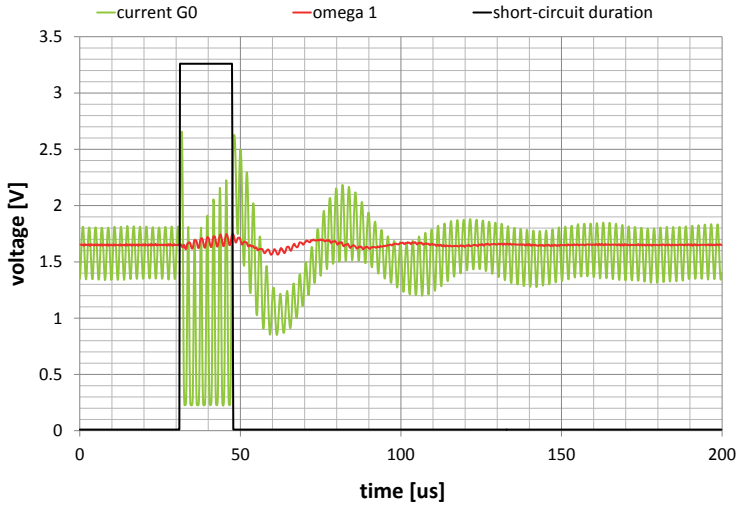


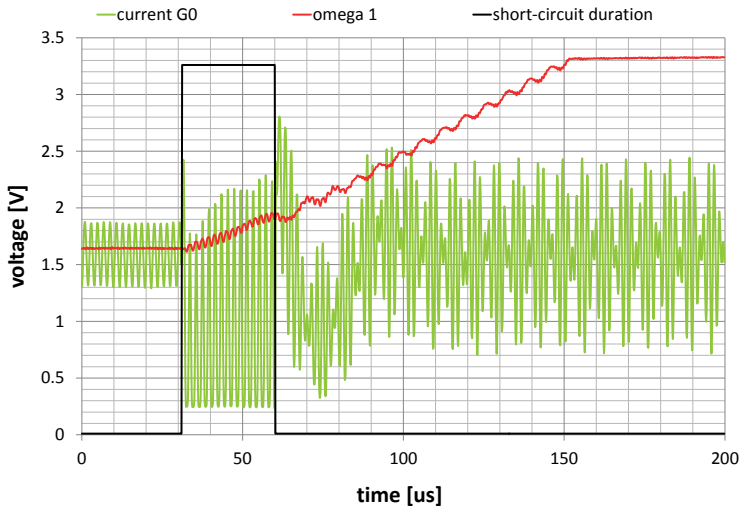
Figure 6.14.: Emulation flow illustrated with measurement results: Steps 0, 1 and 2 don't have to be repeated for every emulation.

2nd aspect: AC signals

It is worth taking a closer look at the AC signals during a stable and an unstable case. To facilitate this, short circuits of t_{dsc}=16.4μs and t_{dsc}=28.8μs are applied and we observe ω_1 and the current propagating on the transmission line. We state that, in the stable case, damping appears, even if no damping is applied. Indeed, the oscillations of ω_1 are attenuated. Moreover, the current saturates during the short circuit. Otherwise, the signals are as expected.



(a) A stable case: t_{dsc}=16.4μs. (*ew*)



(b) An unstable case: t_{dsc}=28.8μs. (*ew*)

Figure 6.15.: Measured emulation results for different short-circuit durations.

3rd aspect: validation

Finally the AC emulation demonstrator is validated, comparing its results to the results obtained by behavioral emulation executed in the Cadence Virtuoso environment using Spectre [52]. In Chapter 4, the results of the behavioral emulator are validated by comparing its results to the results of a numerical simulator.

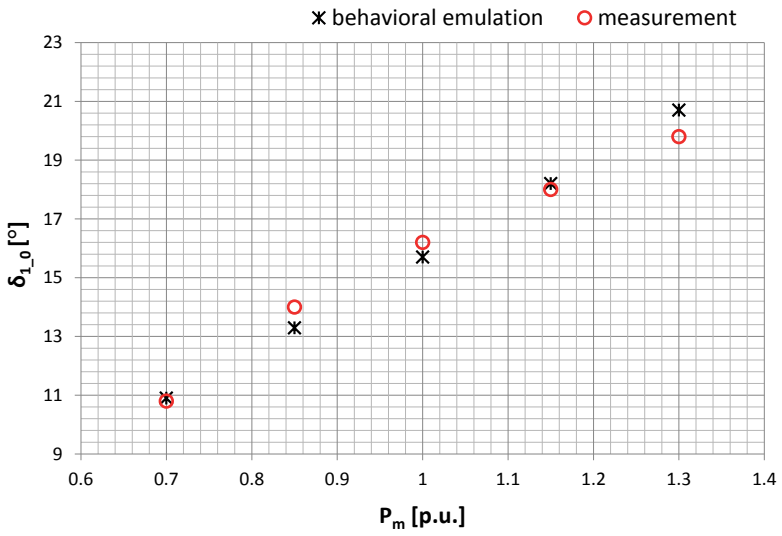


Figure 6.16.: Electrical angle of Generator G_1 at steady state δ_{1_0} for different P_m-values

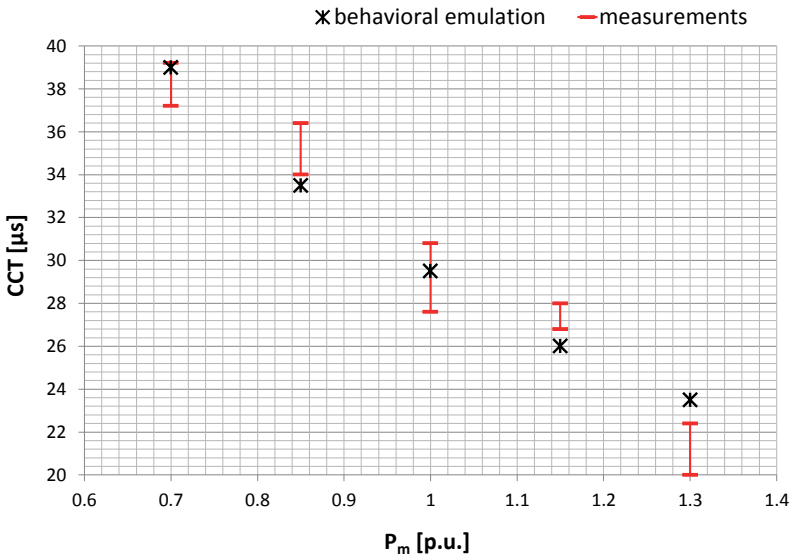


Figure 6.17.: CCT measurement results for repetitive measures with a resolution of 700ns and changing P_m-values (ew)

First, in Fig. 6.16, we validate the electrical angles of G_1 at steady state for different P_m-values of the generator. Repetitive testing permitted the robustness of the results to be confirmed. It is also verified that the same steady state is reached after the emulation of the scenario.

Second, in Fig. 6.17, the results of CCT measurements for different P_m-values are depicted. In this case, repetitive measures led to a range of results.

6.5. Discussion

Several aspects of the presented measurement results have to be discussed before validating the first AC emulation demonstrator.

The characterization of the inductance and the VCO validate the theoretical developments, as well as the design shown in Chapter 5. Both components are tunable and operate in the specified frequency range. Furthermore, the dedicated optimizations developed for application in power system AC emulation are shown to work properly.

The AC emulation demonstrator, which is composed of the designed microelectronic elements and the reduced swing equation block, which is implemented by discrete components on the PCB, works accurately. Results are obtained 10'000 times faster than real time, confirming the high-speed capabilities of AC emulation. Fig. 6.16 affirms that reproducible and accurate results are obtained for steady-state evaluations of different topologies.

Nevertheless, the reader could question the robustness of AC emulation. Indeed, contrary to the steady-state evaluations, repeatability of CCT results is limited and leads to a range of results, as illustrated in Fig. 6.17. This can be traced back to the two imperfections, which appear after the fault and which are visible in Fig. 6.15(a):

1. The saturation of the current during the short circuit.

2. An inadvertent damping after the fault (visible on the ω_1-curve after fault)

The saturation leads to an error in the instantaneous power computation only during the short circuit and falsifies consequently slightly the CCT results. The underestimation of the current needed during a short-circuit is at the origin of this imperfection. Providing more current in the output stages during the redesign of the analog building blocks solves this problem entirely.

Different sources or a combination of them lead to the second imperfection. First, the saturation of the current can assist to the appearance of a damping as late effect. Transistor level simulations confirm, however, that it can not be the unique source of this damping. Second, the CM-variation of the current can cause this damping even if its behavior is

as predicted by simulation (see Section 5.2.5). Indeed, the simulation was done with an ideal reduced swing equation solver neglecting thereby that this variation can saturate the multiplier. This can be identified as the starting point of the damping. Finally, also the low signal level and hence low SNR can assist this damping.

As the damping starts to appear only at the edge of the first oscillation after the fault, it has only marginal impact on the CCT results. That is why the emulation results remain within an acceptable range of $\pm 15\%$ of the simulated values. This permits to validate the functionality of the demonstrator. A dedicated microelectronic implementation of the external feedback loop, taking into account the possible CM-variations during the design of the multiplier, will remove the damping. Moreover the CM-variations at the input of the multiplier will be decreased because the signals can be kept smaller in the case of an integrated solution.

In sum, the promising speed capabilities and the feasibility of AC emulation are largely confirmed. Moreover, it is important to note that only fully integrated solutions providing automated calibration utilities can guarantee robust and accurate results.

Chapter 7.
Conclusion

This work presents the development of a purely analog power system emulation approach, from the theoretical principles to the design and the realization of a first demonstrator. This approach is called the AC emulation approach and is based on analog emulation of the power grid. Its main objective is to overcome the speed limits of commonly used numerical simulators, thereby enabling their use for real-time control and online security assessment.

7.1. Highlights

This thesis starts with a broad focus on the comparison between power system emulation and current numerical simulators by systematically analyzing their speed, modularity, cost and precision. The speed advantage of emulators is explained and an approach to improve the modularity of emulators is presented. Moreover, application examples are shown, aiming to underline that emulators, with their higher-speed, could perfectly complete the very precise but slow numerical simulators.

We then introduce the AC emulation approach, which is a purely analog power system emulation approach. An overview of the power system computation history and the evolution of microelectronics highlights that the renaissance of dedicated analog computation is justified. Modern VLSI technologies can overcome the drawbacks which caused the disappearance of analog computation units in the 1960s.

The uniqueness of the AC emulation approach is that the frequency dependence of the signals is preserved. It is based on the idea of mapping the behavior of the components of the power system one-to-one on CMOS microelectronics. Speed enhancement is simply achieved by frequency transposition. The advantages and disadvantages of the AC emulation approach compared to other emulation approaches was illustrated through a systematic analysis of the state of the art. Moreover, this analysis led to an overview of existing demonstrators.

The second part of this thesis contains the practical work: the implementation of a first AC emulation demonstrator dedicated to transient stability analysis. Behavioral models for the three main components of power systems, the generator, the load and the transmission lines, are proposed. The models have been developed considering their microelectronic implementation and classical power system modeling theory. Systematic errors are analyzed and reduced. Finally, the validity of the AC models is confirmed by behavioral simulations. Particularities appearing as a result of the frequency dependence of the signals are discussed.

The behavioral models have been implemented in a standard 0.35μm 3.3V CMOS technology. We identified adequate topologies by the consideration of application-specific requirements. And where necessary, we developed dedicated solutions. The design of an application-specific floating tunable inductance has to be especially emphasized. Within this work, we present the development of this inductance from the system-level analysis to the design issues and transistor-level implementation. Transistor-level simulations confirm the adequacy of all developed microelectronic building blocks for use in power system emulation.

Finally, a first AC emulation demonstrator is presented. A benchmark using a fixed two-machine topology was implemented. The characteristics of the emulated components (i.e. generators and transmission lines) are reprogrammable and short circuits can be emulated at different distances from the generator. The emulated phenomena are shown to be 10′000 times faster than real time, therefore proving the high-speed capabilities of AC emulation.

7.2. Perspectives

Based on the results of this work, future research and developments can go in several directions. A few ideas are briefly outlined in the following.

Extension of the first AC emulation demonstrator

First, analog building blocks for the on-chip implementation of the reduced swing equation solver should be designed. In doing so, calibration utilities should be directly included, in order to develop a dedicated and automated calibration scheme.

Second, instead of using a system consisting of one generator connected to an infinite bus, two generators could be implemented. This means that the system has not anymore a fixed reference. The rotor angles are referred to the average speed and the initialization of the system becomes a main concern. Such system would permit a study about different ways of initialization leading to different operating conditions.

Increasing modularity and number of nodes

Based on the developed models an AC Power System Atom (PSA) as shown in Fig. 7.1 can be developed and the FPPNS-concept can be applied to AC emulation.

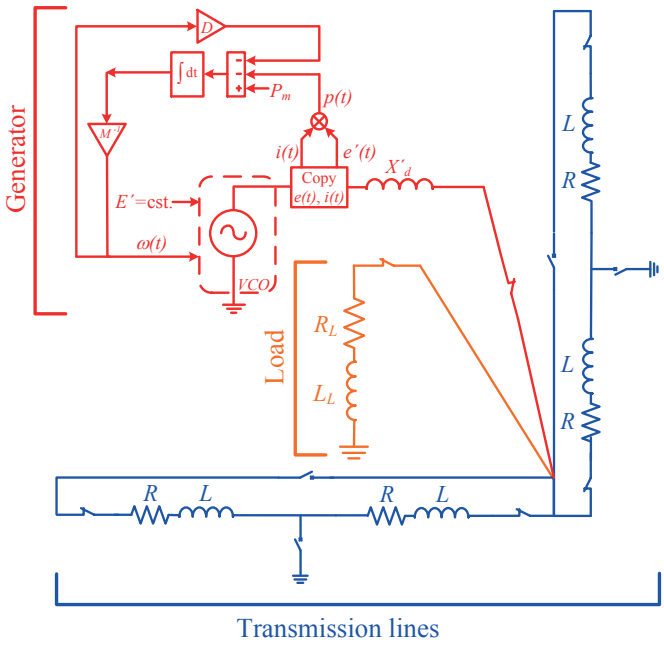


Figure 7.1.: System level of a possible AC emulation PSA

Model extension

In order to benefit from the fact that AC emulation retains the frequency dependence of the signals, the implementation of more advanced models is promising. Extension of the validity of the transient stability simulation can be obtained refining the generator model by implementing, for example, Park's equations [68]. Moreover, including voltage and mechanical power regulators would complete the model. Such advanced model would allow to perform also load flow studies with the AC emulator.

Finally, in terms of phenomena related to AC signals, a three-phase model, including the interactions between the phases (mutual inductances and capacitances), is interesting and opens the door to observing additional phenomena.

Obviously, work on a simulator is an ever-continuing work, as possibilities for improvements, model changes and model additions are unlimited. Fully analog implementations, however, are based on time-consuming developments. Therefore, the scope in which the improvements are made has to be carefully evaluated, in order to systematically achieve enhancement.

A Appendix A. Generator model error computation

This appendix contains the detailed systematic error analysis of the feedback loop of the original generator model with and without damping as they are presented in Section 4.2.2.

A.1. The ideal feedback loop

Ideally, the feedback loop solves the following equation in the time domain:

$$\omega(t) = \frac{1}{M} \int_0^t (P_m - P_e(\tau))\, \mathrm{d}\tau \tag{A.1}$$

Fig. A.1 shows the ideal feedback loop in the Laplace domain. The following transformations from Time domain to the Laplace domain have been applied:

	Time domain	Laplace domain
Mechanical power	$P_m = \text{constant}$	$P_m \cdot \frac{1}{s}$
Electrical power	$P_e(t)$	$P_e(s)$
Integration	$\int \mathrm{d}t$	$\frac{1}{s}$
Angular frequency variation	$\omega(t)$	$Y(s)$

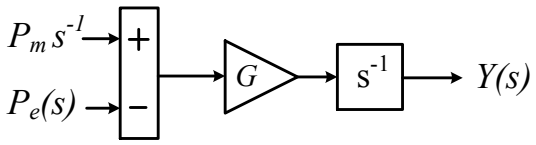


Figure A.1.: Ideal feedback loop in the Laplace domain

The multipliers do not change from one domain to the other. G is defined as

$$G = \frac{1}{M},$$

where M is the inertia factor.

Thus, analytically, the ideal model becomes in the Laplace domain

$$\boxed{Y(s) = G\ \frac{1}{s^2}\ P_m\ -\frac{1}{s}\ G\ P_e(s).} \tag{A.2}$$

A.2. The original AC emulation feedback loop

As explained in Section 4.2.2, we have only direct access to the sinusoidal current and voltage waveforms at the terminal of the generator. Therefore before solving (A.1) the electrical power P_e has to be computed using the instantaneous power $p(t)$. The relationship between P_e and $p(t)$ is defined as

$$P_e = \frac{1}{T}\int_{t-T}^{t} p(\tau)\,\mathrm{d}\tau = \frac{1}{T}\int_{0}^{t}(p(\tau) - p(\tau - T))\,\mathrm{d}\tau. \tag{A.3}$$

T is the period of the current and voltage sine waves propagating on the AC emulated grid. The complete original feedback loop expression combining (A.1) and (A.3) and transformed in the Laplace domain is illustrated in Fig. A.2.

The following transformations have been applied:

	Time domain	Laplace domain
Instantaneous power	$p(t)$	$P(s)$
Delay of T	$p(t-T)$	$\mathrm{e}^{-Ts} \cdot P(s)$

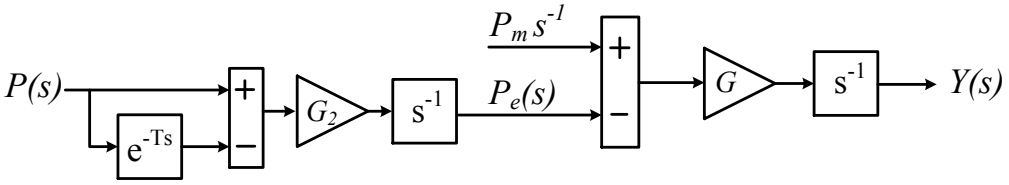


Figure A.2.: Original AC emulation feedback loop in the Laplace domain

The multiplier G_2 equals

$$G_2 = \frac{1}{T}.$$

$P_e(s)$ can therefore be expressed as

$$P_e(s) = (1 - \mathrm{e}^{-Ts})\ G_2\ \frac{1}{s}\ P(s). \tag{A.4}$$

And finally, replacing (A.4) in (A.2) leads to

$$\boxed{Y(s) = G\ P_m\ \frac{1}{s^2}\ - (1 - \mathrm{e}^{-Ts})\ G\ G_2\ P(s)\ \ \frac{1}{s^2}.} \tag{A.5}$$

After transformation back in the time domain, we obtain

$$\omega(t) = G\ P_m\ t - G\ G_2 \int_0^t \tau(p(t-\tau) - p(t-\tau-T))\,\mathrm{d}\tau. \tag{A.6}$$

This equation can be seen as a weighted average of the the function $p(\tau) - p(\tau - T)$ where the weighting is $-\tau$. The back transformation has been established using the transformation of common functions which are listed at the end of this appendix chapter.

A.3. The original AC emulation feedback loop with added damping power

In order to reduce the systematic error of the original model introduced by the P_e- computation block, damping is added to the original model through a negative feedback which multiplies the angular frequency $\omega(t)$ by the damping factor D.

The P_e computation remains unchanged and therefore as expressed in (A.4). Adding the damping to the ideal feedback loop leads to the following equation:

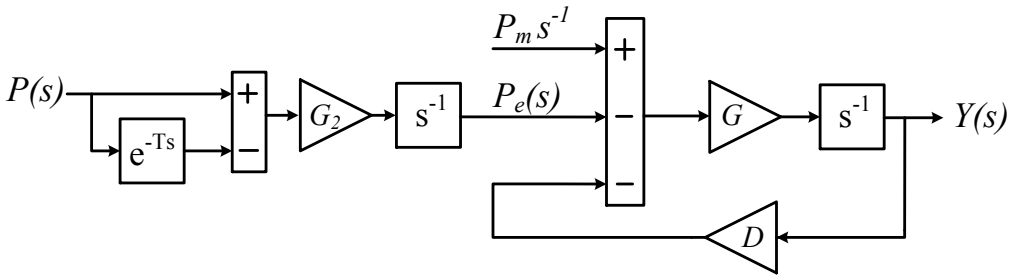


Figure A.3.: Original AC emulation feedback loop with damping in the Laplace domain

$$Y(s) = G\ \frac{P_m\ \frac{1}{s} - P_e(s)}{s + GD}. \tag{A.7}$$

By combining (A.4) and (A.7), we obtain the complete expression for the feedback loop with added damping expressed in the Laplace domain:

$$\boxed{Y(s) = \frac{1}{s}\ \frac{1}{s + GD}\ G\ P_m\ -\ \frac{1}{s}\ \frac{1}{s + GD}\ (1 - \mathrm{e}^{-Ts})\ G\ G_2\ P(s)} \tag{A.8}$$

The transformation back to time domain leads to

$$\omega(t) = \frac{G}{D}\ (1 - \mathrm{e}^{-GDt})\ P_m\ -\ \frac{G_2}{D} \int_0^t (1 - \mathrm{e}^{-GD\tau})\ (p(t-\tau) - p(t-\tau-T))\,\mathrm{d}\tau. \tag{A.9}$$

In this case the electric power is weighted by an exponential function.

The following transformations of common functions have been used for the back transformation:

Laplace domain	Time domain
$\frac{1}{s^2}$	$t \cdot u(t)$ $u(t)$ is the Heaviside step function
$F(s) \cdot G(s)$	$f(t) * g(t) = \int_0^t (f(\tau) g(t-\tau))\,\mathrm{d}\tau$
$\mathrm{e}^{-as} F(s)$	$f(t-a)$
$\frac{a}{s(s+a)}$	$1 - \mathrm{e}^{-at}$

B Appendix B. Labview reference simulator

This abstract gives a quick insight into the LabView reference simulator and its validation. More details can be found in [44]. Most text and all figures are reproduced out of an internal report [69] with kind permission of Laurent Fabre.

Commercial dynamic power system simulators able to carry out temporal analysis of a power system in addition to the load flow are expensive. Moreover, and to the best of the authors knowledge, none of them is accessible in an "open-source" format and none uses the exact implementation of the generator and load models as used in the developed power system emulators. For these two reasons, price and unknown internal implementation, it was decided to realize EPFL's own "open-source" simulator in LabView. An important point in favor of this choice is the ability to compute the load-flow within the same software that runs the temporal analysis.

B.1. A quick insight in the LabView reference simulator

The developed LabView simulator includes 6 different steps illustrated in Fig. B.1.

a: Configuration of load and generator models connected to the nodes

b: Configuration of the power network topology through the admittance matrix

c: Configuration of the scenario through the modification of the admittance matrix before, during and after the fault

d: Computation of the load flow

e: Transient computation

f: Visualization and analysis of the results

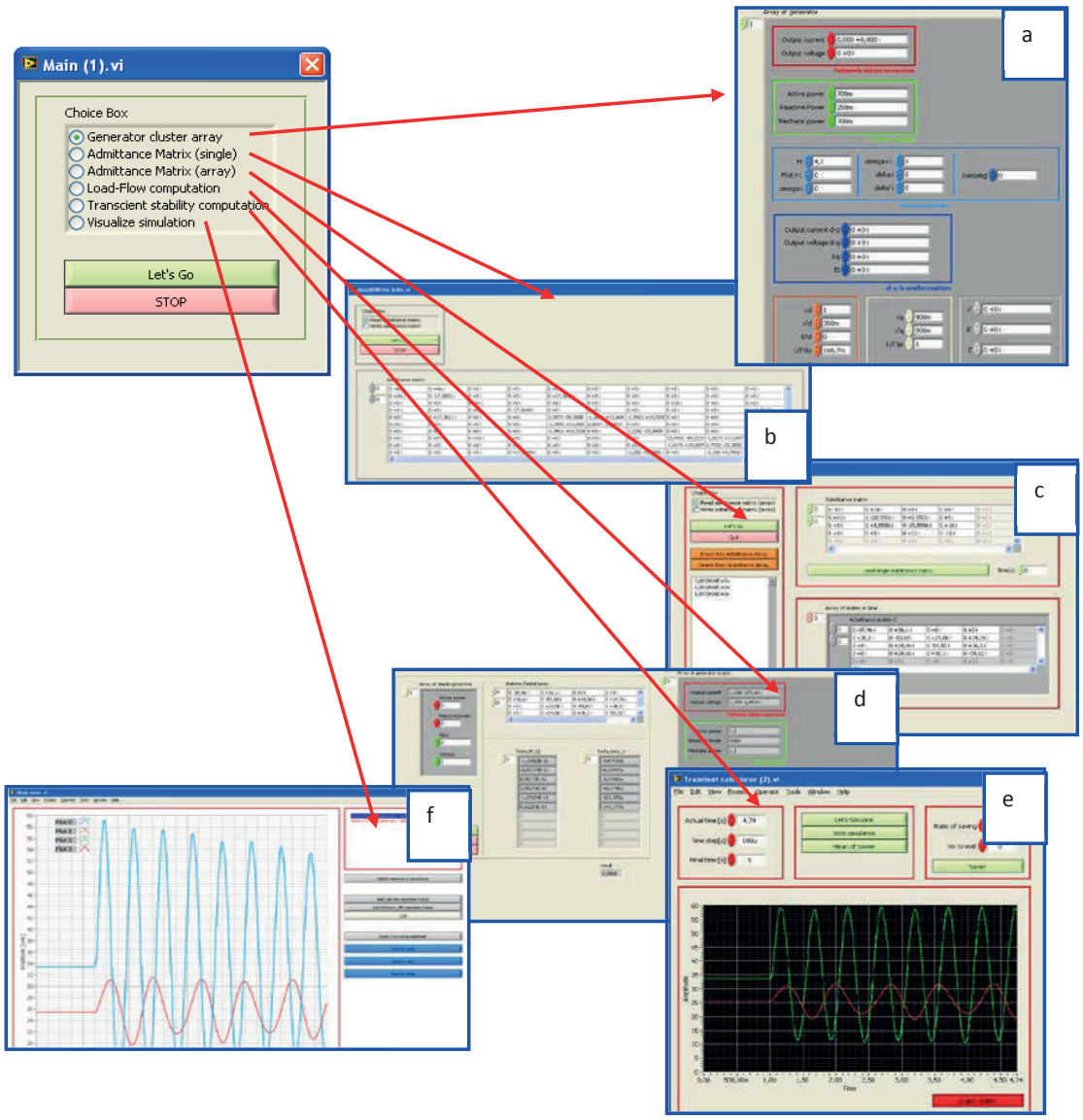


Figure B.1.: Synopsis of the LabView reference simulator

B.2. Validation through reference scenario

The LabView software validation is carried out on a nine-node case study reported in "Power system control and stability" [10]. It represents a transient stability problem on a power system working at 60Hz. It contains one slack generator, three generators and three loads connected as illustrated in Fig. B.2. The Classical Model is used for the generators and the loads are modeled as constant impedances. Tables B.1, B.2 and B.3 show the characteristics of the generators, lines and load respectively.

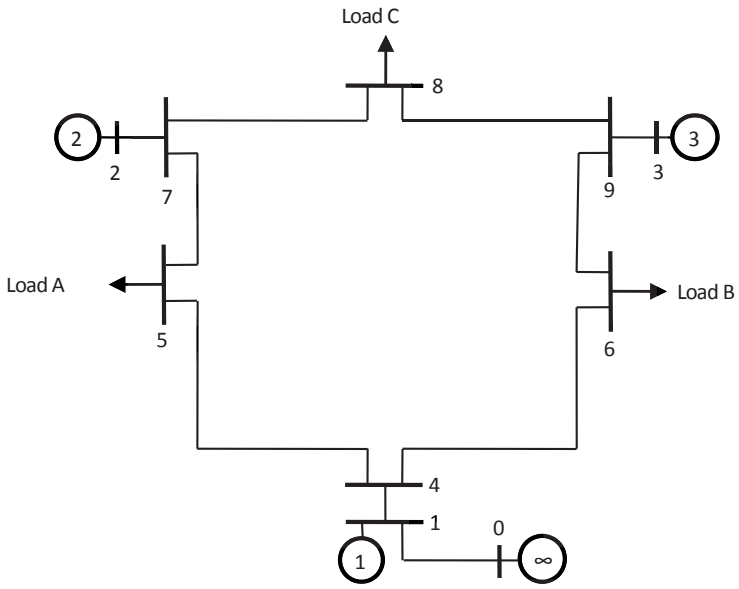


Figure B.2.: Reference topology used for validation

Table B.1.: Generator characteristics

	Gen1	Gen2	Gen3
Power [MVA]	247.5	192.0	128.0
Voltage [kV]	16.5	18.0	13.8
Power factor	1.0	0.85	0.85
Type	hydraulic	gas	gas
Speed [tr/min]	180	3600	3600
x_d [pu]	0.146	0.8958	1.3125
x_d' [pu]	0.0608	0.1198	0.1813
x_q [pu]	0.0969	0.8645	1.2578
x_q' [pu]	0.0969	0.1969	0.25
τ'_{d0} [s]	8.96	6.00	5.89
τ_{q0} [s]	0.00	0.535	0.6
Inertia [MW.s]	2364	640	301

Table B.2.: Load characteristics

	Load A	Load B	Load C
P [MVA]	-125.0	-90.0	-100.0
Q [MVAR]	-50.0	-30.0	-35.0
P [pu]	-1.25	-0.9	-1.00
Q [pu]	-0.5	-0.3	-0.35

Table B.3.: Line characteristics

	Impedance [pu]	Admittance [pu]	Admittance designation
Lines			
4—5	0.0100+j0.0850	1.3652-j11.6041	y_{45}
4—6	0.0170+j 0.0920	1.9422-j10.5107	y_{46}
5—7	0.0320+j 0.1610	1.1876-j5.9751	y_{57}
6—9	0.0390+j 0.1700	1.2820-j5.5882	y_{69}
7—8	0.0085+j 0.0720	1.6171-j13.6980	y_{78}
8—9	0.0119+j 0.1008	1.155-j9.7843	y_{89}
Shunt			
4—5		j0.088	y_{450}
4—6		j0.079	y_{460}
5—7		j0.153	y_{570}
6—9		j0.179	y_{690}
7—8		j0.0745	y_{780}
8—9		j0.1045	y_{890}

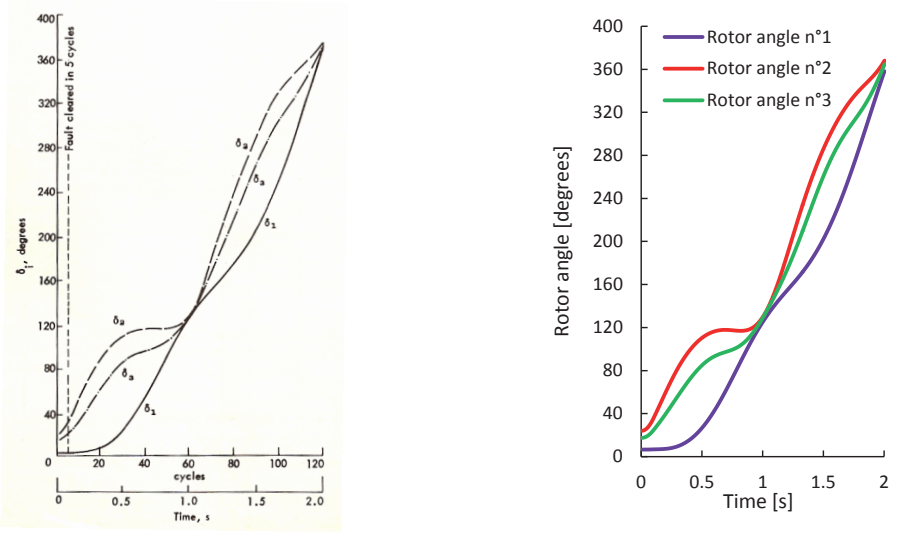
The disturbance initiating the transient phenomenon is a three-phase fault occurring near bus 7 at the end of line 5-7 (refer to Fig. B.2. The fault is cleared after five cycles (83.3ms at 60Hz) and line 5-7 is disconnected afterwards.

Fig. B.3(a) shows the rotor angles for the three generators provided by [10] while Fig. B.3(b) shows the same values but computed with LabView. The slack generator is connected to bus 0. The impedance of line 0-1 is large enough to consider that bus 0 does not provide any active and reactive power. For this reason, node 0 is desynchronizing with the rest of the power system during and after the three-phase fault. Therefore bus 1 is used as the phase reference; the power system is kept stable after the fault as shown in Fig. B.4.

Fig. B.4 shows that the results obtained with LabView are, for this scenario, quantitatively equivalent to those provided by [10], indeed the differences between the angles' values are within 3°. Again, the classical model is used for the generators. These results show that the suitability and accuracy of the LabView software are good enough for our purposes (i.e. validate the emulator). Therefore the LabView implementations of the Classical Model for the generator and the constant impedance model for the load have been validated.

B.3. Validation through comparison with EUROSTAG

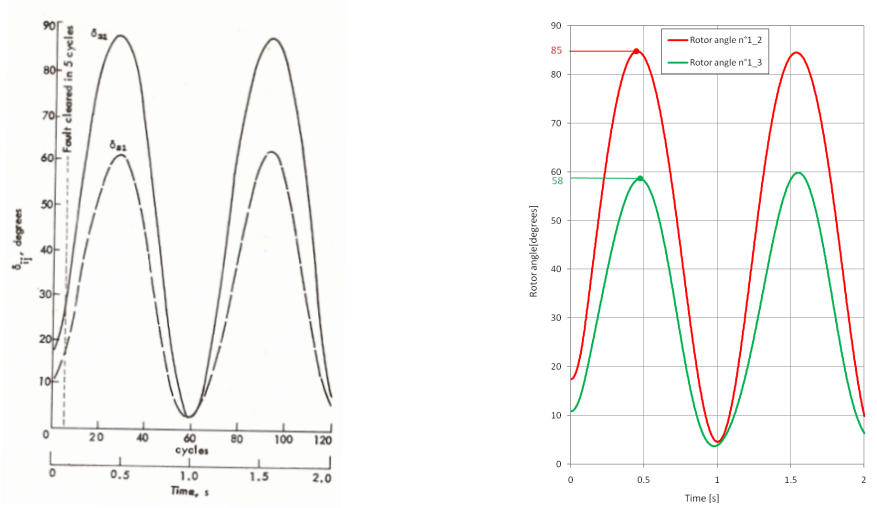
In order to validate the enhanced generator models, we compare results obtained with the LabView simulator to results obtained with EUROSTAG [53]. For this validation we use the scenario shown in Fig. B.5. The chosen topology is the same than the one, which is



(a) Results as printed in [10]

(b) Results as obtained by LabView

Figure B.3.: Plots of rotor angles of the three machines



(a) Results as printed in [10]

(b) Results as obtained by LabView

Figure B.4.: Rotor angles of machines 2 and 3 referred to machine 1

used in Chapter 4 to validate the developed AC emulation models.

The load is modeled as a constant impedance load. The generator model is based on the Park's equations [39]. The scenario is as follows. The disturbance initiating the transients is a three-phase fault occurring in the middle of the line between generator G_2 and the load L. The fault is cleared after three and a half cycles (70ms at 50Hz). The characteristics of the components are shown in Table B.4 and B.5.

B. Labview reference simulator

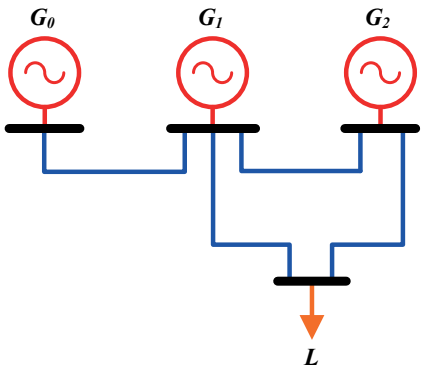


Figure B.5.: Topology used for validation with EUROSTAG

Table B.4.: Generator and load characteristics

	G1	G2	L1
Active power [pu]	0.7	1.1	-1.85
Reactive power [pu]	0.25	0.4	0.4
Inertia [s]	4.2	2.1	-
x_d [pu]	1	1	-
x_d' [pu]	0.35	0.3	-
x_q [pu]	0.9	0.9	-
x_q' [pu]	0.9	0.9	-
τ'_{d0} [s]	6	6	-
τ_{q0} [s]	0	0	-

Table B.5.: Line characteristics

	Line reactance [pu]
Line $G_b - G_1$	0.1
Line $G_1 - G_2$	0.18
Line $L - G_1$	0.2
Line $L - G_2$	0.1

EUROSTAG is a dedicated power system simulator, which uses prediction/correction phases and variable steps of integration. It uses simultaneous methods of simulation with implicit methods of integration [53]. The realized LabView software is based on a partitioned simulation method and uses explicit rather than implicit integration method in order to be coherent with power system emulation, the integration time step is constant. Therefore, the numerical principles behind EUROSTAG and LabView are quite different. While their results are qualitatively comparable, they may not be comparable from a more quantitative point of view.

To compare the results of EUROSTAG and LabView, both programs have been configured with the same topology and used the same generator and load characteristics. The simulation results are depicted in Fig. B.7. The waveforms are qualitatively equivalent and therefore the results provided by the LabView simulator can be validated.

Fig. B.7 shows that the LabView software provides accurate results during the five seconds following the fault. Nevertheless, there is an over-damping in the results provided by the LabView software. This is more clearly seen in Fig B.6, where the differences between the LabView and EUROSTAG results are quantified. The difference clearly increases over time. This is due to fact that EUROSTAG uses a different numerical resolution method than our LabView simulator. Moreover, explicit methods of integration usually over evaluate the generator angle damping [53].

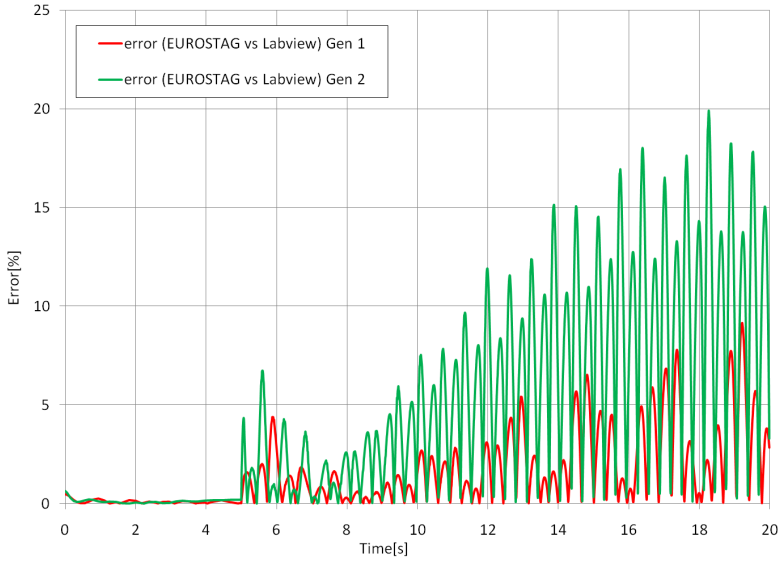
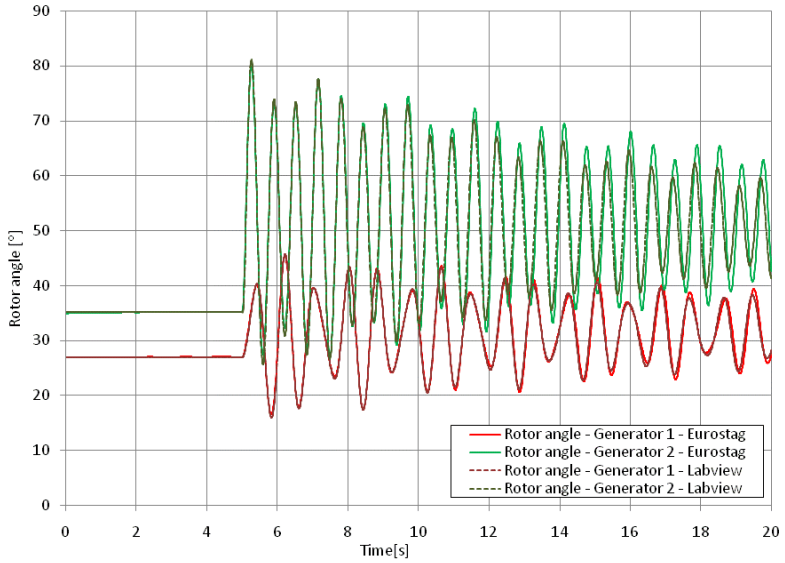
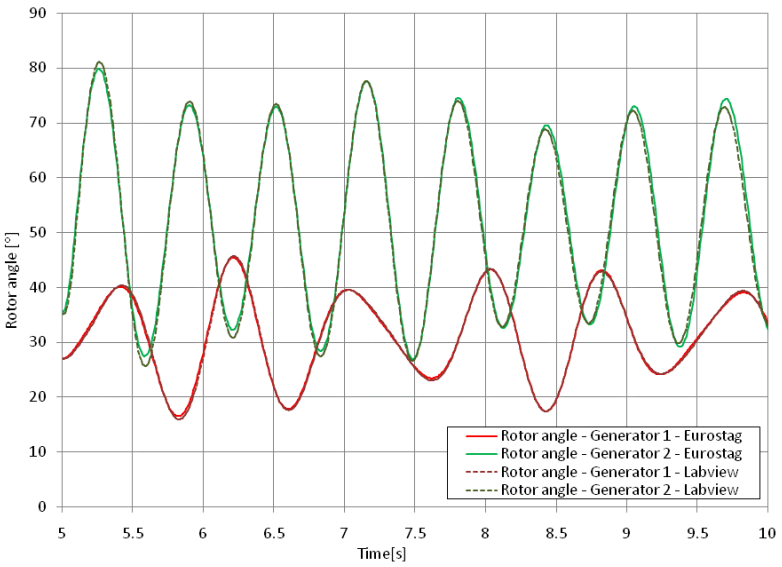


Figure B.6.: Difference between the rotor angles computed with LabView and EUROSTAG



(a) The complete simulation results



(b) A zoom on the first 5 s after the fault

Figure B.7.: Rotor angles for generator 1 and 2 obtained with LabView and EUROSTAG

Bibliography

[1] *IEEE Power Energy Mag., Special Issue: Taking the Measure of the Smart Grid around the World*, Jan. 2011.

[2] "Das Schweizer Stromnetz: Rückgrat der Energieversorgung," swissgrid ag, Jan. 2012.

[3] U.S. Department of Energy, *The Smart Grid: an introduction.* United States of America, Sep. 2011.

[4] U.S. Energy Information Administration, *International Energy Outlook 2006.* United States of America, Jun. 2006.

[5] U.S. Energy Information Administration, *International Energy Outlook 2011.* United States of America, Sep. 2011.

[6] (2012, Sep.) Energy strategy 2050. Swiss Federal Office of Energy. [Online]. Available: http://www.bfe.admin.ch/themen/00526/00527/index.html?lang=en

[7] (2012, Jun.) 10 years of sustainability "made in germany". The Federal Government of Germany. [Online]. Available: http://www.bundesregierung.de/Content/EN/$_$Anlagen/2012-06-01-kurzpapier-n-englisch.pdf?$___$blob=publicationFile$&$v=2

[8] C. Feisst, D. Schlesinger, and W. Frye, *Smart Grid: The Role of Electricity Infrastructure in Reducing Greenhouse Gas Emissions (White Paper).* Cisco Internet Business Solutions Group, Oct. 2008.

[9] C. Duthaler, "Power Transfer Distribution Factors: Analyse der Anwendung im UCTE-Netz," Master's thesis, Eidgenössische Technische Hochschule Zürich (ETHZ), Switzerland, 2007.

[10] P. M. Anderson and A. A. Fouad, *Power System Control and Stability.* Iowa, USA: The Iowa State University Press, 1977.

[11] M. Kayal, L. Fabre, and I. Nagel, "Emulation du réseau électrique: Stabilité dynamique du "smart grid" en temps réel grâce à la microélectronique," *Bulletin, Revue spécialisé et informations des associations electrosuisse et AES*, no. 9, pp. 27–30, 2012.

[12] B. Buggiani, "Parallélisation des calculs de stabilité transitoire des réseaux électriques," Ph.D. dissertation, Ecole Polytechnique Fédérale de Lausanne (EPFL), 1995.

[13] J. Q. Wu, A. Bose, J. A. Huang, A. Valette, and F. Lafrance, "Parallel implementation of power system transient stability analysis," *IEEE Trans. Power Syst.*, vol. 10, no. 3, pp. 1226–1233, 1995.

[14] C. Nwankpa, J. Johnson, P. Nagvajara, T. Chagnon, and P. Vachranukunkiet, "FPGA hardware results for power system computation," in *Proc. PSCE'09*, Seattle, USA, Mar. 15–18, 2011.

[15] J. K. Debnath, W.-K. Fung, A. M. Gole, and S. Filizadeh, "Simulation of large-scale electrical power networks on graphics processing units," in *Proc. EPEC 2011*, Winnipeg, Canada, Oct. 3–5, 2011.

[16] (2012, Oct.) Siemens SIGUARD. [Online]. Available: http://www.siemens.com/siguard

[17] (2012, Oct.) Rtds technologies. [Online]. Available: http://www.rtds.com/

[18] (2012, Oct.) OPAL-RT technologies. [Online]. Available: http://www.opal-rt.com/

[19] R. Fried, R. Cherkaoui, C. Enz, A. Germond, and E. Vittoz, "Approaches for analog VLSI simulation of the tranisient stability of large power networks," *IEEE Trans. Circuits Syst.*, vol. 46, no. 2, pp. 1249–1263, 1999.

[20] A. Oudalov, Y. Maret, I. Nagel, L. Fabre, M. Kayal, and R. Cherkaoui, "Programmable and reconfigurable hardware for real-time power system emulation," European Patent Request EP 2 267 561 A1, Jun. 26, 2009.

[21] A. Oudalov, Y. Maret, I. Nagel, L. Fabre, M. Kayal, and R. Cherkaoui, "Programmable and reconfigurable hardware for real-time power system emulation," U.S. Patent Request 20 100 332 211, Jun. 28, 2010.

[22] G. Cowan, "A VLSI analog computer / math co-processor for a digital computer," Ph.D. dissertation, Columbia University New York, USA, 2005.

[23] A. S. Leger, "Power system security assessment through analog computation," Ph.D. dissertation, Drexel University, 2008.

[24] V. Jalili-Marandi and V. Dinavahi, "SMID-based large-scale transient stability simulation on the graphics processing unit," *IEEE Trans. Power Syst.*, vol. 25, no. 3, pp. 1589–1599, 2010.

[25] U.S.-Canada Power System Outage Task Force, *Final Report on the August 14, 2003*

Blackout in the United States and Canada: Causes and Recommendations. United States of America, Apr. 2004.

[26] K. J. Aström, H. Elmqvist, and S. E. Mattsson, "Evolution of continuous-time modeling and simulation," in *Proc. ESM'98*, Manchester, UK, Jun. 16–19, 1998.

[27] C. P. Steinmetz, "Power control and stability of electric generating stations," *AIEE transactions*, vol. 39, no. 2, pp. 1215–1287, 1920.

[28] P. Kundur, *Power System Stability and Control.* New York: Mc Graw-Hill, Inc., 1994.

[29] P. C. Krause, T. A. Lipo, and D. P. Caroll, "Applications of analog and hybrid computation in electric power system analysis," *Proc. of the IEEE*, vol. 62, no. 7, pp. 994–1009, 1974.

[30] D. P. Atherton, "Control engineering and the analog computer," *IEEE Control Systems Magazine*, vol. 25, no. 1, pp. 63–67, 2005.

[31] H. Doi, M. Goto, T. Kaway, S. Yokokawa, and T. Suzuki, "Advanced power system analogue simulator," *IEEE Trans. Power Syst.*, vol. 5, no. 3, pp. 962–968, 1990.

[32] Y. Tamura, E. Dan, I. Horie, Y. Nakanishi, and S. Yokokawa, "Development of power system simulator for research and education," *IEEE Trans. Power Syst.*, vol. 5, no. 2, pp. 492–498, 1990.

[33] F. Preston, "Vannevar Bush's network analyzer at the Massachusetts Institute of Technology," *IEEE Annals of the History of Computing*, vol. 25, no. 1, pp. 75–78, 2003.

[34] I. Nagel, D. Seetharamdoo, L. Fabre, R. Cherkaoui, and M. Kayal, "Microelectronic emulation for power system computation," in *Proc. PSCC '08*, Glasgow, United Kingdom, Jul. 14–18, 2008.

[35] M. Kayal, R. Cherkaoui, I. Nagel, L. Fabre, F. Emery, and B. Rey, "Toward a power system emulation using analog microelectronics solid state circuits," in *Proc. IEEE Power Tech '07*, Lausanne, Switzerland, Jul. 1–5, 2007, pp. 726–730.

[36] I. Nagel, L. Fabre, F. Emery, B. Rey, R. Cherkaoui, and M. Kayal, "Emulation du réseau électrique à l'aide des circuits électroniques," in *Proc. TAISA '07*, Lyon, France, Oct. 18–19, 2007.

[37] L. Fabre, I. Nagel, R. Cherkaoui, and M. Kayal, "Calculateur analogique faible consommation dédié au calcul transitoire des réseaux électriques," in *Proc. FTFC '09*, Neuchâtel, Switzerland, Jun. 3–5, 2009.

[38] L. Fabre, I. Nagel, R. Cherkaoui, and M. Kayal, "High-speed, mixed-signal emulation for power system dynamic analysis," in *Proc. IEEE Power Tech '09*, Bucharest, Romania, Jun. 1–5, 2009.

[39] L. Fabre, I. Nagel, C. Meinen, R. Cherkaoui, and M. Kayal, "A field programmable power network system (FPPNS) for high-speed transient stability emulation," in *Proc. PSCC '11*, Stockholm, Sweden, Aug. 22–26, 2011.

[40] L. Fabre, I. Nagel, C. Meinen, R. Cherkaoui, and M. Kayal, "A mixed-signal platform dedicated to power system dynamic computation," in *Proc. IEEE ISCAS'11*, Rio de Janeiro, Brasil, May 15–18, 2011, pp. 1860 –1863.

[41] L. Fabre, G. Lanz, T. Kyriakidis, D. Sallin, I. Nagel, R. Cherkaoui, and M. Kayal, "An ultra-high speed emulator dedicated to power system dynamics computation based on a mixed-signal hardware platform," *IEEE Trans. Power Syst.*, submitted for publication.

[42] A. S. Deese and C. O. Nwankpa, "Utilization of FPAA technology for emulation of multiscale power system dynamics," *IEEE Transactions on Smart Grid*, vol. 2, no. 4, pp. 606–614, 2011.

[43] I. Nagel, L. Fabre, M. Pastre, F. Krummenacher, R. Cherkaoui, and M. Kayal, "High-speed power system stability simulation using dedicated microelectronic computation," *IEEE Trans. Power Syst.*, submitted for publication.

[44] L. Fabre, "Mixed-signal emulation for dynamic power system computation (temporary title)," Ph.D. dissertation, Ecole Polytechnique Fédérale de Lausanne, EPFL, 2013.

[45] A. S. Deese, C. O. Nwankpa, J. C. Jiménez, J. Berardino, and J. Hill, "Design of modular field programmable analog array hardware for analysis of large power systems," in *Proc. ISCAS'12*, Seoul, Korea, May 20–23, 2012, pp. 1207–1210.

[46] L. Fabre, G. Lanz, I. Nagel, F. Lo Conte, R. Cherkaoui, and M. Kayal, "An ultra high-speed, mixed-signal emulator for solving power system dynamic equations," in *Proc. IEEE NEWCAS'11,*, Bordeaux, France, Jun. 26–29, 2011, pp. 374 – 377.

[47] J. Machowski, J. W. Bialek, and J. R. Bumby, *Power System Dynamics and Stability.* Chichester, England: John Wiley & Sons, 1997.

[48] G. Andersson, *Modelling and Analysis of Electric Power Systems.* Zürich, Switzerland: Eidgenössische Technische Hochschule Zürich, 2008.

[49] M. Aguet and J.-J. Morf, *Energie électrique.* Lausanne, Switzerland: Presse polytechniques et universitaires romandes, 1987.

[50] M. K. Pal, *Lecture Notes on Power System Stability.* Edison, New Jersey: online, 2007.

[51] I. T. F. on Load Representation for Dynamic Performance, "Load representation for dynamic performance analysis," *IEEE Trans. Power Syst.*, vol. 5, no. 2, pp. 492–498, 1990.

[52] (2012, Sep.) Virtuoso spectre circuit simulator. Cadence Design Systems, Inc. [Online]. Available: http://www.cadence.com/rl/Resources/datasheets/virtuoso_mmsim.pdf#page=4

[53] M. Stubbe, A. Bihain, J. Deuse, and J. Baader, "STAG - a new unified software program for the study of the dynamic behavior of electrical power systems," *IEEE Trans. Power Syst.*, vol. 4, no. 1, pp. 129– 138, 1989.

[54] D. Stefanovic and M. Kayal, *Structured Analog CMOS Design.* Dordrecht, Netherlands: Springer Science+Business Media B.V., 2008.

[55] F. Yuan, *CMOS Active Inductors and Transformers.* New York: Springer Science+Business Media, LLC, 2008.

[56] Y. K. Koutsoyannopoulos and Y. Papananos, "Systematic analysis and modeling of integrated inductors and transformers in RF IC design," *IEEE Trans. Circuits Syst. II*, vol. 47, no. 8, pp. 699–713, 2000.

[57] L.-H. Lu, H.-H. Hsieh, and Y.-T. Liao, "A wide tuning-range CMOS VCO with a differential tunable active inductor," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 9, pp. 3462–3468, 2006.

[58] M. Grozing, A. Pascht, and M. Berroth, "A 2.5V CMOS differential active inductor with tunable L and Q for frequencies up to 5GHz," in *Proc. IEEE RFIC Symposium '01*, Phoenix, USA, May 20–22, 2001, pp. 271–274.

[59] A. Thanachayanont, "A 1.5V high-Q CMOS active inductor for IF/RF wireless applications," in *Proc. IEEE APCCAS '00*, Tianjin, China, Dec. 4–6, 2000, pp. 654–657.

[60] F. Mahmoudi and C. Salama, "8GHz tunable CMOS quadrature generator using differential active inductors," in *Proc. IEEE ISCAS '05*, Kobe, Japan, May23–26, 2005, pp. 2112–2115.

[61] B. Razavi, *Design of Analog CMOS Integrated Circuits.* New York: Mc Graw-Hill, Inc., 2001.

[62] B. Razavi, *Design of Integrated Circuits for Optical Communications.* New York: Mc Graw-Hill, Inc., 2003.

[63] I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "Reconfigurable fully integrated inductance for high-speed transient stability emulation," in *Proc. PSCC'11*, Stockholm, Sweden, Aug. 22–26, 2011.

[64] I. Nagel, L. Fabre, M. Pastre, F. Krummenacher, R. Cherkaoui, and M. Kayal, "Tunable floating active inductor with internal offset reduction," *Electronics Letter*, vol. 48, no. 13, pp. 786–788, 2012.

[65] F. Krummenacher and N. Joehl, "A 4-mhz cmos continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 750–758, 1988.

[66] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. New York: Holt, Rinehard and Winston, Inc., 1987.

[67] J. W. Fattaruso and R. G. Meyer, "Triangle-to-sine wave conversion with mos technology," *IEEE J. Solid-State Circuits*, vol. 20, no. 2, pp. 623–631, 1985.

[68] M. Pavella and P. G. Murty, *Transient stability of power systems*. Chichester, England: John Wiley & Sons, 1994.

[69] L. Fabre, R. Cherkaoui, and M. Kayal, "Generator and load models enhancement," Ecole Polytechnique Fédérale de Lausanne, EPFL, Tech. Rep., Mar. 2009.

[70] I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "High-speed power system stability simulation using analog computation," *International Journal of Microelectronics and Computer Science*, vol. 1, no. 2, pp. 180–187, 2010.

[71] I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "High-speed data processing calculators for power system analysis: Comparison," in *Proc. IEEE NEWCAS '10*, Montréal, Canada, Jun. 20–23, 2010.

[72] I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "High-speed power system stability simulation using analog computation: Systematic error analysis," in *Proc. IEEE MIXDES '10*, Wroclaw, Poland, Jun. 24–26, 2010.

[73] I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "High-speed power system stability simulation using analog computation," in *Proc. IEEE MIXDES '09*, Lodz, Poland, Jun. 25–27, 2009.

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Education and Degrees

2007-2012	**PhD (Dr. ès Sciences) degree** Electronics Laboratory (GR-KA), Prof. M. Kayal Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland
2002-2007	**B.Sc. and M.Sc. degrees in Electrical Engineering** Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland
2004-2005	**Exchange year** Università degli Studi di Siena, Siena, Italy

Postgraduate Courses

MEAD-EPFL
- Advanced Analog IC Design
- Low-Power, Low-Voltage Analog IC Design
- Low-Noise, Low-Offset Analog IC Design

Professional Experience

2007-2012	**Research and teaching assistant** EPFL, Lausanne, Switzerland
2004	**Industrial placement in the Electronics Laboratory** Metrohm AG, Herisau, Switzerland
2002	**Industrial placement in the Coaxial Cable Design Group** Huber & Suhner AG, Herisau, Switzerland

List of Publications

Journal Papers

2012 L. Fabre, G. Lanz, T. Kyriakidis, D. Sallin, I. Nagel, R. Cherkaoui, and M. Kayal, "An ultra-high speed emulator dedicated to power system dynamics computation based on a mixed-signal hardware platform," *IEEE Trans. Power Syst.*, submitted for publication

I. Nagel, L. Fabre, M. Pastre, F. Krummenacher, R. Cherkaoui, and M. Kayal, "High-speed power system stability simulation using dedicated microelectronic computation," *IEEE Trans. Power Syst.*, submitted for publication

M. Kayal, L. Fabre, and I. Nagel, "Emulation du réseau électrique: Stabilité dynamique du "smart grid" en temps réel grâce à la microélectronique," *Bulletin, Revue spécialisé et informations des associations electrosuisse et AES*, no. 9, pp. 27–30, 2012

I. Nagel, L. Fabre, M. Pastre, F. Krummenacher, R. Cherkaoui, and M. Kayal, "Tunable floating active inductor with internal offset reduction," *Electronics Letter*, vol. 48, no. 13, pp. 786–788, 2012

2010 I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "High-speed power system stability simulation using analog computation," *International Journal of Microelectronics and Computer Science*, vol. 1, no. 2, pp. 180–187, 2010

Conference Papers

2011 L. Fabre, I. Nagel, C. Meinen, R. Cherkaoui, and M. Kayal, "A field programmable power network system (FPPNS) for high-speed transient stability emulation," in *Proc. PSCC '11*, Stockholm, Sweden, Aug. 22–26, 2011

I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "Reconfigurable fully integrated inductance for high-speed transient stability emulation," in *Proc. PSCC'11*, Stockholm, Sweden, Aug. 22–26, 2011

L. Fabre, I. Nagel, C. Meinen, R. Cherkaoui, and M. Kayal, "A mixed-signal platform dedicated to power system dynamic computation," in *Proc. IEEE ISCAS'11*, Rio de Janeiro, Brasil, May 15–18, 2011, pp. 1860 –1863

L. Fabre, G. Lanz, I. Nagel, F. Lo Conte, R. Cherkaoui, and M. Kayal, "An ultra high-speed, mixed-signal emulator for solving power system dynamic equations," in *Proc. IEEE NEWCAS'11,*, Bordeaux, France, Jun. 26–29, 2011, pp. 374 – 377

2010 I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "High-speed data processing calculators for power system analysis: Comparison," in *Proc. IEEE NEWCAS '10*, Montréal, Canada, Jun. 20–23, 2010

I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "High-speed power system stability simulation using analog computation: Systematic error analysis," in *Proc. IEEE MIXDES '10*, Wroclaw, Poland, Jun. 24–26, 2010

2009 L. Fabre, I. Nagel, R. Cherkaoui, and M. Kayal, "High-speed, mixed-signal emulation for power system dynamic analysis," in *Proc. IEEE Power Tech '09*, Bucharest, Romania, Jun. 1–5, 2009

L. Fabre, I. Nagel, R. Cherkaoui, and M. Kayal, "Calculateur analogique faible consommation dédié au calcul transitoire des réseaux électriques," in *Proc. FTFC '09*, Neuchâtel, Switzerland, Jun. 3–5, 2009

I. Nagel, L. Fabre, R. Cherkaoui, and M. Kayal, "High-speed power system stability simulation using analog computation," in *Proc. IEEE MIXDES '09*, Lodz, Poland, Jun. 25–27, 2009

2008 I. Nagel, D. Seetharamdoo, L. Fabre, R. Cherkaoui, and M. Kayal, "Microelectronic emulation for power system computation," in *Proc. PSCC '08*, Glasgow, United Kingdom, Jul. 14–18, 2008

2007 M. Kayal, R. Cherkaoui, I. Nagel, L. Fabre, F. Emery, and B. Rey, "Toward a power system emulation using analog microelectronics solid state circuits," in *Proc. IEEE Power Tech '07*, Lausanne, Switzerland, Jul. 1–5, 2007, pp. 726–730

I. Nagel, L. Fabre, F. Emery, B. Rey, R. Cherkaoui, and M. Kayal, "Emulation du réseau électrique à l'aide des circuits électroniques," in *Proc. TAISA '07*, Lyon, France, Oct. 18–19, 2007

Patents

A. Oudalov, Y. Maret, I. Nagel, L. Fabre, M. Kayal, and R. Cherkaoui, "Programmable and reconfigurable hardware for real-time power system emulation," European Patent Request EP 2 267 561 A1, Jun. 26, 2009

A. Oudalov, Y. Maret, I. Nagel, L. Fabre, M. Kayal, and R. Cherkaoui, "Programmable and reconfigurable hardware for real-time power system emulation," U.S. Patent Request 20 100 332 211, Jun. 28, 2010