Editorial

I. Introduction

IN RECENT years, we have observed spectacular advancements in the area of nano-circuits and systems at several levels, from the fabrication material and device levels to the system and application levels.

New emerging materials provide us with a wealth of new devices such as (silicon) nanowires, graphene, and carbon nanotubes fabricated in various technologies. Applications of these devices are vast and include, but are not limited to, new computing and memory structures, super-capacitors, as well as nanobio-sensors based on the molecular combination of molecular probes to electronic devices.

At the system level, we see the useful and prolific combination of components such as sensors and data acquisition systems, energy harvesting, and storage units, as well as signal conditioning, processing, and communication subsystems designed in heterogeneous technologies. The design and realization of such systems require research in related areas, from circuits to architectures and to reliable computing.

At the application level, we witness the emergence of prototypes and products for personalized medicine (e.g., chemical and biological analysis, medical stimulators, labs-on-chips), for environmental control (e.g., sensor networks, smart buildings, smart city, smart grid) and for the consumer market (e.g., next generation cell phone systems, image and signal sensors/processors) and many others.

All these systems are characterized by the growing heterogeneity of components, ranging from materials and devices to circuits and subsystems. Analysis and design of such heterogeneous circuits and systems is a very important problem and to date current solutions have been just scratching the surface. As it can be expected, design and manufacturing issues will become more prominent in the coming years with further device downscaling and hybridization of technologies.

The IEEE Circuits and Systems Society Forum on Emerging and Selected Topics (CAS-FEST)—held in Seoul, Korea, in May 2012 in conjunction with ISCAS, had the objective to provide the audience with a cross-sectional view of the aforementioned areas and challenges. The thematic focus of the CAS-FEST 2012 was Heterogeneous Nano Circuits and Systems.

This special issue of the Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) has the purpose to collect some selected contributions to the workshop as well as other works in these domain, all subject to peer review. In particular, this issue focuses on two specific topics: biomedical circuits and systems, and 3-D integrated circuits and systems. This choice is motivated by a synergy of the spontaneous contributions in these areas as well as by the importance of these fields. We will review these two areas at large before briefly summarizing the contributions.

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II. Biomedical Circuits and Systems

Future health management systems will require an increasingly large presence of automation, information extraction and elaboration, as well as control of the medical procedures. In essence, we can envision three major areas that require innovation:

- real-time sensing and data acquisition of bio-chemical compound concentrations;
- information networking through a specialized physical layer;
- data elaboration, retrieval, and classification.

Sensing is a discipline that traditionally has been developed by communities related to fundamental sciences (e.g., physics, chemistry, and biology) [9], [10]. Despite the large number of sensors available, their effective use is limited by size, power consumption, and lack of effective integration with electronic and information systems. In other words, sensing is still based on discrete components, much like a transistor radio was assembled 50 years ago.

The integration of sensing with electronics, and thus the merging of sensing and electronic design, is key to achieving miniaturized, low-power, low-noise data acquisition chains with detection limits in regions of interest for clinical studies.

The challenges of biomedical electronic systems are related to both data acquisition and communication. Indeed, sensors in the body need to communicate to external devices. Power delivery means can obviate the need of implanted batteries, which always present some risk factor. Sensors on the body communicate through *body-area networks* (BAN), a new technology with several challenges, including energy-efficiency, bandwidth, and security [11]. Bio-compatibility and the selection of materials and related technologies are also important topics of research.

Information systems for biomedical applications have been developed, but they are typically used *offline*. The need of fast responses and their secure interaction with electronics on the body and/or in the body is still an area of research. Nevertheless, the combination of networked databases with online data acquisition chains opens the door to better therapy as well as to promoting the autonomy of the patient and convalescent.

Bio-sensors are used in the medical practice for *online* and *offline* diagnosis. Few systems for online monitoring are available on the market. Monitoring metabolism is a complex and expensive process, mainly because of the unavailability of accurate, fast, and affordable sensing devices that can detect and quantify multiple compounds in parallel and several times a day. To date, medical systems available on the market for human telemetry are using wearable devices (accelerometers, heartbeat monitoring system, etc.) but they do not measure molecular metabolites. The only available real-time, implantable/wearable systems for metabolic control are limited to glucose monitoring in diabetic patients. For other pathologies, molecules are monitored in daily hospital practice by means of blood sampling and offline analysis. This requires large and expensive laboratory equipment. Offline bio-measurements are achieved by

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a wide array of techniques. Still there is a strong potential for improvement, by exploring various sensing mechanisms, using advanced electronic devices and materials, and tightly coupling electronic sensing to data acquisition chains. The Swiss Nano-Tera.ch [1], [2] program has been addressing several of these challenges.

In the bio-circuit and system domain, heterogeneity is present through the use of different materials and technologies. In particular, papers in this issue will feature sensors using hybrid materials, the combination of complementary metal–oxide–semiconductor (CMOS) and flexible electronics, as well as the use of optical technologies to power electronic circuits.

III. Three-Dimensional Integration

Energy efficiency is the most significant challenge for continued integration of systems according to Moore's law, the principal driver behind the semiconductor industry: from supercomputers and large-scale server clouds that face the challenges of cooling power-hungry circuits, all the way to mobile devices that are limited by battery life and form factor.

Three-dimensional integrated circuits (3-D ICs) consist of multiple layers of (electronic) circuits integrated vertically using a variety of integration technologies. This is in sharp contrast to traditional ICs with transistors only on the bottom-most layer. 3-D ICs can enable energy-efficient systems with reduced form factors (or increased integration density), addressing the needs of both high-performance clouds and low-power mobile applications [8]. Recent demonstrations of memory-on-logic [3], [4], memory-on-memory [5], and Xilinx FPGA components integrated on an interposer show promising improvements in energy-efficiency, area, and integration options.

3-D integration also paves a promising path toward heterogeneous integration using a variety of materials such as III-V semiconductors and carbon nanotubes [6], [7].

3-D integration technologies can be broadly classified into two categories.

1) Parallel 3-D integration, where ICs are fabricated separately and integrated afterwards. Through-silicon-vias (TSVs) are generally used for such 3-D integration.
2) Sequential or monolithic 3-D integration where circuits are fabricated layer-by-layer on the same wafer. Unlike parallel 3-D, monolithic 3-D ICs can use conventional vias to connect circuits on different layers. This results in significantly improved via densities.

It is challenging to achieve monolithic 3-D integration using silicon CMOS due to the thermal budget constraints during circuit fabrication. Hence, novel monolithic 3-D integration techniques are essential. This special issue highlights one such technique for silicon CMOS. New materials such as carbon nanotubes create new opportunities for high effective monolithic 3-D integration [7].

3-D ICs face several design challenges. Removal of the heat dissipated on the upper layers is a major problem especially for 3-D ICs with logic-on-logic. Though TSVs can greatly improve the vertical heat conduction, effective lateral thermal conduits are required to obtain good lateral heat conduction in 3-D ICs. For silicon-based monolithic 3-D ICs with silicon substrate thinner than 1 $\mu\mathrm{m}$, lateral heat conduction can be a very significant challenge due to the low thermal resistance path through the silicon substrate. Other significant 3-D IC design challenges include proper system-level partitioning, floorplanning and physical design, distribution of noise-free power supply to circuits on various layers, and ensuring high manufacturing yield, test quality, and reliability.

Heterogeneity within 3-D Integration is intrinsically present due to the variety of materials and processing steps used, as shown by the papers in this special issue.

IV. Contributions to This Issue

This special issue includes seven excellent contributions to bio-circuits and systems and 3-D integration, thus demonstrating the importance of hybridization of fabrication and design technologies, as stressed at the CAS-FEST Symposium, Seoul, Korea. The contributions are summarized next.

A. Biomedical Circuits and Systems

Boero *et al.* presents "A Self-Contained System with CNTs-Based Biosensors for Cell Culture Monitoring." The study of cell cultures, including stem cells, is achieved today mainly by manually sampling the culture and testing the concentration of quantities of interest. Most often cultures are kept in incubators. This new system comprises a peristaltic pump, a sensor array, a data acquisition, and transmission chain that can be placed next to the culture and operate autonomously. The sensors measure glucose and lactate concentrations using a new concept of nanostructured probes with *carbon nanotubes* (CNTs) functionalized by *oxidases*. The readout is achieved wirelessly via bluetooth, and thus can be done while keeping the culture undisturbed within an incubator. The sensor properties compare favorably with the state of the art in several metrics. Moreover, the sensors can be functionalized to sense other chemicals of interest.

Printed electronics provides us with an interesting technology for biomedical circuits and systems. Xie *et al.* in "Heterogeneous Integration of Bio-Sensing System-on-Chip and Printed Electronics" show a prototype of a wearable bio-sensing node. A customized mixed-signal system-on-chip (SoC) with the size of $1.5 \times 3.0\ \mathrm{mm}^2$ is utilized to amplify, digitize, buffer, and transmit the sensed bio-signals, while inkjet printing technology is employed to print silver ink nano-particles on a flexible substrate to realize electrodes and interconnections. A case-study system is designed and optimized for electrocardiogram recording applications. The total size of the implemented bio-sensing node is $4.5 \times 2.5\ \mathrm{cm}^2$, which is comparable with a commercial electrode. This inkjet printed heterogeneous integration approach offers a promising solution for the next-generation cost-effective personalized wearable healthcare monitoring devices.

Sarioglu *et al.* in "An Optically Powered CMOS Receiver System for Intravascular Magnetic Resonance Applications" propose a new low-power optically powered receiver system designed in 0.18 μm triple-well UMC CMOS technology. Optical transmission is used for power delivery and signal transmission. The system can be powered optically, either continuously by a set of on-chip CMOS photodiodes or intermittently by a novel optical power supply unit. Furthermore, they show that the front-end of the receiver can function properly by using only a single on-chip CMOS photodiode. The proposed system can be utilized in a variety of electrically isolated low-power micro-scale applications e.g., implantable devices, wireless sensor, and smart-dust applications, particularly as an intravascular receiver in 1.5 T *magnetic resonance imaging* (MRI) environment.

B. 3-Dimensional Integration

A major challenge in 3-D integration is powering the system, and two papers address this issue within 3-D stacks using TSV technology. Recall that TSVs are manufactured in different ways and at different times of the manufacturing process: this is referred to as *via-first, via-middle*, and *via-last*. Such approaches have each advantages and disadvantages. Satheesh and Salman in "Power Distribution in TSV-Based 3-D Processor-Memory Stacks" show that the area overhead of a power distribution network with via-first TSVs is approximately 9% as compared to less than 2% in via-middle and via-last technologies. Despite this drawback, a via-first based power network is typically overdamped and the issue of resonance is alleviated. A via-last based power network, however, exhibits a relatively low damping factor and the peak noise is highly sensitive to the number of TSVs and decoupling capacitance.

Another related power-distribution challenge in complex ICs is discussed in the paper "Distributed On-Chip Power Delivery" by Kose and Friedman. Future ICs are expected to contain several distributed voltage regulators to achieve energy efficiency. Such a design philosophy requires new techniques to determine the correct locations of on-chip power supplies and decoupling capacitors. This paper presents a methodology to address this challenge.

A different avenue of fabricating 3-D circuits is by monolithic integration. Batude *et al.* present "3-D Sequential Integration: A Key Enabling Technology for Heterogeneous Co-Integration of New Function with CMOS." As discussed earlier, sequential 3-D integration of silicon CMOS ICs suffer from fabrication temperature constraints (less than 650 °C). Unfortunately, conventional silicon MOSFET fabrication does not satisfy this constraint. This paper presents a technique which achieves the temperature budget: a low-temperature process for fabricating silicon MOSFETs (both p- and n-types) on upper layers of 3-D ICs with little performance impact. This is a major result, and can enable future generations of exciting 3-D IC designs: interesting *field programmable gate array* (FPGA) architectures, co-integration of *nanoelectromechanical* (NEM) resonators and CMOS image sensors, or even vertical CMOS library cells.

MOS technologies enable the embedding of readout, analog-to-digital conversion, control, processing and communication circuitry along with high-quality photo-sensors on one chip. Suarez *et al.* in their paper "CMOS-3-D Smart Imager Architectures for Feature Detection" propose a novel multi-layered smart image sensor architecture for feature extraction. This architecture is intended for 3-D IC technologies consisting of two layers (tiers) plus memory. The top tier includes sensing and processing circuitry aimed to perform Gaussian filtering and generate Gaussian pyramids in fully concurrent way. The circuitry in this tier operates in mixed-signal domain. This tier can be further split into two for improved resolution: one containing the sensors and another containing a capacitor per sensor plus the mixed-signal processing circuitry. Regarding the bottom tier, it embeds digital circuitry entitled for the calculation of Harris, Hessian and *difference of Gaussians* (DoG) detectors. The overall system can hence be configured by the user to detect interest points by using the algorithm out of these three better suited to practical applications. The Gaussian pyramid is implemented with a *switched-capacitor* (SC) network. The novelty of the proposed approach relies on the way the circuit structures are arranged into the architecture.

V. Conclusion

We hope that the readers will enjoy this special issue and that the contributions presented here will stimulate their interests in the forthcoming technologies for circuits and systems.

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Prof. Mitra's honors include the Presidential Early Career Award for Scientists and Engineers from the White House, the highest U.S. honor for early-career outstanding scientists and engineers, Terman Fellowship, IEEE CAS/CEDA Pederson Award for the best paper published in the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, and the Intel Achievement Award, Intel's highest corporate honor. He and his students presented award-winning papers at several major conferences: IEEE/ACM Design Automation Conference, IEEE International Test Conference, IEEE VLSI Test Symposium, and the Symposium on VLSI Technology. At Stanford University, he was honored several times by graduating seniors "for being important to them during their time at Stanford." He has served on numerous conference committees and journal editorial boards. Recently, he served on the DARPA's Information Science and Technology Board as an invited member.

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