Vertically-stacked Silicon Nanowire Transistors with Controllable Polarity: a Robustness Study

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***Abstract*—Vertically-stacked *Silicon NanoWire FETs* (SiNWFETs) with gate-all-around control are the natural and most advanced extension of FinFETs. At advanced technology nodes, due to Schottky contacts at channel interfaces, devices show an ambipolar behavior, i.e., the device exhibits *n*- and *p*-type characteristics simultaneously. This property, when controlled by an independent *Double-Gate* (DG) structure, can be exploited for logic computation, as it provides intrinsic XOR operation. Electrostatic doping of the transistor suppresses the need for dopant implantation at the source and drain regions, which potentially leads to a larger process variations immunity of the devices. In this paper, we propose a novel method based on *Technology Computer-Aided Design* (TCAD) simulations, enabling the prediction of emerging devices variability. This method is used within our DG-SiNWFET framework and shows that devices, whose polarity is controlled electrostatically, present better immunity to variations for some of their parameters, such as the *off-current* with 16× less standard deviation.**

Keywords—Nanowires, Ambipolarity, Controllable polarity, Arithmetic gates, XOR, Process variations, TCAD, Variability.

I. INTRODUCTION

Substantial downscaling of the feature size in current CMOS technology has confronted digital designers with serious challenges including the variations in *on*/*off* current ratio, leakage current, and threshold voltage. To address these problems, emerging nanodevices, e.g., *Fin-Shaped FETs* (FinFETs) [1] or *Silicon NanoWire FETs* (SiNWFETs) [2,3], have been introduced by the research community. These devices keep on pursuing Moore's Law by improving channel electrostatic controllability, thereby reducing short-channel effects and *off*-state current. In addition to the improvements in conventional device performances, recent developments introduced devices with enhanced capabilities [4, 5]. In particular, transistors showing the ability of in-field reconfiguration has been recently demonstrated using vertically-stacked *Double-Gate* SiNWFETs [7]. These devices represent a natural evolution of FinFET structure and can be dynamically configured between *n*- and *p*-type (Fig. 1) through an additional terminal, called the *Polarity Gate* (PG). The unique feature of these devices of being polarized electrostatically is of high interest for logic design. They were first employed to build a reconfigurable logic cell [6], and later used to define a static XOR-intensive logic family [5] with improved compactness compared to standard CMOS transistors.

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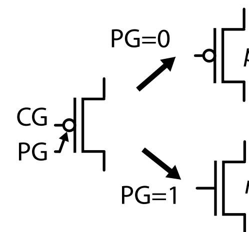

Fig. 1. Polarity control in DG-SiNWFETs [5].

At advanced technology nodes, variability and fabrication defects are expected to significantly affect the reliability of complex systems [8,9]. Indeed, the amount of physical controls, during the fabrication process of nanometer transistors, cannot be precisely determined because of technology fluctuations. Furthermore, due to the novel device geometries, a number of new variation sources may arise during the fabrication. Therefore, fabrication parameters can be very different from their nominal values. On the other hand, novel devices rely on the use of unconventional switching mechanisms with regard to conventional doped source/drain transistors, such as Schottky barrier injection at channel interfaces. These new mechanisms allow technologists to build devices that are less relying on statistical process steps and are therefore prone to exhibit the desired robustness. Hence, giving an *a-priori* conclusion on the variability of advanced technologies is a difficult task and novel estimation methodologies are required.

In this paper, we present the opportunities offered by the polarity-controllable nanowire transistor for compact arithmetic circuit design, such as XOR and *Full-Adder* (FA) gates, in light of its robustness capabilities. In order to study the behavior of an emerging technology in presence of process variations, we introduce a new methodology that allows us to study its reliability even before its fabrication (i) to give some insights to the technologist and (ii) to compare different emerging devices in terms of reliability and early determine the most robust one. Using this methodology, we show that the proposed DG-SiNWFETs that exhibit controllable-polarity are more robust under certain circumstances than their doped source/drain counterparts with, for example, 16× less variability impact of the physical geometries on the *off-current*.

The remainder of the paper is organized as follows. Section II introduces the vertically-stacked silicon nanowire transistor technology and comments on the performance of measured devices. Then, Section III sketches the circuit level opportunities in terms of arithmetic oriented logic gates. Section IV presents a novel methodology for studying the variability of emerging devices and applies it onto the proposed DG-SiNWFETs. Finally, some dis-

cussions and conclusions are respectively drawn in Sections V and VI.

II. VERTICALLY-STACKED SILICON NANOWIRE TRANSISTORS TECHNOLOGY

From 22nm technology node and beyond, planar CMOS transistors have been successfully replaced by novel structures enabling a better electrostatic control on the channel, such as tri-gate FinFET transistors [1]. Following the trend to one-dimensional (1-D) structures, *vertically-stacked Silicon NanoWire Field Effect Transistors* (SiNWFETs) are considered a very promising nanodevice technology [10]. Indeed, by splitting the 2-D thin film channel in a collection of 1-D structures and using a *Gate-All-Around* (GAA) structure, the electrostatic control of the channel is improved. This leads to a higher *Ion/Ioff* ratio and reduced leakage current [3].

At advanced technology nodes (45nm node and below), ambipolar conduction, i.e., simultaneous conduction of *n*- and *p*-type carriers, is observable in several materials, including silicon [11], carbon nanotube [12] and graphene [13]. This phenomenon comes from the trend towards the use of intrinsic transistor channels and Schottky contacts at the source and drain interfaces. While technologists target to suppress the ambipolar behavior of the devices through additional process steps, new design methodologies [6,5] show that its control is of high interest to build devices with a programmable polarity.

By constructing independent double-gate structures, the carriers involved in the device conduction can be electrostatically selected. Hence, the device polarity become programmable on-line to obtain either *n*- or *p*-type behavior. Transistors with controllable polarity have been experimentally fabricated in several novel technologies, such as carbon nanotubes [4], graphene [14] and *Silicon NanoWires* (SiNWs) [15,16].

In this paper, we will refer to a top-down fabricated, vertically-stacked SiNW FET, featuring two *Gate-All-Around* (GAA) electrodes (Fig. 2) [7].

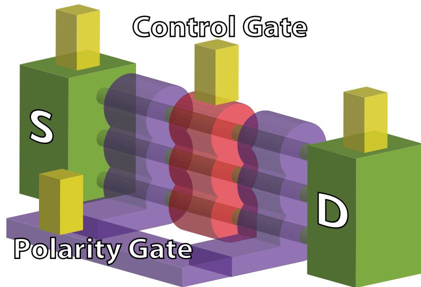

Fig. 2. 3D sketch of the SiNWFET featuring 2 independent gates.

In this device, one gate electrode, the *Control Gate* (CG) acts conventionally by turning *on* and *off* the device. The other electrode, the *Polarity Gate* (PG), acts on the side regions of the device, in proximity of the *Source/Drain* (S/D) Schottky junctions, switching the device polarity dynamically between *n*- and *p*-type (Fig. 3). The applied voltage range is comparable to the voltage range applied to the CG. The input and output voltage levels are compatible, resulting in directly-cascadable logic gates.

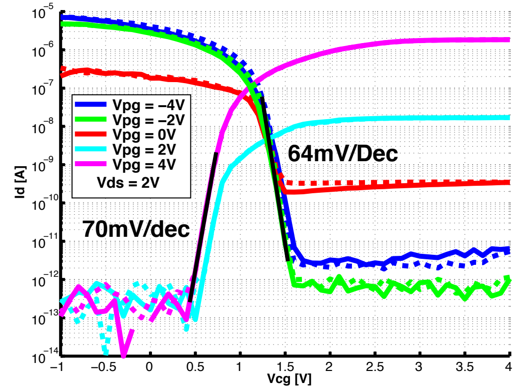

Fig. 3. I_{DS}-V_{CG} logarithmic plot of a measured device for serveral V_{PG} voltages. Curves extracted at V_{DS}=2V [7].

A. Logic Operations

The in-field reconfigurability of the device is appealing for compact logic function realization. Indeed, SiNWFETs are logic biconditional on their two-gate polarities, and intrinsically embed the XOR characteristic. Fig. 4 presents a pseudo-logic XOR gate. The device in the *pull-down* network is polarized by means of the PG. In the case of the *n*-type polarization, the characteristic of a pseudo-logic inverter is obtained (green). In the *p*-type polarization, a buffer is obtained (blue). As shown in the inset truth table, overall an XOR function can be implemented by a single transistor. In the next section, we will show how this novel opportunity can be exploited at the logic gate level.

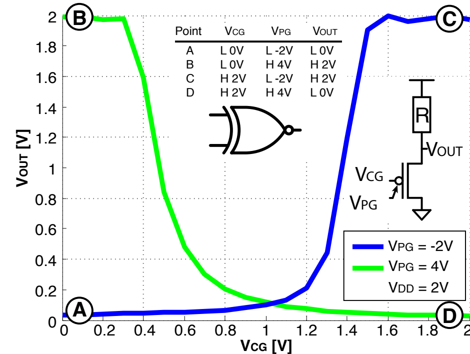

Fig. 4. Pseudo-logic XOR characteristic obtained using a single SiNWFET with controllable polarity [17].

III. CIRCUIT OPPORTUNITIES

Thanks to their improved expressive power, DG-SiNWFETs intrinsically embed the XOR logical connective, therefore enabling compact realizations for XOR/XNOR-dominated circuits. In this section, we will present the circuit realization for both standard and arithmetic logic gates.

A. AND/OR-based Logic Cells

As highlighted in the previous section, DG-SiNWFETs can be reconfigured from *n*- to *p*-type by means of a fixed voltage bias on the polarity gate terminal. Hence, DG-SiNWFETs can implement combinational and sequential function in an effective way. Fig. 5-a shows the polarization to achieve a NAND gate, while Fig. 5-b

shows a NOR gate. The implementation of negative unate functions [18] is kept in a very conventional style. Note that all the transistors are built with the same technological options, i.e., with no segregation between *n*- and *p*-types, therefore increasing the structural regularity and the expected yield of the circuits.

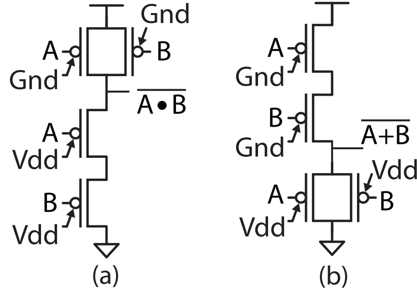

Fig. 5. NAND-2 (a) and NOR-2 (b) gates.

B. Arithmetic Cells

In addition to the realization of standard negative unate logic functions, the introduced technology is of particular interest for the realization of binate logic functions [18], such as XOR or parity functions, which are key components of arithmetic data paths. As the transistors intrinsically embed the XOR logic primitive, a simple full-swing XOR-2 was proposed in [5]. This XOR implementation, reported in Fig. 6-a, uses only 4 transistors while the traditional full-swing static CMOS implementation requires 8 transistors [19]. Note that both the control and the polarity gates are connected to the logic gate inputs. For these reasons, cell libraries that exploit this technology can realize more logic functions (with the same number of transistors) as compared to standard CMOS technology [5]. The proposed XOR is based on *Transmission-Gates* (TG) that are used to propagate logic levels from the power rails to the output. Thanks to the TG structure, an XOR-3 gate was derived in [20] from the structure by replacing the power supply signals with a third variable and its complement (Fig. 6-b).

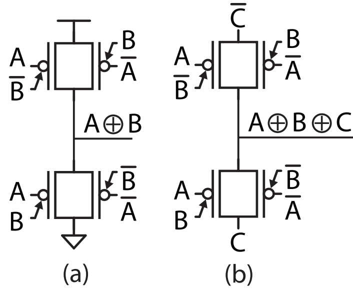

Fig. 6. XOR-2 (a) and XOR-3 (b) gates.

The full adder is a 3-input, 2-output Boolean function defined as:

$$Sum = A \oplus B \oplus C_{in}$$
$$C_{out} = Maj(A,B,C_{in})$$

The *Sum* function can be efficiently implemented in DG-SiNWFETs technology with the XOR-3. The C_{out} function instead requires the computation of the majority operator among the inputs A, B and C_{in}. $Maj(A,B,C_{in})$ can be written as:

$$Maj(A,B,C_{in}) = A.(\overline{A \oplus B}) + C_{in}.(A \oplus B)$$

Consequently, it is possible to adapt the XOR-3 gate to implement the majority function by swapping C_{in} and its complement with *A* and C_{in} respectively. Using the XOR-3 and MAJ-3 gates, the full-voltage swing full adder in Fig. 7 is achieved with only 8 devices, input inverters apart [21]. Note that, in standard CMOS technology, the static CMOS implementation of the full adder requires 28 transistors [19] and 14 transistors for full-voltage swing TG-CMOS [22].

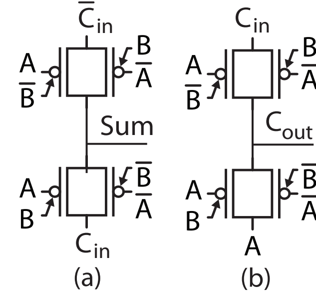

Fig. 7. Full adder with 8 DG-SiNWFETs.

IV. Device Level Robustness Study

As discussed in the previous section, DG-SiNWFETs show an unprecedented opportunity for building arithmetic circuits in a compact way. Emerging technologies always suffer from a common reputation, often justified, of unreliability. However, the processes involved in DG-SiNWFETs device fabrication are extremely simple compared to advanced doped source/drain CMOS. Thus, it is not clear how device geometry and multi-gate stack will impact device reliability. In this section, we will study the robustness of the proposed FETs using a novel prediction methodology based on *Technology Computer-Aided Design* (TCAD) simulations.

A. Defect Sources of SiNW Technology

Vertically-stacked nanowire transistors are built with a very different geometry compared to standard transistors (bulk to FinFETs). Hence, a large uncertainty can arise during the fabrication process. As a first order view, these variations can affect the device during three major fabrication steps:

- *Nanowire patterning through e-beam lithography*: Nanowire patterning is achieved using *Hydrogen SilsesQuioxane* (HSQ) which is very sensitive to variation in electron dose and temperature fluctuation. This directly translates into variations of the *total length of the nanowires* (L_{NW}).
- *Nanowire formation by Bosch process etching*: Variability, in the case of dry etching with Bosch process, originates from various sources. One example is pattern sharpness. Low pattern sharpness, in the case of HSQ, will lead to a tapered nanowire stack, in which bottom nanowires are thicker than top nanowires. This influences the *radius of the nanowires* (R_{NW}).
- *Gate oxide formation and polysilicon deposition*: Variability in this case mainly refers to the *thickness of the grown oxide* (T_{OX}) and the *length of the deposited polysilicon gates* (L_{CG}).

In addition to these main effects, process steps variations may lead to other defects, as listed in Fig. 8. However, the study of their impact is out of the scope of this paper.

Extracting the possible variation and defects of the target device provides the opportunity of both (i) tuning the process technology early in the development (and thus at low cost) and (ii)

studying the device advantages compared to its doped source/drain counterpart.

	DG-SiNWFETs		
	Process	**Variation Model**	**Defect model**
1	Bosch process for nanowire formation	Diameter variation of each nanowire Distance variation among nanowires Variation on number of nanowire	Channel break
2	Oxidation process	Oxide Thickness variation	Oxide break
3	Polysilicon deposition	Variation of PG and CG length and width	Connection between PG and CG Connection between PG and Source, or between PG and Drain Connection miss: Float lateral PG(s), Float PG, and Float CG

Fig. 8. Variations and defects dependence on process steps.

B. *Enabling the Defects Extraction through TCAD*

Nowadays, extraction of device variation and defect models is a costly operation, as it requires the complete characterization of a new technology, which is affordable only when the technology reaches maturity. However, dealing with emerging technologies shifts this paradigm, as it is not possible to wait until the process is mature (for cost reasons) before looking at the reliability of the future devices. Hence, a fast and predictive analysis of the defects and variations is required for advanced technologies.

The proposed method is depicted in Fig. 9. The core of the methodology is based on *Technology Computer-Aided Design* (TCAD) simulations. Widely used by technologists, TCAD simulations are used to predict the electrical behavior of a semiconductor device given its physical description. The physical description indicates the geometry and materials involved. TCAD simulations provide the first order opportunity to design devices without developing or purchasing expensive new fabrication equipment, at a cost of heavy simulation runtime and tough convergence difficulties for complex models.

Using TCAD model description, it is thus possible to describe the impact of the variations related to each process step independently. Our methodology is based on this opportunity. The variations occurring during each process step (such as the variations of gate oxide occurring during nanowire oxidation) are merged with the nominal model using a *homemade* tool that updates the device geometries. The device I/V curve is then computed using *Synopsys Sentaurus* TCAD simulator and processed to extract the device parameters. The procedure is iterated *N* times in order to get enough statistical data.

C. *Application to SiNWFETs*

In this experimental study, we apply the proposed methodology to vertically-stacked SiNWFETs.

1) *Experimental Setup*

The device robustness of DG-SiNWFETs is evaluated and compared to an equivalent single-gate 22nm CMOS technology. The CMOS devices consist of *vertically-stacked Silicon NanoWires FETs* with *doped Source/Drain* contacts (doped S/D SiNWFETs). This technology has been chosen as ultimate extension of FinFETs.

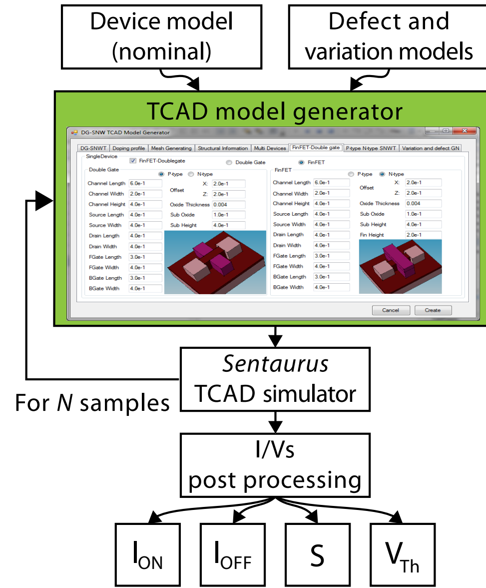

Fig. 9. TCAD device defect and variability extraction tool flowchart.

The nominal voltage is 0.95V. Transistors are both *n*-type (doped S/D SiNWFETs are obtain using Sb dopants, while DG-SiNWFETs are polarized with $V_{PG}=V_{DD}$). Variations, with a standard deviation of 30% from the nominal value, are applied on the *Nanowire Length* (L_{NW} – 107nm nominal for DG-SiNWFETs and 58nm nominal for Doped S/D SiNWFETs), the *Nanowire Radius* (R_{NW} – 7.5nm nominal), the *Oxide Thickness* (T_{OX} – 12nm nominal) and the *Control Gate Length* (L_{CG} – 22nm nominal). These parameters have been selected in order to simulate the impact of each process step involved in the device fabrication, as highlighted previously. For each case study, 100 simulations runs were performed. Non-convergent runs were discarded. Device metrics are the *on-current* (I_{ON}), the *off-current* (I_{OFF}), the *threshold voltage* (V_{Th}) and the *sub-threshold slope* (S).

2) *Experimental Results*

The simulation results of the variation analysis for DG-SiNWFETs and Doped S/D SiNWFETs are shown in Table I. Before looking in detail at the impact of variations through selected plots, some general comments are given. It is worth noting that the average values obtained for the DG-SiNWFETs differ among the different experimental conditions. This is due to convergence issues. Several simulations have been discarded making the input and output distributions no more perfectly Gaussian. However, the global trends remain unchanged and results are still valid under these circumstances. Looking at device performances, DG-SiNWFETs demonstrate lower I_{OFF} values than doped S/D SiNWFETs for the same I_{ON} currents. This means that DG-SiNWFETs exhibit superior I_{ON}/I_{OFF} ratios (around 10^{10} from simulations – 10^{7} from preliminary devices characterization but the measurements reached the resolution limit of the equipment [7]), at a cost of a larger S (around 80mV/dec). Therefore, this makes DG-SiNWFETs extremely well suited for low power applications.

Fig. 10 depicts the I_{ON} evolution under L_{NW}, R_{NW}, L_{CG} and T_{OX} variations. In Fig. 10-a, we observe that L_{NW} is more influent for DG-SiNWFETs than for the doped version (9.2× more). This can

TABLE I
DEVICE LEVEL CHARACTERISTICS UNDER TECHNOLOGICAL VARIATIONS FOR BOTH DG-SINWFETS AND DOPED-SINWFETS

			Double-Gate SiNWFETs				Doped S/D SiNWFETs			
			L_{NW}	R_{NW}	T_{OX}	L_{CG}	L_{NW}	R_{NW}	T_{OX}	L_{CG}
I_{ON}	avg	(µA)	1.34	1.28	1.45	1.44	1.44	1.64	1.44	1.44
	std	(nA)	193.0	**528.7**	48.7	**0.5**	**21.1**	789.4	**0.2**	15.7
I_{OFF}	avg	(fA)	0.70	0.90	0.73	0.72	6.61	9.59	6.07	7.08
	std	(fA)	**0.06**	**0.53**	**0.02**	**0.006**	2.13	8.06	0.43	2.58
V_{Th} (V)	avg	(mV)	338	330	331	333	387	387	388	386
	std	(mV)	17	55	21	9	**5**	**9**	**3**	**8**
S	avg	(mV/dec)	79	80	80	80	64	64	64	64
	std	(mV/dec)	2.4	2.4	4.0	0.9	**1.0**	**1.7**	**0.3**	**0.6**

be explained by the difference between the involved switching mechanisms. DG-SiNWFETs are controlled by two Schottky barriers at the source and drain regions (under the PGs). An increase in L_{NW} does not influence the amount of carriers injected in the device, but creates undesirable undoped intrinsic regions between the gates. In doped devices, an increase in the total length moves the carrier reservoirs away from the gate regions, leading to the slight decrease in I_{ON}. This phenomenon starts to be critical for DG-SiNWFETs even after a variation of 8nm. This confirms the importance for self-aligned structures, that relax the constraints on mask alignments for critical steps.. Fig. 10-b depicts the impact of R_{NW}. I_{ON} of the doped S/D SiNWFETs is almost linear upon the radius of the channel. In doped S/D SiNWFETs, the growth of the nanowire radius corresponds to an increase in transistor width. On the contrary, the *on-current* of DG-SiNWFETs slightly decreases when R_{NW} grows. DG-SiNWFETs rely on the electrostatic control of the source and drain Schottky barriers. Increasing R_{NW} makes the control less precise and fewer carriers are injected. However, it is worth noting that the global deviation is lower in DG-SiNWFETs (1.5× less). This highlights the importance of appropriate nanowire sizing (here the optimum is around 5nm for a 22nm technology node). The significance of the electrostatic doping is also highlighted in Fig. 10-c. Indeed, when T_{OX} increases, I_{ON} of doped devices is not affected significantly, while DG-SiNWFETs are heavily influenced. Finally, the variations of L_{CG}, depicted in Fig. 10-d, is not a dominant factor on the *on-current* of the DG-SiNWFETs while a linear increase in L_{CG} directly translates to I_{ON} in the case of doped S/D SiNWFETs. In DG-SiNWFETs, the gates simply control the barriers, while in doped S/D SiNWFETs, the gate creates the conductive channel. Schottky barrier control is extremely localized, which means that small variations on the gate length do not impact largely their control (3× less).

Fig. 11 also provides some interesting facts about the properties of stacked nanowires. Fig. 11-a demonstrates the effect of R_{NW} variation on the *off-current* (and thus the leakage) for both DG and doped S/D SiNWFETs. Fluctuations in nanowire radius slightly change the I_{OFF} of the DG-SiNWFETs, while it can seriously affect the doped transistor (16× more). Increase in R_{NW} leads to an exponential increase in I_{OFF} for the doped device. This is the impact of a weaker electrostatic control on the channel. On the other hand, DG-SiNWFETs I_{OFF} is less affected by R_{NW} as the carrier injection is blocked at the Schottky barriers and not by the channel depletion. Fig. 11-b shows the variation of V_{Th} under L_{NW} fluctuations. Longer doped nanowires require larger voltages to form the conductive channel, while DG nanowires rely only on their Schottky barriers. This positive effect on the threshold reduction is mitigated by a larger variability (3× more), coming from parasitic intrinsic regions in the device (similarly to Fig. 10-a).

V. DISCUSSIONS

The previous study showed that DG-SiNWFETs present some interesting features for 3 main aspects: device performances, robustness and functionality.

First, we showed that, thanks to their very good I_{ON}/I_{OFF} ratio (10^{10}), DG-SiNWFETs are well suited for *Low-Power* (LP) applications, at a cost of a slightly slower switching (S≈80mV/dec at 22nm node). Such technology opens the way towards a new class of devices in between the regular *High-Performance* (HP) and LP CMOS transistors to address the field of low-power high-performance computing.

Second, DG-SiNWFETs demonstrate interesting robustness properties at the device level. Indeed, for some variations of device geometries, the impact on performances is lower then for standard doped S/D transistors, breaking the traditional cliché about emerging technologies and reliability.

Finally, DG-SiNWFETs enable the realization of very compact arithmetic logic gates, such as XORs and FA. In addition to the gain in area, performance and power consumption, it is possible to appreciate the gate compactness in light of robustness. Indeed, as fewer transistors are used to realize the functionality, the gates will be less prone to variations. Therefore, added to the good robustness properties of the technology, circuits built with DG-SiNWFETs will be even more advantageous with respect to their conventional doped S/D counterparts.

VI. CONCLUSION

In this paper, we introduced the opportunities of DG-SiNWFET technology for building compact and reliable logic gates. Indeed, the in-field polarity control of the devices allows designers to build arithmetic circuits with improved compactness compared to standard doped CMOS transistors. We also studied the performance of the technology with regard to process variations. A novel extraction methodology based on TCAD simulations was then introduced. We demonstrated a good ability of DG-SiNWFETs to tolerate process variations with regard to the off-current showing a 16× smaller standard deviation.

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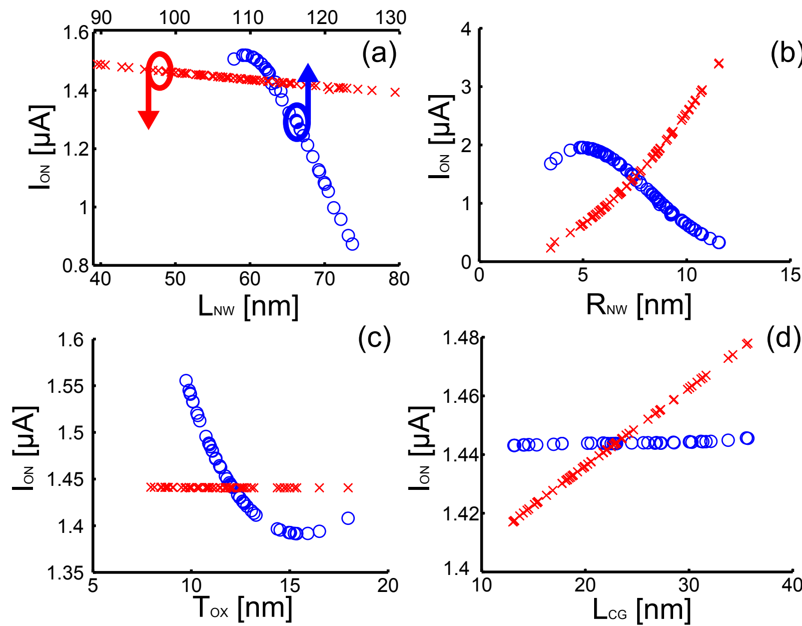

Fig. 10. Impact of L_{NW} (a), R_{NW} (b), T_{OX} (c) and L_{CG} (d) variations on I_{ON} – DG-SiNWFETs (blue) and Doped S/D SiNWFETs (red).

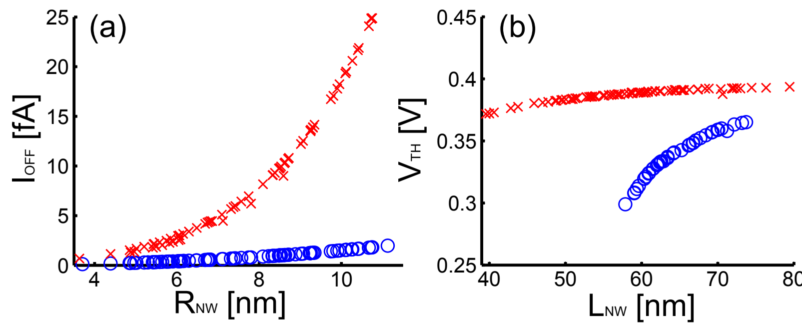

Fig. 11. Impact of R_{NW} on I_{OFF} (a) – Impact of L_{NW} on V_{TH} (b) – DG-SiNWFETs (blue) and Doped S/D SiNWFETs (red).

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