Dual-Threshold-Voltage Configurable Circuits with Three-Independent-Gate Silicon Nanowire FETs

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***Abstract*—We extend ambipolar silicon nanowire transistors by using three independent gates and show an efficient approach to implement dual-threshold-voltage configurable circuits. Polarity and threshold voltage of uncommitted devices are determined by applying different bias patterns to the three gates. Uncommitted logic gates can thus be configured to implement different logic functions for dual-threshold-voltage design using a wiring scheme, to target either high-performance or low-leakage applications. Synthesis of benchmark circuits with these devices shows comparable performance and 54% reduction of leakage power consumption compared to FinFET technology.**

I. Introduction

Leakage power consumption has become an important issue in circuit design [1]. In CMOS technology, multi-threshold-voltage (multi-V_t) design is widely used to reduce the overall leakage power consumption of circuits. Low-V_t devices are used in the critical paths to meet timing constrains, while high-V_t devices with low-leakage are used in slack paths. However, the implementation of multi-V_t circuits requires extra technological steps to build devices with different threshold voltages, which affects the layout regularity and increases the process costs compared to single-V_t design [2]. Adaptive body biasing [3] is another popular technique to mitigate the increasing leakage power consumption, but separate body biasing for tuning threshold voltage of each transistor is hard to achieve due to the area overhead of additional circuits and routing resources [4].

In order to achieve better electrostatic control and reduce short channel effects, FinFETs have been successfully used for the 22-nm technology node [5]. To achieve an even better electrostatic control [6], vertically-stacked *Si*licon *N*ano*W*ire *FETs* (SiNWFETs) with gate-all-around control have shown to be a natural extension of FinFETs. Furthermore, the use of metal contacts in the source and drain regions creates Schottky barriers that can be electrically trimmed to take advantage of the inherent ambipolar behavior, i.e., the simultaneous n-type and p-type characteristics. This ambipolar phenomenon is directly exploited within vertically-stacked *D*ouble-*G*ate (DG) SiNWFET [7]. By using a double-independent-gate structure, the polarity of the device (i.e., type of carriers) can be selected electrically. Ambipolar DG SiNWFETs are desirable for the development of new logic architectures, which are intrinsically not implementable with CMOS in a compact form [8]. Moreover, their leakage current can be further reduced by increasing the threshold voltage of the devices [9].

In this paper, we introduce vertically-stacked *T*hree-*I*ndependent-*G*ate (TIG) SiNWFET. The proposed TIG SiNWFET is ambipolar and also enables tuning of the threshold voltage. Dual-V_t configurable circuits are achievable by applying different connection schemes to uncommitted devices, and are expected to demonstrate high performance with even lower leakage power consumption as compared to circuits built with low-power FinFETs. Synthesis of benchmark circuits onto TIG SiNWFETs shows comparable performance and 54% reduction of leakage power consumption compared to FinFET counterpart.

The remaining parts of this paper are organized as follows. In Section II, we present the vertically-stacked TIG SiNWFET technology and introduce its operation modes under different bias conditions. In Section III, we map basic logic gates onto an uncommitted pattern with both low-V_t and high-V_t configurations and we present the connection strategy for dual-V_t design. Performance of logic gates and benchmark circuits with TIG SiNWFET is compared with FinFET technology in Section IV followed by conclusions in Section V.

II. Three-Independent-Gate Silicon Nanowire FET

In this section, the technology of vertically-stacked TIG SiNWFET is introduced. Polarizability and leakage control of the device are then discussed. TCAD simulation validates the dual-V_t ambipolar characteristic of the device.

A. Technology

Fig.1 illustrates a vertically-stacked silicon nanowire FET with three independent gate-all-around gate regions. In this vertically-stacked structure, the driving strength is determined

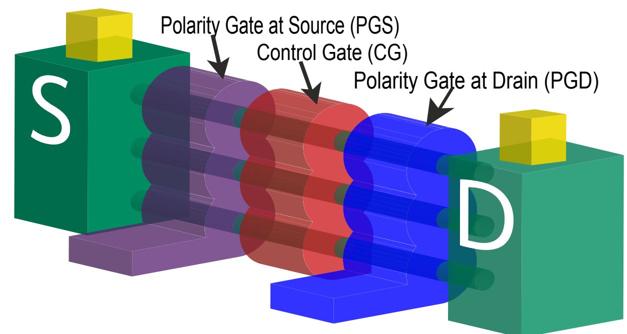

Fig. 1. Structure of a vertically-stacked three-independent-gate SiNWFET.

by the number of nanowires being connected, without any impact on area. This device can be fabricated with the same top-down process of vertically-stacked DG SiNWFET described in [7]. Differently from DG SiNWFET, *P*olarity *G*ate at *S*ource (PGS) and *P*olarity *G*ate at *D*rain (PGD) are independent and modulate the Schottky barrier thickness to tune respectively the tunneling of electrons and holes. The *C*ontrol *G*ate (CG) in the inner region is used to switch the channel conduction as in conventional MOSFETs.

B. Operation of TIG SiNWFET

By independently biasing the three gates to ground or V_{DD}, the 8 possible operation modes of this device are divided into 4 groups: two ON sates, two standard OFF states, two low-leakage OFF states, and two uncertain states which will not be used. Fig.2 illustrates the six most important operation modes and their corresponding band diagrams when $V_{DS}=V_{DD}$ (i.e., S='0' and D='1').

1) ***ON states:*** As shown in Fig.2(a)(b), when PGS=PGD, one of the Schottky barriers is thin enough to allow hole tunneling from drain (*p*-type) or electron tunneling from source (*n*-type). CG controls the flow of majority carriers through the device, and turns the device ON or OFF.

2) ***OFF states:*** Current is shut off due to the barrier induced by opposite biasing of control gate and polarity gates as shown in Fig.2(c)(d). Nevertheless, small number of carriers are still tunneling through the thin barrier into the channel.

3) ***Low-leakage OFF states:*** When PGS=S and PGD=D in Fig.2(e)(f), thick barriers prevent carriers from tunneling at both source and drain and ensure minimum leakage in the device [9].

4) ***Uncertain states:*** When PGS='1' and PGD='0', barriers are thin enough for tunneling. However, this condition may also create an unexpected barrier in the inner region that will block the current flow, and cause signal degradation. Hence, the uncertain states should be prohibited by always fixing PGD='1' (PGS='0') for *n*FET (*p*FET), or using PGD=PGS.

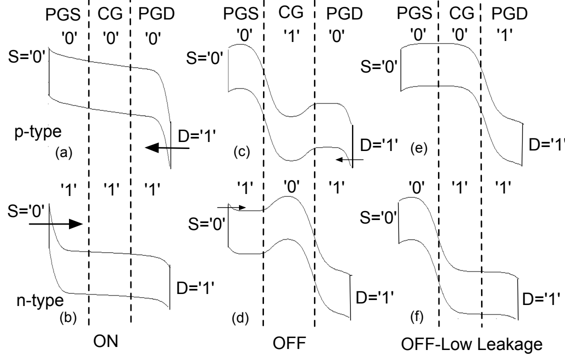

Fig. 2. ON, OFF and low-leakage OFF operation modes and their corresponding band diagrams.

C. TCAD Performance Estimation

A single TIG SiNWFET is simulated by using *Synopsys Sentaurus*. Three 24-nm metal gates with mid-gap workfunction are placed on HfO_2 high-κ dielectric layer. Schottky barrier height for electron is set to 0.35eV in the simulation to get nearly symmetric *n*-type and *p*-type characteristics. V_{DD}=1.2V is applied. Note that, TIG SiNWFET requires larger V_{DD} than conventional MOSFET because of the high Schottky barrier and the longer channel length.

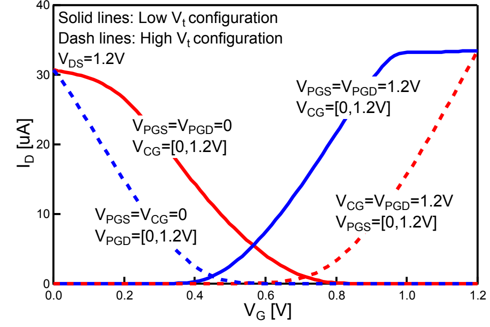

Fig. 3. Dual-V_t ambipolar characteristic of a single TIG SiNWFET.

Dual-V_t characteristic of TIG SiNWFET is depicted in Fig.3. For low-V_t configuration (solid lines), PGS and PGD are biased as in Fig.2(a)(b), and a voltage sweep is applied on CG. In this configuration, the device is switching between ON and standard OFF states. For high-V_t configuration (dash lines), the device is wired unconventionally. Indeed, fixed bias voltages are now applied to CG and PGS for *p*-type (CG and PGD for *n*-type), while a voltage sweep is applied on PGD (PGS). Here, the device is switching between ON and low-leakage OFF states. The difference between the low V_t and the high V_t is about 0.3V. Note that, I_{on} of both low-V_t and high-V_t configurations keep the same value since they have the same ON states shown in Fig.2(a)(b).

III. Physical Design of Dual-V_t Circuits

In this section, an uncommitted logic gate pattern is introduced and basic logic functions are mapped onto it. By using both low-V_t and high-V_t configurations, logic gates towards either *H*igh *P*erformance (HP) or *L*ow *L*eakage (LL) applications are implemented using different connection schemes.

A. Uncommitted Logic Gate Pattern

An uncommitted logic gate pattern built with four TIG SiNWFETs is shown in Fig.4(a). It consists of two parallel transistors in the pull-up/pull-down path. Logic gates are

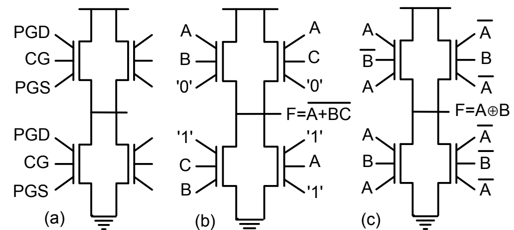

Fig. 4. (a) Uncommitted logic gate pattern, (b) AOI gate and (c) XOR gate mapped onto this logic gate pattern.

mapped onto this pattern avoiding uncertain states (see Section II).

Fig.4(b) presents an example of an AOI gate. Its functionality is obtained by fixing PGS to '0' for *p*FET and PGD to '1' for *n*FET. PGD of *p*FET (PGS of *n*FET) and CG implement the function of two conventional MOSFETs in series. Thus, only 4 transistors are needed for this AOI gate, instead of 6 conventional MOSFETs. In Fig.4(c), an XOR gate is mapped onto this pattern as in [10]. In this XOR circuit, TIG SiNWFETs reduce to DG SiNWFETs, which are efficient to implement binate logic functions. Note that, with the proposed gate pattern, each pull-up and pull-down path has only one series transistor.

B. Dual-V_t Design with Uncommitted Logic Gate Pattern

Fig.5 illustrates two different mapping schemes of NAND gate for HP and LL applications. In Fig.5(a), the HP gate is obtained by connecting inputs to the CGs of *p*FETs. Thus, the performance for pulling the logic gate up is improved by applying the low-V_t configuration of the devices (solid line in Fig.3). In contrast, the LL gate (Fig.5(b)) is obtained by controlling the *p*FETs from the PGDs. Leakage power is thereby reduced by forcing the devices into high-V_t operation (dash line in Fig.3). In both HP and LL gates, PGSs and CGs of *n*FETs are connected to input signals. Hence, delay and leakage in pull-down paths cannot be further tuned.

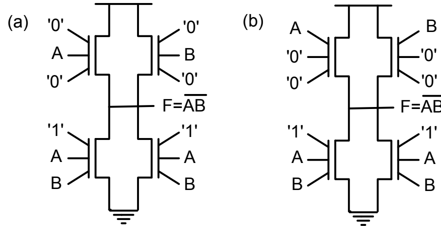

Fig. 5. Mapping of NAND gate towards (a) HP and (b) LL application.

C. Connection Schemes for Dual-V_t Design

As observed previously, most of the TIG SiNWFET access gates have a fixed polarity. Hence, power and ground signals are spread all over the proposed logic gate pattern. In order to minimize the routing effort for power lines, the power distribution network is consequently optimized. A grid network

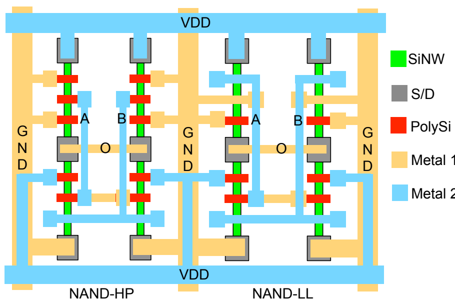

Fig. 6. Connection schemes of NAND gate towards HP and LL application.

is built with a mesh of power and ground lines. Based on this novel power distribution grid, different connection schemes of NAND gate are demonstrated in Fig.6, corresponding to the HP and the LL configurations shown in Fig.5, respectively.

IV. Logic Synthesis of Benchmark Circuits

In this section, the effect of leakage power reduction by applying the physical design approach for dual-V_t configurable circuits is discussed for logic gates and benchmark circuits.

A. Methodology

A simple model for proposed TIG SiNWFET is written in Verilog-A to enable circuit-level simulations. The equivalent circuit of a single TIG SiNWFET is shown in Fig.7. The current source is described by a table model extracted from TCAD simulation. Access resistances are estimated according to the device geometry, and each capacitance is extracted from TCAD simulation as an average value under all possible bias conditions. According to the capability of vertically-stacked silicon nanowire technology, we assume that there are four nanowires per stack. The stack is modeled by parallel arrangement of single TIG SiNWFET model.

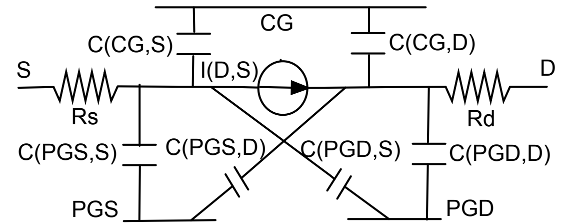

Fig. 7. Equivalent circuit model of TIG SiNWFET.

A logic cell library built from the uncommitted logic gate pattern described in Section III is characterized using *Cadence Encounter Library Characterizer (ELC)*. The library consists of basic combinational logic cells INV, NAND, NOR, XOR, XNOR, AOI, OAI in both HP and LL configurations. The impact of proposed connection scheme is considered in cell area estimation. An ideal wire-load model scaled from 45-nm technology is applied to take into account the capacitance and resistance of the interconnections. The supply voltage of vertically-stacked TIG SiNWFET library is 1.2V.

Since we are demonstrating a physical design approach to implement dual-V_t circuits for standby power reduction, a counterpart library with supply voltage of 0.9V is built with *P*redictive *T*echnology *M*odel (PTM) 24-nm FinFET model for *L*ow-*ST*andby-*P*ower (LSTP) application [11].

With both TIG SiNWFET and FinFET libraries, ISCAS'85 combinational benchmark circuits are synthesized by *Synopsys Design Compiler*.

B. Gate Level Characterization

Table I lists the maximum fanout-of-4 delay, leakage power and area of some logic gates built with TIG SiNWFET and FinFET using *Cadence ELC*. The average comparison results are depicted in Fig.8.

TABLE I
PERFORMANCE OF LOGIC GATES WITH TIG SINWFET AND FINFET

Gates		TIGNW HP	TIGNW LL	FinFET
INV	Delay [ps]	22.2	27.8	20.7
	Leakage [pW]	4.02	0.56	6.43
	Area [μm^2]	0.105	0.105	0.070
NAND	Delay [ps]	26.5	32.0	25.8
	Leakage [pW]	7.17	1.12	6.88
	Area [μm^2]	0.210	0.210	0.140
XOR	Delay [ps]	41.9	47.4	50.1
	Leakage [pW]	13.06	6.15	41.36
	Area [μm^2]	0.420	0.420	0.420
AOI	Delay [ps]	26.4	31.2	30.7
	Leakage [pW]	7.19	4.59	7.05
	Area [μm^2]	0.210	0.210	0.210

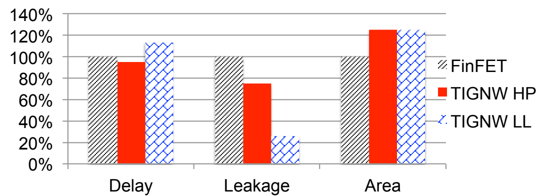

Fig. 8. Comparison results of logic gates with TIG SiNWFET and FinFET.

The LL TIG SiNWFET gates demonstrate a leakage power reduction of 74% compared to FinFET gates, at a cost of a 14% increase in delay. The low-leakage property stems from the good control of the thick Schottky barriers in the device that prevents carriers from tunneling into the channel during OFF state.

The HP TIG SiNWFET gates demonstrate a slight 5% reduction in delay as compared to FinFET gates. Among HP gates, AOI and XOR gates show 15% gain in performance and comparable area than FinFET, while INV and NAND gates show larger delay and area. While INV and NAND gates have the same implementation as in CMOS, AOI and XOR gates are implemented on the proposed uncommitted logic gate pattern in a very different way. Indeed, the gates have only one transistor in each pull-up and pull-down path that is consequently of benefit to the different metrics.

C. Circuit Level Results

Critical path delay, leakage power, and area of ISCAS'85 benchmark circuits are reported for both dual-V_t TIG SiNWFET and LSTP FinFET libraries in Table II. HP gates are applied in critical paths, while LL gates are used in non-critical paths. All the devices used in dual-V_t circuits use the same original uncommitted pattern. Fig.9 shows the average comparison results. Dual-V_t circuits with TIG SiNWFET keep comparable performances but reduce the leakage power consumption by 54% compared to FinFET circuits. An additional area cost of 28% is due to the larger size of three-independent-gate devices.

TABLE II
DELAY, LEAKAGE, AND AREA OF ISCAS'85 BENCHMARK CIRCUITS WITH DUAL-V_t TIG SINWFET AND LSTP FINFET

Circuits	Dual-V_t TIG SiNWFET			LSTP FinFET		
	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]
c432	0.28	0.850	42.95	0.28	1.791	31.15
c499	0.22	2.359	89.57	0.23	5.476	71.82
c880	0.22	2.250	111.51	0.22	4.815	83.44
c1355	0.23	2.821	112.46	0.22	5.623	75.46
c1908	0.31	2.132	92.09	0.32	5.550	77.21
c2670	0.19	2.821	139.44	0.19	7.427	112.14
c3540	0.39	5.841	245.39	0.35	11.579	199.85
c5315	0.26	6.722	329.18	0.26	15.469	250.39
c6288	1.05	19.997	731.43	1.05	28.470	520.17
c7552	0.27	8.315	393.02	0.24	26.661	395.57

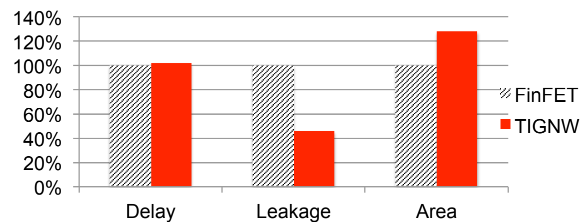

Fig. 9. Average comparison results of ISCAS'85 benchmark circuits with Dual-V_t TIG SiNWFET and LSTP FinFET.

V. CONCLUSIONS

In this work, an efficient approach to implement dual-V_t configurable circuits with a novel three-independent-gate silicon nanowire FETs is presented. This device can be electrically configured in terms of polarity and threshold voltage. Logic gates using these devices can thus be well suited to high performance and low leakage applications, and can be obtained by wiring an uncommitted gate structure. Benchmarking results show that comparable performance can be achieved with a 54% reduction of leakage power consumption for circuits based on TIG SiNWFET compared to FinFET technology.

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