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Post-CMOS Processing and 3-D Integration Based on Dry-Film Lithography

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***Abstract*— This paper presents a chip-level post-complementary metal oxide semiconductor (CMOS) processing technique for 3-D integration and through-silicon-via (TSV) fabrication. The proposed technique is based on dry-film lithography, which is a low-cost and simple alternative to spin-coated resist. Unlike conventional photolithography methods, the technique allows resist patterning on very high topography, and therefore chip-level photolithography can be done without using any wafer reconstitution approach. Moreover, this paper proposes a via sidewall passivation method which eliminates dielectric etching at the bottom of the via and simplifies the whole integration process. In this paper, two 50-μm-thick chips were post-processed, aligned, bonded, and connected by Cu TSVs, which have parylene sidewall passivation. Daisy-chain resistance measurements show 0.5-Ω resistance on average for 60-μm-diameter TSVs, with a yield of more than 99% for 1280 TSVs from five different chip stacks. Subsequently, the techniques were applied to CMOS microprocessor stacking as a test vehicle. Die-level post-CMOS processing for 40-μm-diameter via etching, redistribution layer patterning, and chip-to-chip bonding were successfully demonstrated with the real chips.**

***Index Terms*— 3-D integration, die-level processing, dry-film lithography, parylene bonding, post-complementary metal oxide semiconductor (CMOS) processing, through-silicon via (TSV), via-last TSV.**

I. Introduction

The continuing demand for faster and smaller integrated circuits (IC) has led to aggressive downscaling in transistor sizes, as predicted by Moore's Law [1]. Today's state-of-the-art IC technology offers fascinating levels of performance and functionality while introducing new barriers and challenges for further downscaling. As conventional planar IC designs have almost reached their limits, an emerging technology called 3-D integrated circuit promises new possibilities to achieve higher volumetric transistor density. This technology enables the integration of identical layers (homogeneous integration) or disparate layers with different functionality, size, and technology (heterogeneous integration), as illustrated in Fig. 1. The layers are electrically connected with vertical interconnections, called through-silicon vias (TSVs), providing potential performance improvements even in the absence of device scaling. Extensive studies by numerous research groups have already verified the potential of this technology for better electrical performance, lower power consumption, lower noise, smaller form factor, and more functionality [2].

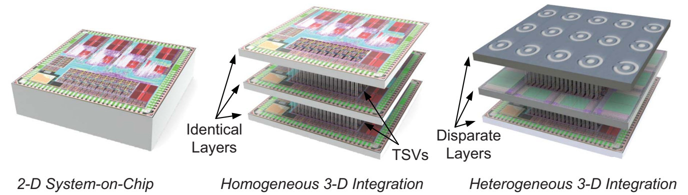

Fig. 1. Illustrations of conventional 2-D, homogeneous 3-D, and heterogeneous 3-D integration concepts.

In this context, this paper aims to develop a generic platform for the stacking of chips fabricated through multiproject-wafer runs, especially for low-cost and flexible prototype development. Therefore, all the layers in the stack are already diced chips and the subsequent process steps are complementary metal oxide semiconductor (CMOS)-compatible. We consider heterogeneous integration for sensing applications [3] and 3-D multiprocessor systems [4] as the target applications for the proposed technology; however, the techniques can be applied to many other applications that require post-CMOS processing in general, such as CMOS-microelectromechanical system (MEMS) cofabrication [5]. We previously presented chip-level post-CMOS processing techniques based on stencil lithography [6] and 3-D integration techniques based on template alignment [7]. In this paper, on the other hand, dry-film resist has been employed as an alternative to traditional photolithography methods. Furthermore, a new parylene deposition technique is proposed for via sidewall passivation without the need for bottom dielectric etching.

Table I summarizes the major 3-D integration techniques, highlighting the ones used in this paper. What follows is a brief summary of the motivation for why those particular methods have been preferred. First, via-first [8]–[10] and via-middle [11], [12] type TSVs can only be fabricated in a CMOS foundry. Therefore, via-last approach is preferred to develop 3-D prototypes in a MEMS clean room after the pretesting and selection of working chips (known-good-die or KGD). Second, chip-to-chip (C2C) integration is employed

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TABLE I
SUMMARY OF THE BASIC PROCESSING STEPS AND 3-D INTEGRATION APPROACHES (THE TECHNIQUES USED IN THIS PAPER ARE IN BOLD)

Process steps	TSV fabrication, thinning, alignment, bonding
TSV type	Via-first, via-middle, via-last before bonding, via-last after bonding
Singulation level	Wafer-to-wafer, chip-to-wafer, chip-to-chip
Stacking orientation	Face-to-face (F2F), back-to-face (B2F)
Bonding	Metal-to-metal, dielectric-to-dielectric, hybrid
Alignment	W2W aligner, pick-and-place, template alignment, electrostatic, magnetic, surface-tension-driven

because of the technological limitations and the difficulties of wafer-level [13]–[15] processing for heterogeneous integration, as well as because of the compatibility issue of the MEMS tools with the CMOS wafers. This paper considers polymer bonding an effective method for chip stacking since it allows bonding at lower temperatures and the bonding quality is not as sensitive to the surface topography as other bonding techniques [16]. TSVs are fabricated after dielectric bonding in order to eliminate the reliability problems related to the metal–metal bonding. Finally, B2F orientation is preferred in order to allow stacking of multiple layers in a modular manner. Compared to the blind-via fabrication techniques where the TSV is etched from the backside till the landing metal [17], the proposed via-after-bonding strategy is much simpler since it eliminates several fabrication steps, such as temporary bonding to handle wafer, metal–metal bonding, and passivation layer patterning inside the via openings. On the other hand, the main drawback is that the frontside vias block the BEOL layers; thus, an exclusion zone is required for each TSV. In the following section, a detailed description of the proposed fabrication process is given and the results of dummy Si chips are provided. Then, the preliminary results on the CMOS microprocessor stacking are presented in the final section.

II. 3-D INTEGRATION BASED ON DRY-FILM LITHOGRAPHY

Dry-film resist is a thick photo-definable polymer film which has been widely used in printed circuit board manufacturing. The film can be applied by lamination regardless of the substrate shape and dimension, and it does not require any clean room facility and expensive processing tools. Thickness uniformity, fast and simple processing, excellent adhesion, and almost vertical sidewalls can be listed among the benefits of dry film, which make it attractive in MEMS applications. It has been demonstrated that the dry film can be used as the electroplating mold in LIGA-type processes as an alternative to SU$-$8 [18]. Vulto *et al.* proposed that the film can be employed in microfluidic channel fabrication by bonding two substrates with the patterned dry film [19], [20]. More recently, 3-D microfluidic structures were fabricated through multilayer lamination and direct projection lithography [21]. Particularly for the 3-D integration technology, CSEM (Switzerland) researchers have presented a CMOS-compatible TSV fabrication process based on dry-film lithography [22]. Later, Jacquet *et al.* employed the dry film to etch the dielectric passivation only at the bottom of the via by using the tenting property of the dry-film lamination [23]. In this paper, we employ dry film for chip embedding, via etching (top chip), surface passivation etching (bottom chip), redistribution layer (RDL) patterning (bottom chip), and via filling by Cu electroplating (bonded stack).

Fig. 2 illustrates the complete process flow used for post-CMOS processing and C2C stacking. For the first verification tests, dummy silicon chips with a thermal oxide layer (1 μm) and Ti/Al (20/200 nm) test patterns are fabricated. The top chip and the bottom chip comprise complementary patterns to form the daisy-chain connections after bonding and TSV fabrication. After dicing the wafers with an automatic dicing tool, the chips are transferred to the UV grinding tape. Then, the top chip and the bottom chip are thinned down to 50 μm using a Disco DAG810 automatic grinder. The chips are then released from the grinding tape after exposing the tape to the UV light (365 nm) by a Powatec U-200 UV curing tool. Fig. 3 shows the camera photos of the wafer after the dicing and grinding steps.

A. Chip Embedding

The proposed technique allows the processing of diced chips without the need of a carrier wafer having through openings for chip embedding. A similar C2W alignment approach was proposed with a patterned BCB layer as the alignment template [24]. Such template alignment techniques eliminate the requirement of C2W bonding tools [25], and they promise comparable alignment accuracy by manual die insertion into the cavity. The photolithography process starts with the lamination of the dry film on a single-side-polished Si wafer (Step 1). Prior to the lamination, the wafer is exposed to O_2 plasma to clean and dehydrate the surface. ORDYL ALPHA940 (from ELGA EUROPE SRL) dry-film resist (40-μm thick) is laminated at 110 °C by using an office laminator. In this film, a negative-tone photosensitive layer is sandwiched between two polyester protective films, where the bottom protective film is removed before the lamination, and the top one is removed after exposure in order to prevent adhesion to the mask. For the exposure, two approaches can be followed: 1) exposure through the mask, and 2) exposure by using the chip itself as the mask since dry film is a negative-tone resist (Step 2). The first approach allows higher throughput, as many chip openings can be patterned at the same time. However, this requires prior chip dimension measurement so that the mask can be designed accordingly. In the latter approach, on the other hand, the chip is placed on the dry

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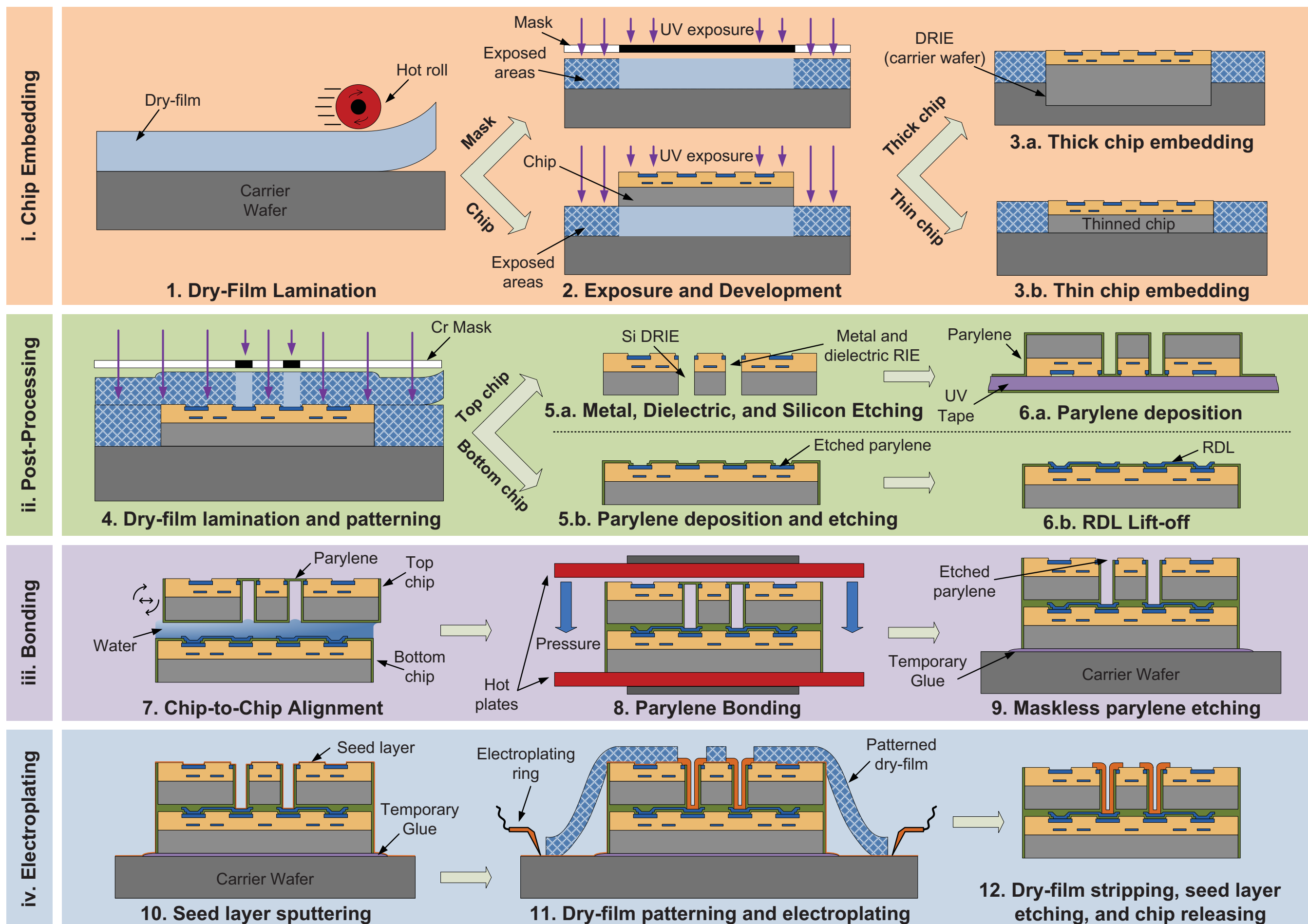

Fig. 2. Process flow for post-CMOS processing and chip-to-chip integration. First, the chips are placed on a carrier wafer and the dry-film resist is laminated and patterned. For the top chip, Al pad, dielectric layers and the Si substrate are etched all the way through to the chip backside. Meanwhile, the bottom chip surface is passivated by parylene deposition and patterning, then the RDL is patterned by the lift-off process employing dry-film resist as the sacrificial layer. Following the via sidewall passivation for the top chip, two chips are aligned and bonded. Finally, the chips are electrically connected by Cu electroplating. If required, these steps can be repeated for a multilayer stack by using the already bonded chips as the bottom chip.

film and the exact chip area is transferred to the film by exposure. The disadvantage of this technique is that chips should be prealigned manually. After the exposure step, the unexposed regions are etched in Na_2CO_3 1% solution. A short O_2 plasma cleaning follows the development and rinsing to remove the dry-film residuals. We verified that a 1-min (500-W) plasma cleaning was usually sufficient. Additional 1-min cleaning can be followed after inspection if there is still any dry film left at the patterned edges. However, long exposure to O_2 plasma may burn and destroy the film.

B. Photolithography and Post-Processing

The chips are placed into the openings in the following step (Step 3). Depending on the thickness of the chip, Si wafer with the dry-film openings can be etched by DRIE to have a deeper opening for thicker chips (Step 3.a). A second dry-film lamination step is then employed for patterning (Step 4). We experimentally verified that the 40-μm-thick dry-film lamination could tolerate up to 100 μm of surface topography. Embedded and laminated chips are exposed to UV-light through a Cr mask for the patterning. In case the chip openings have been patterned by a mask with a multiple chip opening layout, then the whole wafer can be exposed with single exposure in the second photolithography step. Otherwise, if the chip itself has been used as the mask by manual placement, then each chip should be aligned and exposed one by one by using a shadow mask allowing exposure of only one chip at a time. Fig. 4 shows the carrier wafer after chip placement and dry-film lithography, as well as the microscope image of the dry-film patterns for via etching. Based on the photolithography test patterns, it was concluded that the circular openings having diameters less than 40 μm could not be defined precisely due to the resolution limit of the dry-film employed. In order to clean the dry-film residues, especially those left at the edges of the smaller openings, the wafer is exposed to a 500-W O_2 plasma for 2 min.

Following the second dry-film patterning for the via openings (top chip), the Al pad, dielectric layers, and the Si substrate are etched by anisotropic dry etching (Step 5.a). Here, two approaches are possible. If thick chips are used (Step 3.a), a blind via is created by partial etching, then the chip backside is thinned till the via opening is reached. In the alternative approach, chips are thinned prior to the etching

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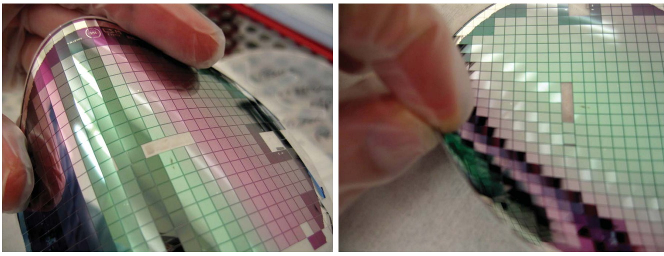
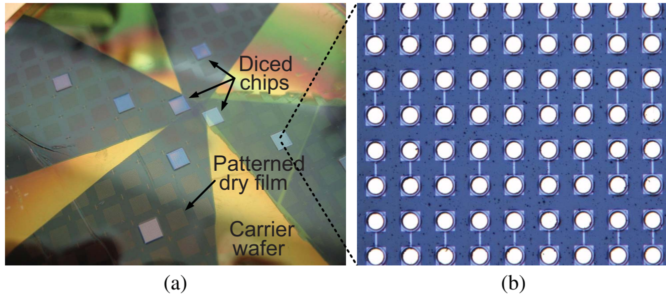


Fig. 3. Camera photos of the diced and thinned wafer, where each chip measures 3.5 by 3.5 mm and the final thickness is 50 μm. (The UV tape is transferred to the backside after grinding for frontside inspection.)



(a) (b)

Fig. 4. Fig. 4. (a) Camera photo of the carrier wafer with the diced chips and patterned dry film. (b) Microscope image showing the via openings on the dry-film and the Al pads on the chip.

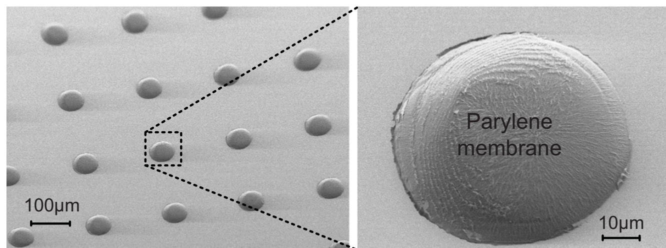
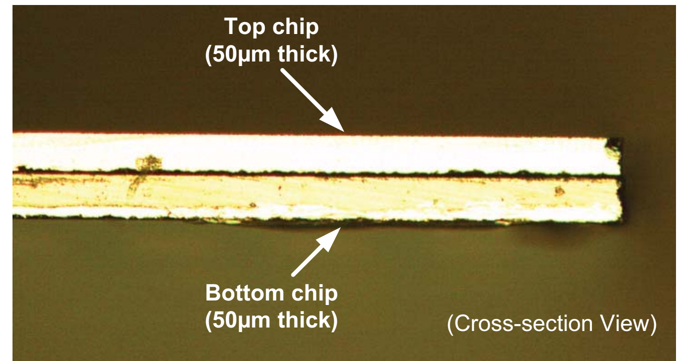


Fig. 5. SEM photo of the chip after releasing the UV tape, leaving a 2-μm-thick parylene membrane on the frontside of the chip.

and embedded into the carrier wafer (Step 3.b), and then vias are formed by through etching. Following the etching process, the via sidewalls are passivated by parylene deposition. The use of polymer liner for TSV passivation has been previously demonstrated [7], [26], [27]. In conventional techniques, the deposited dielectric layer on the landing pad has to be etched. This may require photolithography on high topography and very controlled anisotropic etching to protect the sidewall passivation. In this paper, on the other hand, a novel technique is employed to eliminate the dielectric etching at the bottom of the via. The through-etched chips are placed on a UV-sensitive tape as the chip frontside is facing the tape. Then, a pinhole-free and very conformal parylene layer is deposited at room temperature (Step 6.a). This deposition passivates the sidewalls and forms a parylene layer at the chip backside, which is used as the adhesive layer during C2C bonding. After exposing the tape to UV light, the tape is released, leaving a parylene membrane on the frontside, as shown in Fig. 5. After the bonding, this membrane is etched by using standard etching recipe without any mask.



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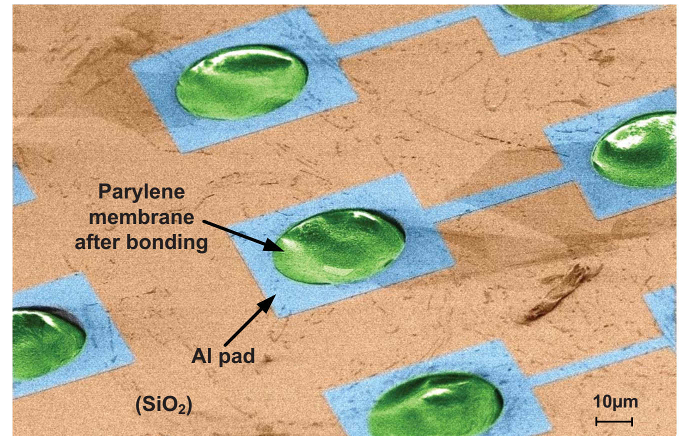

(b)

Fig. 6. (a) Microscope image of the cross-section of two 50-μm-thick chips bonded with parylene intermediate layer. (b) SEM photo of the top chip frontside after bonding.

C. Chip-to-Chip Bonding

After the post-processing, the chips are aligned and bonded (Step 7). Here, both the template alignment technique [7] and surface-tension-driven self-alignment [28] can be employed. In the latter technique, top and bottom chips are exposed to a short O_2 plasma to turn the parylene surface to hydrophilic. The bottom chip is placed on a hydrophobic surface and two chips are aligned by a water droplet. Next, aligned chips are bonded by using a low-cost thermal nanoimprinter tool (Step 8). In the test vehicle, the adhesive bonding is performed at 200 ºC for 30 min in an EHN-3250 Thermal NanoImprinter (ESCO, Japan). Fig. 6 shows the cross-section of two 50-μm-thick chips bonded by the parylene intermediate layer. The SEM photo of the top chip surface is given in Fig. 6, which shows some deformation on the parylene membrane; however, this is not critical since the membrane will be etched in the next step, leaving the parylene only on the sidewalls.

Following the bonding, the chip stack is temporarily attached to a Si carrier wafer by using a thermoplastic polymer wax, QUICKSTICK 135. The parylene membrane is then etched by maskless anisotropic parylene etching in O_2 plasma generated by an STS Multiplex ICP (Step 9). In other TSV fabrication techniques, the dielectric passivation has to be etched at the bottom of the via. This requires either photolithography steps to protect the dielectric layer elsewhere or a well-controlled etching process to properly

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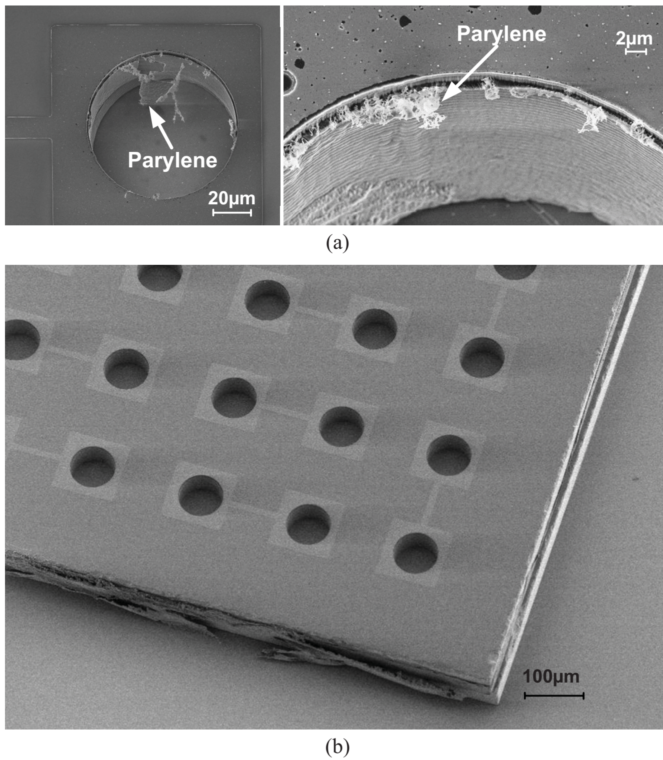

(a)

(b)

Fig. 7. (a) SEM photos showing the parylene residuals after the etching step. (b) SEM photo of the vias after parylene etching and washing steps.

clean the dielectric on the landing pad. This is usually difficult, given that etch rate decreases as the aspect ratio of the via increases. The proposed approach, on the other hand, allows parylene etching only on the surface, which is much easier and more controllable. Moreover, the technique allows both sidewall passivation and backside adhesive layer deposition steps in a single parylene run. Fig. 7 shows the SEM images of the etched and passivated vias just after anisotropic parylene etching, showing the parylene residuals at the via edges. Thereafter, the wafer with the mounted chip stacks is rinsed in DI water and dried with the N_2. Fig. 7 shows the chip stack after the washing and drying steps, showing no visible parylene residuals.

D. Cu Electroplating

In order to finalize the TSV, a conductive layer connecting the bottom pad to the top is required. Cu lining electrodeposition process is preferred since it allows less electrodeposition time compared to fully filling the openings [29]. In addition, more complex electroplating bath chemistries and techniques for void-free superconformal filling are avoided. In this paper, Cu lining is electroplated with an INTERVIA Cu 8510 bath by using sputtered Cu film as the seed layer. Prior to the deposition, the chip surface, particularly the oxide layer on the Al pads, is cleaned by Ar ion bombardment in BAS450 sputtering tool. Then, without breaking the vacuum, 500 nm of Cu is sputtered by dc magnetron sputtering (Step 10). Similar to the aforementioned photolithography steps, dry-film resist is laminated and patterned in order to inhibit the electroplating in the areas other than the TSV openings (Step 11). After dry-film

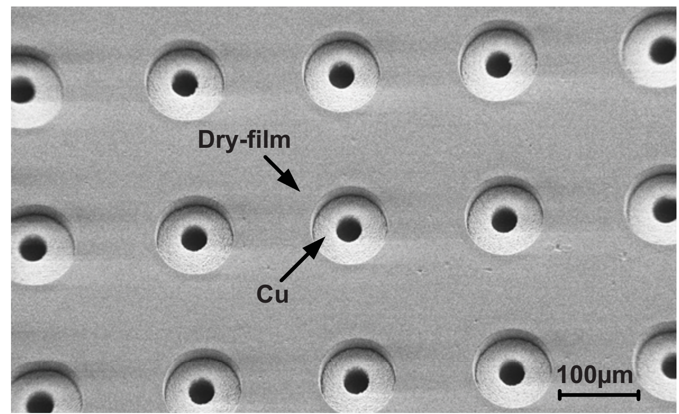

Fig. 8. SEM photo showing the dry-film mask and the electroplated Cu inside the via openings.

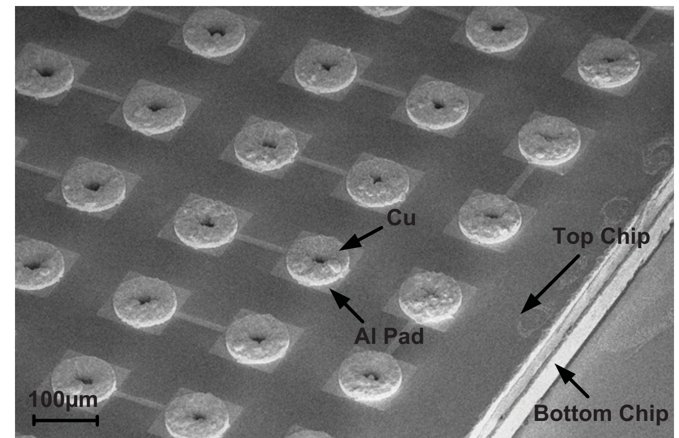

Fig. 9. SEM photo of the vias after maskless seed layer etching.

lithography, the wafer is exposed for 1 min to an O_2 plasma to clean the dry-film residuals inside the openings and to increase the surface wettability. Electroplating is performed by applying a dc current controlled by a general-purpose potentiostat (from AMEL instruments). Fig. 8 shows the electroplated Cu grown inside the dry-film mask.

Following the electroplating, rinsing and drying steps, the dry-film resist is stripped in NaOH 2.5% solution. Alternatively, it was verified that metal-ion-free positive-resist strippers could be employed with the help of elevated temperature (around 65 °C) and ultrasonic agitation. Cu seed layer is etched in a $(NH_4)_2S_2O_8 + H_2SO_4$ (96%) solution for 3 min with an etch rate of 200 nm/min. This etchant also etches the electroplated Cu, but the etched thickness is negligible compared to the initial thickness of the electrodeposited Cu. The compatibility of the temporary mounting wax to this etchant was also verified in this step. The chip stack after the maskless seed layer etching is shown in Fig. 9, which clearly demonstrates the precision of the alignment and uniformity of the electroplating. Some roughness on Cu is observed, which it is believed to be related to poor composition of the electroplating bath.

For the cross-section inspection, the chips are released from the carrier wafer by placing the wafer on a hotplate at around 100 °C, during which the wax softens. The wax residuals at the

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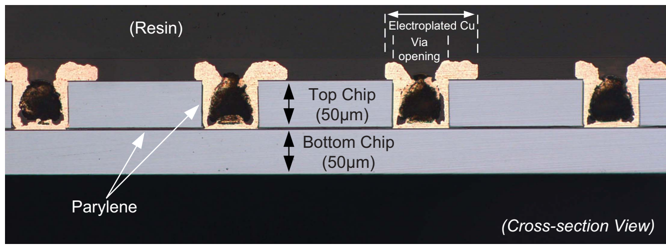


Fig. 10. Cross-sectional view of the TSVs after polishing, showing the 60-μm-diameter TSV opening and 100-μm-diameter electroplated Cu with 15-μm thickness on the surface.

chip backside are cleaned by acetone followed by isopropyl alcohol (IPA). Then, the chip surface is covered by a special resin, and one edge of the stack is polished till the middle of the via. Fig. 10 shows the cross-section of the TSVs after the polishing step. The continuous Cu line from bottom pad to the top and the parylene between the chips and on the sidewalls are clearly visible. The off-centered plating at the top of the via is related to the misalignment of the final dry-film lithography. It is also seen that the Cu thickness decreases at the bottom of the via. This phenomenon is related to the higher electroplating rate at the chip surface, which can be controlled by optimizing the concentrations of the organic additives (accelerator, suppressor, and leveler), and by using reverse pulse electroplating techniques.

E. Daisy-Chain Measurements

After the fabrication is finalized, the resistance measurements are performed for the TSVs connected in daisy-chain pattern. The series resistance is measured by an HP4155B semiconductor parameter analyzer connected to Karl Suss PM8 manual probe station. In order to have a statistical distribution of the TSV resistance and to demonstrate the reliability of the process, row resistance from five different chip stacks (each stack is composed of two 50-μm-thick chips having 16 rows, 16 columns, thus 256 TSVs) is measured. Fig. 11 shows the row resistances (16 TSVs in series) including the interconnection resistance and off-chip cables. Among the 1280 TSVs measured, just 10 open-circuit defects are detected, resulting in more than 99% yield. Moreover, the average row resistance is calculated as 33.8 Ω with 3.3-Ω standard deviation. The total contribution of the interconnections is then subtracted from the measured value and the resistance of single TSV is calculated as 0.5 Ω (average) according to the following equation:

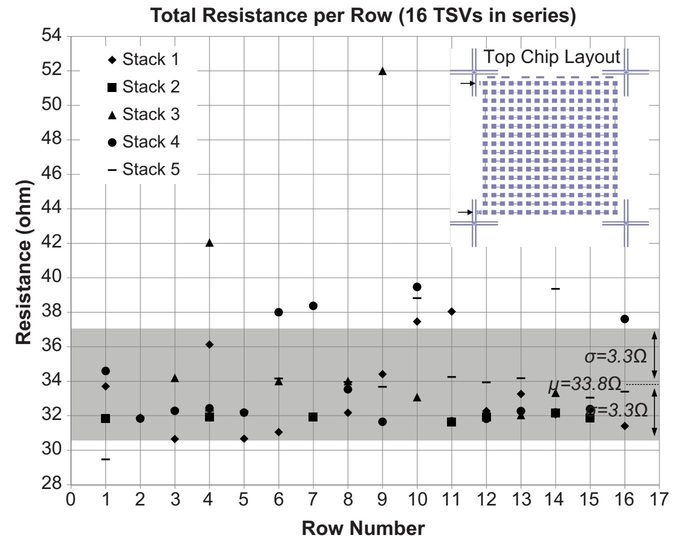
$$R_{\text{TSV}} = (R_{\text{measured}} - R_{\text{wiring}} \times (\#_{\text{TSV}} - 1))/(\#_{\text{TSV}}) \quad (1)$$

where R_{wiring} (interconnects) is calculated as 1.5 Ω and the total number of TSVs in the chain is symbolized as $\#_{\text{TSV}}$. Moreover, the chip is placed on a hotplate at 200 °C for 5 min and the resistance of the same rows are measured again. Fig. 11 gives the average resistance values before and after heat treatment, demonstrating no significant change.

III. CMOS Post-Processing and 3-D Integration

Having verified the reliability of the proposed fabrication process with the dummy Si chips, the method is tested on real CMOS chips. Here, a multiprocessor chip is used as the test vehicle. The platform is aimed to be composed of completely identical stacked dies connected by TSVs, where each die features four 32-bit embedded processors and associated memory modules. The chip is manufactured in a 10-metal UMC 90-nm process and measures 4×4 mm^2. The details of the processor architecture and the modular 3-D multiprocessor approach can be found in [4].

Prior to the post-processing, the dimensions of CMOS chips are measured. Fig. 12 shows the pad-to-edge distance along all directions, where the mean and standard deviation values are calculated as 37 and 1.1 μm, respectively. This result shows that mask and C2C alignment steps can be done with good precision based on the physical dimensions. First, 40-μm-diameter via openings are etched on 60 × 60 μm^2 CMOS pads on the top chip by using Al RIE (1.2 μm), dielectric RIE (10 μm), and Si DRIE (40 μm), respectively. It is verified



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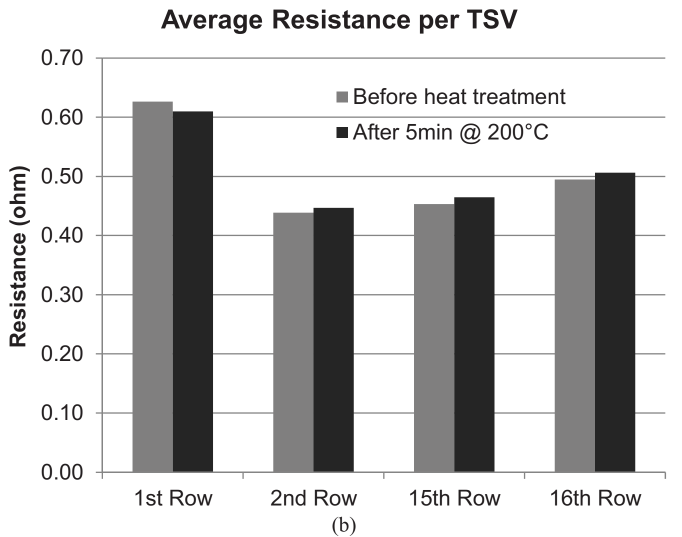

(b)

Fig. 11. (a) Resistance measurement results of five chip stacks fabricated through the same processing steps. (Inset: layout of the top chip showing 16 rows and 256 pads. Chain starts from top left corner and ends at bottom left corner). (b) Average TSV resistance extracted from first two and last two rows before and after heat treatment.

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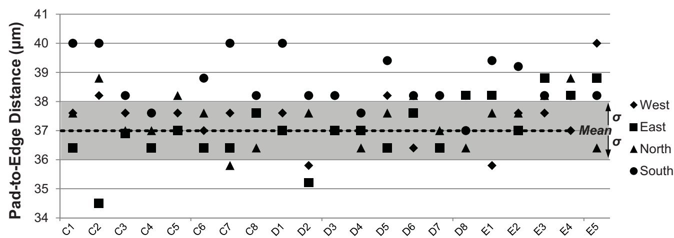
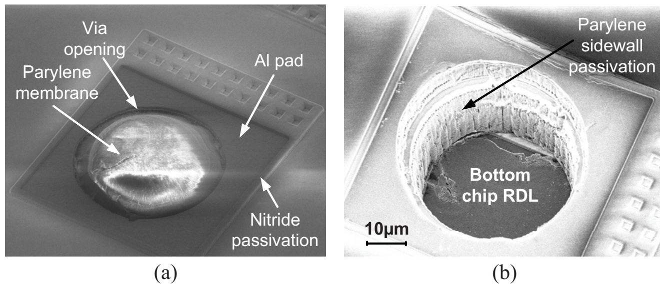


Fig. 12. Pad-to-edge distance along all directions for the chips manufactured in UMC 90-nm process. Mean and standard deviation values are calculated as 37 and 1.1 μm, respectively. [Each chip in the box is labeled with a letter and a number (C1, C2, C3, etc.), where the letters represent the rows and the numbers represent the columns.]



(a) (b)

Fig. 13. (a) SEM image of the CMOS pad after via etching and parylene passivation by frontside UV-tape protection. (b) SEM image of the via opening after bonding and parylene etching, showing the sidewall parylene passivation and the RDL layer on the bottom chip.

that 40-μm-thick dry-film is sufficient to survive till the end of all dry etching steps, especially the dielectric etching which has lower selectivity to the organic resists. To isolate the via sidewalls and the chip backside, 1-μm-thick parylene film is deposited, which will be used as the adhesive layer for bonding. Fig. 13 shows the parylene membrane after releasing the UV tape.

Since the two chips are targeted to be identical to reduce the nonrecurring engineering costs, the surface of the bottom chip is passivated and RDL is patterned to reroute the signal to the upper tier. After the parylene passivation and patterning steps by dry-film lithography, RDL is patterned by lift-off process using the dry film as the sacrificial layer. Alignment and bonding are done as explained for the dummy chips. Finally, parylene membrane on the top chip is etched by anisotropic O_2 plasma etching, as shown in Fig. 13. Fig. 14 shows the SEM images of the 50- and 280-μm-thick CMOS chips post-processed, aligned, and bonded in die level. Currently, the impact of individual steps to the CMOS performance is being tested by the test setup explained in [4].

IV. Conclusion

A C2C 3-D integration platform based on post-CMOS processing and dry-film lithography was presented. The proposed techniques were applied to diced and thinned Si chips emulating real CMOS chips. Although the technology was demonstrated at the die level, some of the process steps are compatible to wafer-level processing as well. After the via etching step, only one parylene deposition step was employed to passivate the via sidewalls and the chip backside, and

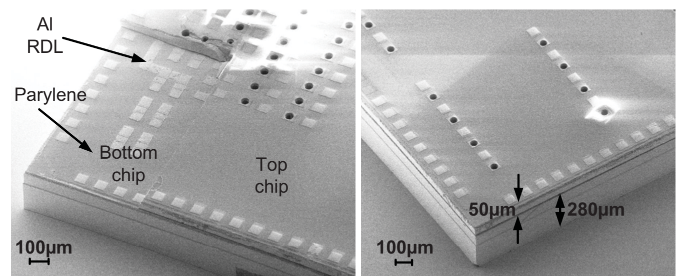


Fig. 14. SEM images of the bonded chips after anisotropic parylene etching. (An already broken chip is used as the top chip to inspect the alignment accuracy.)

to have an intermediate layer for adhesive bonding. Here, a method eliminating the requirement of dielectric patterning at the bottom of the via was also demonstrated. Two 50-μm-thick chips were successfully bonded, and then 60-μm-diameter TSVs with electroplated Cu metallization were fabricated. It is believed that the TSV aspect ratio can be increased by using metal-organic chemical vapor deposition instead of PVD for the seed layer deposition, and by an electroplating setup enabling high-aspect-ratio deposition. Daisy-chain measurements showed 0.5-Ω TSV resistance on average, with a yield of more than 99% for 1280 TSVs from five different chip stacks. Then, the techniques were successfully applied to CMOS microprocessor chips. The techniques described in this paper demonstrate that 3-D integration technology, which is considered to be a very challenging process, can be accomplished in a MEMS clean room without using any expensive tool specialized for this purpose. We believe that this chip-level post-processing technique can be used not only for chip stacking but also for applications where the CMOS layers have to be modified by surface or bulk micromachining, in case full CMOS wafer is not available or compatible, or very expensive for research purposes.

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