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# Design Techniques and Analysis of High-Resolution Neural Recording Systems Targeting Epilepsy Focus Localization

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***Abstract*— The design of a high-density neural recording system targeting epilepsy monitoring is presented. Circuit challenges and techniques are discussed to optimize the amplifier topology and the included OTA. A new platform supporting active recording devices targeting wireless and high-resolution focus localization in epilepsy diagnosis is also proposed. The post-layout simulation results of an amplifier dedicated to this application are presented. The amplifier is designed in a UMC 0.18µm CMOS technology, has an NEF of 2.19 and occupies a silicon area of 0.038 mm$^2$, while consuming 5.8 µW from a 1.8-V supply.**

## I. Introduction

Frequent seizures are typical manifestations of epilepsy [1]. Approximately 50 million people worldwide are diagnosed with epilepsy and more than 30% of them do not respond well to anticonvulsants. For many of these patients with intractable seizures, the ablative surgery may provide a favorable outcome [2]. In some cases, presurgical evaluation requires an invasive recording phase, consisting in implanting brain cortical or depth electrodes in order to determine the precise epileptic focus. Then, resection surgery can be performed in these areas. In such presurgical evaluation phase, multiple wires connect the electrodes to the amplifiers and recording equipment, leaving the patient bound to a bed with an open brain for several days until sufficient electrocorticographic (ECoG) information is recorded to accurately reveal their foci [3]. In addition to the complexity of the procedure, these standard electrodes have a large contact area and a relatively large spacing which can effectively average the activity of millions of neurons and cause significant loss of information in higher spatial resolutions of the cortical units. The development of an implantable system enabling continuous monitoring over long periods of several weeks with high spatial resolution microelectrodes appears to be a relevant goal for the next generation of such therapeutic electrodes.

Current solutions for high-density recording of epileptic activity either consist of spanning the cortical layers using linear array of multielectrodes penetrating the brain tissue [4] or implanting hybrid systems including standard macroelectrodes along with microwire arrays with bundles of wires connected to the electrodes [5]. Considering biocompatibility issues, none of these approaches are feasible for a long-term monitoring period prior to surgery.

A solution is proposed consisting of using highly flexible and thin substrates to create active electrode arrays combining a large number of electrodes with integrated circuits distributed over a relatively large area over the cortex (Fig. 1). By placing several recording systems over potentially epileptic parts of the cortex previously detected by standard non-invasive methods, sufficient information pertaining to the localization of the epileptic foci with high spatial resolution quality can be recorded. The long-term implantation is enabled by the presence of an RF chipset located in a burr hole in the skull for remote powering and wireless data transmission (Fig. 1). Recording with flat non-penetrating electrodes which is a main concern for the safety of patients enables the surgeon to perform a minimally invasive surgery.

This paper is organized as follows. Section II presents the system architecture and a comprehensive analysis of the different LNA topologies and OTA circuits. Section III presents the post-layout simulation results of the proposed architecture.

## II. System Overview

For decades, ablative surgery applied to the treatment of epilepsy has utilized intracranial EEG recorded over a narrow bandwidth (1–100Hz) from large (1–10mm diameter), widely spaced (5–10mm) electrodes placed on the surface of the cortex [6]. Recently, several groups of researchers have investigated the role of higher frequency signals in the generation of convulsions. Researchers in [7] have shown that high frequency oscillations in the ripple (80-250Hz) and fast ripple (250-1000Hz) frequency range may be signatures of an epileptogenic brain. Using hybrid electrodes, they have found that higher frequency signals are primarily generated by highly localized, sub-millimeter scale neuronal assemblies. Authors in [6] reported that seizure-like events which are not detectable using routine clinical macroelectrodes were observed on isolated microelectrodes. Recognizing the pertinence of high resolution recordings on

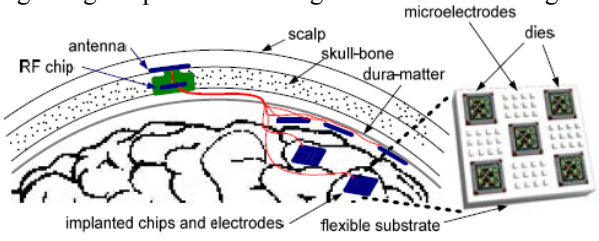


Figure 1. Schematic representation of the proposed distributed monitoring system.

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the surface of the brain, we develop low-noise amplifiers that operate in an intermediate range of frequency to record low as well as high frequency ripple and/or spiking signals which can be representatives of epilepsy.

### *A. Neural Amplifier Topology*

The low-noise amplifier (LNA) used for amplifying and filtering weak neural signals is a fundamental block in almost all integrated neural recording systems. In spite of its widespread use in medical sensing applications, the LNA is designed empirically. In the following, analytical expressions are presented and optimum solutions for different design parameters of LNA's are proposed.

The way in which the signals in the frequency range of interest should be amplified while rejecting the large random DC offsets generated at the electrode-tissue interface is a design criterion of major importance. For this purpose, closed-loop architectures are favored considering their superior linearity, gain stability, high PSRR and additional feedback advantages over open-loop topologies. The authors in [8] have made a comparative study of the noise, power and area of three distinct topologies (Fig. 2) and have shown that the conventional capacitive feedback topology (Fig. 2 (a)) performs better in terms of area and power consumption for a given input-referred noise. The gain of the second topology (Fig. 2 (b)) is defined by the open-loop gain of the first OTA ($A_1$). Consequently, the area overhead due to the input capacitors can be significantly reduced. The major drawback in addition to gain variation is the added noise of the second OTA ($A_2$). The third topology (Fig. 2 (c)) sets the gain by the product of two capacitor ratios which is expected to result in area reduction. The calculated NEF [8] shows the effect of the second OTA on the input-referred noise which requires a larger area compared to (a) to compensate the added noise. In addition, an attenuator in the feedback path and the potential related instability issues, as well as the need to insert a negative sign in the transfer function of the loop gain, are drawbacks of this topology. Consequently, the conventional topology (a) is considered the most efficient and reliable.

Careful consideration should be devoted to the selection of single or multi-stage amplification, as well as bandwidth requirements of different stages. Using an analysis similar to [9], it is possible to calculate the optimum gain of a single-stage topology to minimize the area of the amplifier for a given input-referred noise. It is assumed that the area is dominated by the input and load capacitors and the noise is limited to the thermal noise of the input pair of the OTA. The effect of flicker noise is discussed further.

The input-referred thermal noise PSD for a differential pair operating in subthreshold region is expressed as

$$\overline{v_{nI}^{\,2}} = 2\frac{4KT}{(2\kappa)g_m} = \frac{4KT}{\kappa g_m} \tag{1}$$

where $g_m$ is the transconductance of the input transistors, $\kappa$ is the subthreshold slope factor, $K$ is Boltzmann's constant and $T$ is the absolute temperature. Assuming the amplifier as a single-pole stage, the equivalent brick-wall bandwidth is [9]

$$\Delta f = \frac{\pi}{2} f_H = \frac{\pi}{2}\frac{1}{2\pi}\frac{g_m}{C_L A_M} = \frac{g_m}{4C_L A_M} \tag{2}$$

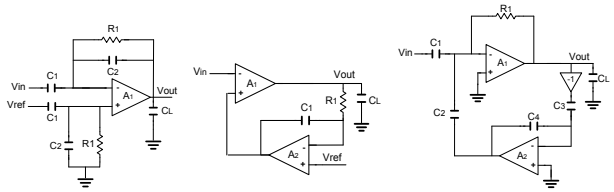


Figure 2. Three feedback-based LNA topologies.

$C_L$ is the load capacitor at the output and $A_M$ is the midband gain. The total input-referred rms noise is

$$v_{ni,rms} = \sqrt{v_{nI}^{\,2}\,\Delta f} = \sqrt{\frac{KT}{\kappa C_L A_M}} \tag{3}$$

The area of a single-stage LNA (Fig. 2(a)) is proportional to $2C_1 + 2C_2 + C_L$. Replacing $C_L$ from (3) and $C_1 = A_M C_2$ and optimizing with respect to $A_M$ yields

$$A_{M,opt} = \frac{1}{v_{ni,rms}}\sqrt{\frac{KT}{2\kappa C_2}} \tag{4}$$

To achieve a lower input-referred noise, a higher gain is needed to optimize the area of the amplifier.

Considering a second stage, as shown in Fig. 3, the optimization of the area depends on the bandwidth settings of the stages. If the high cut-off frequency is set by the first stage, the optimum gain of this stage can be found using (4), and replacing this value in (3) yields the sum of $C_{L1}$ and $C_{21}$ which together form the approximate loading capacitor at the output of the first stage. If a high overall gain is needed, a large capacitor at the input of the second stage and a small load capacitor in the first stage are mandatory. For a low input-referred noise, a high gain is required in the first stage and the advantage of two-stage over single-stage relates to a higher overall gain (more than 50 V/V or 100 V/V for typical values) that is achieved by properly dividing the optimal load capacitor between $C_{L1}$ and $C_{21}$. Hence, the common method consisting of dividing the gain in identical ratios between stages (e.g. 10×10×10) cannot be efficient, unless necessary attention is given to the bandwidth settings of the stages.

If the high cut-off frequency is set by the second stage, the total input-referred rms noise including the effect of second stage is

$$v_{ni,rms} = \sqrt{\frac{KT}{\kappa}\frac{g_{m2}}{C_{L2}A_{M2}}\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}A_{M1}^{\,2}}\right)} \tag{5}$$

and the area is proportional to

$$2C_2\left(1+A_{M1}\right) + C_{22}\left(1+A_{M2}\right) + C_{L1} + C_{L2} \tag{6}$$

Neglecting the small $C_{L1}$ due to the relaxed BW in the first

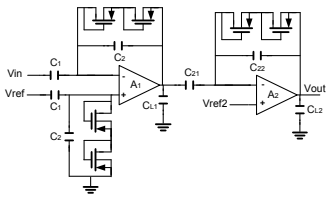


Figure 3. Two-stage capacitive feedback topology.

stage and replacing $C_{L2}$ from (5) into (6), and optimizing with respect to $A_{M1}$ and $A_{M2}$ results in the optimum values of gains. As a practical case, for a unique value of 200fF of feedback capacitors, an input referred noise of $1.18\mu V_{rms}$ requires an optimum gain of 100V/V for one stage, to minimize the area. A large value of 40.4pF as the sum of input and feedback capacitors and another 40pF as the load capacitor for limiting the bandwidth are needed.

Considering the two-stage topology with high cut-off frequency set by the first stage the optimization results in the same gain and input capacitors for the first stage and 40pF as the sum of $C_{L1}$ and $C_{21}$. A higher gain (than 100V/V) can be achieved but the total capacitor is large. For the third case in which $f_H$ is set by the second stage and having a typical value of $g_{m2}/g_{m1}$ equal to 0.05, $A_{M1,opt}$ and $A_{M2,opt}$ are 10 and 20, respectively. The overall gain is 200 and the total capacitance including the input and load is 12.6pF. For smaller ratios of $g_{m2}/g_{m1}$, the required gain of the first stage is set larger to suppress the additional noise of the second stage. This method can be extended for topologies with more than two stages and the stage which sets the high cut-off frequency requires a relatively large gain to suppress the total input-referred noise. As mentioned in [10] and analytically demonstrated in this Section, the two-stage topology achieves a better performance under the condition that $f_H$ is set by the second stage. The optimal distribution of the gain between the stages and the value of the input capacitors and its relation to the area also depend on the flicker noise which is discussed further.

### B. Optimized OTA

The OTA is a critical block irrespective of the LNA's implementation topology. Large input transistors, source degeneration resistors [11, 12], improved effective transconductance [12] and severe current scaling in the non-input branches [11] are the main approaches used to achieve noise reduction. Among commonly used topologies, the telescopic cascode offers the best noise-power trade-off due to the smaller number of current branches and transistors contributing to the overall noise [13]. Biasing the transistors in weak and moderate inversion rather than strong inversion results in relaxed headroom requirements and provides sufficient swing at the output of the telescopic amplifier. In order to further suppress the noise of a telescopic cascode topology, degeneration resistors are used which results in a significant reduction of thermal as well as flicker noise (Fig. 4 (a)). The total current noise at the output node in Fig. 4(b) is expressed as

$$\overline{I_{n,out}^2} = \frac{4KT\gamma g_{m2} + \frac{K_F}{(WL)_2 C_{ox}} \frac{1}{f} g_{m2}^2 + 4KTR g_{m2}^2}{(1 + g_{m2}R)^2} \tag{7}$$

The second term is due to the flicker noise of $M_2$. The above equation is maximum for $R = 0$ and becomes close to zero for larger values of $R$. A large $R$ occupies a large area, limits the voltage swing and affects the biasing points of the transistors. In a source-degenerated folded-cascode topology (Fig. 4(c)), a large $g_{m7,8}R_{1,2}$ and a large $r_{o7,8}$ are mandatory to drive the largest proportion of current to the output and prevent $G_{m,eff}$ reduction. This results in large $W$ and $L$ values in the bottom transistors, which summed up to the large area of the resistors

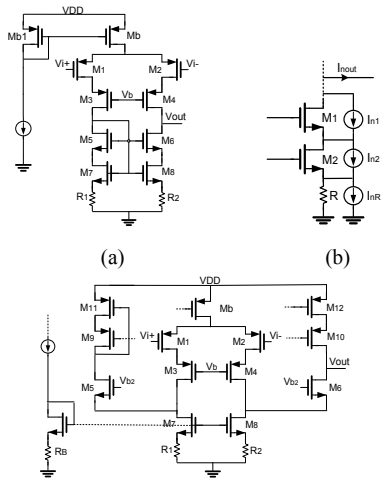


Figure 4. a) Proposed OTA. b) Noise model of the degenerated branch. c) Source degenerated folded cascode OTA [11].

and the larger resistor in the biasing branch [11] results in limited area efficiency. In a telescopic topology, $G_{m,eff}$ degradation is not an issue and careful consideration should be devoted to the size and operation regimes of the bottom transistors. A moderate resistance value of 210K has been chosen to optimize the performance in terms of operation regimes of the transistors, dc gain, area and input-referred noise. The p-implanted poly resistors are used with 10 matched units in each branch which are laid out in parallel and connected in series.

### C. Flicker Noise Effect

Depending on the size of the input differential pair, flicker noise participates in the total input/output noise of the amplifier. Increasing the size of the input transistors to suppress *1/f* noise is accompanied by producing a large parasitic capacitance which results in a larger level of noise transferred to the input of the amplifier. Hence, an optimum size of the input transistors should be derived that provides better noise performance. Assuming that *1/f* noise is dominated by the input transistors, and modeling the parasitic capacitance as shown in Fig. 5(a), the total input referred noise PSD is expressed as

$$v_{nI}^2 = \left(\frac{C_1 + C_P}{C_1}\right)^2 \left[\frac{2K_{fP}}{WLC_{ox}f} + \frac{4KT}{\kappa g_m}\right] \tag{8}$$

The effective parasitic capacitance at the gate of PMOS input transistors in weak inversion (WI) is the sum of $C_{GS}$, $C_{GB}$, and the Miller factor of $C_{GD}$ and is equal to

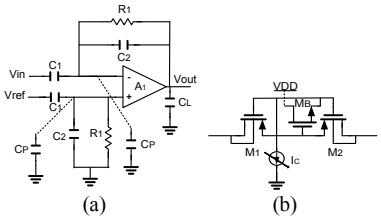


Figure 5. a) Capacitive feedback-based LNA with parasitic capacitors. b) Tunable symmetric resistor.

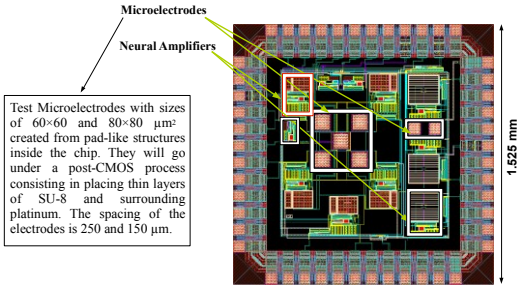


Figure 6. Layout of the neural amplifiers and microelectrodes.

$$C_P \approx WL_{ov}C_{ox} + \left(1 - \frac{1}{n}\right)WLC_{ox} + WL_{ov}C_{ox}(1 + A_v) \qquad (9)$$

$L_{ov}$ is the overlap length and $C_{ox}$ is the oxide capacitance. Replacing (9) as $C_{P0} + \alpha(WL)$ into (8) and minimizing the flicker noise component with respect to $WL$ results in

$$(WL)_{opt,f} = \frac{C_1 + C_{P0}}{\alpha} \qquad (10)$$

which yields

$$v_{nI,opt,f}^{\ 2} \approx \left[\frac{8K_{fP}\alpha}{C_{ox}C_1 f}\right] \qquad (11)$$

A larger input capacitance and closed-loop gain results in a larger optimum size of the input transistors but the corresponding noise level is smaller. Nevertheless, over-increasing the size of the transistors beyond the optimum value requires a larger input capacitance to compensate the increased noise level leading to a suboptimal area usage. In the designed OTA, the optimum point considering both thermal and flicker noise occurs at WL ≈ 250µm² and a size of 500µm/0.5µm of the differential input pair is chosen.

### D. Tunable Resistor

A controlled high-value and low-area resistor is needed to set and tune the low cut-off frequency. Resistors based on [14] are used (Fig. 5(b)). $M_1$ and $M_2$ implement high value resistances and $M_B$ provides the source-gate voltage used to tune $M_1$ and $M_2$ through the bias current ($I_C$). Using these resistors the low cut-off frequency is tuned within a range of 34Hz to 160Hz with a $W/L$ of 250nm/500nm of the transistors $M_1$ and $M_2$.

## III. Simulation Results

Following the above analysis, two prototypes of neural amplifiers are designed and implemented in one and two stages for the amplification of neural signals recorded on the surface of the cortex (Fig. 6). Fig. 7 shows the simulated frequency response of the two-stage high-gain and single-stage tunable-BW amplifiers. The midband gain of the two-stage topology is realized by the product of two capacitive ratios of 20 and 11. The high cut-off frequency is limited in the second stage. The total input-referred noise of this amplifier integrated in the frequency range of 1Hz to100kHz is 1.77$\mu V_{rms}$, thanks to its low-noise OTA and appropriate gain ratios. The noise is computed by dividing the output noise by the midband gain and integrating within the desired frequency range. Table I presents a summary of the results and a comparison with published works.

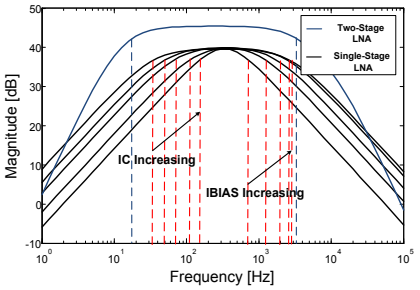


Figure 7. Simulated frequency response of the amplifiers.

TABLE I. Post-Layout Simulation Results

| Parameter | LNA Simulation Results and Comparision | | | | |
|---|---|---|---|---|---|
| | This Work | | [12] | [11] | [13] |
| | 2-Stage | 1-Stage | | | |
| Technology (µm CMOS) | 0.18 | 0.18 | 0.6 | 0.5 | 0.18 |
| Supply Voltage (V) | 1.8 | 1.8 | 2.8 | 2.8 | 1.8 |
| Supply Current (µA) | 3.22 | 2.84 | 0.845 | 2.7 | 4.4 |
| Gain (dB) | 45.2 | 39.9 | 39.4 | 40.8 | 39.4 |
| $f_L$ (Hz) | 18 | 30-160 Tunable | 0.36 | 45 | 10 |
| $f_H$ (kHz) | 3.3 | 0.7-2.5 Tunable | 1.3 | 5.3 | 7.2 |
| Input-Referred Noise ($\mu V_{rms}$) | 1.77 | 1.30 | 3.07 | 3.06 | 3.5 |
| NEF | 2.19 | 1.94 | 3.09 | 2.67 | 3.35 |
| Area (mm²) | 0.038 | 0.048 | 0.13 | 0.16 | 0.062 |
| CMRR (dB) | 89 | 78 | 66 | 66 | 70.1 |
| PSRR (dB) | 44 | 57 | 80 | 75 | 63.8 |

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