Swiss Federal Institute of Technology, Lausanne
Microelectronic Systems Laboratory

Lausanne, August 15, 2008

University of California, Merced
School of Engineering

Design of a 12-bit low-power SAR A/D Converter for a Neurochip

Master's Thesis

Pascal Meinerzhagen, EPFL

Supervisors

Neil Joye, EPFL
Yusuf Leblebici, EPFL
Sangho Shin, UC Merced
Shin-Il Lim, SeoKyeong University

Acknowledgements

My Master's Thesis would not have been possible without the support of many individuals. Neil Joye provided this ADC design as part of his PhD Thesis, guided me throughout the whole project, and read parts of my manuscript. While visiting the Chancellor's Group at UC Merced, Alexandre Schmid helped to organize my stay in California, and supported me in other administrative issues. Alain Vachoux suggested excellent ways to set up an environment for mixed-mode simulation, and provided parts of his lecture material for my consideration. Yusuf Leblebici gave me the unique opportunity to carry out my Master's Thesis in his laboratory, and made my stay at UC Merced, California, possible. I thank all of them.

Jae Jin Jung supported me throughout my time at UC Merced; he helped to fix problems related to Cadence, suggested the reading of many cutting-edge papers, gave hints on my design and revised parts of it. Yong Sin Kim supported me in setting up a working environment when I arrived to California, and generously provided resources from UCSC. In numerous discussions, Sangho Shin helped organize my design on system level, and confirmed many theoretical developments. Shin Il Lim guided me through the entire design process, and reviewed parts of my manuscript. All the group members gave me the chance to discuss technical issues for hours and hours. They contributed a lot of their time to my project, and gave me a lot of helpful advice. Steve Kang accepted me as a visiting researcher in his group at UC Merced. I thank all of them.

Vivianne Greenwood revised chapters 1 to 4 of my manuscript. I thank her.

Abstract

Cutting-edge CMOS neurochips, which consist of a Microelectrode Array (MEA) manufactured on top of CMOS circuitry, allow the recording of the electrical activity of neural networks *in-vitro*, and their stimulation. As CMOS technology continues to scale down, signal processing is favorably done in the digital domain, which requires Analog-to-Digital Converters (ADCs) to be integrated on-chip. To relax the requirements on the neurochip's surface temperature control system, a low-power ADC is targeted[1]. Among various ADC architectures, the Switched-Capacitor (SC) or Charge-Redistribution Successive Approximation Register (SAR) ADC is best suited for low power and 12-bit resolution. To avoid common-mode errors, the SC SAR ADC uses a differential topology. To decrease area, power, and cost while maintaining 12-bit accuracy, the Binary-Weighted (BW) capacitor array is split into three sub-BW capacitor arrays connected through two series capacitors. A comparator with three preamplifier stages and a latch discriminates voltage differences as small as $200\mu V$ while concurrently working with rail-to-rail input signals. The SAR control logic uses only four DFFs for the finite state machine, whereas a classical SAR implementation with shift-registers would use 12 DFFs. Furthermore, a shared register bank contains the output codes and memorizes the position of switches. The SAR ADC will be manufactured in UMC $0.18\mu m$ CMOS technology.

Key words

Microelectrode Array (MEA), Neurochip, Switched-Capacitor (SC) Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC), Binary-Weighted (BW) Capacitor Array, Split Capacitor Array

[1] While carrying out electrophysiological experiments, it is essential to accurately control the surface temperature of the neurochip. In most experiments, the temperature is controlled to 37°C.

Table of Contents

Table of Figures

Table of Tables

1. Introduction

1.1. The use of MEAs in Neuroscience

Microelectrode Arrays (MEAs) have become an essential tool in both fundamental and applied neuroscience research. They enable the transition from the study of single neurons to the study of populations of neural cells. Why is it essential to study the electrical activity of neural networks? The following motivations are key:

- Building hybrid systems, containing a biological and an electronic part. Neuronal networks have the ability to learn, what distinguishes them from electronic circuits, which themselves are well suited for computation. Thus, hybrid systems are augmented with the ability to learn, when compared to conventional electronic systems. An example of a hybrid system is the Hybrot (hybrid robot) presented in [Potter2007].
- Studying the electrical behavior of neural networks is fundamental to understanding the brain's functions in normative states (e.g. learning [Marom2002]) and disorders (e.g. epilepsy [Aziz2006]).
- Studying the propagation of electrophysiological signals can help to better understand and eventually cure diseases like Parkinson's disease and Alzheimer's disease.
- Screening of pharmacological effects of compounds is used for drug development and drug discovery [Stett2003], [Marom2002], [Heer2005].

Commercially available MEAs have the following characteristics [Jimbo2003], [Egert1998]:

- 60 – 120 electrodes
- Electrode diameter of 10 – 30 μm
- Pitch (distance between electrodes) of several hundreds of μm
- No on-chip processing (passive MEAs)

The dimensions of commercially available MEAs are larger than the typical size of vertebrate neurons ($10 \mu m$) used in conventional electrophysiological experiments. Figure 1-1 shows an example of a typical neural network. The limited spatial resolution of commercially available MEAs leads to spatial under-sampling.

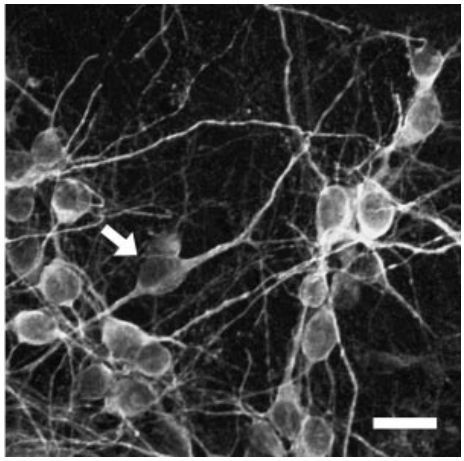


Figure 1-1 Typical neural network. The size of each soma[1] is roughly $10\mu m$. The arrow marks a soma. Scale bar, $20\mu m$ [Wagenaar2005]

In response to spatial under-sampling, a new generation of silicon-based high-density MEAs has been proposed [Eversmann2003], [Frey2007], [Imfeld2008]. These new devices have an electrode diameter of $4.5\mu m$ and a pitch of $7.8\mu m$ [Eversmann2003]. Therefore, they enable electrophysiological experiments at sub-cellular resolution. These CMOS-based devices have additional advantages for managing a large number of electrodes: signal multiplexing, amplification, A/D conversion and filtering are done on-chip, eventually right beneath the MEA. Figure 1-2 shows the conceptual cross-section of a CMOS-based MEA.

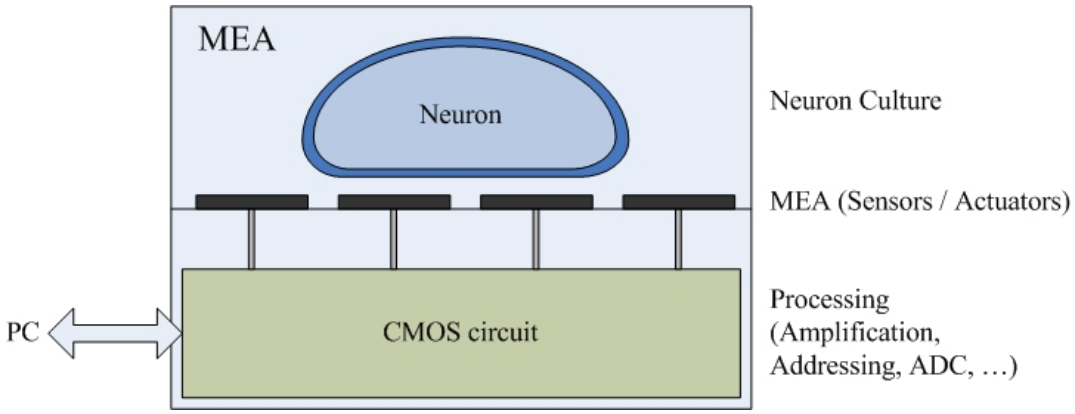


Figure 1-2 Conceptual cross-section of a CMOS-based MEA

1.2. What is a Neurochip?

A neurochip is a complete data acquisition and processing system that aims at observing and understanding the electrical activity of neural networks. It can be augmented with the ability to stimulate neural networks, rather than just recording their electrical activity.

Cutting-edge neurochips consist of MEAs manufactured in post-CMOS processing steps on top of a CMOS chip. Neural cells cultures are grown on top of the MEA. See Figure 1-3 for an example. Most electrophysiological experiments are carried out *in-vitro*, some already *in-vivo*. During electrophysiological experiments, the neurochip acquires, amplifies, converts and processes signals

[1] The soma is the bulb-shaped end of a neuron, containing the cell nucleus.

coming from the neural network and eventually stimulates neurons. Figure 1-4 shows a micrograph of a neurochip.

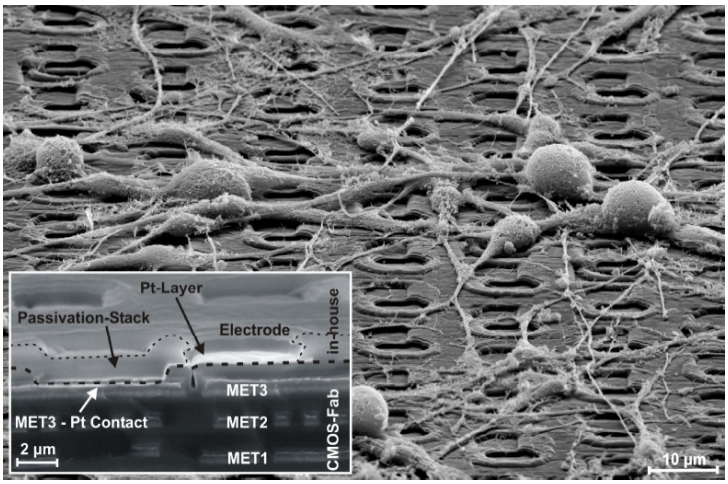


Figure 1-3 SEM image of a MEA with a culture of neurons grown on top of it. The size of a soma is roughly $10\mu m$. The chip was fabricated in an industrial $0.6\mu m$ 3M2P CMOS-process, the electrodes are fabricated in-house using post-CMOS steps [Frey2007]

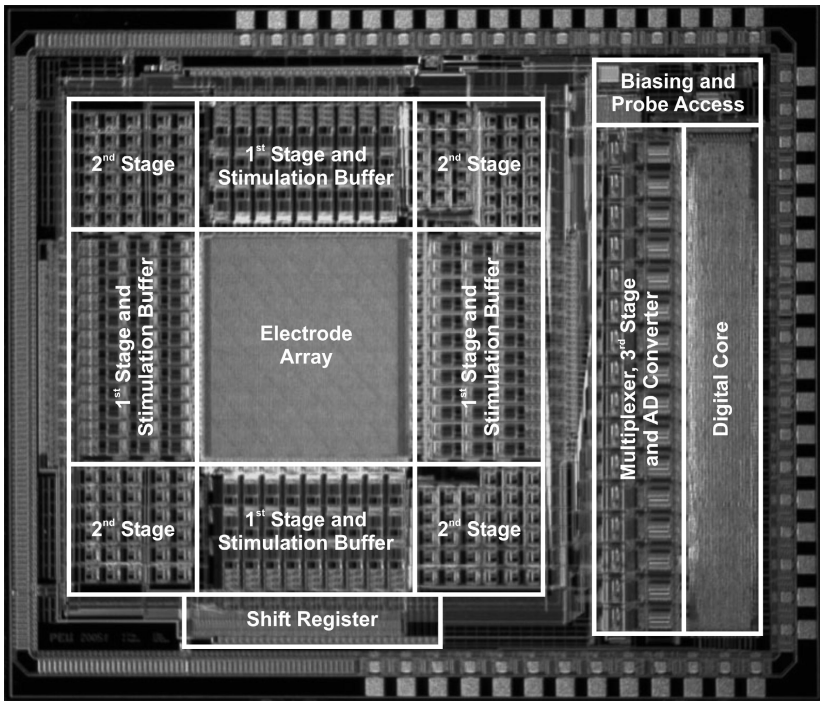


Figure 1-4 Neurochip micrograph [Frey2007]

Weak analog signals will appear at the electrodes in response to electrical activities in the neural network. As signal processing is done preferentially in the digital domain, data converters are integrated on-chip. In fact, for monitoring and recording the electrical activity of neural networks, analog-to-digital converters, also referred to as A/D converter or ADC in the literature, are used. For stimulation of neurons, digital-to-analog converters, also referred to as D/A converter or DAC, are used.

1.3. Neurochips developed in LSM

The goal of Neil Joye[1] is to manufacture very high-density MEAs with on-chip CMOS processing for recording and stimulating the electrical activity of populations of neurons. As for recording, the small Signal-to-Noise Ratio (SNR), resulting from small extracellular voltages, constitutes a main challenge. The extracellular voltage which can be sensed is 2 to 3 orders of magnitude smaller than the intracellular voltage [Joye2008-2]. In fact, the intracellular voltage or *action potential* is about $100mV_{pp}$, while the extracellular voltage ranges from $100\mu V_{pp}$ to $5mV_{pp}$ [Eversmann2003]. Figure 1-5 shows the intracellular and extracellular voltages measured from a snail neuron. The exact value of the extracellular voltage depends on many factors (type of neuron, adhesion to chip, resistivity of bath solution, etc.) and may change over time.

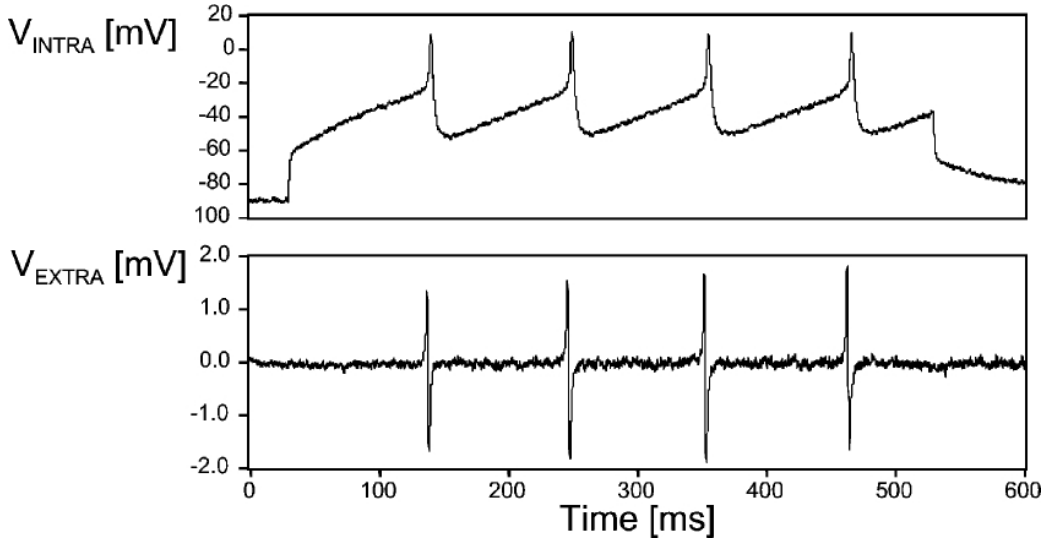


Figure 1-5 Measured data from a snail neuron. (Top trace) intracellular voltage and (bottom trace) extracellular voltage [Eversmann2003]

Passive MEAs with three-dimensional tip electrodes and a pitch of $5-6\mu m$ have been manufactured [Joye2008] (See Figure 1-6). *In-vitro* electrical measurements and electrophysiological experiments using standard planar electrodes and the newly developed three-dimensional electrodes are currently carried out. The results are expected to confirm the superiority of the three-dimensional MEAs in terms of electrical coupling with respect to planar electrodes.

[1] Neil Joye is with the Microelectronic Laboratory (LSM), Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland

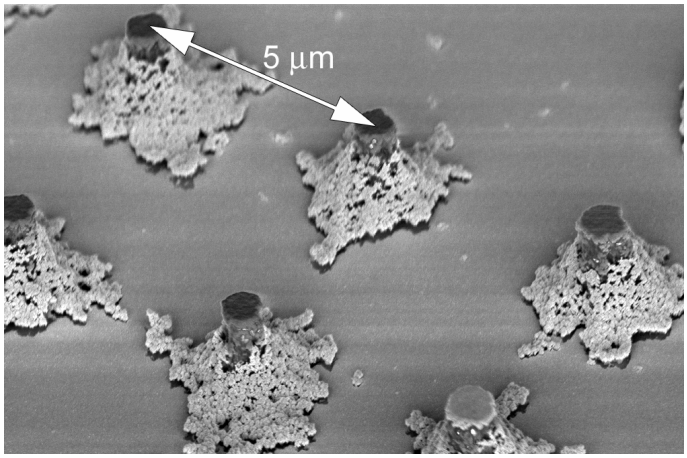


Figure 1-6 SEM micrograph of a three-dimensional tip electrode array with a pitch of $5\mu m$ [Joye2008]

Neurochips containing three-dimensional MEAs connected to CMOS circuitry are currently being developed. Any of these following techniques could be used when connecting MEAs and CMOS circuitry.

- Wire bonding
- Through-silicon vias [Watanabe2006]
- CMOS post-processing [Hafizovic2006], [Frey2007]

CMOS circuits will perform signal amplification, multiplexing, A/D and D/A conversion, filtering and digital signal processing such as spike counting.

1.4. Summary

In *Chapter 2 Specifications*, the specifications of the 12-bit ADC are elaborated, taking into account neighboring blocks on the neurochip and typical electrophysiological quantities. *Chapter 3 ADC Architectures* lists and briefly explains all ADC architectures proposed to date and shows that the Switched-Capacitor SAR-type ADC best meets the specifications. *Chapter 4 Topology of the SC SAR* ADC describes the full data conversion system, including input multiplexing and output code storage and points out the core of the ADC, which performs the actual A/D conversion. *Chapters 5 Comparator, 6 Split capacitor array, 7 SAR control logic, 8 Switches* and *9 Delay elements* describe in detail the design of the various building blocks of the ADC core. In *Chapter 10 Validation of the ADC core* transient simulation results of the entire ADC core, validating its correct operation, are presented; additionally, DFT analysis results are shown, which allow to determine the SFDR, SNDR and ENOB of the ADC core. *Chapter 11 Conclusion* summarizes the achievements of the presented work, explains future work and gives various ideas to further improve the presented design.

2. Specifications

2.1. Organization of the Neurochip

There are two kinds of A/D converters integrated on-chip. First, there are low-resolution (8-bit) ADCs for continuous monitoring of the entire *100x100* MEA. Second, there are high-resolution (12-bit) ADCs to convert a sub-array of *7x7* electrodes, shown in red color on Figure 2-1. The high-resolution ADCs are switched on to perform high-accuracy data conversion as soon as activities in a specific area of the MEA are observed by means of the low-resolution ADCs. The *7x7* sub-array can be selected from anywhere within the *100x100* array; multiplexors will route the 49 selected channels to the 12-bit ADCs.

As discussed in *Section 1.3*, extracellular voltages are very small. Signals sensed at the electrodes are amplified before being routed to the ADCs. As the exact value of the signals depends on many factors and may change over time, the gain of the amplification stage needs to be adaptable in order to always use the full analog input range of the 12-bit ADCs. The amplification stage will be designed with gains ranging from *60dB* to *80dB* and must have a very good noise performance. The low-noise amplifiers must not introduce noise higher than $0.5V_{LSB}$ of the 12-bit ADCs.

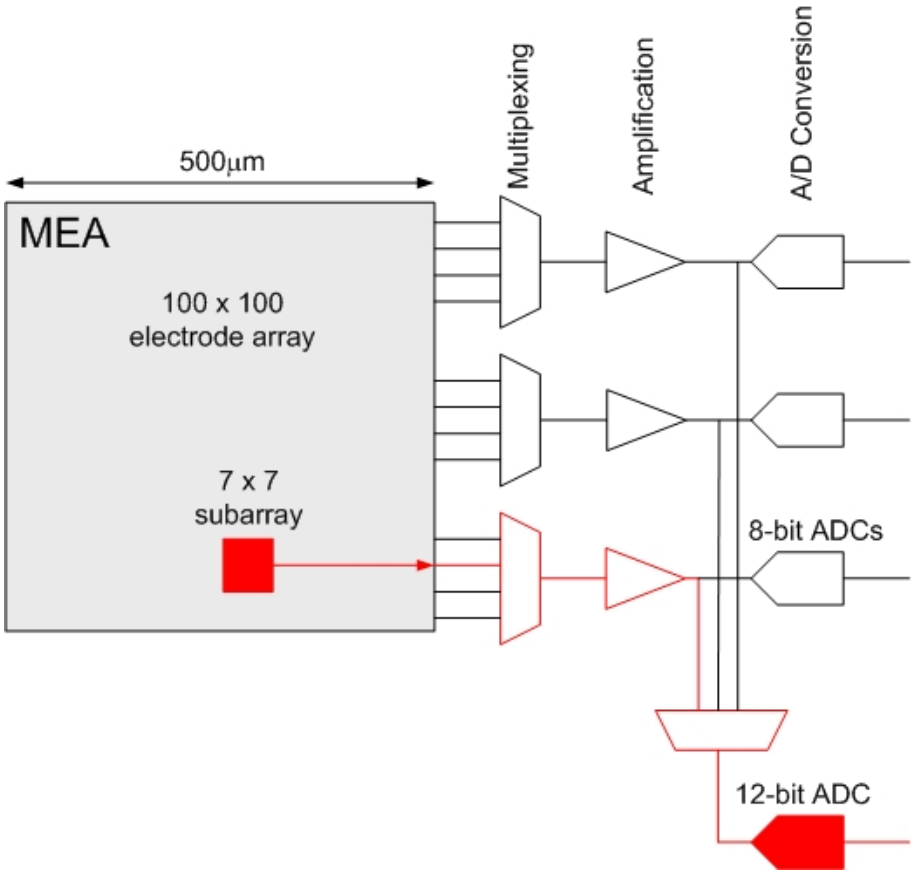


Figure 2-1 The entire MEA contains 100x100 electrodes with a pitch of $5\mu m$. The side length of the square MEA is thus $500\mu m$. A sub-array of 7x7 electrodes, variable in space, is routed to the 49-channel 12-bit ADC.

2.2. Elaboration of specifications

For accurate, high-quality signal conversion, we require a resolution of 12 bits.

The 12-bit ADC must convert an array of *7x7=49* electrodes. Choosing an array of *7x7* electrodes, which consumes an area of $35x35\mu m^2$, we make sure to simultaneously record the electrical activity of an entire soma with several electrodes.

Each electrode or channel needs to be converted at a rate of $40kSPS$. The spectrum of electrophysiological signals is limited to $B = 10kHz$. The corresponding Nyquist frequency is $f_{Nyquist} = 2B = 20kHz$. By choosing $40kHz$ per channel, oversampling with an oversampling factor of *2* is performed. Choosing $40kHz$ rather than the minimum $20kHz$ brings the following advantages:

- The requirements for the anti-aliasing filter are relaxed, easing its design
- Performing oversampling reduces noise

The analog input range of the 12-bit ADC is [*-900mV*, *900mV*]. Assuming an amplifier gain of *9'000* (*79.085dB*) and a $200\mu V_{pp}$ signal, the full analog input range is used.

The ADC will work on voltage signals, and neither on current, nor on charge signals.

The ADC takes differential signals. As the amplification stage will have a single-ended output, a single-ended to differential converter needs to be inserted right before the 12-bit ADC.

No specific representation is required for the output codes. It could be any of binary offset, sign magnitude, 1's complement or 2's complement. If the subsequent digital signal processing units (spike counting, etc.) require a specific representation, an encoder can be introduced. For SAR ADCs, sign magnitude is a convenient output code representation.

In order to convert 49 channels, parallelism could be used. The more ADCs operating in parallel, the smaller the conversion frequency of each ADC. Eq. (2-1) shows how parallelism reduces the conversion frequency.

$$f_{conv} = \frac{N_e}{N_{ADC}} \cdot f_{sample} \tag{0-1}$$

where $N_e = 49$ is the number of electrodes, N_{ADC} the number of ADCs operated in parallel, $f_{sample} = 40kHz$ the sampling frequency and f_{conv} the conversion frequency of the ADC(s). The product $N_e f_{sample}$ is constant and equal to *1.96MHz* if *49* channels are converted. If $N_{ADC} = 1$, we get from Eq. (0-1) $f_{conv} = 1.96MHz$. If a single A/D conversion takes 14 clock cycles, the internal clock frequency becomes $f_{clk} = 14 \cdot 1.96MHz = 27.44MHz$, what is easy to deal with, as pointed out in following chapters.

The ADC should have a width equal to (or smaller than) $500\mu m$, as it will be placed next to the MEA. In fact, the square *100x100* MEA with a pitch of $5\mu m$ has a side length of $500\mu m$. The length of the ADC is not specified. It could be $500\mu m$ or $1mm$.

The maximum power consumption is not specified. However, remember that the electrical activity of populations of neurons depends strongly on the temperature. During electrophysiological experiments, the surface of the neurochip should remain at a constant temperature, 37°C in most cases. A surface

temperature control system will be integrated on the chip. In order to relax the requirements of the surface temperature control system, a low-power ADC must be designed. Low power consumption will become even more important when switching from *in-vitro* to *in-vivo* electrophysiological experiments, as most implantable chips are battery-powered and excessively high temperatures would damage living tissues.

The ADC must have a Differential Non-Linearity smaller than 1 ($DNL < 1$) and an Integral Non-Linearity smaller than 1.5 ($INL < 1.5$).

Table 2-1 summarizes the elaborated specifications for the 12-bit ADC.

Resolution	12 bits
Number of channels	49
Sampling rate	40kSPS per channel
Analog input range	[-900mV, 900mV]
Signals	Voltage Differential
Output code representation	Sign magnitude
Parallelism	No, $N_{ADC} = 1$
Width	$\leq 500\mu$
Length	Not specified
Power consumption	As small as possible. The surface temperature should stay at 37°C
DNL	$< 1V_{LSB}$
INL	$< 1.5V_{LSB}$

Table 2-1 Specifications of the 12-bit ADC

3. ADC Architectures

3.1. ADC Architectures in comparison

A large variety of ADC architectures have been proposed to this day. They can be classified as follows [Kester2005-1]. (Architectures shown in gray cannot be implemented as CMOS integrated circuits; they are here to complete the list.)

- Comparator (1-bit ADC)
- High Speed ADC Architectures
  - **Flash** Converters (sometimes called parallel ADCs)
  - **Successive Approximation** ADCs
  - Subranging, Error Corrected, and **Pipelined** ADCs
  - Serial Bit-Per-Stage Binary and Gray Coded (**Folding**) ADCs
- **Counting** and Integrating ADC Architectures
  - Charge Run-Down ADC
  - Ramp Run-Up ADC
  - Tracking ADC
  - Voltage-to-Frequency Converters (VFCs) combined with Frequency Counter
  - Dual Slope/Multislope ADCs
  - Optical Converters
  - Resolver-to-Digital Converters (RDCs) and Synchros
- **Sigma-Delta** ADC

Figure 3-1 compares integrated circuit ADC architectures in terms of resolution and bandwidth. The attentive reader will see which resolution and frequency range are attainable with each of the architectures.

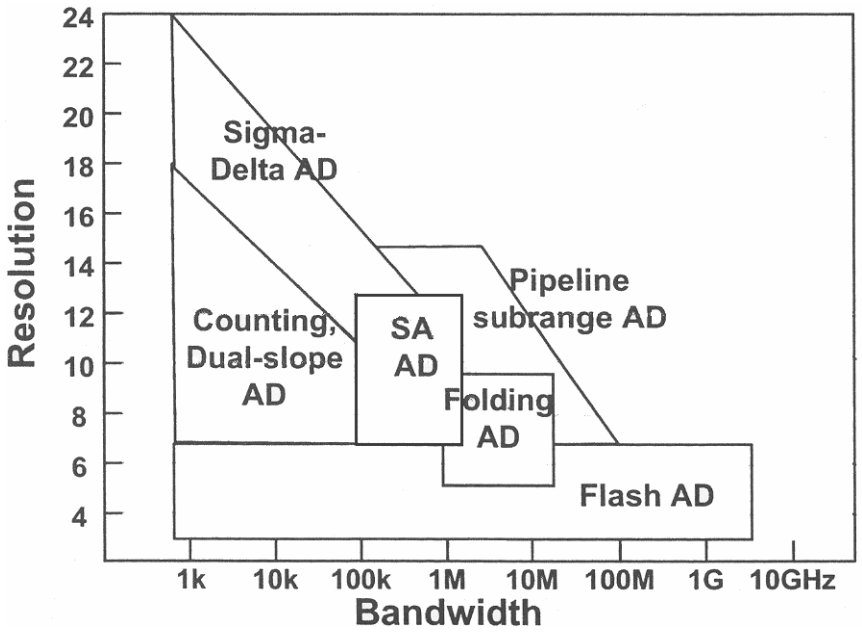


Figure 3-1 ADC architectures in comparison [Pelgrom2007]

The following paragraphs discuss briefly the various ADC architectures and their compatibility with the specifications elaborated in *Chapter 2*.

Flash ADC

Flash ADCs (sometimes called parallel ADCs) are the fastest type of ADC, but have limited resolution, high power dissipation and relatively large chip size.

Successive Approximation ADC

"The successive approximation ADC is by far the most popular architecture for data-acquisition applications, especially when multiple channels require input multiplexing. […] The overall accuracy and linearity of the SAR ADC are determined primarily by the internal DAC's characteristics. […] *Switched-capacitor (or charge-redistribution) DACs* have become popular in newer CMOS-based SAR ADCs, as their accuracy and linearity are primarily determined by high-accuracy photolithography." [Kester2005-2].

As SAR ADCs do not have latency, they outperform Pipelined and Sigma-Delta ADCs in the case of single-shot measurements or repeated ADC power-up and -down cycles. Remember that the 8-bits ADCs are available for continuous monitoring of the entire MEA, while the 12-bit ADC is powered up for high-accuracy data conversion as soon as activities are observed in a specific area, then powered down again.

The challenge is to build a capacitor array that is at least 12-bit accurate, which should be possible in UMC $0.18\mu m$ CMOS technology, as a 12-bit accurate capacitor array has already been realized in a $0.6\mu m$ CMOS process, using a special common centroid layout technique [Promitzer2001]. If 12-bit accuracy is not achieved, calibration in the digital or analog domain can be performed. However, the aim is to build a non-calibrating ADC, as calibration would add a lot of extra circuitry, including a memory. Consequently, the ADC would consume much more area. Calibration would also introduce a delay at each ADC start-up.

Subranging ADC

Subranging ADCs split the A/D conversion in several steps. For example, an N-bit conversion could be split into a coarse N1-bit conversion and a fine N2-bit conversion, where N1+N2=N. Each sub-conversion is carried out in a separate *stage*. Each stage will work on the residue signal (error signal) of the previous stage. Residue signals are amplified to match the input range of the next stage. Subranging ADCs always include operational amplifiers.

Subranging ADCs can be pipelined. In a pipelined subranging ADC, all stages work simultaneously on different samples.

A stage can be repeated in time instead of space. In a cyclic/algorithmic/recirculating ADC, the residue signal is amplified and fed back to the same stage several times.

Pipelined ADC

Pipelined ADCs are used for high-frequency applications. The critical delay time of each stage diminishes, as it performs only a part of the conversion, which allows increasing the frequency. However, to convert a sample, its residue signal needs to propagate through the whole line of stages, which introduces the famous pipeline delay or latency. Due to latency, the pipelined ADC architecture is not appropriate for single-shot operation or repeated ADC start-up and shut-down cycles. However, a pipelined ADC is well suited for continuous data conversion.

Cyclic/Algorithmic /Recirculating ADC

Different authors use different terminology to refer to the same idea: the residue signal is recirculated several times through a single stage. Rudy van de Plassche refers to it as Cyclic or Algorithmic [Plassche2003], while Walt Kester refers to it as Recirculating [Kester2005-1]. This architecture can be adopted to achieve small area in applications where speed is not critical. Cyclic ADCs necessitate an operational amplifier.

Folding ADC

Folding ADCs have limited resolution, in general lower than 10 bits [Pelgrom2007].

Counting and Integrating ADC

Counting-based ADCs are ideal for high-resolution low-frequency applications, especially when combined with integrating techniques. According to [Pelgrom2007], counting ADCs can be operated at frequencies up to 100kHz. As each channel must be sampled at 40kHz, only two channels can be multiplexed into one counting ADC, which would then operate at 80kHz. Thus, with a total number of 64 channels, at least 32 counting ADCs are required, which would use quite a bit of area, remembering that each ADC contains at least one comparator.

Sigma-Delta ADC

The Sigma-Delta ADC architecture is one of the most popular high-resolution medium-to-low-speed ADC architectures in use today. The Sigma-Delta ADC architecture is typically used in applications requiring resolutions from 12 to 24 bits [Kester2005-2]. A Sigma-Delta ADC contains very simple analog electronics (a comparator, voltage reference, a switch and one or more integrators and analog summing circuits), and quite complex digital computational circuitry [Kester2005-1]. Thus, requirements placed on the analog circuitry are relaxed at the expense of more complicated digital circuitry, which becomes a more desirable trade-off for modern submicron technologies [Johns1997].

High resolution, together with on-chip programmable-gain amplifiers (PGAs) allows direct digitization of small output voltages of sensors, requiring no instrumentation amplifier. Sigma-Delta ADCs offer therefore an attractive alternative to traditional approaches using an instrumentation amplifier and a SAR ADC [Kester2005-2].

Sigma-Delta ADCs contain as building blocks a digital filter and decimator. The digital filter does introduce inherent pipeline delay. Consequently, the Sigma-Delta ADC cannot be operated in a single-shot or burst mode [Kester2005-2].

Conclusion

In conclusion, any of Counting, Successive Approximation, Pipelined [1] or Sigma-Delta ADC architectures could be used for converting 49 channels at 40kHz per channel with 12-bit resolution. The Folding and Flash ADC architectures are not taken into consideration because they hardly reach 12-bit resolution. The Counting ADC architecture can be excluded also because it would require at least 32 ADCs operating in parallel, which means an excessively big silicon area.

From the remaining Successive Approximation, Pipeline and Sigma-Delta ADC architectures, none has an obvious advantage at first sight. However, the Successive Approximation ADC architecture has been used extensively in multiplexed data acquisition systems, which is our application, whereas the

[1] Due to its popularity, the Pipelined ADC is taken as representative of all Subranging ADCs.

Sigma-Delta ADC architecture is typical for precision industrial measurement as well as voiceband and audio applications. Finally, the pipelined ADC architecture is most convenient for high-speed applications like instrumentation, video, radar, communications and consumer electronics [Kester2005-2]. Resolution versus sampling rate is displayed in Figure 3-2 for the three remaining ADC architectures, along with their typical applications. Section 3.2 lists further arguments in favor of the Successive Approximation ADC architecture.

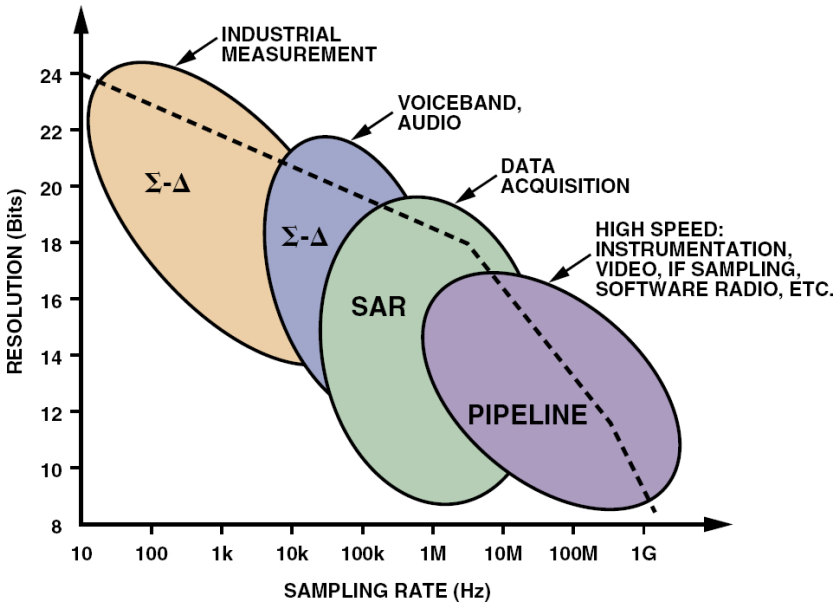


Figure 3-2 ADC architectures, applications, resolution and sampling rates. The dashed line was the state of the art in 2005 [Kester2005-2]

3.2. Advantages of the SAR ADC

- Very simple principle. SAR ADCs implement the binary search algorithm.
- Low power consumption. A SAR ADC does not contain an operational amplifier; operational amplifiers are generally power-hungry. The SAR ADC contains solely a comparator; comparators consume much less power than operational amplifiers. Pipelined and Sigma-Delta ADCs contain power-hungry operational amplifiers. From SAR, Pipelined and Sigma-Delta ADCs, the SAR ADC is most likely low-power.
- No pipeline delay (latency). In a pipelined ADC, the pipeline delay is a multiple of the sampling clock period. For low sampling frequencies, there will be a considerable latency. The SAR ADC can use an internal clock that is independent of (and – if desired – much faster than) the sampling clock; output codes can thus be delivered with a delay negligible with respect to the sampling clock period. Closing the loop[1] requires that ADC and DAC have no latency, a further argument in favor of the SAR ADC.

[1] "Closing the loop" refers to either of the following electrophysiological experiments:

- Stimulate a neural network at one point, let the signal propagate through the neural network and record it at a different location.
- Monitor a neural network and stimulate it at a given location in response to recorded activities.

3.3. Switched-Capacitor or Charge-Redistribution SAR ADC

A SAR ADC has the following building blocks:

- Sample-and-Hold Stage (S/H)
- Digital-to-Analog Converter (DAC)
- Comparator
- Successive Approximation Register (SAR)

Figure 3-3 shows the basic SAR ADC.

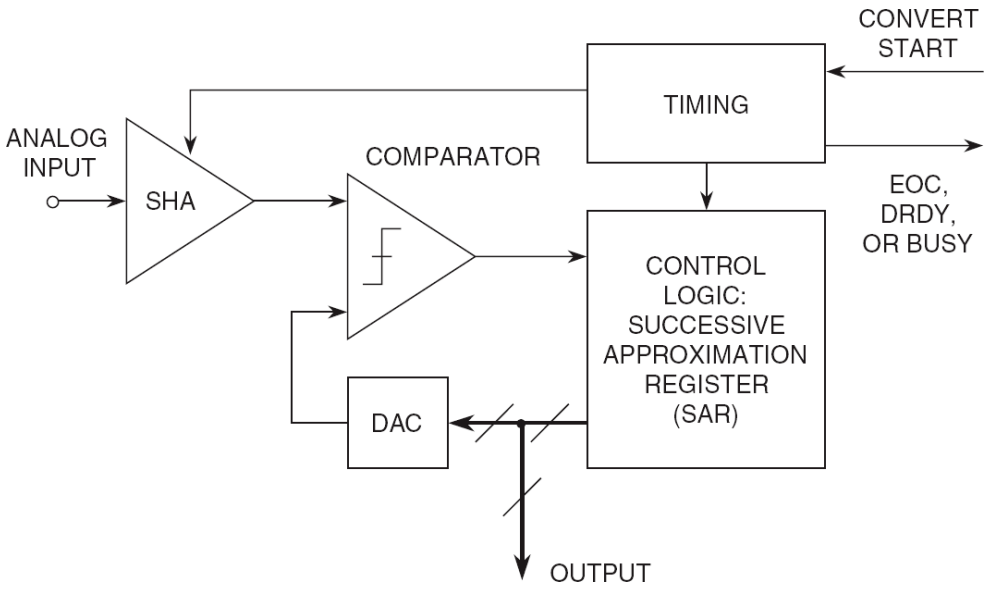


Figure 3-3 Basic SAR ADC with S/H stage, DAC, Comparator and SAR [Kester2005-1]

SAR ADCs can be classified according to the DAC they use. The *Charge-Redistribution* or *Switched-Capacitor (SC)* SAR ADC is by far the most popular one. It combines the S/H stage and the DAC in a single building block, a switched-capacitor array. Figure 3-4 shows a 3-bit SC SAR ADC with its binary-weighted parallel capacitor array.

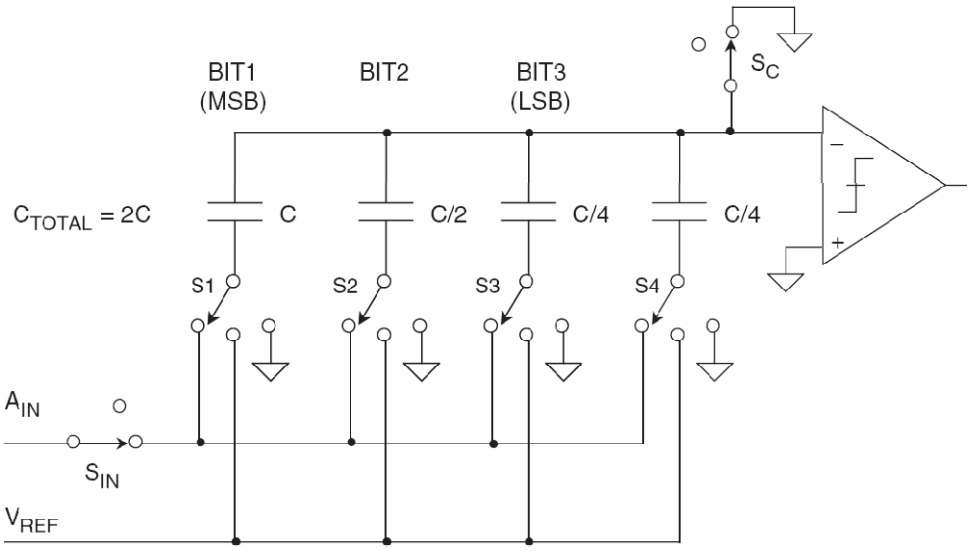


Figure 3-4 3-bit SC SAR ADC with single-ended analog path [Kester2005-1]. The capacitor array serves as DAC and S/H stage at the same time. The SAR control logic, which is not shown here, controls the switches and takes the comparator's response as input.

4. Topology of the SC SAR ADC

4.1. Data conversion system with analog multiplexing and output code synchronization

The entire data conversion system consists of the ADC front-end, ADC core, ADC back-end, clock generator and voltage references. The ADC front-end performs analog signal multiplexing, while the ADC back-end is responsible for output code synchronization. Figure 4-1 shows a block diagram of the entire data conversion system.

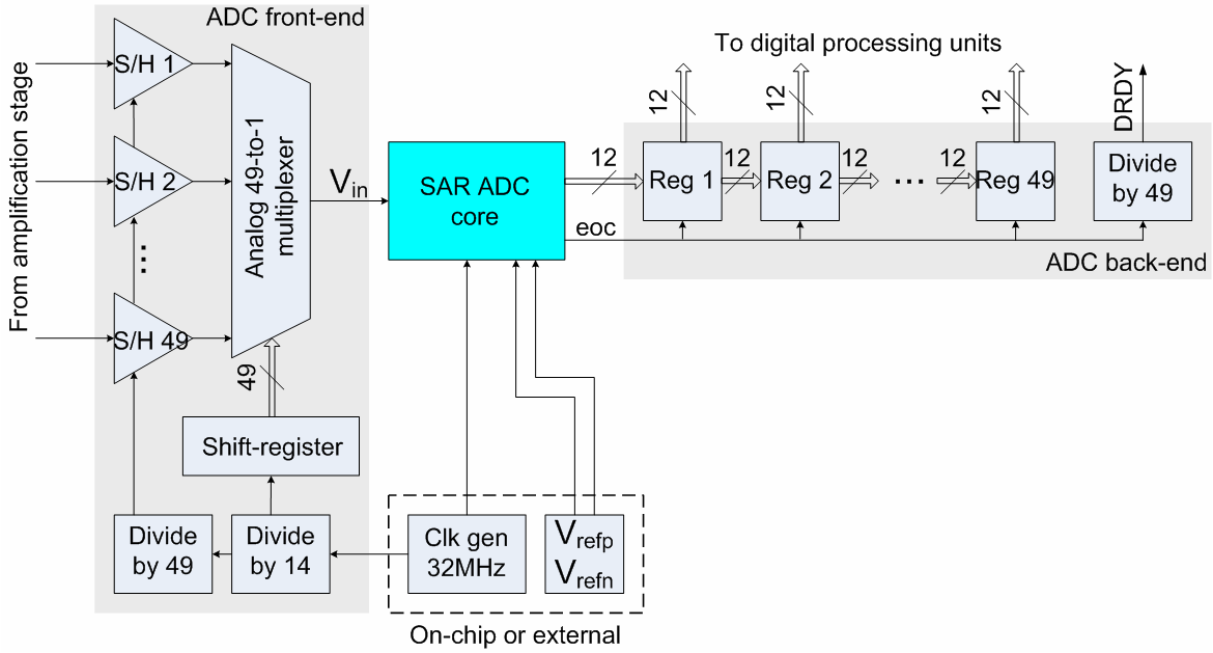


Figure 4-1 Block diagram of the SAR ADC with analog signal multiplexing and output code synchronization

An analog multiplexer chooses sequentially 1 out of 49 channels. The multiplexer consists of analog switches (transmission gates) for the analog signal path, as signals are bipolar and conduction must be guaranteed over the full analog range. To select 1 out of 49 switches, a shift-register consisting of 49 D-flip-flops, producing a one-hot code is used. Alternatively, a 49-counter producing a binary sequence can be used in conjunction with an encoder (binary to one-hot encoder). The shift-register or 49-counter must be clocked from a clock 14 times slower than the internal ADC core clock of 32*MHz*; a simple counter circuit divides the frequency by 14. Using S/H stages at the input of the multiplexer, all channels can be sampled at the same instant. The S/H stages are triggered as soon as 49 conversions have been completed.

The analog multiplexer feeds one channel to the actual ADC, referred to as ADC core in the following text. The ADC core is the main subject of this work and discussed in detail in the following chapters. The ADC core is supported by a clock generator and voltage references.

A 32*MHz* clock signal is available on the neurochip. It is either generated on-chip or comes from an external clock generator. From the 32*MHz* clock signal, different clock signals, as required by the

ADC core, are generated in the ADC core. All clock signals have the same frequency; their phase and duty cycles, however, vary.

The ADC core is backed by both a positive reference voltage $V_{refp} = 900mV$ and a negative reference voltage $V_{refn} = -900mV$. Depending on their stability, the dual analog power supply rails can be used as reference voltages. A 10-bit SAR ADC following this approach is presented in [Bechen2006]. Using the supply voltages as reference voltages saves an extra reference circuit and allows verifying the current consumption of the ADC core. If it is found that the supply voltages are not stable enough, external voltage references will be used. Yet other solutions with on-chip bandgap voltage references are discussed in *Chapter 11.2 Future work*.

Generally, output codes can be delivered sequentially or in parallel. The ADC core issues the 12 bits corresponding to one sample in parallel, at the end of the conversion, every $437.5ns$ [1]. The end of the conversion is signaled by setting the '*eoc'* flag. The 12-bit digital codes corresponding to samples from different channels could either be delivered as soon as they are ready (one 12-bit code every $437.5ns$), or shifted through a 12-bit wide, 49-bit long register bank in order to be issued all at the same time, after all 49 channels have been converted, every $21.4375\mu s$ [2]. Right-shifting is triggered by the *eoc* signal. A simple counter circuit (*Divide by 49*) produces the *Data Ready (DRDY)* signal, which goes high as soon as all 49 12-bit output codes are ready to be read out in parallel.

The whole system is powered from a dual $\pm 900mV$ power supply. Throughout the text, V_{DD} denotes the highest voltage in the circuit and V_{SS} the lowest one. Ground is defined as the middle point between V_{DD} and V_{SS} . For differential signals, the common-mode voltage is ground.

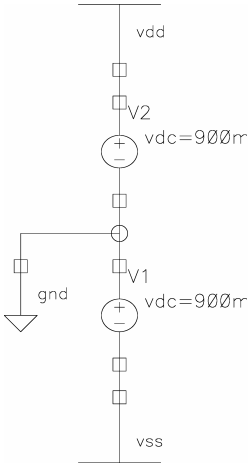


Figure 4-2 Dual power supply: definition of V_{DD} , V_{SS} and ground

4.2. SC SAR ADC core

The ADC core performs the actual A/D conversion. It consists of the following blocks:

- Comparator
- Capacitor array (DAC and S/H)

[1] This is the ADC core's conversion time: $14/32MHz = 14 \cdot 31.25ns = 437.5ns$

[2] This is the time to convert all 49 channels: $49 \cdot 437.5ns = 21.4375\mu s$

- SAR control logic
- Switches
- Delay elements and Drivers

A separate chapter is dedicated to each block. Figure 4-6 on page 23 shows the whole ADC core. Capacitors with switches at their bottom plates are shown as “binary-weighted C-Cells”, denoted C, 2C, 4C and 8C.

Considering single-ended signals, an analog input range of $[-900,900]mV$ and 12-bit resolution, the voltage step corresponding to one LSB change is $V_{LSB}^{s-e} = 1.8V / 2^{12} = 439.45\mu V$. Most analog blocks must have a noise floor lower than $0.5V_{LSB}^{s-e} = 219.725\mu V$.

With fully differential signals, the maximum analog input range becomes $[-1.8,1.8]V$ and $V_{LSB}^{f-d} = 3.6V / 2^{12} = 878.91\mu V$. The minimum voltage difference the comparator has to discriminate has doubled. The two duplicated capacitor arrays still need to have a noise floor lower than $0.5V_{LSB}^{s-e} = 219.725\mu V$.

Following convention is used throughout the text: $V_{LSB} = V_{LSB}^{s-e}$.

4.2.1. Ideal transfer characteristic

Figure 4-3 shows the ideal transfer characteristic of the SAR ADC core. Output code representation is *sign magnitude*. The sign or polarity of the input signal defines the *MSB* or *sign bit*. Positive (negative) input signals have *MSB='0'* (*MSB='1'*). Notice that there are two representations for the number zero, namely $+0$ and -0. In fact, analog input signals in the range $[0, V_{LSB}]$ produce the output code $0000'0000'0000$ (number $+0$), while input signals in the range $[-V_{LSB}, 0]$ produce the output code $1000'0000'0000$ (number -0). The remaining 11 bits are binary coded and disclose the distance from zero. Positive and negative numbers of equal absolute value have, for most part, the same representation; the only part that differs is the sign bit. Table 2-1 details the sign magnitude representation with the example of a 3-bit code.

Number	MSB, sign bit, b0	b1	LSB, b2
+3	0	1	1
+2	0	1	0
+1	0	0	1
+0	0	0	0
-0	1	0	0
-1	1	0	1
-2	1	1	0
-3	1	1	1

Table 4-1 3-bit sign magnitude representation

The ideal step size is $V_{LSB} = 439.45\mu V$. Transition points T_z are defined by multiples of V_{LSB} : $T_z = z \cdot V_{LSB}$, where $z = -2^{11}+1, ..., -1, 0, 1, ...2^{11}-1$. The full range input signals $2^{11} \cdot V_{LSB} = 900mV$ and $-2^{11} \cdot V_{LSB} = -900mV$ yield output codes $0111'1111'1111$ and $1111'1111'1111$, respectively.

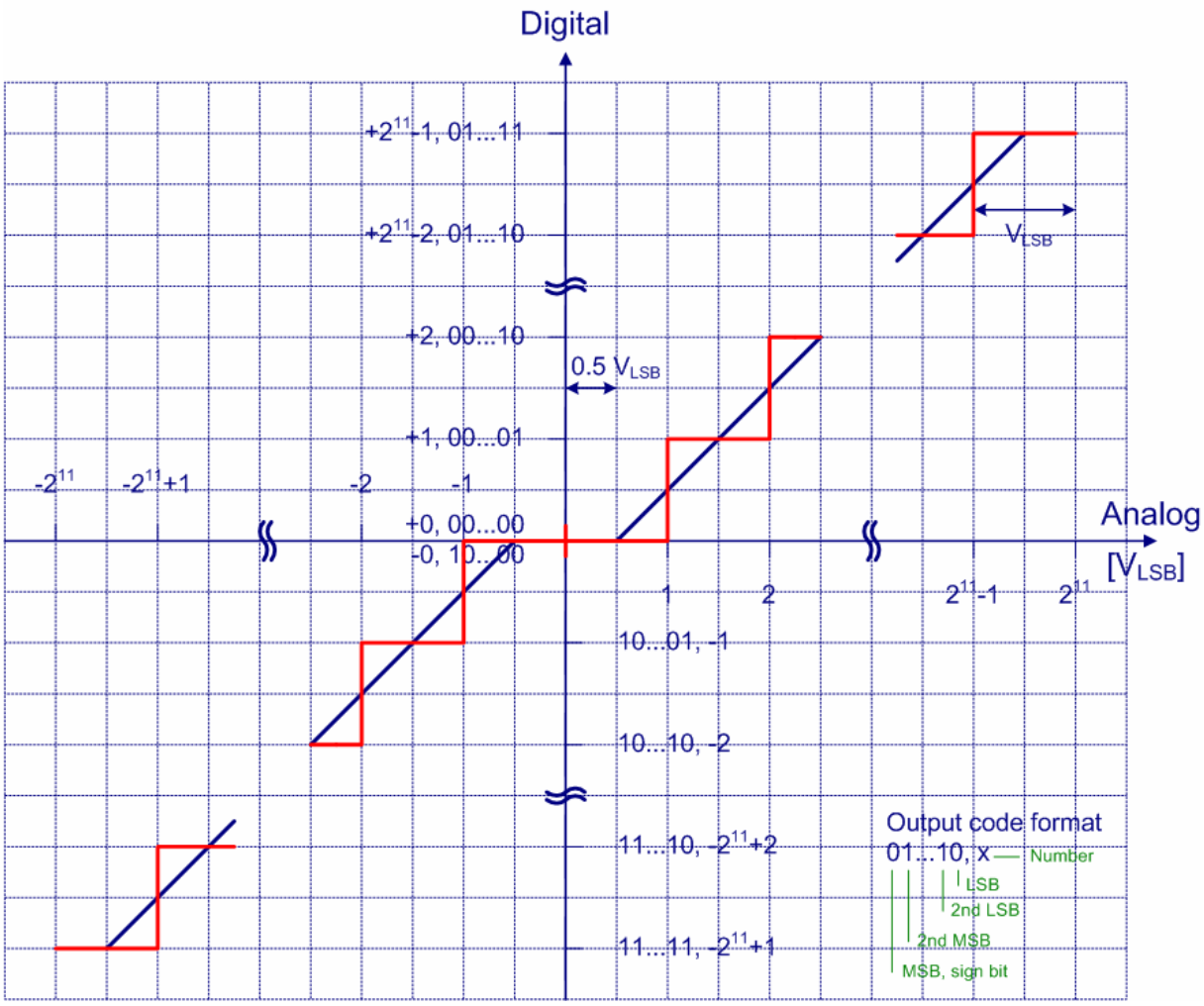


Figure 4-3 Ideal ADC transfer characteristic

4.2.2. Fully differential vs. Single-ended analog signal path

A fully differential analog signal path has several advantages with respect to a single-ended analog signal path.

- Immunity to common-mode noise
- The input dynamic range is doubled. As a consequence, V_{LSB} is doubled, which relaxes the design requirements of the comparator.
- For signals varying slightly around the common-mode voltage, errors due to charge injection (also called charge feedthrough or clock feedthrough) are minimized, which is essential in high-precision switched-capacitor circuits.
- Even harmonics introduced by circuit non-linearities are cancelled, improving the harmonic distortion characteristics of the system [Liechti2004]

Drawbacks of the fully differential topology are increased area, power and cost.

4.2.3. Timing

The presented ADC uses an external clock at a frequency of $f_{clk} = 32MHz$. The corresponding clock period is $T_{clk} = 1/f_{clk} = 31.25ns$. A duty cycle of 50% is considered. The worst-case rise and fall times are $300ps$. Figure 4-4 shows the externally generated clock signal.

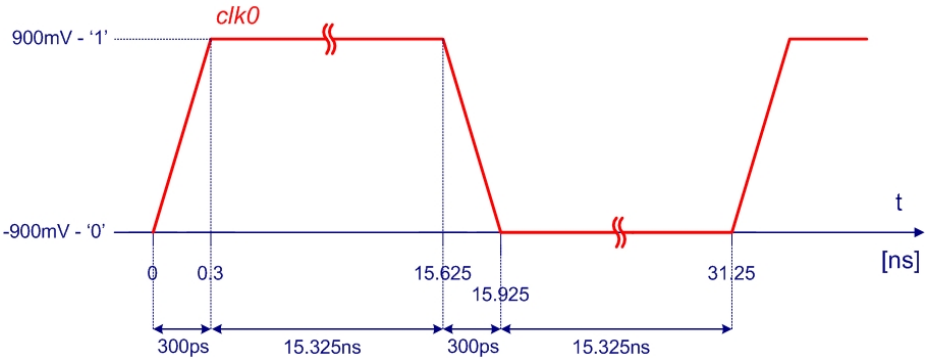


Figure 4-4 Clock signal

The sum of the following terms must be smaller than $T_{clk} = 31.25ns$.

- Critical path delay of SAR control logic
- Delay of switches
- Settling time of the DAC to 12-bit accuracy. In fact, the DAC output (voltage at node V_X) must settle within $\pm 0.5V_{LSB}$ of its final value
- Response time of the comparator. The comparator response time is the sum of the preamplifier delay time and the time the latch takes to establish full logic levels from the moment it has been triggered.

The full clock period of 31.25*ns* is split unequally into maximum delay specifications for the four elements. In general, analog parts are allowed to have higher delays than digital parts, as the latter are easily implemented in an advanced technology like UMC $0.18\mu m$ CMOS, whereas the design of analog parts proved more and more challenging as technology scales down. In particular, the presented ADC design has very strict settling requirements for the DAC and strict resolution requirements for the comparator, making their design challenging, while the design of the SAR control logic is relatively easy. We require that the critical path delay of the SAR control logic be smaller than 2*ns* and each of DAC settling time and comparator response time be smaller than 10*ns*. With these timing requirements, there is enough timing safety margin to allow clock skew (spatial variation in temporally equivalent clock edges) and clock jitter (temporal variation in consecutive clock edges) to a certain extend.

The external clock signal is referred to as *reference clock* or *clk0*. It controls the counter (See *Chapter 7.1 14-Counter*), an internal block of the SAR control logic which lets the ADC cycle through the 14 steps of an A/D conversion. To synchronize the output registers of the SAR control logic (See *Chapter 7.3 Output registers*), a second clock signal, referred to as *clk1*, is created. *clk1* is delayed by approximately 2*ns*[1] with respect to *clk0.* The analog switches are eventually[2] switched at every rising transition of *clk1*. In the time interval from a rising edge of *clk1* to the next rising edge of *clk0*[3], the DAC settles within $\pm 0.5V_{LSB}$ and the preamplifier of the comparator (See *Chapter 5.3 Preamplifier*) amplifies its new input voltage difference ΔV_{in}. At the rising edge of *clk0*, the latch of the comparator

[1] See *Chapter 7.2 Combinational logic* for a justification of this value.

[2] If a switch needs to be switched, then it is switched on the rising edge of *clk1*.

[3] The length of this time interval is $T_{clk} - delay(clk1, clk0) = 31.25ns - 2ns = 29.25ns$.

(See *Chapter 5.4 Latch*) takes a decision. The latch must establish full logic levels before the next rising edge of *clk1*, i.e. within less than 2*ns*, as at this clock edge, the response of the comparator is read into the output registers. Figure 4-5 shows the timing diagram.

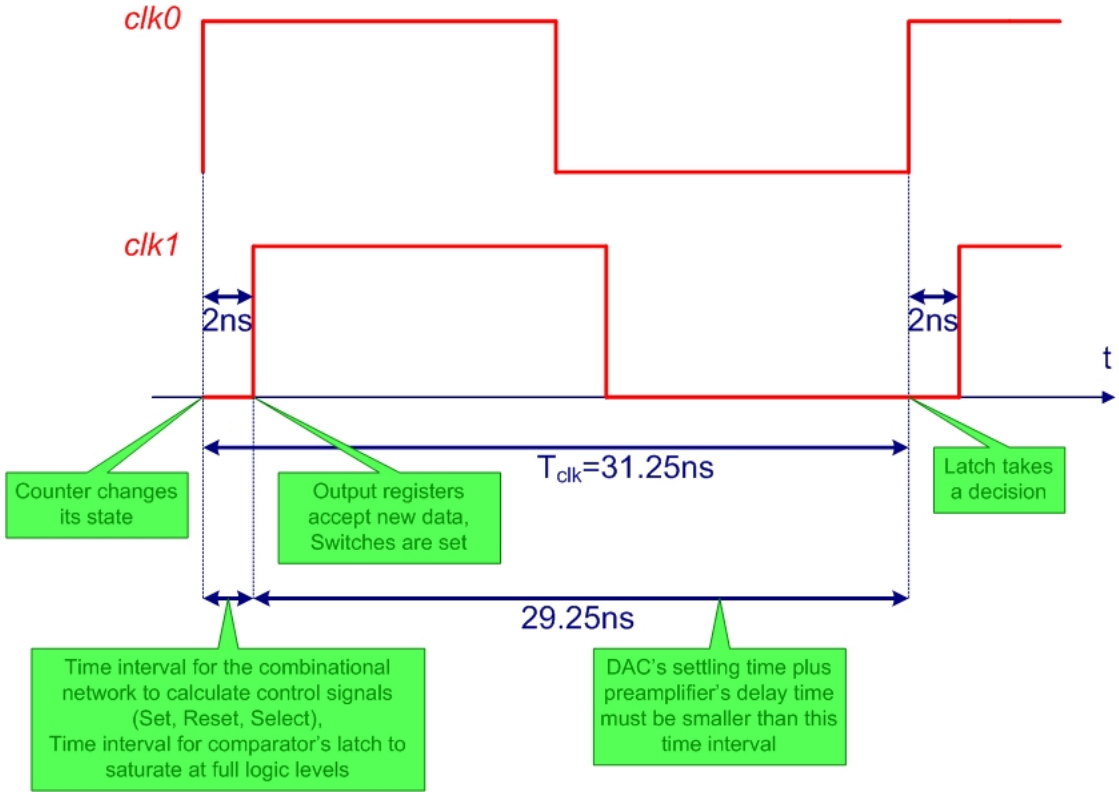


Figure 4-5 Timing diagram

From Figure 4-5, it is understood that the delay time for positive transitions and the rise time of *clk1* must be precisely controlled, while the delay time for negative edges and the fall time of *clk1* do not need to be precisely controlled. In fact, neither level-sensitive elements, nor negative-edge triggered flip-flops are used. Also, notice that negative going transition and delay times can be different from the positive going ones. Delay elements are presented in *Chapter 9 Delay elements*.

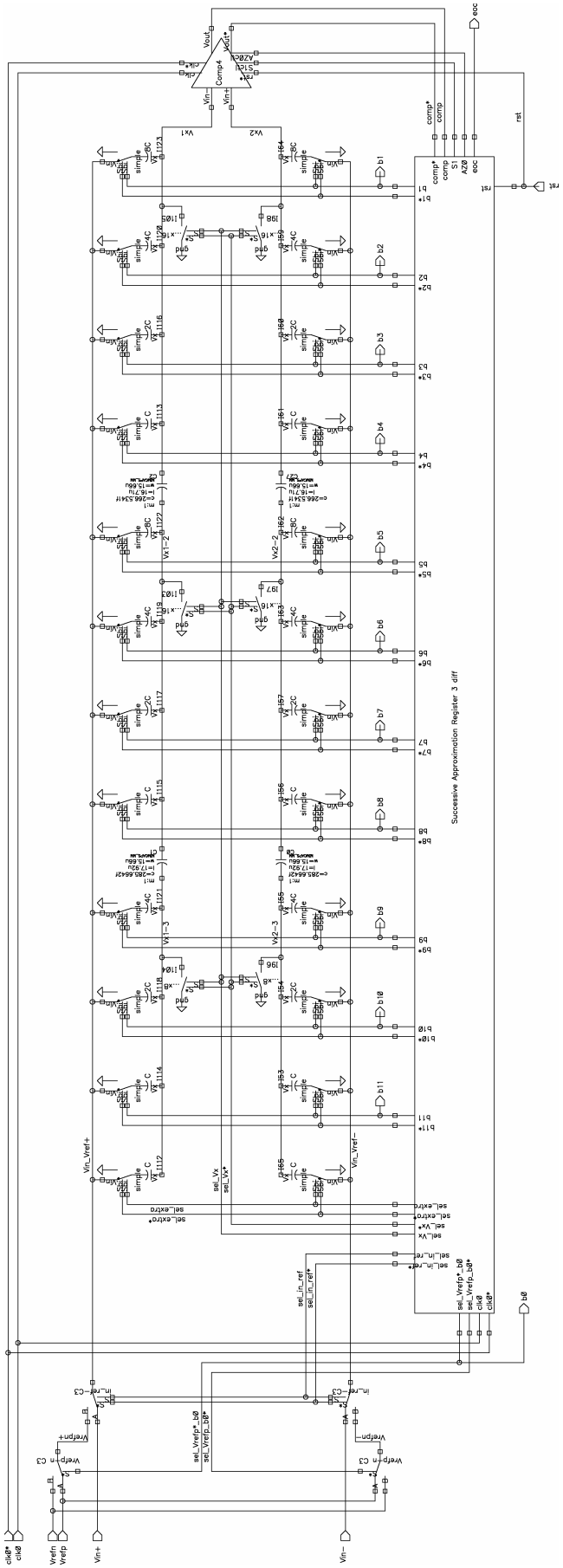


Figure 4-6 ADC core.

5. Comparator

Each A/D Converter contains at least one comparator. A comparator itself can be considered a 1-bit A/D Converter. In the presented ADC design, the comparator plays a key role; it must be able to discriminate voltages as small as $219\mu V$ [1].

5.1. Specifications

Where comparators are incorporated into IC ADCs, their design must consider:

- Offset voltage
- Resolution
- Speed
- Bias current
- Power dissipation
- Area
- Metastability [Kester2005-1]

A critical specification is the offset voltage. We require that the offset voltage V_{OS} be smaller than $0.5V_{LSB} = 219.725\mu V$. Clearly, to reach this requirement, offset-cancellation techniques must be applied. In fact, differential amplifiers, as the ones used in the pre-amplifier of the comparator (See *Section 5.2 Architecture*) have an offset voltage of $1mV$ to $10mV$ if they are realized in CMOS technology [Makinwa2002]. (Differential amplifiers realized in bipolar technology have offset voltages of approximately *0.1mV* [Makinwa2002]). In practice, the residual offset after performing dynamic offset cancellation can be as small as $1\mu V$ to $10\mu V$ [Makinwa2002].

The resolution of a comparator can be defined as $(\Delta V_{IN})_{\min} = \max\{V_{OS}, (V_{SAT+} - V_{SAT-})/A_0\}$, where A_0 is the DC gain [Kayal2008]. As V_{OS} can be reduced to several μV , the dominant term determining the resolution is $(V_{SAT+} - V_{SAT-})/A_0$ .Once more, we require $(\Delta V_{IN})_{\min}$ be smaller than $0.5V_{LSB} = 219.725\mu V$. Thus, the minimum DC gain is

$$A_{0,\min} = \frac{V_{SAT+} - V_{SAT-}}{(\Delta V_{IN})_{\min}} = \frac{V_{DD} - V_{SS}}{0.5V_{LSB}} \tag{0-2}$$

With $V_{LSB} = \frac{V_{DD} - V_{SS}}{2^{12}}$, Eq. (0-2) becomes $A_{0,\min} = 2^{13} = 8'192$. In conclusion, to discriminate voltage differences as small as $0.5V_{LSB}$, a minimum gain of 8’192 is required. The design of the comparator targets a gain of at least 16’000.

[1] To work out the specifications of the comparator, an ADC with single-ended analog signal path has been considered, even though the comparator itself is fully-differential. Using this comparator in a fully differential ADC improves its characteristics such as DNL, INL, etc.

As discussed back in *Section 4.2 SC SAR ADC core*, the response time of the comparator must be smaller than 10*ns*. The comparator's response time is the sum of the pre-amplifier's delay time and the latch's delay time.

The power dissipation is proportional to the bias current. Neither power dissipation, nor bias current is rigorously specified. Nevertheless, efforts will be made to minimize both quantities. Of course, also the area will be kept as small as possible.

Metastability is the ability of a comparator to balance right at its threshold for a short period of time or in other words its occasional inability to resolve a small differential input into a valid output logic level [Kester2005-1]. Metastability can be dealt with by inserting a pre-amplifier [Lim], what is done anyway in the presented comparator design. Anyhow, metastability is an important design issue for high speed ADCs like the Flash type, but not for this kind of low-speed SAR-type ADC.

Table 5-1 summarizes the main specifications of the comparator.

Specification	Value
Offset voltage V_{OS}	$< 0.5V_{LSB} = 219\mu V$
Resolution $(\Delta V_{IN})_{\min}$	$< 0.5V_{LSB} = 219\mu V$
Response time	$< 10ns$

Table 5-1 Main specifications of comparator

5.2. Architecture

The comparator consists of a preamplifier and a latch, as shown in Figure 5-1. The preamplifier, which has an optimized noise performance, isolates the capacitor array from the latch, which could introduce noise, e.g. from the clock, and amplifies the minimum input voltage difference $(\Delta V_{IN})_{\min} = 219\mu V$ to a value bigger than the offset voltage of the latch. The latch regenerates time by taking a decision at each rising edge of clock *clk0* and establishes full logic levels at V_{DD} and V_{SS}.

The preamplifier has 3 stages, in order to relax the gain requirements of each stage, reach a minimum power-delay product and increase the speed. The noise performance of the first stage is most critical one, as it is directly connected to the capacitor array. To improve the preamplifier's noise characteristics, the first stage must have the highest gain.

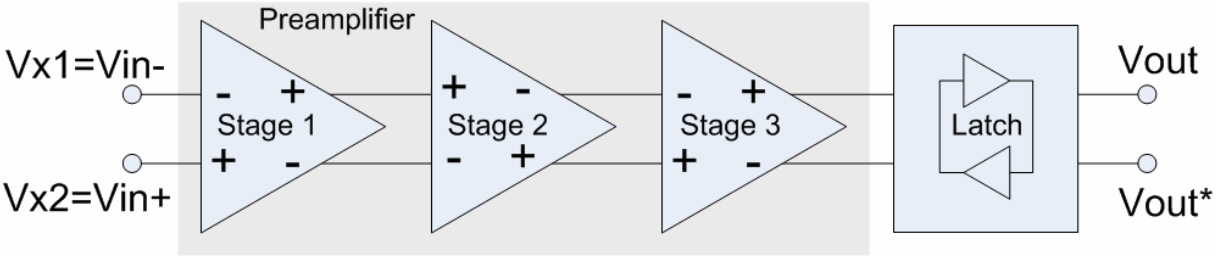


Figure 5-1 Architecture of the comparator

The overall comparator gain is the product of the gain of the preamplifier and the gain of the latch. The gain of inverters inserted after the latch does not contribute to the overall gain anymore, as the latch already establishes full logic levels at V_{DD} and V_{SS}. Nevertheless, additional inverters (called buffers or drivers) are used to drive the capacitive load.

5.3. Preamplifier

5.3.1. Specifications

The main design criteria for each stage are gain and bandwidth (cut-off frequency f_{-3dB}).

If the preamplifier gain is $A_v = 3'375$, the minimum signal we want to look at is amplified to $A_v \cdot (\Delta V_{IN})_{\min} = 0.74V$, a value much higher than the offset voltage of the latch. This gain is reached if each stage has a gain of $A_{vi} = 15 \triangleq 23.52dB$. Adding roughly *3dB* for pre-layout simulations yields $A_{vi} \cong 26dB$.

In order to know the required bandwidth, the input to the preamplifier has to be examined. The comparator's input voltage V_X is modeled as follows.

Let's assume that a full range voltage is sampled. During the hold mode, $V_X = -0.9V$. Next, during the 12 bit-cycling states, V_X approaches zero in a step-like fashion, with the step height being cut in half at each step. Let's model this signal as a continuously increasing analog signal that will be sampled and hold afterward to reach the original step-like increasing signal. The un-sampled analog signal has a bandwidth of 32*MHz*/12=2.67*MHz*, as there are 12 cycles of interest. The baseband of this signal goes from $-f_B = -2.67MHz$ to $f_B = 2.67MHz$, as shown in Figure 5-2.

Now, if sampling this signal at a sampling frequency $f_S = 32MHz$, the baseband is replicated around the multiples of the sampling frequency. The first replica is centered at 32MHz and included between 29.33MHz and 34.67MHz. The second replica is centered at 64MHz and included between 61.33MHz and 66.67MHz.

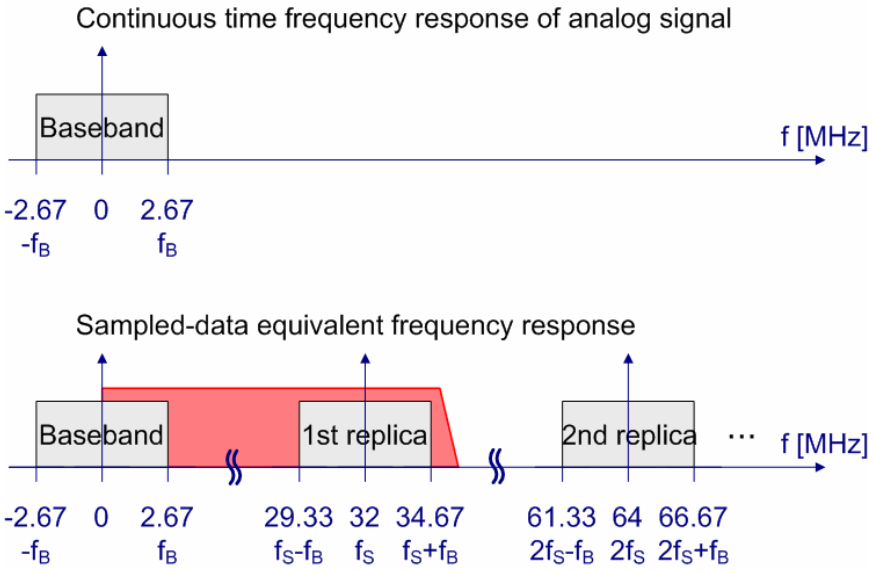


Figure 5-2 Continuous time frequency response of an analog signal and its sampled-data equivalent frequency response. The bandwidth of the preamplifier is shown in red.

To reconstruct the analog signal with little distortion, the bandwidth of the preamplifier must be at least 35MHz, as indicated in Figure 5-2 by the red area. In pre-layout simulations not including any parasitic capacitances, a bandwidth of roughly 70MHz is targeted.

5.3.2. Design approach

The design of stage 1, shown in Figure 5-3 is based on equations (5-2) through (5-7). Equations (5-5) to (5-7) are taken from the EKV model and are true for all transistors shown in Figure 5-3, as they all operate in saturation.

To minimize charge sharing between the capacitor array and parasitic gate capacitances, transistors M22 and M23 are made as small as possible, even though $W_{22/23} \nearrow \Rightarrow g_{m22/23} \nearrow \Rightarrow A_{v1} \nearrow$. The required gain is obtained by increasing $L_{4/10}$. As – due to charge sharing – $g_{m22/23}$ cannot be increased, C_L needs to be minimized to reach the required bandwidth. To decrease C_L, the input transistors of the next stage must be small and the layout must minimize interconnect capacitances.

The gain-bandwidth product f_{GBW} can be increased by increasing the tail current. However, low power consumption is preferable. A tail current of $10\mu A$ is chosen.

Saturation voltages are designed such as to have a DC voltage near to ground (common-mode voltage) at the output nodes *V2+* and *V2-* if the inputs are tied to ground.

$$A_{v1} = -\frac{g_{m22/23}}{g_{ds22/23} + g_{ds4/10}} \tag{0-3}$$

$$f_{GBW} = \frac{g_{m22/23}}{2\pi C_L} \tag{0-4}$$

$$f_{-3dB} = \frac{f_{GBW}}{A_{v1}} \tag{0-5}$$

$$g_{ds} = \frac{I_D}{U_a L} \tag{0-6}$$

$$g_m = \sqrt{\frac{2\beta I_D}{n}} = \beta V_{Dsat} \propto \frac{W}{L} \tag{0-7}$$

$$V_{Dsat} = \sqrt{\frac{2I_D}{\beta n}} \propto \sqrt{\frac{L}{W}} \tag{0-8}$$

Figure 5-3 shows all final transistor dimensions and the biasing current.

The same approach is used to design stages 2 and 3. As for the bandwidth of stage 3, the input transistors of the latch must be considered. Figure 5-4 shows the whole preamplifier and all transistor dimensions.

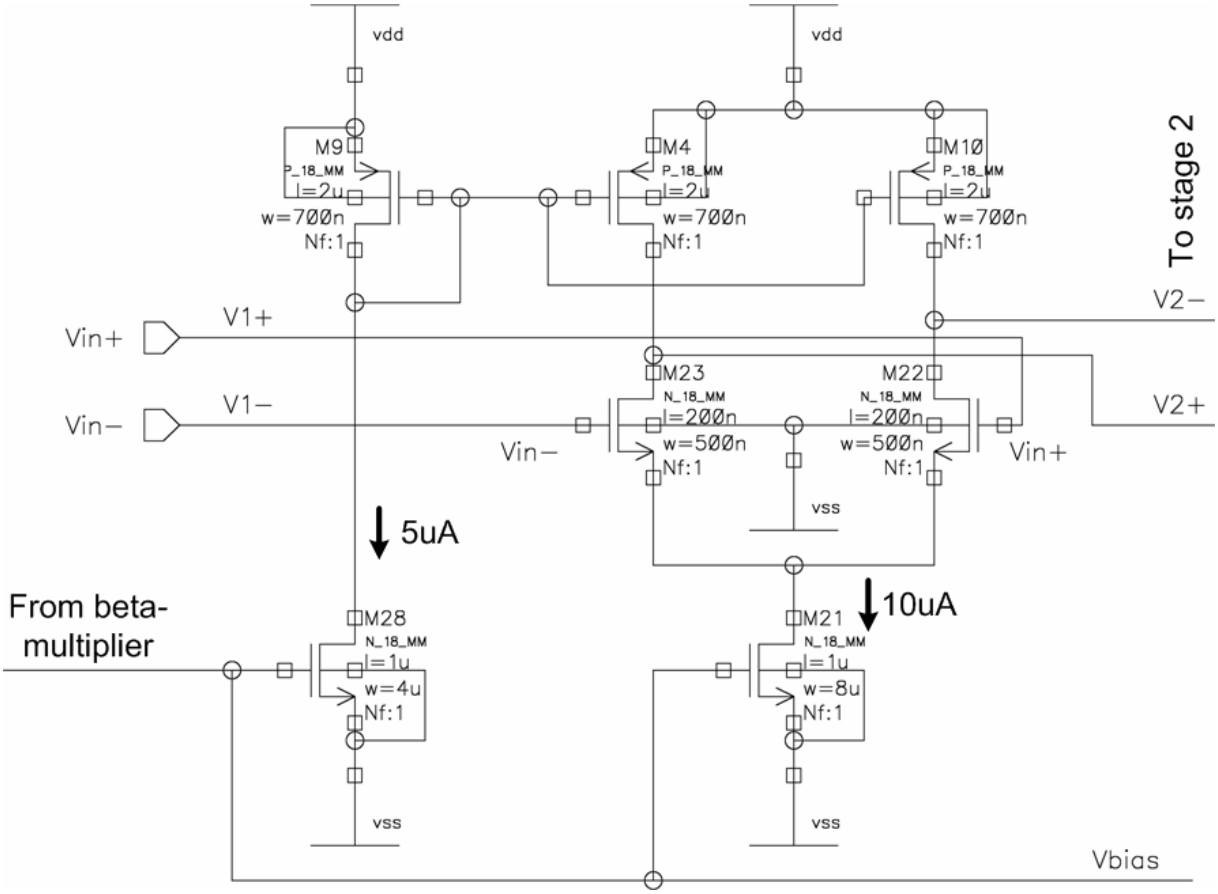


Figure 5-3 Stage 1 of preamplifier.

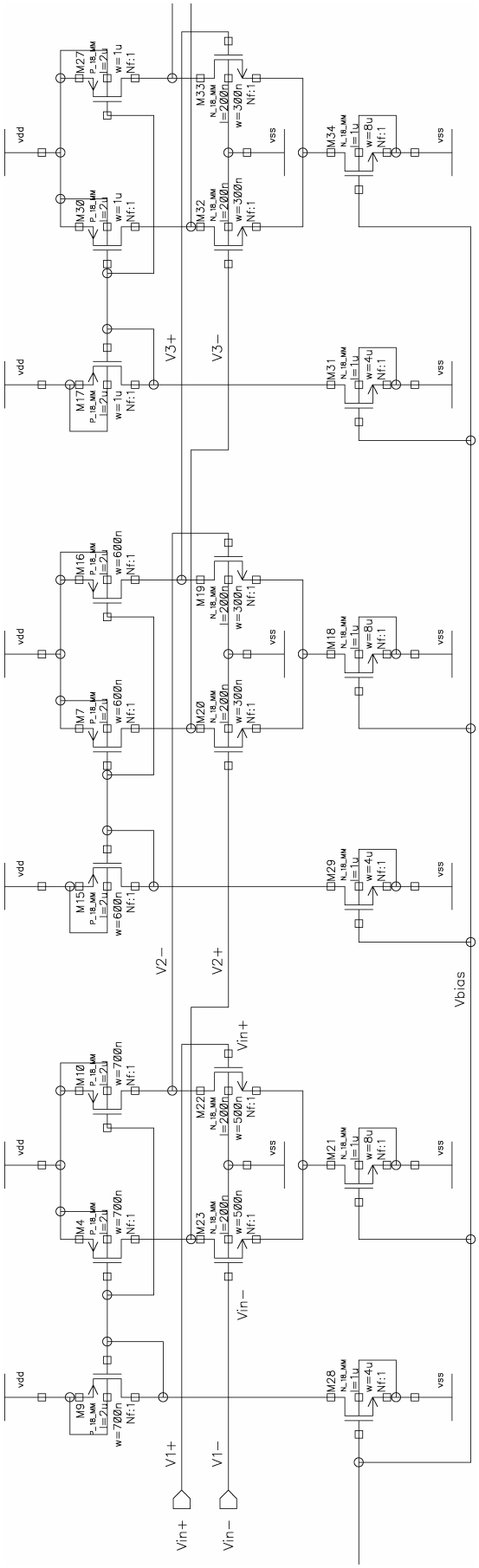


Figure 5-4 Preamplifier: circuit at transistor level

5.3.3. Pre-layout simulation results

	A_{vdB} [dB]	A_v	f_{-3dB} [MHz]
Stage 1	26.3332	20.73	117
Stage 2	26.0294	20.02	95
Stage 3	25.7131	19.30	208
Preamplifier	78.0757	8'012.81	54

Table 5-2 Pre-layout simulation results of the amplifier.

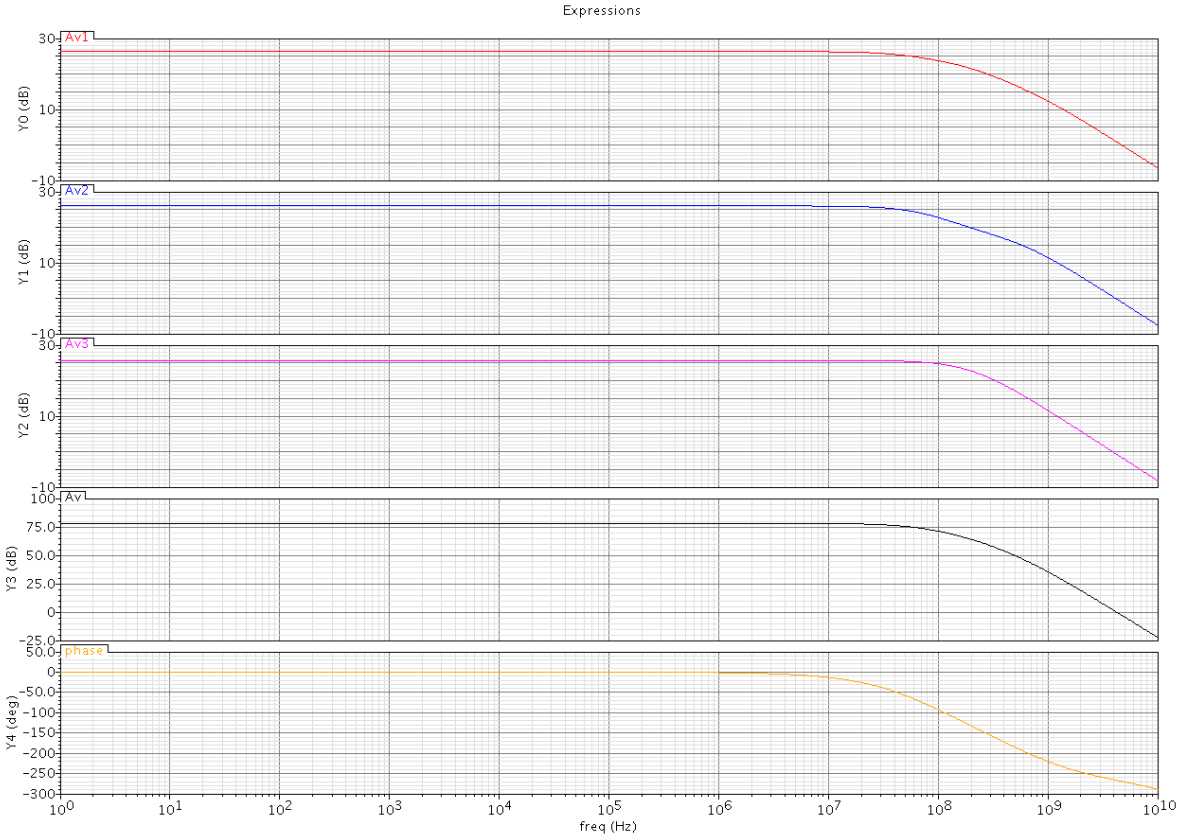


Figure 5-5 Pre-layout simulation results of the preamplifier. From top trace to bottom trace: Av1, Av2, Av3, Av and phase-shift of preamplifier.

At a frequency of 32MHz, the preamplifier has a phase shift of -39°.

Figure 5-6 shows transient simulation results for a sine input signal of $200\mu V$ at $32MHz$. As signals are differential, the magnitude of the input signal *diff1* appears as $400\mu V$ on Figure 5-6. Signal *diff4* is the output of stage 3 and the input of the latch. It can be seen that every stage has a gain of about 20. None of the stages saturate. For the input signal of $200\mu V$, the delay of the preamplifier is $3ns$.

Noise introduced by the latch can be observed on Figure 5-6. At each edge of the clock signal, *diff4* is clearly perturbed. Notice that this perturbation does not propagate through to the input of the first stage; it is attenuated stage by stage.

Figure 5-7 shows transient simulation results for full-range input signals. The outputs of all stages saturate. The preamplifier has a delay of only $590ps$ for full-range input signals.

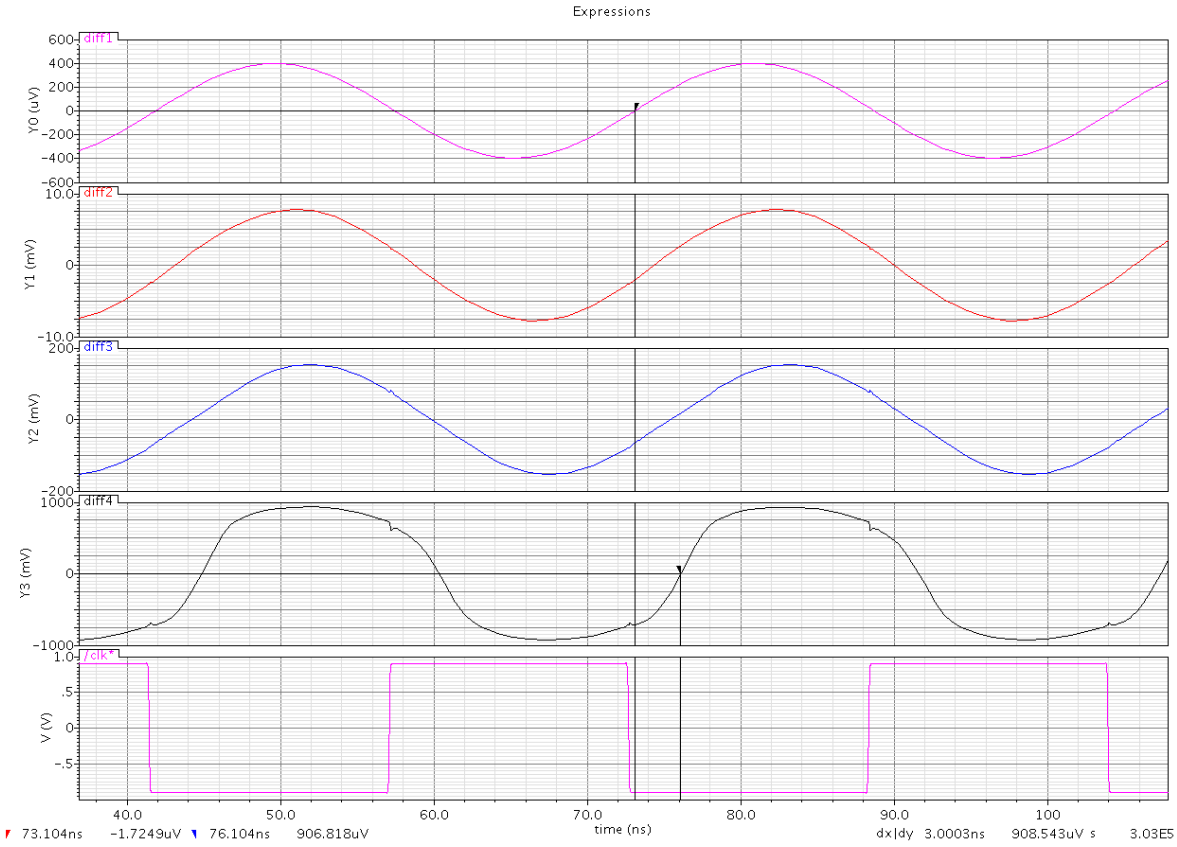


Figure 5-6 Transient simulation results for a $200\mu V$ input signal.

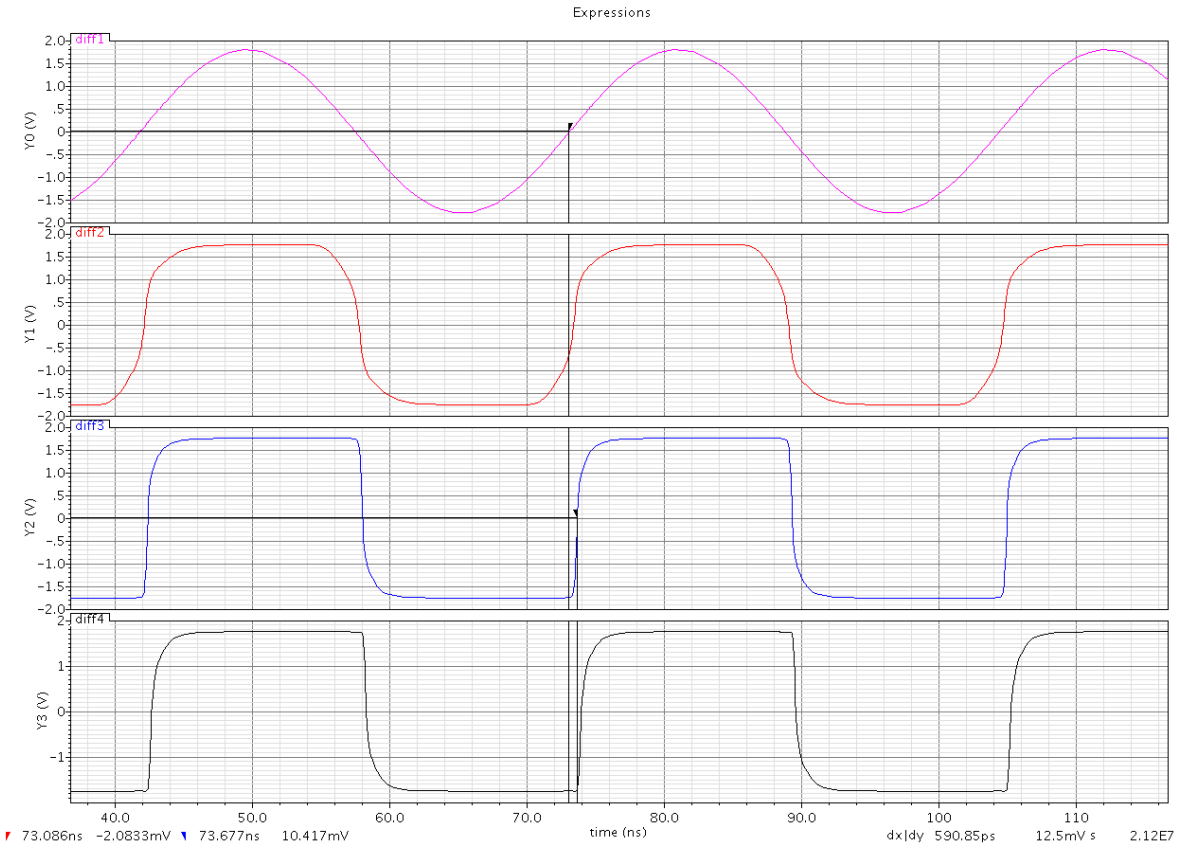


Figure 5-7 Transient simulation results for a full-range input signal.

5.3.4. Noise analysis

"The noise performance of the CMOS differential amplifier can be due to both thermal and 1/f noise. Depending on the frequency range of interest, one source can be neglected in favor of the other. At low frequencies, 1/f noise is important whereas at high frequencies/low currents thermal noise is important. 1/f noise is the dominant source of noise for frequencies below 100kHz." [Allen2002] Remember that a typical signal of interest (the full-range sample) has a baseband of 2.67*MHz* and its first replica centered at 32*MHz*. Thus, thermal noise is dominant; 1/f noise could be neglected.

Noise can be modeled by a current source connected in parallel with the MOS transistor. This current source represents two sources of noise, called thermal noise and flicker noise. The mean-square current-noise source is defined as

$$i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{(KF)I_D}{fC_{ox}L^2} \right] \cdot \Delta f \quad (A^2) \tag{0-9}$$

where

Δf = a small bandwidth (typically 1*Hz*) at a frequency f

$\eta = g_{mbs} / g_m$. From DC simulation

k = Boltzmann's constant. $k = 1.381 \cdot 10^{-23}\ J/K$

T = temperature. $T = 300K$

g_m = small-signal transconductance from gate to channel. From DC simulation

KF = flicker noise coefficient. Typically, $KF = 10^{-28}\ F \cdot A$

f = frequency. *f=32MHz* for this analysis.

The mean-square current-noise can be reflected to the gate of the MOS device by dividing (0-9) by g_m^2, yielding

$$e_n^2 = \frac{i_n^2}{g_m^2} = \left[\frac{8kT(1+\eta)}{3g_m} + \frac{KF}{2fC_{ox}WLK'} \right] \cdot \Delta f \ (V^2) \tag{0-10}$$

where

K' = transconductance parameter. $\beta = K'\frac{W}{L}$. β is determined by DC simulation.

C_{ox} = capacitance per unit area of the gate oxide

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\varepsilon_0}{t_{ox}} = \frac{3.9 \cdot 8.854 \cdot 10^{-12}\ F/m}{4.2 \cdot 10^{-9}\ m} = 8.22157 \cdot 10^{-3}\ F/m^2 = 8.22157\ fF/\mu m^2$$

($t_{ox} = 4.2nm$ is a model parameter of UMC's *N_18_MM* and *P_18_MM* models for nMOS and pMOS transistors, respectively.)

Substituting $K' = \frac{L}{W}\beta$ in Eq. (0-10) yields

$$e_n^2 = \left[\frac{8kT(1+\eta)}{3g_m} + \frac{KF}{2fC_{ox}L^2\beta} \right] \cdot \Delta f \ (V^2) \tag{0-11}$$

The equivalent input mean-square voltage-noise from Eq. (0-11) can be thought of as a voltage source connected to the gate of the MOS transistor.

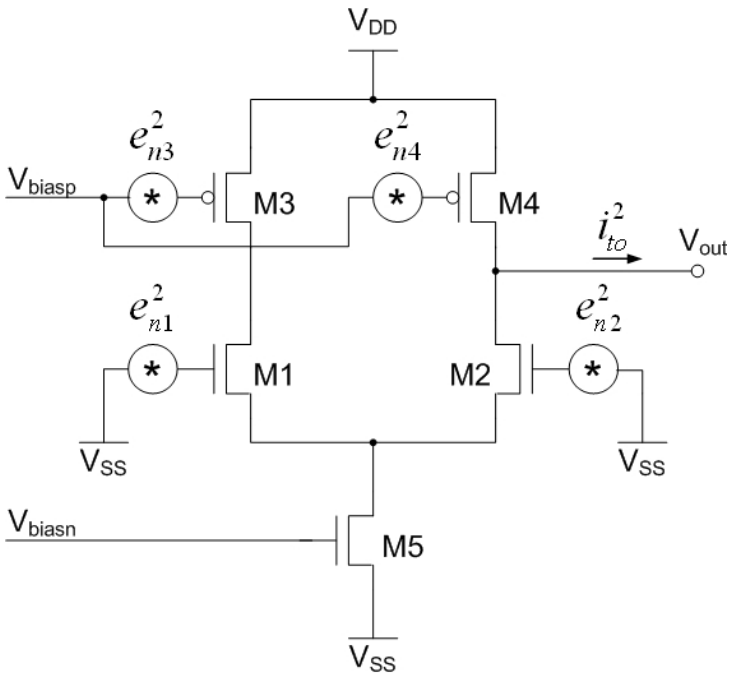


Figure 5-8 First preamplifier stage with equivalent input mean-square noise voltage at the gate of each transistor

Consider the first stage of the preamplifier, depicted on Figure 5-8. The equivalent noise sources e_{n1}^2 through e_{n4}^2 are connected to the gates of transistors *M1* through *M4*, respectively. Noise from the biasing circuit is ignored. The total output-noise current i_{to}^2 is found by summing each of the noise-current contributions.

$$i_{to}^2 = g_{m1}^2 e_{n1}^2 + g_{m2}^2 e_{n2}^2 + g_{m3}^2 e_{n3}^2 + g_{m4}^2 e_{n4}^2 \tag{0-12}$$

Since the equivalent output-noise current is expressed in terms of the equivalent input-noise voltages, we may use

$$i_{to}^2 = g_{m1}^2 e_{eq}^2 \tag{0-13}$$

to get

$$e_{eq}^2 = e_{n1}^2 + e_{n2}^2 + \left(\frac{g_{m3}}{g_{m1}} \right)^2 \left[e_{n3}^2 + e_{n4}^2 \right] \tag{0-14}$$

where we have assumed that $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$.Furthermore, if $e_{n1}^2 = e_{n2}^2$ and $e_{n3}^2 = e_{n4}^2$, Eq. (0-14) simplifies to

$$e_{eq}^2 = 2\left(e_{n1}^2 + \left(\frac{g_{m3}}{g_{m1}} \right)^2 e_{n3}^2 \right) \tag{0-15}$$

The equivalent-noise model is shown in Figure 5-9.

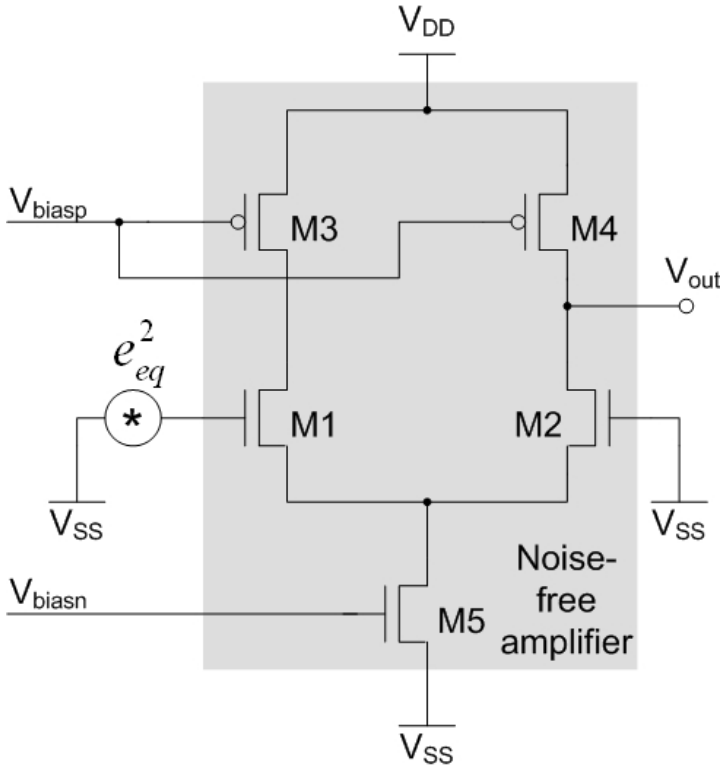


Figure 5-9 Equivalent-noise model of Figure 5-8.

Table 5-3 shows the thermal noise contribution, 1/f noise contribution and equivalent input mean-square voltage-noise of transistors *M1* through *M4*. Numerical values used for calculation are also shown in Table 5-3.

	M1, M2	M3, M4	Comments
L	$200nm$	$2\mu m$	Design parameter
g_m	$68.22\mu S$	$11.8\mu S$	From DC simulation
g_{mbs}	$7.538\mu S$	$3.981\mu S$	From DC simulation
$\eta = g_{mbs} / g_m$	0.110	0.337	
β	$852.9\mu A/V^2$	$16.09\mu A/V^2$	From DC simulation
Thermal noise contribution $\frac{8kT(1+\eta)}{3g_m}\ [V^2/Hz]$	$1.79761\cdot10^{-16}V^2/Hz$	$1.25179\cdot10^{-15}V^2/Hz$	Thermal noise is shown to be dominant over 1/f noise
1/f noise contribution $\frac{KF}{2fC_{ox}L^2\beta}\ [V^2/Hz]$	$5.57067\cdot10^{-18}V^2/Hz$	$2.9526\cdot10^{-18}V^2/Hz$	
e_n^2 with $\Delta f = 1Hz$	$1.85331\cdot10^{-16}V^2$	$1.25475\cdot10^{-15}V^2$	
e_n^2 with $\Delta f = 6MHz$ [12]	$1.11199\cdot10^{-9}V^2$	$7.52848\cdot10^{-9}V^2$	

Table 5-3 Thermal noise, 1/f noise and equivalent input mean-square voltage-noise of transistors M1 through M4 of first preamplifier stage.

From Eq. (0-15), with $\Delta f = (1Hz, 6MHz)$, the equivalent input mean-square voltage-noise of the first preamplifier becomes $e_{eq}^2 = (4.45743\cdot10^{-16}V^2, 2.67446\cdot10^{-9}V^2)$. The corresponding RMS value is $e_{eq}^{RMS} = \sqrt{e_{eq}^2} = (21.1nV, 51.7\mu V)$. Compare this to $0.5V_{LSB} = 219\mu V$. We conclude that the first preamplifier stage has a very good noise performance.

Of course, 1/f noise can be reduced by increasing transistor sizes W and L (See Eq. (0-10)). Unfortunately, this is not true for thermal noise, which is the dominant noise contribution. In fact, thermal noise is inversely proportional to g_m, which itself is proportional to W/L (if the transistor is in saturation). Consequently, decreasing L or increasing W would reduce thermal noise.

We apply the same procedure to determine the input-referred RMS noise voltage of the second and third preamplifier stage. Table 5-4 summarizes the input-referred RMS noise voltages of the three preamplifier stages for $\Delta f = 1Hz$ and $\Delta f = 6MHz$.

	e_{eq}^2		e_{eq}^{RMS}	
Preamplifier stage	$\Delta f = 1Hz$	$\Delta f = 6MHz$	$\Delta f = 1Hz$	$\Delta f = 6MHz$
1	$4.457\cdot10^{-16}V^2$	$2.674\cdot10^{-9}V^2$	$21.1nV$	$51.7\mu V$
2	$5.302\cdot10^{-16}V^2$	$3.180\cdot10^{-9}V^2$	$23.0nV$	$56.4\mu V$
3	$5.016\cdot10^{-16}V^2$	$3.010\cdot10^{-9}V^2$	$22.4nV$	$54.9\mu V$

Table 5-4 Input-referred RMS noise voltage of the three preamplifier stages.

Finally, the total noise voltage, referred to the input of the first preamplifier stage, is given by

[12] Consider the full-range sample. $2\cdot2.67MHz = 5.34MHz \approx 6MHz$

$$e_{total}^{RMS} = \sqrt{e_{eq1}^2 + \frac{e_{eq2}^2}{A_{v1}^2} + \frac{e_{eq3}^2}{A_{v1}^2 \cdot A_{v2}^2}} \tag{0-16}$$

Numerically, considering the case $\Delta f = 6MHz$,

$$e_{total}^{RMS} = \sqrt{\left(2.674 + \frac{3.18}{20.73^2} + \frac{3.01}{20.73^2 \cdot 20.02^2}\right) \cdot 10^{-9} V^2} = 51.78\mu V \tag{0-17}$$

$e_{total}^{RMS} = 51.78\mu V$ is still very small with respect to $0.5V_{LSB} = 219\mu V$. The input-referred noise voltage of stage 2 contributes very little to the total RMS noise voltage at the input of the comparator, and the one of stage 3 even less.

At the input of the comparator, the minimum signal we want to look at is about $200\mu V$. At the input of stage 2, this signal is already amplified by roughly 20, and at the input of stage 3 by 400. The minimum signal at the input of stages 2 and 3 is thus much bigger than the noise introduced by these stages.

5.3.5. Calculation of the Offset Voltage

The input-referred offset voltage of a differential pair with current-source loads, as depicted in Figure 5-10 is given by Eq. (5-17) [Razavi2001].

$$V_{OS,in} = \left\{ \frac{\left|V_{gs} - V_{th}\right|_P}{2} \left[\frac{\Delta(W/L)}{W/L}\right]_P + \Delta V_{th,P} \right\} \frac{g_{mP}}{g_{mN}} + \frac{(V_{gs} - V_{th})_N}{2} \left[\frac{\Delta(W/L)}{W/L}\right]_N + \Delta V_{th,N} \tag{0-18}$$

The causes of the offset voltage are:

- Mismatch of the transistor sizes in the differential pair
- Mismatch of the transistor sizes in the current-source loads
- Mismatch of threshold voltage of transistors in the differential pair
- Mismatch of threshold voltage of transistors in the current-source load

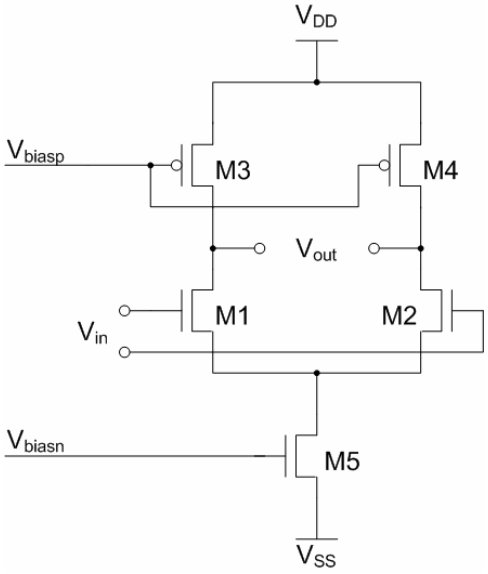


Figure 5-10 Differential pair with current-source loads.

In UMC $0.18\mu m$ CMOS technology, transistor dimension can be defined on silicon with a precision of $10nm$. Nominal, minimum and maximum transistor dimensions of preamplifier stage 1 are given in Table 5-5.

Dimension	Nominal value	Minimum value	Maximum value
L1, L2	$200nm$	$190nm$	$210nm$
L3, L4	$2\mu m$	$1.99\mu m$	$2.01\mu m$
W1, W2	$500nm$	$490nm$	$510nm$
W3, W4	$700nm$	$690nm$	$710nm$

Table 5-5 Nominal, minimum and maximum values of the 8 transistor dimensions.

$$\Delta(W/L)_{N/P,\max} = (W/L)_{N/P,\max} - (W/L)_{N/P,\min} \tag{0-19}$$

$$\Delta(W/L)_{N,\max} = \frac{510}{190} - \frac{490}{210} = 0.351 \tag{0-20}$$

$$\Delta(W/L)_{P,\max} = \frac{710}{1'990} - \frac{690}{2'010} = 0.0135 \tag{0-21}$$

$$\left[\frac{\Delta(W/L)}{W/L}\right]_N = \frac{0.351}{2.5} = 0.1404 \tag{0-22}$$

$$\left[\frac{\Delta(W/L)}{W/L}\right]_P = \frac{0.0135}{0.35} = 0.0386 \tag{0-23}$$

As for $\Delta V_{th,N/P}$, we consult UMC's "0.18um Mixed-Mode 1.8V Process Matching Report" [UMC1.8VPMR]. UMC defines $DVth = |Vth1 - Vth2|$, where *Vth1* is the threshold voltage of the first device and *Vth2* the threshold voltage of the adjacent device. *rDVth* is the standard deviation of *DVth*. For NMOS transistors with W/L=10um/0.18um – the closest data point to W/L=0.5um/0.2um – and a gate spacing of 10um, rDVth=3.8380mV. For PMOS transistors with W/L=10um/1.5um – the closest data point to W/L=0.7um/2um – and a gate spacing of 10um, rDVth=0.5930mV.

The following inequalities are true with a probability of 99.73%:

- $DVthn < 3 \cdot rDVthn = 11.514mV$
- $DVthp < 3 \cdot rDVthp = 1.779mV$

Considering 3σ accuracy, $\Delta V_{th,N} = 11.514mV$ and $\Delta V_{th,P} = 1.779mV$.

The quantities in Table 5-6 have been determined from DC simulation of preamplifier stage 1.

$V_{gs,N}$	$587.5mV$	$V_{gs,P}$	$-1.245V$
$V_{th,N}$	$525.4mV$	$V_{th,P}$	$-491.1mV$
g_{mN}	$68.22\mu S$	g_{mP}	$11.8\mu S$

Table 5-6 Numerical values from DC simulation for calculating offset voltage of preamplifier stage 1

Plugging all numerical values into Eq. (0-18),

$$V_{OS,in} = 18.6979mV \tag{0-24}$$

Since mismatches are independent statistical variables, the sign of V_{OS} does not matter. On a manufactured chip, it can be either positive or negative. The contribution of the pMOS devices to the offset voltage is proportional to g_{mP} / g_{mN}. Here, the contribution of nMOS devices is dominant, as $g_{mP} / g_{mN} = 0.173$. The mismatch of the threshold voltage of the transistors in the differential pair contributes directly, i.e. without a scaling factor to the offset voltage. Typically, the input-referred offset voltage of a CMOS differential amplifier is 5-20mV [Allen2002].

The offset voltage can be referred to the output of the differential amplifier.

$$V_{OS,out} = A_{v1} \cdot V_{OS,in} = 389.724mV \tag{0-25}$$

The next section presents a circuit to sample and store the output-referred offset voltage.

5.3.6. Offset cancellation

For every bit decision to be correct, it is essential to minimize the comparator's offset voltage. The gain of the preamplifier has been designed to overcome the offset voltage of the latch, as it is rather complicated to realize offset-compensated latches. There exist various offset-cancellation techniques for amplifiers, however. They can be classified as input-offset cancellation or output-offset cancellation.

When using input-offset cancellation, no additional capacitor was required for the first preamplifier stage. The offset voltage could be sampled and stored on the existing capacitor array. However, input-offset cancellation results in a residual offset voltage of V_{OS} / A_{v1}, where V_{OS} is the initial offset voltage. Unfortunately, input-offset cancellation is not good enough, as $18.6979mV / 20.73 = 902\mu V$.

Output-offset cancellation is used instead. One limitation of output-offset cancellation is that the amplifier mustn't saturate. Because the amplifiers will saturate for sure, offset cancellation needs to be done before each bit decision, i.e. 12 times for one A/D conversion.

Figure 5-11 shows the clock signal generator, while Figure 5-12 depicts the preamplifier with output-offset cancellation circuitry. The circuit containing tow cross-coupled NAND gates with delayed outputs generates the two non-overlapping signals S1 and AZ0 (see Figure 5-13). Whenever S1 is high, the actual input to the comparator is chosen, which is $V_{X1/2}$ (see Figure 4-6). During the auto-zeroing phase, AZ0 is high and shorts the input of the comparator to ground. If S1 and AZ0 would be high at the same time, charge from the capacitor array would flow into ground, a fatal malfunction.

At the start-up of the ADC, all capacitors used for offset-cancellation are shorted while all AZi signals are high, in order to bring the circuit into a known state. In fact, signal *rst* is an active low reset signal.

Let us size the capacitors sampling the output-referred offset voltage: The bigger the capacitors, the more accurate the offset cancellation. However, the available time to charge the capacitors to the offset voltage, about 17.8ns, limits their size. With 250*fF*, the offset voltage is fully sampled before the pre-amplifier becomes transparent again.

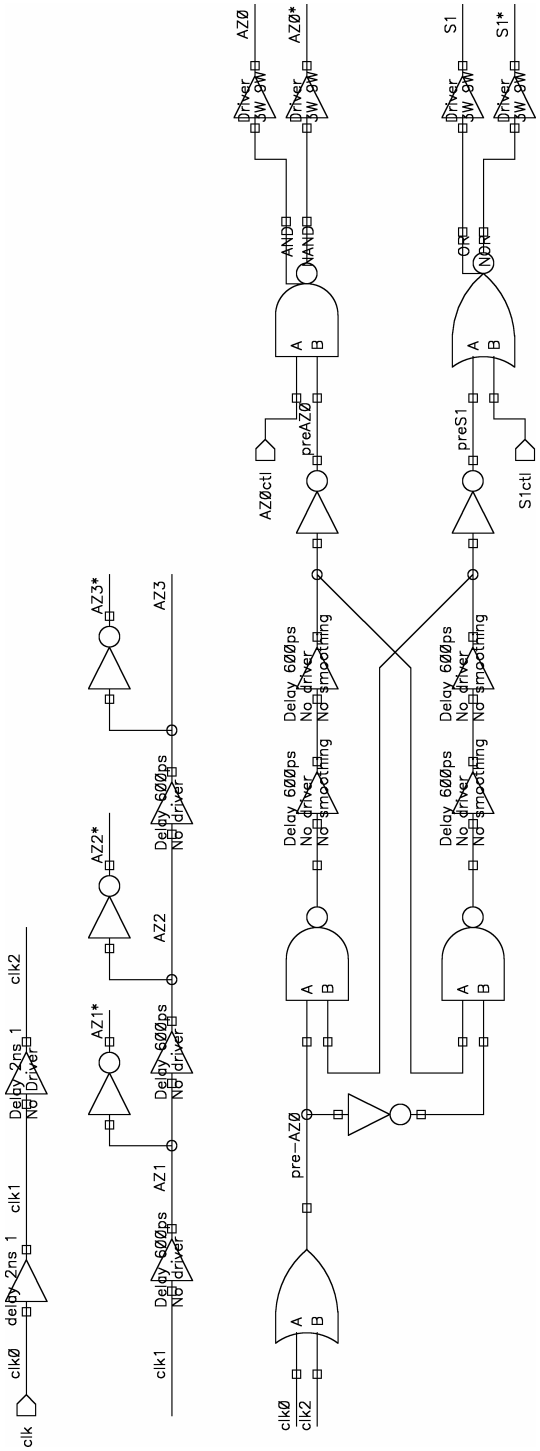


Figure 5-11 Clock generation circuit for offset cancellation. AZ0 and S1 are non-overlapping signals, choosing the common-mode voltage during the auto-zeroing phase and the actual input to the comparator, respectively. The generated signals are shown on Figure 5-13.

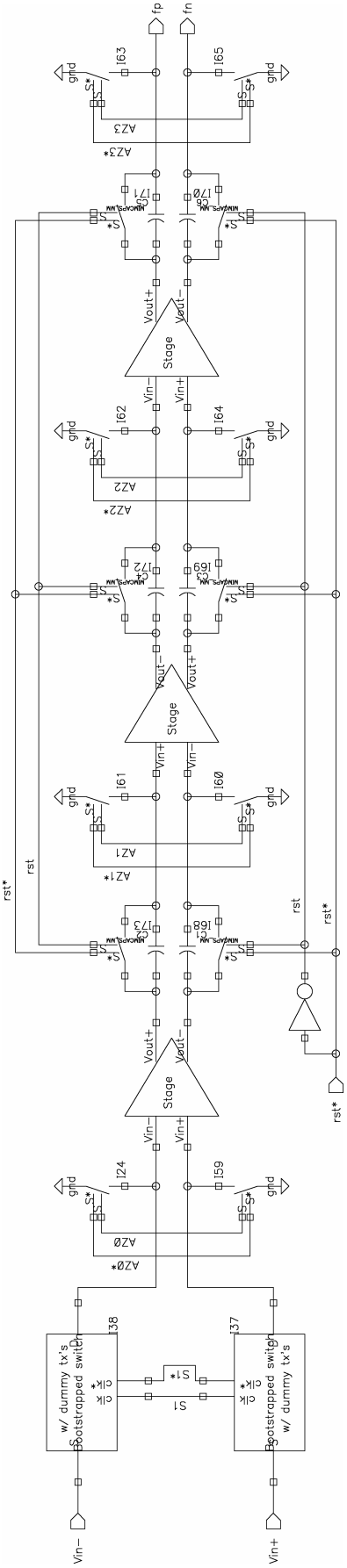


Figure 5-12 Offset cancellation.

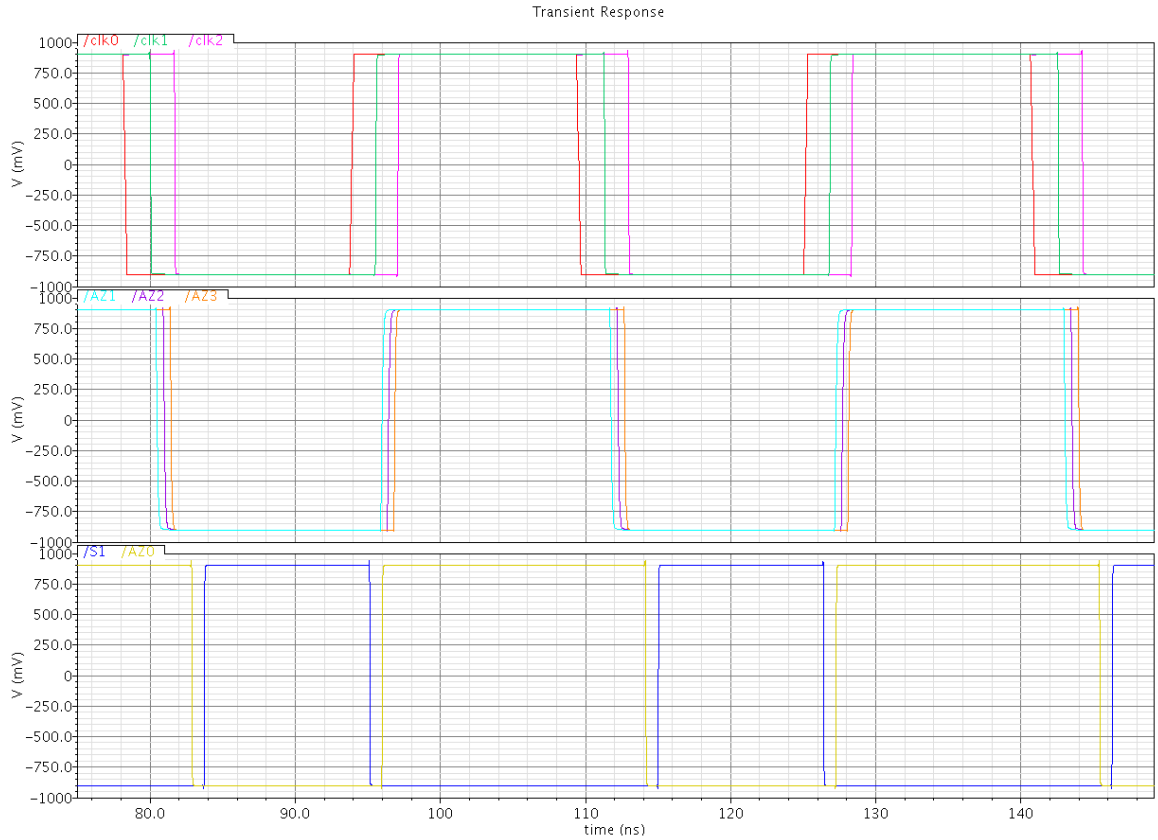


Figure 5-13 Clock signals used to control the offset cancellation circuit.

To test the implemented offset cancellation technique and estimate the residual offset voltage by simulation, a voltage source modeling the input-referred offset voltage is inserted at either the positive or the negative input of each preamplifier stage. The residual output-referred offset voltage of the first pre-amplifier stage is approximately $500\mu V$. Referred to the input, this value becomes $25\mu V$, what is well below $0.5V_{LSB} = 219\mu V$.

If a voltage with absolute value equal to or bigger than $25\mu V$ is applied to the ADC's input, the value of the MSB or sign bit is determined correctly. In the case where the absolute value of the input voltage is smaller than $25\mu V$, the response of the comparator can not be predicted by simulation. In fact, transistor mismatches determine the comparator's response in this case. Even though the response cannot be predicted, it will always be the same for a given chip. It may vary from chip to chip, however.

5.3.7. Biasing: Beta-multiplier

Figure 5-14 shows the beta-multiplier circuit used for biasing the preamplifier. It can avoid variations in the supply voltages, but it cannot avoid variations in temperature. The desired biasing current is reached by sizing the resistor. $R = 6.28k\Omega$ results in a current of $10\mu V$ through transistor M36.

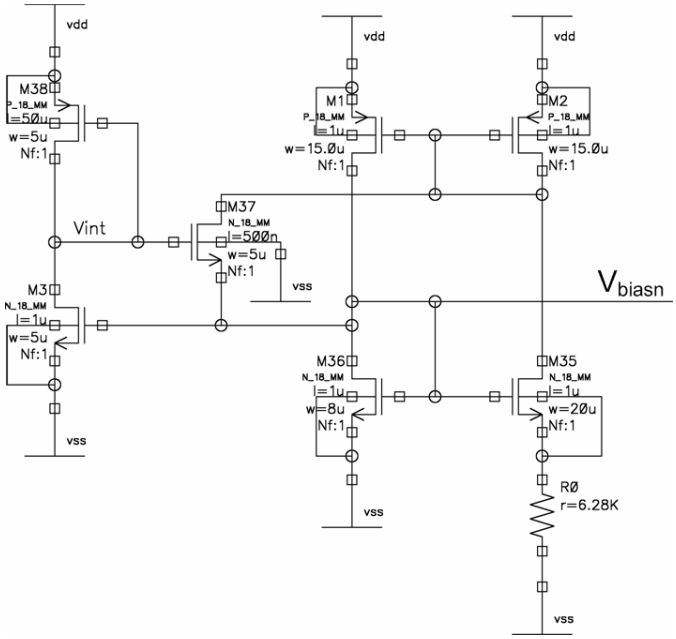


Figure 5-14 Beta-multiplier: circuit at transistor level

5.4. Latch

In order to establish full logic levels and synchronize the instant a decision is taken with other blocks, the back-end of the comparator consists of a latch. The output nodes *iVout* and *iVout** (see Figure 5-15) are precharged to V_{SS} when the clock is low. To prevent static current flow through the two branches of the latch, a pMOS transistor (M0) controlled by *clk** cuts off the cross-coupled inverter pair from V_{DD} during the precharge phase. The amplified signal (output of preamplifier stage 3) is applied to the latch through transistors M24 and M25, which provide an additional gain. Notice that the pre-amplified signal easily overcomes the offset voltage of the latch ($200\mu V \cdot 20^3 = 1.6V$).

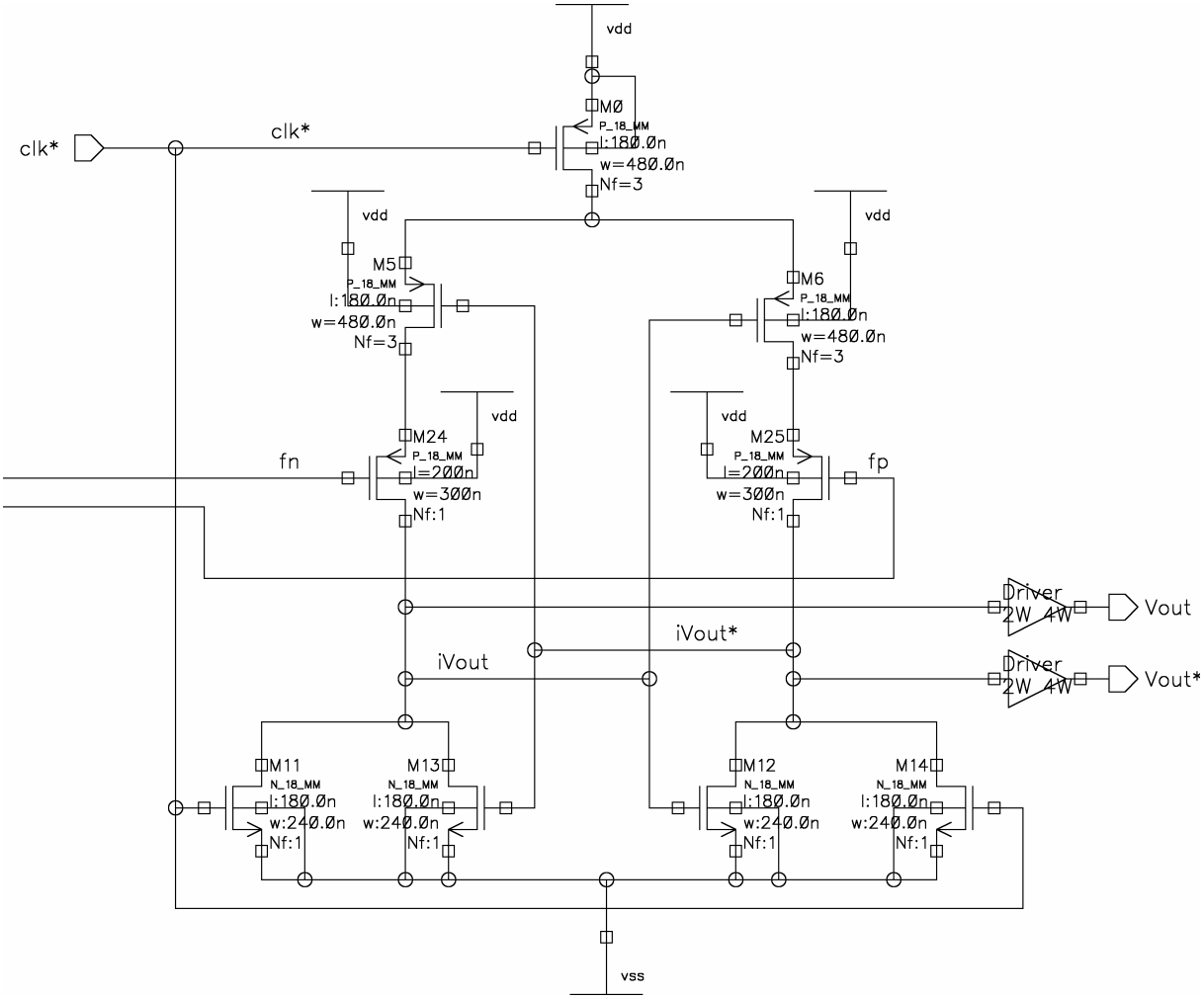


Figure 5-15 Latch: circuit at transistor level.

It is essential for the latch to be correctly unbalanced that both output nodes *iVout* and *iVout** see the same load capacitance. Having two identical output buffers, this condition is satisfied. (Note that *Vout** drives only one DFF (*2MUX-DFFP*), while *Vout* drives 11 DFFs (10 *2MUX-DFFPSRSS* and 1 *DFFPSRSS*), what resulted in severely differently charged output nodes if no buffers were introduced.)

The latch makes a decision at each rising edge of clock *clk0*. Its outputs must reach full logic levels before the rising edge of clock *clk1*, which synchronizes the output registers and is delayed by *1.786ns* with respect to *clk0*. See *Chapter 7 SAR control logic* and *Chapter 9 Delay elements* for details on timing. Briefly, the transitions of the outputs from the pre-charge level (*Vss*) to full logic levels must occur in less than *1.786ns*. With the output buffers in use, these transitions are made in less than *1.1ns* if both *Vout* and *Vout** are loaded with *100fF*, as can be seen in Figure 5-17.

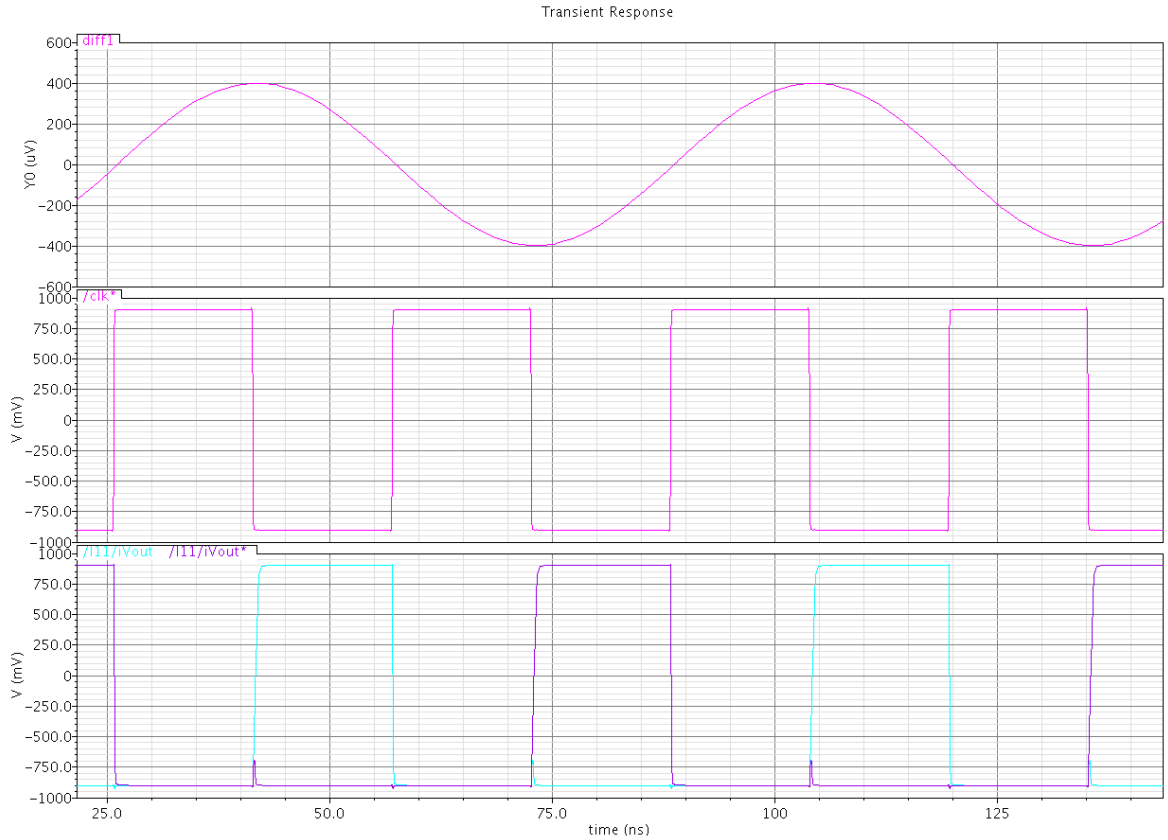


Figure 5-16 Time response of the latch. Whenever clk* is high, the output nodes are reset. At a falling edge of clk*, the latch makes a decision. *diff1* is the minimum $200\mu V$ input signal. If the input signal is positive, iVout goes high. If the input signal is negative, iVout remains low and iVout* goes high.

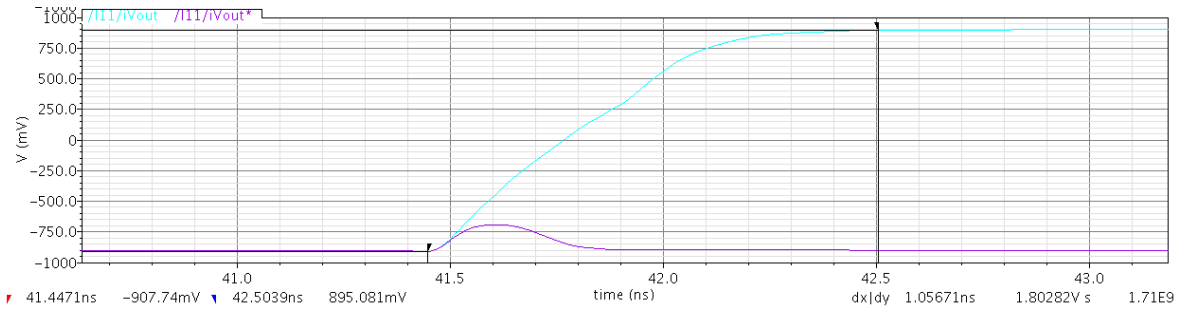


Figure 5-17 Time response of latch: low-to-high transition of node *iVout*.

The gain of the latch consists of two parts:

- Gain of differential input pair formed by transistors M24 and M25
- Gain of the cross-coupled inverters formed by transistors (M5 & M13) and (M6 & M12)

The gain of the differential pair is given as

$$A_1 = \frac{g_{m25}}{g_{ds25} + g_{ds12}} = \frac{35.7\mu S}{1.072\mu S + 4.18\mu S} = 6.79 \qquad (0\text{-}26)$$

The gain of the cross-coupled inverters is found from the Voltage Transfer Characteristic (VTC). To obtain the VTC, put clk*='0', so that M11 and M14 are cut off and M0 is in conduction, and tie the gates of M24 and M25 to ground. The VTC shown in Figure 5-18 is obtained from sweeping iVout* from -900mV to 900mV and plotting iVout versus iVout*. The VTC is shown in red, while its

derivative is shown in blue. The maximum gain is about -15. The same VTC is obtained when sweeping iVout* from 900mV to -900mV.

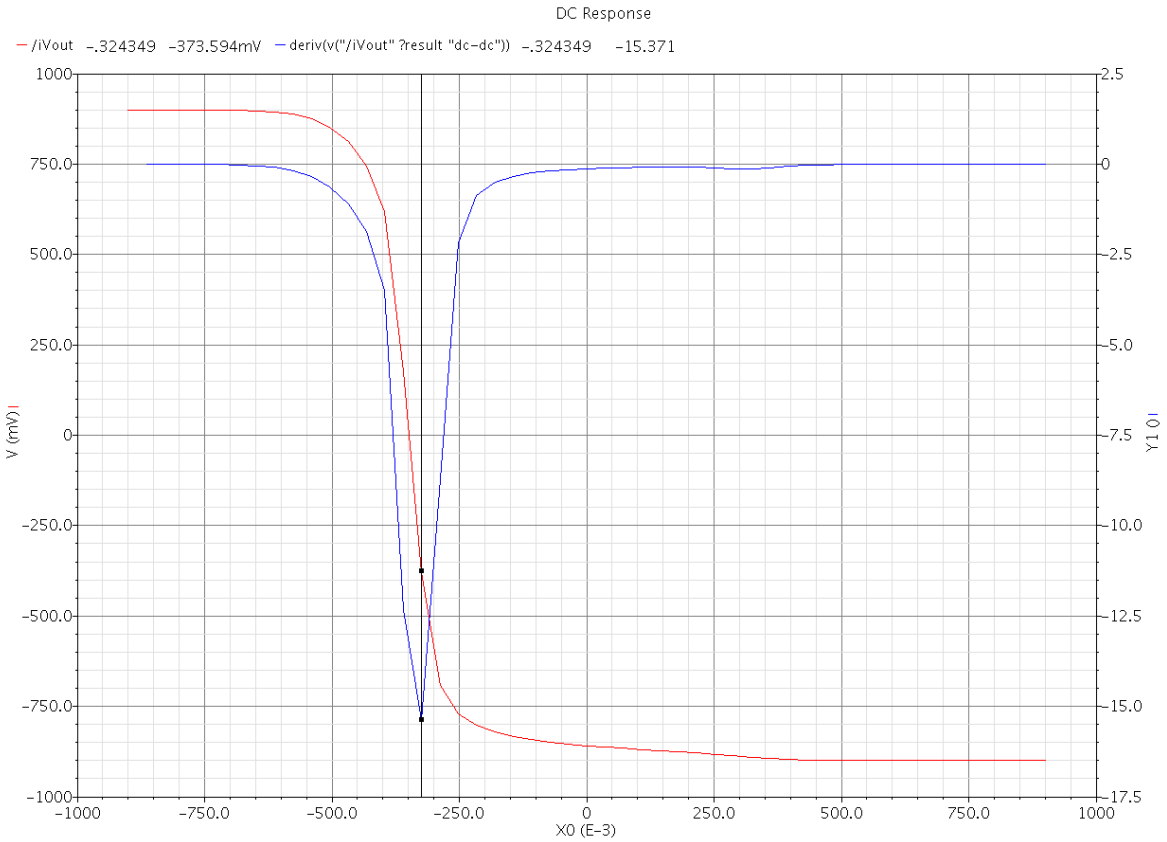


Figure 5-18 Voltage Transfer Characteristic (VTC) of latch.

In conclusion, the gain of the latch is

$$A_{Latch} = 6.79 \cdot 15 = 101.25 \tag{0-27}$$

The gain of the comparator is thus

$$A_{Comp} = 20^3 \cdot 101.25 = 810'000 \tag{0-28}$$

This is largely enough.

6. Split capacitor array

6.1. Topology of capacitor array

A common implementation of SC SAR ADCs uses a binary-weighted capacitor array. For binary-weighted capacitor arrays, however, area and power increase exponentially with resolution. In fact, N-bit resolution requires 2^N unit capacitors.

Split capacitor arrays as well as C-2C ladders reduce the total capacitance, thereby reducing area and power. However, the parasitic bottom-plate capacitance of series capacitors affects the linearity of the ADC. If the ratio of bottom-plate capacitance over nominal capacitance is precisely known, this non-linearity problem can be dealt with during the design phase by scaling some of the unit capacitors [Cong2001, Cong2000]. Another approach consists in shielding the series capacitors.

UMC $0.18\mu m$ CMOS technology comes with a Metal/Metal Capacitor (MMC) module, also referred to as Metal Insulator Metal (MIM) capacitor module. For a lower bottom-plate parasitic capacitance, the MIM module can be inserted between the second-last and last (top) metal layers, i.e. M5 and M6 [UMCCapChar]. A MIM capacitor is then built as parallel plate capacitor with M5 and the MIM layer. [UMCCapChar], a UMC MIM capacitor characterization report gives following MIM capacitance values.

Minimum	Typical	Maximum
$0.85\,fF/\mu m^2$	$1.00\,fF/\mu m^2$	$1.15\,fF/\mu m^2$

Table 6-1 MIM capacitance values

After many considerations like kT/C noise, capacitor matching and timing presented in *Section 6.2 Unit capacitor sizing*, a unit capacitor of $C_u = 250\,fF$ has been chosen. UMC's MIM capacitor model MIMCAPS_MM calculates a capacitance of 249.9336fF for a square MIM capacitor with $W = L = 15.66\mu m$. As UMC's resolution is $0.01\mu um$, this is the closest we can get to 250*fF* for a square MIM capacitor.

The parasitic capacitance C_p between M5 and the substrate has 2 components.

1) C_{p-p} Parallel plate capacitance unit: $fF/\mu m^2$
2) C_f Fringing capacitance to substrate unit: $fF/\mu m/side$

Notice that coupling capacitances to adjacent conductors are not relevant here, as they are almost the same for each unit capacitor when using appropriate layout techniques including dummy unit capacitors. Minimum, typical and maximum values for C_{p-p} and C_f are reported in capacitance look-up tables [CapLookUpTable]. In a worst-case scenario, we are interested in the maximum values. Assuming same area as for the unit capacitor, i.e. $W \cdot L = 15.66^2\,\mu m^2 = 245.2356\mu m^2$, the parasitic parallel plate capacitance is $C_{p-p} = 1.604\,fF$. Considering 4 fringing capacitances over a side length of $15.66\mu m$ each, $C_f = 201.6aF$. The parasitic bottom-plate capacitances of the unit capacitor sum up to $C_p = C_{p-p} + C_f = 1.8056\,fF$.

The ratio of the bottom-plate parasitic capacitance to the nominal value of the unit capacitor is thus $\gamma = \frac{C_p}{C_u} = \frac{1.8056\,fF}{249.9336\,fF} = 7.224 \cdot 10^{-3} = 0.7224\%$. This result is pretty good! Parallel plate capacitors built with standard metal layers have ratios of 20-40% [Cong2000].

Because the MSB is already determined by the sign of the sampled voltage, only 11 parallel capacitors are switched from ground to the reference voltage and eventually back to ground during a conversion. However, an additional parallel capacitor C_e, equal to the unit capacitor needs to be inserted to divide the reference voltage by exactly two at each successive bit cycling step [Martin1997].

In the following, we consider different arrangements of the 12 parallel capacitors, each requiring a different number of series capacitors. A purely binary-weighted capacitor array without a series capacitor can clearly not be used, due to excessively large area, power consumption and cost. Splitting the purely binary-weighted capacitor array in two parts of approximately equal total capacitance leads to the arrangement show in Figure 6-1. For the size of the single series capacitor C_{S1}, refer to *Section 6.3 Series capacitor sizing*. Figure 6-2 and Figure 6-3 show arrangements with 2 and 3 series capacitors, respectively. Going on splitting up binary-weighted capacitor arrays results in the so-called C-2C ladder as shown in Figure 6-4.

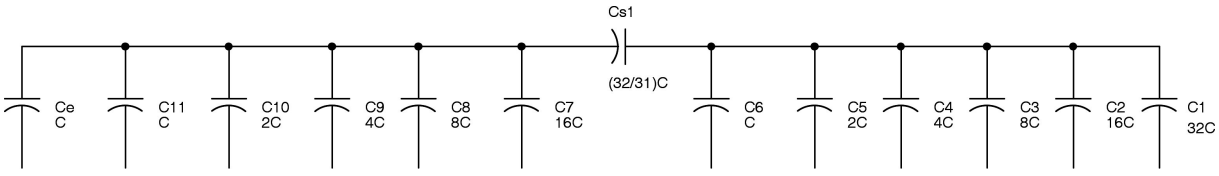


Figure 6-1 Two sub binary-weighted capacitor arrays, one series capacitor (2bw1Cs)

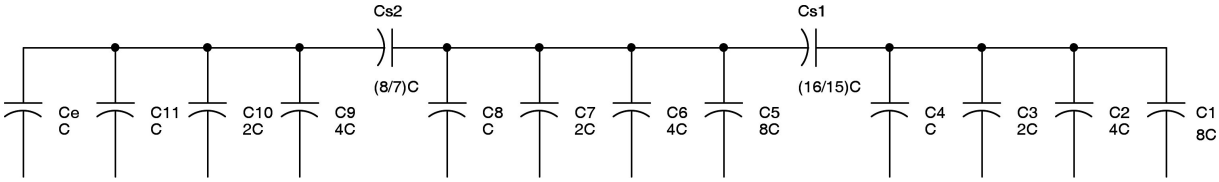


Figure 6-2 Three sub binary-weighted capacitor arrays, two series capacitors (3bw2Cs)

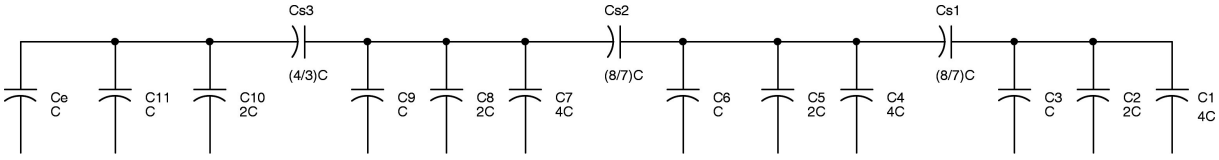


Figure 6-3 Four sub binary-weighted capacitor arrays, three series capacitors (4bw3Cs)

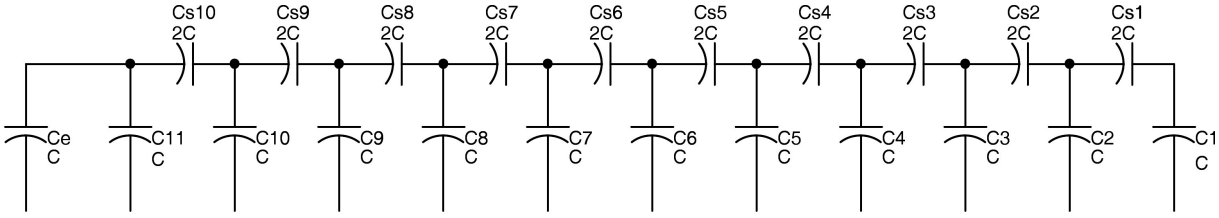


Figure 6-4 C-2C ladder

As primary design criterion to choose one out of the many possible capacitor arrangements, we look at how capacitor mismatch affects the DACs accuracy. Area is considered the second most important decision criterion. First of all, assume that the capacitor array shown in Figure 6-1 is used as DAC. At

the first step of a D/A conversion, all the capacitors except the MSB capacitor C_1 are connected to ground, while C_1 is connected to the positive reference voltage $V_{refp} = 900mV$ (Figure 6-5). The same situation occurs in the ADC core if a zero input signal is converted. Ideally, if there was no capacitor mismatch, $V_X^{ideal} = V_{refp}/2 = 450mV$. Due to capacitor mismatch, the voltage at node V_X varies. We define $\Delta V_X = V_X^{ideal} - V_X^{non-ideal}$.

Intuitively, the maximum ΔV_X occurs at the first step of a conversion. In fact, it is assumed that all the capacitors are built from unit capacitors, which follow a Gaussian distribution. Of course, the MSB capacitor is the biggest capacitor built from the highest number of unit capacitors and can consequently have the highest absolute uncertainty. Having the highest absolute uncertainty, it affects the capacitive voltage division the most, what results in a maximum ΔV_X. Lin claims the same result in [Lin2005]: "The maximum error voltage occurs at the switch combination 1000…0, i.e. MSB equal to 1 and all other bits equal to 0." A similar statement is mad in [Bechen2006]: "The MSB capacitor has the most deleterious effect on the signal-to-noise and distortion ratio (SNDR)."

The unit capacitors deviate from their nominal value due to mismatch. It is assumed that they follow a Gaussian distribution, characterized by the mean value μ_{Cu} and a standard deviation σ_{Cu}. From [UMCCapChar], if a capacitor area of $15 \cdot 15 \mu m^2$ is considered, $\mu_{Cu} = 225 fF$ and $\sigma_{Cu} = 0.14535 fF$. Of course, the bigger the capacitor, the smaller $\Delta C / C$. [UMCCapChar] also shows that if the spacing between capacitors decreases, $\Delta C / C$ improves. Figure 6-7 (1) shows a typical histogram of C_{unit} and the corresponding

R[13] is used to compute the distribution of the voltage at node V_X, starting from the Gaussian distribution of the unit capacitors. It is assumed that each unit capacitor is an independent random variable. 1000 data points are taken, i.e. each unit capacitor is sampled 1000 times. C_1 is the sum of 32 independent unit capacitors; its distribution is shown in Figure 6-7 (2). From statistical computing, $\mu_{C1} = 32\mu_{Cu}$ and $\sigma_{C1} = \sqrt{32(\sigma_{Cu})^2}$. It is a useful fact that the standard deviation does not scale linearly when adding up 32 unit capacitors. In fact, if $\sigma_{Cu} = 0.14535 fF$, then $\sigma_{C1} = 0.8105 fF$. (This observation would lead us to build each unit capacitor from even smaller capacitors, in order to improve matching properties. However, the even smaller capacitors have worse matching properties, what might destroy the statistical matching improvement effect.) Figure 6-7 (3) shows the Gaussian distribution of C_S. In order to calculate V_X, the circuit of Figure 6-5 is simplified to the one shown in Figure 6-6.

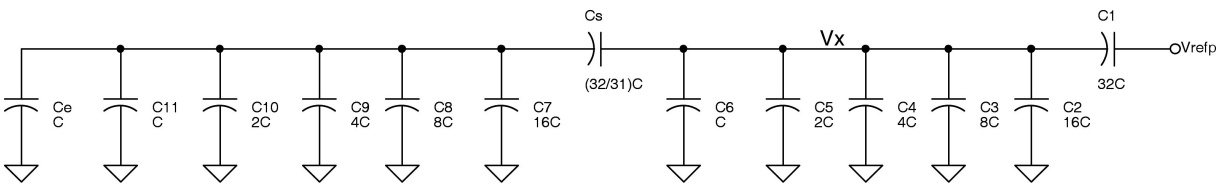


Figure 6-5 The *2bw1Cs* capacitor array used as DAC, at the first step of the conversion.

[13] R version 2.7.1, © 2008 The R Foundation for Statistical Computing

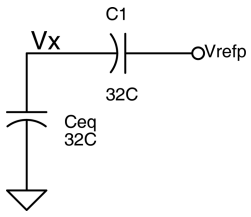


Figure 6-6 Equivalent circuit of the circuit shown in Figure **6-5**.

$$C_{eq1} = C_e + \sum_{k=7}^{11} C_k$$

$$C_{eq2} = \sum_{k=2}^{6} C_k$$

$$C_{eq} = \frac{C_{eq1} \cdot C_S}{C_{eq1} + C_S} + C_{eq2} = \frac{\left(C_e + \sum_{k=7}^{11} C_k \right) \cdot C_S}{C_e + \sum_{k=7}^{11} C_k + C_S} + \sum_{k=2}^{6} C_k$$

Finally, V_X is obtained as

$$V_X = \frac{C_1}{C_{eq} + C_1} \cdot V_{refp} = \frac{C_1}{\frac{\left(C_e + \sum_{k=7}^{11} C_k \right) \cdot C_S}{C_e + \sum_{k=7}^{11} C_k + C_S} + \sum_{k=2}^{6} C_k + C_1} \cdot V_{refp}$$

Figure 6-7 (4) shows the distribution of V_X.

$$\mu_{Vx} = 450.0018mV$$

$$3\sigma_{Vx} = 107.8259\mu V$$

The probability that $V_X \in [\mu_{Vx} - 3\sigma_{Vx}, \mu_{Vx} + 3\sigma_{Vx}]$ is 99.73%, and $3\sigma_{Vx} < 0.5V_{LSB} = 219\mu V$. In conclusion to this analysis, the *2bw1Cs* capacitor array of Figure 6-1, assembled from $15 \cdot 15\mu m^2$ unit capacitors is (more than) 12-bit accurate.

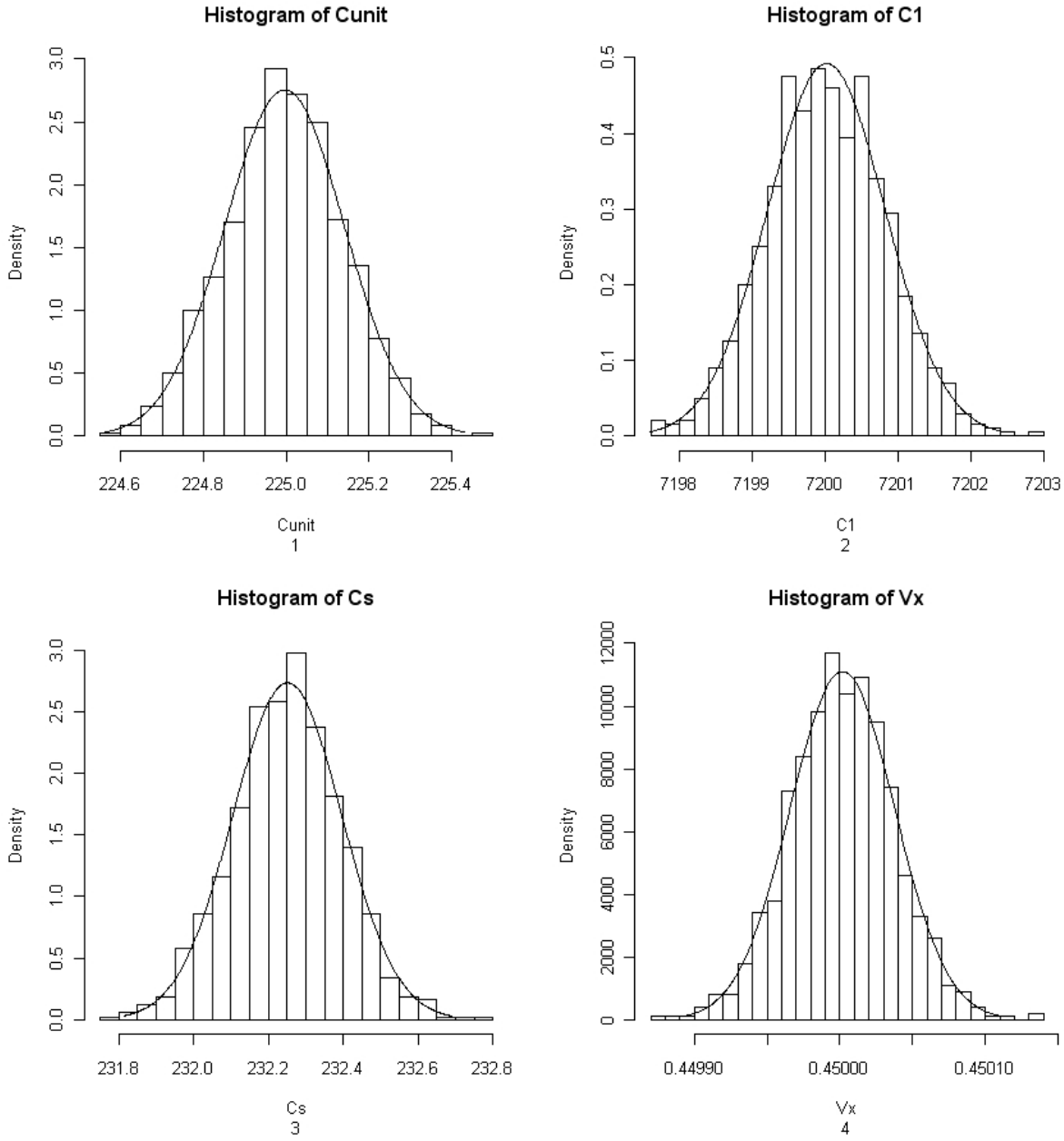


Figure 6-7 Histogram of (1) C_{unit}, (2) C_1, (3) C_{S1} and (4) V_X

Following data corresponds to Figure 6-7.

muVx=0.4500018
sigmaVx=3.594195e-05
3*sigmaVx=0.0001078259
muCunit=224.9964
sigmaCunit=0.1448193
muC1=7200.017
sigmaC1=0.8105068
muCs=232.2506
sigmaCs=0.1458274

The same analysis is made for the *3bw2Cs*, *4bw3Cs* and *C-2C* capacitor arrays of Figure 6-2, Figure 6-3 and Figure 6-4, respectively.

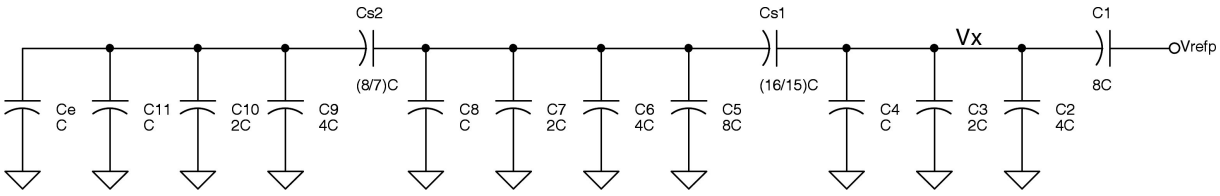


Figure 6-8 The *3bw2Cs* capacitor array used as DAC, at the first step of the conversion

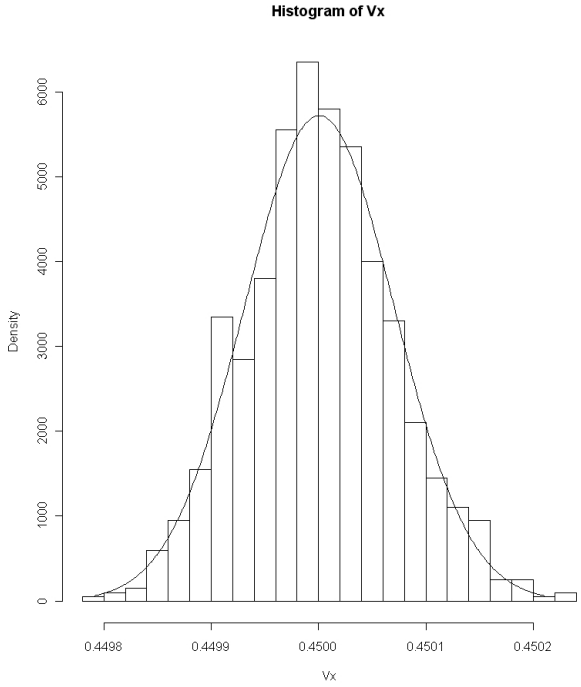


Figure 6-9 Histogram of V_X for the *3bw2Cs* capacitor array

Following data corresponds to Figure 6-9.

muVx=0.4500008
sigmaVx=6.973958e-05
3*sigmaVx=0.0002092187

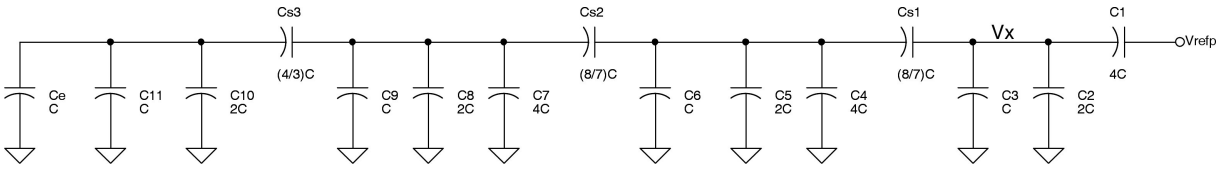


Figure 6-10 The *4bw3Cs* capacitor array used as DAC, at the first step of the conversion

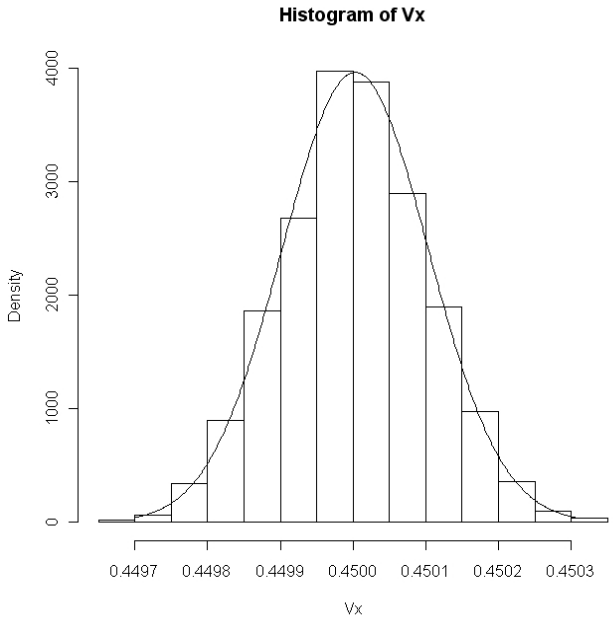


Figure 6-11 Histogram of V_X for the *4bw3Cs* capacitor array

Following data corresponds to Figure 6-11

muVx=0.450003
sigmaVx=0.0001005944
3*sigmaVx=0.0003017832

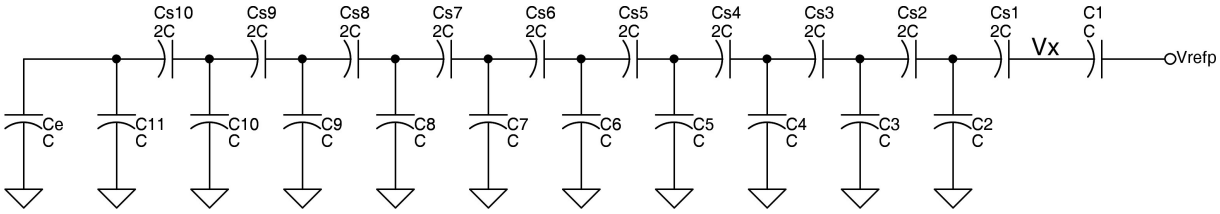


Figure 6-12 The C-2C ladder used as DAC, at the first step of the conversion

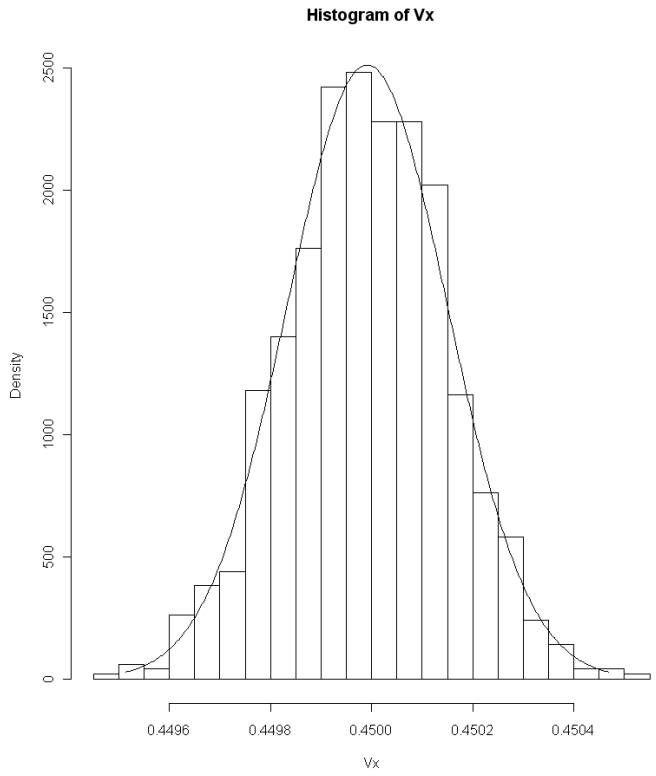


Figure 6-13 Histogram of V_X for the C-2C ladder

Following data corresponds to Figure 6-13.

muVx=0.4499913
sigmaVx=0.0001589060
3*sigmaVx=0.0004767179

σ_{Vx} increases with the number of series capacitors. For the the *3bw2Cs* capacitor array, $3\sigma_{Vx} = 209.2187\mu V$, what is still slightly lower than $0.5V_{LSB} = 219\mu V$. For the *4bw3Cs* and *C-2C* capacitor arrays, $3\sigma_{Vx} > 0.5V_{LSB}$. They are not accurate enough if $15 \cdot 15\mu m^2$ MIM unit capacitors are used.

The *2bw1Cs* capacitor array has a total capacitance of $96.03C_u$, whereas the *3bw1Cs* capacitor array has a total capacitance of $40.21C_u$. For very good accuracy, the *2bw1Cs* capacitor array must be used. Adopting the *3bw1Cs* capacitor array decreases area by more than half while keeping 12-bit accuracy.

The value of the unit capacitor and series capacitor are determined in the following two subchapters.

6.2. Unit capacitor sizing

The unit capacitor sizing must consider kT/C noise, 12-bit accurate matching, timing and power consumption. Of course, to decrease power consumption and increase speed, the unit capacitor should be as small as possible. On the other hand, to improve MIM capacitor matching, noise immunity and consequently the ADC's accuracy, the unit capacitor must be as big as possible. The design approach chosen here gives priority to accuracy. Indeed, the minimum unit capacitor size, dictated by either kT/C noise or capacitor matching, is determined first. It is then shown that timing requirements are met with the found unit capacitance value and that the power consumption is reasonably small.

6.2.1. kT/C noise

Let us consider a unit capacitor in the split binary-weighted capacitor array and its neighboring elements. The bottom plate of each parallel capacitor is connected to a separate switch, while the top plates of unit capacitors in each sub binary-weighted capacitor arrays are connected together. We look at one unitary cell consisting of one unit capacitor and one switch. When the switch is on, its transistor(s) can be modeled as resistor(s). The resulting equivalent circuit is a simple RC circuit (Figure 6-14). Thermal noise (Johnson noise) from the resistor affects the voltage at the capacitor's terminal; the capacitor itself does not introduce any noise. The output-referred RMS noise voltage in a RC circuit is given by $V_{onoise\ ,RMS} = \sqrt{\frac{kT}{C}}$ [Baker2005]. Equivalently, $C_{unit} = \frac{kT}{V_{onoise,RMS}^2}$.

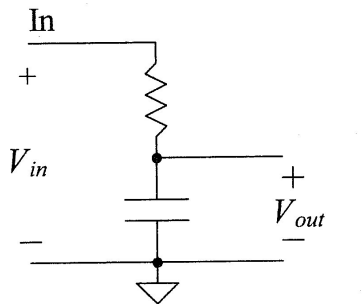


Figure 6-14 Equivalent RC circuit [Baker2005]

As the peak-to-peak value of the thermal noise will be larger than the RMS value, $V_{onoise,RMS}$ must be well below $0.5V_{LSB}$. We impose $V_{onoise,RMS} < 150\mu V$.

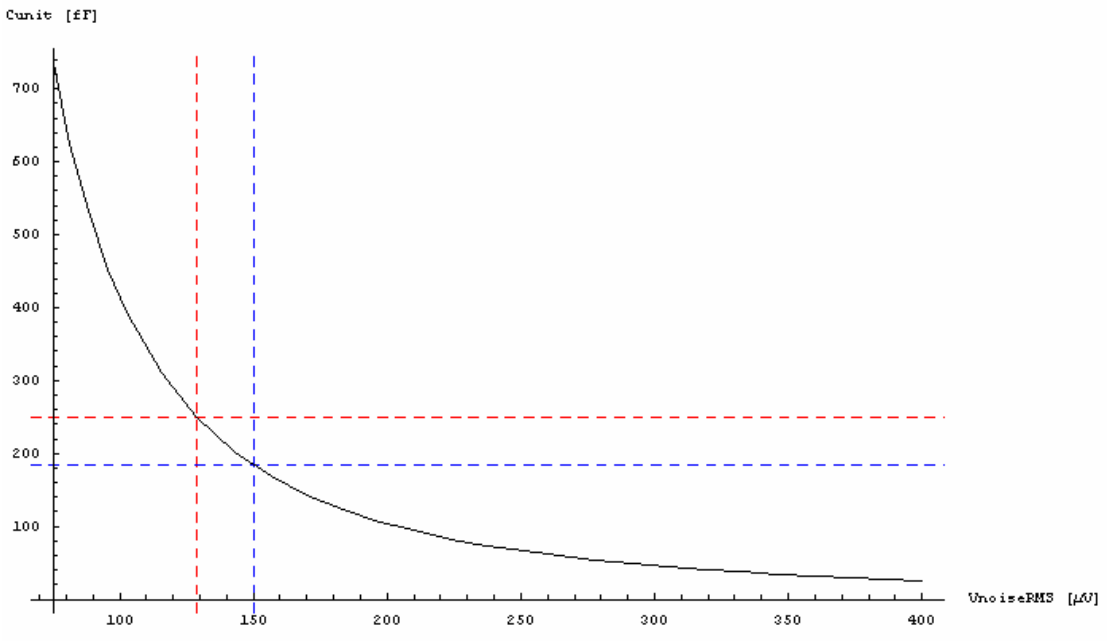


Figure 6-15 C_{unit} as a function of $V_{onoise,RMS}$

For $V_{onoise,RMS} = 150\mu V$, $C_{unit} = 184fF$ (blue gridlines). Choosing $C_{unit} = 250fF$, the RMS noise value is below $128.686\mu V$ (red gridlines).

6.2.2. Matching

It has been shown in Section 6.1 that the *3bw1Cs* capacitor array is 12-bit accurate when assembled from $15 \cdot 15 \mu m^2$ MIM unit capacitors. Using slightly bigger unit capacitors, the accuracy is improved. $15.66 \cdot 15.66 \mu m^2$ MIM capacitors have a capacitance of $C_u = 250\,fF$.

Matching requirements are more restricting than kT/C noise.

6.2.3. Timing

From many transient simulations, it has been seen that RC constants are small enough. Voltages on capacitors settle easily within $\pm 0.5 V_{LSB}$ of their final value. R is the on-resistance of switches.

6.3. Series capacitor sizing

Refer to Figure 6-2. Looking into the top plate of C_{s2}, the capacitive network consisting of C_{s2} and the LSB capacitor array must have an equivalent capacitance of C_u. We write $C_{s2} = \alpha C_u$.

$$\frac{8C_u \cdot \alpha C_u}{8C_u + \alpha C_u} = \frac{\alpha \cdot 8C_u}{8+\alpha} \overset{\text{must be equal to}}{=} C_u$$

$$\alpha = \frac{8}{7}$$

$$C_{s2} = \frac{8}{7} C_u = 285.714\,fF$$

Next, seen from the MSB capacitor array, the equivalent capacitance of the remaining capacitive network must be C_u. We take into account $C_{s2} = 8/7 \cdot C_u$ and write $C_{s1} = \beta C_u$.

$$\frac{16C_u \cdot \beta C_u}{16C_u + \beta C_u} = \frac{\beta \cdot 16C_u}{16+\beta} \overset{\text{must be equal to}}{=} C_u$$

$$\beta = \frac{16}{15}$$

$$C_{s2} = \frac{16}{15} C_u = 266.667\,fF$$

6.4. Layout of capacitor array

The binary-weighted capacitor array is built from unit capacitors. To reach good capacitor matching properties, a common-centroid layout technique is used. A sophisticated wiring scheme leads to binary-weighted parasitic capacitances. Not only are binary weighted the nominal capacitors, but so are their parasitic interconnection capacitances.

7. SAR control logic

The Successive Approximation Register (SAR) sets the switches – as a function of the current state of the conversion and the comparator's response – and stores the digital output code to be issued at the end of the conversion. The main building blocks of the SAR control logic are:

- 14-counter
- Combinational network
- Output registers

In addition, various delay elements and output drivers are required.

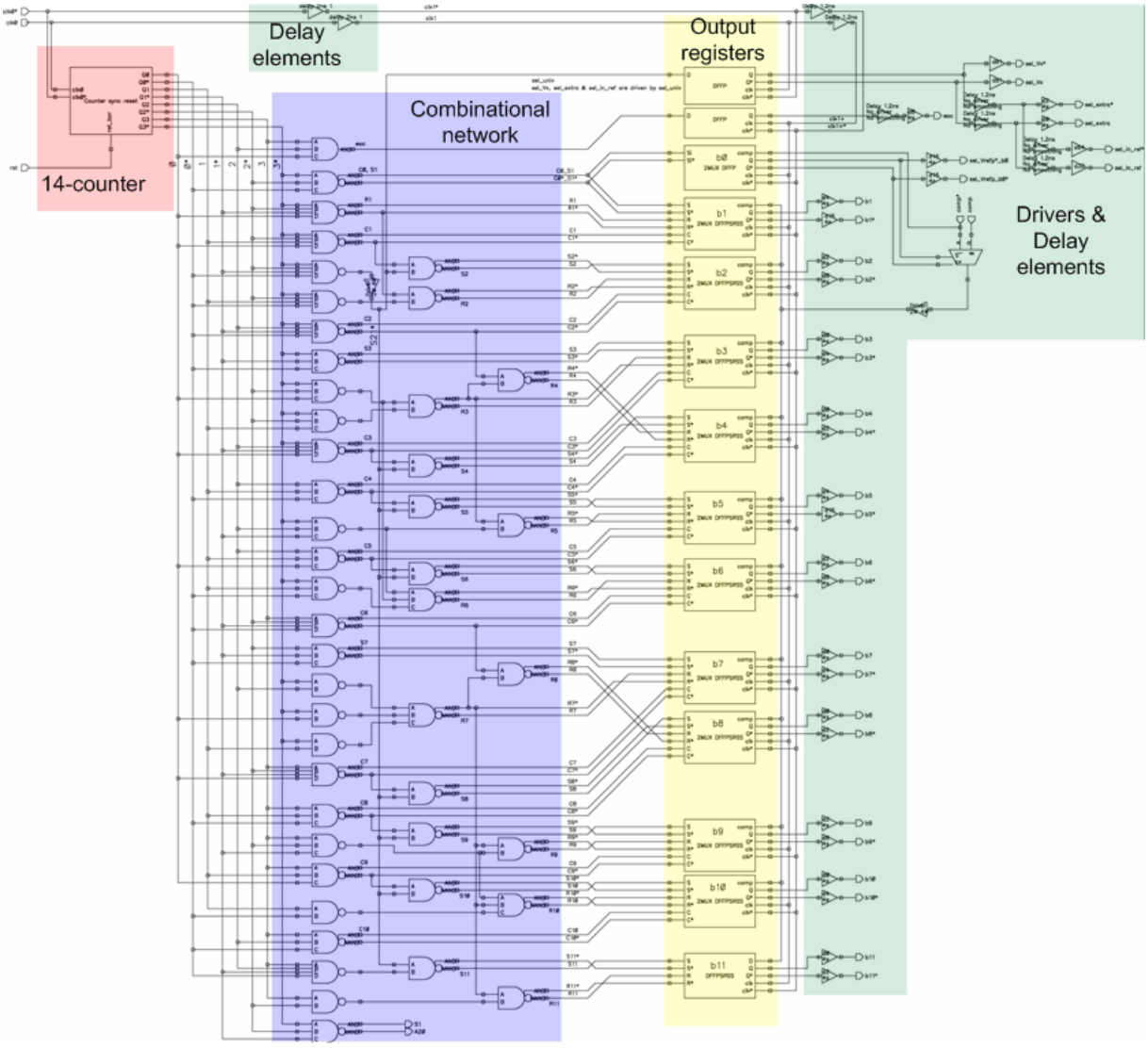


Figure 7-1 SAR control logic. The 14-counter, combinational network, output registers, delay elements and drivers are highlighted.

The 14-Counter counts from 0 to 13, thereby cycling through the 14 states of one conversion. The counter is controlled by the *reference clock* or *clk0*. The *count* or *state* of the counter changes on each positive transition of clock *clk0*. The combinational network calculates the control commands (Set,

Reset and Select) for the output register bank, thereby indirectly setting the switches, accordingly to the history of the current conversion. The output registers store the correct position of the switches for the current conversion and contain the output code at the end of the conversion. They are thus multifunctional. Their multi-functionality saves registers. The output registers eventually change their content on a positive transition of *clk1*, which is delayed with respect to *clk0*.

Basically, all nMOS transistors in all digital blocks have minimum sizes, i.e. $W_n = 240nm$ and $L_n = 180nm$. All pMOS transistors have minimum channel length, i.e. $L_p = 180nm$. To equalize pull-up and pull-down times, pMOS transistors must be 5.4 times wider than nMOS transistors. In fact, following parameters were extracted from simulations: $K_{p,n} = 297\mu A/V^2$ and $K_{p,p} = 55\mu A/V^2$. For equal current pulling and sinking capabilities of pMOS and nMOS transistors, respectively, we require $K_{p,p} \cdot \frac{W_p}{L_p} = K_{p,n} \cdot \frac{W_n}{L_n}$. Therefore, reminding that $L_p = L_n$, $\frac{W_p}{W_n} = \frac{K_{p,n}}{K_{p,n}} = 5.4$. To save area and as it is not required here that pull-up and pull-down times be exactly equal, we set $\frac{W_p}{W_n} = 3$ and size all pMOS transistors with $W_n = 3 \cdot 240nm = 720nm$. Table 7-1 summarizes the *standard transistor sizes* used in digital circuits. Of course, drivers may have wider transistors.

	nMOS	pMOS
Channel length	*180nm*	*180nm*
Channel width	*240nm*	*720nm*

Table 7-1 Standard nMOS and pMOS transistor sizes for digital circuits.

7.1. 14-Counter

The basic 16-counter circuit is taken from [Brown2000]. It contains four DFFs and counts in the sequence 0,1,2,…14,15,0,1, and so on. The basic circuit was modified to introduce a synchronous reset, which is either applied externally or generated every time the counter reaches the state 13. The new sequence is thus 0,1,2,…12,13,0,1, and so on. The 14-counter circuit is depicted in Figure 7-2.

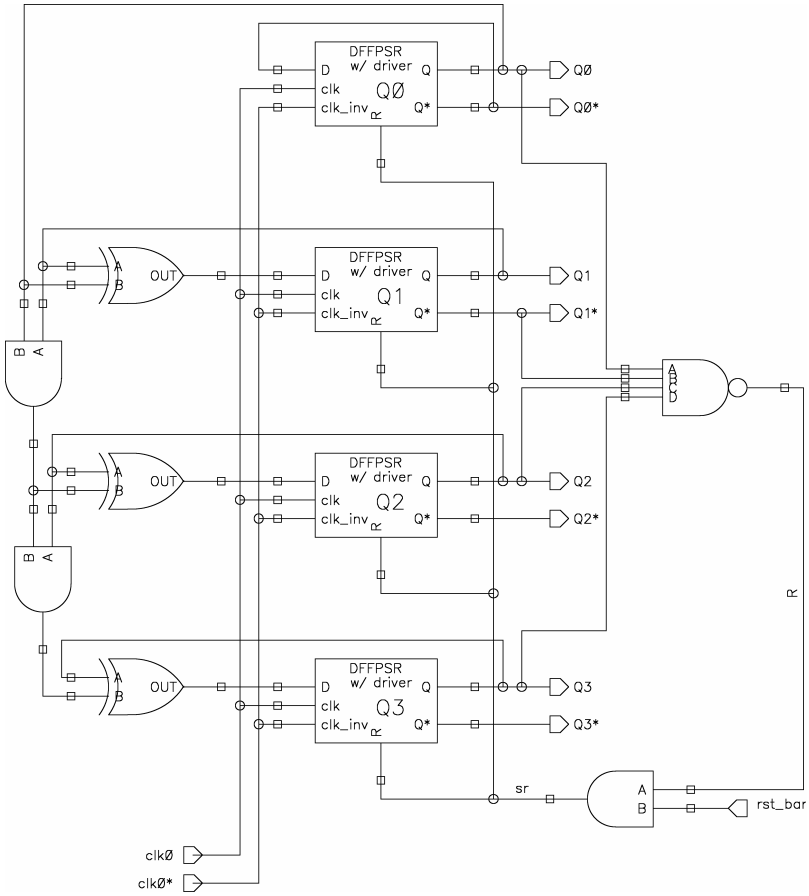


Figure 7-2 14-counter circuit.

The four state variables Q3, Q2, Q1 and Q0 determine the state of the counter. Binary and unsigned decimal representations of the state are adopted. For the unsigned decimal representation, Q3 is considered the MSB and Q0 the LSB. The 14-counter cycles through the states 0 through 13.

Table 7-2 shows how many gates each state variable needs to drive. Each state variable (*Q0,…Q3*) and their inverses (*Q0*,…Q3**) drive in average 11 gates in the combinational network. Therefore, drivers need to be inserted. In fact, the transistors of the DFF slave stage's inverters are made two times wider than standard transistors used in digital circuits. An additional inverter with transistors four times wider than standard transistors is inserted at each of *Q* and *Q** outputs. Figure 7-3 shows the modified DFF circuit with drivers merged into the slave stage. To lay out these transistors, the standard finger widths of 240*nm* and 720*nm* for nMOS and pMOS transistors, respectively, are kept; merely the finger number is increased from 1 to 2 or 4.

Line	# gates
Q0	8
Q0*	13
Q1	10
Q1*	11
Q2	9
Q2*	13
Q3	9
Q3*	16

Table 7-2 Number of gates driven by each state variable (Q0,…Q3) and their inverses (Q0*,…Q3*).

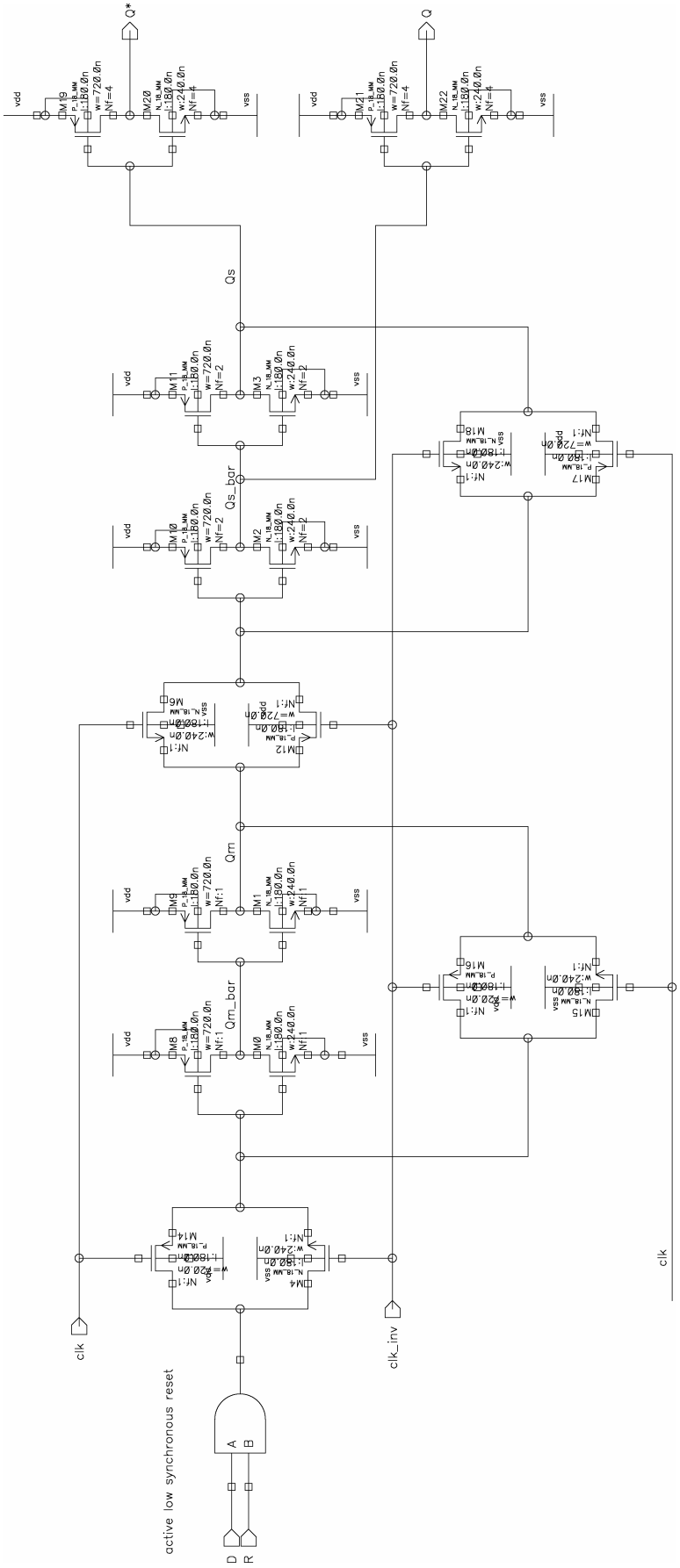


Figure 7-3 Modified DDF circuit containing an active low synchronous reset and output drivers merged into the slave stage.

7.2. Combinational logic

Table 7-3 lists the 14 states in binary and unsigned decimal representation and shows which operation is performed during each state. For example, during state 0, the input voltage is sampled, while its inverse is held on the capacitor array during state 1. As soon as the counter enters state 2, the value of the MSB is determined. Also, during state 2, the capacitor corresponding to bit b1 is switched from ground to the voltage reference, in order to determine the value of b1 when entering state 3. Finally, the LSB is determined when the counter enters state 13. Thereafter, the counter returns to its initial state and accepts a new sample.

Q3	Q2	Q1	Q0	Unsigned decimal	Comments
0	0	0	0	0	Initial state, Sample
0	0	0	1	1	Hold
0	0	1	0	2	MSB, sign bit, b0
0	0	1	1	3	2nd MSB, b1
0	1	0	0	4	b2
0	1	0	1	5	b3
0	1	1	0	6	b4
0	1	1	1	7	b5
1	0	0	0	8	b6
1	0	0	1	9	b7
1	0	1	0	10	b8
1	0	1	1	11	b9
1	1	0	0	12	2nd LSB, b10
1	1	0	1	13	LSB, b11

Table 7-3 The 14 states of the counter and corresponding operations.

Table 7-5 and Table 7-5 show the various functions to be calculated from the current state Q of the counter.

Q	b0	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11
0	x	1	1	1	1	1	1	1	1	1	1	1
1	x	0	0	0	0	0	0	0	0	0	0	0
2	C*	1	0	0	0	0	0	0	0	0	0	0
3	b0-	Y	1	0	0	0	0	0	0	0	0	0
4	b0-	b1-	Y	1	0	0	0	0	0	0	0	0
5	b0-	b1-	b2-	Y	1	0	0	0	0	0	0	0
6	b0-	b1-	b2-	b3-	Y	1	0	0	0	0	0	0
7	b0-	b1-	b2-	b3-	b4-	Y	1	0	0	0	0	0
8	b0-	b1-	b2-	b3-	b4-	b5-	Y	1	0	0	0	0
9	b0-	b1-	b2-	b3-	b4-	b5-	b6-	Y	1	0	0	0
10	b0-	b1-	b2-	b3-	b4-	b5-	b6-	b7-	Y	1	0	0
11	b0-	b1-	b2-	b3-	b4-	b5-	b6-	b7-	b8-	Y	1	0
12	b0-	b1-	b2-	b3-	b4-	b5-	b6-	b7-	b8-	b9-	Y	1
13	b0-	b1-	b2-	b3-	b4-	b5-	b6-	b7-	b8-	b9-	b10-	Y

Table 7-4 Functions to be calculated from the counter's state by the combinational network (a).

Q	sel_extra	sel_Vx	sel_in_ref	sel_Vrefp	eoc
0	1	1	1	x	0
1	0	0	x	x	0
2	0	0	0	C	0
3	0	0	0	sel_Vrefp-	0
4	0	0	0	sel_Vrefp-	0
5	0	0	0	sel_Vrefp-	0
6	0	0	0	sel_Vrefp-	0
7	0	0	0	sel_Vrefp-	0
8	0	0	0	sel_Vrefp-	0
9	0	0	0	sel_Vrefp-	0
10	0	0	0	sel_Vrefp-	0
11	0	0	0	sel_Vrefp-	0
12	0	0	0	sel_Vrefp-	0
13	x	x	x	x	1

Table 7-5 Functions to be calculated from the counter's state by the combinational network (b).

In the two tables above, *x* means don't care. *C* is the response of the comparator, while *C** is its inverse. *f-* means that the function *f* keeps, in the current state, the value from the previous state (*f=b0,...b10,sel_Vrefp*). $Y = C$ if a positive sample is being converted, $Y = C*$ if a negative sample is being converted. Before *Y* needs to be evaluated for the first time, the sign bit *b0* has already been set. To implement *Y* on silicon, a multiplexer, controlled by *b0*, choosing either *C* or *C**, is used: $Y = b0* \cdot C + b0 \cdot C*$.

It is possible to implement *sel_Vrefp* as *b0** and have a single function *sel_univ* that drives *sel_extra*, *sel_Vx* as well as *sel_in_ref*. Refer to Figure 4-6 on page 23 for signal/node names. In order to loose no charge on the capacitor array, *b1* through *b11* and *sel_extra* must be slightly delayed with respect to *sel_Vx*. In fact, nodes *Vx1*, *Vx2, Vx1-2, Vx2-2, Vx1-3* and *Vx2-3* must be floating before the parallel capacitors corresponding to bits *b1* through *b11* are switch from *Vin* to ground. Furthermore, *sel_in_ref* must be slightly delayed with respect to *b1* through *b11* and *sel_extra*, to keep the lines *Vin_Vref+/-* at *Vin+/-* until all parallel capacitors have been switched to ground. Shortly after, lines *Vin_Vref+/-* can be switched to *Vrefpn+/-*. It is convenient to slightly delay *eoc* with respect to *b11*, to make sure that the LSB value has properly been set before setting the end-of-conversion flag. The same delay element as for *sel_in_ref* can be used. To reduce the number of delay elements, we do slightly delay the clock signal triggering the various DFFs rather than separately delay each signal.

In order to appropriately delay *clk1* with respect to *clk0*, the maximum delay (critical path delay) of the combinational logic network must be determined. The *clk1* to *clk0* delay time must be bigger than the critical path delay.

Reset signal Rn (see *Section 7.3 Output registers*) can be built from reset signal Rn-1, n=1,…,11, by adding a product of 3 or 4 state variables. However, this approach would result in a high critical path delay. The strategy followed here minimizes the critical path delay, in order to relax the timing requirements of the analog blocks. Each gate has a propagation time delay of several hundreds of *ps*, depending on input transitions. In order to keep the critical path delay small, the combinational network is required to have a maximum of 3 levels. (See Figure 7-1, combinational network. Levels are counted from the left-hand side to the right-hand side.) In other words, all control signals must be calculated with a cascade of 3 gates or less.

For the conversion of a 300mV sample, the maximum first, second and third level output delay times are given in Table 7-6..

Level	Maximum delay
1	737p
2	814ps
3	919ps

Table 7-6 Maximum delay at logic level 1 through 3 in the combinational network

Consequently, the critical path delay for a $300mV$ conversion is $919ps$. Thus, the output registers must change their state $1ns$ after the state of the counter changes. We do preferentially delay *clk1* by approximately $2ns$ with respect to *clk0*, in order to allow for clock skew and clock jitter.

As the product $Q0^* \cdot Q1^* \cdot Q2^* \cdot Q3^*$ drives more than 10 gates, a driver is needed within the combinational network.

7.3. Output registers

To implement the functions defined in Table 7-4 and Table 7-5, positive-edge triggered DFFs with synchronous set, synchronous reset and a 2-to-1 multiplexor at their input are used (Figure 7-4). To obtain a DFF with active high synchronous set and reset, the circuit of Figure 7-6 is added at the input of a standard DFF. The 2-to-1 multiplexer is implemented with transmission gates (Figure 7-5). Thanks to the multiplexer, either the previous state *Q*- or *Y* can be chosen as input data to the DFF. All DFFs are synchronized with *clk1*. For b1 to b10, three command signals are computed from the current state of the counter.

- Set (S)
- Reset (R)
- Select (C), C as for select Comparator

The DFF for b0 comes without set, neither reset capability, what saves a little area. Merely a select signal is computed for b0. The DFF for b11 needs no multiplexor, again saving area. Merely a set and reset signal are computed for b11. *sel_Vrefp* is taken from the complementary output of b0's DFF. *sel_univ* and *eoc* are computed as standard Boolean function from the current state of the counter and do basically not require a DFF. However, in order to synchronize their transitions with those of the other control signals, basic DFFs (without multiplexor, set or reset) are inserted.

Of course, the DFFs b0 throught b11 contain the output code at the end of the conversion.

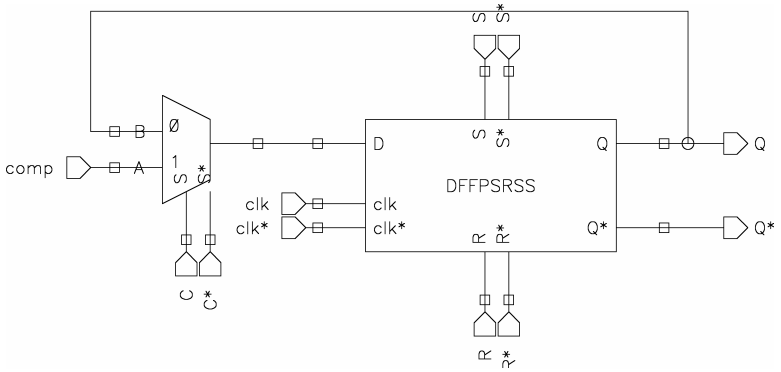


Figure 7-4 Positive-edge triggered DFF with synchronous reset, synchronous set (DFFPSRSS) and 2-to-1 multiplexer

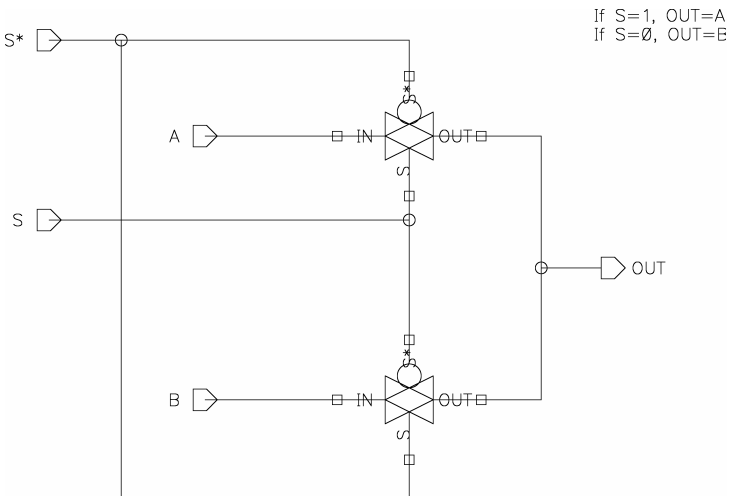


Figure 7-5 Transmission-gate (TG)-based 2-to-1 multiplexer

R	S	Operation
Ø	Ø	f=D
Ø	1	f=1
1	Ø	f=Ø
1	1	f=D

Active high synchronous reset
Active high synchronous set

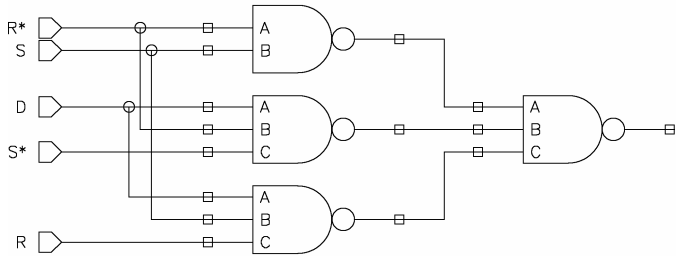


Figure 7-6 Combinational logic circuit setting, resetting or loading the standard DFF.

8. Switches

Voltages to be transmitted may vary from V_{SS} to V_{DD}. In order to guarantee conduction over this voltage range, CMOS transmission gates are used. To reach a symmetric conduction characteristic, pMOS transistors are 3 times wider than nMOS transistors, in all transmission gates. All analog switches have minimum channel length, in order to reduce the equivalent on-resistance/maximize g_{on}. Furthermore, in order to size the transistor widths of each transmission gate, the maximum capacitor which is charge/discharged through is calculated. To have constant RC delays in the whole circuit (thereby easily controlling the DAC settling time),

$$i(t) = C\frac{dv(t)}{dt}$$

$$\frac{dv(t)}{dt} = \frac{i(t)}{C}$$

If we want a constant $\frac{dv}{dt}$, then the ratio $\frac{i}{C}$ must be constant as well. Consequently, if the capacitance increases by a factor of α ($\alpha = 2,4,8$), the current charging/discharging the capacitor needs to be increased by the same factor. The current in a simple analog switch is given by $I_D = \beta_{n/p}(V_D - V_S)\left[V_G - V_{T0n/p} - \frac{n}{2}(V_D + V_S)\right]$, where $\beta_{n/p} = K_{p,n/p}\left(\frac{W}{L}\right)_{n/p}$. $K_{p,n/p}$, $V_{T0n/p}$ and n are technology dependent. V_S and V_D may vary from $-900mV$ to $900mV$. L is set to its minimum value. The only design variable is W. To increase the current by α, increase W by α.

The switch that transmits the positive reference voltage is realized with a single pMOS transistor, while the switch transmitting the negative reference voltage is realized with a single nMOS transistor. This way, silicon area can be saved while maintaining almost equal conduction as compared to a transmission gate. The switch transmitting ground is realized with a single nMOS transistor rather than with a pMOS transistor, as higher conductivity is reached this way for same transistor sizes.

8.1. Charge injection minimization

Charge injection (also called charge feedthrough or clock feedthrough) consists of two components:

1) Channel charge, $Q_{ch} = WLC_{ox}(V_{gs} - V_{th})$
2) Overlap capacitance between the gate and the source/drain diffusion

The error voltage on a capacitor due to charge injection depends on:

- Transistor area (WL)
- Layout of transistor
- Value of capacitor
- Gate waveform
- Impedance levels at source and drain nodes of transistor

Whenever a transistor is turned off, the channel charge is injected into the nodes connected to drain source. Depending on the impedance seen at these nodes, the node voltage varies due to charge injection.

Figure 8-1 shows the transmission gate circuit with dummy transistors for charge injection minimization, embedded in a test-bench. The two drivers are responsible for fast transitions of the TG control signals.

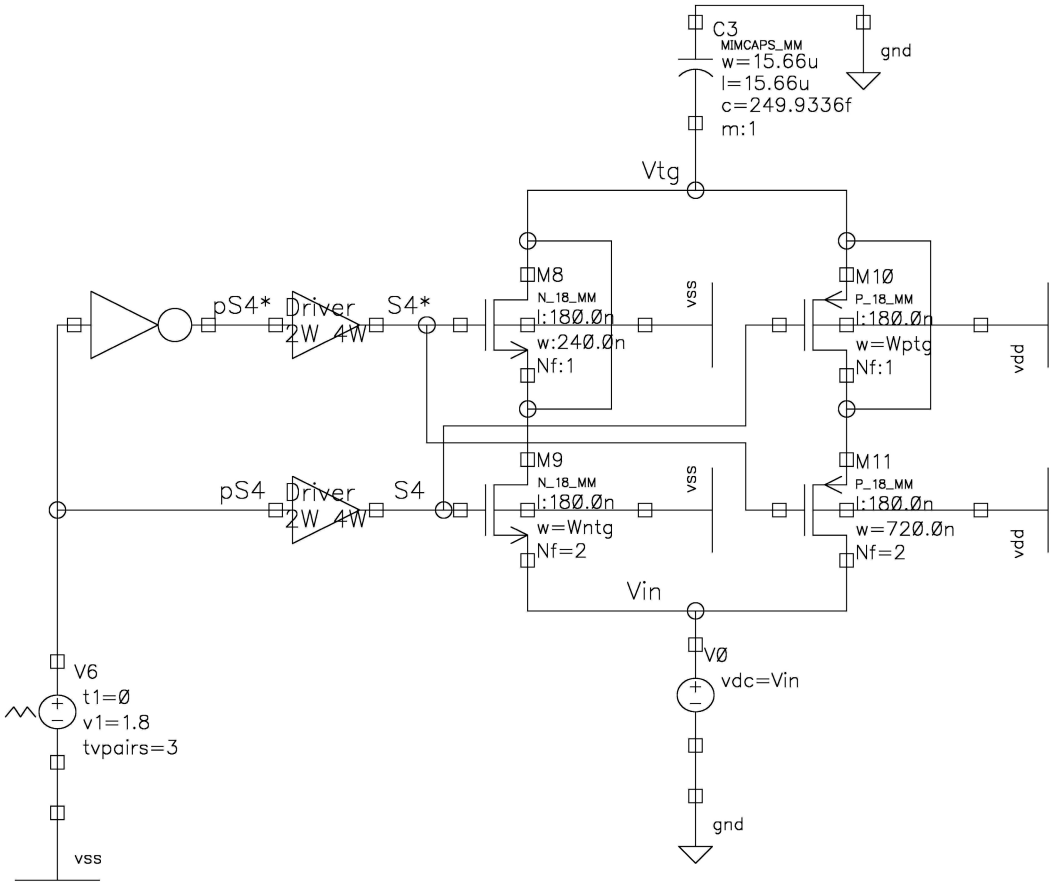


Figure 8-1 Charge injection minimization of transmission gate; Test-bench.

Figure 8-2 shows the waveforms of $V_{tg}-V_{in}$ for $V_{in}=-900,-800,...,-100,0,100,...800,900mV$. With $W_{n,tg}=240nm$ and $W_{p,tg}=770nm$, the voltage difference over the unit capacitor due to charge injection $\left|\Delta V_{tg}\right|$ is kept below $240\mu V$ over the full analog range from $-900mV$ to $900mV$.

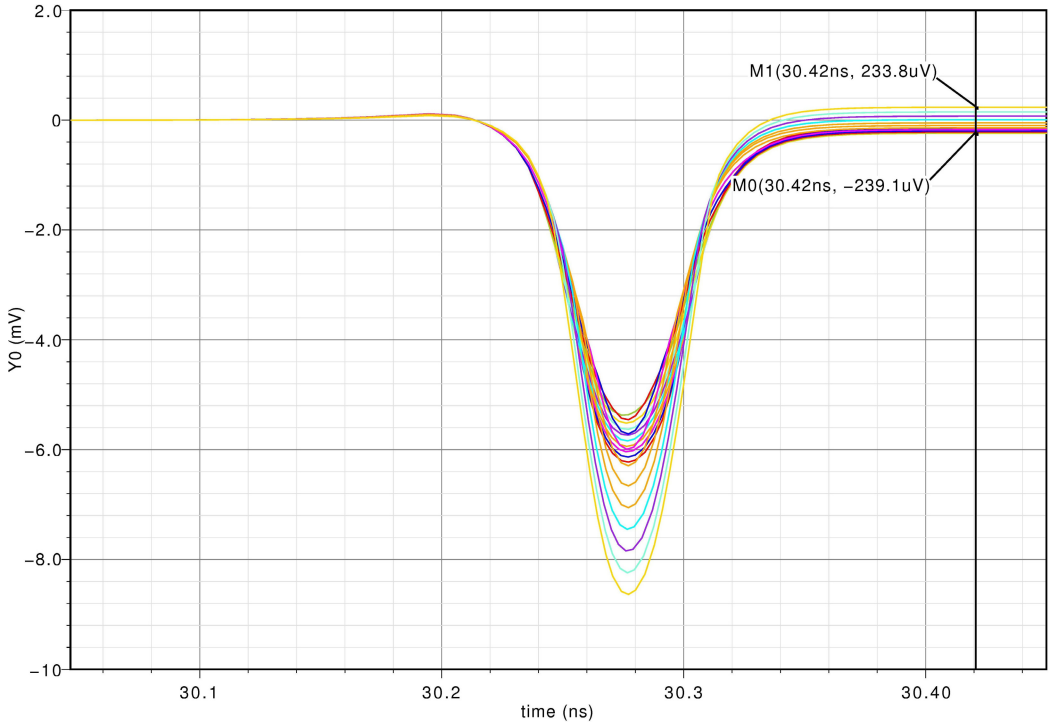


Figure 8-2 Charge injection minimization of transmission gate; residual voltage difference.

If the clock signal turns off fast, the channel charge distributes fairly equally between the adjacent nodes [Baker2005]. If we want to use the circuit of Figure 8-1 as a generic switch, we have to assume variations of fall and rise time of control signals *pS4* and *pS4**, as they come from different nodes in the digital circuitry that are differently loaded. Also, the control signals from the digital circuitry may have transition times as high as several hundreds of *ps*, what results in a poorly controlled distribution of the channel charge when the switch turns off. To equalize and minimize transition times, drivers were inserted in the circuit of Figure 8-1. If signals *pS4* and *pS4** have 10%-to-90% transition times of 240*ps* and 121.48*ps*, respectively, signals *S4* and *S4** make their transitions in 34.69*ps* and 37.69*ps*, respectively. See Figure 8-3.

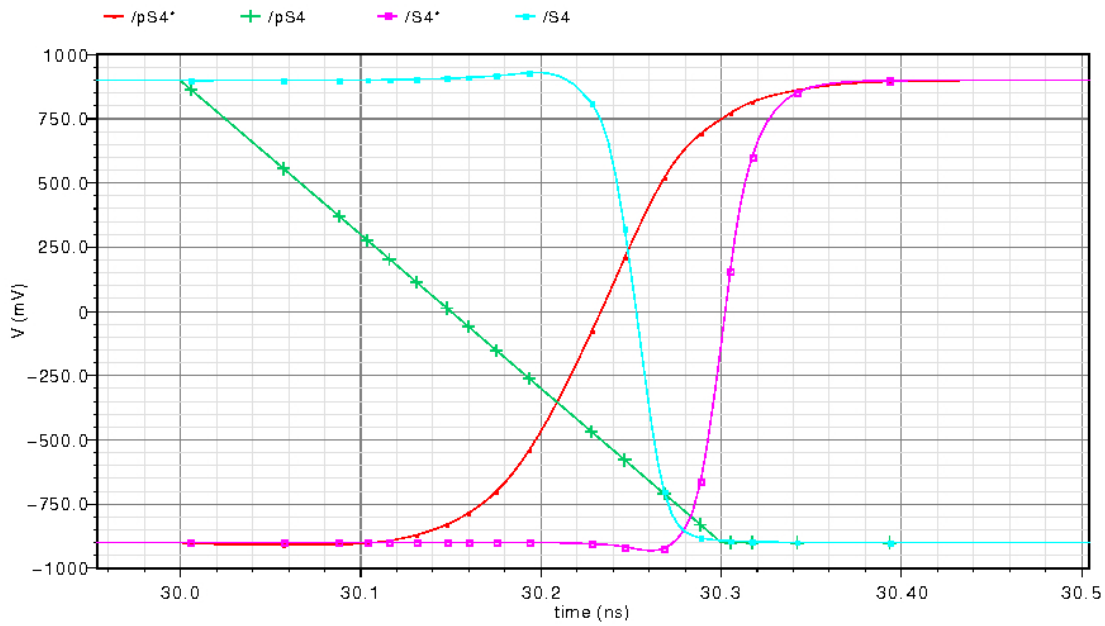
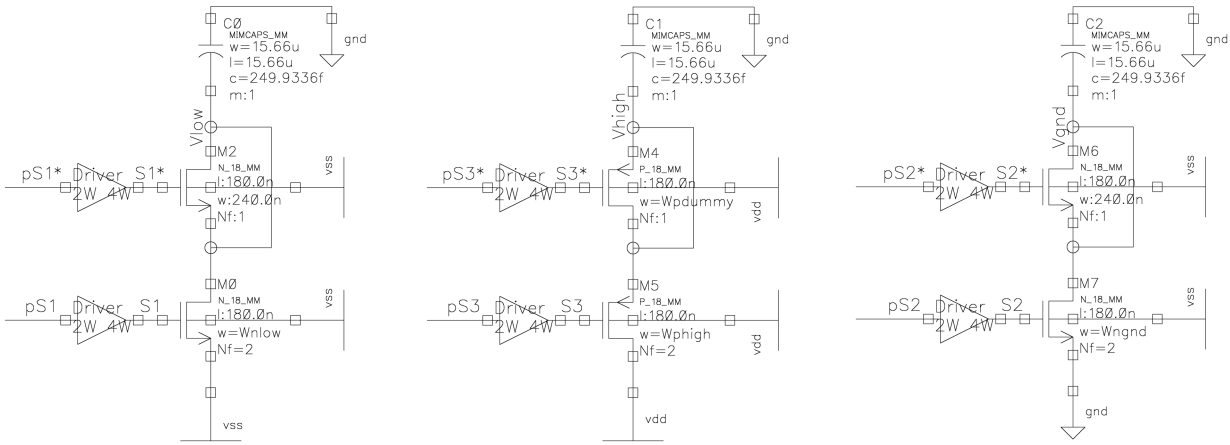


Figure 8-3 Minimized transition times of complementary signals controlling the TG.

For a constant signal level, ΔV due to charge injection can be reduced to several tens of μV by carefully adapting the channel width of either dummy or switch transistor. The precision with which transistor dimensions can be defined – $10nm$ for UMC $0.18\mu m$ CMOS technology – limits the charge injection minimization. nMOS and pMOS transistors are used to transmit V_{SS} and V_{DD}, respectively. To transmit ground, an nMOS rather than a pMOS transistor is used, as it has better conductance and thus smaller on-resistance for equal size. As for the TG, drivers are stuck in.

Referring to Figure 8-4 (a), for $W_{n,low} = 240nm$, ΔV_{low} is $48.5\mu V$. Notice that we would have to increase the switch transistor width to more accurately balance charge injection and absorption of switch and dummy transistors, respectively, as the dummy transistor has minimum width and thus cannot be made narrower. However, with the next possible value $W_{n,low} = 250nm$, $\Delta V_{low} = -62\mu V$. That's why we keep $W_{n,low} = 240nm$. To transmit V_{DD}, we can modify either the switch transistor width, the dummy transistor width or both. Considering that variations of transistor width are small and do hardly affect conductance, $W_{p,dummy}$ is decreased while $W_{p,high}$ is kept at its standard value. Referring to Figure 8-4 (b), for $W_{p,dummy} = 710nm$ and $W_{p,high} = 720nm$, $\Delta V_{high} < 1\mu V$. To transmit ground, setting $W_{n,gnd} = 240nm$ in the circuit of Figure 8-4 (c), $\Delta V_{gnd} < 1\mu V$.



(a) (b) (c)

Figure 8-4 Switches to transmit (a) V_{SS}, (b) V_{DD} and (c) ground. The reference voltages to be transmitted (bottom), the drivers (left) and a unit capacitor (top) are included in the schematics.

8.2. Bootstrapped switch

If the TG with dummy transistors as shown inFigure 8-1 is used at the entrance of the comparator (switch S1), the charge injected from that switch onto the capacitor array is high enough to make the A/D conversion fail. The idea is to use a bootstrapped switch with constant V_{gs}. If V_{gs} is constant, then the channel charge is constant, as $Q_{ch} = WLC_{ox}(V_{gs} - V_{th})$. With the fully differential topology, the same amount of charge would be injected onto both capacitor arrays, whatever the signal level, and the effect would be cancelled out.

Figure 8-5 shows the circuit diagram of the bootstrapped switch [Abo1999]. Even though the gate voltage is always V_{DD} over the source and drain level, terminal-to-terminal voltages of the switch transistor are never higher than V_{DD}, as in other bootstrapped switches. Therefore, the circuit is reliable. Basically, the capacitor C2 is charged to $V_{DD} - V_{SS}$, then connected over the gate-to-source junction of the switch transistorM7. The source and drain level can be anywhere within $[V_{SS}, V_{DD}]$. The concept is illustrated on Figure 8-6.

The current design of Figure 8-5 has a problem. If the capacitor array is connected to one side and the input of the comparator to the other side, the capacitor acting a voltage source, sharing a little of its charge with the gate parasitic capacitance of the comparator input transistor, charge is lost at each switching event and the A/D conversion fails. During a small interval of time, there must be a DC path to V_{SS} through which charge from the capacitor array flows into ground.

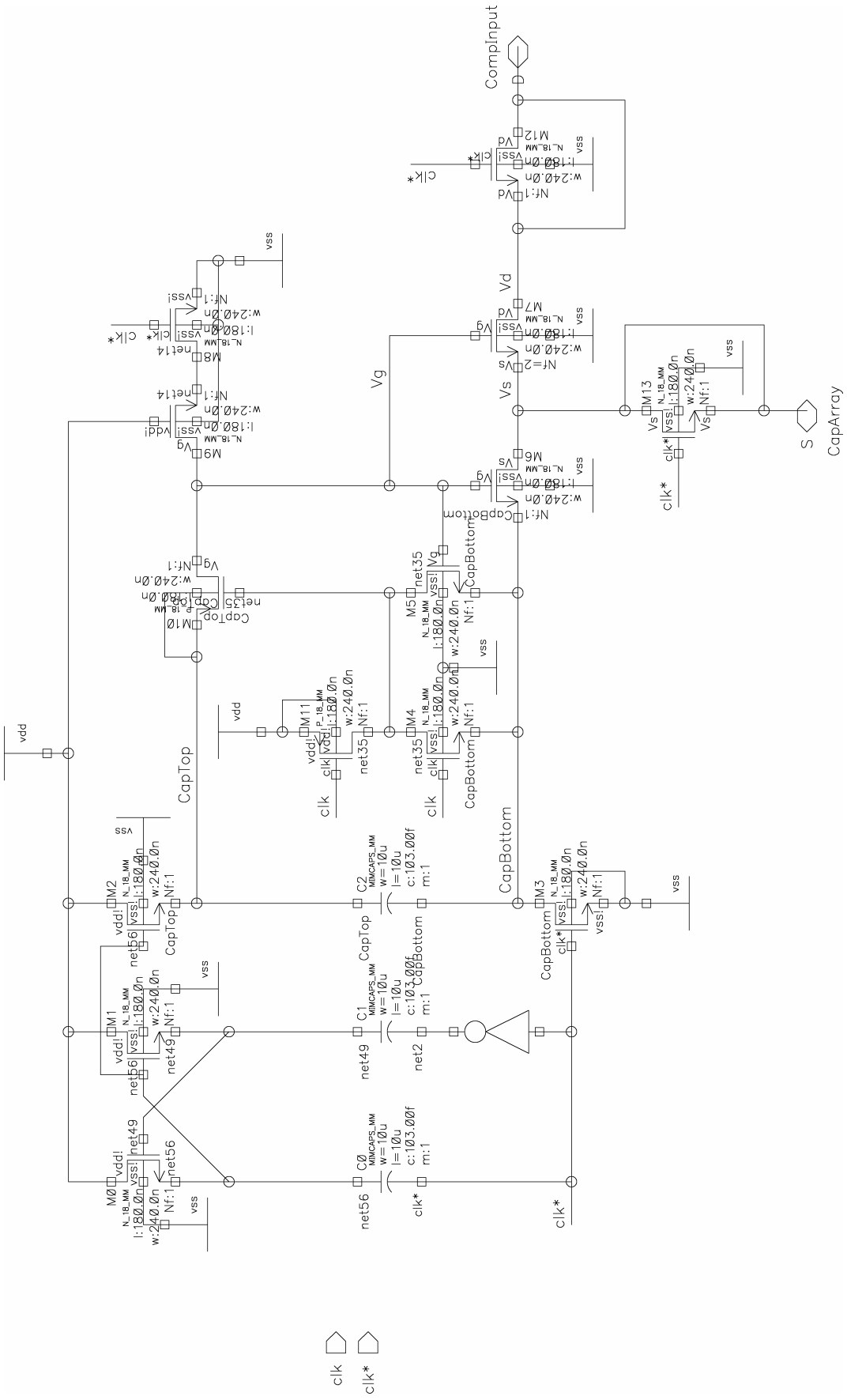


Figure 8-5 Circuit diagram of bootstrapped switch.

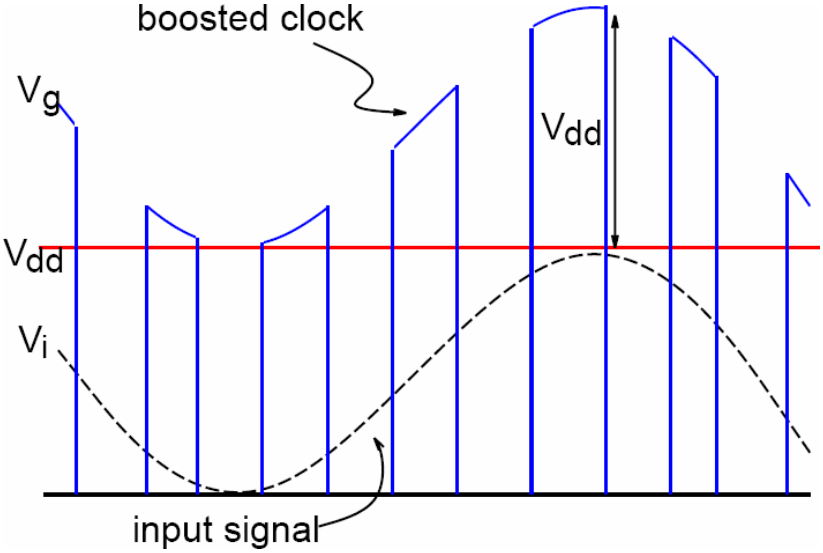


Figure 8-6 Conceptual bootstrapped switch output [Abo1999].

9. Delay elements

9.1. Different delay circuits in comparison

A delay element, delaying *clk1* by *2ns* with respect to *clk0* is being designed. Delay circuits include

Inverter-based delay circuit
Current-starved inverter delay circuit
RC-inverter delay circuit [Kavak2004]

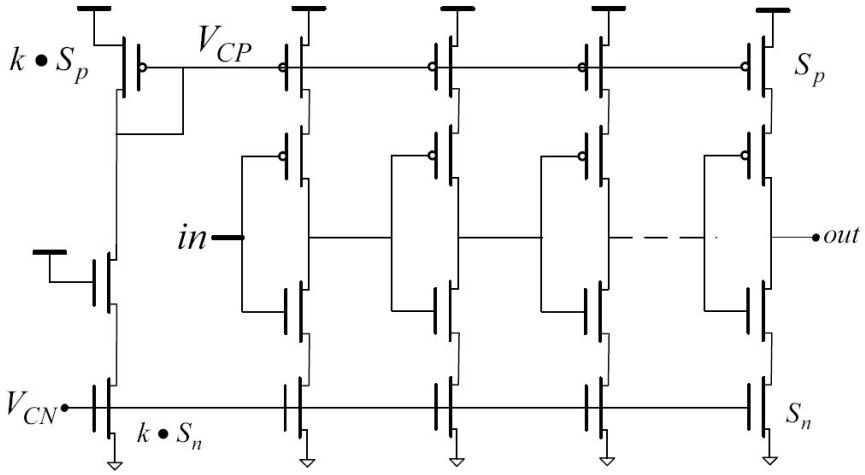


Figure 9-1 Current-starved inverter delay circuit [Kavak2004]

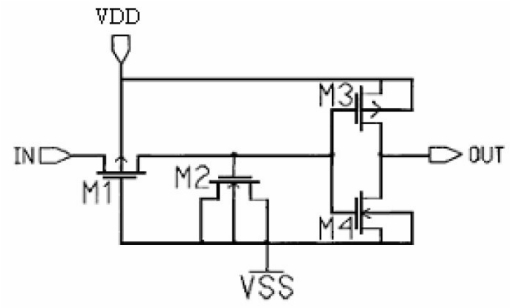


Figure 9-2 RC-inverter delay circuit [Kavak2004]

In the *inverter-based delay circuit*, the desired delay is obtained by cascading a number of inverters. In the *current-starved inverter delay circuit*, the current charging and discharging the MOSFET gate capacitances is restricted by current control transistors in series with the inverter's transistors. In the *RC-inverter delay circuit*, one transistor acts as a resistor, while another one acts as a capacitor; an RC delay is obtained.

In the *inverter-based delay circuit*, many stages are required to realize long delays. The *current-starved inverter delay circuit* requires biasing circuits, in addition to already having more transistors. The *RC-inverter delay circuit* produces signals with long fall and rise times. As no long delay times are required, fall and rise times must be small and circuit complexity as low as possible, inverter-based delay circuits are designed.

9.2. Design of an inverter-based delay circuit

The high-to-low and low-to-high propagation delay times of a CMOS inverter are given by

$$\tau_{PHL} = \frac{C_{load}}{k_n (V_{DD} - V_{T,n})} \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right]$$

and

$$\tau_{PLH} = \frac{C_{load}}{k_p (V_{DD} - |V_{T,p}|)} \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right],$$

respectively, where $k_n = \mu_n C_{ox} \frac{W_n}{L_n}$ and $k_p = \mu_p C_{ox} \frac{W_p}{L_p}$ [Kang2003]. $V_{T,n}$, $V_{T,p}$, μ_n, μ_p and C_{ox} are technology dependent, while V_{DD} is set at system level. C_{load}, W_n, W_p, L_n and L_p are the only design parameters allowing to tune the delay times. The high-to-low and low-to-high propagation delay times depends on nMOS and pMOS transistor sizes, respectively. Note that

$$\tau_{PHL} \propto \frac{L_n}{W_n}$$

and

$$\tau_{PLH} \propto \frac{L_p}{W_p}.$$

An efficient way to increase the propagation delay times of a CMOS inverter consists in increasing the channel lengths of both nMOS and pMOS transistors. Also, a capacitance could be placed at the output node of the inverter to increase delay times. However, adding a capacitance results in high rise and fall times, what is an undesired property for a clock signal.

Using long transistors increases charge injection. As a consequence, the output voltage of the inverter can go several hundreds of *mV* above V_{DD} and below V_{SS}. The positive excursions above V_{DD} are typically higher than the negative excursions below V_{SS} as pMOS transistors are typically wider than nMOS transistors, what means that more charge is injected from pMOS transistors. High voltage excursions may lead to earlier oxide breakdown, worsening the reliability and shortening the lifetime of the chip. That's why the delay element design must avoid excessively high excursions.

Four cascaded inverters with $L = 1\mu m$ are responsible for the *1.786ns* rising-output delay, while two additional inverter with minimum channel length minimize the spikes, thereby smoothing the delayed clock signal. The additional inverters are also responsible for short rise and fall times of the delayed clock signal; the first and second additional inverter have transistors two and four times wider than standard transistors in logic circuits, respectively. The resulting 10%-to-90% rise time for a *100fF* load capacitance is *330ps*. The highest excursion due to charge injection occurs at the output of the first cascaded inverter and goes *183mV* over V_{DD}. (It is not essential that falling-output delay be exactly equal to rising-output delay or fall time be exactly equal to rise time, as nor negative-edge triggered flip-flops neither level-sensitive elements are employed. The falling-output delay is *1.909ns* and the 90%-to-10% fall time is *292.8ps*.)

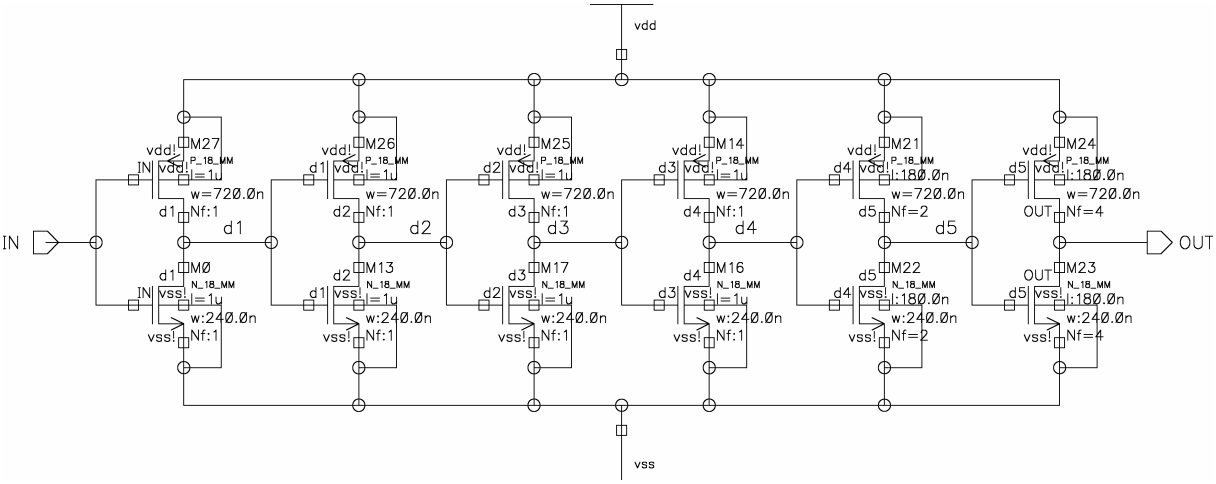


Figure 9-3 Delay element, circuit

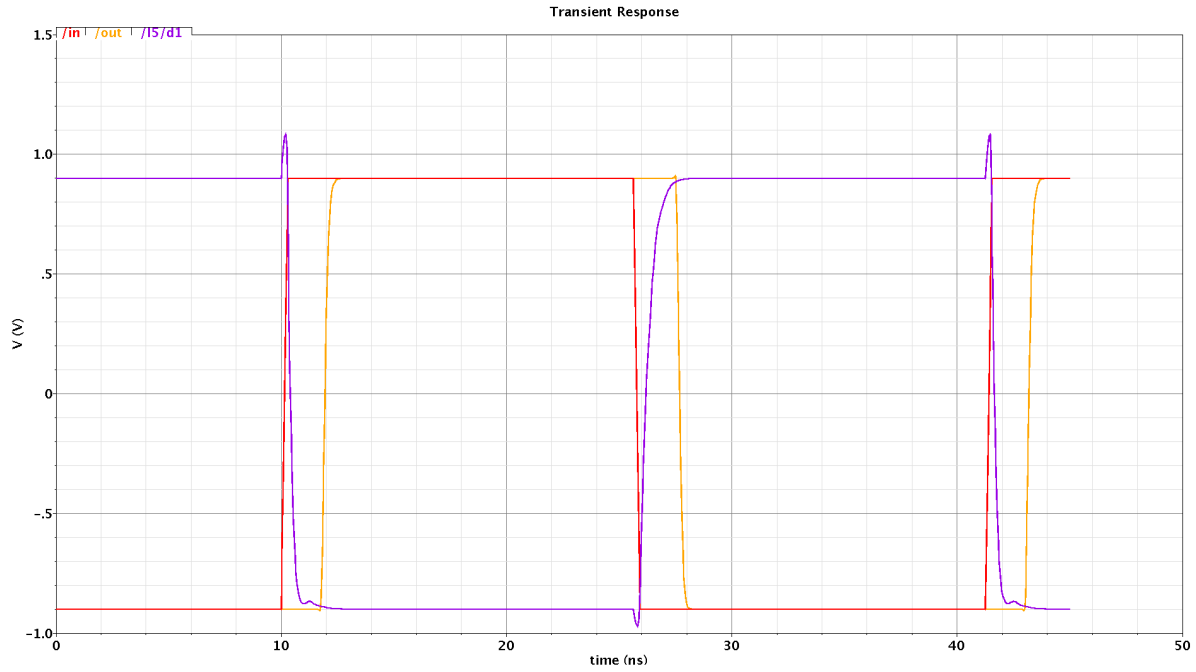


Figure 9-4 Timing diagram. Red: IN (clk0); Orange: OUT (clk1); Violet: d1 (output of first cascaded inverter)

Further delay elements with different delay times are required, but not discussed here any more, as they us similar design approaches.

10. Validation of the ADC core

10.1. Transient simulations

To test the ADC core, the A/D conversions listed in Table 10-1 have been simulated. The offset-voltage of the preamplifier and the offset cancellation circuit are not included in the simulation.

Sample	Expected output code	Simulated otput code
$-900mV$	1111'1111'1111	1111'1111'1111
$-450mV$	1100'0000'0000 or 1011'1111'1111	1011'1111'1111
$-219\mu V$	1000'0000'0000	1000'0000'0000
$219\mu V$	0000'0000'0000	0000'0000'0000
$450mV$	0100'0000'0000 or 0011'1111'1111	0011'1111'1111
$900mV$	0111'1111'1111	0111'1111'1111

Table 10-1 Validation of the ADC core: samples, expected output codes and simulated output codes.

All six tests have been successful. As the samples $-450mV$ and $450mV$ are exactly on a transition point, to different output codes are considered correct.

.Figure 10-1 shows the voltages at nodes Vx1, Vx2, Vx1-2, Vx2-2, Vx1-3 and Vx2-3 for $V_{in} = 900mV$. The effect of the series capacitors can be seen. Figure 10-3 shows the produced output codes and the eoc flag for, again for $V_{in} = 900mV$.

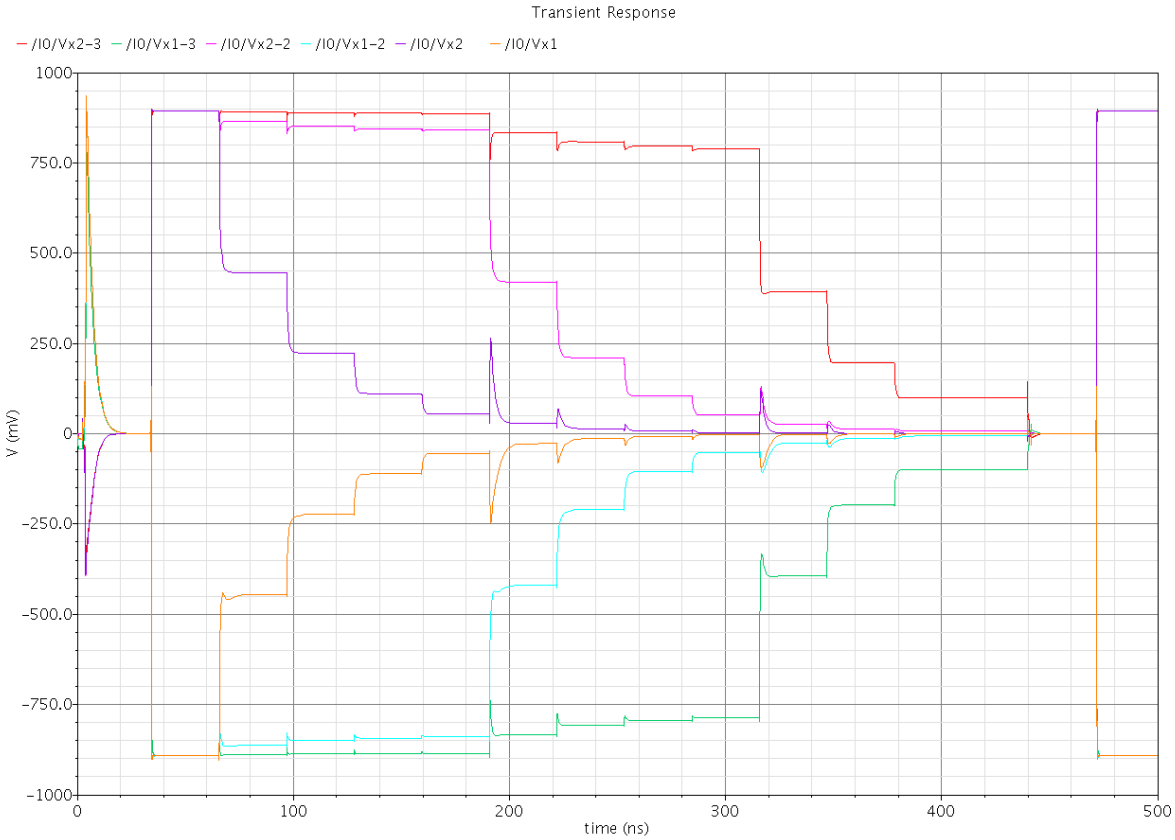


Figure 10-1 $V_{in} = 900mV$, analog signals (1).

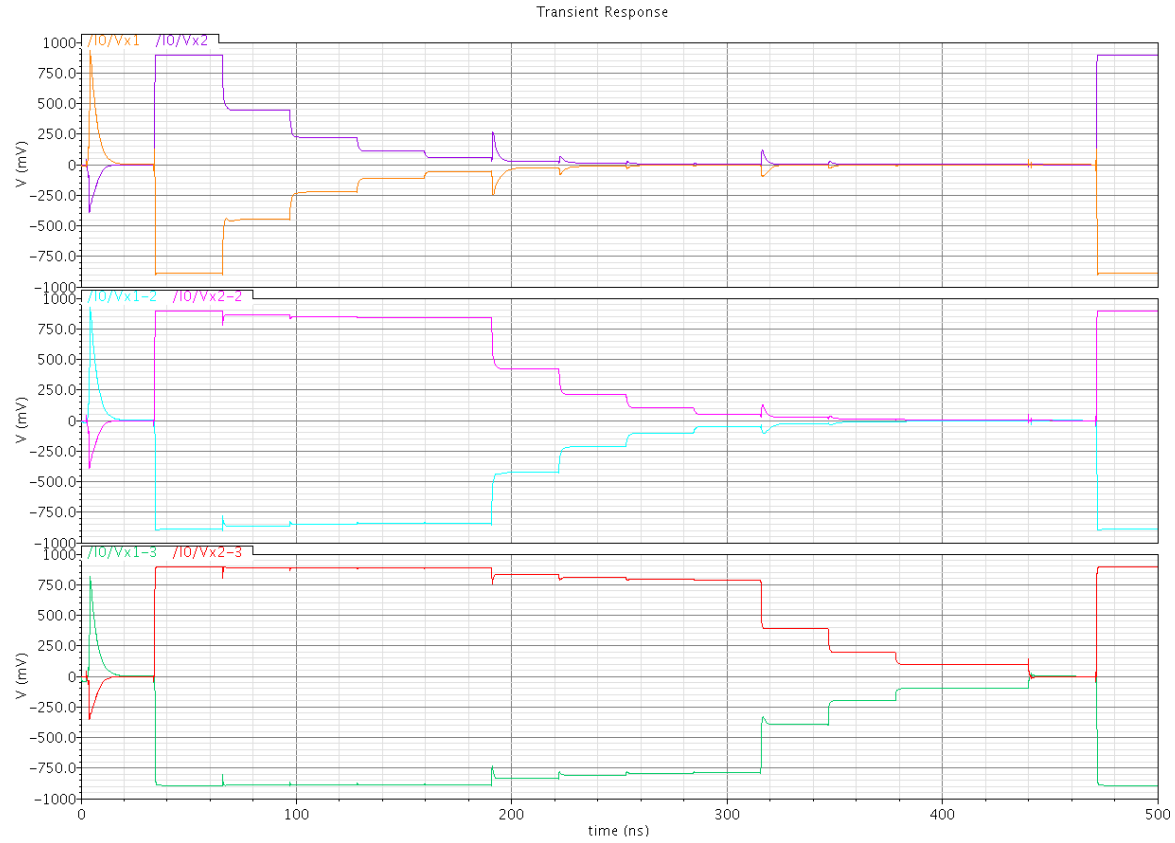


Figure 10-2 $V_{in} = 900mV$, analog signals (2).

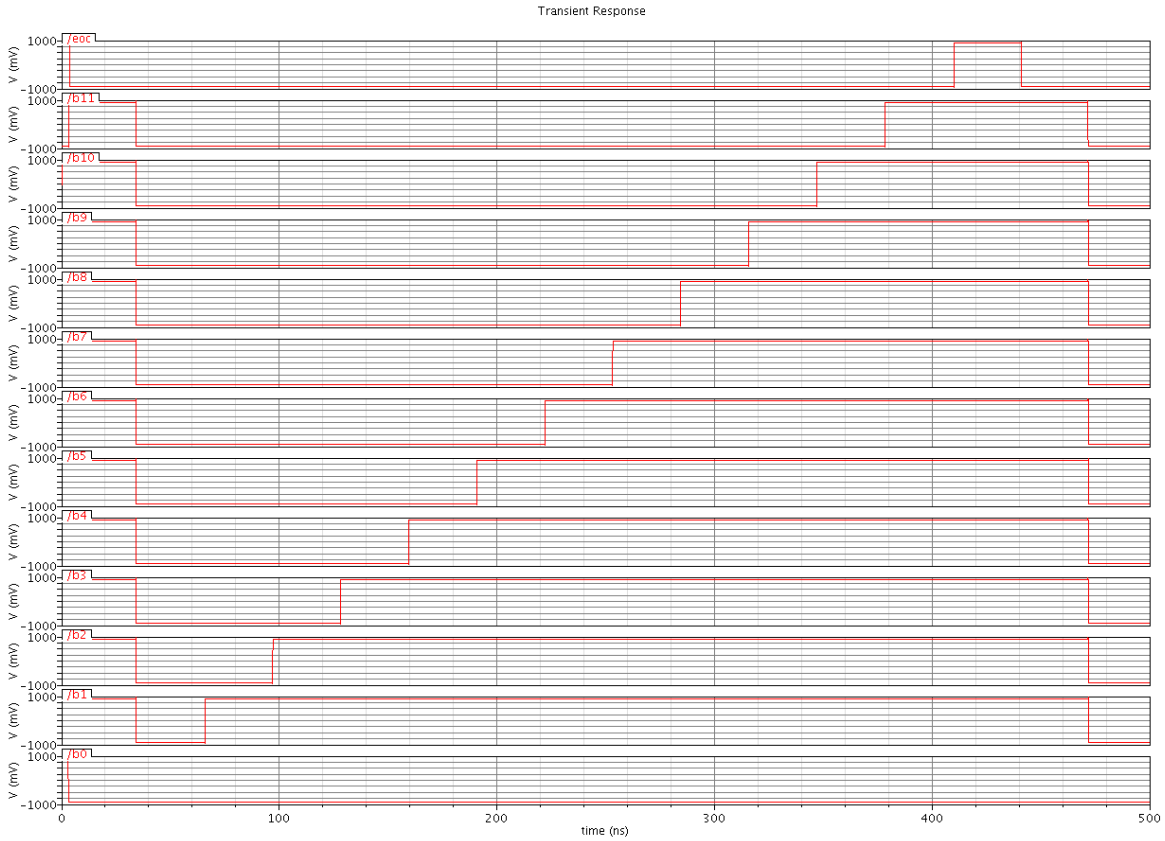


Figure 10-3 $V_{in} = 900mV$, digital signals. The output code 0111'1111'1111 was produced.

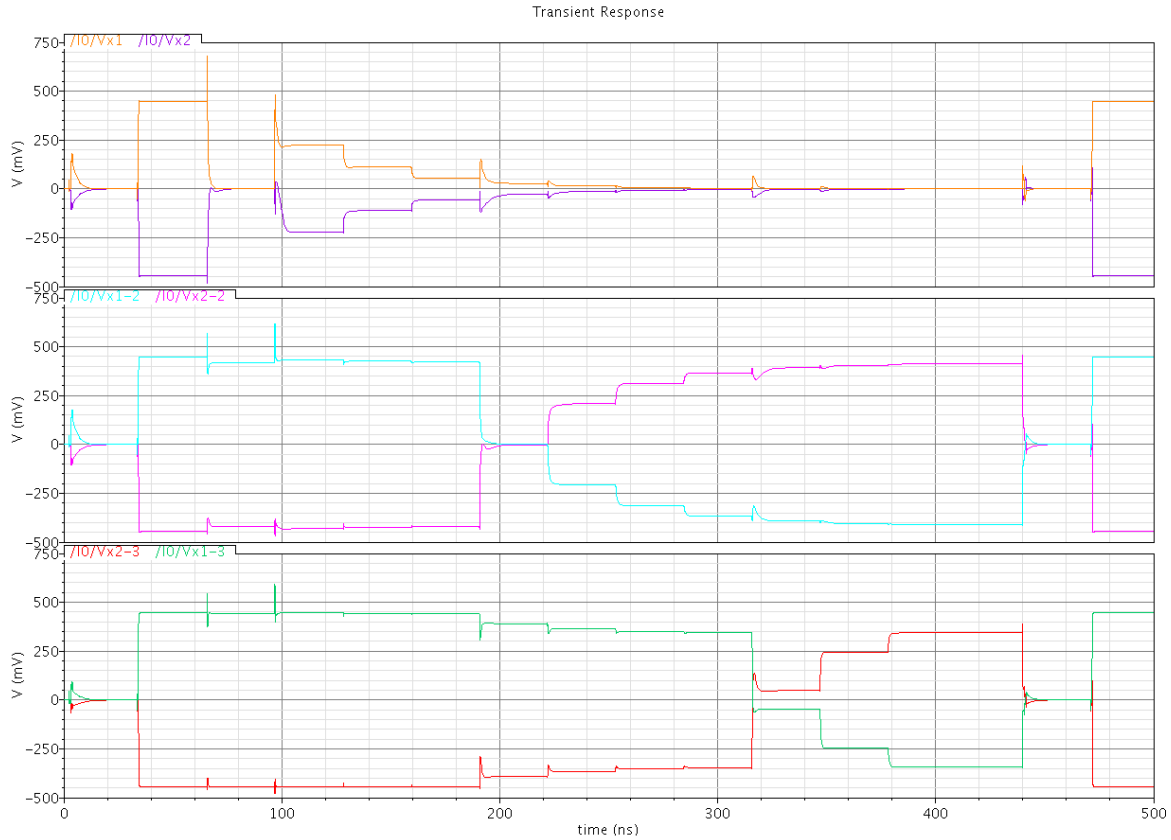


Figure 10-4 $V_{in} = -450mV$, analog signals. After the hold state, Vx becomes exactly equal to zero, theoretically. The comparator's response cannot be predicted. One of two possible output codes will be produced.

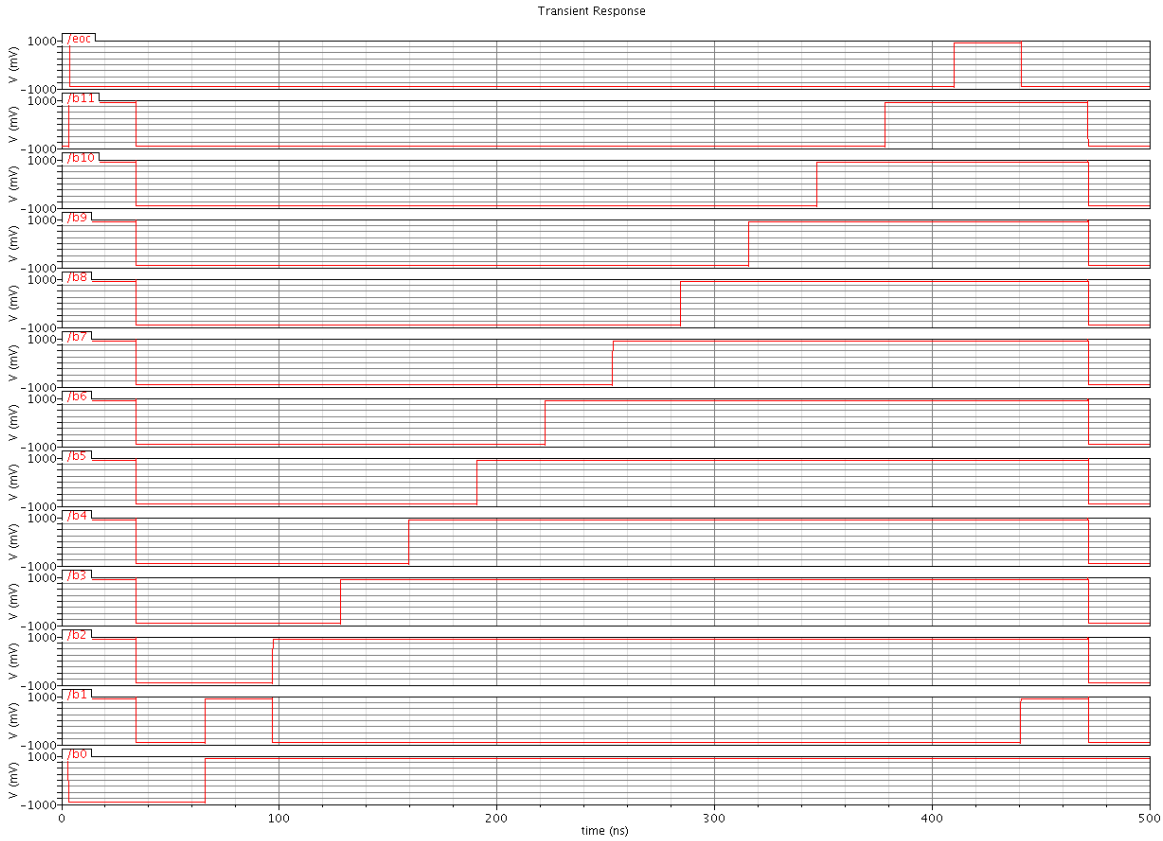


Figure 10-5 $V_{in} = -450mV$, digital signals. The output code 1011'1111'1111 has been produced.

10.2. Are there missing codes?

To rigorously test the ADC core, it must be verified that all 4'096 output codes are produced. The input signal to the ADC core is simply a ramp, as indicated on Figure 10-6 by the blue line, with an offset of $\pm 0.5V_{LSB}$ for the positive and negative part of the ideal transfer characteristic, respectively. With such ramps, a sample for each step's middle-point is converted.

A successful test means that there are no missing codes.

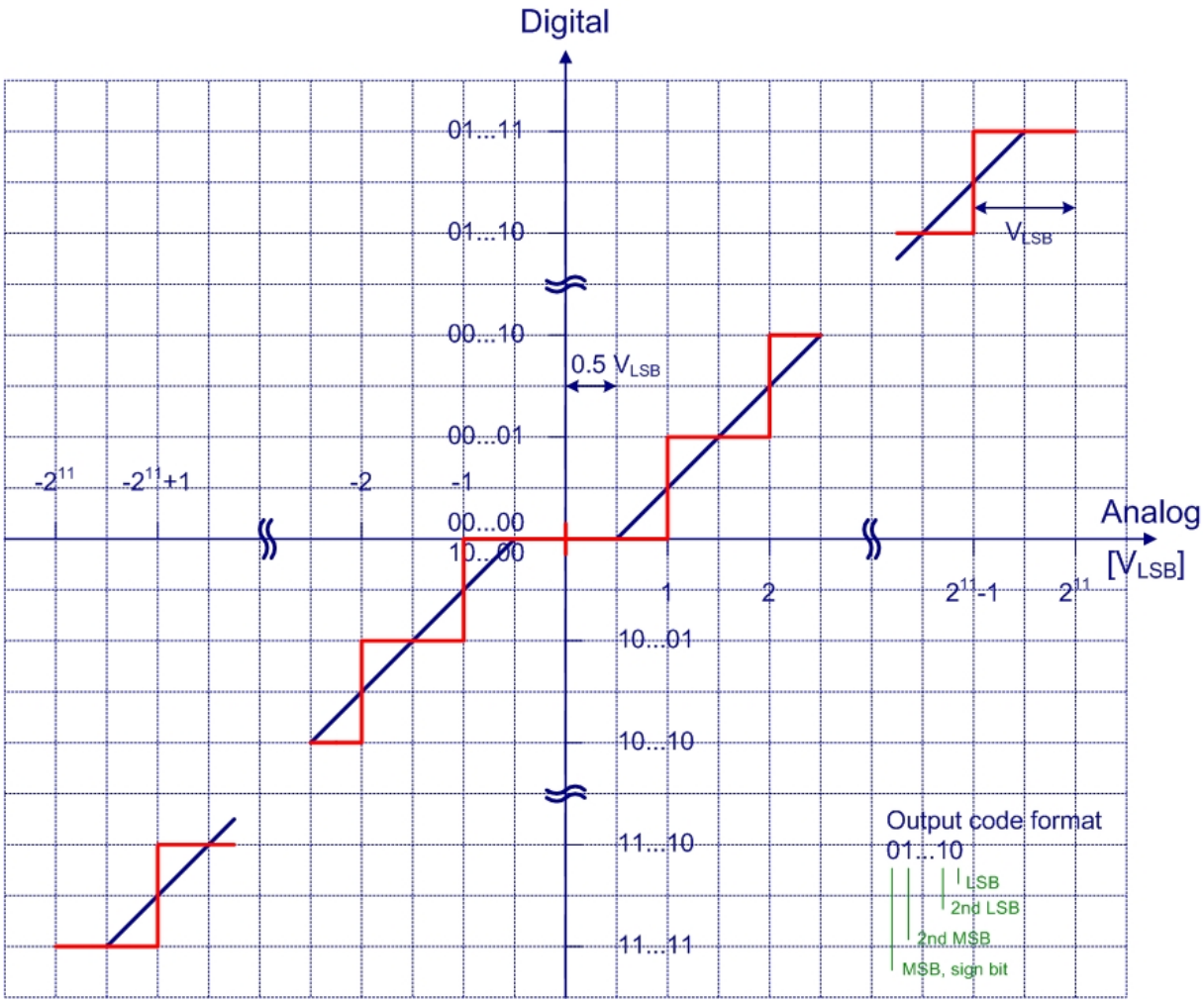


Figure 10-6 Ideal ADC transfer characteristic.

11. Conclusions

11.1. Achievements

After acquiring knowledge about neuroscience, specifications for an A/D converter to be integrated on a neurochip have been elaborated. Next, an extensive literature research has been made, in order to select the ADC architecture – among a large variety of architectures which have been presented so far – which will be most advantageous in the context of the neurochip. The SC SAR ADC architecture has been chosen because of its low power consumption, lack of latency, high enough resolution, high enough frequency to avoid parallelism, simple principle and its popularity in multiplexed data acquisition systems. Three blocks of the SC SAR ADC data acquisition have been identified: ADC front-end, ADC core and ADC back-end. Possibilities to implement the ADC front-end and back-end have been discussed. Then, more detailed specifications for the ADC core have been elaborated: its ideal transfer characteristic and timing diagrams have been defined. The following building blocks of the ADC core have been designed: comparator, capacitor array, SAR control logic, switches, delay elements and drivers. As soon as all building blocks met their requirements, they have been put together and pre-layout simulations of the entire ADC core have been carried out. These simulations confirm the correct operation of the ADC core.

A sampling frequency of 40*kSPS* per channel was required. The designed ADC reaches 46.65*kSPS* per channel if an external clock of 32*MHz* is used. Trimming the external clock to 27.44*MHz* would result in a sampling rate of exactly 40*kSPS* per channel.

11.2. Future work

The ADC front-end and back-end (if desired) and the layout of the whole ADC need to be done. For the layout of the digital part, I suggest a schematic capture and the use of a synthesizer. The bootstrapped switch needs to be reviewed; it seems there is a DC path to Vss during switching events. Eventually, if the ADC will be manufactured individually, I/O ESD protection circuits need to be designed.

The ADC core can be characterized (SFDR, SNDR and ENOB) by a DFT analysis.

After the layout is done, the effect of bottom plate parasitic capacitances of series capacitors on linearity must be studied. Eventually, series capacitors need to be shielded or alternatively, some capacitors need to be resized.

As soon as the ADC is manufactured, its DNL and INL can be determined.

11.3. Ideas to improve the current design

To increase the capacitance density and consequently decrease area, MIM capacitors can be replaced with Vertical Parallel Plates (VPP) or Vertical Bars (VB). VPPs use one lateral capacitance component, while VBs use both lateral capacitance components. None of VPP and VB uses the vertical capacitance component. VPP with a capacitance density of 1.51fF/um2 were manufactured and presented in [Aparicio2002]. Remind that MIM capacitors realized in UMC 0.18um CMOS technology have a capacitance density of merely $1 fF/\mu m^2$. In addition to higher capacitance densities, VPPs are expected to have good matching properties, as lateral dimensions are controlled by lithography and etching, whereas vertical dimensions are controlled by deposition, a less precisely

control manufacturing step. Also, VPPs and VBs have reduced bottom-plate capacitances when compared to parallel-plate or MIM capacitors, what makes them an interesting choice for split-array SAR ADCs.

Using Silicon on Insulator (SOI) technology, bottom-plate parasitic capacitances are eliminated [Culurciello2006]. SAR ADCs with split-capacitor arrays become very interesting and unproblematic in SOI technology.

The following solutions exist to integrate voltage references on-chip:

- Boost the supply voltage using a DC-DC converter, then use a bandgap voltage reference to produce stabilized reference voltages at ±900mV.
- Use the3.3V supply with corresponding transistors to power the bandgap voltage reference.
- From the 1.8V supply, try to reach stabilized voltages at roughly ±700mV or ±800mV using a bandgap voltage reference, and redesign the SC SAR ADC to operate from a reduced analog input range. The design becomes yet more challenging.

Lausanne, August 15, 2008

Pascal Meinerzhagen

References

[Abo1999]
Andrew Masami Abo, “Design for Reliability of Low-voltage, Switched-capacitor Circuits”, PhD Thesis, University of California, Berkeley, 1999

[Allen2002]
Phillip E. Allen, Douglas R. Holberg, “CMOS Analog Circuit Design”, Second Edition, Oxford University Press, 2002

[Aparicio2002]
Roberto Aparicio, Ali Hajimiri, “Capacity Limits and Matching Properties of Integrated Capacitors”, IEEE Journal of Solid-State Circuits, Vol. 37, No. 3. March 2002

[Aziz2006]
J. N. Y. Aziz, R. Karakiewicz, R. Genov, B. L. Bardakjian, M. Derchansky, P. L. Carlen, “Real-Time Seizure Monitoring and Spectral Analysis Microsystem”, IEEE 2006

[Baker2005]
R. Jacob Baker, “CMOS Circuit Design, Layout, and Simulation”, IEEE Press Series on Microelectronic Systems, 2005

[Bechen2006]
B. Bechen, D. Weiler, T.v.d. Boom, and B.J. Hosticka, “A 10 bit very low-power CMOS SAR-ADC for capacitive micro-mechanical pressure measurement in implants”, Adv. Radio Sci., 4, 243-246, 2006.

[Brown2000]
Stephen Brown, Zvonko Vranesic, “Fundamentals of Digital Logic with VHDL Design”, McGraw-Hill Higher Education, 2000

[CapLookUpTable]
Following files by UMC contain the capacitance look-up tables for the minimum, typical and maximum case, respectively.
G-4A-MIXED_MODE_RFCMOS18-1P6M-MMC_TOP_METAL8.6K-INTERCAP.min
G-4A-MIXED_MODE_RFCMOS18-1P6M-MMC_TOP_METAL8.6K-INTERCAP.typ
G-4A-MIXED_MODE_RFCMOS18-1P6M-MMC_TOP_METAL8.6K-INTERCAP.max
UMC Confidential no disclosure

[Cong2001]
Lin Cong, “Pseudo C-2C Ladder-Based Data Converter Technique”, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 48, No. 10. October 2001

[Cong2000]
Ling Cong, “A New Charge Redistribution D/A and A/D Converter Technique – Pseudo C-2C Ladder”, Proc. 43rd IEEE Midwest Symp. on Circuits and Systems, Lansing MI, Aug 8-11, 2000

[Culurciello2006]
Eugenio Culurciello, Andreas G. Andreou, “An 8-bit 800-uW 1.23-MS/s Successive Approximation ADC in SOI CMOS”, IEEE Transactions on Circuits and Systems-II: Express Briefs, Vol. 53, No. 9, Septemper 2006

[Egert1998]
U. Egert, B. Schlosshauer, S. Fennrich, W. Nisch, M. Fejtl, T. Knott, T. Müller, H. Hämmerle, "A novel organotypic long-term culture of the rat hippocampus on substrate-integrated multielectrode arrays", Brain Research Protocols 2 (1998) 229–242

[Eversmann2003]
Björn Eversmann et al., "A 128x128 CMOS Biosensor Array for Extracellular Recording of Neural Activity", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 38, NO. 12, DECEMBER 2003

[Frey2007]
Urs Frey et al., "An 11k-Electrode 126-Channel High-Density Microelectrode Array to Interact with Electrogenic Cells", IEEE ISSCC 2007, Session 8, Biomedical Devices, 8.4, pp. 158-593

[Hafizovic2006]
S. Hafizovic, "CMOS BIDIRECTIONAL ELECTRODE ARRAY FOR ELECTROGENIC CELLS", in Proc. IEEE MEMS 2006, pp. 4-7

[Heer2005]
Flavio Heer, "CMOS-based Microelectrode Array for Communication with Electrogenic Cells", DISS. ETH No. 16330, Swiss Federal Institute of Technology Zürich, Physical Electronics Laboratory, 2005

[Imfeld2008]
Kilian Imfeld et al., "Large-Scale, High-Resolution Data Acquisition System for Extracellular Recording of Electrophysiological Activity", IEEE TRANSACTIONS ON BIOMEDICAL ENGINEERING, VOL. 55, NO. 8, AUGUST 2008

[Jimbo2003]
Yasuhiko Jimbo, Nahoko Kasai, Keiichi Torimitsu, Takashi Tateno, and Hugh P. C. Robinson, "A System for MEA-Based Multisite Stimulation", IEEE TRANSACTIONS ON BIOMEDICAL ENGINEERING, VOL. 50, NO. 2, FEBRUARY 2003

[Johns1997]
David A. Johns, Ken Martin, "Analog Integrated Circuit Design", John Wiley & Sons, Inc., 1997 (Chapter 11 Data Converter Fundamentals, Chapter 13 Nyquiste-Rate A/D Converters and Chapter 14 Oversampling Converters)

[Joye2008]
Neil Joye, Maurizio Lavagnino, Alexandre Schmid, Yusuf Leblebici, "Three-dimensional Tip Electrode Array Technology for High Resolution Neuro-Electronic Systems used in Electrophysiological Experiments *in-vitro*", in Proc. 6th Int. Meeting on Substrate-Integrated Microelectrodes, pp. 310-311, 2008

[Joye2008-2]
Neil Joye, Alexandre Schmid, Yusuf Leblebici, "An Electrical Model of the Cell-Electrode Interface for High-Density Microelectrode Arrays", in the proceedings of IEEE EMBC 2008, to appear.

[Kang2003]
Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw-Hill Higher Education, 2003

[Kavak2004]
Fatih Kavak, "A Sizing Algorithm for Non-Overlapping Clock Signal Generation", Master's thesis, Electronics Systems at Linkoping Institute of Technology, 2004

[Kayal2008]
Maher Kayal, “Transistor-level Analog IC Design II”, Lecture Notes, Electronics Laboratory, Swiss Federal Institute of Technology, Lausanne, Switzerland, 2008

[Kester2005-1]
Walt Kester, "The Data Conversion Handbook", Analog Devices, Inc., 2005 (Chapter 3 Data Converter Architectures, Section 3-2 ADC Architectures and Section 3-3 Sigma-Delta Converter)

[Kester2005-2]
Walt Kester, "Which ADC Architecture is Right for Your Application?", Analog Dialogue 39-06, June 2005

[Liechti2004]
Thomas Liechti, “DESIGN OF A HIGH-SPEED 12-BIT DIFFERENTIAL PIPELINED A/D CONVERTER”, Diploma Project, Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland, 2004

[Lim]
Shin-Il Lim, “Comparator”, Lecture Notes, SeoKyegong University, 16-1 Jungneung-Dong Sungbuk-Ku Seoul, 136-704 Korea

[Lin2005]
Zengjin Lin, Haigang Yang, Lungui Zhong, Jiabin Sun, Shanhong Xia, “Modeling of Capacitor Array Mismatch Effect in Embedded CMOS CR SAR ADC”, Institute of Electronics, Chinese Academy of Sciences, Beijing, 100080, China, IEEE 2005

[Makinwa2002]
Kofi Makinwa, “Dynamic Offset-Cancellation Techniques”, Lecture Notes, Electronic Instrumentation Laboratory, DIMES, Delft University of Technology, Delft, The Netherlands, 2002

[Marom2002]
Shimon Marom, Goded Shahaf, “Development, learning and memory in large random networks of cortical neurons: lessons beyond anatomy”, Quarterly Reviews of Biophysics 35, I, pp. 63-87, 2002

[Martin1997]
David A. Johns, Ken Martin, “Analog Integrated Circuit Design”, John Wiley & Sons, Inc., 1997 (Chapter 13, Nyquist-Rate A/D Converters)

[Pelgrom2007]
M. Pelgrom, I. Galton, U.-K. Moon, Advanced Engineering Course on High-Speed Data Converters, Electronics Laboratories, Lausanne, Switzerland, June 25-29, 2007 (Slide 72 Comparison)

[Plassche2003]
Rudy van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", 2nd Edition, Kluwer Academic Publishers, 2003

[Potter2007]
Steve M. Potter, “What can AI Get from Neuroscience?”, 50 Years of AI, Festschrift, LNAI 4850, pp. 174-185, Springer-Verlag Berlin Heidelberg 2007

[Promitzer2001]
Gilbert Promitzer, "12-bit Low-Power Fully Differential Switched Capacitor Noncalibrating Successive Approximation ADC with 1 MS/s", IEEE Journal of Solid-State Circuits, Vol. 36, No. 7, July 2001

[Razavi2001]
Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill Higher Education, 2001

[Stett2003]
Alfred Stett, Ulrich Egert, Elke Guenther, Frank Hofmann, Thomas Meyer, Wilfried Nisch, Hugo Haemmerle, “Biological application of microelectrode arrays in drug discovery and basic research”, Anal Bioanal Chem 377, pp. 486-495, 2003

[UMC1.8VPMR]
“0.18um Mixed-Mode 1.8V Process Matching Report”, Ver. 1.0_P.1, Approved Date 03/08/2005, UMC CONFIDENTAL, NO DISCLOSURE

[UMCCapChar]
“0.18 um Mixed-Mode Process Al Metal Metal Capacitor Characterization Report (Ver. 1.0_P.1)”, Approved Date: 02/24/2005, UMC Confidential no disclosure

[Wagenaar2005]
Daniel A. Wagenaar, Radhika Madhavan, Jerome Pine, and Steve M. Potter, “Controlling Bursting in Cortical Cultures with Closed-Loop Multi-Electrode Stimulation”, The Journal of Neuroscience, January 19, 2005, 25(3):680–688

[Watanabe2006]
T. Watanabe et al., “Novel Retinal Prosthesis System with Three Dimensionally Stacked LSI Chip”, in Proc. IEEE ESSDERC 2006, pp. 327-330

Swiss Federal Institute of Technology, Lausanne
Microelectronic Systems Laboratory

Lausanne, September 1, 2008

University of California, Merced
School of Engineering

Add-on to: "Design of a 12-bit low-power SAR A/D Converter for a Neurochip"

Master's Thesis

Pascal Meinerzhagen, EPFL

Supervisors

Neil Joye, EPFL

Yusuf Leblebici, EPFL

Sangho Shin, UC Merced

Shin-Il Lim, SeoKyeong University

Table of Contents

Table of Figures

Table of Tables

Table of Codes

1. DFT analysis

1.1. Tutorial: DFT[1] analysis in Cadence

The test signal is a sine wave with full-range amplitude – here, $V_{in} = 900mV$ – and frequency f_{in} given by Eq. (1-1).

$$f_{in} = \frac{P \cdot f_S}{N} \tag{1-1}$$

where P is a prime number, N is the number of samples, and f_S the sampling frequency of the ADC. f_S must be an exact value. Here, we assume that 49 channels need to be sampled at a rate of $40kSPS$ each, which results in exactly $f_S = 1.96MHz$. If the ADC needs 14 cycles for each A/D conversion, its internal clock frequency[2] needs to be $f_i = 14 \cdot f_S = 27.44MHz$. If $P = 3$, $N = 64$ and $f_S = 1.96MHz$, then $f_{in} = 91.875kHz$.

Make sure that the output codes are kept during a full sampling period $T_S = 1/f_S = 510.204ns$. If your ADC does it, you are fine, else add DFFs at the output of your ADC, as shown on Figure 1-1. These DFFs may be triggered by the *eoc* signal.

The simulated time must be at least:

$$T_{sim} = N \cdot T_S + T_{start-up} + T_{latency} \tag{1-2}$$

where

- $T_{start-up}$ is the time interval from the instant the ADC is started up to the instant it takes the first sample.
- $T_{latency}$ is the time interval from the instant the ADC takes a sample to the instant it delivers the corresponding output code.

In a first approximation, we can write $T_{start-up} = T_i$ and $T_{latency} = 12 \cdot T_i$, where $T_i = 1/f_i = 36.443ns$. Eq. (1-2) evaluates to $T_{sim} = 33.127\mu s$. Depending on the ADC being characterized, it might be necessary to simulate some "useless" A/D conversions until the ADC is in an established state and take useful data for the DFT analysis only afterwards. In this case, T_{sim} needs to be accordingly increased.

---

[1] DFT is the abbreviation of Discrete Fourier Transform. The DFT allows a *sampled time domain signal* to be converted into its equivalent representation in the frequency domain. In the context of ADC testing, some authors use the term Fast Fourier Transform (FFT), rather than DFT. In fact, the FFT is simply an algorithm for efficiently calculating the DFT.

[2] Do not confuse the internal clock frequency f_i and the input frequency f_{in}.

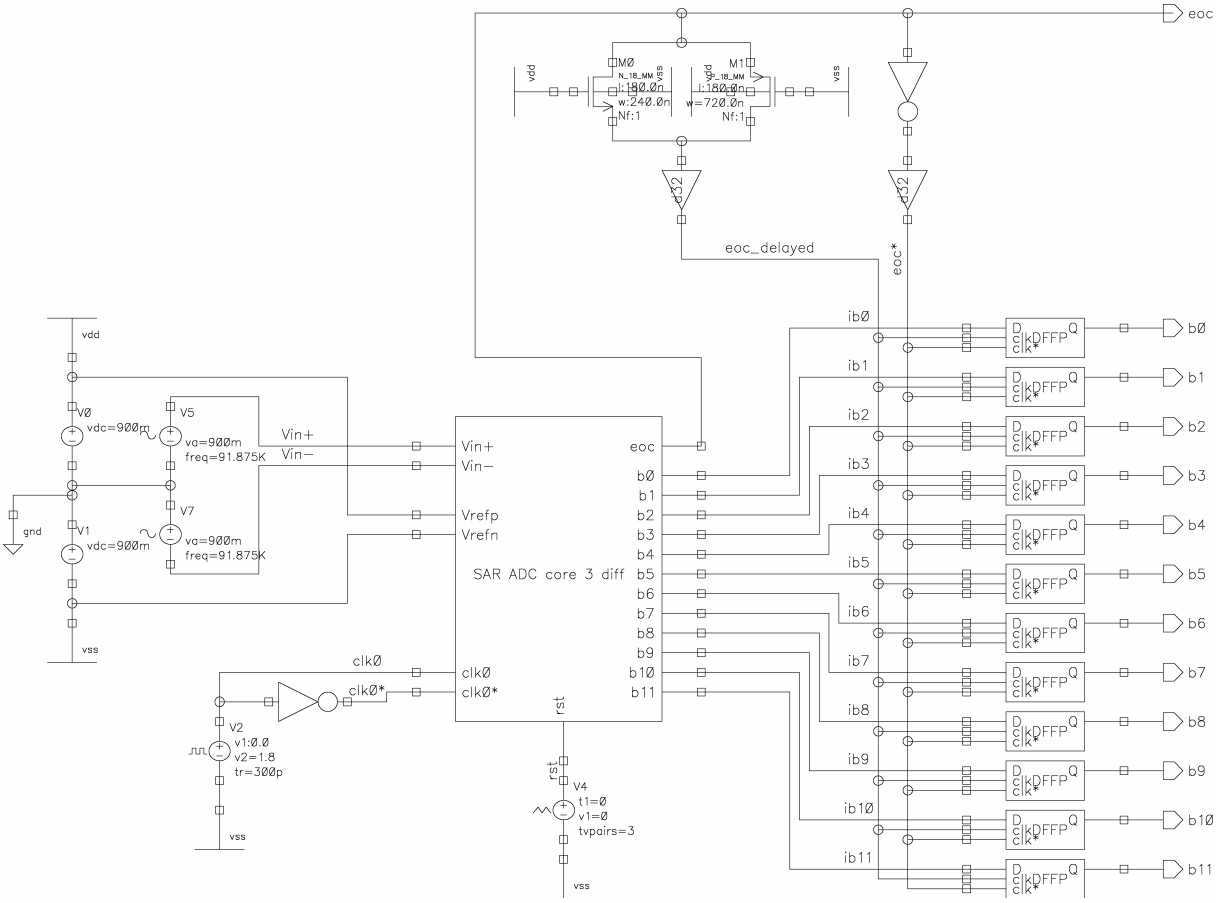


Figure 1-1 Testbench used for the DFT analysis. To keep output codes over a full sampling period T_S, DFFs were added at the output of the ADC.

Run the transient simulation with input signal and simulated time as discussed above. Depending on the number of samples, the simulation time[1] can be very long. On a $4x2.4GHz$ dual-core AMD 880, $32GB$ RAM Cadence server, and with $N = 64$, it takes 4 to $5h$.

As soon as the transient simulation has completed, we use an ideal DAC to restore an analog waveform from the N digital output codes. We can simply use Cadence's calculator to implement the DAC. Depending on the output code representation (binary offset, sign magnitude, 1's complement, 2's complement, etc.) and the definition of logic '0' and logic '1', the expression to be evaluated by the calculator varies. For example, if the output code is given in sign magnitude representation and logic '0' and '1' correspond to $-900mV$ and $900mV$, respectively, the DAC is simulated using Code 1-1.

```
(-1)*VT("/b0")/.9 * ((VT("/b1")+.9)*0.25 + (VT("/b2")+.9)*0.125 + (VT("/b3")+.9)*(2**-4) +
(VT("/b4")+.9)*(2**-5) + (VT("/b5")+.9)*(2**-6) + (VT("/b6")+.9)*(2**-7) +
(VT("/b7")+.9)*(2**-8) + (VT("/b8")+.9)*(2**-9) + (VT("/b9")+.9)*(2**-10) +
(VT("/b10")+.9)*(2**-11) + (VT("/b11")+.9)*(2**-12))
```

Code 1-1 DAC expression.

[1] Do not confuse *simulated time* and *simulation time*.

In Code 1-1, VT("/b0") is the waveform corresponding to the MSB or sign bit b0, while VT("/b1") through VT("/b11") are the waveforms corresponding to bits b1 through b11. The notation x**y means x^y.

As soon as you have entered Code 1-1 into the calculator, click "plot" and observe the reconstructed analog signal in the window that pops up. Do very accurately determine the time instant at which the first useful sample has just settled.

Next, the DFT of Code 1-1 is computed. In the calculator window, click on "Special Functions", then "dft…". The window shown in Figure 1-2 will pop up.

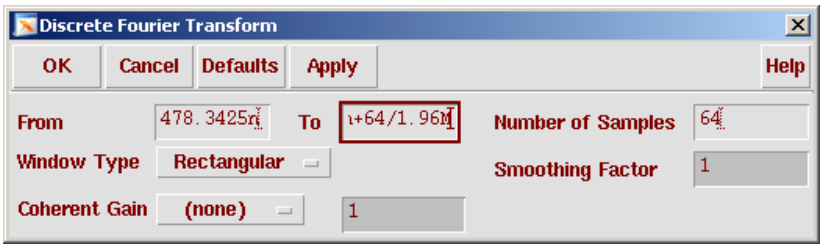


Figure 1-2 Discrete Fourier Transform in Cadence.

Make sure to indicate start time ("From" field), stop time ("To" field), and the "Number of Samples". As for start and stop time, enter with the highest numerical precision possible the time instant at which the first useful sample has settled and the time instant till which the last sample is kept. In order to take advantage of Cadence's built-in maximum numerical precision, use expressions containing exact numerical values rather than approximated numbers. Of course, "Number of Samples" must be the exact number of samples included between start and stop time, 64 samples in this example. Click "OK". The calculator contains now Code 1-2.

```
dft(Code 1-1,478.3425n,478.3425n+64/1.96M,64,"Rectangular",1,1)
```

Code 1-2 DFT.

Now, simply click "plot", and the N-point DFT magnitude data will pop up. In order to plot the data in a meaningful way, the magnitude data must be converted to decibels (dB), which can be done using Eq. (1-3) [Kester2005].

$$dB = 10\log_{10}\left[\frac{Magnitude^2}{Magnitude_{Max}{}^2}\right] = 20\log_{10}\left[\frac{Magnitude}{Magnitude_{Max}}\right] \qquad (1\text{-}3)$$

where

- $Magnitude$ is the individual array elements computed by the FFT
- $Magnitude_{Max}$ is the maximum magnitude element in the array

$Magnitude_{Max}$ can be determined either graphically or using ymax(abs(**Code 1-2**)). Using the latter way, the normalized DFT in dB is obtained as:

```
dB20((Code 1-2)/ymax(abs(Code 1-2)))
```

Code 1-3 Normalized DFT in dB.

Substituting Code 1-2 in Code 1-3, and Code 1-1 in Code 1-2, the final expression to be plotted becomes:

```
dB20(dft((-1) * VT("/b0")/.9 * ((VT("/b1")+.9)*0.25 + (VT("/b2")+.9)*0.125 +
(VT("/b3")+.9)*(2**-4) + (VT("/b4")+.9)*(2**-5) + (VT("/b5")+.9)*(2**-6) +
(VT("/b6")+.9)*(2**-7) + (VT("/b7")+.9)*(2**-8) + (VT("/b8")+.9)*(2**-9) +
(VT("/b9")+.9)*(2**-10) + (VT("/b10")+.9)*(2**-11) + (VT("/b11")+.9)*(2**-12)),
478.3425n, 478.3425n+64/1.96M, 64, "Rectangular", 1, 1) / ymax(abs(dft((-1) *
VT("/b0")/.9 * ((VT("/b1")+.9)*0.25 + (VT("/b2")+.9)*0.125 + (VT("/b3")+.9)*(2**-4) +
(VT("/b4")+.9)*(2**-5) + (VT("/b5")+.9)*(2**-6)+(VT("/b6")+.9)*(2**-7) +
(VT("/b7")+.9)*(2**-8) + (VT("/b8")+.9)*(2**-9) + (VT("/b9")+.9)*(2**-10) +
(VT("/b10")+.9)*(2**-11) + (VT("/b11")+.9)*(2**-12)), 478.3425n, 478.3425n+64/1.96M,
64, "Rectangular", 1, 1))))
```

Code 1-4 Final expression to be plotted.

In a different approach, the waveforms corresponding to b0 – b11 can be sampled at sampling rate T_S and exported in tabular form after the transient simulation. The reconstruction of the analog signal and the computation of the FFT can then be done in MATLAB.

The following three definitions are taken from [Kester2005]:

Effective Number of Bits (ENOB). With a sinewave input, Signal-to-Noise-and-Distortion (SINAD) can be expressed in terms of the number of bits. Rewriting the theoretical SNR formula for an ideal N-bit ADC and solving for N:

$$N = \frac{SNR - 1.76dB}{6.02} \tag{1-4}$$

The actual ADC SINAD is measured using FFT techniques, and ENOB is calculated from:

$$ENOB = \frac{SINAD - 1.76dB}{6.02} \tag{1-5}$$

Signal-to-Noise-and-Distortion Ratio (SINAD). The ratio of the rms signal amplitude (set 1 dB below full-scale to prevent overdrive) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Spurious-Free Dynamic Range (SFDR). The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (related back to converter full-scale).

In the literature, SINAD is also referred to as *S/N+D* and *SNDR*.

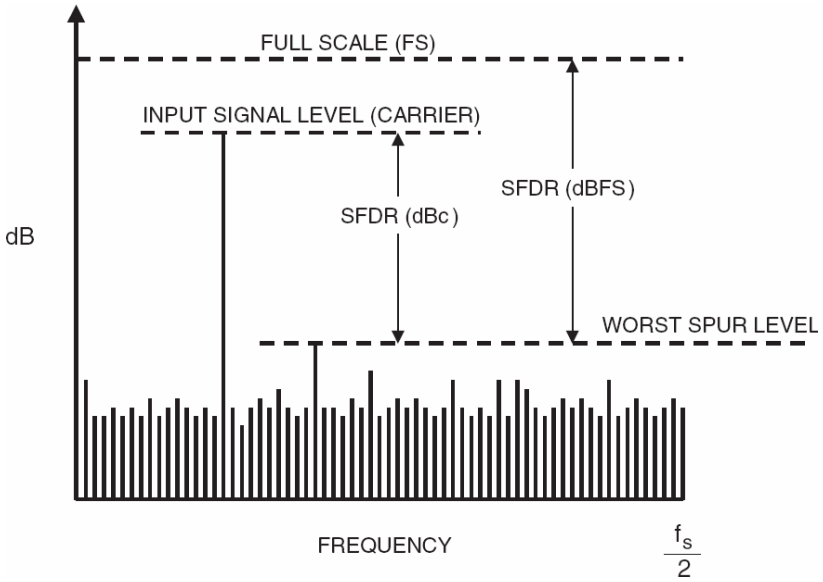


Figure 1-3 Definition of SFDR [Kester2005].

The SFDR can be determined graphically from the DFT signal. Clearly, SFDR is reported in dBc here.

For a first estimation of ENOB, the following observation might be interesting: If we calculate SINAD from a set of data and graphically determine SFDR from the same set of data, following approximate relation between SINAD and SFDR is found[1]:

$$SFDR \cong SINAD + 10dB \tag{1-6}$$

To accurately determine ENOB, we calculate SINAD according to above definition. One convenient way to do it is:

- Navigate to Analog Design Environment → Session → Options… and choose WaveScan as Waveform Tool
- Open a new calculator: Analog Design Environment → Tools → Calculator
- Copy & Paste **Code 1-2** into the calculator, substituting **Code 1-1**
- Choose Calculator → Tools → Table or click on the corresponding symbol, located next to the plot symbol
- In the Calculator Results Display window, choose Value as Data
- In the Table window, choose File → Save as CSV…
- Import the CSV file into MS Excel and calculate SINAD according to the above definition

1.2. Characterization of the ADC core

Neither offset voltage of the comparator nor offset cancellation circuitry is included in the transient simulation. Data extracted from layout is not included either.

Figure 1-4 shows the full-range input signal – shown as single-ended signal here –, and the analog signal reconstructed from the digital output codes, assuming an ideal DAC implemented with Cadence's calculator and $V_{ref} = 900mV$. The ADC's latency is $T_{latency} = 12 \cdot T_i$, while the DAC has

[1] I could not find this or a similar relation published. This result was suggested by Jae Jin Jung, who has designed and characterized a lot of ADCs.

no latency. As the additional DFFs shown on Figure 1-1 do eventually not change their state at exactly the same time, there are some glitches in the reconstructed analog signal.

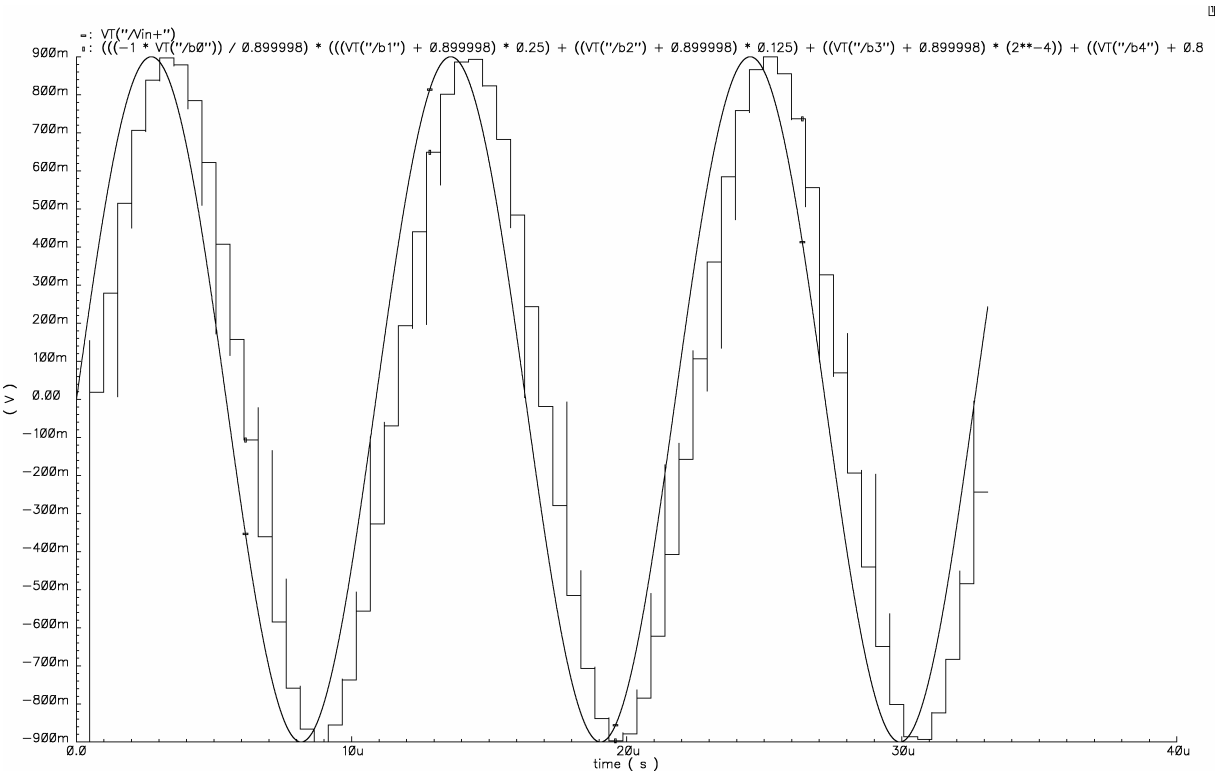


Figure 1-4 Transient simulation results: input signal and reconstructed analog signal.

To get a first impression of the ADC's accuracy, let us compare the reconstructed analog signal with a signal obtained by sampling and holding the full-rang input signal. Figure 1-5 (Top trace) shows the sampled-and-held analog signal, which – by design of the experiment – is not quantized in amplitude. For comparison, Figure 1-5 (Bottom trace) shows again the reconstructed analog signal. The input signal of the ideal S/H stage is delayed by $12 \cdot T_i$ with respect to the ADC's input signal, while the signal defining the S/H stage's sampling instants is delayed by $13 \cdot T_i$ with respect to the ADC's input signal. This way, the sampled-and-held and the reconstructed analog signal make their transitions at the same time, even though the ideal S/H stage has no latency, and can easily be compared.

As can be seen on Figure 1-6, the reconstructed analog signal and the sampled-and-held signal coincide very well. According to the ADC's ideal transfer characteristic (*Figure 4-3* in [Meinerzhagen2008]), the sampled-and-held signal – which is not quantized in amplitude – is allowed to deviate by $0.5V_{LSB} = 219\mu V$ from the reconstructed signal. For $DNL \leq 0.5V_{LSB}$, the deviation is allowed to be up to $V_{LSB} = 439\mu V$.

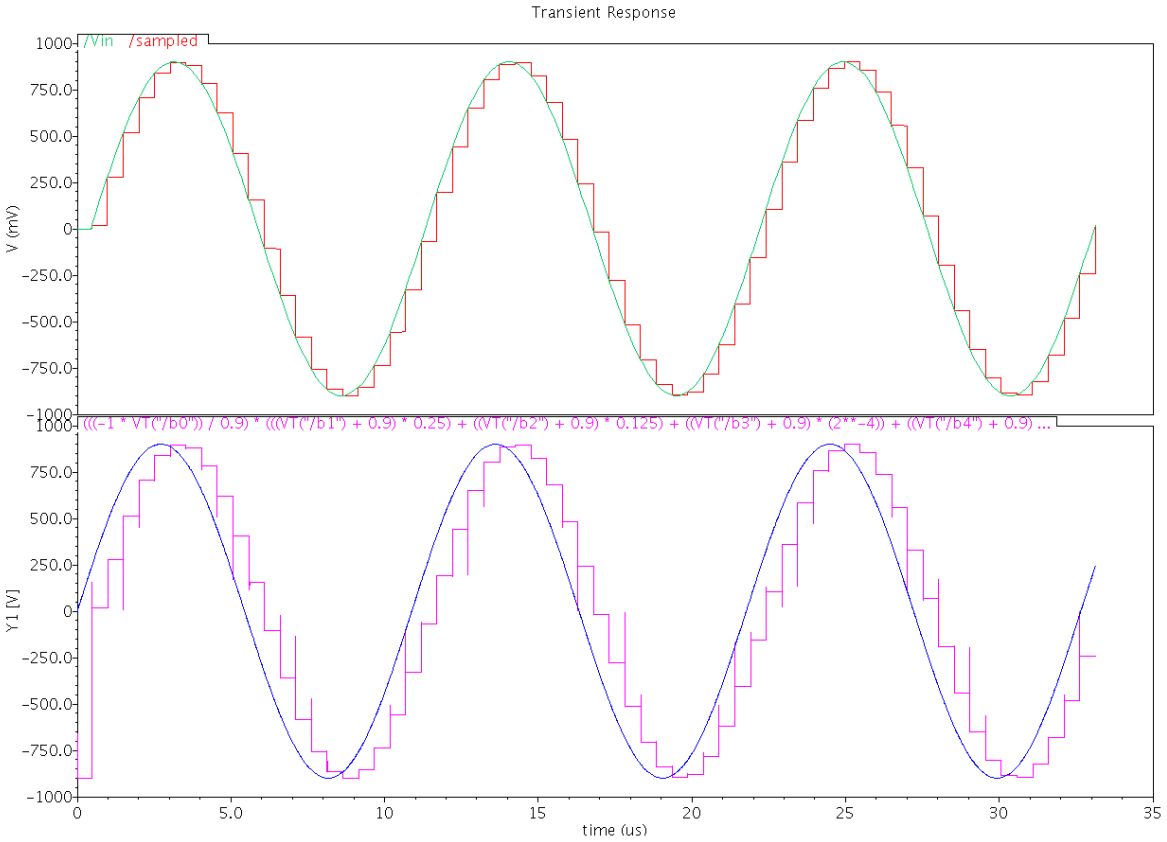


Figure 1-5 (Top trace) Sampled-and-held analog signal and (Bottom trace) reconstructed analog signal.

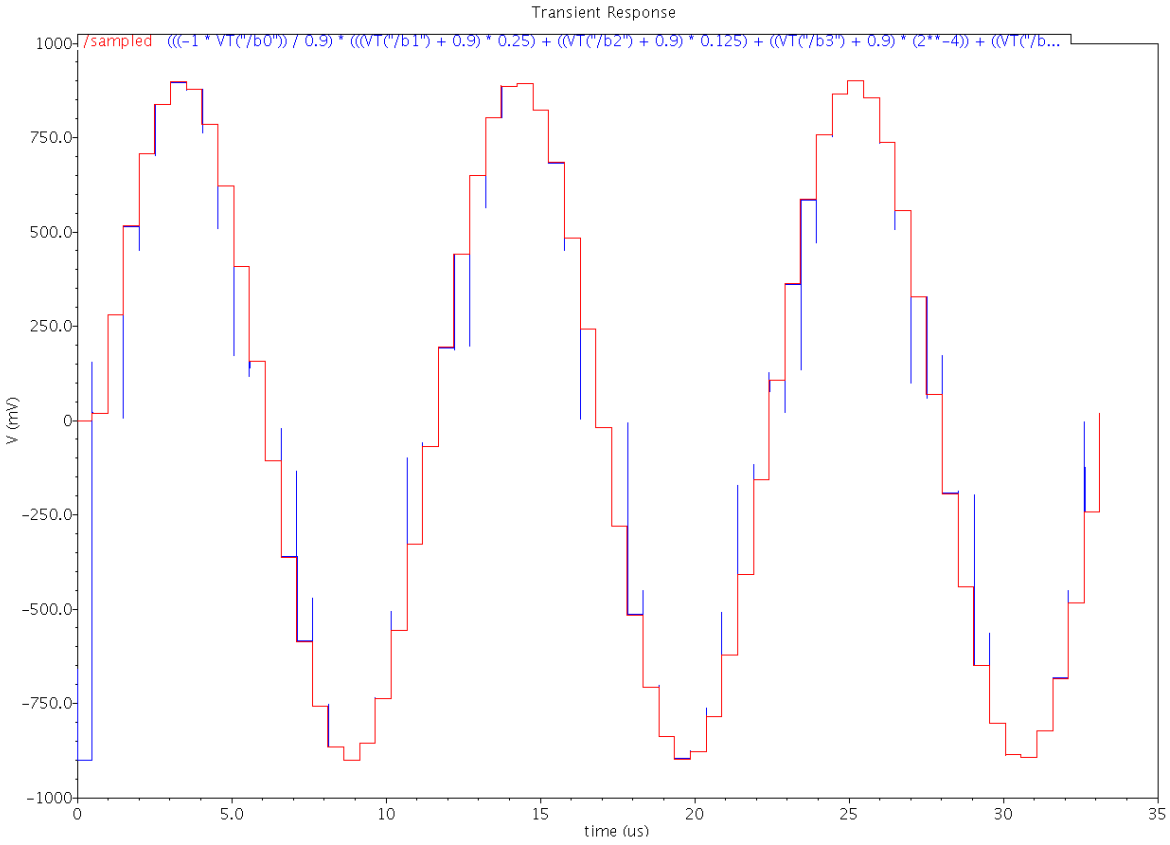


Figure 1-6 Sampled-and-held analog signal (red) and reconstructed analog signal (blue).

Figure 1-7 shows the 64-point DFT signal of the reconstructed analog signal. The highest peak ($0dB$) is at $f_{in} = 91.875kHz$, while the last peak is at $f_S / 2 = 980kHz$. The DFT signal has no harmonics of f_{in}. In fact, in order to prevent repetitive data patterns, we have chosen P a prime number in Eq. (1-1), and not any other integer number. Graphically from Figure 1-7, $SFDR = 72.0701dBc$.

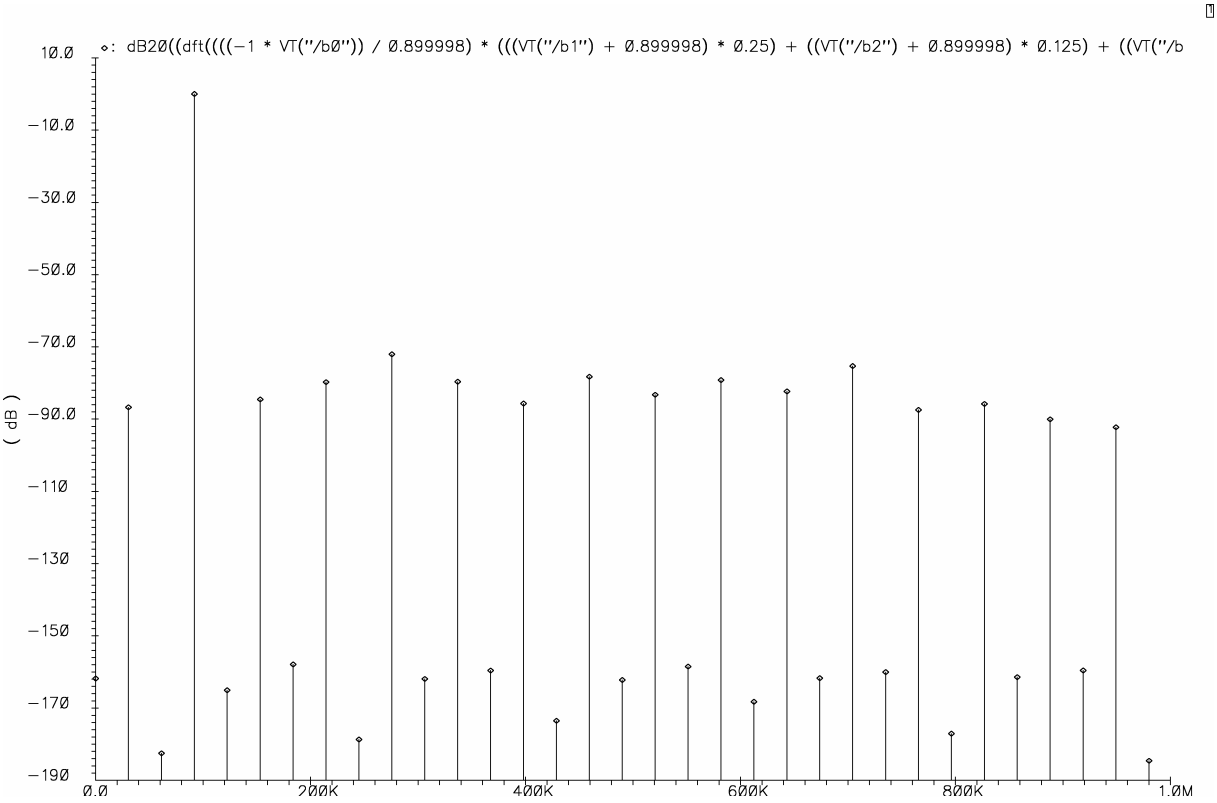


Figure 1-7 64-point DFT signal of the reconstructed analog signal.

From the 64-point DFT magnitude data shown in Table 1-1, $SINAD = 67.84206dB$.

f [Hz]	Mag. [V]	f [Hz]	Mag. [V]	f [Hz]	Mag. [V]
0	7.27E-09	3.37E+05	9.34E-05	6.74E+05	7.37E-09
3.06E+04	4.13E-05	3.68E+05	9.38E-09	7.04E+05	1.54E-04
6.13E+04	6.72E-10	3.98E+05	4.66E-05	7.35E+05	8.94E-09
9.19E+04	0.8996	4.29E+05	1.89E-09	7.66E+05	3.81E-05
1.23E+05	5.01E-09	4.59E+05	1.10E-04	7.96E+05	1.26E-09
1.53E+05	5.32E-05	4.90E+05	6.94E-09	8.27E+05	4.60E-05
1.84E+05	1.14E-08	5.21E+05	6.16E-05	8.58E+05	7.61E-09
2.14E+05	9.22E-05	5.51E+05	1.07E-08	8.88E+05	2.82E-05
2.45E+05	1.04E-09	5.82E+05	9.86E-05	9.19E+05	9.41E-09
2.76E+05	2.24E-04	6.13E+05	3.47E-09	9.49E+05	2.19E-05
3.06E+05	7.19E-09	6.43E+05	6.86E-05	9.80E+05	5.28E-10

Table 1-1 64-point DFT magnitude data.

Finally, using Eq. (1-5), $ENOB = 10.97709$.

Even though a 64-point DFT analysis reveals much information, a typical FFT size to test a 12-bit ADC is $N = 2^{14} = 16'384$ in practice [Kester2005].

2. Effect of bottom-plate parasitic capacitances of series capacitors

2.1. Numerical value of parasitic capacitances

A square MIM capacitor with $W = L = 15.66\mu m$ has a nominal capacitance of $C_u = 249.9336\,fF$ and a bottom-plate parasitic capacitance of $C_p = 1.8056\,fF$ [Meinerzhagen2008]. As $C_{s1} = 16/15 \cdot C_u$ and $C_{s2} = 8/7 \cdot C_u$ (see Figure 2-1), the bottom-plate parasitic capacitances of C_{s1} and C_{s2} become $C_{s1,p} = 1.9259\,fF$ and $C_{s2,p} = 2.0635\,fF$, respectively.

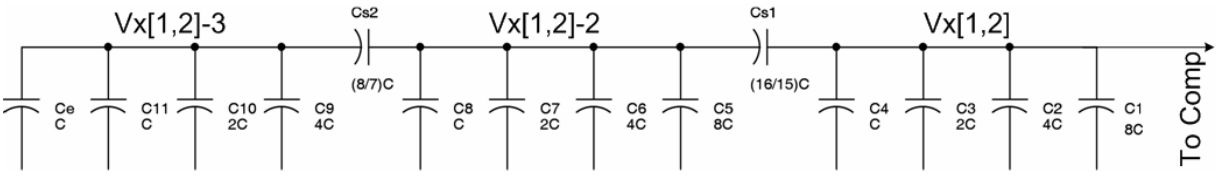


Figure 2-1 *3bw2Cs* capacitor array. $C = C_u$.

2.2. Set-up of experiment

The bottom-plate parasitic capacitances $C_{s1,p}$ and $C_{s2,p}$ are inserted between the bottom-plates of the series capacitors and V_{SS}. Next, the conversion of the full-range sample $V_{in} = 900mV$ is simulated, with and without bottom-plate parasitic capacitances. Additionally, in order to better understand the effect of bottom-plate parasitic capacitances, $C_{s1,p}$ and $C_{s2,p}$ are multiplied by 10, then by 100. To simulate all four scenarios at the same time and easily compare results, we define the parasitic capacitances as $C_{s1,p} = \alpha \cdot 1.9259\,fF$ and $C_{s2,p} = \alpha \cdot 2.0635\,fF$, and run a parametric analysis with sweep parameter $\alpha = [0,1,10,100]$. At the risk of stating the obvious, $\alpha = 0$ corresponds to the ideal case without bottom-plate parasitic capacitances, while $\alpha = 1$ corresponds to the real case. Table 2-1 summarizes the four scenarios and defines a waveform color for each scenario.

	Ideal case	Reality	Reality $x10$	Reality $x100$
α	0	1	10	100
iteration_sweep1	1	2	3	4
Waveforms	Red	Blue	Green	Black

Table 2-1 Effect of bottom-plate parasitic capacitances: Ideal case, reality and augmented reality.

2.3. Results

In all scenarios, the correct output code $0111'1111'1111$ is obtained, as suggested by Figure 2-2.

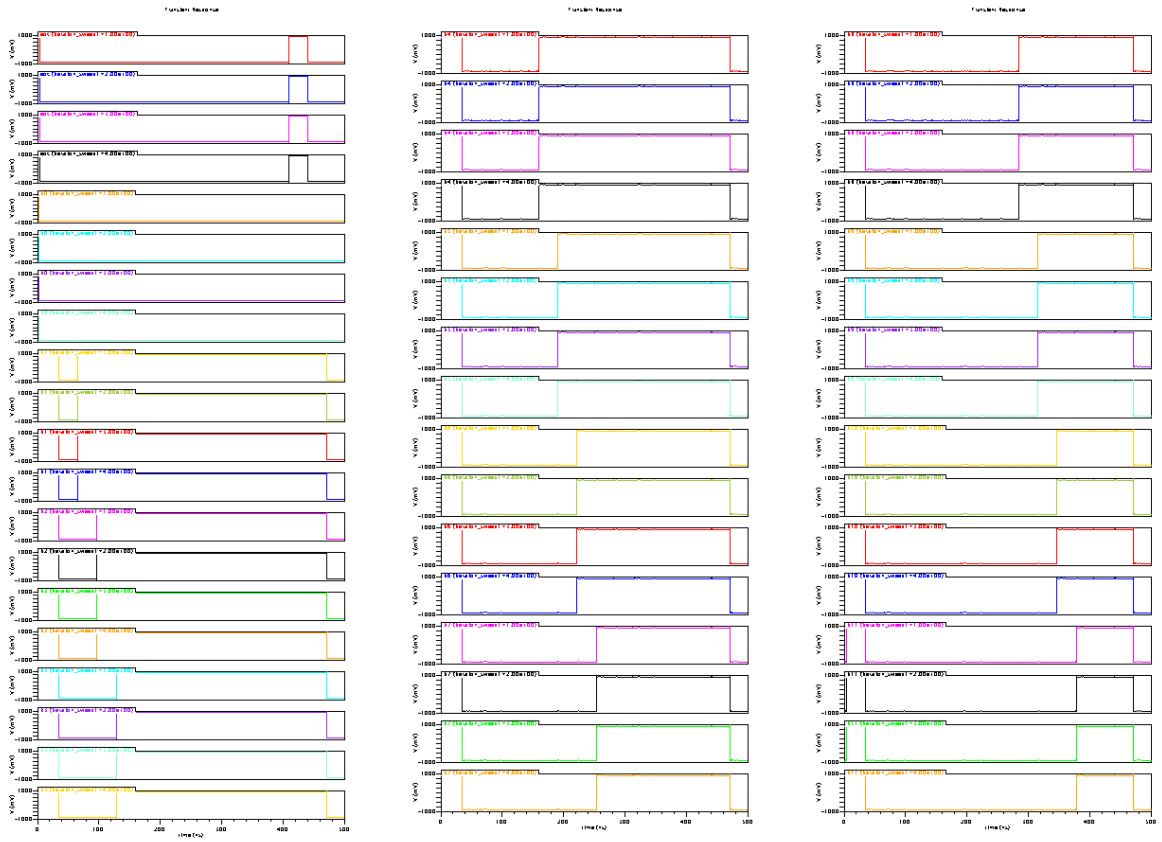


Figure 2-2 Digital output codes, presented in packets of four corresponding to $\alpha = [0,1,10,100]$. The packets are: (Left column, top to bottom) eoc, b0 – b3, (Middle column, top to bottom) b4 – b7, (Right column, top to bottom) b8 – b11.

To understand the effect of bottom-plate parasitic capacitances, the voltage waveforms at nodes Vx1-3, Vx2-3, Vx1-2, Vx2-2, Vx1 and Vx2 are observed (see Figure 2-1 for naming conventions). Waveforms are presented in the following order:

- LSB capacitor array, Vx[1,2]-3
- Middle capacitor array, Vx[1,2]-2
- MSB capacitor array, Vx[1,2]

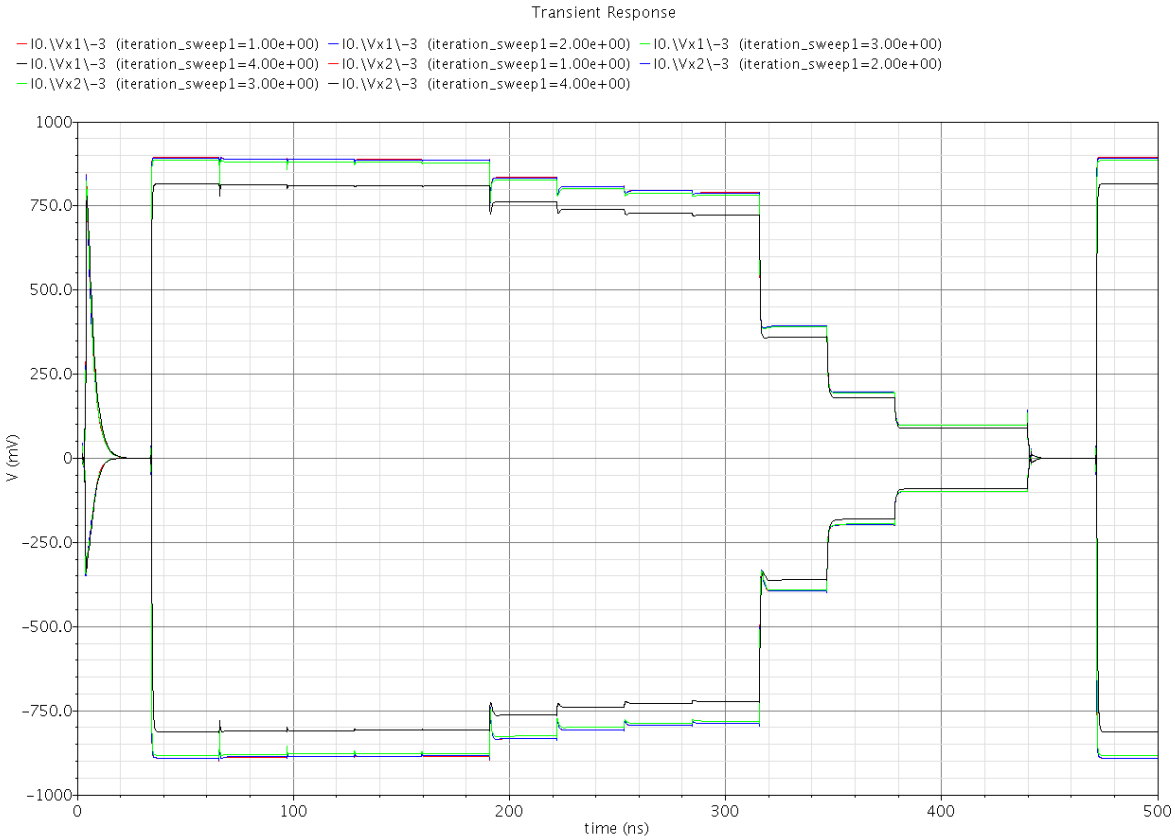


Figure 2-3 Waveforms at nodes Vx[1,2]-3 for $\alpha = 0,1,10,100$.

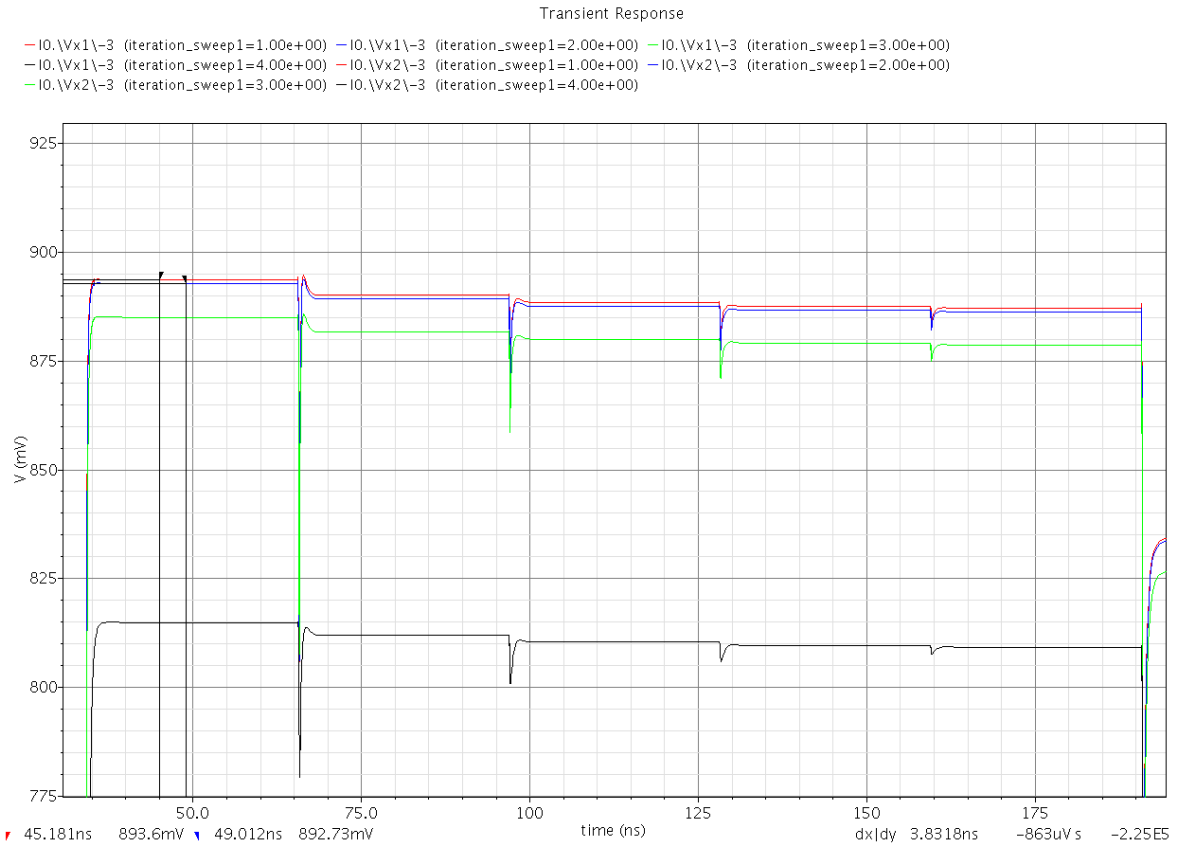


Figure 2-4 Detail of Figure 2-3 showing settling before MSB, b1 – b4 decisions.

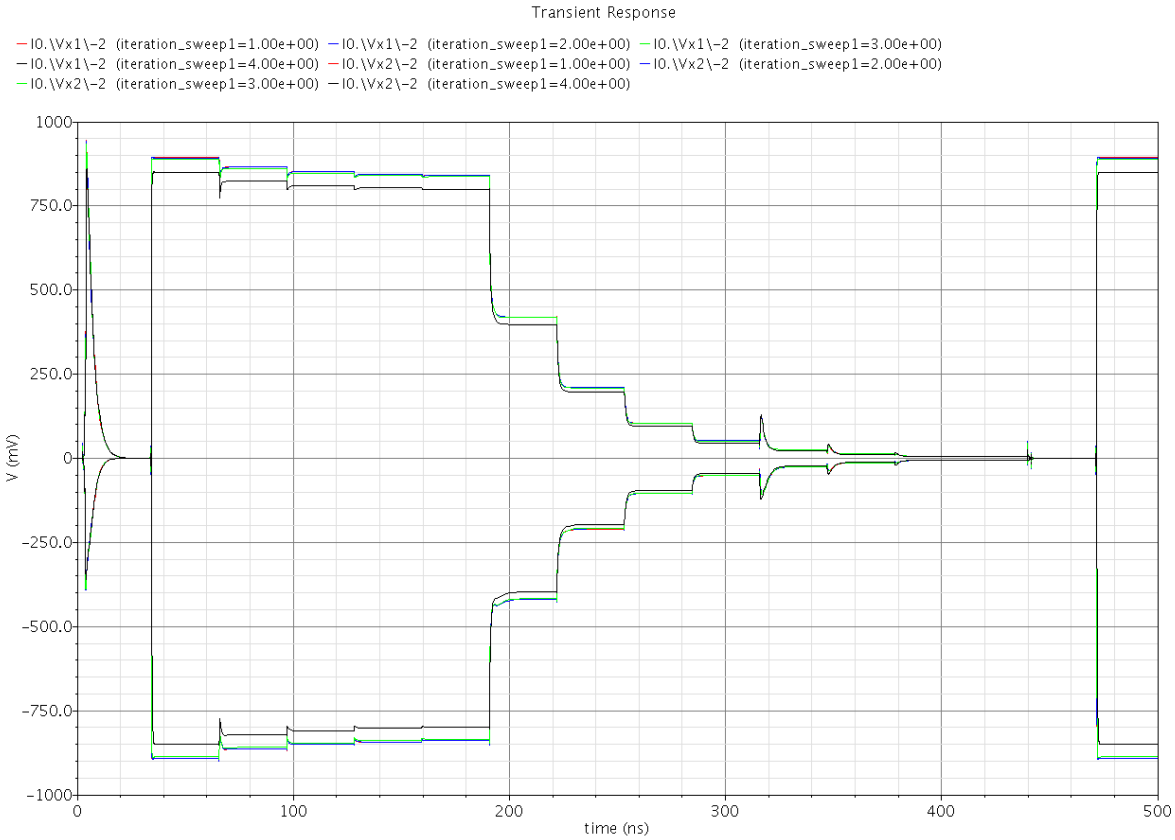


Figure 2-5 Waveforms at nodes Vx[1,2]-2 for $\alpha = 0,1,10,100$.

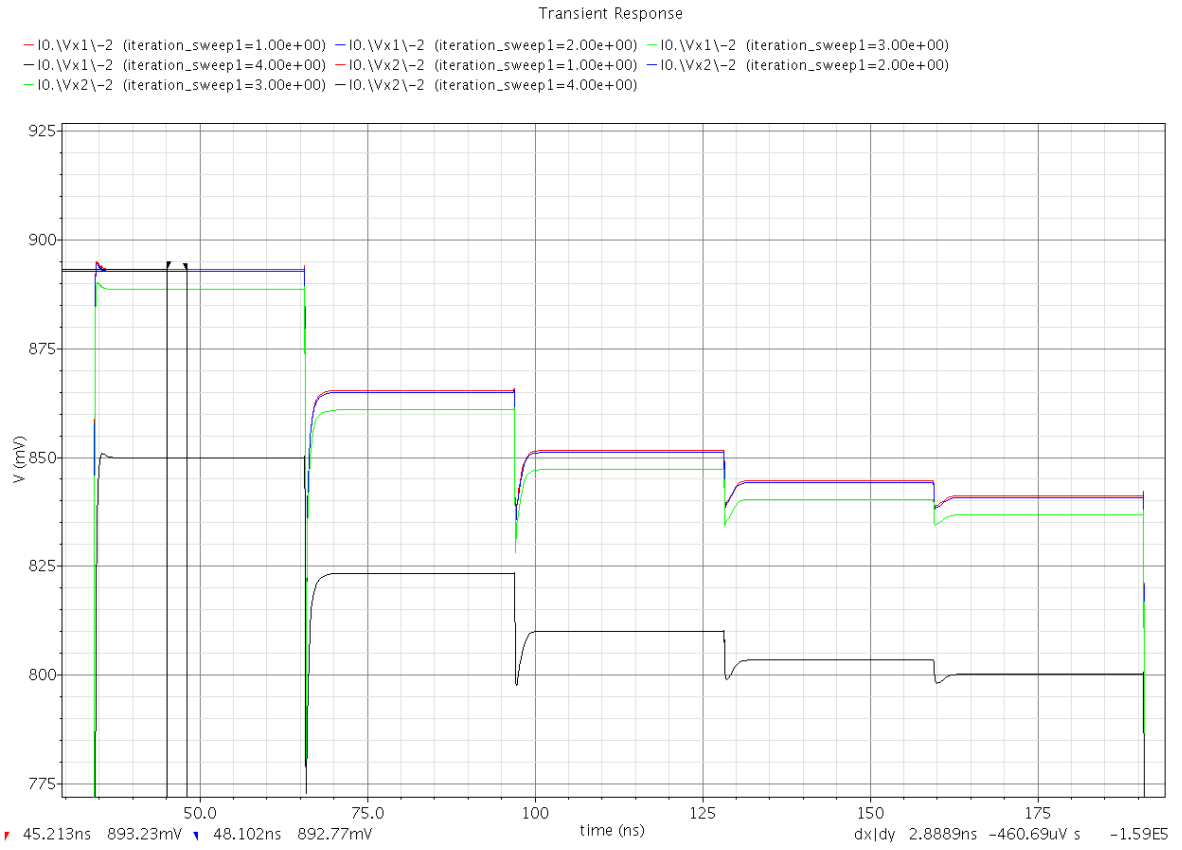


Figure 2-6 Detail of Figure 2-5 showing settling before MSB, b1 – b4 decisions.

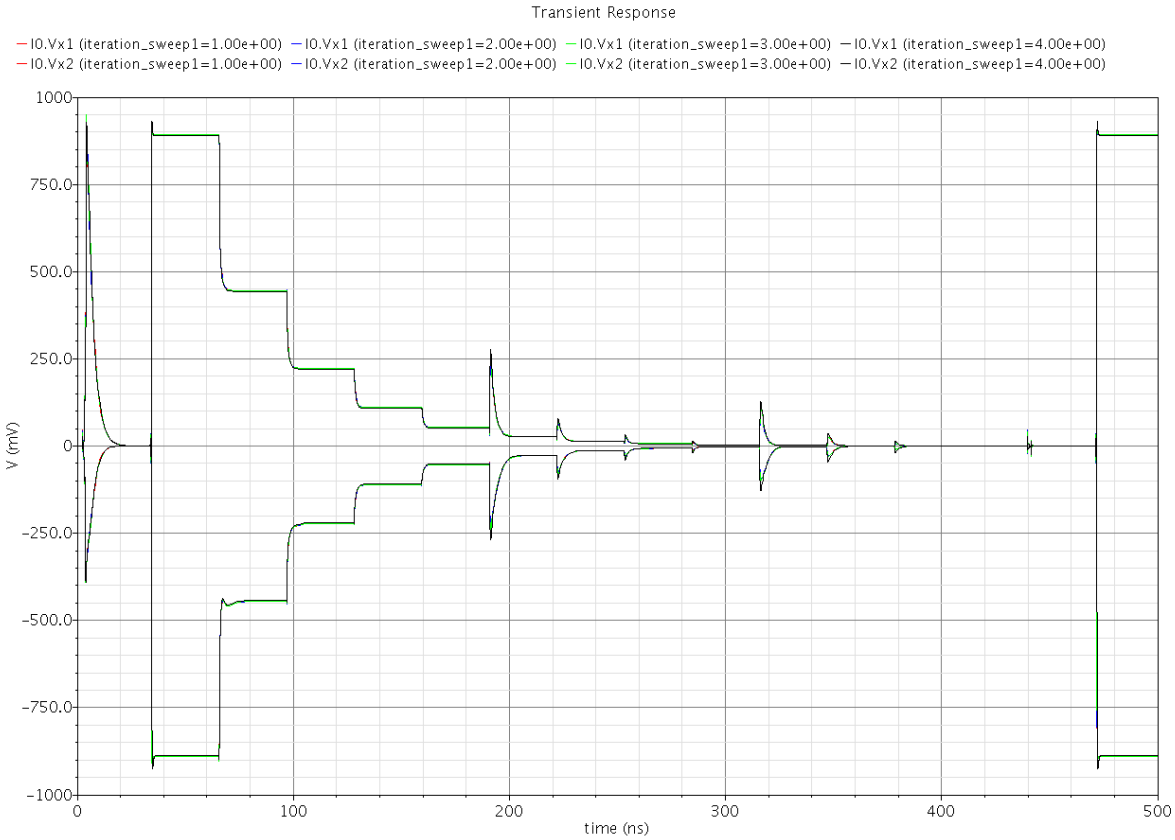


Figure 2-7 Waveforms at nodes Vx[1,2] for $\alpha = 0,1,10,100$.

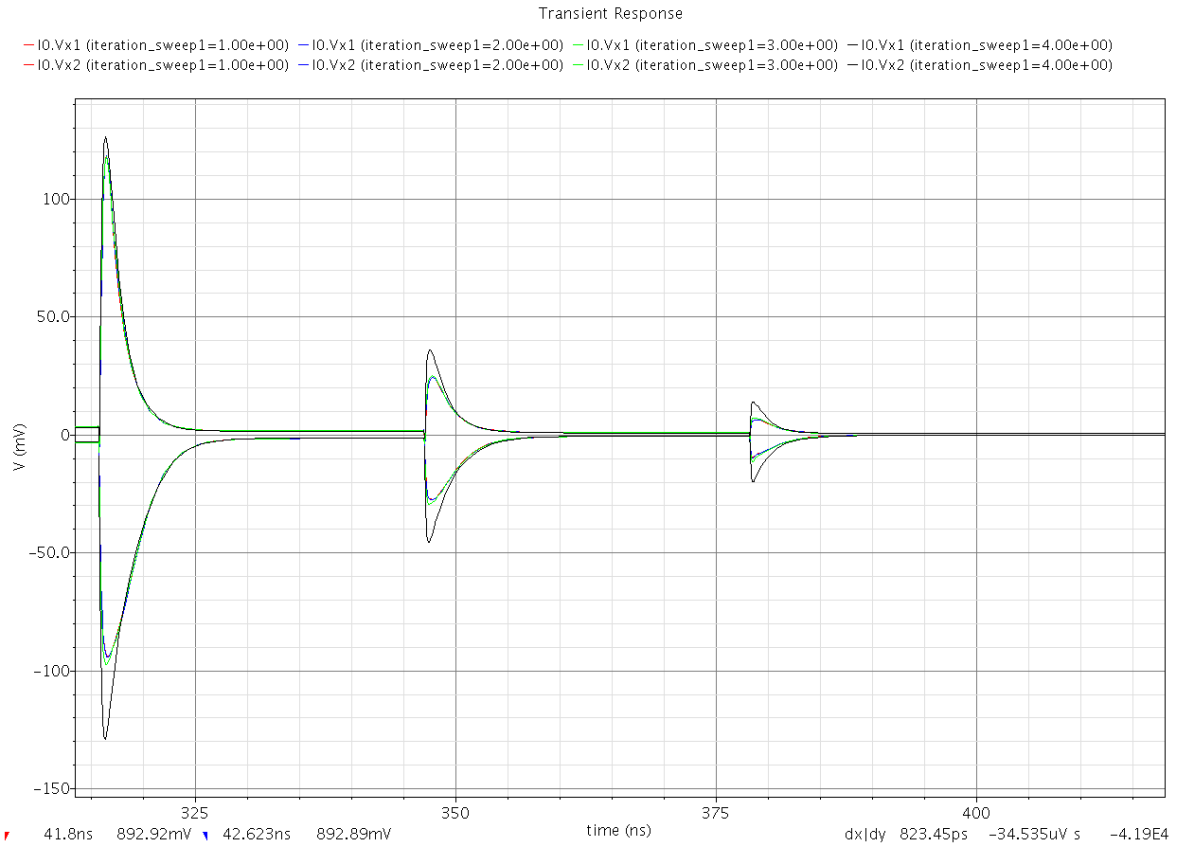


Figure 2-8 Detail of Figure 2-7 showing settling before b9 – b11 decisions.

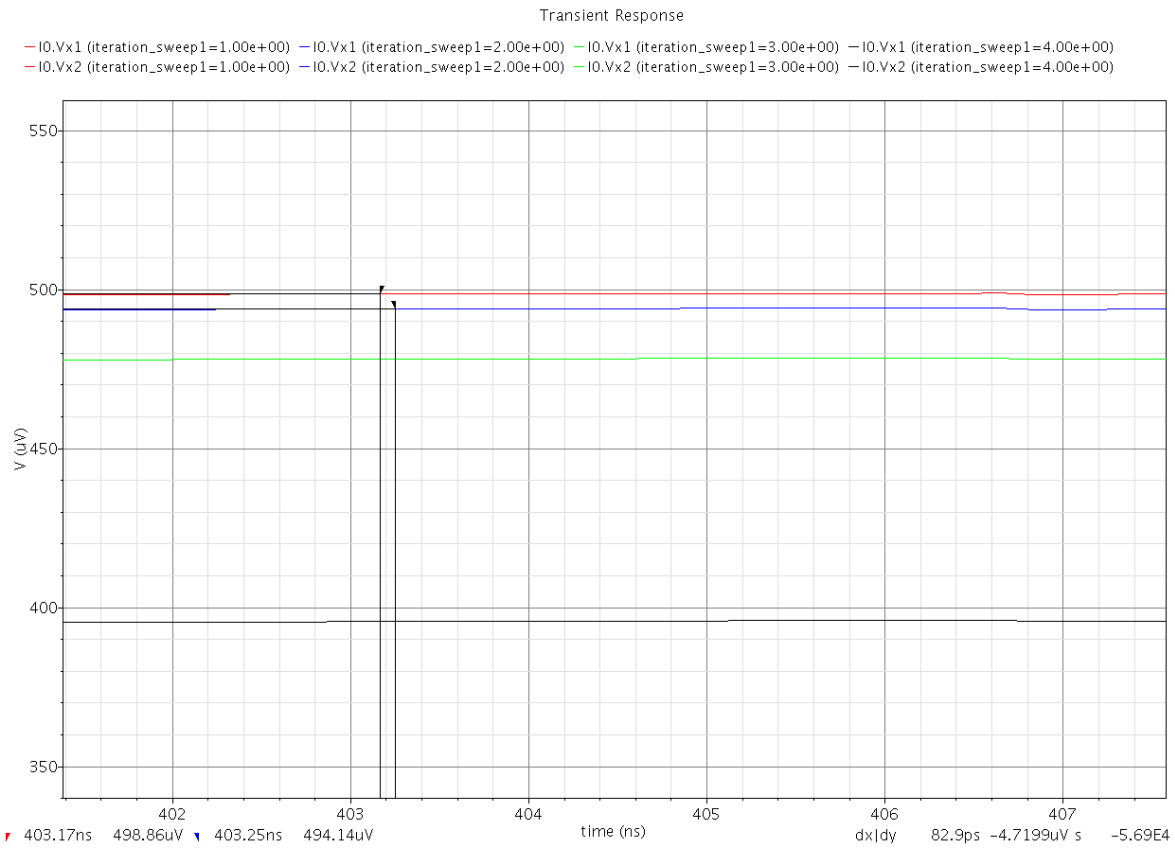


Figure 2-9 Zoom of Figure 2-8 showing settling before b11 decisions.

2.4. Discussion

From Figure 2-3 through Figure 2-9, we can draw the following conclusions:

- The bigger is the bottom-plate parasitic capacitance, the smaller is the signal level (or the higher is the reduction of the signal level with respect to the ideal case). The reduction of the signal level is due to charge sharing between the capacitor array [LSB capacitor array, Middle capacitor array] and corresponding parasitic capacitor [$C_{s2,p}$, $C_{s1,p}$].

- Differences in signal level between the ideal and real case are attenuated by the series capacitors, i.e. from node Vx[1,2]-3 to node Vx[1,2]-2, and again from node Vx[1,2]-2 to node Vx[1,2]. At node Vx[1,2], differences are as small as several μV .

- The red and blue waveforms, corresponding to ideal and real case, respectively, do almost always coincide. The maximum observed difference is $863\mu V$ at nodes Vx[1,2]-3.

Generally, a reduction in signal level is undesired, even though it is unproblematic here.

2.5. Charge sharing model

If the signal level would be reduced by the same factor at each node, the binary research algorithm would not be affected at all. Let us determine the reduction factor for each parallel capacitor array (LSB, Middle, MSB).

In general, if a capacitor C_a is charged to a voltage V_1, it accumulates a charge $Q = C_a \cdot V_1$. If C_a is then connected to C_p, the former capacitor will share some of its charge with the latter capacitor.

Assuming conservation of charge and that the two capacitors are in parallel, a reduced voltage V_2 defined by Eq. (2-1) appears – after charge sharing – across both capacitors.

$$Q = C_a \cdot V_1 = (C_a + C_p) \cdot V_2 \tag{2-1}$$

From Eq. (2-1), we get

$$V_2 = \frac{C_a}{C_a + C_p} \cdot V_1 \tag{2-2}$$

The *signal level reduction factor due to charge sharing* is defined by:

$$\eta = \frac{V_2}{V_1} = \frac{C_a}{C_a + C_p} \tag{2-3}$$

If C_a is the equivalent capacitance of a parallel capacitor array and C_p the corresponding parasitic capacitance, the signal level reduction factors of the LSB and Middle capacitor arrays are given by Eq. (2-4) and Eq. (2-5), respectively.

$$\eta_{LSB} = \frac{8C_u}{8C_u + \frac{8}{7}C_u \cdot \gamma} = 0.998969 \tag{2-4}$$

$$\eta_{Middle} = \frac{15C_u}{15C_u + \frac{16}{15}C_u \cdot \gamma} = 0.999487 \tag{2-5}$$

$\gamma = 7.224 \cdot 10^{-3}$ is the ratio of the bottom-plate parasitic capacitance to the nominal capacitance of a MIM capacitor manufactured in UMC $0.18\mu m$ CMOS technology [Meinerzhagen2008].

As for the MSB capacitor array, there is no bottom-plate parasitic capacitance; $C_{p,MSB}$ is the sum of the parasitic gate capacitance of the input transistor of the comparator and parasitic capacitances of the switches connected to Vx[1,2]. η_{MSB} is evaluated numerically in *Chapter 3*.

As for the LSB capacitor array, we obtain from Figure 2-4:

$$\eta_{LSB}^{sim} = \frac{892.73}{893.6} = 0.999026 \tag{2-6}$$

As for the Middle capacitor array, we obtain from Figure 2-6:

$$\eta_{Middle}^{sim} = \frac{892.77}{893.23} = 0.999485 \tag{2-7}$$

Notice that on Figure 2-4 and Figure 2-6, the signal level is already diminished due to charge sharing with parasitic capacitances from the switches. Were there no parasitic capacitances at all, the signal level would $900mV$.

Eq. (2-8) and Eq. (2-9) show the excellent agreement of simulation data with the developed charge sharing model.

$$\frac{\left|\eta_{LSB}^{sim} - \eta_{LSB}\right|}{\eta_{LSB}} \cdot 100\% = 0.0057\% \tag{2-8}$$

$$\frac{\left|\eta_{Middle}^{sim} - \eta_{Middle}\right|}{\eta_{Middle}} \cdot 100\% = 2 \cdot 10^{-4}\% \tag{2-9}$$

We have seen that $\eta_{LSB} \cong \eta_{Middle}$. Furthermore, η_{MSB} has approximately the same numerical value too, as apparently, the binary research algorithm still works, even though there is charge sharing.

2.6. Conclusion

Referring back to Figure 2-2, parasitic bottom-plate capacitances do not affect the A/D conversion of a positive full-range sample, even if they are multiplied by a factor of 100. To rigorously study the effect of bottom-plate parasitic capacitances, other samples must be considered.

The signal level reduction factor due to charge sharing has been defined and has been numerically evaluated for the LSB and Middle capacitor arrays, taking into account only bottom-plate parasitic capacitances. The signal level reduction factor for all LSB, Middle and MSB capacitor arrays is approximately the same.

3. Effect of parasitic capacitances of switches and comparator's input transistors

3.1. Numerical values of parasitic capacitances and signal level reduction factors

There are more parasitic capacitances at nodes Vx[1,2]-3, Vx[1,2]-2 and Vx[1,2]. Switches are connected to each node in order to reset it to ground at the beginning of an A/D conversion. In general, MOS transistors have different source/drain parasitic capacitances $C_{p,on}$ and $C_{p,off}$ in their on and off states, respectively. Here, charge sharing will occur after the switches have been turned off.

In order to minimize *charge injection* onto the parallel capacitor arrays, switches use a shorted dummy transistor controlled by the complementary clock signal S*, as shown in Figure 3-1. The *switch transistor*, controlled by the clock signal S, is two times wider than the *dummy transistor*. Each time the switch transistor is turned off, approximately half[1] of its channel charge is injected onto node Vgnd, where it is absorbed by the dummy transistor, which at this time is turned on. Whenever the switch is off, the switch transistor is off, while the dummy transistor is on. The following parasitic capacitances contribute to the total parasitic capacitance at node Vgnd:

- Switch transistor, off, drain (Read: *Drain* capacitance of the *switch transistor* in its *off* state)
- Dummy transistor, on, drain
- Dummy transistor, on, source

The corresponding numerical values – highlighted on Figure 3-1 – are extracted from DC simulation. The *total contribution of one switch* to the total parasitic capacitance at node Vxi-j is:

$$C_{switch,p} = (186.4 + 344.3 + 333)aF = 863.7aF \tag{3-1}$$

In order to have the same RC constant and equal signal level reduction factors η in each parallel capacitor array, the LSB capacitor array has 8 switches as the one shown in Figure 3-1 in parallel, while both Middle and MSB capacitor arrays have 15 switches in parallel.

As for nodes Vx[1,2], there is also the parasitic gate capacitance $C_{comp,p}$ of the comparator's input transistors. However, the design of the comparator minimizes these parasitic gate capacitances. From DC simulation, $C_{comp,p} = 840.2aF$.

Taking into account parasitic capacitances of switches and the comparator, but not considering bottom-plate parasitic capacitances of series capacitors, the signal level reduction factors of the LSB, Middle, and MSB capacitor arrays become:

[1] The driver seen on Figure 3-1 is responsible for fast transitions of the switch transistor's gate voltage. Fast transitions in the clock signal result in a well controlled distribution of the channel charge onto nodes attached to drain and source.

$$\eta_{LSB} = \frac{8C_u}{8C_u + 8C_{switch,p}} = 0.996556 \tag{3-2}$$

$$\eta_{Middle} = \frac{15C_u}{15C_u + 15C_{switch,p}} = 0.996556 \tag{3-3}$$

$$\eta_{MSB} = \frac{15C_u}{15C_u + 15C_{switch,p} + C_{comp,p}} = 0.996334 \tag{3-4}$$

By design, $\eta_{LSB} = \eta_{Middle}$. Due to the parasitic capacitance of the comparator's input transistors, η_{MSB} is slightly smaller $\eta_{LSB} = \eta_{Middle}$.

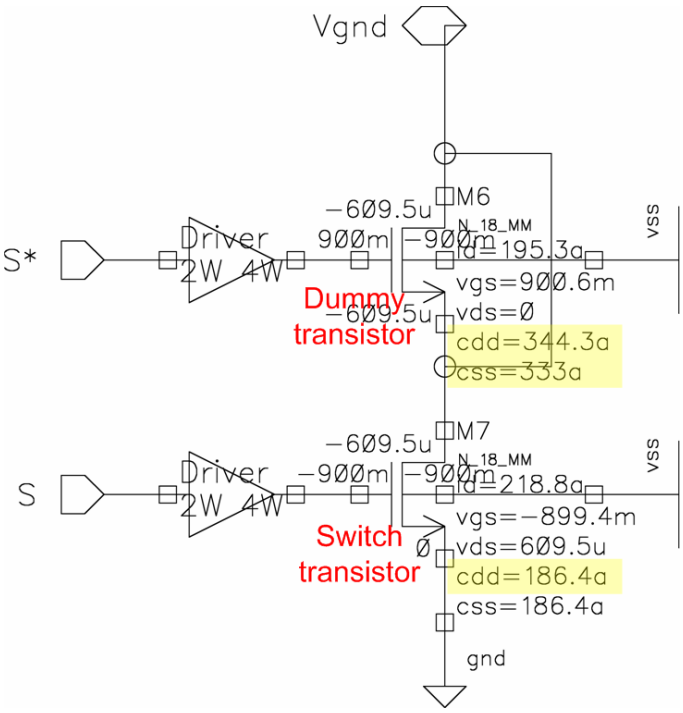


Figure 3-1 Switch with charge injection minimization. The source/drain parasitic capacitances contributing to the total parasitic capacitance at node Vgnd are highlighted. Of course, Vgnd is Vx[1,2]-3, Vx[1,2]-2 or Vx[1,2].

3.2. Set-up of experiment

To see the effect of parasitic capacitances from switches and the comparator, the conversion of a full-range sample is simulated with the following set-ups:

- ADC core built from ideal switches and ideal comparator
- Real ADC core

The transient simulation results are compared. In addition, reduction factors extracted from simulation are compared with their theoretical values given by Eq. (3-2) through Eq. (3-4).

3.3. Results

Of course, in all cases, the digital output code is correct.

Figure 3-2 through Figure 3-8 show the voltage waveforms at nodes Vx[1,2]-3, Vx[1,2]-2 and Vx[1,2]. Ideal waveforms are shown in red, while real waveforms are shown in blue.

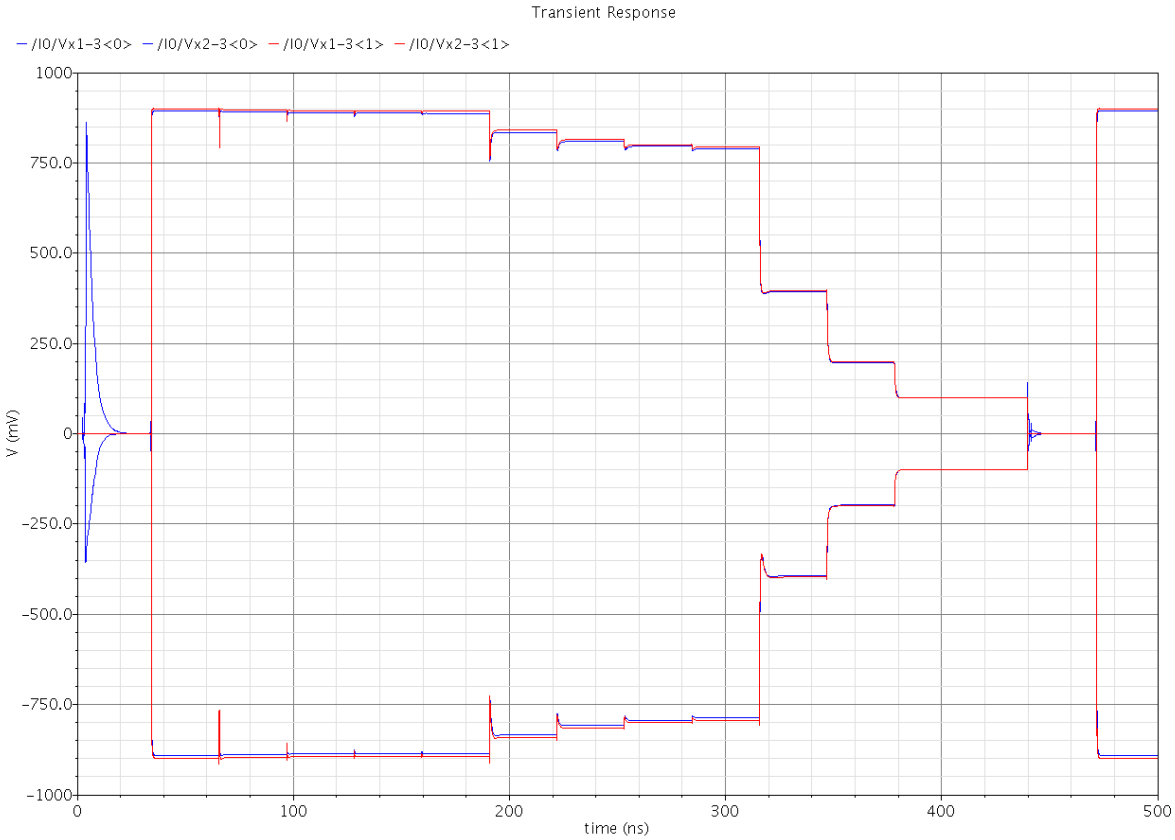


Figure 3-2 Waveforms at nodes Vx[1,2]-3 in the ideal (red) and real (blue) case.

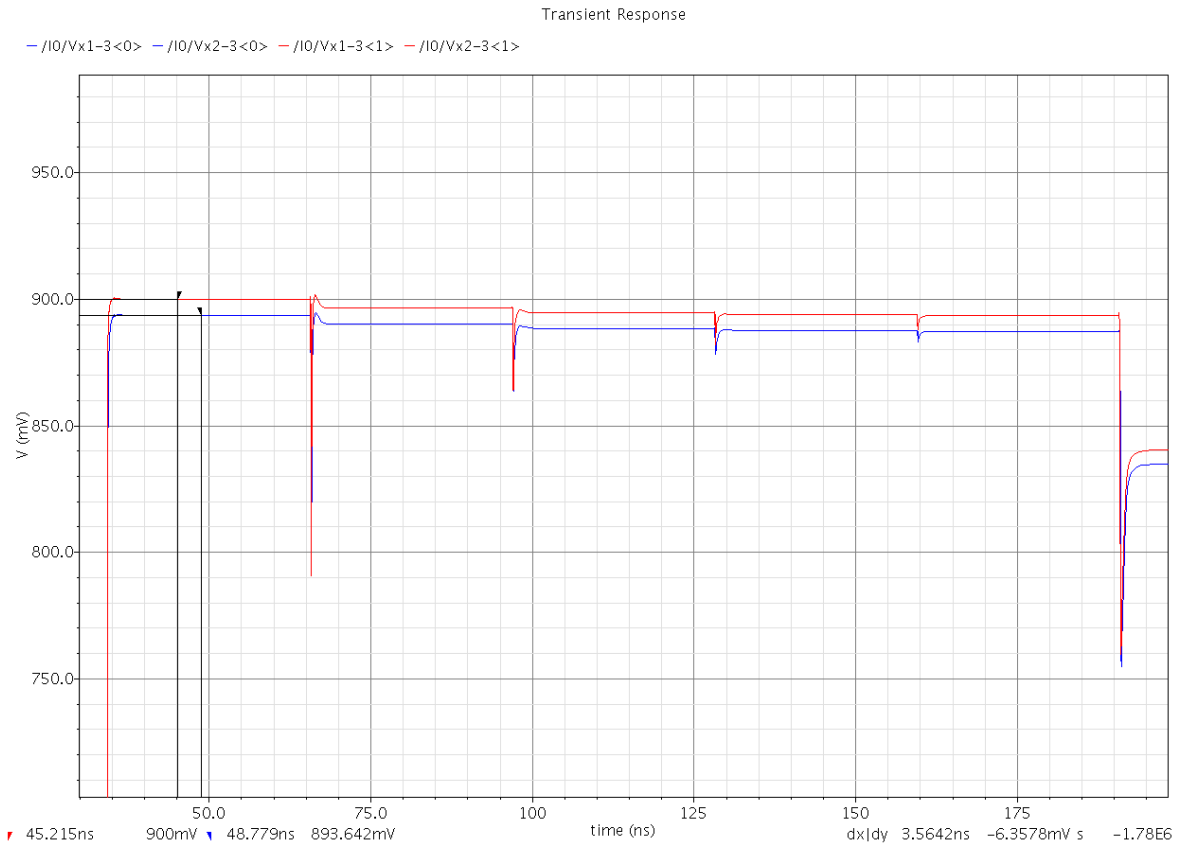


Figure 3-3 Detail of Figure 3-2.

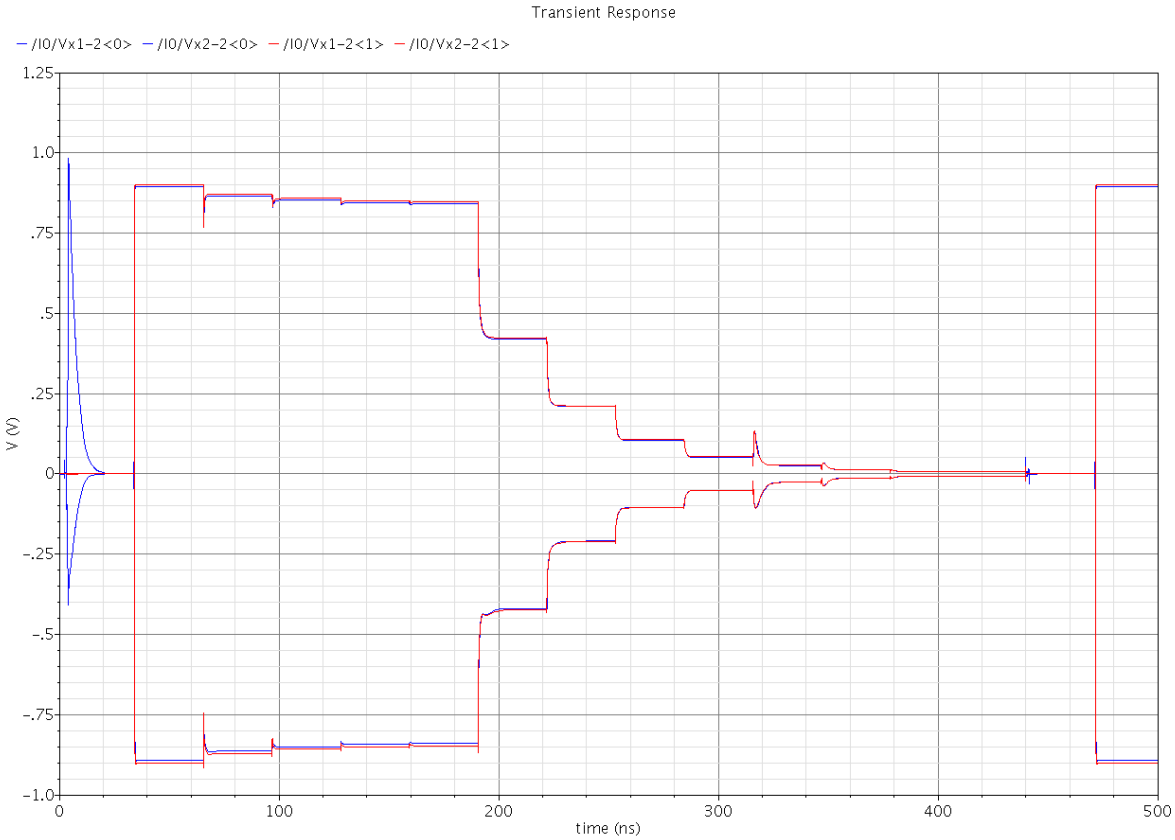


Figure 3-4 Waveforms at nodes Vx[1,2]-2 in the ideal (red) and real (blue) case.

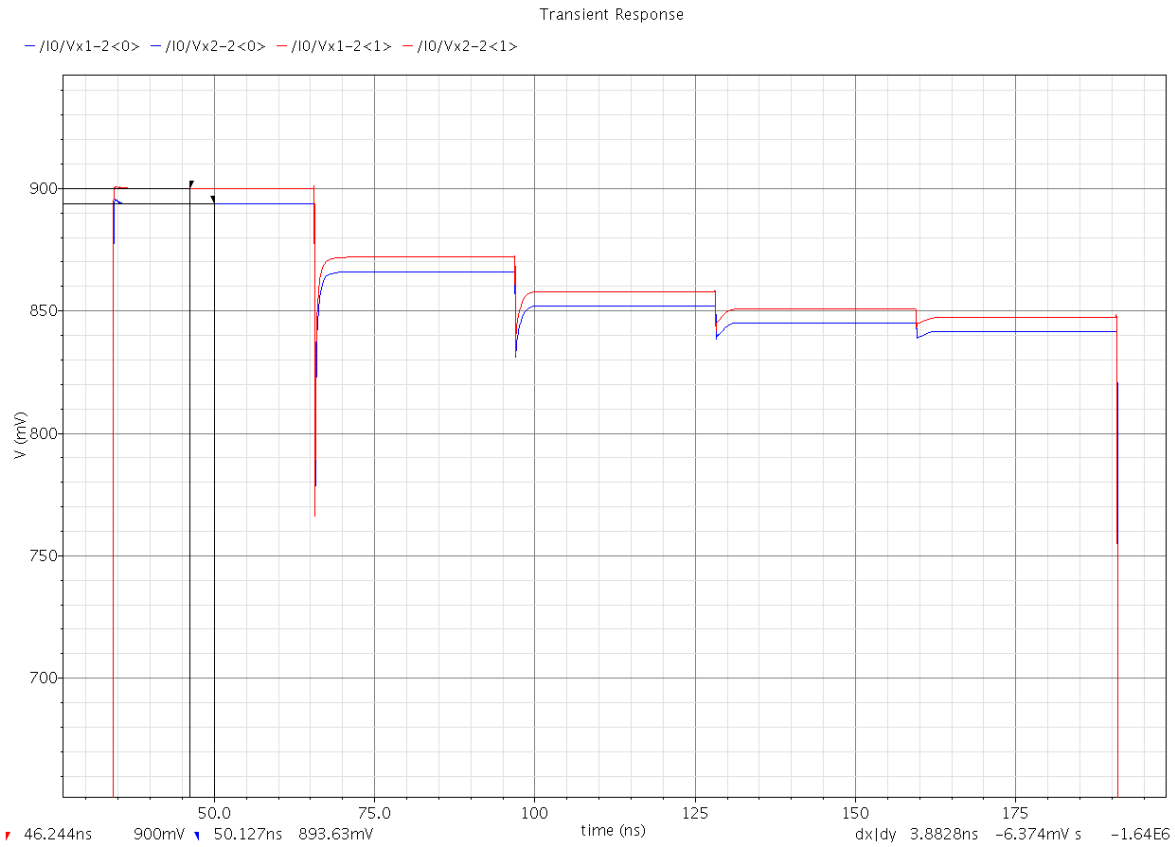


Figure 3-5 Detail of Figure 3-4.

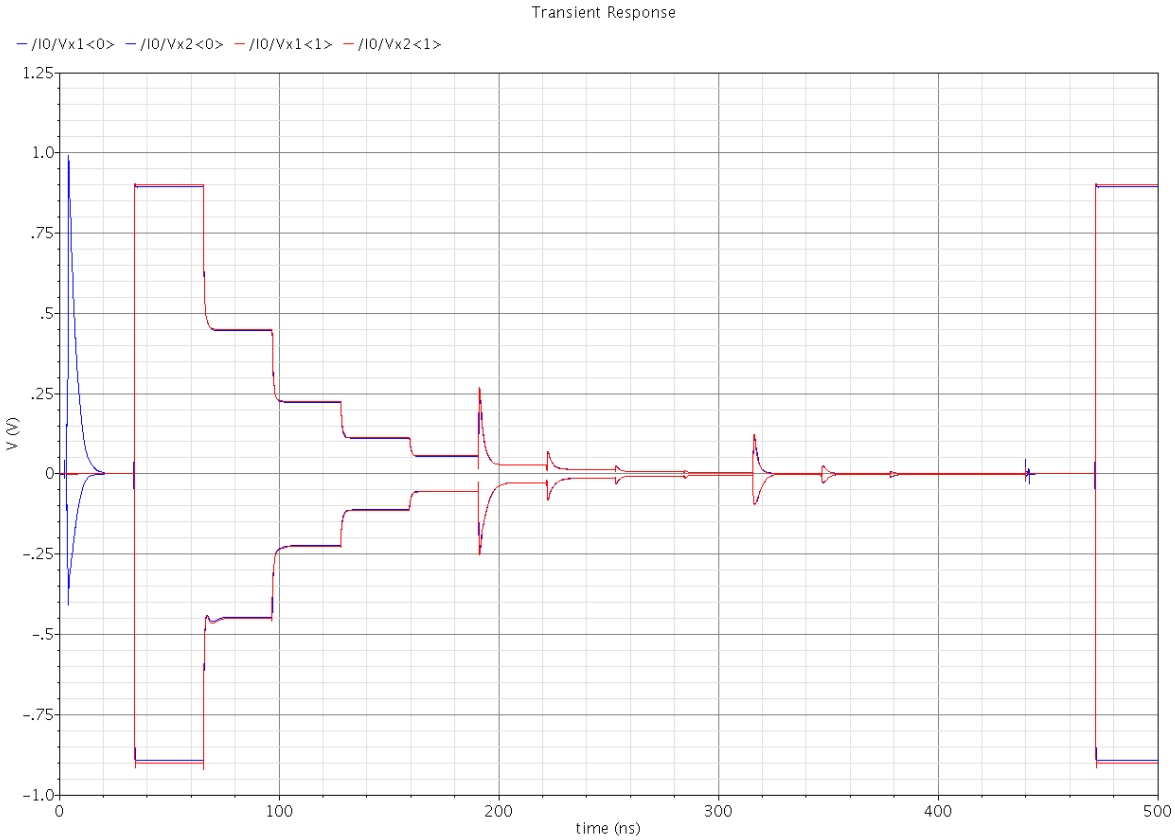


Figure 3-6 Waveforms at nodes Vx[1,2] in the ideal (red) and real (blue) case.

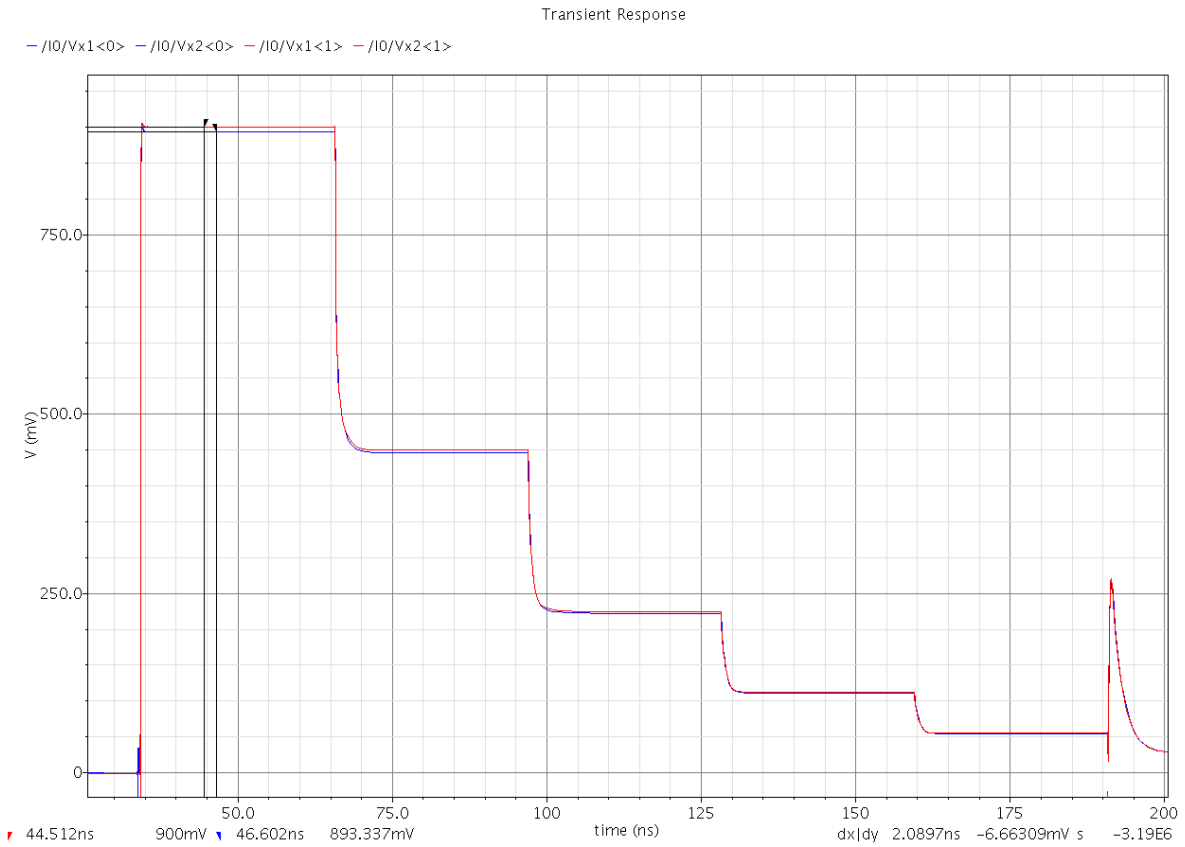


Figure 3-7 Detail of Figure 3-6 (a).

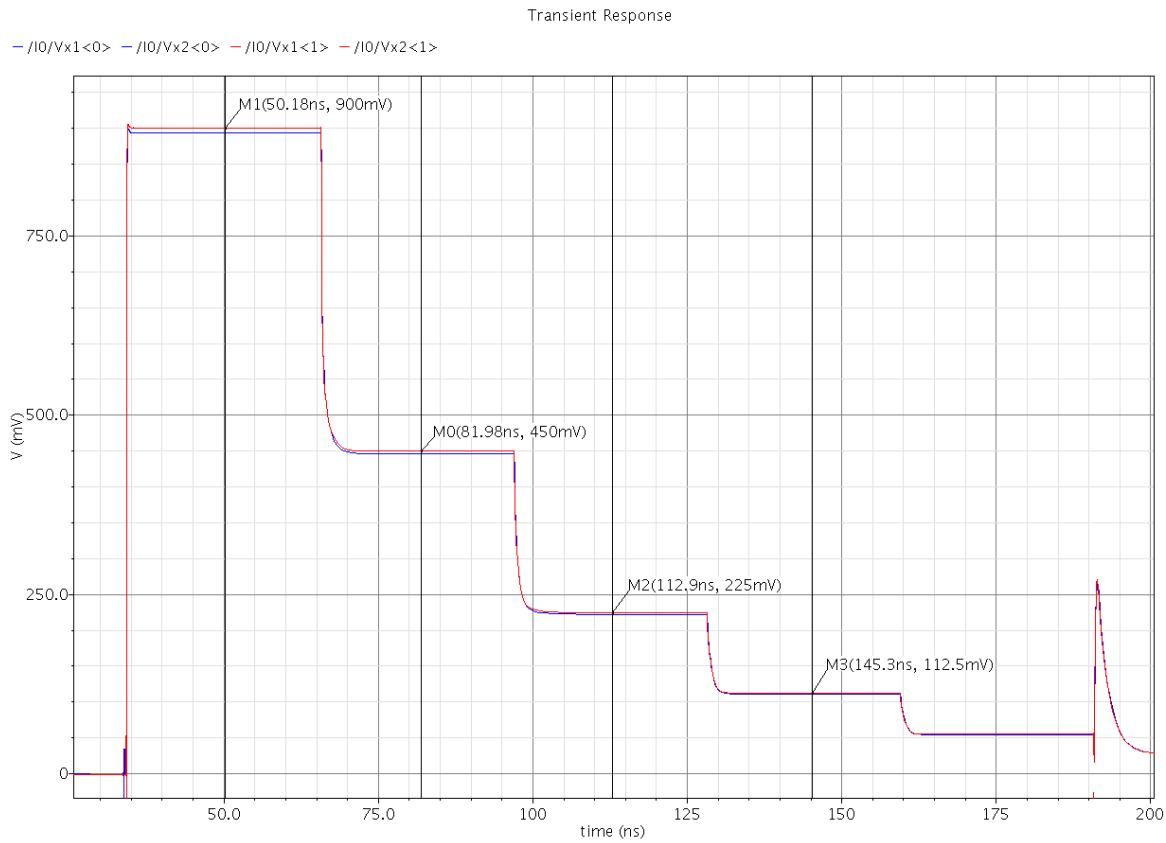


Figure 3-8 Detail of Figure 3-6 (b).

3.4. Discussion

On Figure 3-2 through Figure 3-8, we clearly see that the absolute value of all ideal waveforms is always higher than the absolute value of corresponding real waveforms.

On Figure 3-3, Figure 3-5 and Figure 3-7, the ideal value of nodes Vx2-3, Vx2-2, and Vx2 during the hold state – which is $900mV$ when converting a positive full-range sample – can clearly be seen. Nodes Vx1-3, Vx1-2, and Vx1 are ideally at $-900mV$ during the hold state.

From Figure 3-3, Figure 3-5 and Figure 3-7, the *signal level reduction factors due to charge sharing* of the LSB, Middle and MSB capacitor arrays are found to be:

$$\eta_{LSB}^{sim} = \frac{893.642}{900} = 0.992936 \tag{3-5}$$

$$\eta_{Middle}^{sim} = \frac{893.63}{900} = 0.992922 \tag{3-6}$$

$$\eta_{MSB}^{sim} = \frac{893.337}{900} = 0.992597 \tag{3-7}$$

These values correspond well to the values given by Eq. (3-2) through Eq. (3-4). In particular, η_{MSB}^{sim} is smaller than η_{LSB}^{sim} and η_{Middle}^{sim}.

On Figure 3-8, notice the ideal values that arise at node Vx2 during the conversion of a positive full-range sample, which are $900mV$ in the hold state, $450mV$ before the b1 bit decision, $225mV$ before the b2 bit decision, etc.

3.5. Conclusion

In conclusion, if the number of parallel switches to reset each parallel capacitor array to ground is proportional to the total capacitance of the capacitor array, the parasitic capacitances of the switches do not affect the binary research algorithm, but do merely slightly lower the signal level. Due to the parasitic capacitance of the comparator's input transistor, η_{MSB} is slightly lower than $\eta_{LSB} = \eta_{Middle}$, which still does not make the A/D conversion of a positive full-range sample fail.

4. Combination of all parasitic capacitances

4.1. Numerical values of signal level reduction factors

Considering all parasitic capacitances together, the *signal level reduction factors due to charge sharing* of the LSB, Middle, and MSB capacitor arrays are:

$$\eta_{LSB} = \frac{8C_u}{8C_u + \frac{8}{7}C_u \cdot \gamma + 8C_{switch,p}} = 0.995532 \tag{4-1}$$

$$\eta_{Middle} = \frac{15C_u}{15C_u + \frac{16}{15}C_u \cdot \gamma + 15C_{switch,p}} = 0.996046 \tag{4-2}$$

$$\eta_{MSB} = \frac{15C_u}{15C_u + 15C_{switch,p} + C_{comp,p}} = 0.996334 \tag{4-3}$$

4.2. Additional capacitors equalizing signal level reduction factors

As the bottom-plate parasitic capacitances of the LSB and Middle capacitor array are not the same fraction ξ of the equivalent capacitance of the associated capacitor array, $\eta_{LSB} \neq \eta_{Middle}$. If we could write $C_{s2,p} = \xi \cdot 8C_u$ and $C_{s1,p} = \xi \cdot 15C_u$, then $\eta_{LSB} = \frac{C_u}{C_u + \xi C_u + C_{switch,p}} = \eta_{Middle}$. Unfortunately, $\xi_{LSB} = \frac{\gamma}{7}$ and $\xi_{Middle} = \frac{16\gamma}{15^2}$. Inserting an additional capacitor C_{add}^{Middle} at nodes Vx[1,2]-2 yields $\eta_{LSB} = \eta_{Middle}$. C_{add}^{Middle} is defined by:

$$\xi_{LSB} \cdot 15C_u = C_{s1,p} + C_{add}^{Middle} = \frac{16}{15}C_u \cdot \gamma + C_{add}^{Middle} \tag{4-4}$$

From Eq. (4-4), substituting $\xi_{LSB} = \frac{\gamma}{7}$,

$$C_{add}^{Middle} = \left(\frac{15}{7} - \frac{16}{15}\right) \cdot C_u \cdot \gamma = 1.9431 fF \tag{4-5}$$

It is easily verified that after insertion of C_{add}^{Middle},

$$\eta_{Middle} = \frac{15C_u}{15C_u + \frac{16}{15}C_u \cdot \gamma + C_{add}^{Middle} + 15C_{switch,p}} = \frac{C_u}{C_u + \frac{\gamma}{7} \cdot C_u + C_{switch,p}} = \eta_{LSB} \tag{4-6}$$

As for the MSB capacitor array, the lack of bottom-plate parasitic capacitance is partially made good for by the parasitic capacitance of the comparator's input transistor $C_{comp,p}$.

Also at nodes Vx[1,2] we can insert an additional capacitor C_{add}^{MSB} in order to bring η_{MSB} down to $\eta_{LSB} = \eta_{Middle} = 0.995532$. C_{add}^{MSB} is defined by:

$$\eta_{MSB} = \eta_{LSB} \tag{4-7}$$

or more conveniently,

$$\frac{16}{15} \cdot C_u \cdot \gamma + C_{add}^{Middle} = C_{comp,p} + C_{add}^{MSB} \tag{4-8}$$

From Eq. (4-8), substituting $C_{add}^{Middle} = \left(\frac{15}{7} - \frac{16}{15} \right) \cdot C_u \cdot \gamma$,

$$\frac{15}{7} \cdot C_u \cdot \gamma = C_{comp,p} + C_{add}^{MSB} \tag{4-9}$$

Finally, from Eq. (4-9),

$$C_{add}^{MSB} = \frac{15}{7} \cdot C_u \cdot \gamma - C_{comp,p} = 3.0288\,fF \tag{4-10}$$

It is easily verified that after insertion of C_{add}^{MSB},

$$\eta_{MSB} = \frac{15C_u}{15C_u + 15C_{switch,p} + C_{comp,p} + C_{add}^{MSB}} = \frac{C_u}{C_u + \frac{\gamma}{7} \cdot C_u + C_{switch,p}} = \eta_{LSB} = \eta_{Middle} \tag{4-11}$$

4.3. Conclusion

In conclusion, inserting $C_{add}^{Middle} = 1.9431\,fF$ at nodes Vx1-2 and Vx2-2, and inserting $C_{add}^{MSB} = 3.0288\,fF$ at nodes Vx1 and Vx2, the signal level reduction factors of all capacitor arrays are equalized: $\eta_{LSB} = \eta_{Middle} = \eta_{MSB} = \eta$. As a consequence, the real ADC behaves like an ideal ADC, expect for signal levels reduced by $\eta = 0.995532$, and apart from non-idealities other than parasitic capacitances. By insertion of C_{add}^{Middle} and C_{add}^{MSB}, DNL, INL, SFDR, SINAD, and ENOB are expected to improve.

To keep the advantages brought by C_{add}^{Middle} and C_{add}^{MSB}, the capacitor arrays and connection lines to switches and comparator must be laid out very carefully, so that the sum of interconnect capacitances seen from each parallel capacitor array is proportional to the equivalent capacitance of the parallel capacitor array. In a different design approach, C_{add}^{Middle} and C_{add}^{MSB} are incorporated as interconnect capacitances, and the remaining part of interconnect capacitances is proportional to the equivalent capacitance of parallel capacitor arrays.

5. Drivers

5.1. Definitions

The ***standard load (capacitance)*** C_{std} is defined as the gate capacitance of a ***standard or minimum size transistor***, i.e. a transistor with $W_{std} = 240nm$ and $L_{std} = 180nm$.

Standard nMOS transistors (std nMOS tx) used in the SAR control block are minimum size transistors ($240nm/180nm$) and have a gate capacitance of C_{std}, while ***standard pMOS transistors (std pMOS tx)*** are three times wider ($720nm/180nm$) and have a gate capacitance of $3C_{std}$.

Driving a ***standard inverter***, built from a standard nMOS transistor and a standard pMOS transistor, corresponds to driving $4C_{std}$.

In a ***n-chain***, each inverter has transistors n times wider than the previous inverter, with $n \in [2,3]$. All transistors in the chain have $L = L_{std}$. To ease layout, only $n = 2$ and $n = 3$ are considered, so that the number of fingers is multiplied by n from stage to stage. Of course, to obtain a non-inverting n-chain, the number of stages must be even.

5.2. 2- and 3-chains and their driving capabilities

Table 5-1 shows the driving capabilities which can be achieved with a n-chain, $n = 2,3$ and the corresponding driver names. As for the driving capability, it is assumed that an inverter with given transistor sizes can drive 2 to 3 times its own input capacitance. Driving capabilities are expressed in units of C_{std}. Drivers with equal n have equal delay times (see *Section 5.4*). d0 is a delay element.

	$n = 2$			$n = 3$		
Stage M	$\frac{W_{n,p}^{M}}{W_{n,p}^{std}}$	Driving capability of stage M [C_{std}]	Driver name	$\frac{W_{n,p}^{M}}{W_{n,p}^{std}}$	Driving capability of stage M [C_{std}]	Driver name
0	1	2 – 3	d0	1	2 – 3	d0
1	2	4 – 6	d2	3	6 – 9	d3
2	4	8 – 12	d4	9	18 – 27	d9
3	8	16 – 24	d8	27	54 – 81	d27
4	16	32 – 48	d16	81	162 – 243	d81
5	32	64 – 96	d32	243	486 – 729	d243
6	64	128 – 192	d64	729	1458 – 2187	d729
7	128	256 – 384	d128	2187	4374 – 6561	d2187

Table 5-1 Driving capabilities of n-chain, $n = 2,3$ with M stages.

5.3. Evaluation of total capacitive load for each control signal

The following signals are produced by the *SAR control logic* and drive a number of switches: *sel_in_ref*, *sel_Vx*, *sel_extra*, *sel_Vrefp*_b0*, *b1 – b11*, *eoc*. All signals except *eoc* are needed in complementary form.

The signal *Comp* and its complement *Comp** are produced by the *Comparator* and are fed back to the *SAR control logic*. Depending on the current state of the A/D conversion, the total capacitive load that *Comp* and *Comp** experience varies; drivers for *Comp* and *Comp** must be able to drive the maximum load seen during the conversion.

Also the distribution of the clock signals *clk0* and *clk0** requires drivers.

The following signals drive – in addition to switches – external loads C_{ext}, i.e. loads outside the ADC which are unknown at present: *b0 – b11*, *eoc*. To design drivers, all external loads are assumed to be $4C_{std}$. If necessary, driving capabilities can easily be augmented later.

Table 5-2 shows the total load capacitance C_{total} to be driven by each control signal. C_{total} is calculated as:

$$C_{total} = \left[(\#\, std\ nMOS\ tx) + 3 \cdot (\#\, std\ \ pMOS\ tx)\right] \cdot Multiplier + C_{ext} \quad [C_{std}] \qquad (5\text{-}1)$$

C_{ext} and C_{total} are expressed in units of C_{std}. The $Multiplier$ takes into account the repetition of the same switch and the ADC's fully differential topology.

Because we considered only gate parasitic capacitances for the computation of C_{total}, but did not take into account interconnect capacitances – which are difficult to estimate at present –, drivers listed in Table 5-2 are by trend over-dimensioned. In many cases, C_{total} coincides with the lower bound of the driving capability range. Furthermore, for signals *Comp* and *Comp**, we neglected drain/source parasitic capacitances from TG-based 2-to-1 multiplexers on the signal path, and choose stronger drivers than required by gate parasitic capacitances. Drivers listed in red are a 3-chain, while all other drivers are a 2-chain.

Signal	# std nMOS tx	# std pMOS tx	Multiplier	C_{ext} [C_{std}]	C_{total} [C_{std}]	Driver
sel_in_ref	38	8	2	0	124	d64
sel_in_ref*	8	38	2	0	244	d128
sel_Vx	2	2	76	0	608	d243
sel_Vx*	2	2	76	0	608	d243
sel_extra	1	0	2	0	2	d0
sel_extra*	1	1	2	0	8	d4
sel_Vrefp*_b0	8	8	1	4	36	d16
sel_Vrefp_b0*	8	8	1	0	32	d16
b1	1	0	16	4	20	d8
b1*	1	1	16	0	64	d32
b2	1	0	8	4	12	d8
b2*	1	1	8	0	32	d16
b3	1	0	4	4	8	d4
b3*	1	1	4	0	16	d8
b4	1	0	2	4	6	d4
b4*	1	1	2	0	8	d4
b5	1	0	16	4	20	d8
b5*	1	1	16	0	64	d32
b6	1	0	8	4	12	d8
b6*	1	1	8	0	32	d16
b7	1	0	4	4	8	d4
b7*	1	1	4	0	16	d8
b8	1	0	2	4	6	d4
b8*	1	1	2	0	8	d4
b9	1	0	8	4	12	d8
b9*	1	1	8	0	32	d16
b10	1	0	4	4	8	d4
b10*	1	1	4	0	16	d8
b11	1	0	2	4	6	d4
b11*	1	1	2	0	8	d4
eoc	0	0	0	4	4	d2
Comp	1	1	2	0	8	d9
Comp*	1	1	2	0	8	d9
clk0	13.556	13.556	1	0	54.224	d27
clk0*	15.556	15.556	1	0	62.224	d27

Table 5-2 Total capacitive load to be driven by each control signal and most appropriate driver.

5.4. Equalizing delay of drivers with different driving capabilities

In order to satisfy timing requirements, such as relative delays of control signals – which is essential for the SC DAC to operate correctly –, drivers are designed to have equal delays, while delay elements are responsible for relative delays. To obtain equal delays for drivers with different driving capabilities, drivers with lower driving capabilities contain dummy stages, so that all drivers have the same number of stages. All stages must have the same RC delay constant.

For all drivers, the first stage ($M = 0$) – which is not necessarily part of the n-chain itself, but typically part of a DFF – is a *standard inverter* with the following characteristics:

- $W_n^0 = W_{std}$
- $W_p^0 = 3 \cdot W_n^0$

- $C_{in}^{0} = 4 \cdot C_{std}$
- $R_{pull-down}^{0}$ (Resistance of the pull-down path)
- $R_{pull-up}^{0}$ (Resistance of the pull-up path)

$R_{pull-down}^{0} \neq R_{pull-up}^{0}$ for $W_p^0 = 3 \cdot W_n^0$. In UMC $0.18\mu m$ CMOS technology, the two paths would have the same resistance for $W_p^0 = 5.4 \cdot W_n^0$.

Stage $M+1$ has the following characteristics, expressed recursively in terms of stage M, where $M = 0,1,2...$:

- $W_n^{M+1} = n \cdot W_n^M$
- $W_p^{M+1} = n \cdot W_p^M$
- $C_{in}^{M+1} = n \cdot C_{in}^M$, because $W_n^{M+1} = n \cdot W_n^M$ and $W_p^{M+1} = n \cdot W_p^M$
- $R_{pull-down}^{M+1} = \frac{R_{pull-down}^{M}}{n}$, because $W_n^{M+1} = n \cdot W_n^M$
- $R_{pull-up}^{M+1} = \frac{R_{pull-up}^{M}}{n}$, because $W_p^{M+1} = n \cdot W_p^M$

As the ratios $R_{pull-down}^{M+1} / R_{pull-down}^{M}$ and $R_{pull-up}^{M+1} / R_{pull-up}^{M}$ are the same, they are collectively referred to as R^{M+1} / R^{M}. In the following, R refers to the resistance of either the pull-down or pull-up path. The RC constant of stage $M+1$ is given by:

$$(RC)_{M+1} = R^{M+1} \cdot C_{in}^{M+2} = \frac{R^M}{n} \cdot n \cdot C_{in}^{M+1} = R^M \cdot C_{in}^{M+1} = (RC)_M \tag{5-2}$$

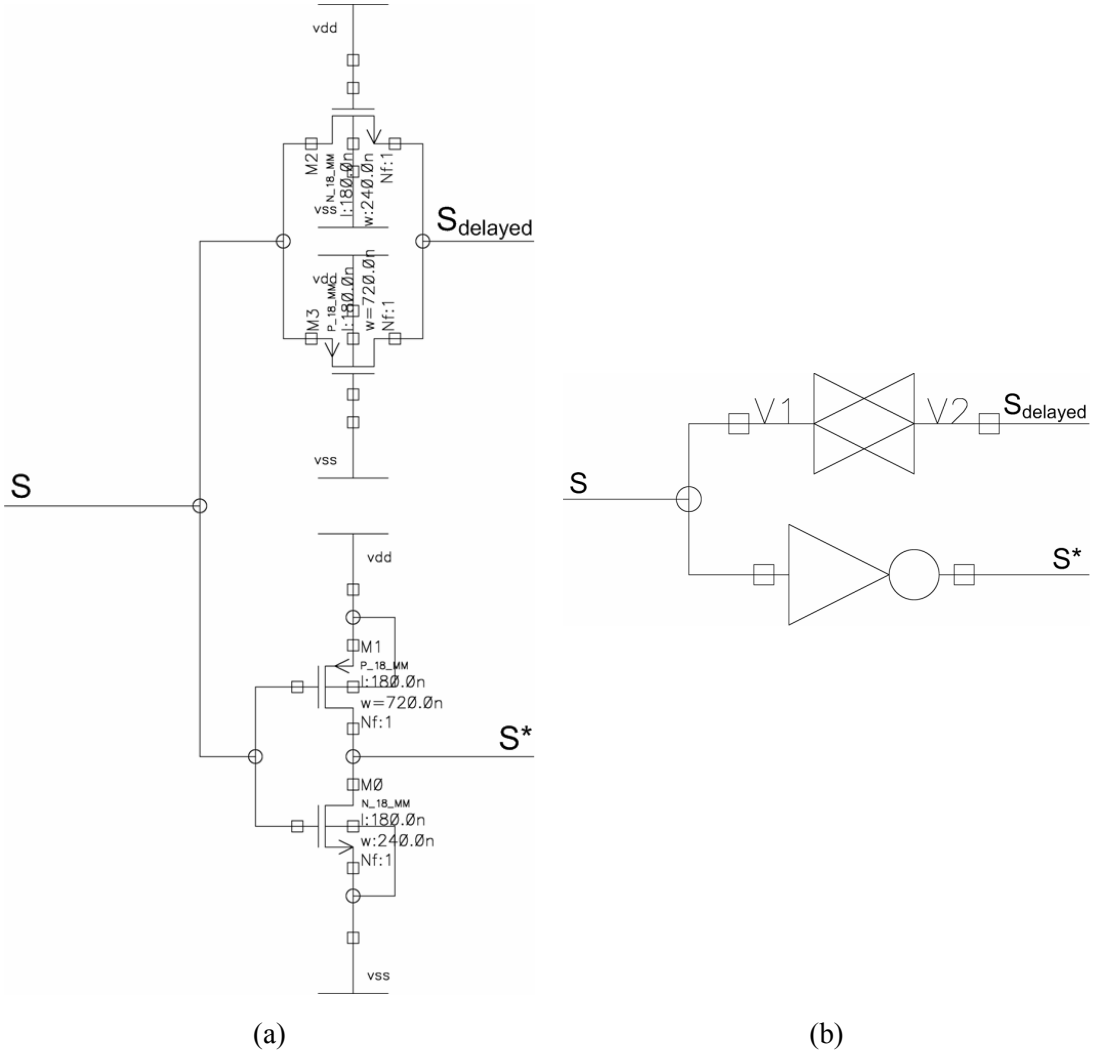
In a n-chain, stage $M+1$ has the same RC constant as stage M, where $M = 0,1,2....$ In conclusion, all stages of a n-chain have the same RC constant.

However, 2-chains and 3-chains have a different RC delay per stage. In fact, a 2-chain has a delay of $8R_{std}C_{std}$ per stage, whereas a 3-chain has a delay of $12R_{std}C_{std}$ per stage. Only *sel_Vx*, *sel_Vx**, *Comp, Comp**, *clk0* and *clk0** need a 3-chain, while all other signals need a 2-chain (see Table 5-2). As *sel_Vx* and *sel_Vx** must be advanced in time with respect to all other signals controlling a switch, delay elements are employed anyway. *Comp* and *Comp** are fed back to the *SAR control logic* and do not control switches. *clk0* and *clk0** are the reference clock signals. As a consequence, a difference in delay time per stage of the 2-chain and the 3-chain is not critical and does not need to be corrected for in the design of drivers.

For a given n-chain, a dummy stage must have the same RC constant as all other stages. Dummy stages are implemented as *standard inverters* added at the front-end of the n-chain, driving another dummy stage or the first stage in the chain ($M = 1$). In both cases, a capacitor $C_{dummy} = (n-1) \cdot 4C_{std}$ must be connected to the input of the dummy stage to obtain the required RC constant. C_{dummy} is conveniently incorporated by tying together the input of $n-1$ *standard inverters*.

5.5. Producing complementary signals

In order to produce the complementary signal *S** from a given signal *S*, a standard inverter is used. *S** is then delayed by one standard inverter delay with respect to *S*. To countervail this delay, a Transmission Gate (TG) – which is always on – is added on the signal path of *S*, as shown on Figure 5-1 (a). Figure 5-1 (b) shows the symbol used for the inverter/always-on-TG stage.

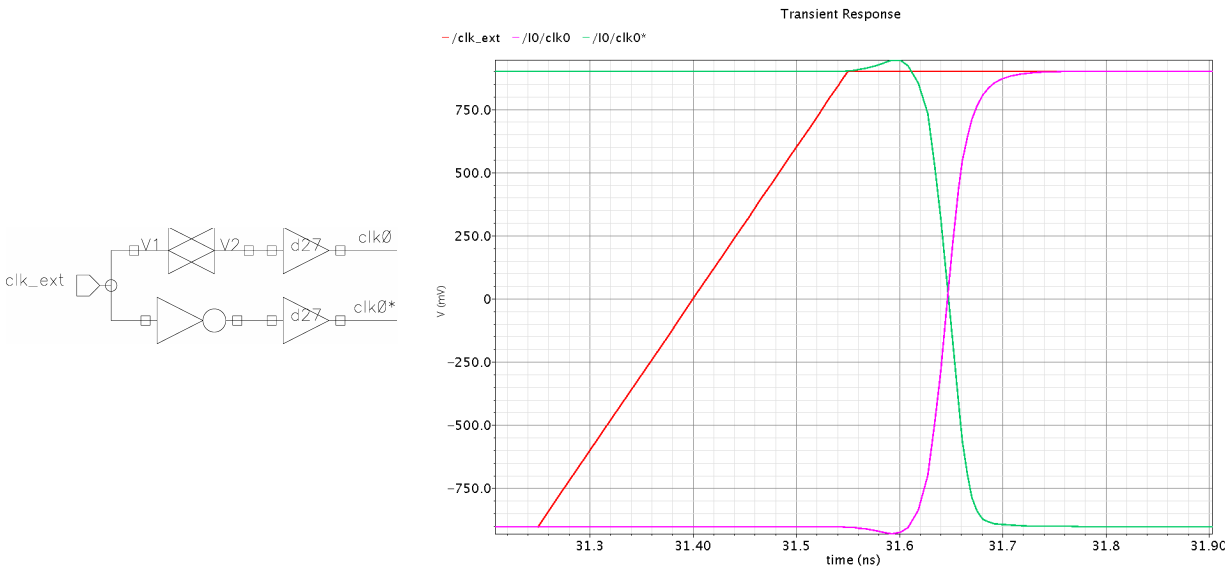


(a) (b)

Figure 5-1 Inverter/TG stage: (a) circuit diagram and (b) symbol.

Signals are fed to the drivers only after they have passed the inverter/always-on-TG stage, which may be incorporated in DFFs or used separately.

As an example, let us consider the generation of the complementary clock signals *clk0* and *clk0** from the external clock signal *clk_ext*. After propagating through the inverter/always-on-TG stage, the signals are fed to the driver d27, as shown on Figure 5-2 (a). Waveforms are shown on Figure 5-2 (b). Both *clk0* and *clk0** reach the 50% transition point (ground) at the same time. Furthermore, *clk0* and *clk0** transition in several tens of ps, thanks to the drivers, while *clk_ext* has a worst case rise/fall time of $300\,ps$.



(a) (b)

Figure 5-2 Generation and distribution of the complementary clock signals *clk0* and *clk0**: (a) circuit diagram and (b) simulation results.

5.6. Simulation results

Using the drivers listed in Table 5-2 gives rise to fast transitions with equal transition times in all control signals – even though loads do significantly differ –, and precisely controlled relative delays, as can be seen on Figure 5-3, which shows waveforms during the changeover from sampling to hold state. External loads are included in the simulation. Signals *b1 – b11* and *sel_extra* are safely delayed with respect to *sel_Vx*, by approximately $800\,ps$, and the signal *sel_in_ref* is safely delayed with respect to signals *b1 – b11* and *sel_extra* by about the same delay time. The same relative delays are obtained for the complementary signals, due to the employment of inverter/always-on-TG stages. Signals *b1 – b11* and *sel_extra* and their complements transition at almost the same time, which minimizes the glitch at nodes Vx[1,2]-3, Vx[1,2]-2 and Vx[1,2] occurring at the changeover from sampling to hold state. For all signals on Figure 5-3, transition times are as small as several tens of *ps*.

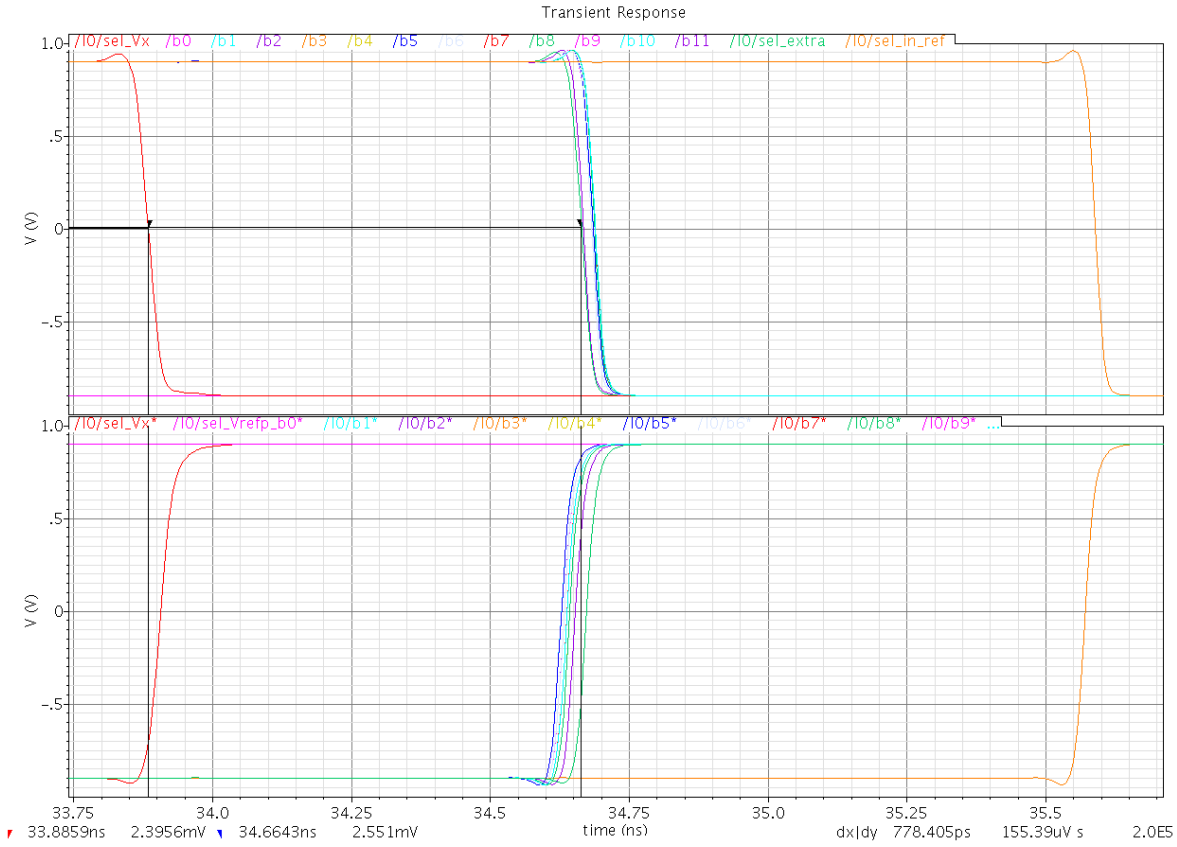


Figure 5-3 (Top trace) [Left-hand side] sel_Vx, [Middle] b0 – b11 and sel_extra, [Right-hand side] sel_in_ref. (Bottom trace) All complementary signals in the same sequence.

6. Considerations about layout

6.1. Floor planning

The split capacitor array consumes by far the biggest area, while the comparator, switch matrix, and SAR control logic including delay elements and drivers are relatively small.

The whole design must not be wider than $500\mu m$, but it can be longer than $500\mu m$.

6.2. Split capacitor array

Considering the *3bw2Cs* split capacitor array and a fully differential analog signal path, 80.419 unit capacitors need to be laid out. Each unit capacitor consumes an area of $15.66^2\ \mu m^2 = 245.2356\mu m^2$. If neither M5 enclosure of MIM, nor M5-to-M5 / MIM-to-MIM spacing is considered, the mere MIM capacitor area is $19721.60\mu m^2 = 140.43^2\ \mu m^2$. UMC $0.18\mu m$ CMOS technology has the following topological layout rules [UMCTLR2007]:

R1.	Minimum M5 to M5 spacing	
	a. M5 width < 10um	0.28um
	b. M5 width ≥ 10um	0.32um
R2.	Minimum MIM to MIM spacing	0.55um
R3.	Minimum M5 enclosure of MIM	0.5um

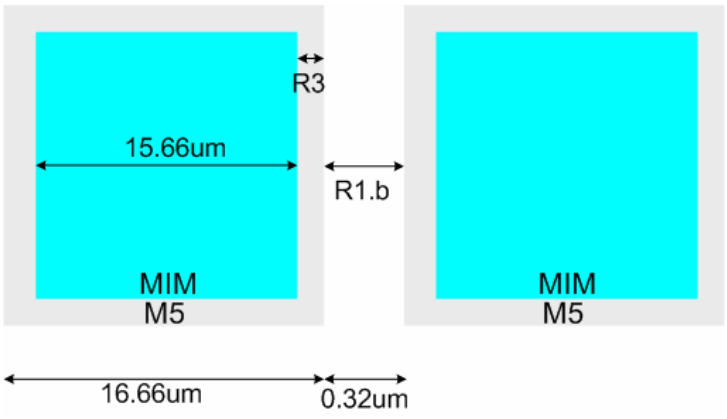


Figure 6-1 UMC's Topological Layout Rules (TLRs.)

From Figure 1-7, R2 is automatically satisfied if R3 and R1.b are satisfied. Even though series capacitors need a different layout than the unit capacitor, consider laying out 81 unit capacitors in a $9x9$ capacitor array using a common-centroid layout technique. Adding dummy unit capacitors on each side of the $9x9$ capacitor array, a $11x11$ capacitor array is obtained. The side length of the square $11x11$ capacitor array is:

$$L_{11x11} = 11 \cdot 16.66\mu m + 10 \cdot 0.32\mu m = 186.46\mu m \tag{6-1}$$

The corresponding area is:

$$A_{11x11} = L_{11x11}^2 = 34'767.33\mu m^2 \tag{6-2}$$

In conclusion, the by far biggest block of the ADC core consumes much less than $500x500\mu m^2$. Even the entire ADC core will be smaller than $500x500\mu m^2$.

7. Cadence issues

Typographical note: Commands you type into a terminal, keyboard shortcuts, file names, directory names, absolute/relative paths, navigation through menus, button names, messages in a terminal, and text in a file are printed in Arial, while the body text is printed in Times New Roman.

7.1. Fixing netlists

When re-creating the netlist of testbenches created on UC Merced's Cadence server, then transferred to EPFL's Cadence server, the wrong absolute paths to libraries needed for simulation may be included. E.g., when modifying the schematic view of:

- Library: Comparator
- Cell: tb_Comp6,

re-creating the netlist and running the simulation (Analog Design Environment → Simulation → Netlist and Run), several error messages like the one in Code 7-1 will appear in the *spectre.out* output file.

```
Error found by spectre during circuit read-in.
    "input.scs" 9: Unable to open library file
        `/projects/kang/PDK/UMC/UMC_18_CMOS/../Models/Spectre/MM180_SPECTRE
        _MAIN_V142.lib.scs'.
        No such file or directory.
```

Code 7-1 Error in *spectre.out* due to wrong absolute paths to libraries.

Here is my way to work around these errors:

- Analog Design Environment → Simulation → Netlist → Display
- In the header of the window that pops up, you see the name of and absolute path to the netlist. E.g. /home/meinerzh/Endspurt/cds/simulation/tb_Comp6/spectre/schematic/netlist/input.scs
- In the same window, you see 8 include instructions containing the wrong absolute path.
- In your terminal, navigate to the folder containing the netlist, e.g. by typing: cd /home/meinerzh/Endspurt/cds/simulation/tb_Comp6/spectre/schematic/netlist
- Using your favorite text editor, and conveniently one with the *Find and Replace* function, open the netlist. I recommend: gedit input.scs &
- In gedit, go to Search → Replace or use the shortcut key Ctrl + R.
- In the Replace window, write into the Search for field: /projects/kang/PDK/UMC/UMC_18_CMOS/..
- In the Replace window, write into the Replace with field: /.amd/immsunsrv1/root/da2/dkits/umc/msrf18_c01pb/fdk
- Click Replace All
- Information pop-up window: Found and replaced 8 occurrences. Click OK.
- Back in gedit: Save & Quit (Ctrl + S, Ctrl + Q)
- With the modified netlist: Analog Design Environment → Simulation → Run (Of course, do not re-create the netlist choosing Analog Design Environment → Simulation → Netlist and Run. If unintentionally you did so, repeat all the above steps.)

I am sure that Mr. Vachoux can find a better fix to this problem. In fact, there must be a way to tell Spectre the absolute path to technology files which need to be included when creating the netlist.

7.2. Finding Artist States and Simulation Data

Different installations of Cadence store Artist States and Simulation Data in different directories.

When you have opened an Analog Design Environment and want to load previously saved states, make sure to search for states in both of the following State Load Directories:

- ./artist_states absolute path: [project root]/artist_states
- ./.artist_states absolute path: [project root]/.artist_states

where [project root] is the project directory. In my case, [project root] is /home/meinerzh/Endspurt. Depending on where you install my libraries (see *Section 7.3*), your [project root] will be different.

Artist states I saved on UC Merced's Cadence server are stored in the hidden directory .artist_states (with initial dot), while artist states I saved on EPFL's Cadence server are stored in the directory artist_states (without a dot).

Simulation data is stored in the following two directories:

- [project root]/simulation/
- [project root]/cds/simulation/

In fact, UC Merced's Cadence server stores simulation data in the directory [project root]/simulation/, while EPFL's Cadence server stores it in [project root]/cds/simulation/.

Of course, for both artist states and simulation data, directories could be merged.

7.3. Installing my libraries

The following *.tar.gz files contain my libraries, artist states and simulation data:

- C_CELLS.tar.gz
- Comparator.tar.gz
- Digital.tar.gz
- Drivers.tar.gz
- SAR_ADC.tar.gz
- Switches.tar.gz
- artist_states1.tar.gz Extracts automatically into directory ./.artist_states
- artist_states2.tar.gz Extracts automatically into directory ./artist_states
- simulation1.tar.gz Extracts automatically into directory ./simulation
- simulation2.tar.gz Extracts automatically into directory ./cds/simulation

To install and re-use these libraries, along with UMC $0.18\mu m$ CMOS libraries, do the following:

- Log in onto EPFL's Cadence server with your account information.
- Navigate to your home directory and create a project directory. E.g.:
  - cd /home/misterx/
  - mkdir ADC_Meinerzh_2008
- Your project directory is now /home/misterx/ADC_Meinerzh_2008 and is also referred to as [project root] in the following text.
- In your home directory or project directory, you already have or need to create a user configuration file called edadk.conf including the line dk umc msrf18_c01pb. If you do not yet have one, you can create it, e.g. by typing:

  - cd /home/misterx
  - gedit edadk.conf &
  - Type the line dk umc msrf18_c01pb into the text file you are about to create
  - Save and quit (Ctrl + S, Ctrl + Q)
- Install the project directory for full-custom design with the UMC mixed-signal/RF 0.18um CMOS design kit:
  - cd [project root]
  - dk_setup -k umc -p msrf18 -t cadence_ic
- Copy all *.tar.gz files listed above into [project root]
- Unzip and extract all *.tar.gz files. We take Comparator.tar.gz as an example:
  - gzip –d Comparator.tar.gz (now the file is called Comparator.tar, and not Comparator.tar.gz anymore)
  - tar –xvf Comparator.tar
- After you have extracted all libraries and navigated to [project root], type icfb& to start Cadence
- In the icfb window, go to Tools → Library Path Editor…
- You will be informed that the file [project root]/cds.lib is not edit locked. Click OK.
- As you have run the dk_setup script, at least the libraries analogLib, basic and UMC_18_COMS and their associated library paths must already be defined. Check it in the Library Path Editor window.
- In the Library Path Editor window, define – in the way detailed in the next step – the following libraries and their absolute library paths:
  - C_CELLS
  - Comparator
  - Digital
  - Drivers
  - SAR_ADC
  - Switches
- We take the library Comparator as an example:
  - Enter Comparator in the Library field. Here, you define the name of the library as it will appear in the Library Manager. Use exactly the names given above, as otherwise instantiated cellviews cannot be found by Cadence.
  - Enter [project root]/Comparator in the Path field. In fact, you enter the absolute path to and name of the directory into which Comparator.tar has previously been extracted.
- After you have defined all library paths, in the Library Path Editor window, go to File → Save As and save the edited file as cds.lib in [project root]. When you are prompted if you want to overwrite the file, click Yes.
- From the icfb window, go to Tools → Library Manager…. You must see, at least, the following libraries:
  - C_CELLS
  - Comparator
  - Digital
  - Drivers
  - SAR_ADC
  - Switches
  - UMC_18_CMOS
  - analogLib

- basic

As for Artist States and Simulation Data, they are automatically extracted into the directories indicated in *Section 7.2*.

7.4. Unlocking locked files

When Cadence crashes due to a segmentation fault, it locks schematic and symbol views. When opening a locked file, you are prompted if you want to open it in ready-only mode. If you do so, you cannot make it editable afterwards using Design → Make Editable as usual.

Should this ever happen, navigate to the directory containing the cellview and remove the *.cdslck file. For example, if you try to open:

- Library: Digital
- Cell: dffpsrss
- View: schematic

for editing and it is locked, type into the terminal:

```
cd [project root]/Digital/dffpsrss/schematic
```

and remove the file sch.cdb.cdslck by typing:

```
rm sch.cdb.cdslck
```

Then, you can either open the cell view again or use Design → Make Editable to make it editable.

Lausanne, September 1, 2008

Pascal Meinerzhagen

References

[Meinerzhagen2008]
Pascal Meinerzhagen, “Design of a 12-bit low-power SAR A/D Converter for a Neurochip”, Master’s Thesis, Microelectronic Systems Laboratory, Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland and University of California, Merced, California, USA, 2008

[Kester2005]
Walt Kester, “The Data Conversion Handbook”, Analog Devices, Inc., 2005

[UMCTLR2007]
“0.18 um Mixed-Mode and RFCMOS 1.8 V/3.3 V 1P6M Metal Metal Capacitor Process Topological Layout Rule”, Ver. 2.10_P.1, Approved Date:12/07/2007, UMC Confidential no disclosure

CD, Content of ~

Typographical note: Slash (‘/’) denotes the root of the CD if not indented, and substitutes an absolute path if indented. Double-dash (‘--’) initiates a comment.

/ Design of a 12-bit low-power SAR ADC for a Neurochip.pdf -- M.Sc. Thesis Report
/ Add-on to Design of a 12-bit low-power SAR ADC for a Neurochip.pdf -- This Document
/ Design of a 12-bit low-power SAR ADC for a Neurochip.ppt -- PowerPoint Presentation
/ Cadence
    -- See *Section 7.3* for an installation guide of the Cadence database
    / C_CELLS.tar.gz
    / Comparator.tar.gz
    / Digital.tar.gz
    / Drivers.tar.gz
    / SAR_ADC.tar.gz
    / Switches.tar.gz
    / artist_states1.tar.gz
    / artist_states2.tar.gz
    / simulation1.tar.gz
    / simulation2.tar.gz
/ Mathematica
    / kToverC.nb -- Unit capacitor sizing, kT/C noise
    / NoisePreampli.nb -- Preamplifier Stage 1, thermal and 1/f noise
    / NoisePreampli2.nb -- Preamplifier Stage 2, thermal and 1/f noise
    / NoisePreampli3.nb -- Preamplifier Stage 3, thermal and 1/f noise
    / OffsetStage1.nb -- Preamplifier Stage 1, offset voltage
/ R
    / 2bw-1Cs.R -- Capacitor matching, 2bw1Cs capacitor array
    / 3bw-2Cs.R -- Capacitor matching, 3bw2Cs capacitor array
    / 4bw-3Cs.R -- Capacitor matching, 4bw3Cs capacitor array
    / C-2C.R -- Capacitor matching, C-2C ladder
/ UMC
    -- Capacitance Look-up Tables
    / G-4A-MIXED_MODE_RFCMOS18-1P6M-MMC_TOP_METAL8.6K-INTERCAP.min
    / G-4A-MIXED_MODE_RFCMOS18-1P6M-MMC_TOP_METAL8.6K-INTERCAP.typ
    / G-4A-MIXED_MODE_RFCMOS18-1P6M-MMC_TOP_METAL8.6K-INTERCAP.max