

# Breakdown of High-Performance Monolayer MoS<sub>2</sub> Transistors

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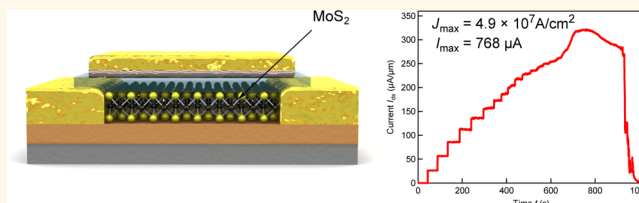
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Due to their atomic-scale thickness, two-dimensional materials such as graphene and molybdenum disulfide (MoS<sub>2</sub>) represent the ultimate limit of material scaling in the vertical dimension. Their planar geometry makes them interesting for incorporation into nanoelectronic devices where they could offer significant power savings due to reduced short channel effects. While graphene has received widespread attention due to its massless charge carriers,<sup>1,2</sup> the lack of an intrinsic band gap limits its applications in electronics to radio frequency (RF) and high-speed analog electronics. Monolayer MoS<sub>2</sub><sup>3</sup> on the other hand is a two-dimensional semiconductor with a direct band gap of 1.8 eV.<sup>4</sup> Silicon-level mobility and high current on/off ratio have recently been demonstrated<sup>5</sup> as well as its ability to amplify signals<sup>6</sup> and perform logic<sup>7</sup> operations in integrated circuits. Its high stiffness and breaking strength<sup>8</sup> also make it interesting for applications in flexible electronics, while the broken inversion symmetry in MoS<sub>2</sub> could be exploited for valleytronics.<sup>9,10</sup>

MoS<sub>2</sub> is a prototypical semiconductor from the transition metal dichalcogenide (TMD) family of materials with the common formula MX<sub>2</sub>, where M stands for a transition metal (M = Mo, W, Nb, Ta, Ti, Re) and X for Se, S, or Te. TMD crystals are formed by vertical stacking of layers, 6.5 Å thick. Layers are weakly bonded to each other by van der Waals forces which allows easy cleavage using either the micromechanical cleavage technique<sup>11,12</sup> commonly used for the production of graphene or liquid phase exfoliation.<sup>13</sup> Large-area MoS<sub>2</sub> can also be grown using CVD-like growth techniques.<sup>14,15</sup>

Metal and chalcogenide atoms are strongly bound within the layers, resulting in high mechanical strength, 30 times higher than steel in the case of MoS<sub>2</sub><sup>8</sup> and stability up to 1100 °C in inert atmosphere. MoS<sub>2</sub> is a semiconductor with a band gap that can be tuned by reducing the number

## ABSTRACT



Two-dimensional (2D) materials such as monolayer molybdenum disulfide (MoS<sub>2</sub>) are extremely interesting for integration in nanoelectronic devices where they represent the ultimate limit of miniaturization in the vertical direction. Thanks to the presence of a band gap and subnanometer thickness, monolayer MoS<sub>2</sub> can be used for the fabrication of transistors exhibiting extremely high on/off ratios and very low power dissipation. Here, we report on the development of 2D MoS<sub>2</sub> transistors with improved performance due to enhanced electrostatic control. Our devices show currents in the 100  $\mu\text{A}/\mu\text{m}$  range and transconductance exceeding 20  $\mu\text{S}/\mu\text{m}$  as well as current saturation. We also record electrical breakdown of our devices and find that MoS<sub>2</sub> can support very high current densities, exceeding the current-carrying capacity of copper by a factor of 50. Our results push the performance limit of MoS<sub>2</sub> and open the way to their use in low-power and low-cost analog and radio frequency circuits.

**KEYWORDS:** two-dimensional materials · dichalcogenides · MoS<sub>2</sub> · nanoelectronics · breakdown · transistors

of layers: bulk MoS<sub>2</sub> is semiconducting with an indirect band gap of 1.2 eV,<sup>16</sup> while single-layer MoS<sub>2</sub> is a direct gap semiconductor<sup>4,17–19</sup> with a band gap of 1.8 eV<sup>4</sup> due to quantum confinement.<sup>19</sup> The presence of a band gap in single-layer MoS<sub>2</sub> allowed the fabrication of transistors<sup>5</sup> and circuits<sup>7</sup> based on this two-dimensional semiconductor. These transistors showed high mobility (typically 200 cm<sup>2</sup>/V·s, reaching as high as 780 cm<sup>2</sup>/V·s) and high current on/off ratios (>10<sup>8</sup>). The maximal measured on-current in these devices was 10  $\mu\text{A}$  (2.5  $\mu\text{A}/\mu\text{m}$ ) for a drain bias  $V_{\text{ds}} = 500$  mV, while the highest transconductance, defined as  $g_{\text{m}} = dI_{\text{ds}}/dV_{\text{tg}}$  observed at  $V_{\text{ds}} = 500$  mV was  $\sim 4$   $\mu\text{S}$  (1  $\mu\text{S}/\mu\text{m}$ ). Although these characteristics were extremely promising for applications in low-power digital electronics, several improvements could still be

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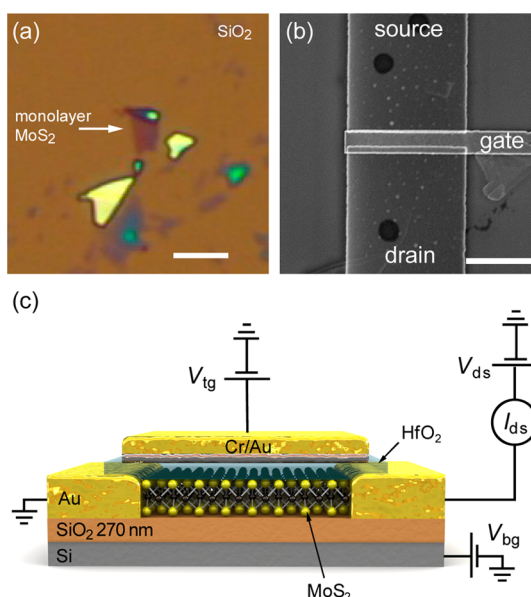
desirable from the point of view of device performance. For example, the lack of observed saturation together with the relatively low transconductance value would imply low transistor gain,<sup>20,21</sup> an important number for applications in analog electronics and power amplification. In the case of graphene, drain current saturation is very difficult to achieve, with devices in general showing weak saturation<sup>22,23</sup> or no saturation at all.<sup>24</sup>

Furthermore, it is unclear at this point what would be the performance limits and maximal on-current that two-dimensional (2D) MoS<sub>2</sub> field-effect transistors (FET) could support. They have so far been explored only using theoretical calculations in the ballistic regime.<sup>25,26</sup> Here we report a single-layer transistor with enhanced performance due to reduced access resistance and improved electrostatic control due to full-channel gating. Our transistors show a factor of 30 improvement in transconductance, 2 orders of magnitude improvement in the on-current ( $I_{on} = 600 \mu\text{A}$  or  $250 \mu\text{A}/\mu\text{m}$ ) during normal operation, the first observation of drain current saturation in monolayer MoS<sub>2</sub> transistors, and the highest mobility reported so far for monolayer MoS<sub>2</sub>. The high on-current in our devices also allows us to measure the breakdown current density in MoS<sub>2</sub> which is close to  $5 \times 10^7 \text{ A/cm}^2$  and 50 times higher than in copper. Our results demonstrate that monolayer MoS<sub>2</sub> could be used in analog circuit applications where it could provide power gain and support large current densities.

## RESULTS AND DISCUSSION

Monolayer flakes of MoS<sub>2</sub> were prepared by mechanical cleavage and scotch-tape exfoliation techniques.<sup>12,27</sup> Commercially available bulk crystals of MoS<sub>2</sub> (SPI Supplies Brand Moly Disulfide)<sup>28</sup> served as the material source. The material was deposited on a degenerately doped silicon substrate covered with 270 nm of dry SiO<sub>2</sub> (Figure 1a).<sup>29</sup> Monolayer flakes were detected and distinguished from thicker layers by measuring their optical contrast with respect to the substrate. We have previously established the correlation between contrast and thickness as measured by atomic force microscopy.<sup>29</sup>

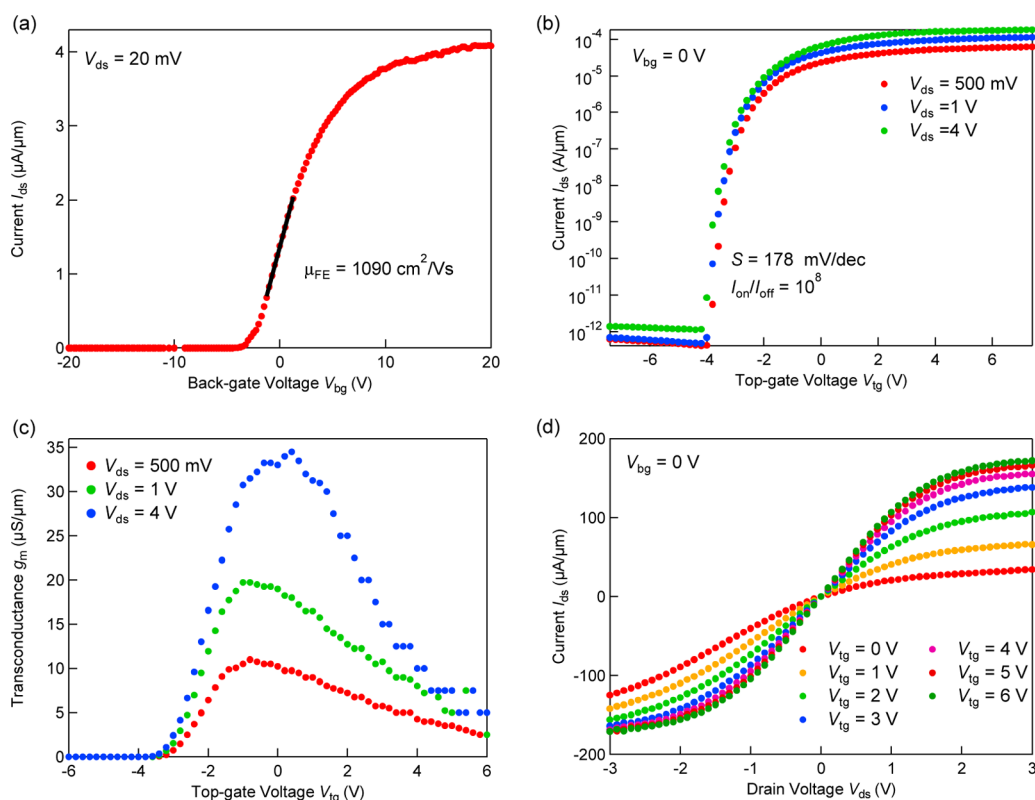
Electrical contacts were fabricated applying electron-beam lithography followed by the deposition of 90 nm Au. After acetone lift-off, the devices were annealed for 2 h in inert Ar atmosphere at 200 °C to improve contact resistance and clean the MoS<sub>2</sub> surface before top-gate oxide deposition by atomic layer deposition (ALD). A 30 nm thick layer of HfO<sub>2</sub> serving as the gate dielectric and mobility booster<sup>5,30</sup> is grown on top of MoS<sub>2</sub>. A Cr/Au top-gate of 10/50 nm thickness was then fabricated using another electron-beam lithography step (Figure 1b). The substrates were cleaved and glued to a chip carrier. Final interconnects



**Figure 1.** MoS<sub>2</sub> FET device architecture. (a) Optical image of monolayer MoS<sub>2</sub> (6.5 Å thick) exfoliated on a silicon substrate covered with a 270 nm thick SiO<sub>2</sub> layer. Scale bar is 5 μm. (b) SEM image of the final device with a HfO<sub>2</sub> gate dielectric and a local top-gate fabricated on top of the flake shown in a. Au leads of the shown device are separated by 500 nm, and the Cr/Au top-gate is 750 nm long and covers the entire channel between source and drain contact. Scale bar is 2 μm. (c) Three-dimensional representation of the monolayer MoS<sub>2</sub> FET architecture utilized in this study. The Si substrate serves as the back-gate. One of the 90 nm thick Au contacts is grounded, while the other side serves as the drain. The Cr/Au top-gate 10/50 nm thick is separated from the MoS<sub>2</sub> flake by a 30 nm thick HfO<sub>2</sub> layer.

were wire-bonded. Electrical characterization of all devices was performed at room temperature in ambient conditions (air) using an Agilent E5270B parameter analyzer. The cross section of the device is presented in Figure 1c.

This monolayer MoS<sub>2</sub> FET was first characterized by applying a fixed low drain voltage  $V_{ds}$  while sweeping the back-gate voltage  $V_{bg}$ . In Figure 2a, the corresponding measurement at  $V_{ds} = 20 \text{ mV}$  is depicted. We use the expression for the low-field field-effect mobility  $\mu = [dI_{ds}/dV_{bg}] \times [L/WC_iV_{ds}]$ , where channel length is  $L_{ch} = 500 \text{ nm}$ , channel width  $W = 2 \mu\text{m}$ , and back-gate capacitance  $C_i = \epsilon_0\epsilon_r/d = 1.3 \times 10^{-4} \text{ F/m}^2$  ( $\epsilon_r = 3.9$ ,  $d = 270 \text{ nm}$ ). With this, a field-effect mobility of  $\mu = 1090 \text{ cm}^2/\text{V}\cdot\text{s}$  at a drain voltage of  $V_{ds} = 20 \text{ mV}$  can be estimated. This value is the highest mobility presented to date in MoS<sub>2</sub> FETs and represents a lower limit of the mobility in the 6.5 Å thick semiconducting MoS<sub>2</sub> monolayer since contact resistance is not being accounted for. Errors in the estimate of capacitive coupling could be a further source of experimental uncertainty. A possible cause for the significant increase in mobility could be the fact that in a shorter channel the charge-trap density of the SiO<sub>2</sub> surface right below the 6.5 Å thick charge carrier channel is reduced. Access resistance could also be reduced in



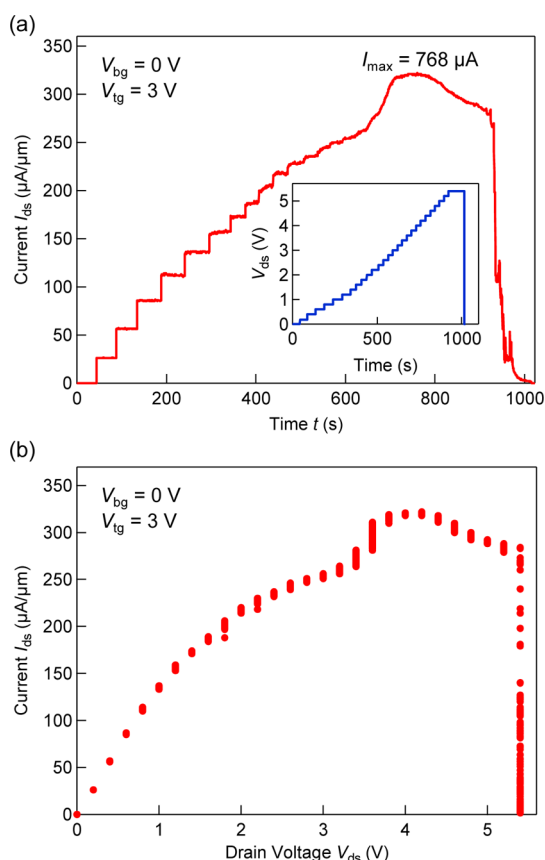
**Figure 2.** Characterization of a monolayer MoS<sub>2</sub> FET transistor. (a) Room-temperature back-gate transfer characteristic for the MoS<sub>2</sub> FET depicted in Figure 1a,b under the applied drain voltage  $V_{ds} = 20$  mV. We estimate an effective field-effect mobility  $\mu_{FE} = 1090$  cm<sup>2</sup>/V·s. (b)  $I_{ds}$ – $V_{tg}$  curve recorded for three different drain voltages:  $V_{ds} = 500$  mV, 1 V, and 4 V. The  $I_{on}/I_{off}$  ratio exceeds  $10^8$ . The subthreshold swing  $S$  at  $V_{ds} = 500$  mV is 178 mV/dec. (c) Transconductance  $g_m = dI_{ds}/dV_{tg}$  derived from  $I_{ds}$ – $V_{tg}$  characteristics shown in b. The peak transconductance for  $V_{ds} = 4$  V is  $g_{m,max} = 34$   $\mu$ S/ $\mu$ m and is the highest value of transconductance reported for MoS<sub>2</sub> transistors to date. (d)  $I_{ds}$ – $V_{ds}$  characteristics measured for different top-gate voltages  $V_{tg}$  for drain voltages  $V_{ds}$  reaching 3 V. In this device, the on-current is  $I_{on} = 344$   $\mu$ A (172  $\mu$ A/ $\mu$ m) for  $V_{tg} = 6$  V and  $V_{ds} = 3$  V, corresponding to a current density of  $J = 2.5 \times 10^7$  A/cm<sup>2</sup>. This value is 25 times larger than the breakdown current density of copper. At typical bias voltages with  $V_{ds}$  exceeding  $\sim 2$  V, the drain current shows saturation with the drain–source  $g_{ds} = dI_{ds}/dV_{ds}$  close to 0 ( $g_{ds} < 2$   $\mu$ S/ $\mu$ m) at  $V_{ds} = 3$  V. At low bias voltages, the curves are linear, indicating that the contacts are ohmic.

this case due to full-channel gating. This motivates further studies on even shorter channel lengths ( $L_{ch} < 500$  nm). In Figure 2b the  $I_{ds}$ – $V_{tg}$  characteristics for varying  $V_{ds}$  is depicted. The  $I_{on}/I_{off}$  ratio for an applied drain voltage of  $V_{ds} = 4$  V and the  $\pm 6$  V variation of top-gate voltage  $V_{tg}$  is on the order of  $10^8$ . This  $I_{on}/I_{off}$  ratio exceeds the value of  $10^4$ – $10^7$  considered necessary for applications in CMOS-like digital circuits.<sup>21,31</sup> At  $V_{ds} = 500$  mV, a subthreshold slope, defined as  $S = (d(\log I_{ds})/dV_{tg})^{-1}$ , of  $S = 178$  mV/dec can be extracted. In earlier studies, a lower value for the subthreshold swing in this case could be partial electrostatic shielding of the top-gate by source and drain contacts and a higher trap charge density in either the MoS<sub>2</sub>/SiO<sub>2</sub> or MoS<sub>2</sub>/HfO<sub>2</sub> interface.

The electrical conductivity of the monolayer MoS<sub>2</sub> can be controlled in a wide range using a top-gate because of the presence of a band gap and large degree of electrostatic control due to its atomic-scale thickness.<sup>25</sup> From the top-gating ( $I_{ds}$ – $V_{tg}$  characteristics ( $I_{ds}$ – $V_{tg}$ ) shown in Figure 2b, the transconductance  $g_m = dI_{ds}/dV_{tg}$  can be derived. In Figure 2c, we plot the

2D MoS<sub>2</sub> device transconductance for three different drain voltages:  $V_{ds} = 500$  mV, 1 V, and 4 V. The maximal derived transconductance  $g_{m,max}(V_{ds} = 4$  V) = 34  $\mu$ S/ $\mu$ m and is the highest value of transconductance reported for MoS<sub>2</sub> transistors to date. The transconductance at  $V_{ds} = 1$  V is  $\sim 20$   $\mu$ S/ $\mu$ m.

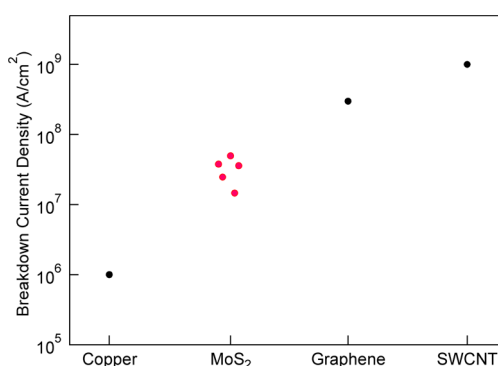
Subsequently, the drain–source bias ( $I_{ds}$ – $V_{ds}$ ) characteristic is probed and reported in Figure 2d. For these measurements, the back-gate voltage  $V_{bg}$  is kept at 0 V. At relatively low drain voltages exceeding  $V_{ds}$  of 1 V, the current-carrying capacity of the MoS<sub>2</sub> charge-carrying channel exhibits saturation, making this the first observation of drain current saturation in monolayer MoS<sub>2</sub> FETs. The drain–source conductance  $g_{ds} = dI_{ds}/dV_{ds}$  is close to 0 ( $g_{ds} < 2$   $\mu$ S/ $\mu$ m) in this region of operation. In this regime, the transistor can operate as a voltage-regulated current source. Saturation is also important for achieving maximum possible operating speeds.<sup>21</sup> This measurement was repeated on the same device with varying top-gate voltages  $V_{tg}$  ranging between 0 and 6 V (the maximum value is limited by the dielectric strength of the oxide and at a HfO<sub>2</sub> thickness of 30 nm oxide breakthrough has been



**Figure 3.** Maximum current density of monolayer MoS<sub>2</sub> FETs. (a) Time trace of the drain current  $I_{ds}$  recorded during the breakdown of a monolayer MoS<sub>2</sub> FET. Back-gate voltage  $V_{bg} = 0$  V, top-gate voltage  $V_{tg} = 3$  V. Inset: corresponding  $V_{ds}$  vs time.  $V_{ds}$  is increased in steps of 200 mV approximately every 30 s. The current is allowed to stabilize between the steps. The maximum recorded value of the current for this device is  $I_{ds,max} = 768 \mu\text{A}$  ( $320 \mu\text{A}/\mu\text{m}$ ) for  $V_{ds} = 4.2$  V, which marks the beginning of the electrical deterioration of the device and its current-carrying capacity with final breakdown occurring at  $V_{ds} = 5.4$  V. This corresponds to a current density of  $J = 4.9 \times 10^7$  A/cm<sup>2</sup> and represents the highest current density reported for MoS<sub>2</sub> so far. (b)  $I_{ds}$ – $V_{ds}$  characteristics for the same measurement as depicted in part a.

observed at  $V_{tg}$  values exceeding 8 V). At a top-gate voltage of  $V_{tg} = 6$  V and a drain voltage of  $V_{ds} = 3$  V, the monolayer MoS<sub>2</sub> channel is carrying a current of  $344 \mu\text{A}$  ( $172 \mu\text{A}/\mu\text{m}$ ). When the thickness of the material ( $t = 6.5 \text{ \AA}$ ) is taken into account, this corresponds to an exceptionally high current density of more than  $2.5 \times 10^7$  A/cm<sup>2</sup>. For low bias voltages, the curve shows linear and symmetric behavior, indicating that our Au–MoS<sub>2</sub> contacts are ohmic.

The ratio of transconductance to drain conductance ( $A = g_m/g_{ds}$ ) is an important figure of merit, and it represents the highest gain achievable using a single transistor.<sup>20</sup> With relatively high values of transconductance ( $g_m = 20 \mu\text{S}/\mu\text{m}$  for  $V_{ds} = 1$  V and  $g_m = 34 \mu\text{S}/\mu\text{m}$  for  $V_{ds} = 4$  V) and observed current saturation ( $g_{ds} < 2 \mu\text{S}/\mu\text{m}$ ), our results show that MoS<sub>2</sub> could be interesting not only for applications in digital electronics<sup>7</sup>



**Figure 4.** Comparison of breakdown current density for different nanoelectronic materials. The current-carrying capacity of copper is reported to be on the order of  $10^6$  A/cm<sup>2</sup>. Breakdown currents demonstrated in this study for a single layer of semiconducting MoS<sub>2</sub> are close to  $5 \times 10^7$  A/cm<sup>2</sup>. This value is 50 times higher than the electromigration-limited current-carrying capacity of copper.<sup>35</sup> For graphene and metallic single-walled carbon nanotubes, values on the order of  $10^8$  and  $10^9$  A/cm<sup>2</sup> for devices on SiO<sub>2</sub> substrates have been reported in the literature.<sup>32,33</sup>

but also for analog applications where it could offer gain  $>10$ .

We further investigate the high current-carrying capacity and electrical breakdown of monolayer MoS<sub>2</sub> using two different measurement schemes. In the first one, the  $V_{ds}$  is increased in steps of 200 mV approximately every 30 s in order to keep the current flowing under constant conditions for a short period of time. This stepwise increase of  $V_{ds}$  is continued until the device breaks down. The time dependence of the drain current for a typical device at the back-gate voltage of  $V_{bg} = 0$  V and a top-gate voltage  $V_{tg} = 3$  V is shown in Figure 3a with the corresponding  $I_{ds}$ – $V_{ds}$  dependence presented in Figure 3b. For small values of the drain voltage, the drain current increases as a linear function of the voltage, and above  $\sim 1$  V, the current begins to saturate, reaching a value of  $600 \mu\text{A}$  ( $250 \mu\text{A}/\mu\text{m}$ ) for  $V_{ds} = 3.4$  V. Further increase in bias voltage results in a rapid increase of the current, possibly due to Joule heating-induced contact annealing, up to a value of  $768 \mu\text{A}$  ( $320 \mu\text{A}/\mu\text{m}$ ) for  $V_{ds} = 4.2$  V, which is the maximum recorded current for this device. With the thickness of a monolayer of  $t = 6.5 \text{ \AA}$ , this corresponds to a current density of  $4.9 \times 10^7$  A/cm<sup>2</sup>. Further increase of the voltage results in a gradual current decrease and complete failure at a bias voltage of  $V_{ds} = 5.4$  V. The described behavior has been similarly observed for five additional devices. We have also used a second measurement method in which the drain voltage  $V_{ds}$  is continuously swept between increasing values of maximal voltage until breakdown occurs. Both methods result in similar maximal current values.

We compare the breakdown current density of monolayer MoS<sub>2</sub> with other typical nanoelectronic materials in Figure 4. Record values for maximum current densities are reported for graphene on



SiO<sub>2</sub> (>10<sup>8</sup> A/cm<sup>2</sup>),<sup>32</sup> metallic single-walled carbon nanotubes (>10<sup>9</sup> A/cm<sup>2</sup>),<sup>33</sup> and copper (~10<sup>6</sup> A/cm<sup>2</sup>).<sup>34</sup> Considering that MoS<sub>2</sub> is a semiconductor, the extracted maximum current density demonstrated is extremely high and is 50 times higher than the limit set for metals by electromigration.<sup>35</sup> This is due to strong intralayer Mo–S covalent bonds<sup>8,36</sup> which are much stronger than metallic bonds. Integration with high thermal conductivity substrates such as diamond<sup>37</sup> could result in further increase of breakdown current density.

## CONCLUSION

To summarize, we have produced high-performance 2D transistors based on monolayer MoS<sub>2</sub> showing the highest on-current, highest transconductance and highest estimated mobility reported to date for a 2D

transition metal dichalcogenide, while keeping the extremely high room-temperature current on/off ratio of 10<sup>8</sup>. Our transistors with a channel length of 500 nm and no underlap show drain current saturation for the first time in monolayer MoS<sub>2</sub>, with drain conductance  $g_{ds}$  lower than 2  $\mu$ S and maximum transconductance of  $g_m = 34 \mu$ S/ $\mu$ m. We also find that monolayer MoS<sub>2</sub> can support large current densities, close to  $5 \times 10^7$  A/cm<sup>2</sup>, exceeding breakdown current density of copper by a factor of 50.

Our results demonstrate that MoS<sub>2</sub> is suitable for the production of high-performance transistors with high internal gain capable of supporting high current densities. This is an important step in realizing 2D nanoelectronic circuits and devices characterized with high-performance, low-power dissipation, and low cost.

## METHODS

Single layers of MoS<sub>2</sub> are exfoliated from commercially available crystals of molybdenite (SPI Supplies Brand Moly Disulfide)<sup>28</sup> using the scotch-tape micromechanical cleavage technique method pioneered for the production of graphene. After 90 nm thick Au contact deposition, devices are annealed in 100 sccm of Ar at 200 °C for 2 h.<sup>38</sup> ALD is performed in a commercially available system (Beneq) using a reaction of H<sub>2</sub>O with tetrakis(ethyl methylamido)hafnium. Electrical characterization is carried out using an Agilent E5270B parameter analyzer and a home-built shielded probe station with micro-manipulated probes.

**Conflict of Interest:** The authors declare no competing financial interest.

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## REFERENCES AND NOTES

- Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Katsnelson, M. I.; Grigorieva, I. V.; Dubonos, S. V.; Firsov, A. A. Two-Dimensional Gas of Massless Dirac Fermions in Graphene. *Nature* **2005**, *438*, 197–200.
- Zhang, Y.; Tan, Y.-W.; Stormer, H. L.; Kim, P. Experimental Observation of the Quantum Hall Effect and Berry's Phase in Graphene. *Nature* **2005**, *438*, 201–204.
- Joensen, P.; Frindt, R. F.; Morrison, S. R. Single-Layer MoS<sub>2</sub>. *Mater. Res. Bull.* **1986**, *21*, 457–461.
- Mak, K. F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T. F. Atomically Thin MoS<sub>2</sub>: A New Direct-Gap Semiconductor. *Phys. Rev. Lett.* **2010**, *105*, 136805.
- Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS<sub>2</sub> Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150.
- Radisavljevic, B.; Whitwick, M. B.; Kis, A. Small-Signal Amplifier Based on Single-Layer MoS<sub>2</sub>. *Appl. Phys. Lett.* **2012**, *101*, 043103.
- Radisavljevic, B.; Whitwick, M. B.; Kis, A. Integrated Circuits and Logic Operations Based on Single-Layer MoS<sub>2</sub>. *ACS Nano* **2011**, *5*, 9934–9938.
- Bertolazzi, S.; Brivio, J.; Kis, A. Stretching and Breaking of Ultrathin MoS<sub>2</sub>. *ACS Nano* **2011**, *5*, 9703–9709.
- Xiao, D.; Liu, G.-B.; Feng, W.; Xu, X.; Yao, W. Coupled Spin and Valley Physics in Monolayers of MoS<sub>2</sub> and Other Group-VI Dichalcogenides. *Phys. Rev. Lett.* **2012**, *108*, 196802.
- Mak, K. F.; He, K.; Shan, J.; Heinz, T. F. Control of Valley Polarization in Monolayer MoS<sub>2</sub> by Optical Helicity. *Nat. Nanotechnol.* **2012**, *7*, 494–498.
- Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666–669.
- Novoselov, K. S.; Jiang, D.; Schedin, F.; Booth, T. J.; Khotkevich, V. V.; Morozov, S. V.; Geim, A. K. Two-Dimensional Atomic Crystals. *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 10451–10453.
- Coleman, J. N.; Lotya, M.; O'Neill, A.; Bergin, S. D.; King, P. J.; Khan, U.; Young, K.; Gaucher, A.; De, S.; Smith, R. J.; et al. Two-Dimensional Nanosheets Produced by Liquid Exfoliation of Layered Materials. *Science* **2011**, *331*, 568–571.
- Liu, K.-K.; Zhang, W.; Lee, Y.-H.; Lin, Y.-C.; Chang, M.-T.; Su, C.-Y.; Chang, C.-S.; Li, H.; Shi, Y.; Zhang, H.; et al. Growth of Large-Area and Highly Crystalline MoS<sub>2</sub> Thin Layers on Insulating Substrates. *Nano Lett.* **2012**, *12*, 1538–1544.
- Zhan, Y.; Liu, Z.; Najmaei, S.; Ajayan, P. M.; Lou, J. Large-Area Vapor-Phase Growth and Characterization of MoS<sub>2</sub> Atomic Layers on a SiO<sub>2</sub> Substrate. *Small* **2012**, *8*, 966–971.
- Kam, K. K.; Parkinson, B. A. Detailed Photocurrent Spectroscopy of the Semiconducting Group VIB Transition Metal Dichalcogenides. *J. Phys. Chem.* **1982**, *86*, 463–467.
- Lebegue, S.; Eriksson, O. Electronic Structure of Two-Dimensional Crystals from *Ab Initio* Theory. *Phys. Rev. B* **2009**, *79*, 115409.
- Splendiani, A.; Sun, L.; Zhang, Y.; Li, T.; Kim, J.; Chim, C.-Y.; Galli, G.; Wang, F. Emerging Photoluminescence in Monolayer MoS<sub>2</sub>. *Nano Lett.* **2010**, *10*, 1271–1275.
- Kuc, A.; Zibouche, N.; Heine, T. Influence of Quantum Confinement on the Electronic Structure of the Transition Metal Sulfide TS<sub>2</sub>. *Phys. Rev. B* **2011**, *83*, 245213.
- Horowitz, P.; Hill, W. *The Art of Electronics*; Cambridge University Press: Cambridge, UK, 1989.
- Schwierz, F. Graphene Transistors. *Nat. Nanotechnol.* **2010**, *5*, 487–496.
- Meric, I.; Han, M. Y.; Young, A. F.; Ozyilmaz, B.; Kim, P.; Shepard, K. L. Current Saturation in Zero-Bandgap, Top-Gated Graphene Field-Effect Transistors. *Nat. Nanotechnol.* **2008**, *3*, 654–659.

23. Bai, J.; Liao, L.; Zhou, H.; Cheng, R.; Liu, L.; Huang, Y.; Duan, X. Top-Gated Chemical Vapor Deposition Grown Graphene Transistors with Current Saturation. *Nano Lett.* **2011**, *11*, 2555–2559.
24. Lin, Y.-M.; Dimitrakopoulos, C.; Jenkins, K. A.; Farmer, D. B.; Chiu, H.-Y.; Grill, A.; Avouris, P. 100-GHz Transistors from Wafer-Scale Epitaxial Graphene. *Science* **2010**, *327*, 662.
25. Yoon, Y.; Ganapathi, K.; Salahuddin, S. How Good Can Monolayer MoS<sub>2</sub> Transistors Be?. *Nano Lett.* **2011**, *11*, 3768–3773.
26. Liu, L.; Kumar, S. B.; Ouyang, Y.; Guo, J. Performance Limits of Monolayer Transition Metal Dichalcogenide Transistors. *IEEE Electron Device Trans.* **2011**, *58*, 3042–3047.
27. Frindt, R. F. Single Crystals of MoS<sub>2</sub> Several Molecular Layers Thick. *J. Appl. Phys.* **1966**, *37*, 1928–1929.
28. Purchased from SPI supplies, www.2spi.com, catalog number 429 ML-AB. Collected by a professional geologist at Otter Lake deposit in Ontario, Canada. Specifications available at <http://www.2spi.com/catalog/molybdenum.shtml>.
29. Benameur, M. M.; Radisavljevic, B.; Heron, J.-S.; Sahoo, S.; Berger, H.; Kis, A. Visibility of Dichalcogenide Nanolayers. *Nanotechnology* **2011**, *22*, 125706.
30. Jena, D.; Konar, A. Enhancement of Carrier Mobility in Semiconductor Nanostructures by Dielectric Engineering. *Phys. Rev. Lett.* **2007**, *98*, 136805.
31. *The International Technology Roadmap for Semiconductors*, <http://www.itrs.net/Links/2009ITRS/Home2009.htm> (Semiconductor Industry Association, 2009).
32. Moser, J.; Barreiro, A.; Bachtold, A. Current-Induced Cleaning of Graphene. *Appl. Phys. Lett.* **2007**, *91*, 163513.
33. Yao, Z.; Kane, C. L.; Dekker, C. High-Field Electrical Transport in Single-Wall Carbon Nanotubes. *Phys. Rev. Lett.* **2000**, *84*, 2941–2944.
34. Robertson, J. Growth of Nanotubes for Electronics. *Mater. Today* **2007**, *10*, 36–43.
35. Christou, A. *Electromigration and Electronic Device Degradation*; Wiley: New York, 1994.
36. Ataca, C.; Şahin, H.; Ciraci, S. Stable, Single-Layer Mx<sub>2</sub> Transition-Metal Oxides and Dichalcogenides in a Honeycomb-like Structure. *J. Phys. Chem. C* **2012**, *116*, 8983–8999.
37. Yu, J.; Liu, G.; Sumant, A. V.; Goyal, V.; Balandin, A. A. Graphene-on-Diamond Devices with Increased Current-Carrying Capacity: Carbon sp<sup>2</sup>-on-sp<sup>3</sup> Technology. *Nano Lett.* **2012**, *12*, 1603–1608.
38. Ishigami, M.; Chen, J. H.; Cullen, W. G.; Fuhrer, M. S.; Williams, E. D. Atomic Structure of Graphene on SiO<sub>2</sub>. *Nano Lett.* **2007**, *7*, 1643–1648.