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RF Compact Modeling of High-voltage MOSFETs

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ABSTRACT

The High-Voltage MOSFET is used in a wide variety of applications covering from power systems up to RF-IC. Compact models that describe the high-frequency behavior of the device are required to predict high-frequency operation and switching capabilities of these elements in HV state-of-the-art systems. In this paper, an RF model is presented and verified against extensive Y-parameter measurements, which were carried out on a long channel Lateral double-Diffusion MOS device. Assessment of the model with measurements confirms the validity of this approach.

Keywords:
Drift region, *High-frequency regime*, *High-Voltage MOSFET*, *HV-MOS*, *LDMOS*, *Physics-based analytical compact model*, *RF*.

1. INTRODUCTION

The importance of the High-Voltage (HV-MOS) as a device in state-of-the-art applications has been reported extensively in scientific literature [1-5]. One of the reasons is that modern HV-MOS devices, like Lateral double-Diffusion MOS (LDMOS), may be integrated together with low-voltage modules in CMOS processes [3,5]. The systems, where such devices are used, range from power components for automotive and consumer products [2] up to radio frequency applications [6-8]. Therefore, compact modeling of HV-MOS is an enabling factor that will help in predicting how these devices can be optimally integrated in complex architectures [9-26]. More particularly, the RF characterization and modeling of HV-MOS should receive extra attention since the high-frequency behavior is, still, a quite demanding and challenging issue. The results presented here are a continuation of a previous work that has already been published [27].

2. MODEL DESCRIPTION

The structure of an HV-MOS, if simplified, may be regarded as the in series combination of two simpler elements. On one side lays the low-voltage part which closely resembles to a classical MOSFET, except for the relatively high longitudinal doping gradient across the channel [9,27]. On the other side, beyond the inner drain of the low-voltage part there is the high-voltage section which protects the low-voltage MOSFET from excessively high potentials. This part, also called drift region, has the same type doping as the outer drain and source of the HV-MOS. Its quite long extension, i.e., a few microns, ensures safe operation needed for the device to function at dozens of volts [26].

The compact model used in this work takes advantage of the above simplification, describing the whole structure as a macromodel of two basic elements. The connection of these two elements takes place at a node called the K-point, which is, in physical terms, the metallurgical junction point where the doping profile changes its type, between the channel of the low-voltage part and the drift region [14,25]. In order to model the device at RF, additional extrinsic components must be added. Among them, there are a gate resistance and two asymmetrical junction diodes between the source and the drain terminals and the substrate. In addition, it has been observed that overlap capacitances between the gate and other nodes are not negligible. These overlap capacitances become even more important for specific small geometries.

The elements of the intrinsic part of the model can be considered as a small signal equivalent network built upon transcapacitances and current sources. For the core of the model, and omitting higher order effects like impact ionization current, the low-voltage part of the device can be represented by three transcapacitances between the gate and other nodes, and a current source between the K-point and the source node. In addition, a similar representation can de adopted for the drift region. Here, again a current source is needed between the outer drain and the K-point, and also two transcapacitances, one between the gate and the K-point that describes the charge behavior of the carriers just below the oxide, and one more between

the gate node and the outer drain, which accounts for the charges laying in the rest of the drift region. This is sketched in the small signal equivalent circuit schematic of Figure 1.

2.1 Dynamic Charge Behavior of the Drift Region

The dynamic behavior of the low-voltage part of the device including a MOSFET with lateral non-uniform doping is analyzed in [9,28-30], while a detailed analysis of the charge has been discussed in [27]. In this article, the discussion on the dynamic behavior of the HV-MOS devices will be pursued by giving a transcapacitance representation of the charges in the drift region.

Considering the charge-sheet approximation [31], the charge of the drift region may be considered as the sum of two components. The first component (q_k) is the charge accumulated just below the thin oxide and has been analyzed in [27]. If W_{DK} and $L_{OV.DK}$ are the width and the effective gate length overlap the drift region, respectively, and T_{OX} is the effective thickness of the thin oxide above the drift region, then the total charge at the K-point is calculated from:

$$Q_{K.DK} = \frac{\varepsilon_{OX} \cdot W_{DK} \cdot L_{OV.DK}}{T_{OX}} \cdot q_k , \quad (1)$$

Where, ε_{OX} is the permittivity of the oxide, and q_k and $Q_{K.DK}$ are respectively the normalized and absolute charge densities [32].

On the other hand, the sum of the charge in the drift region will be equal (in absolute value and opposite in sign) with the charge that will accumulate at the gate node ($Q_{G.DK}$). If $Q_{D.DK}$ denotes the charge at the inner part of the drift region, we get:

$$Q_{G.DK} = -\left(Q_{K.DK} + Q_{D.DK}\right). \quad (2)$$

Note that $Q_{G.DK}$ stands only for the part of the gate charge that is connected with the drift region, and does not represent the whole charge of the gate node. This charge may be calculated after the following equation.

$$Q_{G.DK} = \frac{\varepsilon_{OX} \cdot W_{DK} \cdot L_{OV.DK}}{T_{OX}} \cdot \left(V_G - V_{FB.DK} - \Psi_K\right). \quad (3)$$

In the above equation, $V_{FB.DK}$ denotes the Flat-Band voltage of the drift region and the Ψ_K is the surface potential at the K-point. The latter is calculated from the potential of the internal node of the K-point (V_K), which is evaluated considering the continuity of the current at the K-point [27]. Therefore, the above set of equations form the core of the model for the dynamic behavior of the drift region.

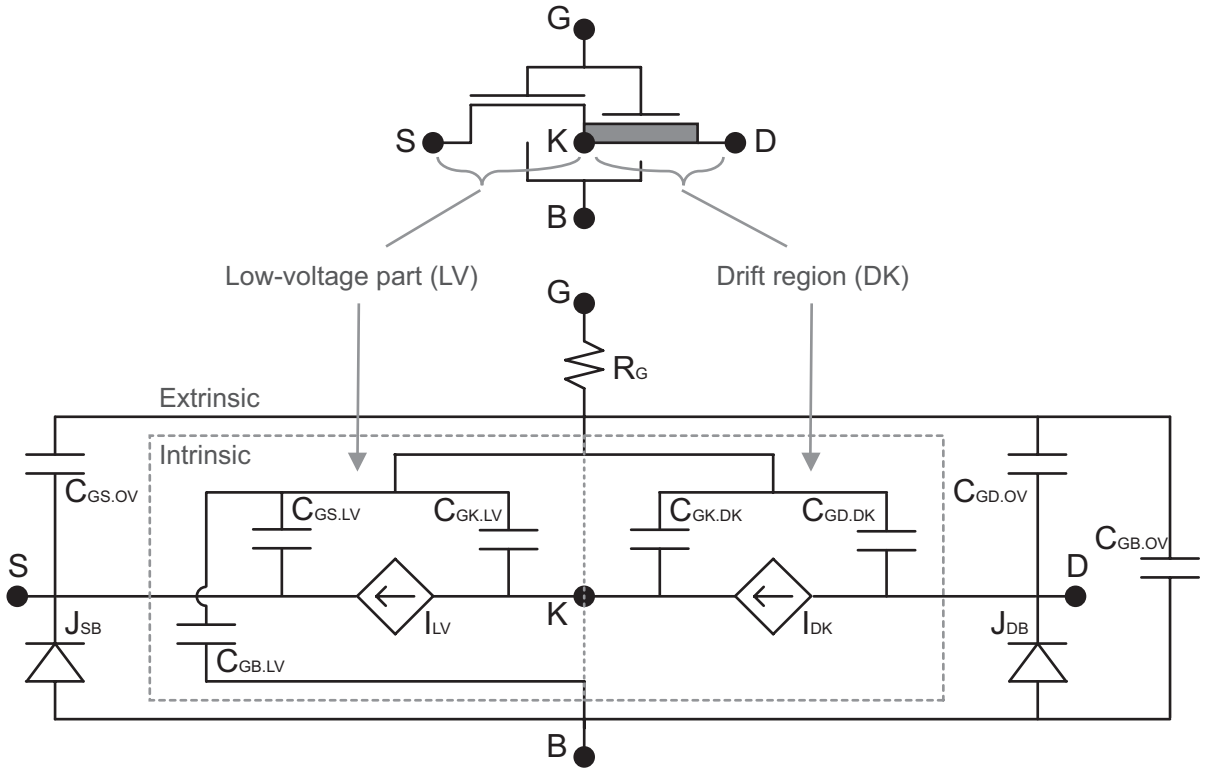

Figure 1: Small Signal equivalent circuit of the macromodel for the HV-MOS. The intrinsic and extrinsic parts are shown, while the intrinsic part is further divided into the low-voltage part and the drift region. For the intrinsic part, transcapacitances and current sources are used, while the extrinsic part consists of junction-diodes, resistors, and capacitors.

3. COMPARISON WITH MEASUREMENTS

The model has been verified against numerical simulations of Technology Computer-Aided Design (TCAD) tools and real measurements [27]. Few selected results will be presented in this section in order to demonstrate its capabilities. For this purpose, an LDMOS device has been chosen with a minimum gate length of L = 500 nm. The gate width is W = 40 μm, while the thickness of the oxide is T_{OX} = 15 nm in order to withstand a gate potential up to 5 V.

3.1 Static Current Aspects

In Figure 2, a comparison between the model and measurement for various static current conditions is presented. The model shows good capabilities under all bias conditions. The device's behavior is more complicated than the classical MOSFET case since there is a continuous balance between the two parts of the device that sets the quasi-fermi potential of the K-point. In principle, it could be said that for low gate potential, when the channel of the low-voltage MOSFET of the device is in weak inversion, the overall device acts similarly to a classic MOSFET having a resistive load at its drain. As the inversion level increases and the low-voltage part gets deeper in strong inversion, more and more carriers can be provided to the drift region. Under these bias conditions, it is the drift region that will govern the overall behavior of the device, especially for high V_{DS} values, and the device differentiates importantly from the classic MOSFET.

3.2 Dynamic Behavior Analysis

In order to validate the model according to its dynamic behavior, the LDMOS device was also measured at high frequencies. Considering the device as a two-port network, where the input (port 1) is between gate and source, and the output (port 2) is between drain and source (which is connected to the ground), S-parameter measurements were performed up to 6 GHz. The measurements were done under various bias conditions. When V_{DS} was zero, the gate potential varied between -4V and 4V, while with positive $V_{DS,}$ the gate potential swept between 0.8V and 4.8V. The S-parameters were transformed to Y-parameters, which are better suited for the voltage-to-current terminology already used in static analysis. Figure 3 shows some selective results of the above measurements for a specific frequency, f = 1.2 GHz, displayed along with the simulation obtained from the model. The model covers adequately the high-frequency behavior of the device under an extended range of bias conditions providing good results in terms of Y-parameters for all modes of operation.

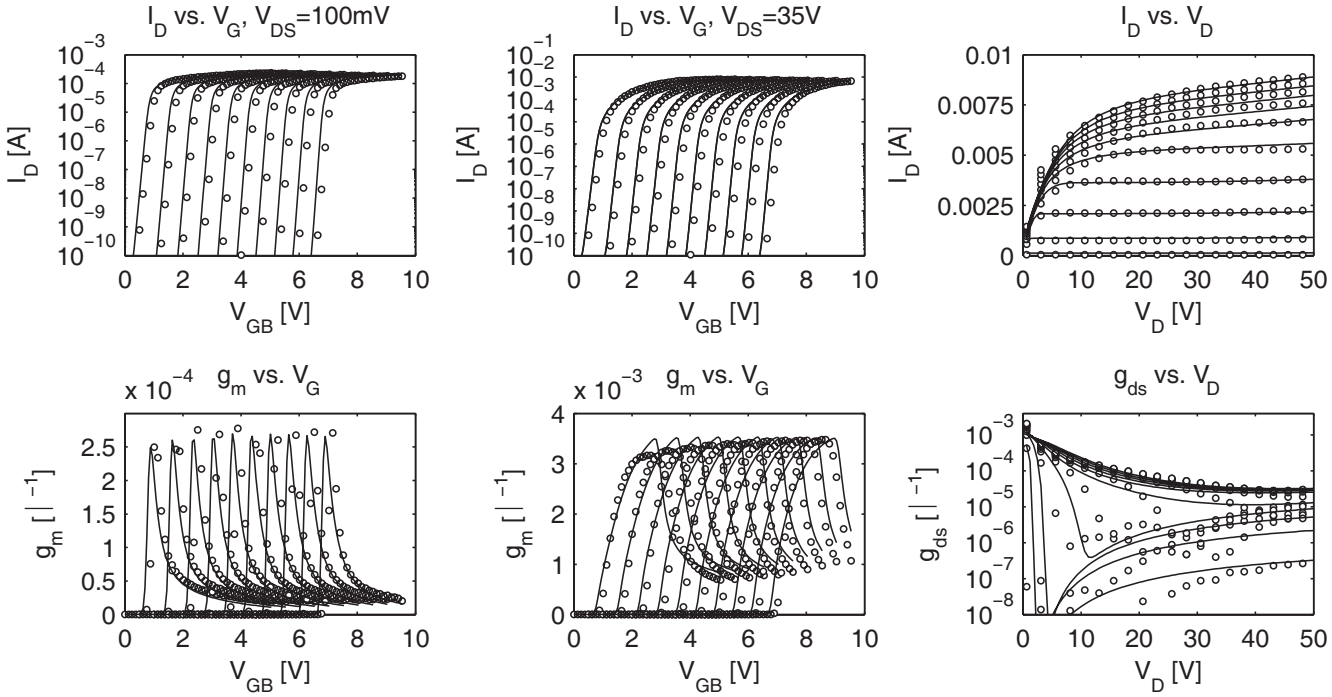

Figure 2: Static current measurements (markers) and model behavior (lines) of an LDMOS (L=500 nm, W=40 μm, TOX=15 nm). The two plots on the left are an I_D vs. V_G analysis with a low value for V_{DS}=100 m and for various *V*SB values between 0V and 4.5V. The two plots in the middle repeat the same analysis with high value for V_{DS}=35 V. The two plots on the right illustrate and I_D vs. V_D where V_{SB}=0V and V_{GS} ranges between 1V and 5.5V. The upper graphs show the current while the lower either the transconductance, gm for the analyses I_D vs. V_G, or the output conductance, gds, for the I_D vs. V_D analysis.

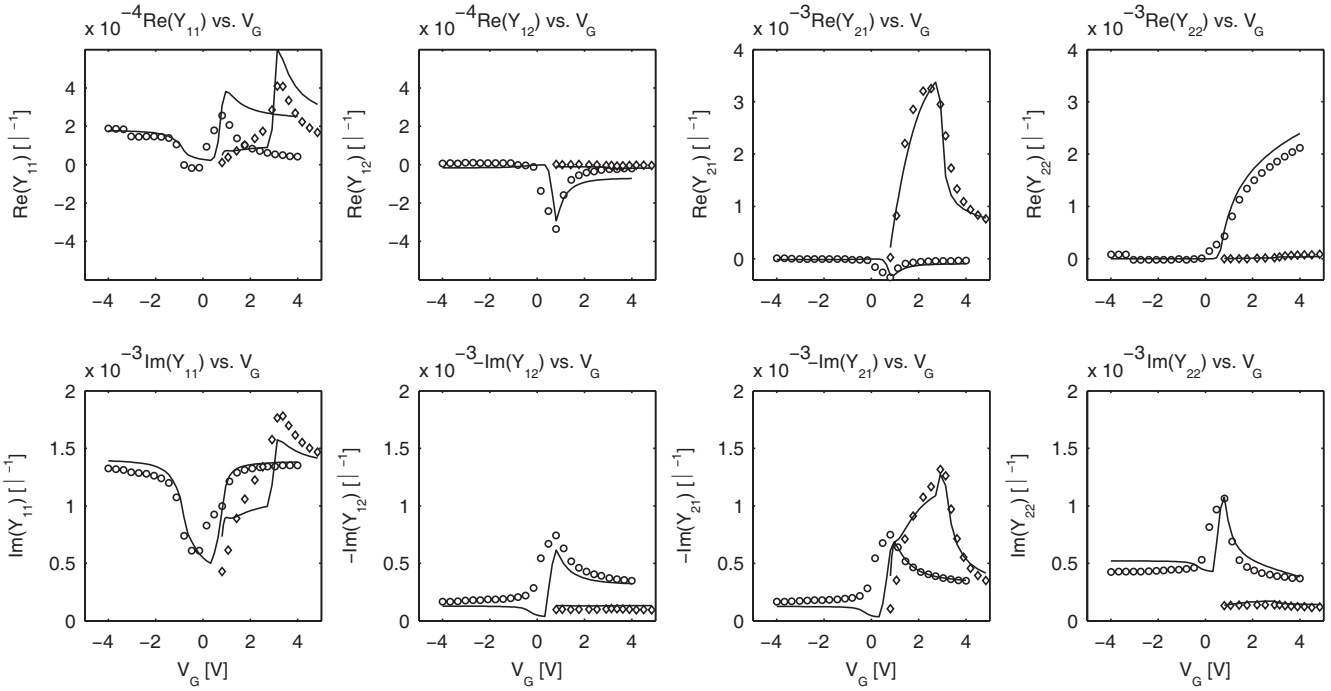

Figure 3: Y-parameters, in real and imaginary part, of an LDMOS device with geometric parameters of L=500 nm, W=40 μm, and T_{OX}=15 nm. The markers (V_{DS}=0V: ○ and V_{DS}=30V: ◊) are for measurements while the lines are the model's behavior. Port 1 is gate-to-source and port 2 is drain-to-source, and V_{SB}=0V. The results are shown for frequency f=1.2GHz.

4. EXTRINSIC NETWORK AND RF PARAMETER EXTRACTION

In this section, a short analysis on the parameter extraction procedure will be discussed. It shall be focused on the extraction of the parameters related to the extrinsic part of the device which may benefit from the high-frequency analysis of the device [33-36]. Although the core of the following techniques is based on the classic MOSFET, it shall be shown that there is enough space for its application to HV-MOS devices.

4.1 Gate Resistance

By analyzing the small signal equivalent circuit, and its functionality under small signal conditions, the gate resistance can be estimated by the following equation [33,37].

$$R_G = \frac{Re(Y_{11})}{Im(Y_{11})^2}. \quad (4)$$

In Figure 4, the estimation of the gate resistance is plotted against the gate potential for the LDMOS device under test. The extraction of the value of the gate resistance is best performed under negative gate bias conditions and with V_{DS} = 0V, since this bias minimizes the influence of the rest of the device. For the simulations shown here, a value of 90Ω has been used for R_G which is very close to the estimation of (4) for low enough values of the gate

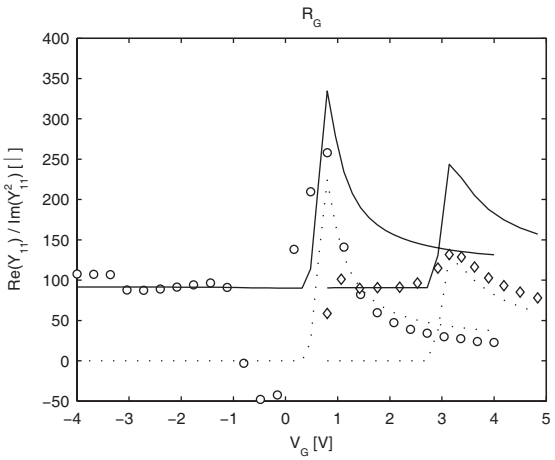

Figure 4: The Gate Resistance (R_G) as estimated by (4) under various bias conditions with V_{SB}=0V and f=1.2 GHz, for an LDMOS device with L=500 nm, W=40 μm and T_{OX}=15 nm. Markers stand for measurements (V_{DS}=0V: ○ and V_{DS}=30V: ◊), while lines are model simulations. The accurate value of the resistance is best extracted under negative gate bias and zero drain-to-source difference potential, as these conditions minimize the influence of the rest of the device. Here, the RG used for the model is 90Ω. The dotted line is for the simulation of the model minimizing the gate resistance.

potential. These results verify that this equation is valid for the HV-MOS devices as well.

4.2 Capacitances

Viewing the transistor as a two-port network, the imaginary parts of the Y-parameters hold information on the capacitances and the transcapacitances of the devices. This way, the following equation, which contains $\mathrm{Im}(Y_{11})$, can be used as an estimation of the capacitance seen from the gate node, meaning the total gate capacitance.

$$C_{GG} = \frac{\mathrm{Im}(Y_{11})}{2\pi f}. \quad (5)$$

In Figure 5, an estimation of the total gate capacitance is shown against the gate potential. The profile resembles to the classical MOSFET one, where the regions of operation of the device according to the gate potential are well separated, especially for the V_{DS} = 0V case. For the lowest values of the gate potential, the gate capacitance is maximized as the device works in accumulation. As the gate potential increases, the area below the thin oxide gets depleted and the device enters in depletion. Further increment of the gate potential leads to an inversion layer where the total gate capacitance reaches again its maximum value [38]. Under a positive V_{DS}, the device shows some clear deviation with respect to corresponding basic MOSFET device. Due to Miller effect, the total gate capacitance exceeds the maximum expected and exhibits a different shape [9].

The rest of the Y-parameters can be used in order to extract information on the extrinsic capacitances, see Figure 6. These can be obtained from the following relationships.

$$C_{GD} = \frac{\mathrm{Im}(Y_{12})}{2\pi f}, \quad (6)$$

$$C_{DG} = \frac{\mathrm{Im}(Y_{21})}{2\pi f}, \quad (7)$$

$$C_{DD} = \frac{\mathrm{Im}(Y_{22})}{2\pi f}. \quad (8)$$

Similarly, to the total gate capacitance, the $\mathrm{Im}(Y_{22})$ represents the capacitance of the device seen from the drain node. A major component of C_{DD} is the junction diode capacitance. On the other hand, one can see that at low and negative gate potentials, the estimations of C_{GD} and C_{DG} coincide. By inspection of the equivalent small-signal circuit, C_{DD} may be regarded as the sum of the extrinsic overlap capacitance between the gate and the drain ($C_{GD.OV}$) with the gate-to-drain capacitive load of the drift region. If this sum is substracted from C_{DD}, under the same bias conditions, the rest holds for the drain-to-substrate parasitic junction diode ($C_{J.DB}$) capacitance. Again, these parasitic elements are magnified for negative gate biases, where the channel does not influence the overall behavior of the device. Note that, under positive V_{DS}, the reciprocity between these two transcapacitances breaks down due to the saturation of the device from the drain side.

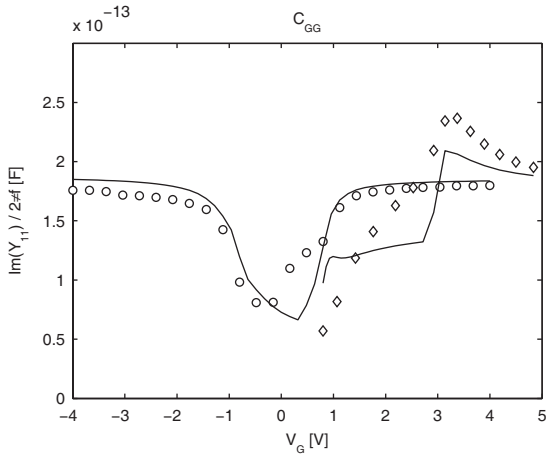

Figure 5; Total Gate Resistance (C_{GG}) as estimated by (5), under various bias conditions with V_{SB}=0V and f=1.2 GHz, for an LDMOS device with L=500 nm, W=40 μm, and T_{OX}=15 nm. Markers stand for measurements (V_{DS}=0V: ○ and V_{DS}=30V: ◊), while lines are model simulations.

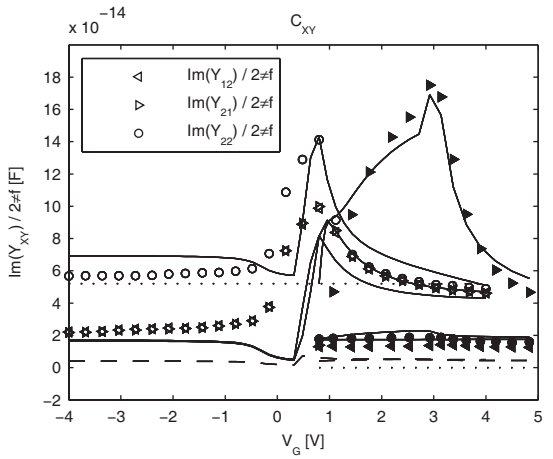

Figure 6: Various capacitances and transcapacitances as estimated by (6), (7), and (8), under various bias conditions with V_{SB}=0V and f=1.2 GHz, for an LDMOS device with L=500 nm, W=40 μm, and T_{OX}=15 nm. The non-filled markers stand for measurements with V_{DS}=0V and the filled markers for V_{DS}=30V, while the lines show the model simulation. The dotted lines represent the contribution of the junction diode capacitance to C_{DD}, while the dashed lines stand for the contribution of the extrinsic, gate-to-drain, overlap capacitance to C_{DD}.

Table 1: Analysis parameters

Parameter	Value	Description/Comments
T_{OX}	15 nm	Thickness of the gate oxide
W	40 µm	Drawn gate width of the device
L	500 nm	Nominal gate length of the device
$L_{eff.LV}$	1.2 µm	Effective gate length of the device[1]
$L_{OV.DK}$	120 nm	Effective overlap length of the drift region[1]
$V_{FB.DK}$	-350 mV	Flat-Band Voltage of the Drift Region[1]
R_G	90 Ω	Scalable gate resistance[2]
$C_{J.DB}$	50 fF	Scalable bias-depended junction diode capacitance[2,3]
$C_{GD.OV}$	3.5 fF	Scalable bias-depended overlap gate-to-drain extrinsic capacitance[2,3]
$C_{GD.DK}$	13.5 fF	Scalable bias-depended gate-to-drain drift region capacitance[2,3]

[1]Model fitting parameter. [2]Value for the specific geometry. [3]Value under zero bias conditions

Table 1 displays the related models parameters used for the above analyses.

5. CONCLUSION

Compact modeling of High-Voltage MOS devices is critical and merits a careful analysis at RF. In this work, we present an RF HV-MOS model along with its core equations that provides good results up to the GHz range of frequency. Further analysis of the dynamic behavior of the HV-MOS verifies the adequacy of the foundations of our RF model in terms of equivalent circuit built upon passive elements.

6. ACKNOWLEDGMENT

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