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(54) **FASTER CADZOW DENOISING BASED ON PARTIAL EIGENVALUE DECOMPOSITION**

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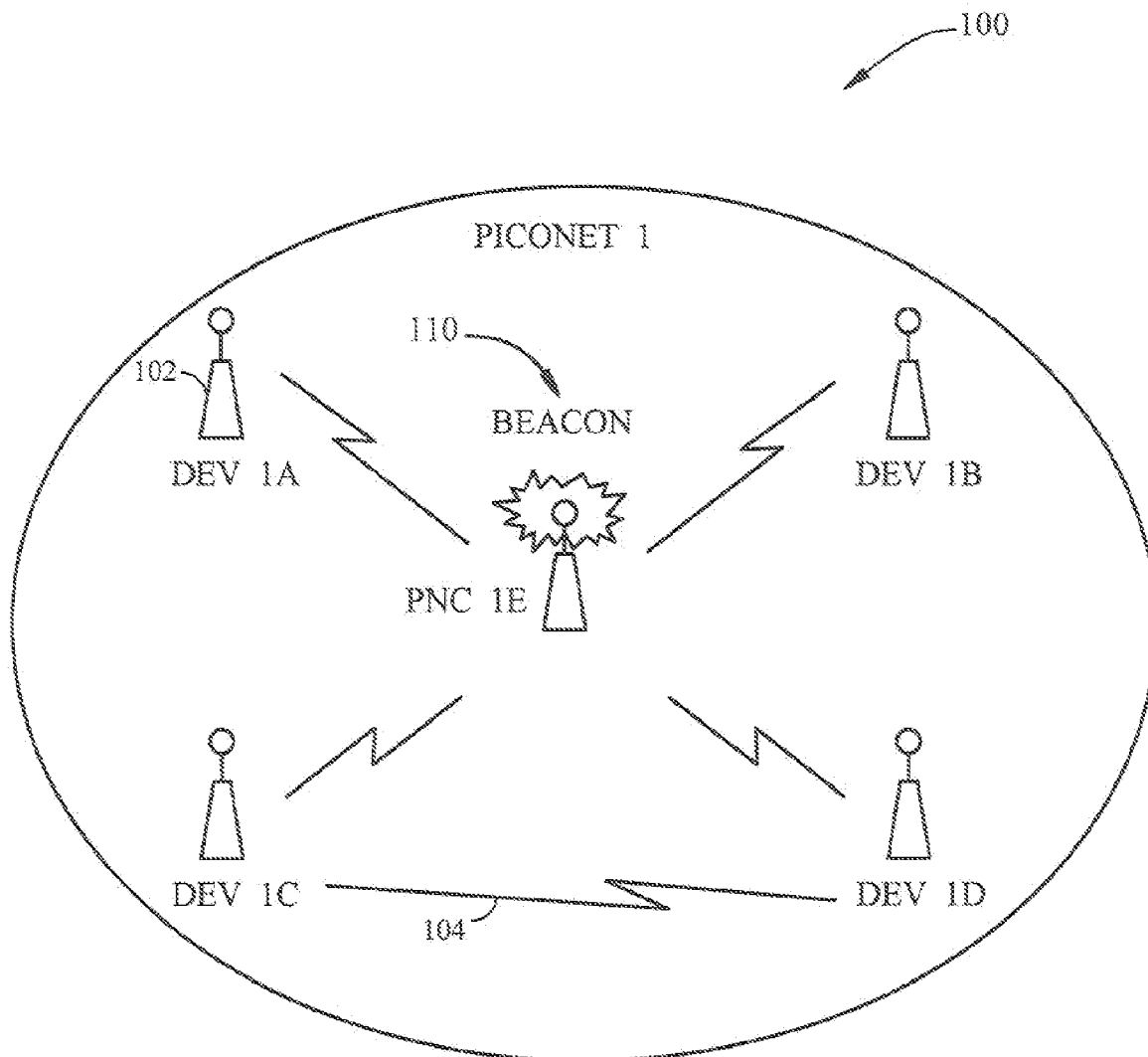
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(52) **U.S. Cl. 381/94.1; 375/238**
(57) **ABSTRACT**

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Certain aspects of the present disclosure relate to a method for speeding up the Cadzow iterative denoising algorithm as a part of the Finite Rate of Innovation (FRI) processing and for decreasing its computational complexity.



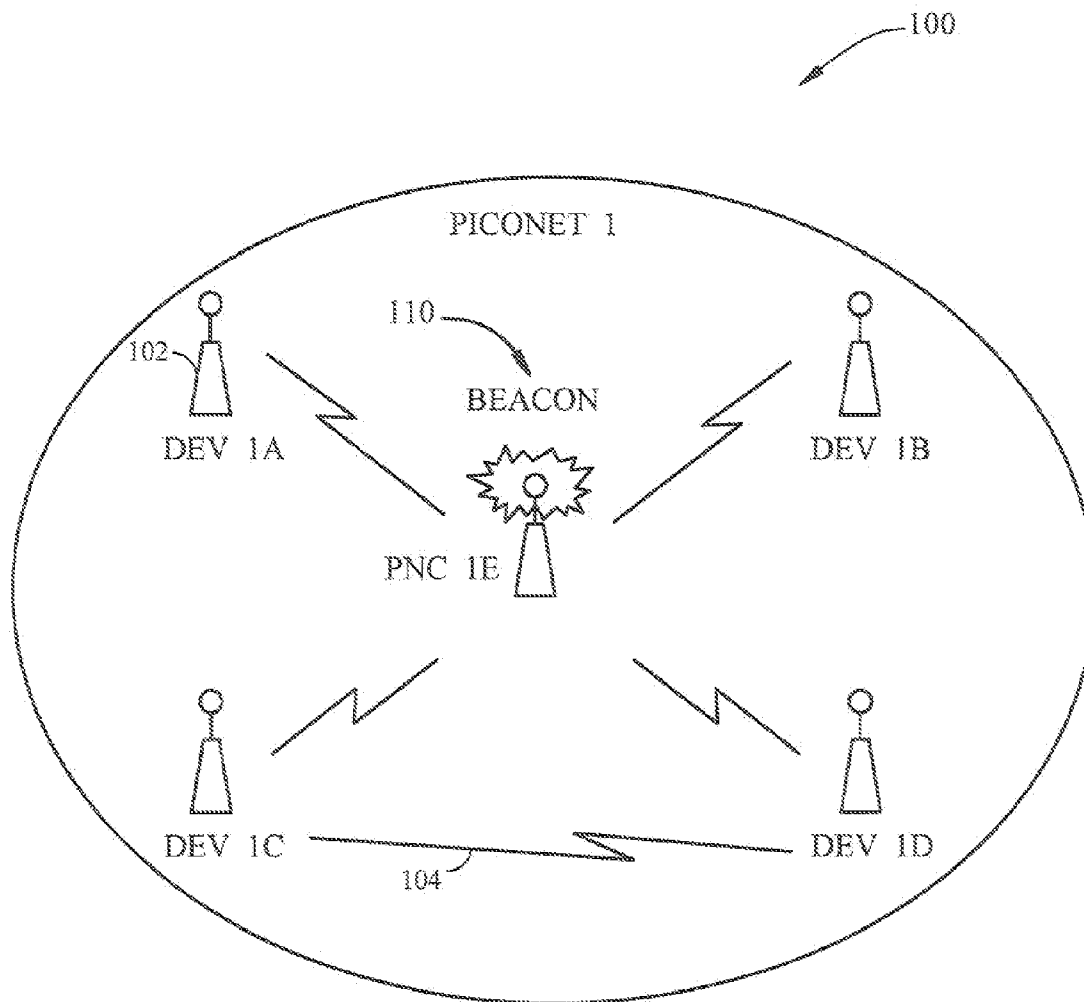


FIG. 1

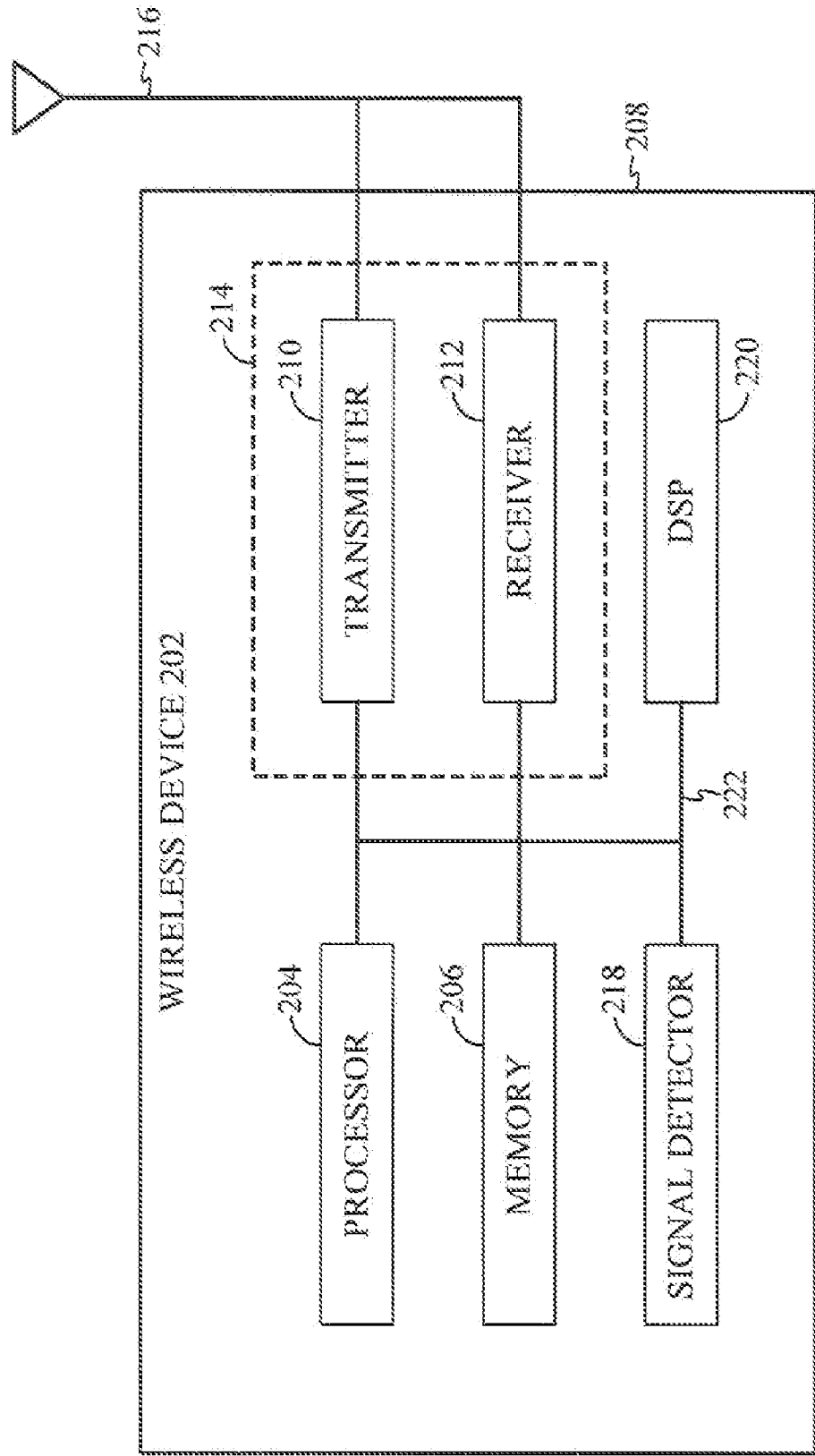


FIG. 2

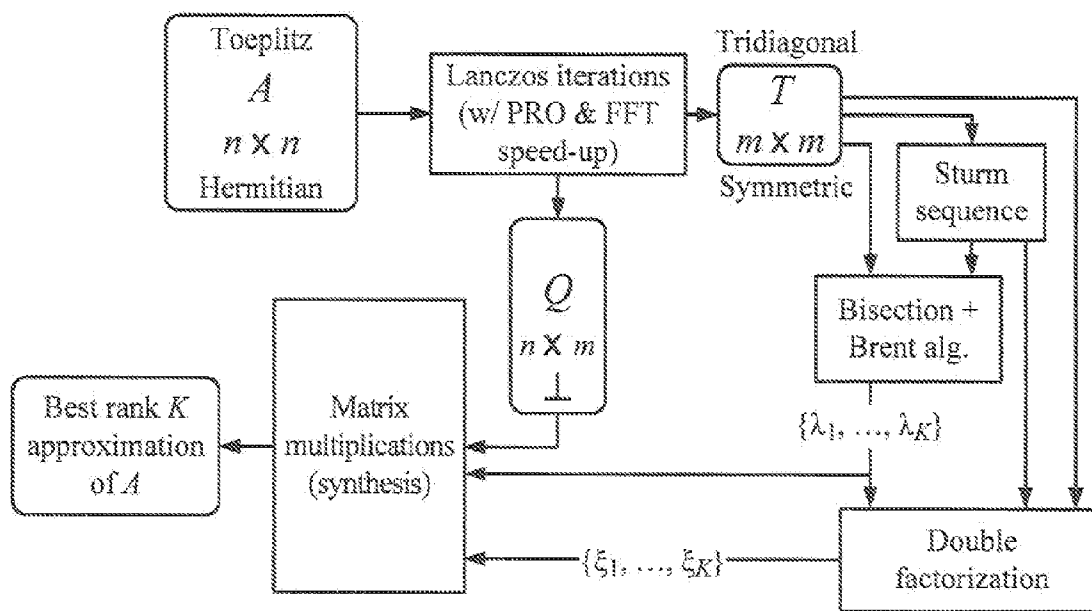
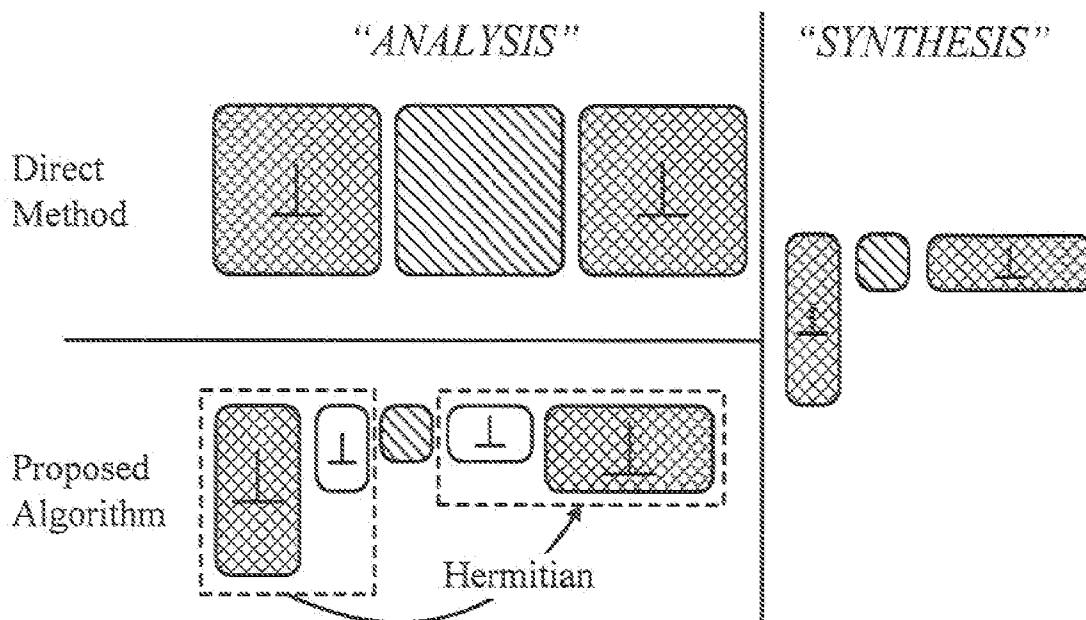


FIG. 3



Legend

- Real; hermitian/symmetric
- Real; diagonal
- Complex; hermitian/symmetric
- ⊥ Orthonormal

FIG. 4

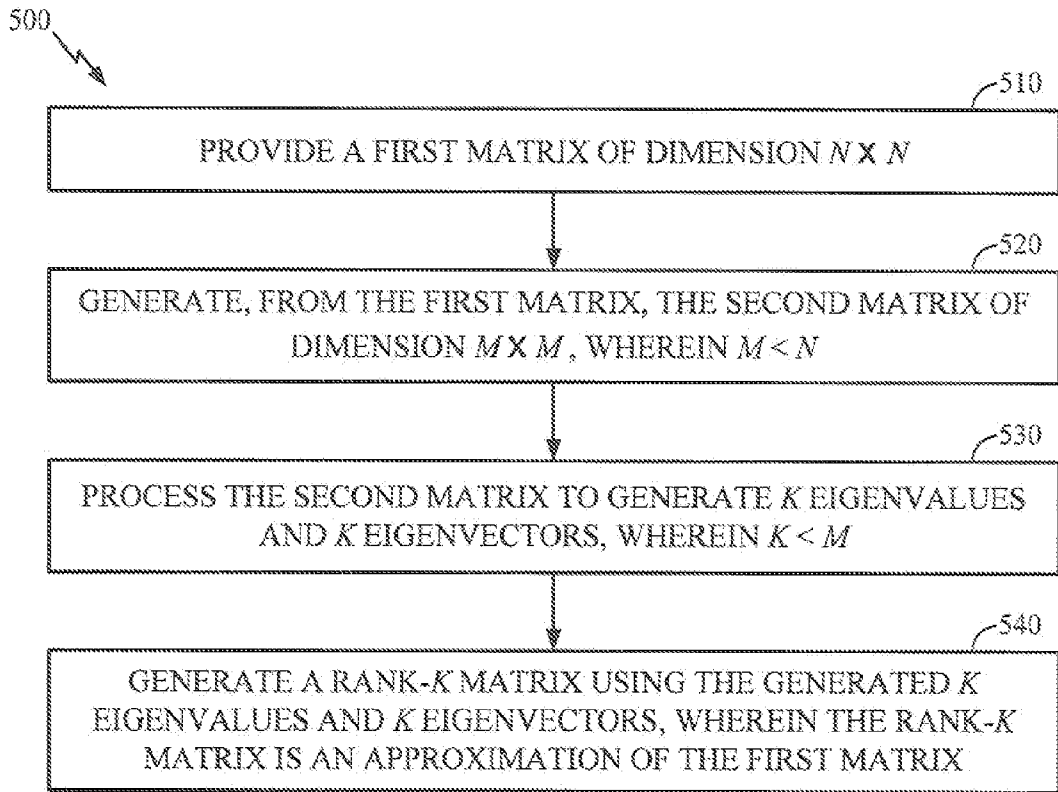


FIG. 5

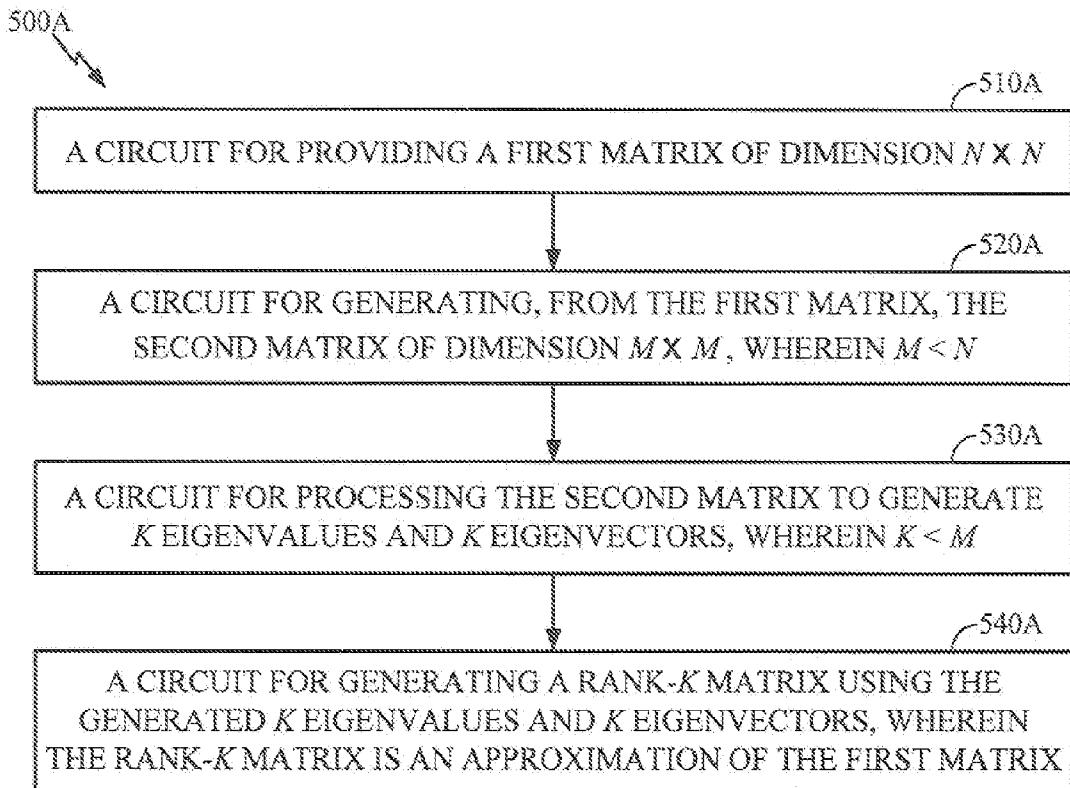


FIG. 5A

FASTER CADZOW DENOISING BASED ON PARTIAL EIGENVALUE DECOMPOSITION

CLAIM OF PRIORITY UNDER 35 U.S.C. §119

[0001] The present Application for Patent claims benefit of Provisional Application Ser. Nos. 61/161,348 filed Mar. 18, 2009 (Our Docket No.: 091638P1), 61/161,656 filed Mar. 19, 2009 (Our Docket No.: 091638P2), 61/224,808 filed Jul. 10, 2009 (Our Docket No.: 091638P3), and 61/247,115 filed Sep. 30, 2009 (Our Docket No.: 091637P1), and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

BACKGROUND

[0002] 1. Field

[0003] Certain aspects of the present disclosure generally relate to a wireless communication and, more particularly, to fast denoising of a received signal.

[0004] 2. Background

[0005] Ultra-Wideband (UWB) communications are radio communications that use a frequency bandwidth larger than 500 MHz. In comparison to narrow-band communications which rely on modulation of a carrier frequency, the large bandwidth of UWB communications allows sending signals with features well-localized in time. If a signal is more localized in time, then it is more spread in frequency. This allows communications based on pulses, while information can be encoded in a distance between pulses (i.e., a Pulse Position Modulation: PPM), in a pulse amplitude (i.e., a Pulse Amplitude Modulation: PAM) or in a pulse width (i.e., Pulse Width Modulation: PWM). One of the key advantages of pulse-based communication is ability to precisely localize time of arrival of the information (i.e., arrival of the pulse).

[0006] A signal at the UWB receiver is typically based on a pulse signal corrupted by stationary and non-stationary noise and by various channel effects, wherein the pulse signal can be different than a periodic sinc (i.e., Dirichlet kernel) shaped pulse signal. On the other hand, a parametric Finite Rate of Innovation (FRI) processing technique that can be applied after the UWB processing requires an input signal based on the periodic-sinc signal. Therefore, the received UWB pulse signal needs to be properly adjusted (i.e., equalized) before being processed by the FRI module. However, the equalized pulse signal at the input of the FRI module can still be corrupted by a prohibitively high level of noise.

[0007] The well-known Cadzow iterative algorithm can be used as an integral part of the FRI processing for denoising of the input signal of the FRI receiving module. The standard Cadzow algorithm provides, given a Toeplitz Hermitian square matrix of dimension $N \times N$ associated with the noisy signal, a Toeplitz Hermitian square matrix of the same dimension with rank K , where $K \ll N$. In order to achieve this low-rank approximation (i.e., signal de-noising), the standard Cadzow algorithm performs eigenvalue decomposition (EVD) of the Toeplitz Hermitian square matrix of dimension $N \times N$, and reconstructs the "best" rank K approximation by keeping only the K principal eigenvalues and eigenvectors. The reconstructed rank- K matrix is made Toeplitz by averaging its diagonals. This process is iterated until convergence. However, the standard iterative Cadzow algorithm is slow and computationally complex.

[0008] A method is proposed in the present disclosure to speed up the standard Cadzow denoising algorithm and to lower its computational complexity.

SUMMARY

[0009] Certain aspects provide a method for signal processing. The method generally includes providing a first matrix of dimension $N \times N$, generating, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$, processing the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$, and generating a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix.

[0010] Certain aspects provide an apparatus for signal processing. The apparatus generally includes a circuit configured to provide a first matrix of dimension $N \times N$, a first generator configured to generate, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$, a processor configured to process the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$, and a second generator configured to generate a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix.

[0011] Certain aspects provide an apparatus for signal processing. The apparatus generally includes means for providing a first matrix of dimension $N \times N$, means for generating, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$, means for processing the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$, and means for generating a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix.

[0012] Certain aspects provide a computer-program product for signal processing. The computer-program product includes a computer-readable medium comprising instructions executable to provide a first matrix of dimension $N \times N$, generate, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$, process the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$, and generate a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix.

[0013] Certain aspects provide a headset. The headset generally includes a receiver configured to receive a signal, a first circuit configured to provide a first matrix of dimension $N \times N$, a first generator configured to generate, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$, a processor configured to process the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$, a second generator configured to generate a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix, a second circuit configured to process the received signal based on the generated rank- K matrix, and a transducer configured to provide an audio output based on the processed signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] So that the manner in which the above-recited features of the present disclosure can be understood in detail, a more particular description, briefly summarized above, may be had by reference to aspects, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only certain typical aspects of

this disclosure and are therefore not to be considered limiting of its scope, for the description may admit to other equally effective aspects.

[0015] FIG. 1 illustrates an example wireless communication system in accordance with certain aspects of the present disclosure.

[0016] FIG. 2 illustrates various components that may be utilized in a wireless device in accordance with certain aspects of the present disclosure.

[0017] FIG. 3 illustrates an example block diagram of a partial eigenvalue decomposition (EVD) algorithm in accordance with certain aspects of the present disclosure.

[0018] FIG. 4 illustrates an overview of matrix computations involved in a low-rank approximation using the regular full EVD algorithm and the partial EVD algorithm in accordance with certain aspects of the present disclosure.

[0019] FIG. 5 illustrates example operations for performing the partial EVD in accordance with certain aspects of the present disclosure.

[0020] FIG. 5A illustrates example components capable of performing the operations illustrated in FIG. 5.

DETAILED DESCRIPTION

[0021] Various aspects of the disclosure are described more fully hereinafter with reference to the accompanying drawings. This disclosure may, however, be embodied in many different forms and should not be construed as limited to any specific structure or function presented throughout this disclosure. Rather, these aspects are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to those skilled in the art. Based on the teachings herein, one skilled in the art should appreciate that the scope of the disclosure is intended to cover any aspect of the disclosure disclosed herein, whether implemented independently of or combined with any other aspect of the disclosure. For example, an apparatus may be implemented or a method may be practiced using any number of the aspects set forth herein. In addition, the scope of the disclosure is intended to cover such an apparatus or method which is practiced using other structure, functionality, or structure and functionality in addition to or other than the various aspects of the disclosure set forth herein. It should be understood that any aspect of the disclosure disclosed herein may be embodied by one or more elements of a claim.

[0022] The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any aspect described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other aspects.

[0023] Although particular aspects are described herein, many variations and permutations of these aspects fall within the scope of the disclosure. Although some benefits and advantages of the preferred aspects are mentioned, the scope of the disclosure is not intended to be limited to particular benefits, uses or objectives. Rather, aspects of the disclosure are intended to be broadly applicable to different wireless technologies, system configurations, networks, and transmission protocols, some of which are illustrated by way of example in the figures and in the following description of the preferred aspects. The detailed description and drawings are

merely illustrative of the disclosure rather than limiting, the scope of the disclosure being defined by the appended claims and equivalents thereof.

An Example Wireless Communication System

[0024] The techniques described herein may be used for various broadband wireless communication systems, including communication systems that are based on a single carrier transmission. Aspects disclosed herein may be advantageous to systems employing Ultra-Wideband (UWB) signals including millimeter-wave signals. However, the present disclosure is not intended to be limited to such systems, as other coded signals may benefit from similar advantages.

[0025] The teachings herein may be incorporated into (e.g., implemented within or performed by) a variety of wired or wireless apparatuses (e.g., nodes). In some aspects, a node implemented in accordance with the teachings herein may comprise an access point or an access terminal.

[0026] An access terminal (“AT”) may comprise, be implemented as, or known as an access terminal, a subscriber station, a subscriber unit, a mobile station, a remote station, a remote terminal, a user terminal, a user agent, a user device, user equipment, or some other terminology. In some implementations an access terminal may comprise a cellular telephone, a cordless telephone, a Session Initiation Protocol (“SIP”) phone, a wireless local loop (“WLL”) station, a personal digital assistant (“PDA”), a handheld device having wireless connection capability, or some other suitable processing device connected to a wireless modem. Accordingly, one or more aspects taught herein may be incorporated into a phone (e.g., a cellular phone or smart phone), a computer (e.g., a laptop), a portable communication device, a portable computing device (e.g., a personal data assistant), an entertainment device (e.g., a music or video device, or a satellite radio), a global positioning system device, a headset, a sensor or any other suitable device that is configured to communicate via a wireless or wired medium. In some aspects the node is a wireless node. Such wireless node may provide, for example, connectivity for or to a network (e.g., a wide area network such as the Internet or a cellular network) via a wired or wireless communication link.

[0027] FIG. 1 illustrates an example of a wireless communication system 100 (i.e., a Piconet 1) in which aspects of the present disclosure may be employed. As illustrated, Piconet 1 may include a number of wireless devices 102 or “terminals” 1A-1E that can communicate with one another using relatively short-range wireless links 104. In the illustrated example, terminal 1E acts as a PNC for Piconet 1. Although illustrated with five devices, it should be appreciated that any number of devices (i.e., two or more) may form a wireless personal area network.

[0028] Each of the terminals 102 in the Piconet 1 may include, among other things, a wireless transceiver to support wireless communication and controller functionality to manage communication with the network. The controller functionality may be implemented within one or more digital processing devices. The wireless transceiver may be coupled to one or more antennas to facilitate the transmission of signals into and the reception of signals from a wireless channel. Any type of antennas may be used including, for example, dipoles, patches, helical antennas, antenna arrays, and/or others.

[0029] The devices in the Piconet 1 may include any of a wide variety of different device types including, for example,

laptop, desktop, palmtop, or tablet computers having wireless networking functionality, computer peripherals having wireless networking capability, personal digital assistants (PDAs) having wireless networking capability, cellular telephones and other handheld wireless communicators, pagers, wireless network interface modules (e.g., wireless network interface cards, etc.) incorporated into larger systems, multimedia devices having wireless networking capability, audio/visual devices having wireless networking capability, home appliances having wireless networking capability, jewelry or other wearable items having wireless networking capability, wireless universal serial bus (USB) devices, wireless digital imaging devices (e.g., digital cameras, camcorders, etc.), wireless printers, wireless home entertainment systems (e.g., DVD/CD players, televisions, MP3 players, audio devices, etc.), and/or others. In one configuration, for example, a wireless personal area network may include a user's laptop computer that is wirelessly communicating with the user's personal digital assistant (PDA) and the user's printer in a short-range network. In another possible configuration, a wireless personal area network may be formed between various audio/visual devices in, for example, a user's living room. In yet another configuration, a user's laptop computer may communicate with terminals associated with other users in a vicinity of the user. Many other scenarios are also possible.

[0030] Standards have been developed, and are currently in development, to provide a framework to support development of interoperable products that are capable of operating as part of a wireless personal area network (e.g., the Bluetooth standard (Specification of the Bluetooth System, Version 3.0, Bluetooth SIG, Inc., April 2009), the IEEE 802.15 standards, etc.). The IEEE 802.15.3c standard, for example, is a high data rate wireless personal area network standard. In accordance with the IEEE 802.15.3c standard, one of the terminals within a piconet is selected as a Piconet Coordinator (PNC) to coordinate the operation of the network. For example, with reference to FIG. 1, the device PNC 1E represents a PNC for the Piconet 1 in an IEEE 802.15.3c implementation.

[0031] As illustrated, PNC 1E may transmit a beacon signal 110 (or simply "beacon") to other devices of Piconet 1, which may help the other terminals within Piconet 1 synchronize their timing with PNC 1E. Thus, the beacon, typically sent at the beginning of every superframe, contains information that may be used to time-synchronize the terminals in the piconet. Each terminal in the piconet, including the PNC, may reset its superframe clock to zero at the beginning of the beacon preamble. If a terminal does not hear a beacon, it may reset its superframe clock to zero at the instant where it expected to hear the beginning of the beacon preamble (e.g., based on previous superframe timing).

[0032] In addition, terminals 102 can be communicating with one another in a peer-to-peer configuration. For example, the device DEV 1C may be in communication with the device DEV 1D using the link 104. In peer-to-peer ad hoc networks, devices (nodes) within range of each other, such as the devices DEV 1C and DEV 1D in the network 100, can communicate directly with each other without an access point, such as the PNC 1E, and/or a wired infrastructure to relay their communication. Additionally, peer devices or nodes can relay traffic. The devices 102 within the network 100 communicating in a peer-to-peer manner can function similar to base stations and relay traffic or communications to other devices, functioning similar to base stations, until the traffic reaches its ultimate destination. The devices can also

transmit control channels, which carry information that can be utilized to manage the data transmission between peer nodes.

[0033] The communication network 100 can include any number of devices or nodes that are in wireless (or wired) communication. Each node can be within range of one or more other nodes and can communicate with the other nodes or through utilization of the other nodes, such as in a multi-hop topography (e.g., communications can hop from node to node until reaching a final destination). For example, a sender node may wish to communicate with a receiver node. To enable packet transfer between sender node and receiver node, one or more intermediate nodes can be utilized. It should be understood that any node can be a sender node and/or a receiver node and can perform functions of either sending and/or receiving information at substantially the same time (e.g., can broadcast or communicate information at about the same time as receiving information) or at different times.

[0034] FIG. 2 illustrates various components that may be utilized in a wireless device 202 that may be employed within the wireless communication system 100. The wireless device 202 is an example of a device that may be configured to implement the various methods described herein. The wireless device 202 may be the PNC 1E or a terminal 102 in the Piconet 1.

[0035] The wireless device 202 may include a processor 204 which controls operation of the wireless device 202. The processor 204 may also be referred to as a central processing unit (CPU). Memory 206, which may include both read-only memory (ROM) and random access memory (RAM), provides instructions and data to the processor 204. A portion of the memory 206 may also include non-volatile random access memory (NVRAM). The processor 204 typically performs logical and arithmetic operations based on program instructions stored within the memory 206. The instructions in the memory 206 may be executable to implement the methods described herein.

[0036] The wireless device 202 may also include a housing 208 that may include a transmitter 210 and a receiver 212 to allow transmission and reception of data between the wireless device 202 and a remote location. The transmitter 210 and receiver 212 may be combined into a transceiver 214. An antenna 216 may be attached to the housing 208 and electrically coupled to the transceiver 214. The wireless device 202 may also include (not shown) multiple transmitters, multiple receivers, multiple transceivers, and/or multiple antennas.

[0037] The wireless device 202 may also include a signal detector 218 that may be used in an effort to detect and quantify the level of signals received by the transceiver 214. The signal detector 218 may detect such signals as total energy, energy per subcarrier per symbol, power spectral density and other signals. The wireless device 202 may also include a digital signal processor (DSP) 220 for use in processing signals.

[0038] The various components of the wireless device 202 may be coupled together by a bus system 222, which may include a power bus, a control signal bus, and a status signal bus in addition to a data bus.

[0039] Ultra-Wideband (UWB) communications performed by the wireless system 100 comprise radio communications that use a frequency bandwidth larger than 500 MHz. In comparison to narrow-band communications which rely on modulation of a carrier frequency, the large bandwidth

of UWB communications allows sending signals with features well-localized in time. If a signal is more localized in time, then it is more spread in frequency. This allows communications based on pulses, while information can be encoded in a distance between pulses (i.e., a Pulse Position Modulation: PPM), in a pulse amplitude (i.e., a Pulse Amplitude Modulation: PAM) or in a pulse width (i.e., Pulse Width Modulation: PWM). One of the key advantages of pulse-based communication is ability to precisely localize time of arrival of the information (i.e., arrival of the pulse).

[0040] Finite Rate of Innovation (FRI) is a parametric processing approach that may be applied on signals received by a typical Ultra-Wideband (UWB) device, such as the device **202**. The FRI processing may require an input signal based on the periodic-sinc function, while the received UWB signal is based on different types of pulses. Because of that, the received UWB signal may need to be properly adjusted (i.e., equalized) before being input into an FRI module. However, the equalized pulse signal at the input of the FRI module can still be corrupted by a prohibitively high level of noise.

Fast Cadzow Denoising Algorithm

[0041] The Cadzow iterative algorithm can be utilized as a part of the FRI processing for denoising of the input signal. In the Cadzow denoising procedure, the discrete Fourier transform (DFT) coefficients of N input samples may be arranged in a Toeplitz Hermitian square matrix of dimension $N \times N$. If the original signal (i.e., the signal without noise) comprises K distinct samples, where $K \ll N$, the Toeplitz Hermitian square matrix may be eventually of rank K . Therefore, each denoising iteration may consist of finding a preferred low-rank approximation of the original Toeplitz Hermitian square matrix, i.e., given the Toeplitz Hermitian square matrix of dimension $N \times N$, a Toeplitz Hermitian square matrix of the same dimension with rank K may be obtained.

[0042] The standard Cadzow algorithm performs eigenvalue decomposition (EVD) of the Toeplitz Hermitian square matrix of dimension $N \times N$, and reconstructs the preferred rank- K approximation by keeping only the K principal eigenvalues and eigenvectors. The reconstructed rank- K matrix is made Toeplitz by averaging its diagonals. This process can be iterated until convergence. However, the standard Cadzow iterative algorithm can be slow and computationally complex. Certain aspects of the present disclosure support speeding up the Cadzow denoising algorithm and reducing its computational complexity.

[0043] It can be observed that the Cadzow algorithm requires a relatively small number of eigenpairs (i.e., eigenvalues and eigenvectors). Therefore, instead of applying the full EVD algorithm, the signal matrix may be denoised based on a partial EVD approach. At each iteration, the signal matrix to be denoised may be projected into a Krylov subspace of a smaller dimension, which saves computations. Then, a particular structure of the projected signal may be used to extract only relevant eigenpairs, which saves additional computations.

[0044] FIG. 3 illustrates an example block diagram of the proposed partial EVD algorithm in accordance with certain aspects of the present disclosure. FIG. 4 illustrates an overview of matrix computations involved in the low-rank approximation using the regular full EVD algorithm and the proposed partial EVD algorithm. It can be observed from FIG. 4 that the computational complexity of the proposed

partial EVD approach may be substantially reduced compared to the conventional full EVD algorithm.

[0045] FIG. 5 illustrates example operations **500** for performing the proposed partial EVD algorithm in accordance with certain aspects of the present disclosure. The DFT coefficients of the noisy signal may be arranged in a first matrix of dimension $N \times N$. At **510**, the first matrix of dimension $N \times N$ may be provided for processing. The first matrix may be a Toeplitz Hermitian matrix, as illustrated in FIG. 3. At **520**, a second matrix of dimension $M \times M$ may be generated from the first matrix, wherein $M < N$. As illustrated in FIG. 3, the generation of the second matrix may be based on an iterative partial Lanczos tridiagonalization that may also produce a unitary matrix of dimension $N \times M$ which spans an M -dimensional Krylov subspace of the first matrix. The generated second matrix may be a real, symmetric and tridiagonal matrix, and may represent a projection of the first matrix in the M -dimensional Krylov subspace. This particular structure of the second matrix may simplify following computations.

[0046] It should be noted that the partial Lanczos tridiagonalization procedure may be numerically unstable, i.e., orthogonality between basis vectors may be lost after a few iterations. The most conservative treatment is to orthogonalize each new basis vector against already obtained ones. This approach is known in the art as the full orthogonalization (or the Gram-Schmidt procedure). As illustrated in FIG. 3, it is proposed in the present disclosure to employ a faster and less complex partial re-orthogonalization (PRO) approach. The PRO estimates the loss of orthogonality at each iteration and re-orthogonalize the new basis vector against the ones with an inner-product crossing a defined threshold and their adjacent basis vectors. Another approach that simplifies the full orthogonalization is known in the art as the selective orthogonalization (SO). In the preferred aspect of the present disclosure, the PRO is chosen over the SO for its relative simplicity, while being sufficiently effective against the loss of orthogonality during the iterative Lanczos procedure. In other aspects of the present disclosure, the Gram-Schmidt procedure or the SO may be employed instead of the PRO.

[0047] Referring back to FIG. 5, at **530**, the generated second matrix of dimension $M \times M$ may be processed in order to obtain K eigenvalues $\{\lambda_1, \dots, \lambda_K\}$ and K eigenvectors $\{\xi_1, \dots, \xi_K\}$, wherein $K < M$. The generated K eigenvectors may be related to K principal eigenvectors of the first matrix, and may represent the projection of the eigenvectors of the first matrix in the Krylov subspace. As illustrated in FIG. 3, the generated second matrix of dimension $M \times M$ may be processed by utilizing the bisection search algorithm and the fast rooting Brent algorithm to generate K eigenvalues $\{\lambda_1, \dots, \lambda_K\}$. Recovery of the eigenvectors $\{\xi_1, \dots, \xi_K\}$ may be performed in a fast and stable manner by using a Fernando's double factorization applied on the second matrix, while also utilizing the eigenvalues $\{\lambda_1, \dots, \lambda_K\}$.

[0048] At **540**, a rank- K matrix may be obtained, as illustrated in FIG. 3, using the previously generated K eigenvalues, the K eigenvectors and the unitary matrix, wherein the rank- K matrix may represent a lower-rank approximation of the first matrix. This low-rank approximation is possible because the principal eigenpairs of the first matrix of dimension $N \times N$ may belong to the M -dimensional Krylov subspace, wherein $M < N$.

[0049] The value of M (i.e., the size of Krylov subspace) may be determined as follows. In one aspect of the present disclosure, the K^{th} eigenvalue may be monitored at each itera-

tion of the Lanczos tridiagonalization procedure. Once this particular eigenvalue is converged (i.e., stopped moving), it is likely that the K principal eigenpairs of the subspace projection may be mapped to the original K principal eigenpairs by using an inverse projection. Then, the value of M may correspond to the number of iterations of the Lanczos procedure. In another aspect of the present disclosure, the value of M may be set beforehand, and then it may be required to empirically confirm that an obtained K^{th} eigenvalue has converged for this particular M .

[0050] The various operations of methods described above may be performed by any suitable means capable of performing the corresponding functions. The means may include various hardware and/or software component(s) and/or module(s), including, but not limited to a circuit, an application specific integrate circuit (ASIC), or processor. Generally, where there are operations illustrated in Figures, those operations may have corresponding counterpart means-plus-function components with similar numbering. For example, blocks 510-540 illustrated in FIG. 5 correspond to circuit blocks 510A-540A illustrated in FIG. 5A.

[0051] As used herein, the term “determining” encompasses a wide variety of actions. For example, “determining” may include calculating, computing, processing, deriving, investigating, looking up (e.g., looking up in a table, a database or another data structure), ascertaining and the like. Also, “determining” may include receiving (e.g., receiving information), accessing (e.g., accessing data in a memory) and the like. Also, “determining” may include resolving, selecting, choosing, establishing and the like.

[0052] As used herein, a phrase referring to “at least one of” a list of items refers to any combination of those items, including single members. As an example, “at least one of: a, b, or c” is intended to cover: a, b, c, a-b, a-c, b-c, and a-b-c.

[0053] The various operations of methods described above may be performed by any suitable means capable of performing the operations, such as various hardware and/or software component(s), circuits, and/or module(s). Generally, any operations illustrated in the Figures may be performed by corresponding functional means capable of performing the operations.

[0054] The various illustrative logical blocks, modules and circuits described in connection with the present disclosure may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array signal (FPGA) or other programmable logic device (PLD), discrete gate or transistor logic, discrete hardware components or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any commercially available processor, controller, microcontroller or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0055] The steps of a method or algorithm described in connection with the present disclosure may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in any form of storage medium that is known in the art. Some examples of storage media that may be used include random access memory (RAM), read only memory (ROM),

flash memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM and so forth. A software module may comprise a single instruction, or many instructions, and may be distributed over several different code segments, among different programs, and across multiple storage media. A storage medium may be coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor.

[0056] The methods disclosed herein comprise one or more steps or actions for achieving the described method. The method steps and/or actions may be interchanged with one another without departing from the scope of the claims. In other words, unless a specific order of steps or actions is specified, the order and/or use of specific steps and/or actions may be modified without departing from the scope of the claims.

[0057] The functions described may be implemented in hardware, software, firmware or any combination thereof. If implemented in software, the functions may be stored as one or more instructions on a computer-readable medium. A storage media may be any available media that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Disk and disc, as used herein, include compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-rays® disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers.

[0058] Thus, certain aspects may comprise a computer program product for performing the operations presented herein. For example, such a computer program product may comprise a computer readable medium having instructions stored (and/or encoded) thereon, the instructions being executable by one or more processors to perform the operations described herein. For certain aspects, the computer program product may include packaging material.

[0059] Software or instructions may also be transmitted over a transmission medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of transmission medium.

[0060] Further, it should be appreciated that modules and/or other appropriate means for performing the methods and techniques described herein can be downloaded and/or otherwise obtained by a user terminal and/or base station as applicable. For example, such a device can be coupled to a server to facilitate the transfer of means for performing the methods described herein. Alternatively, various methods described herein can be provided via storage means (e.g., RAM, ROM, a physical storage medium such as a compact disc (CD) or floppy disk, etc.), such that a user terminal and/or base station can obtain the various methods upon coupling or providing the storage means to the device. Moreover, any

other suitable technique for providing the methods and techniques described herein to a device can be utilized.

[0061] It is to be understood that the claims are not limited to the precise configuration and components illustrated above. Various modifications, changes and variations may be made in the arrangement, operation and details of the methods and apparatus described above without departing from the scope of the claims.

[0062] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

1. A method for signal processing, comprising:
 - providing a first matrix of dimension $N \times N$;
 - generating, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$;
 - processing the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$; and
 - generating a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix.
2. The method of claim 1, wherein the generated K eigenvectors comprise rotated version of K principal eigenvectors of the first matrix.
3. The method of claim 1, wherein generating the second matrix comprises performing a Lanczos iterative transformation of the first matrix.
4. The method of claim 3, wherein the Lanczos iterative transformation of the first matrix produces a unitary matrix of dimension $N \times M$.
5. The method of claim 4, wherein generating the rank- K matrix further comprises utilizing the unitary matrix.
6. The method of claim 1, wherein processing the second matrix comprises:
 - performing a bisection search algorithm and a fast rooting Brent algorithm to generate the K eigenvalues.
7. The method of claim 6, further comprising:
 - performing a Fernando's double factorization algorithm utilizing the K eigenvalues generated by the bisection search algorithm and by the fast rooting Brent algorithm to obtain the K eigenvectors.
8. The method of claim 1, wherein the second matrix comprises a tridiagonal real symmetric matrix.
9. An apparatus for signal processing, comprising:
 - a circuit configured to provide a first matrix of dimension $N \times N$;
 - a first generator configured to generate, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$;
 - a processor configured to process the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$; and
 - a second generator configured to generate a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix.
10. The apparatus of claim 9, wherein the generated K eigenvectors comprise rotated version of K principal eigenvectors of the first matrix.
11. The apparatus of claim 9, wherein the first generator configured to generate the second matrix comprises a circuit configured to perform a Lanczos iterative transformation of the first matrix.

12. The apparatus of claim 11, wherein the Lanczos iterative transformation of the first matrix produces a unitary matrix of dimension $N \times M$.

13. The apparatus of claim 12, wherein the second generator configured to generate the rank- K matrix comprises a circuit configured to utilize the unitary matrix.

14. The apparatus of claim 9, wherein the processor configured to process the second matrix comprises:

- a first circuit configured to perform a bisection search algorithm and a fast rooting Brent algorithm to generate the K eigenvalues.

- 15. The apparatus of claim 14, further comprising:
 - a second circuit configured to perform a Fernando's double factorization algorithm utilizing the K eigenvalues generated by the bisection search algorithm and by the fast rooting Brent algorithm to obtain the K eigenvectors.

16. The apparatus of claim 9, wherein the second matrix comprises a tridiagonal real symmetric matrix.

- 17. An apparatus for signal processing, comprising:
 - means for providing a first matrix of dimension $N \times N$;
 - means for generating, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$;
 - means for processing the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$; and
 - means for generating a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix.

18. The apparatus of claim 17, wherein the generated K eigenvectors comprise rotated version of K principal eigenvectors of the first matrix.

19. The apparatus of claim 17, wherein the means for generating the second matrix comprises means for performing a Lanczos iterative transformation of the first matrix.

20. The apparatus of claim 19, wherein the Lanczos iterative transformation of the first matrix produces a unitary matrix of dimension $N \times M$.

21. The apparatus of claim 20, wherein the means for generating the rank- K matrix further comprises means for utilizing the unitary matrix.

22. The apparatus of claim 17, wherein the means for processing the second matrix comprises:

- means for performing a bisection search algorithm and a fast rooting Brent algorithm to generate the K eigenvalues.

- 23. The apparatus of claim 22, further comprising:
 - means for performing a Fernando's double factorization algorithm utilizing the K eigenvalues generated by the bisection search algorithm and by the fast rooting Brent algorithm to obtain the K eigenvectors.

24. The apparatus of claim 17, wherein the second matrix comprises a tridiagonal real symmetric matrix.

25. A computer-program product for signal processing, comprising a computer-readable medium comprising instructions executable to:

- provide a first matrix of dimension $N \times N$;
- generate, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$;
- process the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$; and
- generate a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix.

26. A headset, comprising:
a receiver configured to receive a signal;
a first circuit configured to provide a first matrix of dimension $N \times N$;
a first generator configured to generate, from the first matrix, a second matrix of dimension $M \times M$, wherein $M < N$;
a processor configured to process the second matrix to generate K eigenvalues and K eigenvectors, wherein $K < M$;

a second generator configured to generate a rank- K matrix using the generated K eigenvalues and K eigenvectors, said rank- K matrix being an approximation of the first matrix;
a second circuit configured to process the received signal based on the generated rank- K matrix; and
a transducer configured to provide an audio output based on the processed signal.

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