Vertically-stacked gate-all-around polysilicon nanowire FETs with sub-μm gates patterned by nanostencil lithography

Davide Sacchetto*, Shenqi Xie, Veronica Savu, Michael Zervas, Giovanni De Micheli, Jürgen Brugger, Yusuf Leblebici

Ecole Polytechnique Fédérale de Lausanne, Switzerland

Abstract

We report on the top-down fabrication of vertically-stacked polysilicon nanowire (NW) gate-all-around (GAA) field-effect-transistors (FET) by means of Inductively Coupled Plasma (ICP) etching and nanostencil lithography. The nanostencil is used to form sub-μm GAA gates over polysilicon NW array channels with high aspect ratio, considerably simplifying the lithographic steps above regions with deep 3D topography and non-planar surface features. This process lead to fabrication yields larger than 70% and authors envisage even larger yields of ≥ 85% with optimized mask design. Electrical measurements confirm the results obtained from similar devices fabricated with a standard lithography method while achieving higher density, larger reproducibility and yield, maintaining the performance improvement related with scaling.

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1. Introduction

Future technological innovations enabling ever higher circuit densities predicted by Moore’s law will most likely be concentrated on novel materials, innovative device structures, and significant modifications of the planar transistor design [1,2]. Considering novel device structures, multiple-gated transistors have been proved of better electrostatic control and larger drive current with respect to the traditional planar transistor design [3]. These features are particularly attractive as enablers for further device scaling. In fact, double-gate and finFET structures are the first non-planar 3D gate constructions being successfully employed into commercial products. Nowadays, growing research efforts are spent with gate-all-around constructions with sub-10 nm diameter nanowire (NW) channels. Nevertheless, as the dimensions reduce and 3D structures are introduced, major difficulties arises due to the need of scaling while keeping large fabrication yields.

We report on a fully CMOS-compatible top-down fabrication flow of polysilicon channel finFETs and vertically-stacked polysilicon NW gate-all-around (GAA) FETs by means of an optimized Bosch process [4] and nanostencil lithography [5]. In a previous work, the authors envisaged stencil lithography [6] as a key enabler for gate patterning on 3D structures, such as vertically-stacked Si NW transistors [4]. In this work, nanostencil lithography is used to deposit the Al mask used to pattern sub-μm GAA polysilicon gates deposited with LPCVD as alternative solution for patterning nanoscaled features having high aspect ratio, which is a non trivial issue in photo-resist lithography. Moreover, a simple method to form vertically-stacked Si NWs on bulk-Si substrates [7] has been adapted to form vertically-stacked NWs onto polycrystalline Si substrates. Preliminary electrical characterizations performed before the metal contact formation demonstrate functional memristive FET operation and confirming the behavior of previously reported devices fabricated with standard processing technology and μm-scale gate lengths [8]. The finFETs and the vertically-stacked polysilicon NW GAA devices are fabricated with yields larger than 70%, demonstrating a promising new method for 3D transistor fabrication with sub-μm nanostencil lithography.

In Section 2.1 we describe the structure of both finFETs and vertically-stacked GAA SiNW FETs. Then in Section 2.2 the fabrication flow for the devices is explained in detail, whereas the fabricated structures and discussion on the nano-fabrication results are provided in Section 3. Hence, the electrical measurement results are reported Section 4, with discussion among the difference in performance achieved by finFETs and vertically-stacked polysilicon NW GAA FETs. Finally, in Section 5 we draw the conclusions.

2. Device Fabrication

2.1. Device Description

The devices built can be grouped into two categories: finFETs and vertically-stacked SiNW FETs. In the first case, FETs or inverters having either 1 to 11 fins channels and tri-gate construction are built (in Fig. 1(a), a finFET with 3 fins is depicted). In the second

* Corresponding author.
E-mail address: davide.sacchetto@epfl.ch (D. Sacchetto).

0167-9317/$ - see front matter © 2012 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.mee.2012.07.048
case, FETs or inverters with 1 to 11 parallel strands consisting of 3 vertically-stacked SiNWs and GAA construction are built (in Fig. 1(b), a 3 times 3 SiNW matrix with GAA construction is shown). Apart from the fabrication of non-planar channels in such devices, the lithography definition of tri-gate or all-around gate structures above 3D channel regions is considered to be a significant challenge [1].

2.2. Process Flow

The fabrication starts with the substrate preparation for the two separate wafer batches. Bulk-Si wafers are oxidized in wet atmosphere to form 500 nm thermal oxide. Then either 50 nm or 350 nm thick LPCVD polysilicon is deposited as the device layer to build finFETs or vertically-stacked SiNW FETs, respectively. Individual or arrays of lines of widths of 50 nm and length of 8 µm are patterned with diluted hydrogen silsesquioxane (HSQ) using e-beam lithography (EBL) (see Fig. 2(a)). The HSQ is then used as hard mask for the fins and the vertically-stacked SiNWs etching (Fig. 2(b)). For the fin formation, a Cl2 based plasma etching is used to obtain vertical sidewalls, whereas for the vertically-stacked SiNWs the etching consists of 3 cycles of passivation and etching steps, alternating low frequency pulses of CF4 and SF6 plasmas. The etching technique used for the stacked SiNW formation has been calibrated from the recipes previously described by the authors for the formation of vertically-stacked SiNWs in crystalline Si substrates [7]. Next, a 10 nm dry oxidation followed by a 100 nm LPCVD polysilicon deposition form the gate stack (see Fig. 2(c)). At the same time a low stress SiN nanostencil mask has been patterned with the gate design. The fabrication details of the nanostencil are described by the authors in a different publication [5]. In this work, the nanostencil is made of 100 nm thick LPCVD low stress SiN. The gate and contact pads are defined by EBL, followed by consecutive etching steps to open the apertures and back side windows. Then the nanostencil mask is aligned with a dedicated optical alignment tool and mechanically clamped with the device substrates. After loading the substrates with the nanostencil into a commercial e-beam evaporator, 40 nm Al are deposited, leaving an Al hard mask reproducing the gate design on top of the polysilicon sidewalls (Fig. 2(d)). The Al mask gives better selectivity than SiO2 hard masks for dry Si etching, thus enabling the patterning of higher aspect ratio structures. Hence, polysilicon gates are etched and SiN spacers are formed to provide good isolation barrier between the gate and the source/drain regions (Fig. 2(e)). This step is thus used to form pad areas for electrical characterization as well as polysilicon gates with lengths between 100 nm and 500 nm. Finally, a 30 nm thick Ni layer is deposited on the substrates, and a thermal annealing process at 400 C is utilized to form a stoichiometric 1:1 NiSi phase (Fig. 2(f)). After Ni blanket deposition and a thermal annealing at 400 C, a Piranha wet etching is used to remove unreacted Ni from either BOX and spacer regions, thus forming self-aligned SiN source/drain and gate areas.

Thanks to the self-alignment of the SiN spacers with the gates, self-aligned source/drain regions are formed and the devices are ready for electrical characterization.

3. Fabricated Devices

The fabricated devices included FETs or inverters designed with different number of channels, having either 1 to 11 parallel SiNWs for the finFETs. For the vertically-stacked SiNWs the same design is used, nevertheless, thanks to stacking 3 levels, the same devices have 3 to 33 parallel SiNW channels. Another difference among finFETs and vertically-stacked FETs is notably the gate structure, which are tri-gates and GAA, respectively. In Fig. 3, a finFET with 11 parallel SiNWs and tri-gate construction is shown. The SiNWs are interconnected every 500nm in order to improve the mechanical stiffness and so to avoid bending. In Fig. 4, a vertically-stacked FET with 3 stacked SiNWs of 30 nm diameter and GAA construction is shown. In the inset, conformal coverage of 10nm thick SiO2 dielectric and LPCVD polysilicon gate is shown.

In all substrates, the design included 150 FETs and 150 inverters, for which the fabrication yield has been checked. In Table 1 fabrication yields larger than 70% are reported, showing excellent reproducibility, considering the experimental nature of the
Moreover, the failing sites have been observed the same for all the substrates, regardless of the process flow. This is the reason for the very similar yield reported for finFETs and vertically-stacked FETs. It is worth noticing that failing devices are mainly related with defects in the mask design, and that this aspect of the work has not been optimized. Thus, the main limitation on the fabrication yield is related with systematic errors in the design.

For instance, one of the major fabrication issues is the mechanical stability of the nanostencil, whose robustness is crucial for the correct patterning of the Al mask. If we consider the device subset of finFET inverters, the the larger yield of 85% is mainly attributed to the lower number of defective nanostencil patterns. Using a smaller size for the nanostencil, which would be a natural consequence when fabricating more scaled devices, improves stability and, at the same time, reduces the frequency of defective patterns. Hence, there is indication that fabrication yields larger than 85% with this process flow is possible with relatively little effort in the mask design.

4. Electrical Measurements

Electrical characterization is carried out with a manual probe station connected to a Agilent B1500 semiconductor parameter

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branches up to 300 mV/dec.

Ambipolarity with inverse subthreshold slopes for n- and p-

tightly-stacked FETs with 3 stacked SiNWs show typical device

efficiency of the 3D mesh with respect to the single

curves (see Fig. 7). The hysteresis reflects the fact that the Ids

Tungsten tips are put in contact with the polysilicon

Another interesting result is the hysteresis observed for Ids

these results are then

The hysteresis lead to different saturation threshold due to

dynamics of charges with interface states at either the Shortky junctions or at

as shown in Table 1.

vertical subthreshold slopes of about 1500 mV/dec and average

Inverter operation obtained by biasing a FET with constant current. The

Vout − Vin characteristics switched from high to low Vout at Vin ≈ 1 V.

amplifier. Tungsten tips are put in contact with the polysilicon

Fig. 7. $I_{ds} − V_{gs}$ memristive/hysteresis curve for vertically-stacked SiNW GAA FET with 3 stacked channels. The hysteresis lead to different saturation threshold due to the dynamics of charges with interface states at either the Shortky junctions or at the polysilicon grain boundaries.

curve for forward $V_{ds}$ sweep is not identical to the same curve for

backward $V_{ds}$ sweep. This behavior can be attributed to the presen-
tice of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [9]. More detailed explanation of the memristive electrical behavior can be found for simi-
lar, previously reported devices [8].

Fig. 8. Inverter operation obtained by biasing a FET with constant current. The

5. Conclusions

In conclusion, we demonstrated for the first time vertically-

stacked Si nanowire FETs with polysilicon GAA having gate lengths
down to 100 nm and yield larger than 70%. Moreover, the reported

ambipolar behavior for vertically-stacked FETs achieves $I_{on}/I_{off}$ ratio up to 4 orders of magnitude and inverse subthreshold slopes (SS) up to 300 mV/dec, effectively improving the SS of 1500 mV/dec obtained for finFETs. The method provide excellent step coverage on either finFETs and vertically-stacked SiNW FETs with strongly non-planar topography, thanks to the use of an Al etch mask deposited with nanostencil. The electrical behavior con-

firm the results obtained from similar devices fabricated with a standard lithography approach while achieving higher density, lar-
gre reproducibility and yield, maintaining the performance

improvement related with scaling. Finally, functional inverter

and logic NAND operations are obtained, confirming the discussed fabrication flow as valuable tool to build logic circuits.

References