Modular DC/DC Converter for DC Distribution and Collection Networks

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Nidschi hälfunt alli Heiligu, obschi hilft nidemal der Tyfil.
— Proverb from the Wallis

To my parents…

Preface

A PhD is a long journey and many people contributed to bringing mine to a successful end. First of all I would like to thank Prof. Alfred Rufer for accepting me as his PhD student. Since the very beginning of his tutoring, he surprised me with his vision and the confidence he had in me investigating my ideas.

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However, the fact that I even have gotten this far I owe to my parents, who supported me unconditionally in every activity and who were always a guide for me.

Lausanne, June 2012 Stephan Kenzelmann

Abstract

A major change in the electrical transmission and distribution system is taking place in Europe at the moment. The shift from a centralised energy production to a distributed generation profoundly changes the behaviour of the grid. Environmental or social issues associated with the construction of new power lines to relieve bottlenecks, together with aged equipment dating from the 1960s, pose some serious challenges to government, the research community and the economy. Concepts of reactive compensation, harmonic cancellation, voltage stability, power quality and bulky low-frequency transformers need to be redefined for power exchange and transmission in the future. Photovoltaics, wind turbines, fuel cells, storage systems and uninterruptible power supplies use many power electronic interface circuits, where DC intermediate levels already exist. Large photovoltaic- or wind- powered installations, which are connected to a cable network, are characterised by non-negligible distances due to their low power-by-surface density. On the side of the consumer, current trends show an increasing use of DC in end-user equipment.

In such a context, the numerous advantages of power electronics and DC cables may sometimes out-weigh their higher cost. In the future, high-power semiconductor devices that allow higher switching frequencies of the converters may make it possible to downsize even more the passive components. This would significantly reduce raw material consumption and therefore cost, something that is crucial for the market to accept the technology.

In the first part of this PhD thesis, the advantages of DC distribution in terms of transmission losses are illustrated with the help of three case studies.

The second part and the main contribution of this thesis is the analysis of a promising candidate for a power electronic transformer, the key component of any DC based grid. It is a bidirectional isolated DC/DC converter based on modular multilevel converters, which are well suited for medium or even high voltage range. The motivation was to investigate a converter operation with important voltage elevation ratios, capable of adapting the voltage level between low, medium and high voltage. A medium-frequency isolation stage provides the possibility of downsizing the passive components. Two modulation methods, a multilevel and a two-level operation, were analysed and compared in terms of losses.

The modular DC/DC converter is an attractive solution for the sensitive aspect of the short-circuit behaviour of classical DC links and power lines. The converter can also handle short circuits without the need for additional protection devices, such as circuit breakers.

Given the many advantages of DC systems (reduced environmental impact, reduced space requirements, reduced raw material use, high power quality, power flow control, low transmission losses), this new technology must, at least, be considered when assessing the extension or the renovation of conventional AC grids.

Keywords : DC Distribution and Collection, DC/DC Converter, HVDC transmission, Power Electronic Transformer, Multilevel Converter, Medium-Frequency Transformer, DC Grid Protection

Zusammenfassung

Die Europäische Stromversorgung steht im Zeichen des Wandels. Im Stromnetz verteilte, erneuerbare Energiequellen stellen die herkömmliche, zentralisierte Energieproduktion in Frage. Um das grösstenteils in den 60er Jahren erbaute Wechelstromnetz zu erweitern, müssen administrative Hürden überwunden werden. Sozial- und umweltverträgliche Einschränkungen erschweren diesen Vorgang zusätzlich. Dies stellt grosse Herausforderungen an Regierung, Forschung und Industrie.

Blindleistungskompensation, Energiequalität, Netzstabilität und materialintensive Spannungsumformer verlangen zudem eine Wiederbewertung der konventionellen Wechselstromversorgung. Erneuerbare Energien wie Photovoltaik und Windkraft, Brennstoffzellen und unterbrechungsfreie Stromversorgungen weisen oft schon eine Gleichstrometage in der Wandlerstufe auf. Durch die relativ niedrige Leistungsdichte der Wind- und Sonnenenergieanlagen drängt sich zudem ein effizientes Energiesammelnetz auf, welches wenig Verluste in den verkabelten Leitung aufweist. Auch zeigt sich auf der Verbraucherseite eine Tendenz zum vermehrten Gebrauch von Geräten welche Gleichstrom benötigen.

In diesem Zusammenhang scheint eine Gleichstromversorgung basierend auf Kabelsystemen und Leistungselektronik oft die Nachteile der erhöhten Kosten aufzuwiegen. Zukünftige Hochleistungshalbleiter, die höherfrequent getaktet werden können, werden diese Entwicklung nur beschleunigen, da mit geringerem Materialverbrauch die Kosten sinken.

Der erste Teil dieser Doktorarbeit zeigt die Vorteile eines Gleichstromnetzes im Mittelspannungsbereich auf und wertet diese anhand dreier konkreter Beispiele aus. Der zweite Teil beinhaltet den wesentlichen Beitrag dieser Arbeit. Der wichtigste Bestandteil eines Gleichstromnetzes ist der leistungselektronische Spannungsumformer, welcher das Bindeglied zwischen den verschiedenen Spannungsebenen ist. Es ist ein isolierter Gleichstromwandler, basierend auf dem Konzept eines modularen Stromrichters, welcher sich besonders für Mittel- und Hochspannungsnetze eignet. Besonderes Interesse lag in der Analyse der Spannungserhöhungseigenschaften dieses Wandlers, welche es ermöglichen sollten, die hohen Spannungsunterschiede zwischen Nieder-, Mittel- und Hochspannung zu meistern. Eine mittelfrequente Isolationsstufe ermöglicht zudem die Reduzierung der passiven Bausteine und somit des Gewicht und Volumen der Anlage. Zwei Modulationsmethoden, eine Mehrpunkt- sowie eine Zweipunktschaltung werden vorgestellt, welche es zum Ziel haben die Taktfrequenz der Leistungselektronik auf ein Minimum herabzusetzen. Die zwei Modulationsmethoden werden in Bezug auf die Schaltungsverluste verglichen.

Zusammenfassung

Das für konventionelle Gleichstromwandler und Gleichstromnetze heikle Fehlerverhalten bei Kurzschlüssen wird mit der vorgeschlagenen Wandlerstruktur entschieden entschärft. Der Wandler ermöglicht es Kurzschlüsse ohne zusätzliche Sicherheitsvorrichtungen oder Gleichstromschalter handzuhaben.
Die Vorteile eines Gleichstromnetzes (bessere Umweltverträglichkeit, geringer Platzverbrauch, niederiger Materialverbrauch, gute Versorgungsqualität, Anpassungsfähigkeit, genaue Kontrolle des Leitsungsflusses, geringe Übertragungsversluste) müssen unbedingt in Betracht gezogen werden bei der Erweiterung oder Erneuerung des herkömmlichen Wechselstromnetzes.

Stichworte : Gleichstromnetze, Gleichstromwandler, Leistungselektronische Spannungsumformer, Hochspannungs-Gleichstromübertragung, Mehrpunktschaltungen, Mittelfrequente Spannungsumformer, Gleichstromnetzschutz

Résumé

Le réseau électrique européen est dans une phase de changement radical. Le passage d'un concept de production centralisée à une génération d'énergie distribuée affecte profondément les notions de contrôle et de stabilité du réseau. Les barrières administratives suscitées par les enjeux environnementaux et sociaux pour construire de nouvelles lignes électriques accentuent les difficultés d'évolution/adaptation du système. De plus le fait que les équipements en place aient été en grande partie construits dans les années 60 pose de sérieux défis aux gouvernements, chercheurs et industriels. La compensation d'énergie réactive, la qualité de tension, la stabilité du réseau, ainsi que l'utilisation de grands transformateurs basse-fréquence requièrent une réévaluation des technologies actuelles basées sur des grandeurs courant/tension alternatives. Les sources renouvelables telles que le photovoltaïque et l'énergie éolienne d'une part, ainsi que les systèmes de stockage et de sauvegarde d'autre part, utilisent souvent des interfaces d'électronique de puissance où un étage continu est déjà présent. La faible densité de puissance des installations photovoltaïques et éoliennes nécessite un réseau de collection d'énergie Ã haut rendement. Du coté des consommateurs, on note une transition vers l'utilisation d'équipements alimentés en continu.

Dans un tel contexte, les nombreux avantages de l'utilisation de l'électronique de puissance et des réseaux continus peuvent souvent compenser le prix plus élevé inhérent à de cette technologie. En revanche, des futurs composants semi-conducteur de haute puissance, qui permettent une fréquence de commutation plus élevée, permettront de réduire le volume et donc le coût des matières premières, paramètre crucial pour l'acceptation de cette technologie.

Dans la première partie de cette thèse de doctorat, les avantages d'un réseau de distribution continu sont démontrés et illustrés par trois exemples.

La deuxième partie est dédiée à l'analyse d'un candidat de convertisseur continu-continu prometteur, contribution novatrice de cette thèse. Le convertisseur est l'élément clé d'un réseau continu, car il adapte les niveaux de tension. Une topologie modulaire permet son utilisation, que ce soit pour la moyenne ou bien la haute tension. Dans l'analyse, un soin particulier est porté à l'examen des propriétés d'élévation de tension à fort rapport. L'utilisation d'un étage alternatif à moyenne fréquence permet la réduction de la taille des composants passifs. Deux méthodes de modulations ont été analysées, une modulation multi-niveau et une modulation deux-niveau, ayant comme but de minimiser le nombre de commutations dans le convertisseur. Les deux méthodes ont été comparées par rapport

aux pertes dans les éléments semi-conducteurs. La topologie proposée est une solution attractive pour résoudre le comportement de convertisseur continu-continu standard ou de réseaux continus en cas de court-circuit. Le convertisseur est en effet capable de tolérer de telles fautes sans moyen de protection additionnel.
Dans l'éventuelle extension ou rénovation du réseau alternatif conventionnel, compte tenu des avantages des systèmes à courant continu (impact environnemental réduit, peu d'espace occupé, utilisation réduite des matières premières, bonne qualité et flexibilité du réseau, contrôle exacte des flux de puissance et peu de pertes de transmission), les technologies à courant continu doivent au moins être prises en compte.

Mots-Clés : Réseau de Collection et Distribution Continu, Convertisseur continu-continu, Transmission à Haute Tension Continue, Transformateur à base de l'Électronique de Puissance, Convertisseur Multiniveau, Transformateur Moyenne Fréquence, Protection des Réseaux Continus

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Glossary

A_e	Cross section of the core of a transformer	131, 132
A_w	Cross section of the windings of a transformer	131, 132
B_{max}	Maximum flux density in the transformer core	131
$\cos\phi$	Power factor of an AC system	76
C'	Capacity of a high voltage cable per unit length	13
δ	Phase between primary and secondary voltage waves	43, 87, 88
δ_{max}	Maximal phase shift considered for converter design	92, 94
ϵ	Voltage ripple on a capacitor in percent	76
f_p	Switching frequency	119
i_{ac}	AC current on the level of the transformer or AC load	64, 66, 86, 113, 115, 121, 156, 167
i_C	Collector current of the IGBT	137, 138
i_{circ}	Current difference between the upper and lower branch current	72, 74, 75
I_{dc}	DC current	68, 162
I_{dc1}	DC current of the primary MMC	120

I_{dc2}	DC current of the secondary MMC	88, 120
i_F	IGBT diode current	138
I_{ki}	Additional DC current due to the unbalance of the branch energies	68, 162
i_l	Current in the lower branch of a single phase leg of the MMC	65, 66, 165
i_u	Current in the upper branch of a single phase leg of the MMC	65, 66, 165
k	Parameters which indicates the degree of DC unbalance between the upper and lower branch voltage in a MMC	68
κ	Number of periods that are considered for the loss evaluation	137
k_{core}	Coefficient that represents the scale of the core losses	134
k_d	Coefficient that represents the scale of the dielectric losses	134
k_i	Parameters which indicates the degree of DC unbalance between the upper and lower branch current in a MMC	68, 162
k_p	Elevation factor of the primary MMC	91, 108, 111, 118–120
k_s	Elevation factor of the secondary MMC	91, 109, 118, 119
k_W	Coefficient that represents the scale of the winding losses	134
L'_i	Metric inductance of a cable	13
L_m	Magnetizing inductance of the transformer	45
L_σ	Leakage inductance of a transformer	43, 86
m	Modulation index	67, 70, 74, 99, 162
m_{2L}	Equivalent modulation index for the two-level operation of the MMC	108
m_l	Modulation index of the lower branch of a MMC	70, 74
m_u	Modulation index of the upper branch of a MMC	70, 74
μ	Conductivity of a conductor in Siemens per meter [S/m]	9
n	Scaling factor relating the AC quantities with the DC quantities	67, 162

N_{ac}	Number of cells connected in the "AC-loop"	111
N_{dc}	Number of cells connected in the "DC-loop"	111, 118
N_p	Number of submodules per branch in the primary MMC	112
N_s	Number of submodules per branch in the secondary MMC	112
ϕ_l	Phase shift between voltages at the terminals of an electrical line	17
Q_p	Reactive power on the primary side	88
Q_s	Reactive power on the secondary side	88
R'_{ac}	Effective metric AC resistance due to the skin effect	9
$R_{ac,90^{\circ}\mathrm{C}}$	AC resistivity at 90 °C	15
R_{dc}	DC resistance of a cable	8
$R_{dc,90^{\circ}\mathrm{C}}$	DC resistivity at 90 °C	15
ρ	Resistivity of a conductor	8
SiFe	Silicon-Steel, material used for transformer cores	136, 168
S_{rms}	Current density in the transformer windings	132
T	Period of an AC signal given by $T = \frac{1}{F}$	69
T_{Calc}	Calculation and measurement delay	104, 119
T_{cm}	Command organ time delay	104, 119
T_f	Filter time constant	104
T_i	Integral time constant of PI controller	103, 119
T_n	Proportional time constant of PI controller	103, 119
T_{pE}	Equivalent time constant that summarises the small time constants in the system	104, 119
u_{ac}	Generic AC voltage waveform	67
u_{ac1}	Primary transformer terminal voltage	86, 110, 112, 113, 120, 121, 123, 167

u_{ac2}	Secondary transformer terminal voltage	86, 111, 114, 115, 120, 121, 123, 167
u_{ce}	Collector- Emitter voltage of the IGBT	137
u_{circ}	Voltage on the branch impedance due to the circulating current	72
u_{cl}	Sum of the voltages at the terminals of the submodules of the lower branch of a MMC	68
u_{cu}	Sum of the voltages at the terminals of the submodules of the upper branch of a MMC	68
U_{dc}	Generic DC voltage	162
U_{dc1}	Primary DC voltage	110, 112
U_{dc2}	Secondary DC voltage	110, 111, 118, 120, 126
$\hat{U}_p$	Amplitude of the sinusoidal part of the primary branch voltage	85
u_p	Primary transformer voltage without considering the branch impedance	87
$\hat{U}_s$	Amplitude of the sinusoidal part of the primary branch voltage	85
u_s	Secondary transformer voltage without considering the branch impedance	87
U_{sm}	Submodule voltage	53, 62, 76, 91, 124, 138
u_x	Terminal voltage of one submodule	53, 116
VITROPERM	Nano-crystalline alloy used for transformer cores	136, 168
W_c^{circ}	Difference of the energies in the upper and lower branch	73, 76
W_c^{sum}	Sum of the energies in the upper and lower branch	73, 76

W_l	Energy variation over a period of the lower branch of a MMC	70
W_u	Energy variation over a period of the upper branch of a MMC	70
$y_{proximity}$	Empirical factor influencing the AC resistivity of a line due to the proximity effect	10
y_{skin}	Empirical factor influencing the AC resistivity of a line due to the skin effect	10

Acronyms

AAF	Anti-Aliasing filter	154
AC	Alternative Current	1
ADC	Analogue-to-Digital Converter	154
APOD	Alternative Phase Opposition Disposition	55
ARW	Anti-Reset Windup	103
DAB	Dual Active Bridge	43, 45–47, 108, 109, 126–128
DC	Direct Current	1
DFIG	Double Fed Injection machine	22, 29, 31
DSP	Digital Signal Processor	151, 152, 154
ESR	Equivalent Series Resistance	65
FLC	Flying Capacitor converter	47, 49
FMEA	Failure Mode and Effects Analysis	160
FPGA	Field-Programmable Gate Array	151, 152, 154
HV	High Voltage	3
HVAC	High Voltage Alternative Current	2
HVDC	High Voltage Direct Current	2, 51, 159

IGBT	Insulated Gate Bipolar Transistor	47, 49, 145
LCC	3th order resonant converter based on one inductance and two capacitors	46
LF	Low Frequency	3
LLC	3th order resonant converter based on two inductances and one capacitor	46
LV	Low Voltage	3
LVDC	Low Voltage Direct Current	2, 159
MF	Medium Frequency	4, 41, 42, 48, 59, 81, 88, 131
MLC	Multilevel Converter	47
MMC	Modular Multilevel Converter	4, 51, 65, 67, 70, 73, 76–79, 81, 82, 84, 86, 89, 94–96, 100, 101, 106–110, 112, 113, 116, 120, 122, 126, 140, 147

MPPT	Maximum Power Point Tracking	33, 34
MV	Medium Voltage	3
MVDC	Medium Voltage Direct Current	2, 159
NLC	Nearest Level Control	59, 60, 62
NPC	Neutral Point Clamped converter	34, 47, 49
PCC	Point of Common Connection	21, 25, 26
PD	Phase Disposition	55, 56
POD	Phase Opposition Disposition	55
PRC	Parallel Resonant Converter	46
PSPWM	Phase Shifted Carriers PWM	55
PV	Photovoltaic	2
PWM	Pulse Width Modulation	53–55
RMS	Root Mean Square	66, 74
SDRAM	Synchronous Dynamic Random-Access Memory	154
SHE	Selective Harmonic Elimination	59, 62, 64, 96, 99
SMC	Stacked Multi-Cell converter	47, 49
SMPS	Switched-Mode Power Supply	36
SPI	Serial Peripheral Interface	151, 152
SPRC	Series Parallel Resonant Converter or LCC	46
SRC	Series Resonant Converter	46
SVC	Space Vector Control	59, 60, 62
SVM	Space Vector Modulation	55, 57, 58, 60–62
THD	Total Harmonic Distortion	62, 96, 98

UPS	Uninterruptible Power Supply	3, 36
ZCS	Zero Current Switching	45
ZVS	Zero Voltage Switching	45

1 Introduction

1.1 Historical Development

The first electrical systems were used to power lights in industrial and commercial buildings. With the intention of building lighting that requires less maintenance, Thomas A. Edison conceived 1882 an entire lighting system including electrical generation and distribution based on Direct Current (DC) [1]. At that time it was not possible to step up the DC voltage, therefore limiting the use of DC to local production and consumption. However the introduction of the transformer and polyphase Alternative Current (AC) motors by Nikola Tesla was a game changer. Now it was possible to transport electrical energy over large distances and the land-stone for our today's AC network has been laid. Since the Chicago's World Fair in 1893 [2] where an AC based power system was used to power more than 100'000 incandescent light bulbs, AC quickly eclipsed the DC power system technology. Even if the use of AC became the dominant technology, DC systems remained in operation. For example in Stockholm, Sweden, the residential DC distribution grid was replaced by AC only in the 1970's [3]. Telecommunication systems are still based on 48Vdc. DC offered speed control to the electrical machines for trams, subways, trains and other industrial drive systems and is still used nowadays. Since the introduction of the semiconductor technology in the 1970, DC systems have become again an attractive alternative to AC systems.

1.2 AC versus DC

1.2.1 Transmission

The AC distribution and transmission system has been in place almost for 100 years now and only since the 1970's DC has become in some cases a real alternative.

The today's AC transmission faces several challenges. First the entire grid infrastructure is rather old, most of it has been built in the 1960's. Modernization is urgently needed, but there are many constraints for building new lines. Many bottlenecks exist that lead to serious congestion problems. Reactive power compensation decreases the transmission capacity of AC lines. Furthermore the deregulation of the market has led to a declining investment in the infrastructure.

DC lines could solve or at least relieve some of the problems in transmission. However, for short distances the cost is still higher for a High Voltage Direct Current (HVDC) line. In general the break-even distance illustrated in Fig. 1.1 depends on various aspects, such as right of way (the required width of the corridor around the HVDC power line is almost half of the space required for High Voltage Alternative Current (HVAC) systems), the transmission medium (cable or overhead lines), the type of substation (HVAC, thyristor based HVDC, VSC-HVDC) and environmental aspects (generally in disfavour of AC systems). For a thyristor HVDC system, the break-even distance using overhead lines is between 500km and 800km [4]. For cabled systems, the break-even distance is much lower, generally between 40km and 80km. The total losses for HVDC are more important than for HVAC for low distances, since the efficiency of the HVDC converter cannot match the efficiency of the transformer in an AC system. On the other side, line losses are smaller for HVDC.

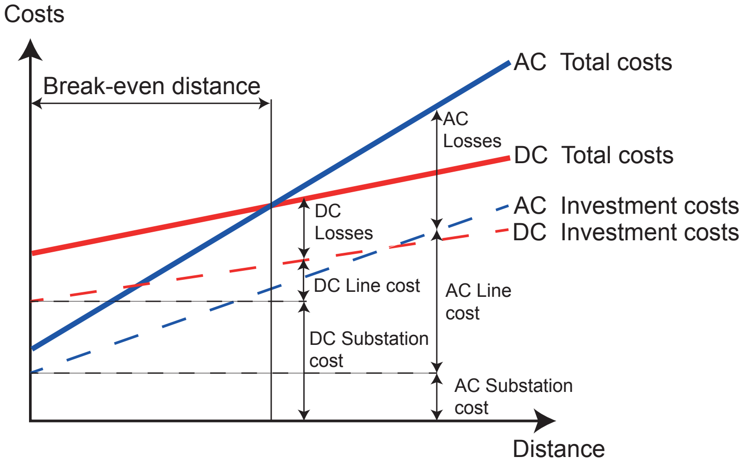


Figure 1.1: Break-even distance of HVDC versus HVAC [5]

1.2.2 Distribution

The way energy is produced is about to change from a centralised to a more distributed production [6]. These distributed generators include many DC output based technologies, such as Photovoltaic (PV), fuel cells and even micro- and wind turbines often have a DC intermediate circuit.

First investigations in the field of Medium Voltage Direct Current (MVDC) or Low Voltage Direct Current (LVDC) distribution concepts have been proposed within dedicated contexts like feeding of large Computer Server Farms. In this approach, multiple, decentralised sources are considered, but also back-up power like classical Uninterruptible Power Supply (UPS). However, the cascade of multiple classic AC/DC and DC/AC conversions can lead to poor energy efficiency [7]. The use of bulky Low Frequency (LF) electromagnetic transformers furthermore requires a lot of raw material.

Storage technologies are to play an important role in the future grid due to the stochastic production of the renewable energy. Battery based storage or even electrical vehicles could be used in the future to support the electricity network. These storage technologies are based on DC and will most probably be used in the distribution level.

On the side of the loads, many domestic devices such as computers, lighting and sometimes even washing machines require a supply with DC power.

1.2.3 Actual State

The crucial element to either DC or AC grids is the voltage transformation devices. In an AC system, the transformers can easily adapt the voltage to a higher level for energy transport or reduce it to meet the load requirements. Conventionally the High Voltage (HV), Medium Voltage (MV) and Low Voltage (LV) networks are interfaced with multiple low frequency electromagnetic transformers. Voltage conversion for DC is yet not so simple and requires the use of power electronics, also called power electronic or DC transformer. The efficiency of conventional distribution transformer is generally higher than 98%. In order to match the efficiency of an AC system, the DC transformer should obtain at least the same efficiency.

Another decisive element in a distribution and transmission network is the protection. AC circuit breakers are available for all power levels and normally extinguish a short-circuit current after 10-100ms, taking advantage of the natural zero crossing in an AC network. Today, the strongest argument against a DC based transmission system is the fact that present circuit breaker technology is not available for high powers. Since the natural zero crossing in DC does not exist, active semiconductor devices that turn off the current have to be used. The technology for DC circuit breaker is not yet as mature as for AC, many circuit breakers have been proposed [8, 9], but not yet commercialised.

1.3 Objectives

When classical voltage transformation devices reach their optimal design and the limits of their capacities, new aspects from decentralised generation using DC voltage levels are expected to influence the general concept of power exchange between generators and consumers.

On the base of the previously given reflections and arguments, the proposal of a study is made for a MVDC energy collection and distribution grid. Indispensable voltage shift stages based on Medium Frequency (MF) power electronic transformations will be studied, where a large potential for secure, flexible and efficient power flow exists. New power electronic converter concepts are expected to become attractive solutions against the sensible aspect of the short-circuit behaviour of classical DC links and lines.

In particular the following points will be analysed in this thesis:

- DC collection networks and their properties and advantages
- New means of bidirectional interface converters between HV, MV, and LV
- Controllability and voltage boosting capacity of converters with important voltage step-up ratios is analysed
- Practical work will validate the proposed concepts

1.4 Outline

This work is organised in two parts and 9 chapters.

The first part is dedicated to DC collection and distribution grids, and illustrates the advantages of a DC system:

- In chapter 2, DC grids are compared to AC grids regarding efficiency and power transport capability. Three application fields are presented, where a DC grid could be employed. An AC and DC load flow is performed for each of the three collection and distribution grids and the losses are compared.
- Chapter 3 identifies the requirements to realise such DC networks and analyses possible converter candidates for the voltage adaptation. It has been found that the common drawback of the state of the art converters lies in the protection.

In the second part a converter topology, capable of coping with the short-comings of the conventional converter topologies regarding protection is presented:

- Chapter 4 introduces the Modular Multilevel Converter (MMC), which is a part of the proposed DC/DC converter structure. The possible modulation methods are described and a mathematical model is established. The internal control methods are depicted and the component sizing is tackled.

- In chapter 5, the modular DC/DC structure is presented. The mathematical model for this particular structure is derived and a formal parameter design is proposed.

- Chapter 6 is the main contribution of the thesis, which explains the converter operation. Section 6.1 focuses on the multilevel modulation method applied to the DC/DC converter. Two fundamental switching frequency modulation methods are compared in terms of harmonic performance. The strategies for the internal and external control are detailed. Simulation results are shown and a start-up strategy is proposed.
  An alternative modulation method based on a two-level modulation is shown in section 6.2. This method can achieve very high voltage elevation factors without using the transformer as voltage elevation device. Again the internal and external control is explained. Simulation results confirm the theoretical developments. The description of the start-up strategy completes this chapter.
  The protection issues of DC networks are approached in section 6.3. The proposed structure is compared to a state of the art DC/DC converter for different faults.

- In chapter 7, the efficiency of the topology is analysed. In section 7.1, a short description of the transformer design procedure is given and finally different designs are compared in terms of weight and loss distribution.
  Section 7.2 focuses on the losses created by the semiconductors. First the utilised evaluation method is described and then the different modulation methods are compared in terms of losses for a particular case.

- The laboratory prototype is depicted in chapter 8. Results are obtained for both the multilevel and two-level modulation.

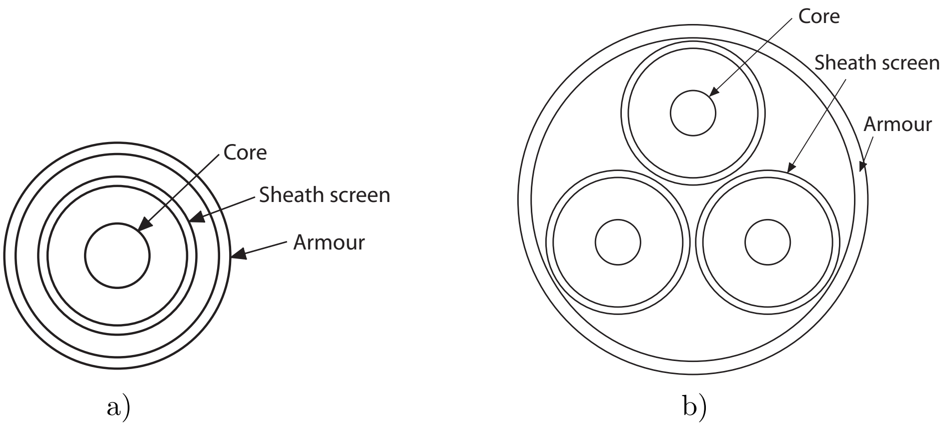
- Finally, chapter 9 gives the main conclusions and contributions of this thesis. The achieved objectives are discussed and future work will be pointed out.

2 DC Grid Applications and Case Studies

2.1 Efficiency of DC Distribution Systems

The efficiency and the power transport capability of MV networks will be investigated in this section. The efficiency of the producing or consuming units will not be considered, since efficiencies of converters depend very much on the actual stand of technology.

For this study only cable networks will be analysed. Both for offshore and onshore wind farms the collection network are compulsory undersea or in the ground. For solar plants, isolation favours the use of cables instead of open conductors. As far as the MV networks of cities is concerned, power transport is mostly done underground. Cables for AC systems are either single or three-core cables, depicted in Fig. 2.1.



a) b)

Figure 2.1: a) Single-core cable b) Three-core cables

Typically XLPE-insulated cables are used for isolation, therefore they have been chosen for the following analysis. The considered cables have a layer of heavy armour on the outside to give added strength both for laying and for protecting against mechanical damage. The electromagnetic effects between the layers within the cable need to be considered carefully when developing impedance models. Cables behave differently for AC than for DC, several effects have to be taken into consideration, which will be explained in the following.

2.1.1 Cable Parameters

A cable is determined by four parameters: resistance, inductance, capacitance and conductance, which can be influenced by various effects.

Cable Resistance

The line resistance R_{dc} is determined by the following formula

$$R_{dc} = \frac{\rho l}{A} \tag{2.1}$$

where ρ is the resistivity of the conductor, l is the cable length and A the cross-sectional area. The current in the conductor is equally distributed only for DC currents.

The Temperature Effect The resistivity of a conductor varies linearly with the temperature over the normal range of operation, given in the following equation.

$$R_{th} = R_{dc}\,(1 + \alpha(T - T_0)) \tag{2.2}$$

where α stands for the temperature coefficient of the material. T is the temperature in Kelvin and T_0 is the initial temperature.

The Skin Effect The non-uniform current distribution in conductors carrying alternative current is due to the skin effect. With higher frequency the current density is increased near the surface, since the conductor centre will be enveloped by a greater magnetic field. In Fig. 2.2 the skin effect in a single conductor is depicted, the darker the region, the higher the current density.

The skin effect makes the effective resistance of a cable depended on the frequency. The problem is one-dimensional in cylindrical coordinates and depends only on the radius ρ.

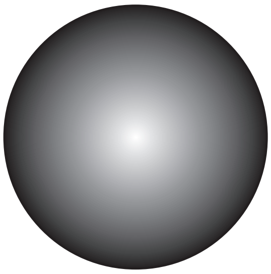


Figure 2.2: Skin effect

Using the Maxwell equations a relation for the current density can be found in (2.3) [11].

$$\frac{1}{\rho}\frac{d}{d\rho}\left(\rho\frac{d\underline{J}_z(\rho)}{d\rho}\right) - j\omega\mu\sigma\underline{J}_z(\rho) \cong 0 \tag{2.3}$$

The solution of this equation is a J_0-type Bessel function of order 0. The current distribution within the conductor is characterised by the skin depth, defined in (2.4). μ is the conductivity of the conductor in [S/m].

$$\delta = \sqrt{2/\omega\mu\sigma} \tag{2.4}$$

Below this depth the current density decays to $1/e \approx 0.37$ of the current density at the surface J_0. $\mu = \mu_0\mu_r$ is the absolute magnetic permeability of the conductor, μ_0 is the permeability of free space ($4\pi 10^{-7} NA^{-2}$) and μ_r is the relative permeability of the conductor (for a copper conductor $\mu_r = 1$).

The relation (2.4) can be simplified, considering that the equivalent current conducting space is a hollow tube, with a thickness of δ_s carrying direct current [12]. R'_{ac} is the effective resistance for the AC system.

$$R'_{ac} = \frac{1}{\sigma_r \pi \delta_s (2r - \delta_s)} \tag{2.5}$$

This approximation is only valid for cables with pronounced skin effect ($r \gg \delta_s$).

The Proximity Effect The proximity effect is often ignored when treating cable impedance models. It occurs when two conductors are situated closely together and their magnetic fields are influencing each other. The current is not equally distributed on the surface and can either be on the outer side of the conductor (current in the same direction) or the inner side of the conductor (current in opposite direction). Fig. 2.3 displays this effect.

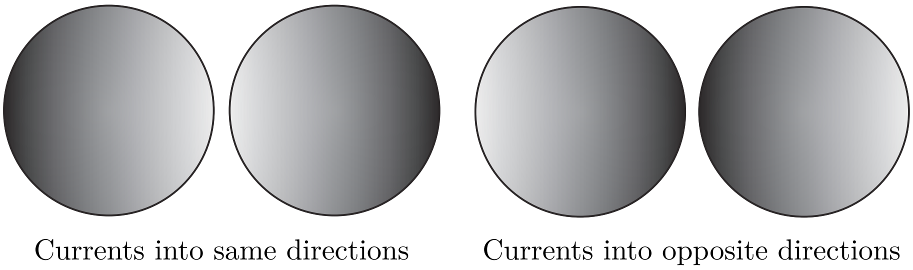

Currents into same directions
Currents into opposite directions

Figure 2.3: Proximity effect on two conductors

It has been shown in [11] that the proximity effect for single-core cables can be ignored, but not for three-core cables. For single-core cables only the skin effect has to be taken into account; for three-core cable, both, skin and proximity effect need to be taken into account. For calculating the proximity effect of three-core cables which are used for offshore energy collection, knowledge of the cable geometry is fundamental. The shielding and the layer arrangements can have an important impact on whether the proximity effect is influential or not. Since the proper determination of the proximity effect will exceed the frame of this thesis, it will only be referred to the development in [11].

Empirical Approach to Skin and Proximity Effect A somewhat more empiric approach is given in [13]. Skin and proximity effect are summarised to a factor y_{skin} and $y_{proximity}$ depending on the frequency which is multiplied with the DC resistance.

$$R_{ac} = R_{dc}(1 + y_{skin} + y_{proximity}) \tag{2.6}$$

The skin effect factor is given in (2.7) for single or multi-core conductors.

$$y_{skin} = \frac{x_s^4}{192 + x_s^4} \tag{2.7}$$

The proximity effect for a single-core cable can be described as follows:

$$y_{proximity} = 2.9 \frac{x_p^4}{192 + 0.8x_p^4} \frac{d_c^2}{S^2} \tag{2.8}$$

The proximity effect for a three-core cable can be described as follows:

$$y_{proximity} = \frac{x_p^4}{192 + 0.8x_p^4} \frac{d_c^2}{S^2} \left(0.312 \frac{d_c^2}{S^2} + \frac{1.18}{\frac{x_p^4}{192+0.8x_p^4} + 0.27} \right) \tag{2.9}$$

where

- $x_s^2 = 8\pi f 10^{-7} \frac{k_s}{R_{dc}}$
- $x_p^2 = 8\pi f 10^{-7} \frac{k_p}{R_{dc}}$
- k_s: Factor determined by conductor construction. 1 for circular, stranded compacted and sectored conductor.
- f: Frequency [Hz]
- k_p: Factor determined by conductor construction ($k_p = 1$ for circular, stranded and sectored conductors, $k_p = 0.8$ if the conductor is dried and impregnated)
- d_c: Diameter of conductor [mm]
- R_{dc}: DC resistance at operating temperature T
- S: Spacing between conductor centres [mm]

Generally for a 50Hz power network, the increase of the AC resistance is about 2%. Fig. 2.4 shows the proximity and the skin on a three-core cable used in a three phase system.

Stranded Conductors Since the strands within a cable are twisted, the DC resistance is not corresponding exactly to the cables length times the distributed resistance, but is about 1% higher [14].

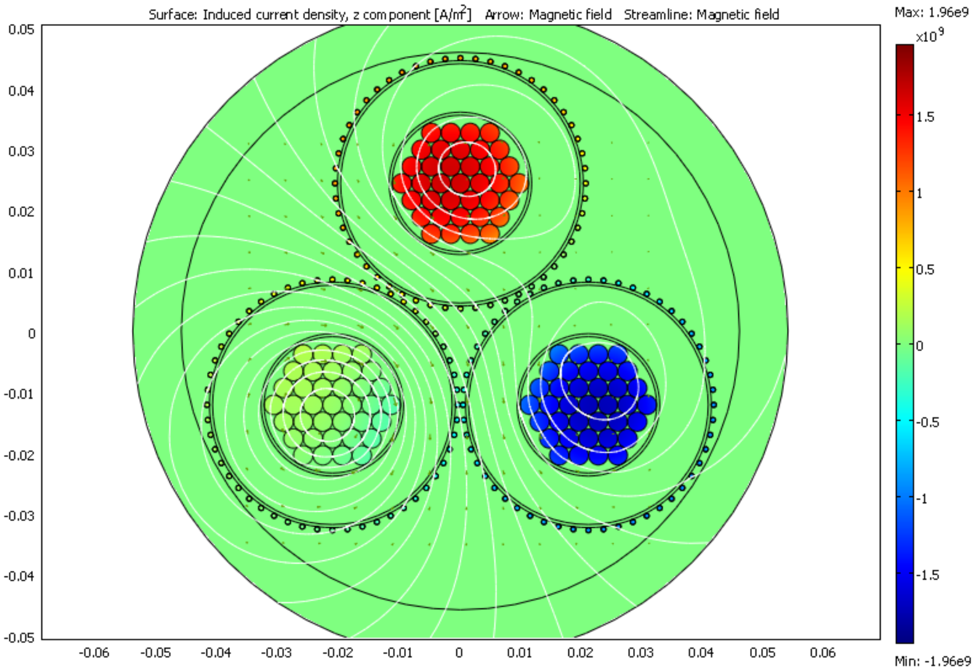


Figure 2.4: Proximity and skin effect on a three-core cable (Nexans $300mm^2$)

Cable Inductance

A rather easy evaluation of the cable inductances can be found by applying the "mean geometric distance" g_{ij} between two conductors i and j and the "mean geometric radius" g_{ii} introduced by Maxwell [15].

The mutual inductance per unit length of a conductor can so be defined [16].

$$M'_{ij} = \frac{\mu_0}{2\pi} \ln \frac{g_{in} g_{jn}}{g_{ij} g_{nn}} \tag{2.10}$$

The self inductance is defined by

$$M'_{ii} = \frac{\mu_0}{2\pi} \ln \frac{g_{in}^2}{g_{ii} g_{nn}} \tag{2.11}$$

Three-Core Cable The symmetric structure of the three-core, three-phase cable allows to introduce the cyclic inductance $L'_i = M'_{ii} - M'_{ij}$. This is only valid for systems that respect the equation $i_1 + i_2 + i_3 = 0$ and for which the mutual inductance M'_{ij} is identical for the three phases. The cyclic inductance L'_i per unit length of this cable, depicted in Fig. 2.1 is given in (2.12).

$$L'_i = \frac{\mu_0}{2\pi}\left(\ln\frac{2 * D_{12}}{d} + \frac{1}{4}\right) \tag{2.12}$$

where

- μ_0: permeability of free space
- D_{12}: centre to centre distance of two conductors
- d: conductor diameter

Cable Capacitance

Capacitance is the ability to store electrical energy in a dielectric media due to a potential difference between two conductors. A capacitive effect can take place between the conductor and the sea and soil, as well as with the armouring and sheathing. In contrast to overhead lines, where reactive power is consumed, cabled conductors are producing reactive power because the cable capacitance is much higher. This capacitance has several important impacts on system design and operation. For an AC system, the capacitive reactive power produced in the line has an impact on the reactive power balance of the feeder and the whole distribution system. The large charging current of cable networks may also hinder the operation of MV network circuit breakers even in a lightly loaded system [17]. As the total length of the MV feeder system is known, it is possible to evaluate the requirements for reactive power compensation and earth fault current compensation and/or the earthing impedance.

For a DC transmission system, a capacitive cabled line provides can be exploited to reduce the size of the DC capacitor bank required for providing DC voltage stability and for filtering of the switching noise [11]. (2.13) indicates the capacitance per unit length C' for a cable [18].

$$C' = \frac{2\pi\epsilon_0\epsilon}{\ln\left(\frac{D}{d}\right)} \tag{2.13}$$

- $\epsilon_0 = \frac{10^{-9}}{36\pi}\frac{F}{m}$: permittivity of free space
- ϵ: relative dielectric constant of the insulation (2.4 for XLPE)

- D: outer diameter including insulation
- d: inner diameter without insulation

Equivalent Model for the Cable

With the parameters given above an equivalent model for the cable can be established. For this work the equivalent π-model is selected, depicted in Fig. 2.5.

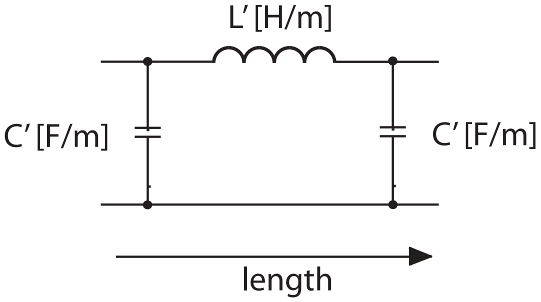


Figure 2.5: π-model of the power cable

2.1.2 Current Carrying Capacity

In an AC network, much more attention is allocated to the line reactance and often the line resistance is neglected. However, for DC systems the line reactance is nonexistent which leads to a much higher power transport capability [19]. To have a mean of comparison, cables with the same characteristics are going to be used for AC and DC, i.e. a three phase cable is used for AC without a neutral conductor. For the DC system, the same cable is used in a bipolar way with a positive, a neutral and a negative pole such as depicted in Fig. 2.6. The central conductor is the neutral and for a balanced system there should not be any current in this conductor.

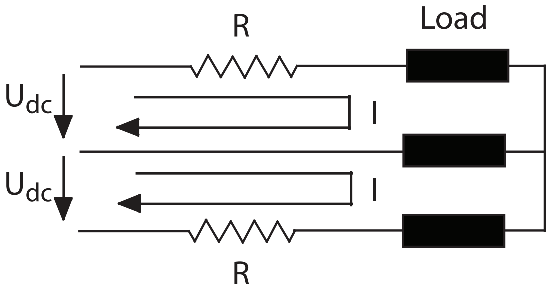


Figure 2.6: Three line DC model

Limitation of Power Flow due to the Resistive Losses

The maximum current in a conductor is determined by the maximum operating temperature. The temperature in a conductor increases due to the ohmic losses in the conductor. The maximal current for a given cable for either AC or DC transmission is found by determining and comparing the conduction losses for both cases. The losses for a three phase AC system or DC system are given in (2.15). $R_{ac,90^\circ\mathrm{C}}$ respectively $R_{dc,90^\circ\mathrm{C}}$ is the equivalent line resistance of the AC respectively DC system at 90 °C.

$$\Delta P_{ac,3} = 3R_{ac,90^\circ\mathrm{C}} I_{ac,3}^2 \tag{2.14}$$

$$\Delta P_{dc} = 2R_{dc,90^\circ\mathrm{C}} I_{dc}^2 \tag{2.15}$$

Working at the limit of operation for both AC and DC systems results in equal losses $\Delta P_{AC,3} = \Delta P_{DC} = \Delta P_{max}$). From this assumption the ratio of the AC and DC current can be determined. [20] gives a more thorough analysis of the losses of three phase cable dependent on the temperature.

$$\frac{I_{dc}}{I_{ac,3}} = \sqrt{\frac{3}{2}\frac{R_{ac,90}}{R_{dc,90}}} \approx \sqrt{\frac{3}{2}} \tag{2.16}$$

In order to simplify the above equation, the skin and proximity effect are neglected (around 3% only) and the AC resistance is supposed to be equal to the DC resistance.

Since the three phase cable is used in a bipolar way (see Fig. 2.6), the maximum DC voltage is twice the phase-neutral voltage of the three phase cable.

$$U_{dc} = 2\sqrt{\frac{2}{3}} U_{ac,3} \tag{2.17}$$

The power transport for AC and for DC is depicted in (2.18) and (2.19).

$$P_{ac,3} = \sqrt{3} I_{ac,3} U_{ac,3} \cos\phi \tag{2.18}$$

$$P_{dc} = I_{dc} U_{dc} \tag{2.19}$$

With the help of (2.16), (2.17), (2.18) and (2.19), the ratio of AC and DC power transport can be determined in (2.20). Fig. 2.7 illustrates the power transport capability dependent on the phase angle. However, one needs to take into account that this calculation does not consider the reactive energy needs of the cable, which can demand a certain value for $cos\phi$. This will be analysed further in the following.

$$\frac{P_{dc}}{P_{ac,3}} = \frac{2}{\sqrt{3}\cos\phi} \tag{2.20}$$

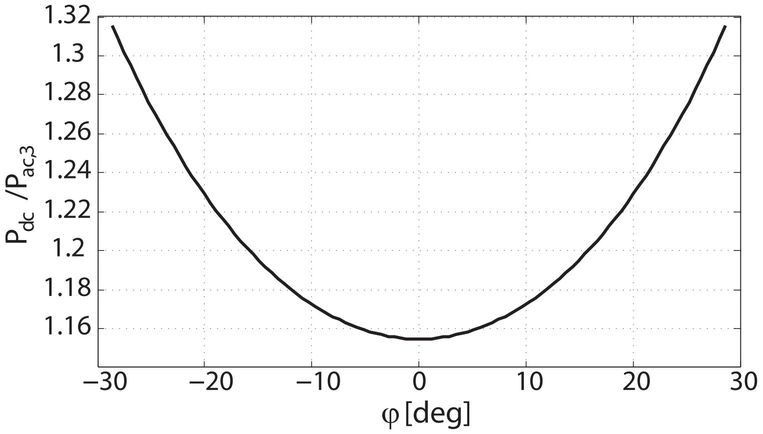


Figure 2.7: Ratio of AC and DC power transport

Limitation of Power Flow due to the Reactive Power

DC Power Transport The transported power for a DC system can be expressed as the difference between input power and cable losses. R' is the metric resistance of the cable in Ω/m and l is the length of the cable.

$$P_{dc} = U_{dc}I_{dc} - 2I_{dc}^2R'l \tag{2.21}$$

(2.21) is valid for a three line system, such as depicted in Fig. 2.6.

AC Power Transport Electrical lines for AC transmission can only be used within certain limits. For example, the phase difference between two points should not exceed a given angle, defined by the cable parameters and the transmitted power, since the maximum voltage and current should be respected. The active power transported by a three-phase AC system is limited not only by the resistive losses, but also by the reactive losses, since the reactive current in a line produces also resistive losses.

The transported complex apparent power can be described as the difference of input power and losses.

$$\underline{S}_{ac} = 3U_p I_l^* - (P_{losses} + jQ_{losses}) = P_{ac} + jQ_{ac} \tag{2.22}$$

with

$$P_{losses} = 3R'lI_l^2 \tag{2.23}$$

$$Q_{losses} = 3\omega L'lI_l^2 - 3\omega C'l\frac{U_p^2 + U_q^2}{2} \tag{2.24}$$

Considering a π-section model of a transmission line, represented in Fig. 2.5, the power transfer from the sending port (s) to the receiving port (r) is expressed in (2.26).

$$P_{sr} = \frac{3|U_s|^2}{|Z_l|}\left(\cos(\phi_l) - \frac{|U_r|}{|U_s|}\cos\left(\theta_{sr} - \phi_l\right)\right) \tag{2.25}$$

$$Q_{sr} = \frac{3|U_s|^2}{|Z_l|}\left(\sin(\phi_l) + \frac{|U_r|}{|U_s|}\sin\left(\theta_{sr} - \phi_l\right)\right) + 3U_q^2 B_t/2 \tag{2.26}$$

In the equations derived above, the equivalent π-model has been used for the long transmission line, for which the parameters Z_l and ϕ_l are given in the following equation.

$$\underline{Z_l} = R'l + j\omega L'l = R_l + jX_l \tag{2.27}$$

$$\phi_l = \arctan\frac{\omega L'}{R'} \tag{2.28}$$

$$\underline{B_t} = j\omega C'l \tag{2.29}$$

θ_{SR} = Phase shift between the voltages at both ends

Fig. 2.8 explains the needed compensation of reactive power. The more active power is transported, the more reactive power must be injected to keep the voltages at the extremities constant. Often the loads consume reactive power, which must be transported in addition.

A line or a network can be operated trying to keep all the voltages constant. This means

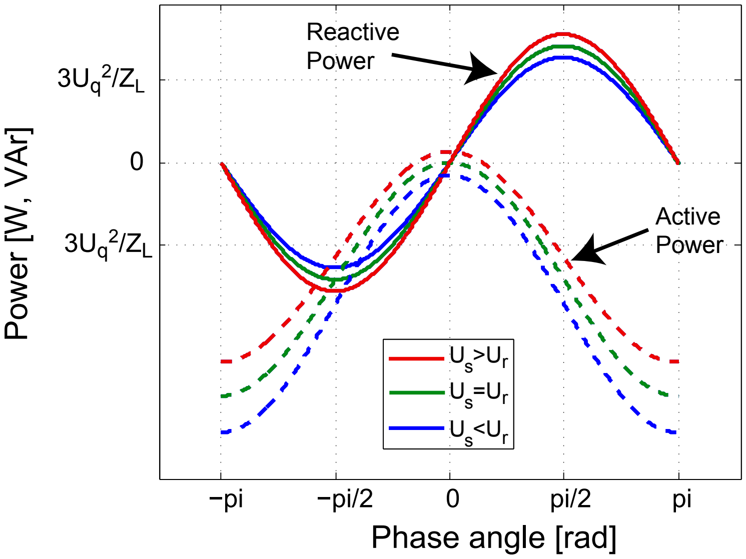


Figure 2.8: Transportable AC power in a power cable

that somehow reactive power needs to be introduced to compensate the voltage drop. If the receiving end is not consuming any reactive power, so we can set $Q_{ac} = 0$. This implicates that the reactive power consumption of the line needs to be compensated by the input. The reactive power for the voltage compensation flows into the opposite direction of the active power flow.

The reactive or charging current limits therefore the cable power rating. In a cable network the charging current is determined by the capacitance per unit length and the voltage level. As the cable capacitance increases with the length of the cable, there is a critical point where the actual heat losses due to the charging current is as high as the entire thermal rating capacity [21], which means that no active power is any more transported. This is known as the critical length, which depends on the on the frequency, the capacitance per unit length, the charging current and the voltage level. In Fig. 2.9, the power transport capability of underground transmission lines is shown in dependence of the transmission distance [21]. It becomes clear that for transporting AC power over longer distances, compensation of the charging current is required.

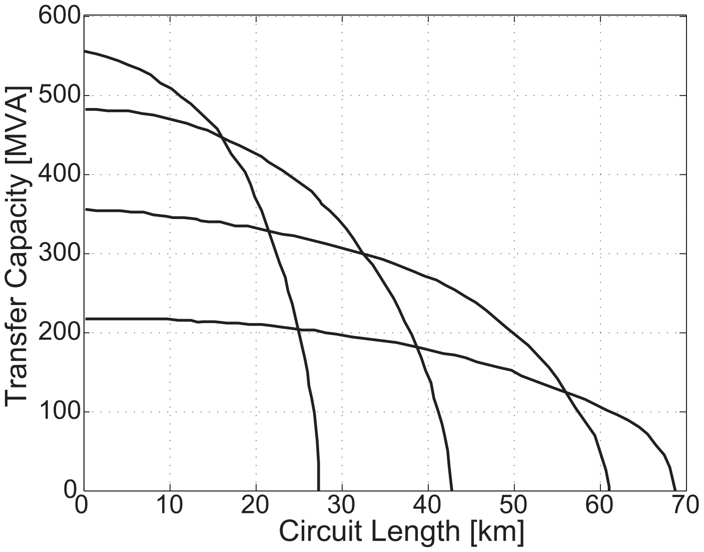


Figure 2.9: Critical length of a $1000mm^2$ underground power cable [21] for an AC power transmission

2.2 DC Collection Grid for Wind Power, PV and Cities

In this section the collection networks of two main renewable energy sources will be presented, wind power and photovoltaic power. What distinguishes these two energy sources among others (hydro power, biomass power, geothermal power, ocean power) is the fact, that the energy is not produced in a single point, but collected from a wider area.

2.2.1 Wind Power

Wind power has seen a huge development in the last years and is one of the most promising renewable energy sources. It would be more efficient to place the turbines near the consumer, but wind turbines are highly visible elements in the landscape and therefore not so easily integrable into the environment. To reduce cost, many wind turbines form a wind farm. A recent trend is to place these wind farms offshore, where the wind is more constant and more space is available.

Generally the life time of a wind turbine is 20 years, depending on the stress on both mechanical and electrical side. Within this life time the turbine produces 80 times the energy that was needed to build and install it [22].

Grid Interaction The inertia of the rotating mass constitutes a kind of energy storage, which is not so much affected by small variations of the wind power. However, wind turbines can have a significant effect on a grid, especially on a weak grid. Flicker during continuous power mode (i.e. not at start-up) is mostly due to power fluctuations. These fluctuations are due to variation in the wind speed, the tower shadow effect and mechanical properties of the turbine (mostly pitch control) [23]. Also the start-up and stop sequence introduces flicker. Power electronic converters are injecting harmonic pollution into the grid, but the effect can be smoothed with the help of filters. Other effects, such as the generator and gear box behaviour have less impact.

Implications and Tendencies of Wind Power

The globally installed wind power has reached 240GW by the end of 2011, whereas the China has passed the USA in terms of installed power [24]. The wind energy sector experiences a substantial growth of about 16% per year. In 2006 eight of the 45 completed wind projects were over 100MW, so there is a clear tendency to build bigger wind farms [25]. Another tendency is to use larger turbines (Today's turbines are twice as powerful as six years ago).

An important role for a successful wind farm project plays the transmission lines. The resources of remote located wind farms can only by unlocked by new transmission lines. The existing transmission lines should be used as efficiently as possible; a generally more flexible power network is needed to grant full integration. The connection of these large wind farms can have a severe impact on the grid and therefore there are several specifications set to the wind farm operator, which can be significantly different from the condition up to now (the example is given for the Horns Rev 160MW Offshore wind farm [26]):

- Perform control tasks similar to conventional power plants (Primary and secondary control)
- Disconnection or reduced production when transmission capacity is limited. The power rate of change should correspond to a reduction from 100% to 20% in 5 seconds in the worst case.
- The balance of reactive power should be neutral.
- The wind farm should withstand a three phase fault.

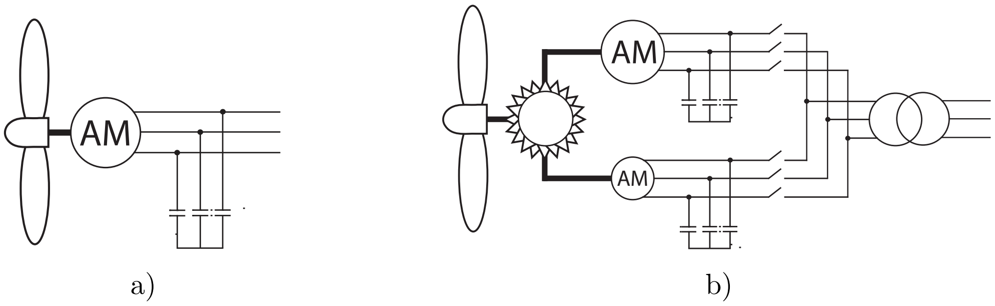
Most of the wind farms today are situated onshore, but especially in the densely inhabited Europe, the space is limited. Offshore wind farms are a good alternative, as there is big potential and shallow water. Germany is planning to provide till 2030 25% of the electrical power by wind power, whereas 10% produced onshore and 15% offshore [27]. In Denmark, the "Energy 21" plan of the Danish government previews by 2030 to have installed 5.5GW wind power, whereof 4GW offshore.

The costs of operating and maintaining of wind farms are expected equal or higher to the initial installation costs. So every contribution of reducing maintenance, such as monitoring, remote fault diagnostic are fundamental to offshore wind farms, since often the access is impossible for some periods of the year.

Wind Turbines

Generally speaking, two types of wind turbines can be distinguished, fixed speed turbines and variable speed turbines. They will shortly be presented in the next sections.

Fixed-Speed Turbines Fixed-speed generators, shown in Fig. 2.10a) are directly connected to the Point of Common Connection (PCC). Often squirrel cage induction generators are used (known as the "Danish concept"), since they are reliable and inexpensive [28]. The more active power they produce, the more reactive power is consumed. A shunt capacitor bank is used to compensate the reactive power.



a) b)

Figure 2.10: a) Electrical scheme of the fixed-speed wind turbine b) Direct connection of two different sized induction generators

Basically, the turbines work at constant speed, but some generators may change the number of their poles, making the turbine turn at different speeds for high and low wind periods. Another possibility is to install two generators rated at different powers in the turbine, one for high wind speeds, and the other for low wind speeds, as depicted in Fig. 2.10b).

Variable-Speed Turbines Variable-speed turbines allow a generator to turn at variable speed while the stator windings are still connected to the stiff grid with its fixed frequency. The excessive energy of the wind is stored as rotational energy and this way mechanical stress is reduced. Generally the system efficiency is improved, since turbine speed and wind speed are correlated to produce maximum output power. The pitch control is simplified and only needed to limit the maximum output power at high wind speeds.

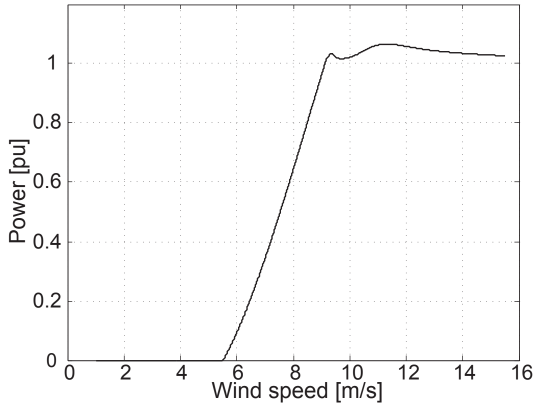
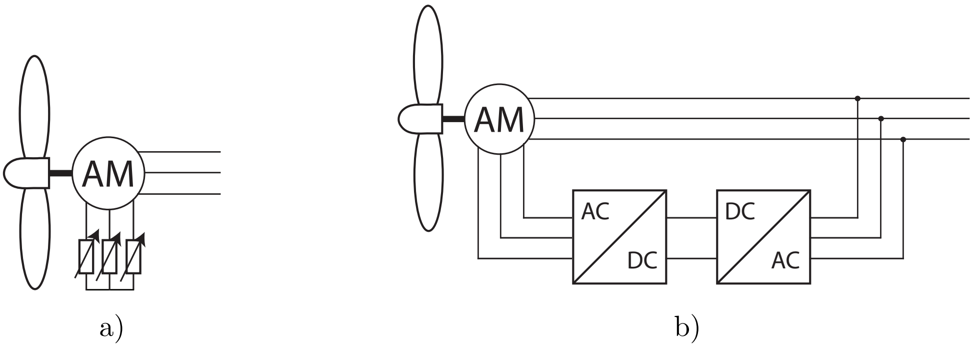


Figure 2.11: Activated pitch to control maximum power output

The slip of the induction generator is adapted to vary the rotational speed and is normally very small for better efficiency. Changing the resistances in the rotor, the slip can be increased or decreased. This can be done by external rotors resistors connected by the means of brushes and slip rings, visible in Fig. 2.12a).



a) b)

Figure 2.12: a) Variable rotor resistors b) Doubly fed induction generator

This is clearly a drawback, since the mechanical use of brushes is quite important and needs maintenance. An answer could be mounting the external resistors directly on the rotor.

Rotor cascade technique, as depicted in Fig. 2.12b), is another possibility of creating variable speed turbines. This is often referred to as Double Fed Injection machine (DFIG). Instead of variable resistors, a four-quadrant AC/AC converter is connected to the rotor windings. Typically the inverter is rated 25% of the nominal power and a speed variation of ±33% around the synchronous speed is possible [29]. Also the filter only needs to be designed for 25% of the nominal power.

The power factor can be easily controlled, as the induction generator with a rotor cascade works similarly as a synchronous generator. These generators have a market share of 45%

in the variables speed drive market. The major drawback is the behaviour during grid faults and voltage sags. The lower grid voltage will produce an increase of the current, which affects the power electronics given the magnetic coupling between stator and rotor and might damage it [30].

In series connection of an AC/AC converter is shown in Fig. 2.13. The variable frequency AC power of the generator is injected into the fixed frequency network. Series connected systems have been built up to a power of 1.5MW. The converter and the filter needs to be rated at the nominal power of the turbine. The efficiency of such a system is lower than for doubly fed induction generators, therefore a highly efficient converter design is needed. The advantage of the series connection is the speed range of 0% to 100% of the nominal speed.

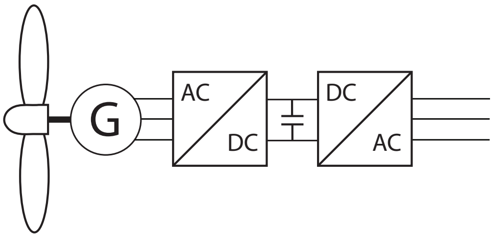


Figure 2.13: Full size converter in series

Wind Farms

The wind speed is generally more constant and higher offshore than onshore, up to an increase of 20% is possible [28]. As the yield of energy is proportional to the cube of the wind speed, almost 73% more energy can be collected offshore than onshore. The offshore wind is less turbulent, as the temperature difference is more moderate than onshore, resulting in less mechanical stress on the equipment.

However the drawback of an offshore wind farm is before all the cost of installation; the further away the farm and the deeper the water makes a big influence on the price. The towers are generally higher (if the submerged part is taken into account) than for onshore wind farms. The equipment should be adapted to face the harsh ocean conditions (Oil platforms are laid out for a life of 50 years, so the technology for appropriate technology exists). To reduce the installation cost, the weight and volume of the conversion system has to be reduced. Therefore, medium frequency converter technology could be an effective solution [31]. The weight and size of a 3MW 1.3kHz transformer is less than 8% of an 50Hz equivalent unit [32].

Onshore Wind Farms The largest wind farms are located onshore (2012). The 782MW Roscoe wind farm, the 735.5MW Horse Hollow wind farm and the 705MW

Tehachapi wind farm in the USA are among the largest wind farms in the world [33].

Offshore Wind Farms The biggest offshore wind farms reach a power level of almost 200MW and only a few produce more power, such as the Walney wind farm (367MW) and the Thanet wind farm (300MW) in the United Kingdom [33]. A lot of larger projects are in progress, for example the 500MW Greater Gabbard wind farm in the UK [34] or the 400MW BARD Offshore 1 wind farm in Germany [35]. 100km of cable offshore and 80km cables onshore are needed to connect the latter to the next grid connection point, which is illustrated in Fig. 2.14.

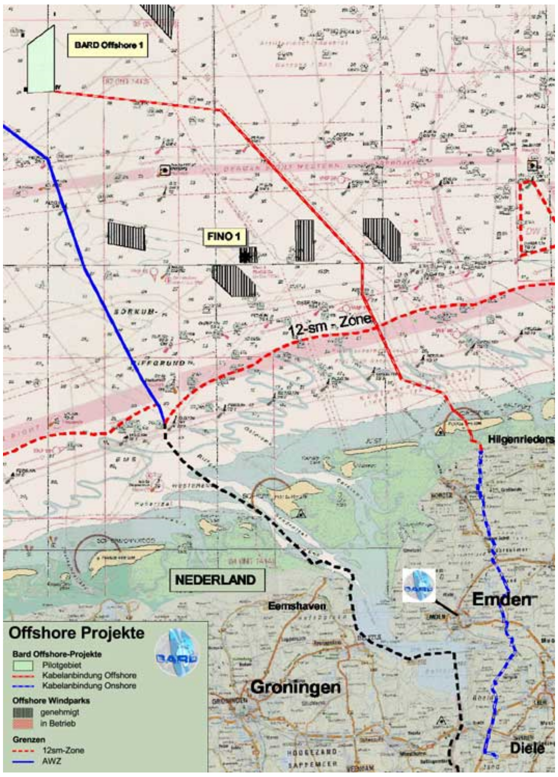

BARD Offshore 1
FINO 1
12-sm - Zone
Hilgenrieders
NEDERLAND
Eemshaven
Emden
Groningen
Diele
Offshore Projekte
Bard Offshore-Projekte
Pilotgebiet
Kabelanbindung Offshore
Kabelanbindung Onshore
Offshore Windparks
genehmigt
in Betrieb
Grenzen
12sm-Zone
AWZ

Figure 2.14: 400MW wind farm Bard Offshore 1 [35]

Two offshore wind farms using a VSC based HVDC technology are going to be built for transporting a power of 800MW (DolWin1, commissioning in 2013) and 900MW (DolWin2, commissioning in 2015) [36]. Several offshore projects with a Modular Multilevel Converter based HVDC transmission are announced [37], in order to connect to following wind parks to the German network:

- Borwin 1: 576MW, 85km offshore, to be commissioned in 2013
- Borwin 2: 800MW, 96km offshore, 200km cable, to be commissioned in 2013
- Sylwin1: 846MW, 210km cable, to be commissioned in 2014

- Helwin2: 690MW, 131km cable, to be commissioned in 2015

The clear tendency is to increase the wind farm size. Several projects are in the planning phase that face a total installed power of more than 500MW (for example the 1.2GW Triton Knoll wind farm and the 630MW London Array wind farm in connection with the round 2 policy of UK government [38] or the 960MW Innogy Nordsee 1 wind farm in Germany [39]). These wind farms are situated only a few kilometres offshore (40km for the Innogy Nordee 1, 24km for the London Array and 33km for the Triton Knoll wind farm).

Wind farms cannot be connected anywhere to the grid, especially large wind farms must be connected to a point where the onshore grid is strong enough. In some cases, the transmission distance is significantly extended and DC transmission could be more advantageous than AC transmission [40].

Voltage Levels In a conventional offshore wind farm based on AC, there are several voltage levels: 690V is generally the generation voltage of wind turbine with a power up to 2MW. Turbines with higher output power have higher voltages (Vestas 3MW 90V turbine generates 1000V [41]). The actual high power wind turbines such as the M5000 [42], propose a generator voltage of 3.3kV (5MW). Even 6.6kV (6.15MW) generators are used for high power wind turbines [43]. In general high voltage generators are an interesting alternative for turbines with a rated power higher than 3MW [44].

Firstly the voltage is elevated to 33kV (medium voltage) for the collection network and secondly to 150kV (high voltage) for the transmission[1]. The PCC is situated in the middle of the wind farm. The 33-150kV transformer is built on a platform, providing space to a number of other service facilities, like a helicopter platform.

The choice of the collection voltage levels is a compromise between losses and cost. The current capacity of the cables is between 1kA and 1.5kA. If the voltage is too low, the losses will be too high, but on the other hand high voltage equipment is expensive because of the additional space and isolation needed.

For an offshore application several points do favour the use of DC instead of AC:

- Fixed-speed turbines with induction generators require reactive power. When the active power increases, also the reactive power consumption increases. This is not a problem for variable speed turbines.
- The capacitive charging of high voltage AC transmission lines undersea is substantial to a point where longer distances cannot be covered by AC lines.

---

[1] These figures are from the BARD Offshore 1 wind farm, but are commonly used voltage levels [35]

- The cost for DC systems are actually higher than for AC systems. This is mainly due to the power converter and in particular to the semiconductors they contain. But the trend shows an increase of the power density and a decrease of the cost of these elements. This is also valid for AC technology which is advancing as well and reducing cost.
- The losses in the conversion stations are higher for DC, but this is compensated by smaller transmission losses.

Wind Farm Layouts

Most of the wind farms (onshore as well as offshore) are connected to a local collection network (33kV). Similar to Fig. 2.15, the different "strings" are merged at the PCC, where the voltage is elevated for transmission (typically 150kV). The wind farm operator is liable to assure that the voltage level, frequency and reactive power (for an AC interconnection) is adapted to meet the needs at the PCC.

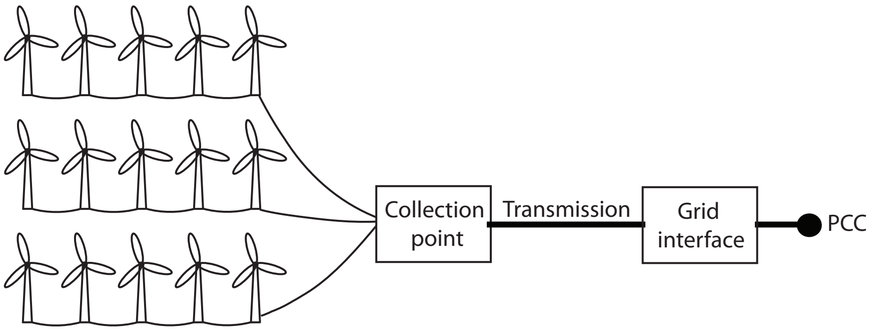


Figure 2.15: A representative scheme of a wind farm

It is very probable that wind farms bigger than 300MW are divided in clusters [12]. This implicates that the wind farm can be build in stages, producing power before the total accomplishment of the wind park. A modular approach is more reliable. Wind farms with 60MW are considered as small wind farms, since the effect of even smaller wind farms will be negligible from a grid operator point of view. As a rule of thumb the distance between the wind turbines is somewhere between 5 and 9 rotor diameters in the prevailing wind direction and 3 to 5 diameters in the direction perpendicular to the prevailing winds [45]. Therefore the energy density for a wind farm is generally low (around 5MW- 8MW per km^2). The turbulences created by a turbine can be important and result in an increased mechanical stress and energy loss for the turbine situated close to it.

The power of the turbines can be collected either in an radial or loop configuration [46], which is depicted in Fig. 2.16. Different layouts for wind farms are proposed in literature [12].

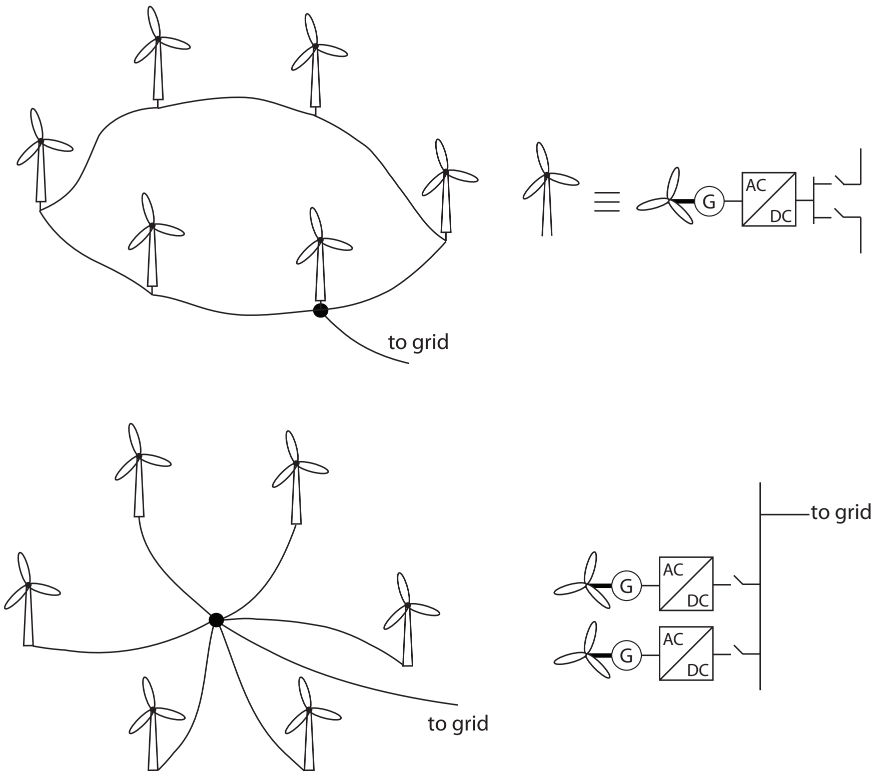


Figure 2.16: Connection layouts for wind farms

AC Collection for Wind Farms Almost all of the existing wind farms today use an AC collection network from the turbine to the grid. A typical wind power AC collection network is shown in Fig. 2.17.
The voltage level of the collection network is between 20kV and 35kV and the frequency 50Hz, so every turbine is equipped with the corresponding medium voltage transformer, to elevate the 690V output of the turbine to the medium voltage of the collection network. The transformer at the collection point elevates the voltage to the transmission voltage of 150kV. For an offshore wind farm, the transformer is placed on a platform.

Mixed AC/DC Collection for Wind Farms The power is collected with an AC medium voltage grid, similar to a pure AC collection network. In addition to the high voltage transformer there is a AC/DC converter rectifying the voltage to 150kVdc for the transmission, depicted in Fig. 2.18. The voltage of the local AC system is fully controllable, both in amplitude and frequency. It is possible to use a collective variable speed system for the whole wind farm in order to increase the efficiency. This topology, also known as HVDC transmission, is discussed widely and by various authors.

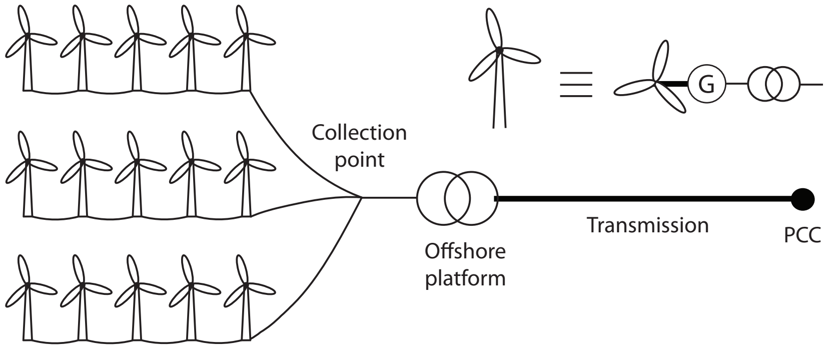


Figure 2.17: AC Collection network for wind farms

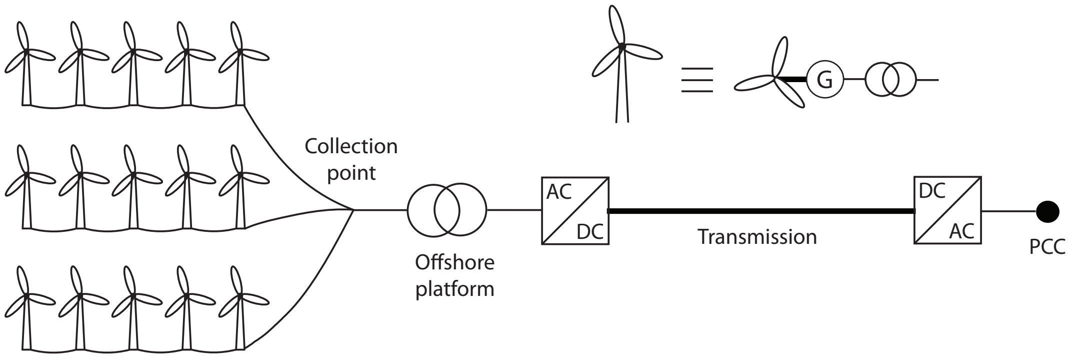


Figure 2.18: AC/DC collection network for wind farms

DC Collection: Parallel Connected Wind Turbines This topology is based on the AC collection grid with the only difference that the AC transformers are replaced by DC transformers. If the transformation ratio is high enough so that the turbine output voltage reaches 20-40kV, only a single transformation is used to elevate the voltage to the transmission level of 150kV. If the turbine output voltage is below 5kV, an additional DC/DC transformer is needed [12]. In Fig. 2.19 a topology with two transformation steps is depicted.

DC Collection: Series-Connected Wind Turbines Instead of increasing the voltage by the means of a DC transformer, the series-connected wind farm takes advantage out of series connection to reach the necessary voltage level for transmission [46]. Fig. 2.20 shows such a topology. Large wind farms can so be realised without any offshore platform carrying the equipment needed for preparing the transmission (DC or AC transformer). The drawback of such a topology is that if one of the turbines does not produce any power, the others need to compensate by increasing their output voltage.

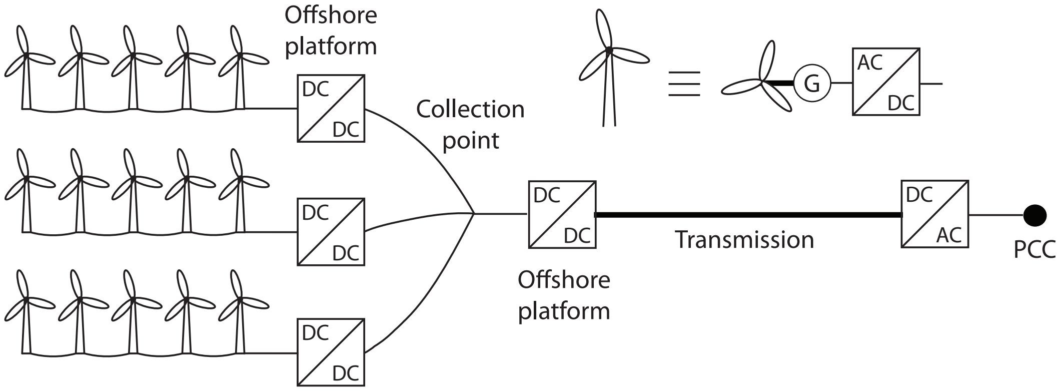


Figure 2.19: Parallel connected DC collection wind farm

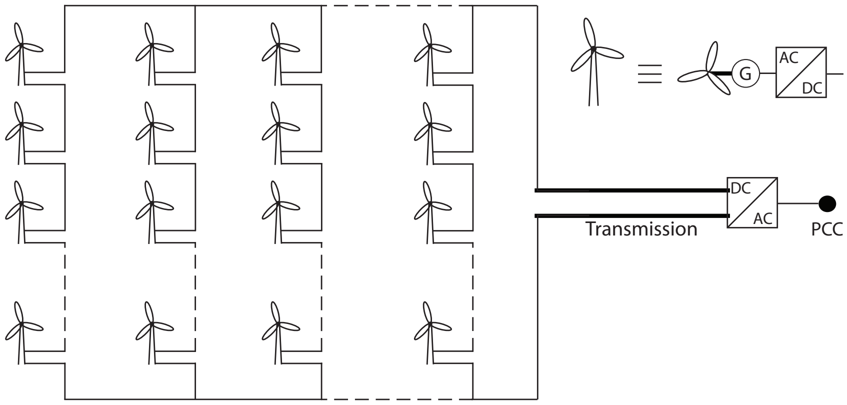


Figure 2.20: Series-connected DC collection wind farm

Case Study - Wind Power Collection Network

In this section, a collection network for distributed generation will be studied. As an example, the load flow of a 400MW offshore wind park, equipped with 5MW DFIG wind turbines will be analysed. The turbines are arranged in clusters of 8 turbines, which are linked to the step up platform, situated about 7km from each cluster, as depicted in Fig. 2.21. The cables are considered to be lying on the sea bed at a depth of 50m and the conductor temperature is 90°C when operational. The current rating depends on the permissible temperature inside the insulation. The parameters of the proposed wind farm are summarised in table 2.1.

Since cable laying cost is about 1-3 times the cost of the cable, depending on soil conditions, depth and length, three-core cables are going to be the preferred ones to reduce the installation cost [47]. The most significant difference between AC and DC in the context of submarine transmission is that AC cables have a high line capacitance and generate considerable reactive current. The buried cable itself acts as a long capacitor, and charging current is produced along its entire length, so the longer the cable, the

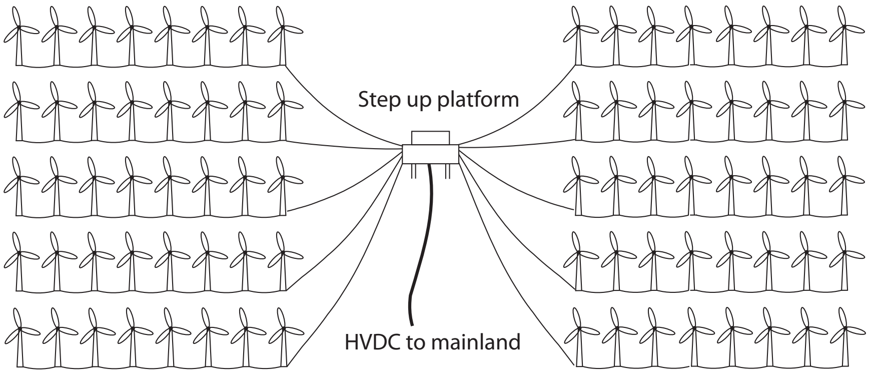


Figure 2.21: Layout for a 400MW wind farm

Table 2.1: Wind farm parameters

Wind farm power [MW]	400
Number of 5MW turbines	80
Rotor diameter [m]	120
Horizontal spacing [m]	840
Number of turbines per cluster	8
Number of clusters	10
Mean distance cluster- step up platform	7km
Power production density [MW/km^2]	7.01

more reactive energy is generated. Typical amounts of reactive energy are in the range of 100-150kVAR/km for 33kV XLPE cable and 1000kVAR/km for 132kV XLPE cable [14].

Although the use of HVDC converters leads to losses on either end, the DC system has lower overall losses above a certain cable length. The losses in the cable are significantly lower for DC cables because of the lack of both the charging currents in the main conductor and the induced current in the shielding. The additional reactive current not only reduces the active current-carrying capacity of the cable, but also requires a scheme to absorb the reactive current. For any length over about 10km, some form of reactive power compensation will be required [47]. A lot of publications discuss the efficiency of the power transport over long distances, considering both AC and DC transmission (HVAC, HVDC). The analysis will uniquely focus on the collection level that means on the medium voltage collection grid, linking the wind turbines to the voltage step-up station. Since a given cable can carry more power in DC than AC, a set of cables that now feeds a medium-sized AC wind farm could later be used for a DC wind farm four times the size if a converter is added along with more wind turbines [48]. Different generator topologies are considered, which behave differently in terms of reactive power generation:

- Full size converter, with $\cos\phi$ fully controllable
- DFIG with $\cos\phi = 0.9$ lagging or leading
- Induction generator with $\cos\phi = 0.8$ leading

The AC and DC load flow analysis is based on the Newton-Raphson algorithm. The results for the analysis are summarised in Table 2.2. The active losses in a DC system are about 3 times lower than for any configuration based on AC. Additionally the reactive losses in the AC system further increases the current in the cables which might in some cases require higher cable diameters.

Power factor	$Q_{turbine}$	P_{losses}	Q_{losses}	Voltage variation
1	0MVar	8.2687MW	7.0194MVar	33- 33.5kV
0.9 leading	2.4MVar	9.9261MW	9.5149MVar	33- 34.5kV
0.9 lagging	-2.4MVar	10.4494MW	10.5172MVar	33- 33.3kV
0.8 leading	3.75MVar	12.4152MW	13.3524MVar	33- 34.9kV
DC collection	0MVar	3.1854MW	0	53.9kV- 54.5kV

Table 2.2: Results of the wind farm power flow

2.2.2 Solar Power

Photovoltaic power is a way of producing electrical energy from the sun, without passing by electromechanical or thermal means. The annual production of photovoltaic cells has increased 60% in 2007 [49]. During the last five years, annual growth in average was over 40%. Collection networks are only becoming interesting from a certain power level on, since most residential grid-connected PV installations do feed the energy directly into the AC network.

The actually largest solar plants are the Gujarat solar park in India (214MW) and the Golmud solar park in China (200MW). Gigantic photovoltaic power plants are planned, such as the 800 MW photovoltaic power planed by PG&E in California, USA (finishing 2013) [50] or the 1GW plant in Qaidam Bassin, China (starting 2009) [51]. In order to manage such big quantities of power, high voltage is going to be used for power collection and transport.
Another concept is to build offshore solar plants, similar to the concept of "Solar Islands" by the CSEM [52]. The platform is orientable towards the sun, increasing thus the efficiency by around 15%. In the case of the solar island, steam is produced and then transported onshore to be transformed into electricity by a steam power plant. The same concept could be used for photovoltaic, using offshore photovoltaic energy production

and transporting it to the mainland with the help of underwater cables. Not only offshore is a lot of available place, but also in the deserts or arid regions, that offer abundant sun irradiation. Very large scale photovoltaic power generation (VLS-PV) systems are considered to be built in these regions [53]. Another concept is the Desertec project [54]. If only 10% of the Sahara is covered with solar panels, the worldwide energy consumption is covered. However more than on the technical side, the problems are of political nature.

PV Modules

The efficiency of the most current PV technologies is summarised in table 2.3 [55]. The market share of wafer-based PV is 87% in 2007.

Wafer-based		Thin film		
Mono crys.	Multi cryst.	α -Si	CdTe	CIGS
15-18% (25%)	14% (42%)	7%	13% (18%)	(19.9%)

Table 2.3: Typical efficiencies of the most common PV technologies (in brackets record efficiencies)

PV cells are usually connected together to make PV modules, consisting of 36 or 72 PV cells, which generates a DC voltage between 23V and 45V and have a power between 100W and 200W, depending on temperature and solar irradiation.

Collection Networks

In the past, the photovoltaic power injection into the grid was based on centralised inverters. A typical topology is shown in Fig. 2.22a), where a large number of series connected panels are summarised to a string to achieve a high voltage. Several strings are connected in parallel to reach higher power levels. This topology has some considerable drawbacks [56]:

- Mismatching losses (not every panel has identical parameters and solar irradiation)
- Poor expandability
- High DC voltages between the panels
- Losses in string diodes
- Use of thyristor inverters cause harmonics and reactive energy

Responding to these limitations, a more modular technology was introduced. The string technology from Fig. 2.22b), a compromise between single panels interfaces and centralised inverter, is introduced in the mid 1990’s, leading to cost reduction, reliability improvement and design simplification. For each string a separate maximum power point tracking (MPPT) can be applied, improving the system efficiency.

For European countries, up to 16 panels are series connected to form a string in order to reach 450V- 510V for normal working conditions. The open circuit voltage can reach up to 720V [57], so it is necessary to use high voltage rated components, with poor utilisation. It is also possible to adjust the DC voltage using an additional DC/DC converter.
A future development is the multi-string inverter [58], depicted in 2.22c). Several strings are connected to an inverter by the means of a DC/DC converter. This has several advantages, such as per-string Maximum Power Point Tracking (MPPT) control and the flexibility of extension of the plant. Another strategy is to equip each solar panel with a converter shown in Fig. 2.22d), achieving a MPPT for each panel.

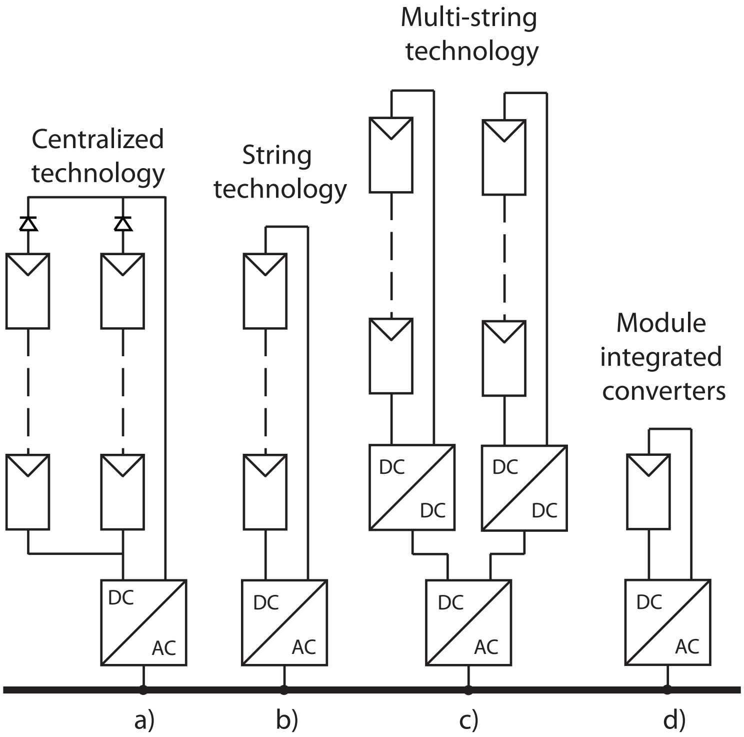


Figure 2.22: Past, present and future collection networks [58]

The energy density of photovoltaic plants is low (around 100MW-200MW per km^2) compared to wind power without taking into account the availability. For large photovoltaic plants the voltage level for the collection necessarily needs to be very high, in order to reduce the conduction losses over large distances. At the same time the number of conversion stages should be low to keep overall efficiency high.

In Fig. 2.23a) a DC based collection grid is depicted. The DC/DC converter connecting the string to the DC-bus should be able to elevate the voltage considerably. The nominal string output voltage is low voltage (around 500V, depending on the number of panels in series) and an ideal output voltage should be several kV. Bidirectional power flow is not explicitly necessary.

A second proposition uses module integrated converters to elevate the DC output voltage of the single panel by the means of non-isolated DC/DC converter in Fig. 2.23b) [59]. This has the advantage of respecting the MPPT of every single panel (statistically, there is a mismatch of 2.5% for open-voltage and short-circuit current for panels of the same type [60]). Protection strategies can be followed on a per-panel-basis and redundancy in case of errors are only some of the advantages [59].

To reach even higher voltage levels, the DC/DC converter are put in series, as depicted in Fig. 2.23b), and then introduced to the DC collection circuit.

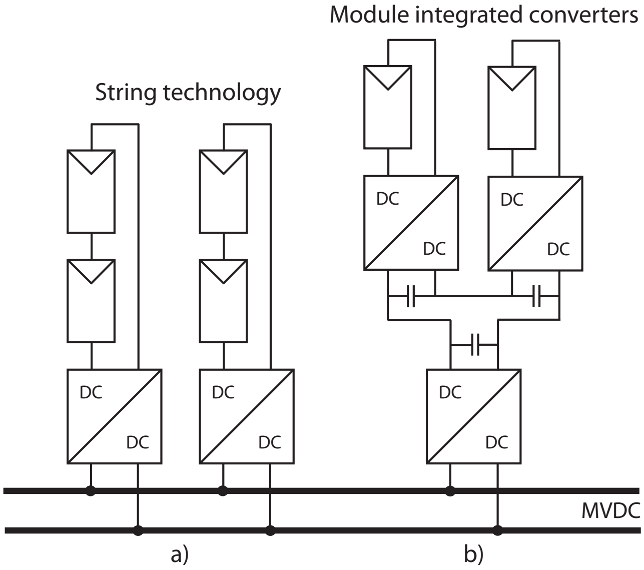


Figure 2.23: DC collection bus: a) String technology b) Module integrated converters

Totally new topologies for the interconnection of PV panels can be thought of by using multilevel converters. The proposed scheme in Fig. 2.24a) takes advantage out of the innate properties of the Neutral Point Clamped converter (NPC). The converter is able to control the voltage level of the two PV-strings independently and makes a closer maximum power point tracking possible. An AC version has been proposed in [61]. The boost multilevel converter in Fig. 2.24b) is another possible multilevel topology among others [59, 62].

Case Study - Solar Collection Network

A rather futuristic idea of producing electrical energy would be covering Itaipu hoover dam with solar panels. For an example a part of the surface of the lake will be covered with solar cells of 10% efficiency. The lake of Itaipu has an average surface of $13500km^2$.

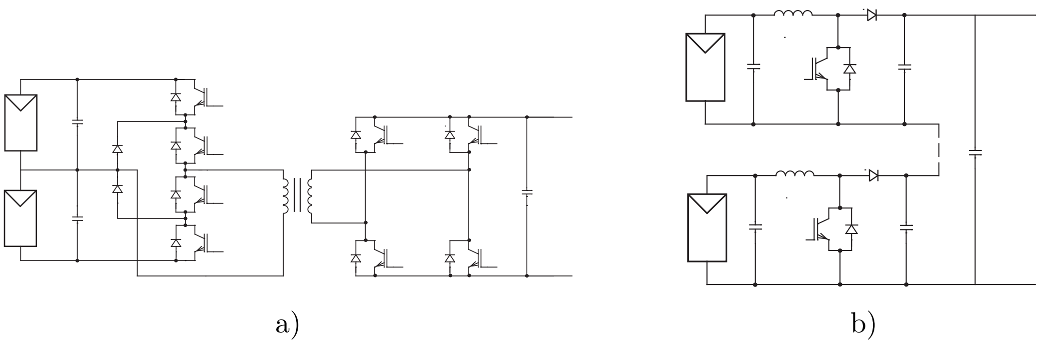


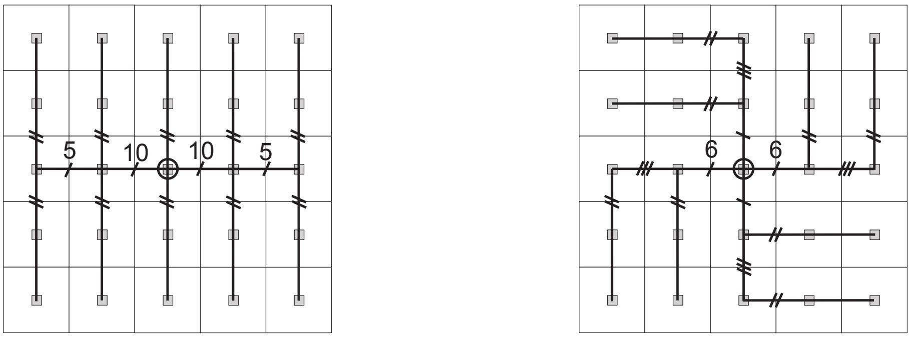
Figure 2.24: Example of use of multilevel converters with solar panels a) NPC converter b) Boost converter

If only 10% of the surface is covered, the resultant PV power plant would produce 13.5 GW, as much as the hydraulic energy production of the dam. However if we compare the annual energy yield we get for the PV plant 27600GWh/year, whereas for the hydro plant 95000GWh/year.

Table 2.4: PV power plant parameters

Power	13.5GW
Area	$1350km^2$
Energy production density $[MW/km^2]$	100
Mean daily solar isolation $[Wh/m^2]$	5600 [63]
MV collection cell power [MW]	6
MV cell size $[km^2]$	0.6
MV collection cluster power [MW]	150
MV cluster size $[km^2]$	1.56
Mean distance from cell to next HV connection [m]	600
Cable length per MV cluster [km]	15
Number of clusters	90

The parameter of such a plant are summarised in table 2.4. Fig. 2.25a) and 2.25b) show two possible layouts for the medium voltage collection network. A modular approach has been adopted in order to assure reproducibility and a more reliable behaviour in case of out-takes.
The results of the load flow is summarised in Table 2.5. Again the active losses in the DC collection system are approximately 3 times lower than the losses in an AC collection system.



a) b)

Figure 2.25: a) Radial PV plant b) Distributed PV plant

Table 2.5: Load flow analysis for the PV plant

Topology	$Q_{turbine}$	P_{losses}	Q_{losses}	Voltage variation
Radial AC	0MVar	19.6MW	52.7MVar	33kV- 33.8kV
Radial DC	0MVar	7.35MW	0 MVar	53.88kV- 53.93kV
Distributed AC	0MVar	23.44MW	12MVar	33kV- 33.09kV
Distributed DC	0MVar	8.81MW	0MVar	53.88kV- 53.94kV

2.2.3 Urban DC Distribution

In a somewhat greater extent than a microgrid, an urban DC distribution can be imagined, such as depicted in Fig. 2.26 [64]. In a city most of the transmission and distribution network is built underground for safety and environmental issues. The increasing energy need of today's society requires more transportable energy. The use of a DC instead of an AC distribution system can enhance the power transport capacity as much as by a factor 10 for a given 3 line system [19].

An urban DC distribution would ease the integration of renewable energies, DC energy producing units (micro-turbines, fuel cells) and storage systems. HVDC city in-feeders can be used to supply the city centre [65], eliminating the need of overhead transmission lines. DC power can even go down to the low voltage level, since many loads in a household are DC loads. Lightning, Switched-Mode Power Supply (SMPS), electric baseboard, water heating units and UPS can be directly fed by a DC power supply and thus eliminating conversion losses from AC to DC. However, the bigger share of the electrical consumption is due to motors (freezer, laundry machine) which need to be driven with AC. Using variable frequency drives allows to work in the optimal operating condition and so contribute to energy savings up to 10% [66]. Considerable research was done on LVDC systems [3, 7], but they are mainly on laboratory level.

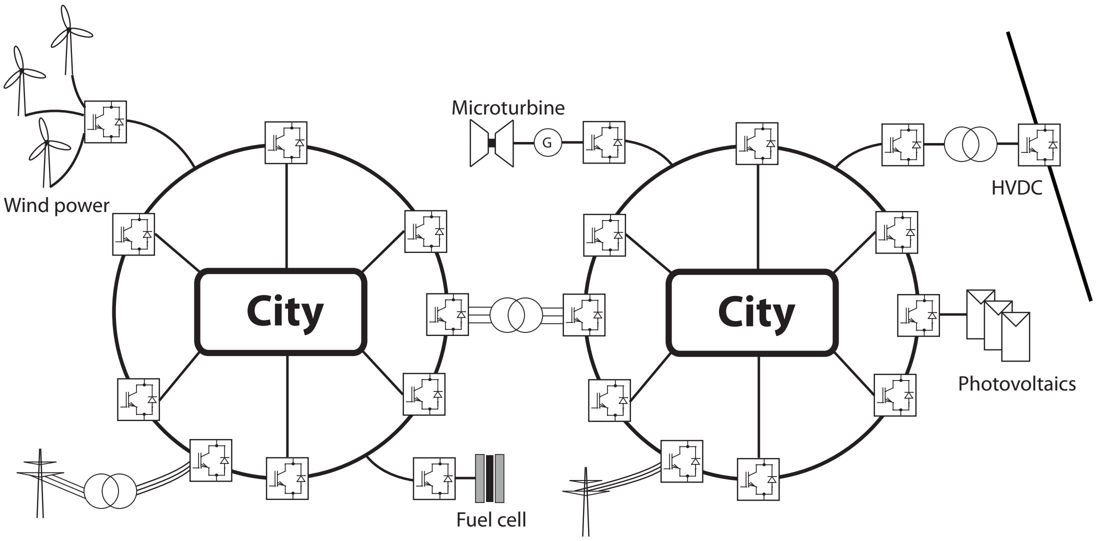


Figure 2.26: Urban DC distribution [64]

Case Study - MV Network of a City

The electrical network of a city can be separated into LV consumer level, MV distribution level, HV transmission level. Since the investment in infrastructure is very important, the following analysis will be based on the already existing line parameters for an AC distribution. A small size city (150'000 inhabitants) is being considered in this analysis, as for example the city of Lausanne. Typical network data for an urban core is given in Table 2.6.

Table 2.6: MV network for small size city

MV load density	$31 MWh/km^2$
Connection point density of MV/LV network stations	$55/km^2$
Mean distance between connections of the MV network	0.20km
Line length for MV network	$14.75 km/km^2$
Voltage level	20kV
Total active load	124MW
Total reactive load	62MVar
Number of HV/MV transformers	4
Number of main consumers	31
Number of 450A lines	25
Number of 200A lines	50
Medium distance between connection points	700m

A simplified connection layout has been adopted, shown in Fig. 2.27.
The line parameters of for 20kV distribution lines are given in Table 2.7. Three-core underground cables are used with aluminium cores due to financial reasons.
The results of the analysis are depicted in Table 2.8. The load flow analysis shows clearly that the DC based network is more efficient, in the present case a factor 10 less losses can be expected, without considering the increased current due to the reactive power that needs to be injected in the AC based network.

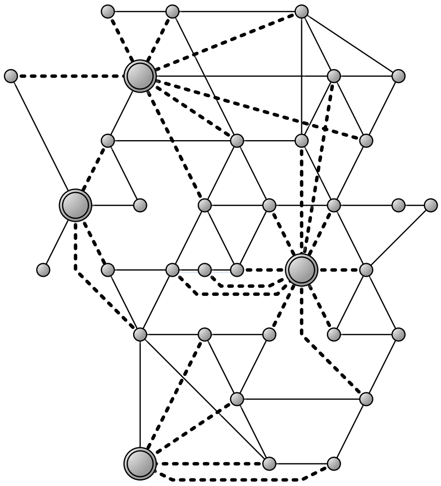


Figure 2.27: MV network of a city

Table 2.7: Line component data for 20kV underground lines

	AL 70	AL 300
Rated current [A]	212	474
Resistance at 20 °C [Ω/phase,km]	0.443	0.1
Resistance at 90 °C [Ω/phase,km]	0.568	.13
Reactance [Ω,km]	0.123	0.09
Capacitance [μF/km]	0.19	0.33

Table 2.8: Results of the load flow analysis for a city

Topology	P_{losses}	Q_{losses}	Voltage variation
AC	0.96413MW	-1.47MVar	20kV- 20.13kV
DC	0.08945MW	0MVar	39.95kV- 40.05kV

2.2.4 Conclusions

The three case studies for a DC collection and distribution grid show the advantage of using DC in order to decrease the active losses and to eliminate the reactive losses. The load flow calculations have been based on the fact that the same cables are used for AC and DC networks and that the isolation of the cables can support the higher DC voltage, which is equal to the peak voltage in the AC system. The losses in the conversion stages where the voltage level is adapted are not considered. Normally these losses are more important in DC systems, which could change the overall conclusion of this chapter. The DC/DC converter is the most crucial device in a DC grid and should be designed carefully in order to reach high efficiencies.

3 Means of Power Electronic Interfaces between HV, MV and LV

> "At the beginning of the 21th century DC/DC converter technology is not yet able to cope with high powers in the order of some megawatts. Losses and cost were also to high to have a significant impact on the market [48]."

3.1 Requirements for DC Networks

As it comes out of the load flow analysis in section 2.2, a DC distribution grid can often be more advantageous than the same grid exploited in AC. This analysis however does not take into account conversion stages that adapt the voltage levels between transmission, distribution and consumption. In an AC network it is the line frequency transformer at 50Hz/60Hz which adapts the voltages. Distribution transformers typically have efficiencies higher than 98%, which should be a benchmark also for alternative DC technologies, when the citation at the beginning of the chapter should be contradicted. For DC networks voltage elevation is achieved with the help of converters, either by using an AC link transformer elevating the voltage or by a series-parallel connection of the input and output.

Since the voltage levels in medium and high voltage exceed the semiconductor blocking rating, either a series connection of semiconductors or the use of multilevel converter is advisable. In addition, if a modular structure is used, the converter can easily be up-scaled to the desired power and voltage level.
On the other hand, for high powers a low frequency transformer presents a considerable investment in copper and core material. DC technology can reduce the raw material use with the help of MF galvanic isolation. As shown in section 7.1, the volume or mass of the transformer is almost inversely proportional to the frequency, so a 1MVA medium frequency transformer at 4kHz has an estimated weight of about 150kg [67], whereas the weight for a 1MVA transformer at 50Hz is about 3 tons. Another point in favour of the DC based grid is the fact that the power flow can be controlled directly and accurately,

which could prove indispensable for future electricity networks.

In order to make DC technology worthwhile to be introduced, it must have some improvements over the conventional AC systems, where the different elements are standardised and produced in big quantities. As already mentioned, the main elements of DC distribution systems are the DC transformers which should have at least the following characteristics:

- High transformation ratio (high step up or step down capability)
- Very high efficiency >98%, even at partial load
- High reliability
- Galvanic Isolation
- Redundancy
- Use of standard components

An extended list of properties can be established, which is well suited in the case where semiconductor technology is applied.

- High flexibility in power flow control with bi-directionality
- Protection possibilities
- Modularity and multi-system compatibility
- Low component stress

In this chapter power flow reversible converter configuration will be analysed, suited for an effective voltage level adaptation between the LV, MV and HV circuits. Galvanic isolation will be provided by MF transformers. A significant benefit regarding cost and size is discernible, when the switching frequency is high enough to use amorphous or nano-crystalline core material effectively (close to saturation level without overheating problems, even if the price is high compared to ferrite) [68].
Generally the galvanic isolation requires a structure as depicted in Fig. 3.1, consisting of two converters and an AC isolation stage. Within this chapter, converter topologies based on this principle are listed.

Since parameters such as efficiency (at full and partial load) and cost depend much on the optimisation of a given converter. This chapter intends to give an overview of the different technologies. A high voltage transformation ratio is important, since the field of application is the interconnection between the HV, MV and LV electricity networks.

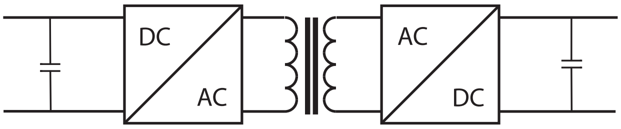


Figure 3.1: General structure of an isolated converter

3.2 Conventional Converters

3.2.1 Dual Active Bridge Converter

The Dual Active Bridge (DAB) converter [69], depicted in Fig. 3.2, is one of the most commonly used DC/DC converters [70–72]. In most cases it is operated at constant frequency under a pulse width control strategy. The converter has small voltage and current stress in the devices and little reactive power circulation between the H-bridges leads to lower transformer current rating and low output voltage ripple. This converter uses the leakage inductance L_σ of the transformer for the main energy transfer. Two square waves are phase-shifted by an angle δ in order to control the desired output power. Power is delivered by the side with the leading square wave. As it is shown later, this converter proposes also soft-switching within restricted working conditions. This converter can achieve both voltage step-up and voltage step-down, but in order to stay within the soft-switching region, there will be no voltage elevation or reduction.

With the two-level square wave modulation, the load range is restricted to 40-100%. Either the transformer leakage inductance is decreased, the switching frequency reduced or additional free-wheeling states are introduced, thus becoming a three-level square wave modulation [73].

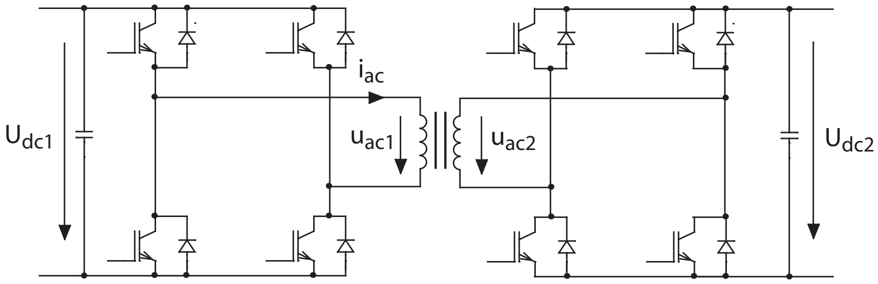
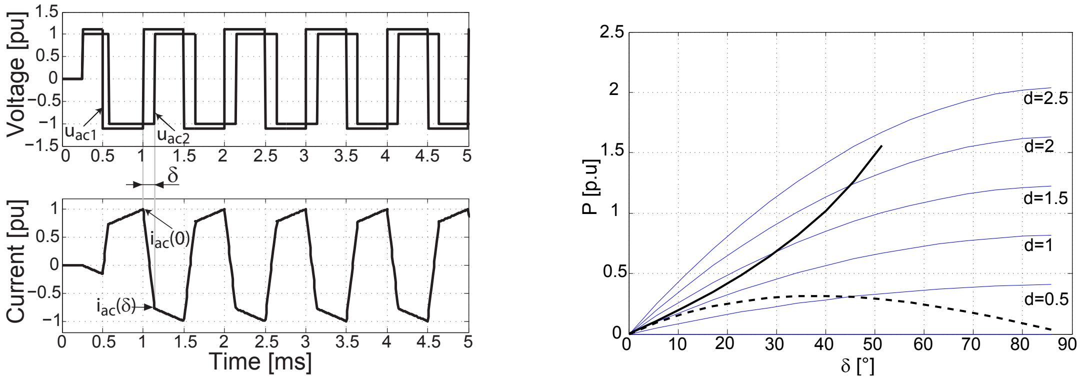


Figure 3.2: Double active bridge converter

There is the possibility to drive the DAB with variable frequency. This mode is not advised, since for a wide load range the frequency varies considerably and the transformer will not be optimised any more [74].

Soft-Switching of the DAB

In dependence of the phase angle θ, two cases can be distinguished, defined in (3.1) and (3.2).



a) b)

Figure 3.3: a) Current and voltage waveform of the transformer in a DAB b) Soft-switching boundaries

$$i_{ac}(\theta) = \left(\frac{U_{dc1} + U_{dc2}}{\omega L_\sigma}\right)\theta + i(0) \text{ for } 0 \leq \theta \leq \delta \tag{3.1}$$

$$i_{ac}(\theta) = \left(\frac{U_{dc1} - U_{dc2}}{\omega L_\sigma}\right)(\theta - \delta) + i(\delta) \text{ for } \delta \leq \theta \leq \pi \tag{3.2}$$

With the condition $i(\pi) = -i(0)$, the initial conditions $i(\delta)$ and $i(0)$, indicated in Fig. 3.3a) can be determined:

$$i_{ac}(0) = \frac{U_{dc2}}{2\omega L_\sigma}(\pi - 2\delta) - \frac{U_{dc1}}{2\omega L_\sigma}\pi \tag{3.3}$$

$$i_{ac}(\delta) = \left(\frac{U_{dc2} - U_{dc1}}{2\omega L_\sigma}\right)\pi + \frac{U_{dc1}\omega L_\sigma}{\delta} \tag{3.4}$$

Soft-switching is achieved with the condition $i_{ac}(0) \leq 0$ for the lower boundary and $i(\delta) \geq 0$ for the upper boundary, shown in Fig. 3.3b). These conditions do have an impact on the ratio of the voltages $d = U_{dc2}/U_{dc1}$. In order to maintain soft-switching over a wide load range, $d = 1$ is chosen.

$$d \leq \frac{\pi}{\pi - 2\delta} \tag{3.5}$$

$$d \geq 1 - \frac{2\delta}{\pi} \tag{3.6}$$

The magnetising inductance L_m has also an impact on the soft-switching region. The lower the magnetising inductance the bigger the soft-switching region which can be observed in Fig. 3.4a). The load appears more lagging, which is a precondition for Zero Voltage Switching (ZVS). However the transformer utilisation is poorer for a smaller magnetising inductance [70].

The snubber capacitor influences also the soft-switching region as it can be seen in Fig. 3.4b). The soft-switching region is depicted for two cases, for $\omega_n = \infty$ and $\omega_n = 10$. ω_n relates the snubber capacitor value to the leakage inductance L_σ and the switching frequency ω:

$$\omega_n = \frac{\omega}{\sqrt{L_\sigma C}} \tag{3.7}$$

The larger the snubber capacitor (low ω_n), the more restricted is the soft-switching region [73], but the lower the switching losses.

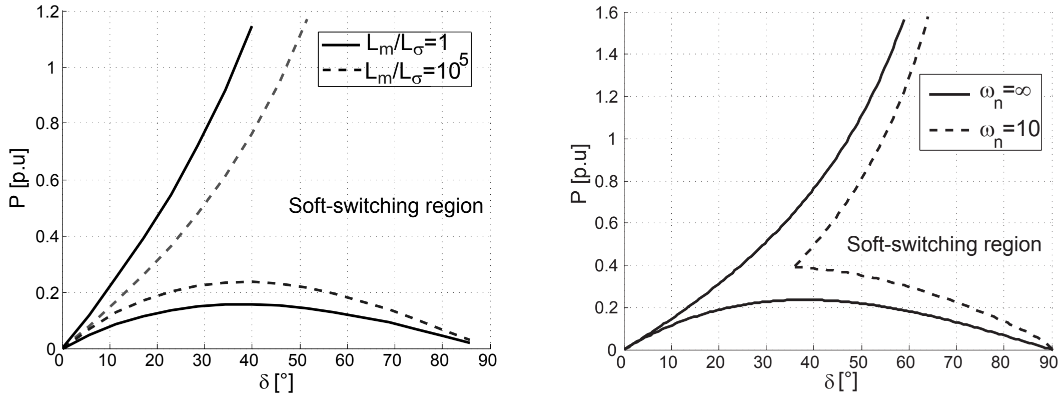


Figure 3.4: a) Influence of L_m b) Effect of the snubber capacitor

The effect of the snubber capacitor and the magnetising inductance does somehow compensate each other. For a proper design of the DAB, both parameters need to be chosen carefully.

3.2.2 Resonant Converters

In order to reduce the switching losses in the H-bridge, a resonant tank can be introduced into the DAB converter. Depending on the type and frequency of the resonant tank either Zero Current Switching (ZCS) or ZVS can be achieved [69, 75].

Resonant converters feed sinusoidal currents into the transformer, thus reducing copper and core losses because there are no high frequency harmonics inserted into the windings. This converter needs a large resonant capacitor and a large resonant inductor that must process all the power as well as circulate additional reactive power (The inductor kVA rating is typically 3 times the power delivered) [76]. The transformer is a part of the resonant tank resulting in a higher peak voltage, as well as a higher peak current for the transformer. This has an important effect when it comes to the design, because the converter and its components need to support higher voltages and currents, up to 3 times more as for the DAB for equal power ratings [77].

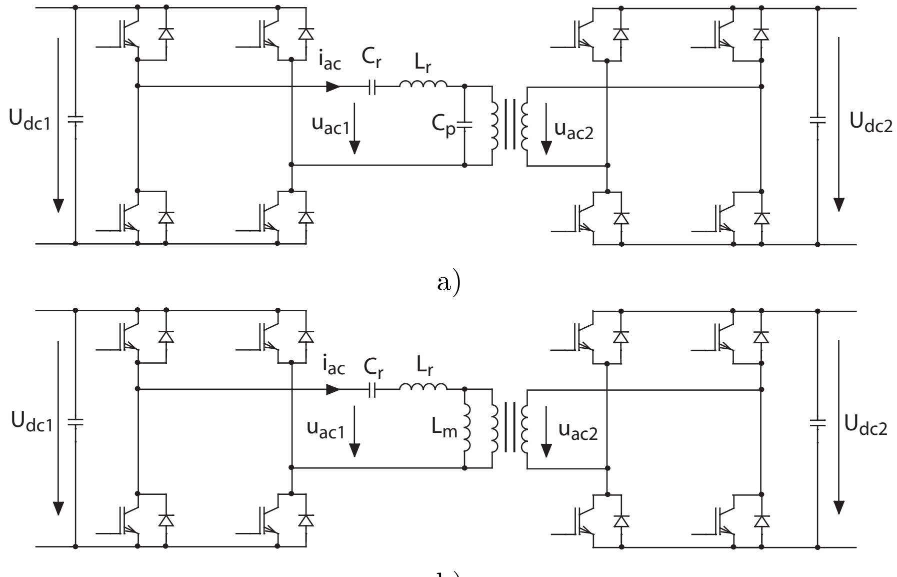
The power is controlled with the frequency; for a wide range of power, a wide range of frequency is necessary, which makes the dimensioning of the passive components quite difficult. Variable switching frequency can be a significant drawback in systems with several resonant converters. The converters cannot be synchronised since switching frequency depend on their loads. It may happen that different switching frequencies generate low-frequency beat harmonics that are hard to filter. Especially at low load there are large ripple currents at the input and output [78].

The Series Resonant Converter (SRC) converter has a capacitor on its primary side which acts as a DC blocking capacitor making the current decrease when the load decreases. The disadvantage of the SRC is that the output voltage cannot be controlled at no load and the output filter capacitors is subject to high ripple currents. The Parallel Resonant Converter (PRC) is able to control the voltage at light load by having its switching frequency adjusted above the resonance frequency. However the current in the switches is independent of the load, leading to low efficiency at light load.

Out of the different types of resonant converters (SRC and PRC), the Series Parallel Resonant Converter or LCC (SPRC) or 3th order resonant converter based on one inductance and two capacitors (LCC), illustrated in Fig. 3.5a) seems to combine the advantages of both (inherent short circuit protection due to the series connection of the capacitor (SRC) and control of the voltage at no load (PRC)) and eliminates the main disadvantages (independence of the current on the load (PRC)) [77].

The leakage inductance cannot be implemented directly into the transformer because the second resonant capacitor needs to be in parallel with the transformer. Since transformers are not ideal devices, the leakage inductance has to be taken into account. The 3th order resonant converter based on two inductances and one capacitor (LLC) converter, shown in Fig. 3.5b) acquits oneself of the design limitation of the LCC. The magnetising and leakage inductance are participating in the resonance phenomena as parallel and series inductance [75].

Resonant converters (SRC, PRC, LCC, LLC) are not attractive at high power levels due to the difficulty of implementing a compact, high efficiency resonant inductor that must process the entire load power [76].



a)

b)

Figure 3.5: a) LCC converter b) LLC converter

3.3 Multilevel Converters

The main interest of using Multilevel Converter (MLC) in high power application is the multilevel waveform output with low harmonic content, the ability to reach higher voltages due to the "pseudo" series connection of semiconductors and the high availability, using for example redundant elements within the converter. For DC/DC applications, instead of the high output voltage resolution, a high voltage elevation ratio (from input to output) is desirable. Some multilevel converters are very well adapted for this task. In addition, the modular architecture of some of these converters allow to scale to any desired voltage and power level. Galvanic isolation is a necessary condition and the transformer demands a compulsory AC intermediate stage.

There are many multilevel converter topologies: the NPC, the Flying Capacitor converter (FLC), the Stacked Multi-Cell converter (SMC) to cite some of them. In this section only one concrete example of an isolated converter using the NPC technology is presented, that is particularly interesting. This topology is able to support an output voltage which is higher than the blocking voltage of a single device, without taking to a delicate synchronisation of series-connected semiconductors. The topology is shown in Fig. 3.6 [79, 80].

The converter consists of an H-bridge on the low voltage side and an NPC converter on the high voltage side. In respect to the conventional DAB converter, using the NPC inverter allows to double the transformer voltage. Using standard 6.5kV Insulated Gate Bipolar Transistor (IGBT) devices, voltages up to 6.6kV can be attained.

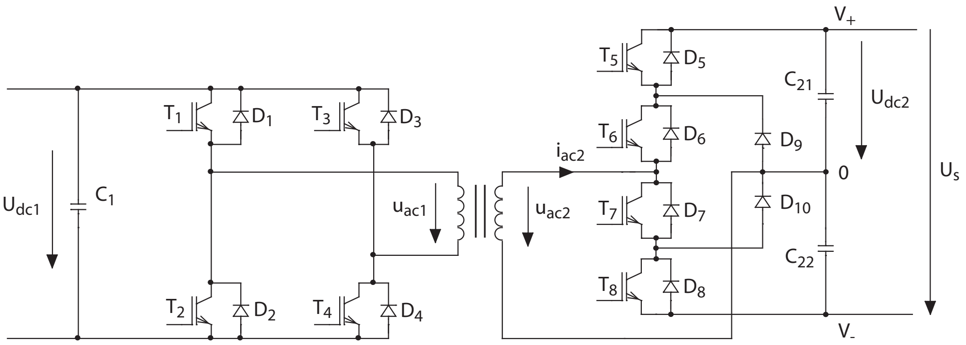


Figure 3.6: Isolated NPC converter

3.3.1 Cascaded Converters

Basically the idea of cascaded converters is to have floating voltage sources (due to galvanic isolation) that can be connected together to form a higher output voltage or a higher current rating [81]. The cascaded converter has a modular construction and there is no limitation on the number of levels except for insulation, in contrast to the other multilevel topologies. The harmonic content of the output can be decreased considerably by adding more levels in a phase-shifted way. The performance of the converter is much dependent on the performance of a single converter block. In the literature several topologies have been proposed for the use in the AC MV grid [71, 82], which can be modified for the use in DC grids according Fig. 3.7a). By connecting converters in parallel at the input and in series at the output a high voltage elevation ratio can be achieved without passing by a transformer. Due to the modular configuration, the different phases can be standardised and the cost can be reduced. The number of levels can be increased and provide the desired power and voltage rating.

In contrast to a topology where a single converter is managing all the power, in the series-parallel connected converters the power is equally shared by all the levels. Due to their modularity, semiconductors with lower blocking rating (<6.5kV) can be used even for applications in the medium voltage field (up to 30kV). The transistors are in series to support the higher voltage and as long the DC voltage of the capacitor is controlled, they won't be exposed to high voltage. Redundancy is given with the help of an additional switch that can bypass the faulty level.

A large number of MF transformers however are less advantageous than having one central MF transformer in terms of weight and required space. Examples of the series parallel connected converter can be found in [83, 84]. A modified version, called the multi-winding transformer is presented in Fig. 3.7b) [81, 85].
Instead of using a hard-switched topology as the DAB for the isolation stage, it could be considered to use a resonant topology for the isolation [86, 87].

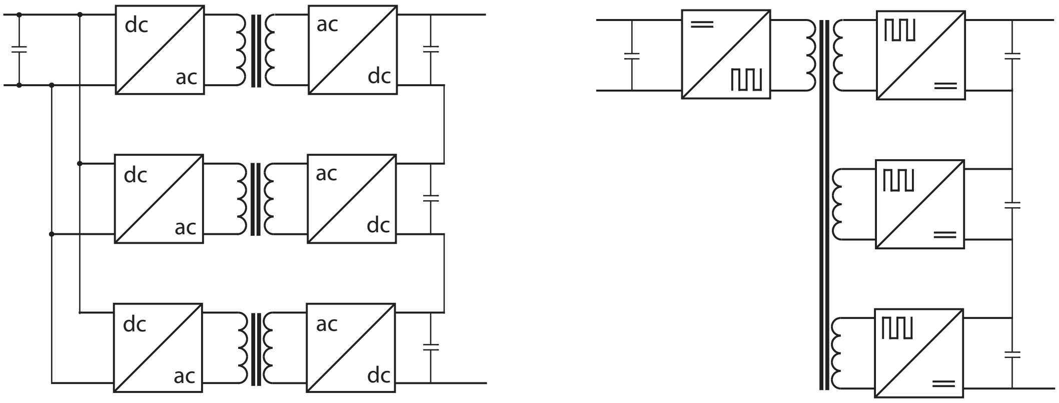


Figure 3.7: a) Series-parallel connection b) Multi-winding transformer

Instead of using a hard-switched topology as the DAB for the isolation stage, it could be considered to use a resonant topology for the isolation [86, 87].

3.4 Conclusion

When working with high voltages and high currents, often IGBT are put in series or parallel. The synchronous switching of semiconductors is not as simple to handle and alimenting the different gate drivers often requires a power supply isolated against high potentials. Therefore the multilevel approach seems to be an effective solution, since distributed capacitors equalise the semiconductor voltage stress and the driver can be supplied from this very same capacitor.

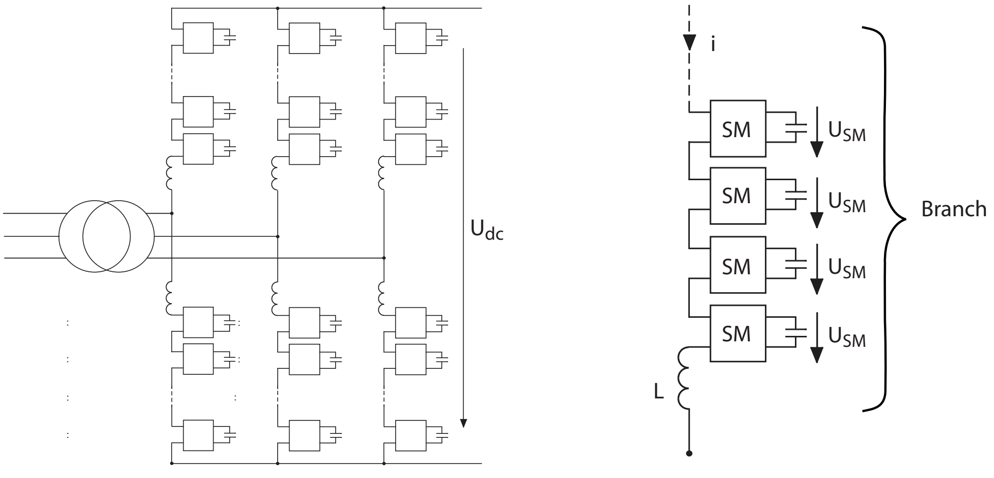
This work focusses on flexible solutions, allowing a high voltage conversion ratio with high efficiency. Solutions based on the FLC, NPC, SMC are not easily scalable, unless they are used in a series-parallel configuration, such as depicted in section 3.3.1. Furthermore, to assure a highly reliable system, a certain degree of redundancy is advisable. For the series-parallel structure redundancy can be introduced by adding additional switches and levels.

The main drawback of the converters presented in this chapter is their protection capability. The presented designs increase the short-circuit power due to the output and input capacitor. In case of a short circuit or inappropriate control, the energy contained in the capacitor will be consumed and the system needs to support a high short circuit current if no protection actions are taken within a short time delay. Circuit breakers in the MV or HV level are either very costly or they don't exist yet. In chapter 5, a topology based on a modular topology will be introduced, which will overcome the limitation of the state of the art converters.

4 Modular Multilevel Converter

In [88], a modular multilevel converter, also known as MMC, M2C or M2LC has been introduced. The MMC is linked to the idea of chain converters [89], typically used for Static Compensator (STATCOM) or even for UPS devices [90]. Only few examples exist in industry today, but it is an emerging technology. A first commercially exploited MMC has been built in the USA in 2010, realising a point-to-point HVDC connection [37].

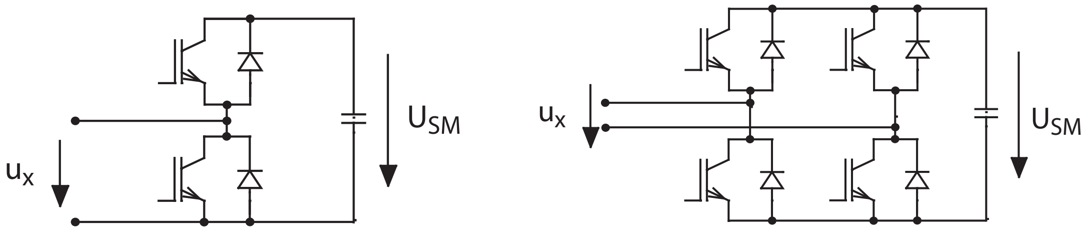
This section intends to give a review of the actual state of the art of MMC technology. In Fig. 4.1a) a conventional three phase MMC is shown. Typical applications of this converter are in the context of a 50/60Hz grid for an AC/DC conversion. Each phase leg has an upper and lower branch, illustrated in Fig. 4.1b), which consists of a series connection of N identical submodules and a branch inductance.



a) b)

Figure 4.1: a) Conventional 3 phase MMC b) An MMC branch

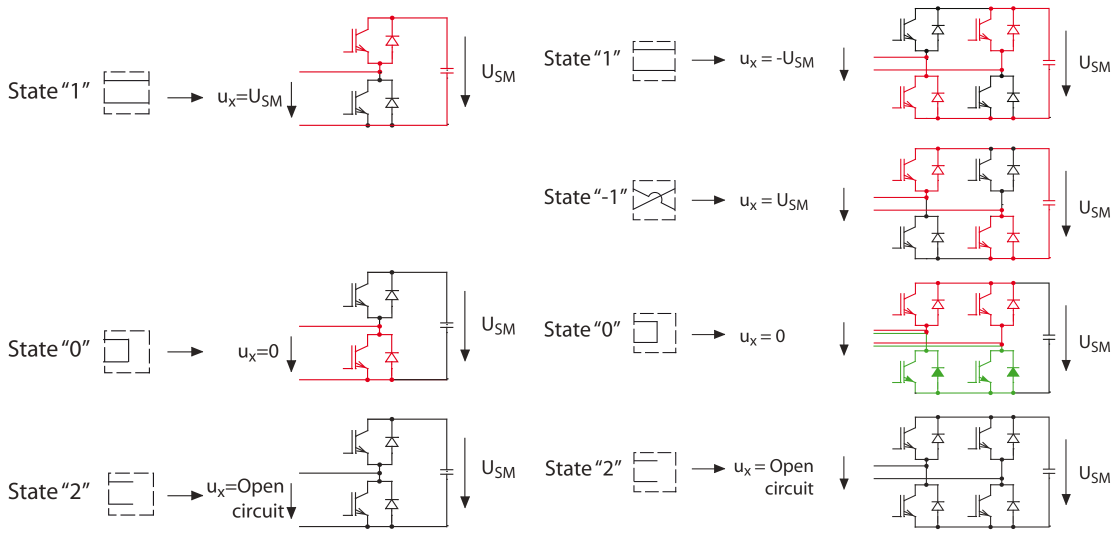
The submodules are two terminal devices, consisting of a half- or a full-bridge converter and a capacitor as shown in Fig. 4.2a) and 4.2b). In most cases a half-bridge is sufficient but if an AC/AC conversion is desired, a full-bridge converter is needed. The capacitors need to remain charged during normal working conditions, therefore the commutation strategy needs to take into account the voltage of each submodule and assure that the capacitor voltages remain in a certain range. The switches are three quadrant switches, normally IGBTs or MOSFETs, enabling bidirectional current circulation.


u_x
U_{SM}
u_x
U_{SM}

a) b)

Figure 4.2: a) Half-bridge submodule b) Full-bridge submodule

The submodules have three or four different states, illustrated in Fig. 4.3a) for the half-bridge submodules and in Fig. 4.3b) for the full-bridge submodules.


State "1"
u_x=U_{SM}
U_{SM}
State "0"
u_x=0
U_{SM}
State "2"
u_x=Open circuit
U_{SM}
State "1"
u_x = -U_{SM}
U_{SM}
State "-1"
u_x = U_{SM}
U_{SM}
State "0"
u_x = 0
U_{SM}
State "2"
u_x = Open circuit
U_{SM}

a) b)

Figure 4.3: a) Possible submodule states for half-bridges b) Full-bridge submodule states

- State "1" is defined by a positive terminal voltage independent of the current direction. Energy can either flow into the submodule, or can be extracted from the submodule.

- State "-1" is defined by a negative terminal voltage which is independent of the current direction. Energy can either flow into the submodule or can be extracted from the submodule.

- For state "0", the two terminals have the same potential, i.e. the voltage at the terminals is zero and the current can flow in either direction.
- In state "2", the submodule only stores energy and no energy can be extruded. This state is used for all submodules in the case of failure. An uncontrolled release of energy, as for example during short-circuits at the converter terminals is therefore prohibited.

The states "0", "1" and "2" apply for any of the two submodule structures, the state "-1" applies only for full-bridge submodules. State "2" is only defined if the external voltage u_x is smaller than the submodule voltage U_{sm}.

In comparison to a conventional converter, the MMC does not rely on single components. Due to its modular construction, the commonly used DC-link capacitor for maintaining the high voltage on the DC-bus is replaced by the various capacitors in the submodules. The absence of this external capacitor enhances the modularity and security [91]. For additional protection an inductance is placed in series with each branch to limit peak currents. In some cases the inductance of the conductors within a branch are already inductive enough. Redundancy can easily be implemented: If one element fails, it can be bypassed and the converter is able to maintain the power flow even with this faulty submodule. The bypass element can be a physical switch or semiconductor such as a thyristor in parallel with the submodule. The idea behind the architecture of the MMC is the modularity and the possibility to scale the converter to any voltage and power level without major changes in the layout or the component design.

The MMC can ideally be used offshore, for a wind farm HVDC transmission since the filtering requirements are low (and therefore the required space) due to the high resolution output voltage. From 2013 to 2015 at least 4 wind parks will be equipped with HVDC lines, transporting in total almost 3GW [37].

4.1 Modulation Methods

Modulation techniques for multilevel converter have been thoroughly invested in the last 20 years. The conventional modulation methods for AC/DC converters are summarised in Fig. 4.4 [92]. The main difference between the three modulation families is the switching frequency: The Pulse Width Modulation (PWM) is associated with high frequency switching, the fundamental switching frequency has the lowest switching frequency and the mixed switching frequency modulation method is between the above mentioned modulation methods in terms of switching frequency.

In most cases the multilevel converters are used as inverter/rectifier, producing a low frequency, high resolution AC waveform at 50Hz/ 60Hz from a DC voltage. For high power converters, the switching frequency should be as low as possible to minimize commutation losses. In contrast, a high voltage resolution and dynamic range is achieved with higher switching frequencies.

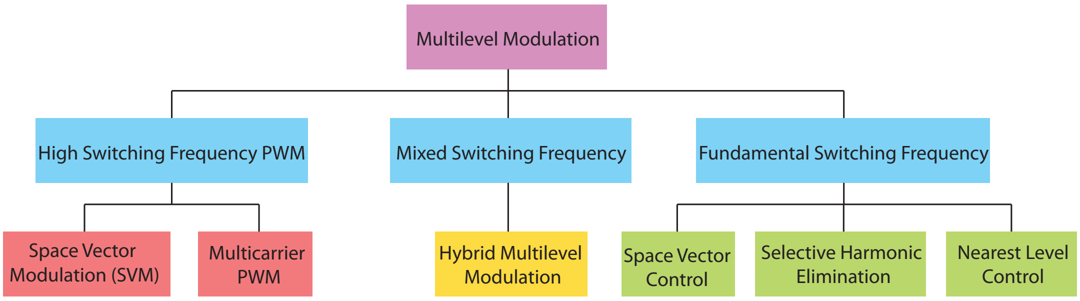

Multilevel Modulation
High Switching Frequency PWM
Mixed Switching Frequency
Fundamental Switching Frequency
Space Vector Modulation (SVM)
Multicarrier PWM
Hybrid Multilevel Modulation
Space Vector Control
Selective Harmonic Elimination
Nearest Level Control

Figure 4.4: Multilevel Modulation techniques

For the MMC in particular, the used modulation strategies are the PWM related modulations, either the space vector modulation or the naturally sampled modulation. In order to work with analogue quantities, most of the research groups work with a PWM modulation approach, building the mean value over a PWM period.

The modulation methods used by the main research groups are listed in Table 4.1. So far only little research is done within the fundamental switching frequency modulation.

4.1.1 High Switching Frequency PWM

The PWM is one of the most popular modulation methods due to the simplicity of implementation. Two subcategories can be distinguished, either the space vector PWM or the carrier based sinusoidal PWM.

In principle, PWM modulation aims at creating a pulsed signal having the same fundamental average as a reference waveform. The carrier based PWM uses either phase shifted or level shifted carrier functions to increase the effective output switching frequency. This

Table 4.1: Utilized modulation methods for MMC

Modulation Method	Research group
Space Vector Modulation	Marquardt [91]
Carrier based PWM	Rohner [93], Nee [94], Akagi [95]
Selective Harmonic Elimination PWM	Agelidis [96]
Selective Harmonic Elimination	Nee [97]

type of modulation is often called sinusoidal PWM (SPWM) or naturally sampled PWM, since the reference function to be compared with the carriers is often a sinusoidal. In general the multi-carrier based PWM aims at higher frequency and is not advisable if the switching frequency should be minimized.

The Space Vector Modulation (SVM) is based on the idea of building the average voltage vector between two switching states over a switching period. The determination of the next switching state is normally defined by a geometrical research of the nearest state vectors. With an increased number of levels the complexity increases considerably, especially if there are many redundant states. The redundant states however can be advantageous to achieve a voltage balancing of internal capacitors. The space vector PWM is often used with three level inverters.

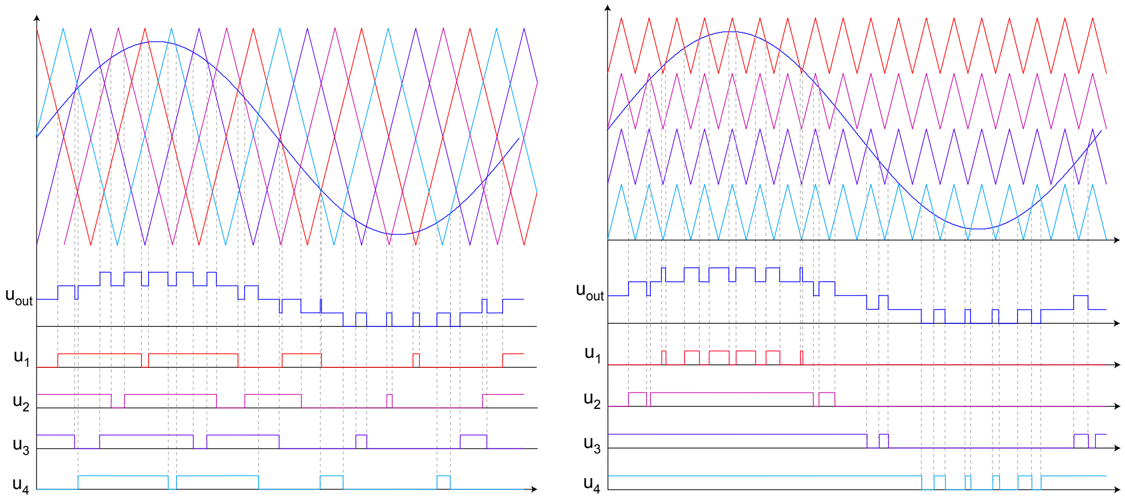
Multicarrier PWM

For the level shifted or carrier disposition methods a lot of freedom is given by the choice of the high frequency carrier [98]:

- Alternative Phase Opposition Disposition (APOD): The carriers are 180° phase shifted from the adjacent carrier.
- Phase Opposition Disposition (POD): The carriers above zero are in opposition of phase with the carriers below zero.
- Phase Disposition (PD): The carriers are in phase, but level shifted.

In a carrier based modulation, each submodule requires a carrier of its own, shown in Fig. 4.5a). Within the PWM techniques, the Phase Shifted Carriers PWM (PSPWM) techniques seems the most utilized methods for cascaded topologies [99]. In general the multi-carrier based PWM aims at higher frequency and is not advisable if the switching frequency should be minimized.

In contrast to cascaded multilevel converter, the submodule of an MMC is not supplied from a secondary side and the commutation strategy needs to assure a balanced state. The PWM methods cannot be applied as such, since the average energy over a period issued by a submodule must be zero. In Fig. 4.5 it becomes clear that the average power is not zero, in particular for the PD-PWM in Fig. 4.5b). Rather than one carrier attributed to one submodule, a single carrier is used to provide the switching instants which is illustrated in Fig. 4.6. Given a voltage reference u_{ref}, a discrete number of active cells can be determined which gives place to the staircase voltage u_{ac}. The difference between the resulting waveform u_{ac} and the reference voltage u_{ref} gives place to u_{diff}, which is compared to the triangular carrier. At each switching instant of the output voltage u_{out}, a selection algorithm decides which submodule to connect or disconnect



a) b)

Figure 4.5: a) Phase shifted carriers b) Phase disposition PWM

to maintain a balanced converter. This method is related to the PD-PWM and the AC output voltage has the same harmonic content.

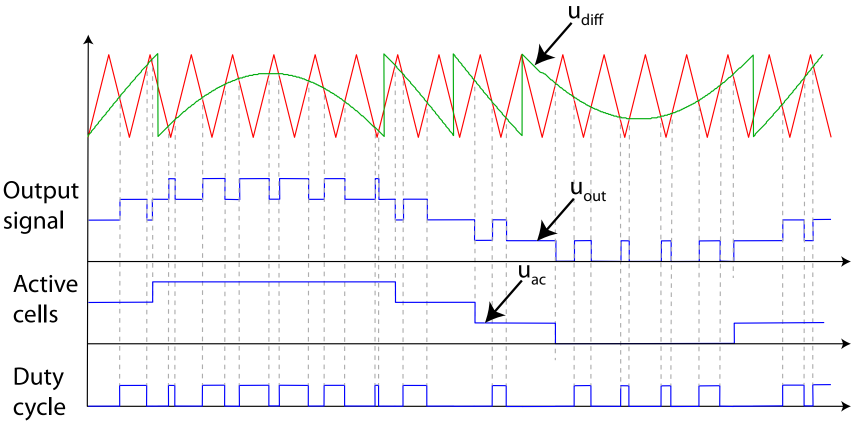


Figure 4.6: Appropriate PWM for MMC

Average Switching Frequency The average switching frequency F_{sm} of one submodule depends on the frequency of the carrier signal F_{tri}. When the carrier has a positive slope, one submodule is inserted in the upper branch and one submodule is bypassed in the lower branch. During the negative slope of the carrier, one submodule is bypassed in the upper branch and one submodule is inserted in the lower branch. In addition, at each sampling time there could be one submodule added or bypassed, since the number of active submodule is adapted. The occurrence of such an event depends on the amplitude of the modulation index $\hat{m}$.

With a modulation index equal to one, during one period of the line frequency F_{line} each cell of the branch is inserted once and bypassed once. The contribution is therefore the line frequency F_{line} times the amplitude of the modulation index. The expected value for the equivalent switching frequency of the submodule is given in (4.1) [100].

$$F_{sm} = \hat{m}F_{line} + \frac{F_{tri}}{N} \tag{4.1}$$

Space Vector PWM

The SVM is a vectorial representation of the reference voltage. The converter output can have a discrete number of switching states, which leads to a discrete number of output voltages. The linear combination of the different voltage levels should have the same averaged output voltage as the reference voltage. If a three phase system is balanced, a 2D representation can be used (in the α-β plane [101]), otherwise a 3D representation has to be adopted [102].

Three phase systems can easily represented by phasors as in (4.2)

$$\underline{U} = U_a + U_b e^{-\frac{j2\pi}{3}} + U_c e^{-\frac{j4\pi}{3}} = Re(\underline{U}) + jIm(\underline{U}) \tag{4.2}$$

The created phasor should be as close to the reference vector $\underline{U}_{ref}$ as possible. A phase vectors can take discrete values, which will be normalized to the nominal submodule voltage, therefore the voltage $\underline{U}_{abc}$ takes values between 0 and N.
In Fig. 4.7, different phasors in the α-β plan are depicted. Each crossing point is a possible output voltage. There are many states that are redundant, for example the state vector (2,3,0) can also be attained by the configuration (3,4,1). The different switching vectors have an impact on the neutral-point voltage.

In respect to the reference point $\underline{U}_{ref}$ the three nearest space vectors $\underline{U}_a$, $\underline{U}_b$ and $\underline{U}_c$ are selected, so that the line-line voltage contains the fewest harmonics. The corresponding duty cycles (also called dwelling times) can now be determined in (4.3), where T_s is the sampling period.

$$\underline{U}^* T_s = t_1 \underline{U}_a + t_2 \underline{U}_b + t_3 \underline{U}_c \tag{4.3}$$

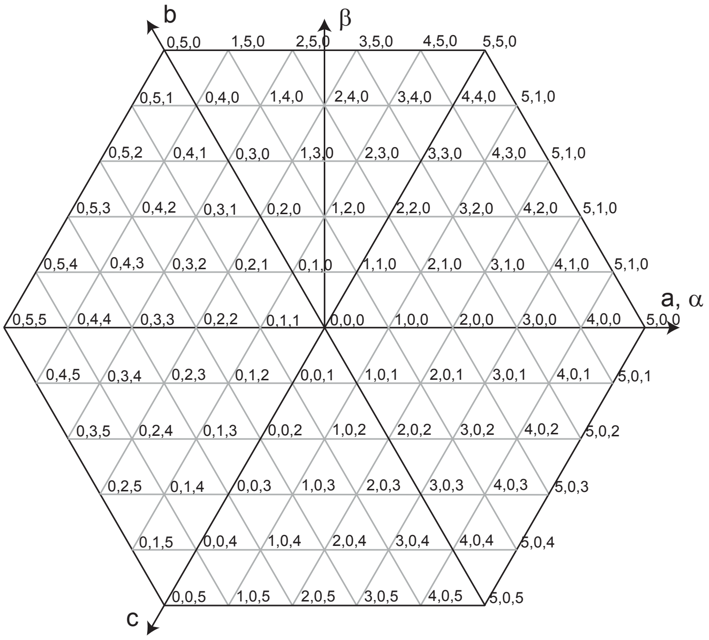


Figure 4.7: Space vectors of the voltages for a converter with 5 levels

with the constraint

$$t_1 + t_2 + t_3 = T_s \tag{4.4}$$

To obtain the switching states during one sample period, four steps have to be followed [103]:

- Choice of the basic vectors
- Calculation of the dwelling times of each vector
- Selection of the sequence of each pulse
- Control of the neutral-point potential

With this simplified approach, the computational cost and complexity of the SVM stays the same independent of the number of levels. Generally the SVM methods have good utilization of the DC link voltage and low ripple current [92].

4.1.2 Mixed Switching Frequency

Mixed frequency switching is a combination of low frequency switching techniques and MF PWM techniques [104]. This modulation method is mostly used for asymmetrical multilevel converters where the different levels process different amounts of power. Generally the cell with the lowest power operates with PWM, whereas cells with higher power are operated with lower frequency. This operation will not be detailed here.

4.1.3 Fundamental Frequency

Very low switching losses can be achieved with the fundamental switching method. Three different types can be identified for a multilevel converter, the Nearest Level Control (NLC), the Space Vector Control (SVC) and the Selective Harmonic Elimination (SHE). This section gives the theoretical background of the modulation methods which will be evaluated for the modular DC/DC converter in section 6.1.1.

Generally, the switching frequency of the single cell is equal to the frequency of the AC waveforms. The basic waveforms have a staircase form.

Nearest Level Control

The easiest way to obtain a staircase voltage waveform is to use the NLC [105], which considers the closest voltage level to the given reference. It is similar to the SVC, however the implementation is enhanced in particular for a high number of submodules. It is based on approximation of the voltage levels and not a time average of the reference signal. This method is not suited for converters with a low number of levels and a low modulation index, since the total harmonic distortion of the output is very high in that case [106].

Given a voltage reference u_{ref}, the nearest level n_{nl} can easily be determined with (4.5).

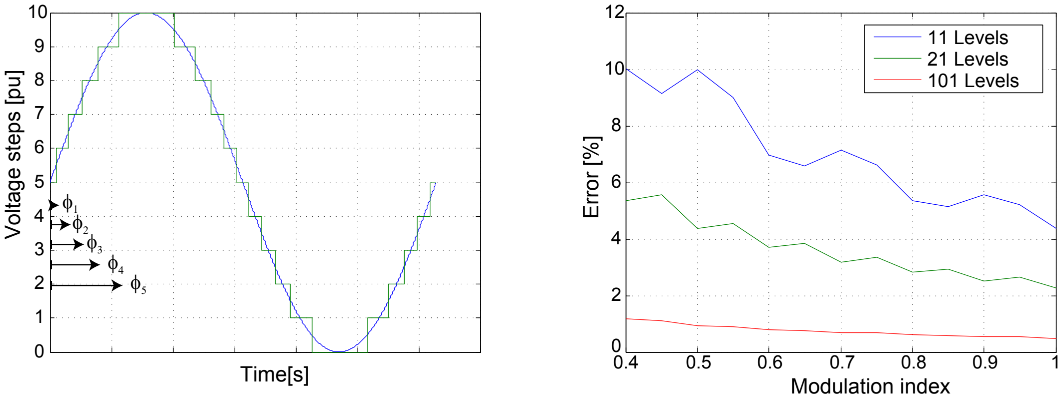
$$n_{nl} = \frac{1}{U_{sm}} round(u_{ref}) \tag{4.5}$$

It is not properly speaking a modulation, since it doesn't involve the use of duty cycles. With a high number of submodules, the error in respect to the voltage reference is really low.
The committed error depends on the number of levels and the modulation index. The

relative error is defined by (4.6).

$$E_{rel} = \frac{\frac{1}{T}{}_0\int^{T}|(u_{ref}-n_{nl}U_{sm})|dt}{\hat{u}_{ref}} \tag{4.6}$$

Just considering a single branch of the MMC, the voltage waveform for a branch with 10 submodules is shown in Fig. 4.8a) for a modulation index of 1. N+1=11 voltage levels can be distinguished. Fig. 4.8b) shows the relative error of the synthesised waveform in respect to the voltage reference according (4.6). Generally speaking, the higher the number of submodules and the higher the modulation index, the lower is the relative error.



a) b)

Figure 4.8: NLC: a) Approximated voltage waveform for a branch with 11 levels b) Relative voltage error in dependence of the modulation index for different number of levels

The nearest level control is a simple way to obtain a staircase voltage waveform and particularly effective for multilevel converters with a high number of levels.

Space Vector Control

The SVC tries not to build the mean value of the desired output voltage as in the SVM at every switching action, but aims at delivering a voltage vector that minimises the space error or distance to the reference vector. The time domain equivalent of this modulation is the NLC [105], where the closest voltage level is chosen instead of the closed voltage vector.

A vector can be represented in the complex plane with the help of (4.7):

$$\underline{U}(t) = u_x + ju_y \tag{4.7}$$

For a three phase system the components u_x and u_y are given by

$$u_x = \frac{1}{3}(2u_{an} - u_{bn} - u_{cn}) \tag{4.8}$$

$$u_y = \frac{1}{\sqrt{3}}(u_{bn} - u_{cn}) \tag{4.9}$$

Similarly to the SVM, the possible voltage vectors are represented in Fig. 4.7, where each intersection is a possible voltage vector. The appropriate choice of the vector is defined by the real and imaginary part of the reference vector $\underline{U}_{ref}$, which defines the coloured rectangle in Fig. 4.9. The points on the corner of the rectangle are two different converter vectors $\underline{U}_h$ and $\underline{u}_l$. The decision which vector $\underline{U}_{sel}$ to choose depends on the following relation:

$$If \;\; u_y > y_{tr} \;\; then \;\; \underline{U}_{sel} = \underline{U}_h \;\; else \;\; \underline{U}_{sel} = \underline{U}_l \tag{4.10}$$

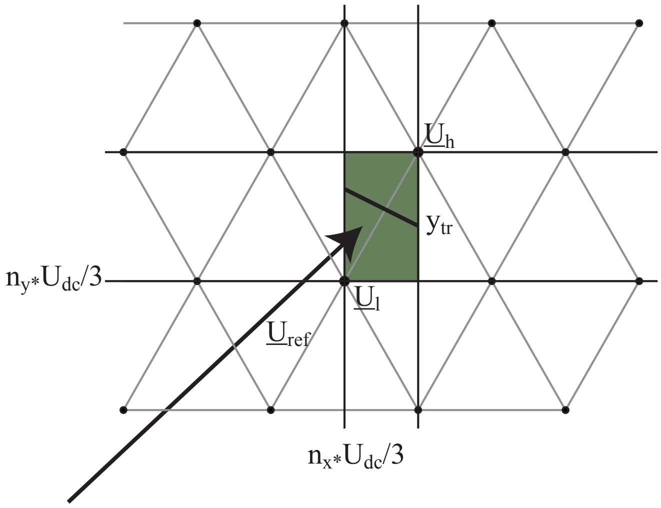


Figure 4.9: Vector selection for the space vector control

Each rectangle can be identified by two parameters n_x and n_y, that also define the threshold value y_{tr} [99].

The more levels a converter disposes, the smaller will be the error in respect to the reference vector. This method is particularly appropriate for high number of levels. Compared to the SVM, the modulation index can be much smaller using SVC at a lower Total Harmonic Distortion (THD) and a lower number of commutations [92]. The computational burden is lower than for the SVM, but higher than for the NLC.

Selective Harmonic Elimination

The SHE is a modulation method, where the on- and off-time of the different submodules are calculated the way to get the desired output wave form with selected eliminated harmonics. The switching angles are calculated off-line and stored in a table [105], which are interpolated according to the operation conditions. This modulation technique is not suited for closed loop operation due to its heavy computational needs. With a higher number of levels (>5) the SVC technique is more suitable because of the complexity of the calculation.

The considerations which follow here after are focussing on a multilevel converter with equal DC sources, since otherwise the transcendental equations are no longer symmetric and their resolution requires the solution of high-degree equation system [107]. The Fourier series expansion of the synthesised converter output voltage is shown in (4.11).

$$U(\omega t) = \sum_{k=1,3,5}^{\infty} \frac{4U_{dc}}{k\pi}(\cos(k\theta_1) + \cos(k\theta_2) + \cdots + \cos(k\theta_N))\sin(k\omega t) \tag{4.11}$$

The modulation index m is defined by $\pi u_1/4U_{sm}$, where u_1 is the amplitude of the fundamental waveform of the AC signal and U_{sm} the voltage of a submodule. Eliminating harmonics from the voltage waveform defined in (4.11) comes back to finding a solution to the equation set defined in (4.12). h_k indicates the number of the harmonic to be eliminated.

$$\begin{aligned}
\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_N) &= Nm \\
\cos(h_1\theta_1) + \cos(h_1\theta_2) + \cdots + \cos(h_1\theta_n) &= 0 \\
\cos(h_2\theta_1) + \cos(h_2\theta_2) + \cdots + \cos(h_2\theta_N) &= 0 \\
&\vdots \\
\cos(h_k\theta_1) + \cos(h_k\theta_2) + \cdots + \cos(h_k\theta_N) &= 0
\end{aligned} \tag{4.12}$$

The switching angles can be found by finding a solution to the transcendental equations of (4.12). (4.12) can be separated into 4 parts, as shown in (4.13).

$$U(\omega t) = U_{p1}(t) + U_{p2}(t) + U_{p3}(t) + U_{p4}(t) \tag{4.13}$$

- Fundamental frequency:

$$U_{p1}(t) = \frac{4U_{sm}}{\pi}\left[\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_N)\right]\sin(\omega t) \tag{4.14}$$

- Triplen harmonics:

$$U_{p2}(t) = \sum_{k=3,9,15,\ldots} \frac{4U_{sm}}{k\pi}\left[\cos(k\theta_1) + \cos(k\theta_2) + \cdots + \cos(k\theta_N)\right]\sin(k\omega t) \tag{4.15}$$

- Low order harmonics:

$$U_{p3}(t) = \sum_{k=5,7,11,13} \frac{4U_{sm}}{k\pi}\left[\cos(k\theta_1) + \cos(k\theta_2) + \cdots + \cos(k\theta_N)\right]\sin(k\omega t) \tag{4.16}$$

- High order harmonics:

$$U_{p4}(t) = \sum_{k=17,19,23,\ldots} \frac{4U_{sm}}{k\pi}\left[\cos(k\theta_1) + \cos(k\theta_2) + \cdots + \cos(k\theta_N)\right]\sin(k\omega t) \tag{4.17}$$

Solution to this equation system can either be found by applying the resultant method [108], genetic algorithms [109] or the Newton-Raphson Method [110].
The Newton-Raphson method for the solution of the (4.12) can easily be implemented also for a higher number of levels. To do so, (4.12) can be rewritten as follows:

$$F(\theta) = B(m) \tag{4.18}$$

Then the following steps are applied:

1. Defining the initial modulation index m, calculate the Jacobian J
2. Define the initial guess for the angles θ such as $0 \leq \theta_1 < \theta_2 < \cdots < \theta_n \leq \frac{pi}{2}$
3. Calculate the $F(\theta^{\mathbf{k}})$, $J(\theta^{\mathbf{k}})$ and $B(\mathbf{m})$
4. Evaluate the correction $\mathbf{d}\theta = J^{-1}(B(\mathbf{m}) - F(\theta^{\mathbf{k}})$
5. Updating the switching angles $\theta^{\mathbf{k+1}} = \theta^{\mathbf{k}} + \mathbf{d}\theta$
6. Considering the upper limit $\theta^{\mathbf{k+1}} = \arccos(abs(\cos(\theta^{\mathbf{k+1}})))$
7. If convergence is given: $Error = \mathbf{d}\theta'\mathbf{d}\theta \leq 1e^{-5}$, otherwise back to point 3 with $k = k + 1$

If convergence is given, the algorithm converges rapidly [110]. A disadvantage of the SHE is the narrow modulation index. For a 5 level converter the solutions can only be found for modulation indexes between $m = 0.376$ and $m = 0.846$ [107]. The modulation index range does not cover the high and the low end. The generalised selected harmonic modulation scheme tries to correct this disadvantage [92].

4.2 Mathematical Description

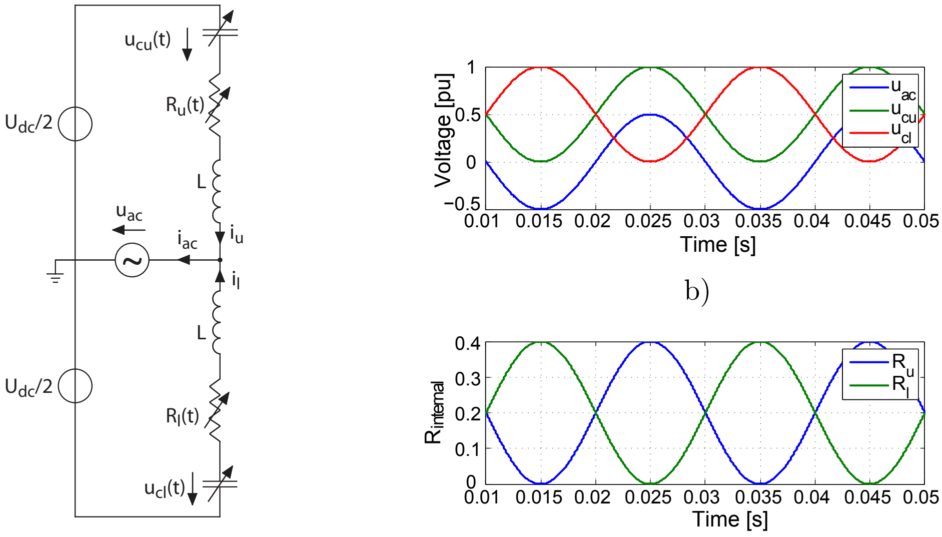
4.2.1 Considerations

Conventionally several assumptions are made in order to simplify the mathematical description of the converter. The first assumption is that the two branches are loaded symmetrically [88]. Considering the branch impedance as constant is the second assumption. It is considered that both branch currents contribute in equal quantities to the AC current i_{ac}. It can be shown that this is only the case if the branch impedance is big enough. In Fig. 4.10a) the branch impedance has on the one hand a fixed inductive part and on the other hand a resistive part that is variable due the variable number of submodules connected in the branch.

The capacitors are considered to be ideal voltage sources, which behaves according (4.19) for the upper branch and according (4.20) for the lower branch [94]. The relation $m = \frac{2\hat{U}_{ac}}{U_{dc}}$ has been used to simplify the equation.

$$u_{cu} = \frac{1}{2}U_{dc} - \hat{U}_{ac}\sin(\omega t) = \frac{1}{2}U_{dc}\left(1 - m\sin(\omega t)\right) \tag{4.19}$$

$$u_{cl} = \frac{1}{2}U_{dc} + \hat{U}_{ac}\sin(\omega t) = \frac{1}{2}U_{dc}\left(1 + m\sin(\omega t)\right) \tag{4.20}$$



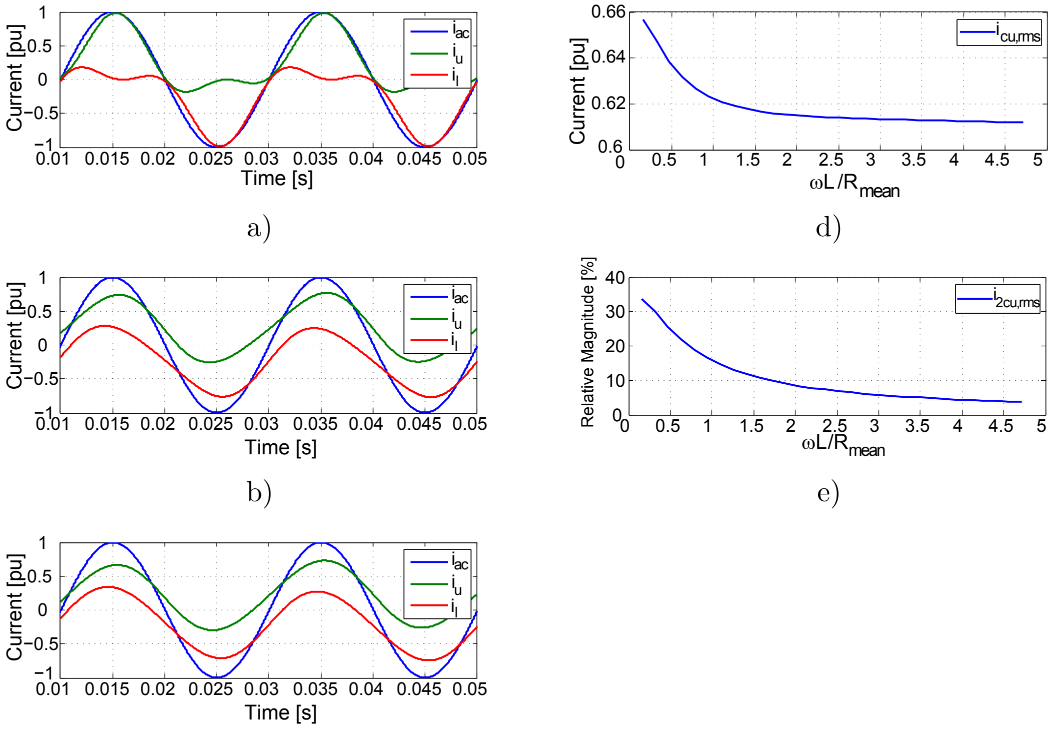
a) b) c)

Figure 4.10: a) Single leg equivalent circuit with a variable branch impedance b) Voltage of the capacitors and the AC output voltage c) Change rate of the internal resistance of the branch

This circuit can be perceived as two parallel circuits consisting of an ideal voltage source in series with the internal impedance. The respective branch resistance varies with the number of inserted submodules or capacitors due to the Equivalent Series Resistance (ESR).

Fig. 4.10b) illustrates the capacitor voltages of the upper and lower branch. Furthermore it can be assumed that the series resistance of the branch R_u, R_l is changBing with the same qualitative manner as the respective branch voltage, which is displayed in Fig. 4.10c), whereas the branch inductance L remains constant. In the simulation, a total number of 20 submodules per branch are considered with each one an internal resistance of 0.02Ω.

The current in the upper respectively the lower branch depends on the respective branch impedance: If two ideal voltage sources with identical internal impedances and identical voltages are connected in parallel on a load, the two sources are providing the same current. This however is not the case for the MMC as the branch impedance is variable. In Fig. 4.11 the branch currents are shown for different values of the branch inductance, with the variable series resistance of Fig. 4.10c). If the branch inductance is small compared to the average branch resistance $\frac{\omega L}{R_{mean}} << 1$, the branch currents show an important second harmonic content, illustrated in Fig. 4.11a). If the inductance is more significant than the average branch resistance $\frac{\omega L}{R_{mean}} \geq 1$, the currents show low second harmonic content, visible in Fig. 4.11c), where the branch currents i_u and i_l are almost purely sinusoidal with a DC offset.



a)

d)

b)

e)

c)

Figure 4.11: Branch currents i_u, i_l with a) $\frac{\omega L}{R_{mean}} = 0.15$ b) $\frac{\omega L}{R_{mean}} = 0.78$ c) $\frac{\omega L}{R_{mean}} = 4.7$; d) RMS value of the upper branch current e) relative value of the second harmonic in respect to the fundamental of the branch current

The Root Mean Square (RMS) value of the total branch current including the DC offset is shown in Fig. 4.11d). The higher the ratio $\frac{\omega L}{R_{mean}}$, the lower is the second order harmonic in the branch currents that is filtered out. The relative magnitude of the second order harmonic in respect to the fundamental is illustrated in Fig. 4.11e).

Therefore the assumption that the AC current i_{ac} is equally provided by both branches only holds true when the branch inductance conforms (4.21).

$$\frac{\omega L}{R_{mean}} \geq 1 \tag{4.21}$$

If this condition is given, the relation for AC, DC and branch currents can be established in (4.22) and (4.23).

$$i_u = \frac{i_{ac}}{2} + i_{dc} \tag{4.22}$$

$$i_l = \frac{i_{ac}}{2} - i_{dc} \tag{4.23}$$

4.2.2 Natural Balancing of the Branch Energies

Some authors mention that without an intrinsic branch energy control, the capacitor voltages become unstable [94]. The aim of this section is to prove the natural tendency of the converter to balance the energies in the upper and lower branch.

In Fig. 4.12a) a single MMC leg is shown. The branch impedance is neglected in this example and the capacitors are modelled as a voltage source. An unbalance in the branch energies has the effect of creating a DC component on the AC signal u_{ac} on the load side.

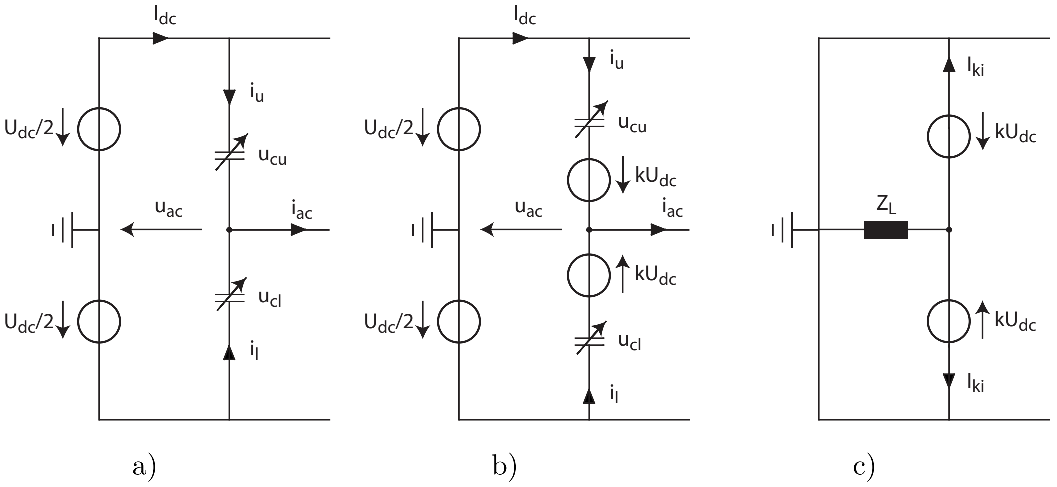


Figure 4.12: a) Balanced single leg [88] b) DC bias of the branch voltage c) DC bias using the superposition principle

The unbalance of the branch energies respectively total branch voltages $\sum U_{sm}$ will be modelled with the introduction of an additional voltage source in the branches, shown in Fig. 4.12b). The additional DC source has to be added in both branches in a complementary way, since the sum of the voltages must still respect (4.24).

$$U_{dc} \approx u_{cu} + u_{cl} \tag{4.24}$$

In order to normalise the magnitudes, the parameters m and n are introduced:

$$m = \frac{2\hat{U}_{ac}}{U_{dc}} \tag{4.25}$$

$$n = \frac{\hat{I}_{ac}}{2I_{dc}} \tag{4.26}$$

The branch voltages u_{cu} and u_{cl} are now defined by (4.27) and (4.28). The parameter k expresses the DC unbalance in the upper and lower branch and relates it to the DC input voltage U_{dc}.

$$u_{cu} = \frac{1}{2}U_{dc} - \hat{U}_{ac}\sin(\omega t) + kU_{dc} = \frac{1}{2}U_{dc}\left((1+2k) - m\sin(\omega t)\right) \tag{4.27}$$

$$u_{cl} = \frac{1}{2}U_{dc} + \hat{U}_{ac}\sin(\omega t) - kU_{dc} = \frac{1}{2}U_{dc}\left((1-2k) + m\sin(\omega t)\right) \tag{4.28}$$

The unbalance causes a DC bias of the AC load. According to the Kirchhoffs laws, the DC offset will give place to a DC current, called I_{ki}, depicted in Fig. 4.12c), which can be found by applying the superposition principle to the circuit in Fig. 4.12b). The parameter k_i is relating the additional DC branch current I_{ki} to the initial DC branch current I_{dc}. The details on the calculation are given in annex A.1.1. $cos\phi$ is the power factor on the load.

$$k_i = \frac{I_{ki}}{I_{dc}} = \frac{8k}{m^2\cos\phi} \tag{4.29}$$

The branch currents are defined by (4.30) and (4.31).

$$i_u = I_{dc} + \frac{1}{2}\hat{I}_{ac}\sin(\omega t) - I_{ki} = I_{dc}\left((1-k_i) + n\sin(\omega t + \phi)\right) \tag{4.30}$$

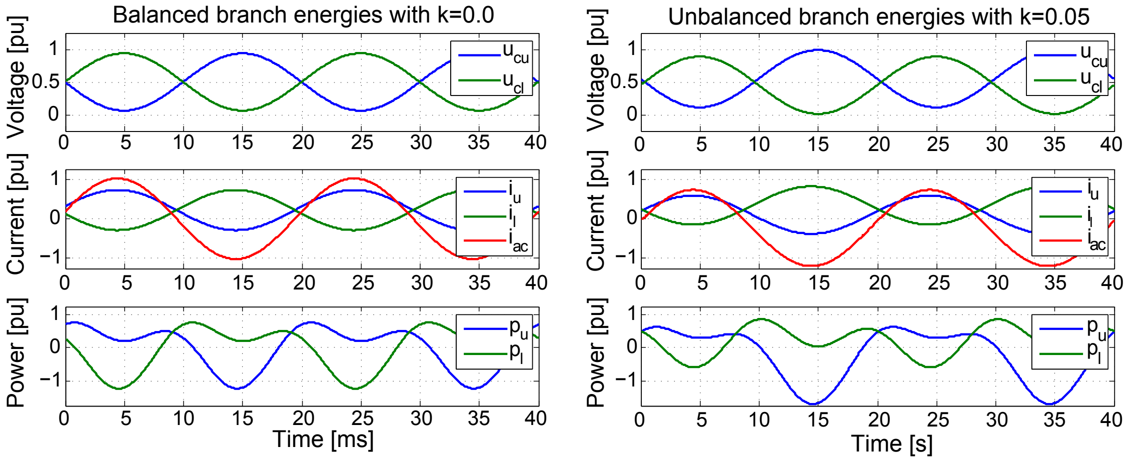
$$i_l = I_{dc} - \frac{1}{2}\hat{I}_{ac}\sin(\omega t) + I_{ki} = I_{dc}\left((1+k_i) - n\sin(\omega t + \phi)\right) \tag{4.31}$$

The instantaneous power of the capacitors is the product of their voltage and current $P_u = u_{cu}i_u$ respectively $P_l = u_{cl}i_l$.

$$P_u = u_{cu}i_u = \frac{1}{2}U_{dc}I_{dc}\left((1+2k) - m\sin(\omega t)\right)\left((1-k_i) + n\sin(\omega t+\phi)\right) \tag{4.32}$$

$$P_l = u_{cl}i_l = \frac{1}{2}U_{dc}I_{dc}\left((1-2k) + m\sin(\omega t)\right)\left((1+k_i) - n\sin(\omega t+\phi)\right) \tag{4.33}$$

Fig. 4.13a) shows the voltages, currents and powers of the converter in a balanced state with $k = 0.0$, whereas Fig. 4.13b) shows the case of an unbalance between the branch voltages of the upper and the lower branch. The positive value of the parameter $k = 0.05$ reflects the fact that the upper branch is charged to a higher level. The branch currents i_u , i_l as well as the instantaneous power P_u, P_l are altered due to the introduction of the voltage unbalance.



a)　　　　b)

Figure 4.13: a) Branch voltages, branch currents and instantaneous branch powers in balanced state with $k = 0.0$ b) Branch voltages, branch currents and instantaneous branch powers in unbalanced state with $k = 0.05$

The integral of the instantaneous power over one period defines the energy variation of the branch, whether on the long term the energy of the branch is increasing or decreasing. Using trigonometric relations, the energy variation over a period T can be found in (4.34) and (4.35).

$$W_u = \int_0^T P_u \mathrm{d}t = \frac{1}{2}U_{dc}I_{dc}\left((1+2k)(1-k_i) - \frac{mn}{2}\cos\phi\right) \tag{4.34}$$

$$W_l = \int_0^T P_u \mathrm{d}t = \frac{1}{2}U_{dc}I_{dc}\left((1-2k)(1+k_i) - \frac{mn}{2}\cos\phi\right) \tag{4.35}$$

As it has been shown in annex A.1.2, a relation between the parameter m and n exist, which is defined in (4.36).

$$\frac{2}{m\cos\phi}\left(1-\frac{8k^2}{m^2\cos\phi}\right)=n \tag{4.36}$$

The energy variation is therefore given by:

$$W_u=\frac{1}{2}U_{dc}I_{dc}\left((1+2k)(1-k_i)-(1-\frac{8k^2}{m^2\cos\phi})\right) \tag{4.37}$$

$$W_l=\frac{1}{2}U_{dc}I_{dc}\left((1-2k)(1+k_i)-(1-\frac{8k^2}{m^2\cos\phi})\right) \tag{4.38}$$

Fig. 4.14 depicts the quantities W_u and W_l in respect to the parameter of unbalance k. If k is positive, it means that the energy in the upper branch is higher than the energy in the lower branch. In this case W_u is negative, which means that there is a tendency to decrease the energy in the upper branch.
As soon as there is an unbalance in the branch energy, which results in a condition where $k \neq 0$, the respective energy variation is favourable to re-establish a balanced system.

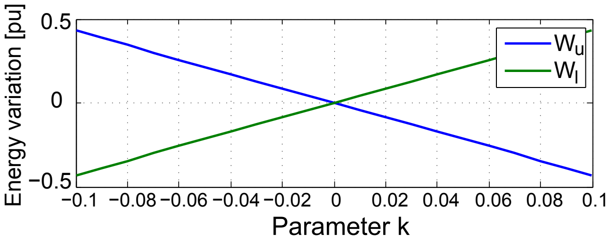


Figure 4.14: Energy variation over a period in dependence of the parameter k

4.2.3 Idealised Model

Conventionally the MMC is modelled with constant branch impedance, as illustrated in Fig. 4.15. In the continuous model, the switching effects will not be considered and the submodules appear as variable voltage source with a variable capacitance [111]. The voltage sources depend on the modulation index m_u for the upper branch and m_l for the lower branch. The capacity of one branch is variable in time and dependant on the respective modulation index.

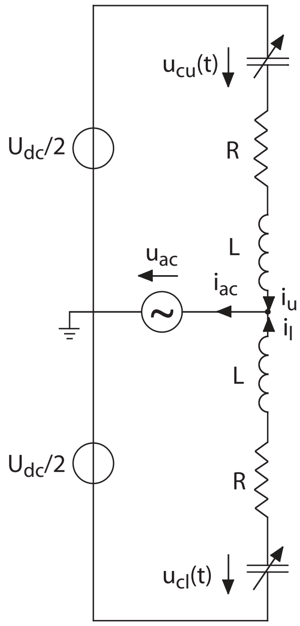


Figure 4.15: Single leg equivalent circuit [111]

$$C_u(t) = \frac{C}{N * m_u(t)} \tag{4.39}$$

$$C_l(t) = \frac{C}{N * m_l(t)} \tag{4.40}$$

The branch voltages without considering the voltage drop on the branch inductance is defined by (4.41) and (4.42).

$$u_{cu}(t) = m_u(t) \sum U_{sm,u} \tag{4.41}$$

$$u_{cl}(t) = m_l(t) \sum U_{sm,l} \tag{4.42}$$

The capacitors change their voltage according to the integral of the branch current, which is shown in (4.43) and (4.44).

$$\frac{\mathrm{d}u_{cu}(t)}{\mathrm{d}t} = \frac{N}{C} m_u(t) i_u \tag{4.43}$$

$$\frac{\mathrm{d}u_{cl}(t)}{\mathrm{d}t} = \frac{N}{C} m_l(t) i_l \tag{4.44}$$

The sum of the arm currents i_u and i_l defines the output current i_{ac}.

$$i_{ac} = i_u + i_l \tag{4.45}$$

As it has been shown in section 4.2.1, if the branch inductance is chosen high enough, one can say that the AC current is provided in equal parts by the upper and lower branch currents. This leads to the introduction of the DC branch current i_{circ}, equivalent to (4.22) and (4.23).

$$\left.\begin{aligned} i_u &= \frac{i_{ac}}{2} + i_{circ} \\ i_l &= \frac{i_{ac}}{2} - i_{circ} \end{aligned}\right\} \quad i_{circ} = \frac{i_u - i_l}{2} \tag{4.46}$$

The circuit analysis of Fig. 4.15 gives the following relation:

$$\frac{U_{dc}}{2} - Ri_u - L\frac{\mathrm{d}i_u}{\mathrm{d}t} - m_u(t)\sum U_{sm,u} = u_{ac} \tag{4.47}$$

$$-\frac{U_{dc}}{2} - Ri_l - L\frac{\mathrm{d}i_l}{\mathrm{d}t} + m_l(t)\sum U_{sm,l} = u_{ac} \tag{4.48}$$

Summing up (4.47) and (4.48), the AC terminal voltage becomes:

$$u_{ac} = \frac{m_l(t)\sum U_{sm,l} - m_u(t)\sum U_{sm,u}}{2} - \frac{R}{2}i_{ac} - \frac{L}{2}\frac{\mathrm{d}i_{ac}}{\mathrm{d}t} \tag{4.49}$$

The difference of (4.47) and (4.48) leads to the DC terminal voltage U_{dc}.

$$U_{dc} = -\frac{R}{2}i_{circ} - \frac{L}{2}\frac{\mathrm{d}i_{circ}}{\mathrm{d}t} - \left(m_u(t)\sum U_{sm,u} + m_l(t)\sum U_{sm,l}\right) \tag{4.50}$$

A new variable u_{circ} can be introduced, defined by (4.51).

$$u_{circ} = Ri_{circ} + L\frac{\mathrm{d}i_{circ}}{\mathrm{d}t} \tag{4.51}$$

The total branch energies in the upper and lower branch are given in (4.53).

$$W_{uc}^{\Sigma} = N\left[\frac{C}{2}\left(\frac{\sum U_{sm,u}}{N}\right)^2\right] = \frac{C}{2N}\left(\sum U_{sm,u}\right)^2 = \frac{C_u(t)}{2}\left(\sum U_{sm,u}\right)^2 \tag{4.52}$$

$$W_{lc}^{\Sigma} = N\left[\frac{C}{2}\left(\frac{\sum U_{sm,l}}{N}\right)^2\right] = \frac{C}{2N}\left(\sum U_{sm,l}\right)^2 = \frac{C_l(t)}{2}\left(\sum U_{sm,l}\right)^2 \tag{4.53}$$

The differentiation of the stored energies leads to (4.54) and (4.55). (4.53), (4.43) and (4.44) has been used to simplify the equations.

$$\frac{\mathrm{d}W_{cu}^{\Sigma}}{\mathrm{d}t} = i_u u_{cu} = \left(\frac{i_{ac}}{2} + i_{circ}\right)\left(\frac{U_{dc}}{2} - u_{ac} - u_{circ}\right) \tag{4.54}$$

$$\frac{\mathrm{d}W_{cl}^{\Sigma}}{\mathrm{d}t} = i_l u_{cl} = \left(\frac{i_{ac}}{2} + i_{circ}\right)\left(\frac{U_{dc}}{2} + u_{ac} - u_{circ}\right) \tag{4.55}$$

The sum and the difference of the branch energy leads to two new variables, W_c^{sum} and W_c^{circ}:

$$W_c^{sum} = W_{cu}^{\Sigma} + W_{cl}^{\Sigma} \tag{4.56}$$

$$W_c^{circ} = W_{cu}^{\Sigma} - W_{cl}^{\Sigma} \tag{4.57}$$

The derivation of the of these two quantities is given in (4.59).

$$\frac{\mathrm{d}W_c^{\Sigma}}{\mathrm{d}t} = i_u u_{cu} = (U_{dc} - 2u_{circ})i_{circ} - u_{ac}i_{ac} \tag{4.58}$$

$$\frac{\mathrm{d}W_c^{circ}}{\mathrm{d}t} = -i_l u_{cl} = 2u_{ac}i_{circ} + \left(\frac{U_{dc}}{2} - u_{circ}\right)i_{ac} \tag{4.59}$$

These quantities are going to be used for the development of the branch energy controller in section 4.3.2.

4.3 Internal Controller

The inner working of an MMC is somehow complex. Several problems must be addressed at the same time: balancing the submodule capacitors, controlling the upper and lower branch energy and following the reference coming from an external controller. Generally speaking, for a three phase MMC there are 6 degrees of freedom, one for each controllable branch. The number of state variables however exceeds the number of degrees of freedom, the five branch currents and the six branch voltages give a total of 11 state variables for the whole converter [112].

The motivation of this section is to present two methods of calculating the modulation indexes of each branch m_u, m_l in function of the global modulation index m given from the external controller.

4.3.1 Direct Modulation

Ideally the AC output voltage of any converter in an H bridge set-up follows the relation given in (4.60). m is the global modulation index.

$$u_{ac} = m(t)U_{dc} \tag{4.60}$$

If the voltage drop on the branch inductance is neglected, the following equations can be written, considering Fig. 4.15:

$$\frac{U_{dc}}{2} - u_{cu}(t) = u_{ac} \tag{4.61}$$

$$-\frac{U_{dc}}{2} + u_{cl}(t) = u_{ac} \tag{4.62}$$

The branch voltages are equal to the insertion index $m_u(t)$, $m_l(t)$ times the total branch capacitor voltage $\sum U_{sm,u}(t)$, $\sum U_{sm,l}(t)$ according (4.41) and (4.42). The insertion indexes for the lower and upper branch become:

$$m_u(t) = \frac{1 - m(t)}{2} \tag{4.63}$$

$$m_l(t) = \frac{1 + m(t)}{2} \tag{4.64}$$

Depending on the value of the branch impedances and the submodule capacitors, a second harmonic component in the circulating current i_{circ} will be more or less pronounced, which may increase the RMS value of the current [94], shown in section 4.2.1.

4.3.2 Branch Energy Controller

In order to maintain the energy in the converter constant at a desired level, the inner dynamics of the converter can be controlled. In [113], a simple method to control the energy contained in the converter is shown. The analysis is based on the model of Fig. 4.15, but can easily be extended to a multiphase topology. For the calculation, switching effects are not considered and the number of submodules is supposed to be high enough to work with continuous quantities. Furthermore the branch impedance is assumed to be constant, which is not the case in reality.

As a first assumption, the circulating current i_{circ} defined in (4.46) consists only of a DC component.

$$i_{circ} = \hat{i}_{circ} \tag{4.65}$$

Considering the capacitors as ideal controllable voltage source the voltage references u_{cu}^{ref} and u_{cl}^{ref} can be calculated. It is assumed that the voltage drop on the branch impedance $u_{circ_0} = R\hat{i}_{circ}$ is the same for the upper and the lower branch.

$$u_{cu,ref}(t) = \frac{U_{dc}}{2} - u_{ac,ref} - u_{circ_0} \tag{4.66}$$

$$u_{cl,ref}(t) = \frac{U_{dc}}{2} + u_{ac,ref} - u_{circ_0} \tag{4.67}$$

The total branch voltage depends on the stored energy, defined in section 4.2.3.

$$u_{cu}^{\Sigma}(t) = \sqrt{\frac{2W_{cu}^{\Sigma}(t)}{C_{arm}}} \tag{4.68}$$

$$u_{cl}^{\Sigma}(t) = \sqrt{\frac{2W_{cl}^{\Sigma}(t)}{C_{arm}}} \tag{4.69}$$

Now the insertion indexes for the upper and lower branch can be calculated:

$$m_u = \frac{u_{cu}^{ref}}{u_{cu}^{\Sigma}(t)} \tag{4.70}$$

$$m_l = \frac{u_{cl}^{ref}}{u_{cl}^{\Sigma}(t)} \tag{4.71}$$

In this approach, the circulating current i_{circ} is estimated with the help of the AC quantities and then used to estimate the respective branch energy. The total energy and the difference of the energies in the upper and lower branch can be controlled by influencing the energies in (4.69). In order to stabilise the system, two PI controller are controlling the two variable W_c^{sum} and W_c^{circ} given in (4.57) [94]. With this branch energy control, smaller capacitors can be used, because the ripple of the capacitor is not influencing the AC nor the DC parameters [114].

4.4 Component Sizing

4.4.1 Capacitor Design

The size of the capacitor in the submodules depends on the energy fluctuation of the branch, which is related to the frequency of the AC currents and voltages at the input and output of the converter. For a conventional three phase MMC, a formal capacitor sizing has been proposed in [88]. Here it will be only referred to the result of the capacitor sizing, since a more general concept will be detailed in section 5.2.1 .

The variables m and n, defined in (4.72) and (4.73), are relating the input to the output quantities.

$$m = \frac{2\hat{U}_{ac}}{\hat{U}_{dc}} \tag{4.72}$$

$$n = \frac{\hat{I}_{ac}}{2\hat{I}_{dc}} \tag{4.73}$$

The energy variation per submodule is given in relation 4.74. S is the apparent output power, $\cos\phi$ is the power factor.

$$\Delta W_{sm} = \frac{2}{3}\frac{S}{mN\omega}\left(1-\left(\frac{m\cos\phi}{2}\right)^2\right)^{3/2} \tag{4.74}$$

A certain voltage ripple ϵ is tolerated, which leads to the design of the submodule capacitor in (4.75). U_{sm} is the average submodule voltage.

$$C = \frac{\Delta W_{sm}}{2\epsilon U_{sm}^2} \tag{4.75}$$

4.4.2 Inductance Design

Little literature is available on the subject of the design of branch inductances. Indicated values can vary between some tenth of a per cent and several per cent [115]. Basically the arm currents full fills two tasks, on the one hand they are necessary for protection and on the other hand for the current control.

Inductance Design due to Control [116] proposes a criterion to dimension the branch inductance in respect to the peak of the circulating current. However if the circulating current is controlled, such as presented in [111], this criteria cannot be applied. In [115] another control criteria is proposed based on the Nyquist criteria: The system is basically of 1st order, with the cut-off frequency f_0 defined by the total inductance. Sufficient bandwidth of the control is given if the Nyquist frequency is at least 5 times the cut-off frequency f_0. Generally the Nyquist frequency is half of the apparent switching frequency Nf_{SW}. (4.76) summarises the design criteria, R is the total branch resistance and L is the total branch inductance.

$$f_N = \frac{N}{2} f_{SW} = 5f_0 = 5\frac{1}{\tau} = 5\frac{R}{L} \tag{4.76}$$

Inductance Design due to Protection Both authors [115] and [116] propose a dimensioning criteria of protection, in which the MMC should be able to handle short-circuits on the AC side and on the DC side. The simplest approach is to consider the equivalent circuit of Fig. 4.16.

Different degrees of protection can be considered [115]:

- Normal operation: The branch inductance is not designed to withstand faulty operation such as short-circuits, but only normal modulation. With an N+1 modulation, the voltage steps on the branch inductance are almost zero, $\Delta U \approx 0$,

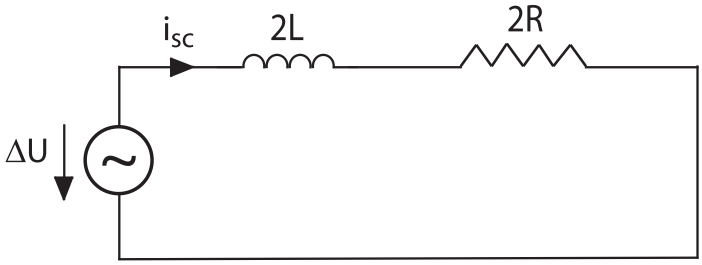


Figure 4.16: Equivalent circuit of one phase in case of an DC short-circuit

since always the same number of submodules is connected to the DC bus. In the case of a 2N+1 modulation, the voltage steps on the inductance are in the order of the voltage of one submodule: $\Delta U \approx \pm U_{sm}$.

- Faulty operation: The most severe fault is a short-circuit on the DC terminal: $\Delta U = U_{dc} = NU_{sm}$.

It is assumed that the capacitor voltages remain stable during the current rise time. In addition the resistive part of the branch impedance is rather low, therefore the circuit of Fig. 4.16 is simplified to the following relation:

$$2L\frac{\mathrm{d}i_{sc}}{\mathrm{d}t} - \Delta U = 0 \tag{4.77}$$

The current rise rate $\alpha = \frac{di}{\mathrm{d}t}$ can be introduced, which finally leads to the design criteria of the branch inductance:

$$L = \frac{\Delta U}{2\alpha} \tag{4.78}$$

For example, if a line-to-line DC short-circuit occurs at the terminals of a conventional MMC connected to the three phase 50Hz grid, a short-circuit current can establish. Assuming that the AC circuit breaker reaction time is 20ms, the maximum allowed current is 1.5kA and the DC line-to-line voltage is 300kV, an branch inductance of approximately 2.1H has to be used. Therefore conventionally thyristor are used to bypass the submodules during a short-circuit in order support higher currents and decrease the inductance rating. If additional protection devices are utilised, the weakest design criteria can be applied, namely the one for the 2N+1 modulation: $\Delta U \approx \pm U_{sm}$.

However if the reaction time can be decreased to the range of switching-off times of semiconductors ($2\mu s$ for 4500V IGBT devices and $5\mu s$ for 6500V IGBT devices), the branch inductance rating reduces to 1mH (at $10\mu s$ reaction time). It becomes clear that additional protection devices such as thyristors become obsolete in the proposed back-to-back structure, where the switching-off times are a multiple of μs.

4.5 Current Research

At the moment an impressive number of research groups in university and industry are dedicated to MMC related topics. The main research interests are

- Low output frequency - Medium voltage drives: Investigating the reduction of the submodule voltage ripples at low output frequencies during the start-up of drives [117].
- HVDC: Conventional use of the MMC used in a back-to-back configuration [88, 118]. The focus is laid on control, modulation [93, 96, 97], branch energy control [94, 113], fault management [119], Parameter design [88, 115, 116].
- Multi-terminal DC grids: Studies are focussed mostly on the system level and control [120, 121].
- Integrated storage: [122, 123].

5 DC/DC Structure

The MMC is normally used as interface between the AC grid and a HVDC line, where two MMC are connected at their DC terminal over the transmission line, illustrated in Fig. 5.1. Generally, the galvanic isolation is done on the AC grid side with bulky transformers at 50Hz or 60Hz.

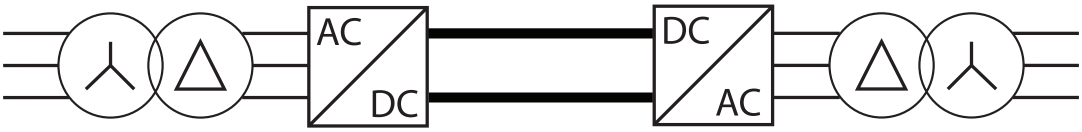


Figure 5.1: Point-to-point connection of a HVDC line based on MMC

Lately multi-terminal DC grids using MMC have been proposed [65, 79, 124], however even in this configuration the MMC is still mainly used to interface a low frequency AC source with a DC line. Several different configurations of the MMC have been proposed: A single phase AC/AC converter [125] or a three phase matrix converter [126, 127]. An alternative back-to-back configuration is presented in Fig. 5.2 [126], using a transformer between two MMCs for galvanic isolation. AC respectively DC output can be achieved, if unipolar respectively bipolar submodules are used. This topology is limited to single phase applications because a centre tapped transformer is used.

A generalisation of this concept is presented in Fig. 5.3. The bidirectional converter consists of two MMCs, called in the following primary MMC and secondary MMC. The primary and the secondary are connected to one or several transformers which are referred to as the "MF AC stage". The transformer(s) can have a ratio different or equal to 1:1. It can be a single transformer with multiple phases or several transformers connected together in different configurations. The two MMCs and the transformer build a single unit. Primary and secondary MMC are build of several branches in a bridge or matrix arrangement. The number of input phases can vary from the number of output phases; however the number of phases connected to the AC stage is the same for the primary

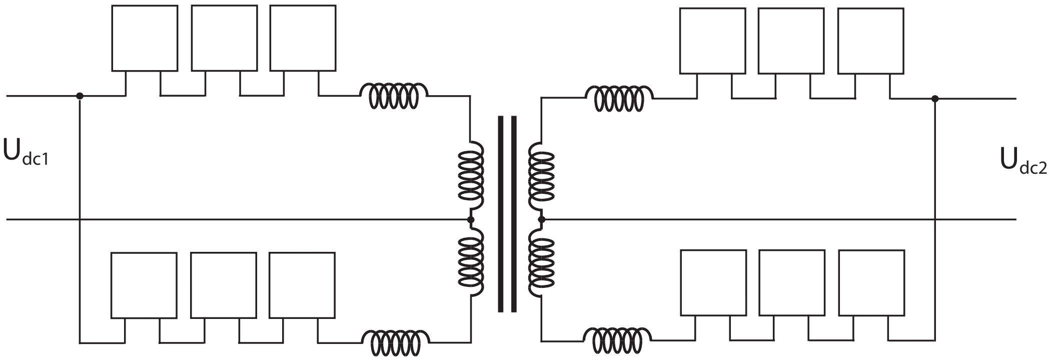


Figure 5.2: Alternative back-to-back connection

and secondary MMC.

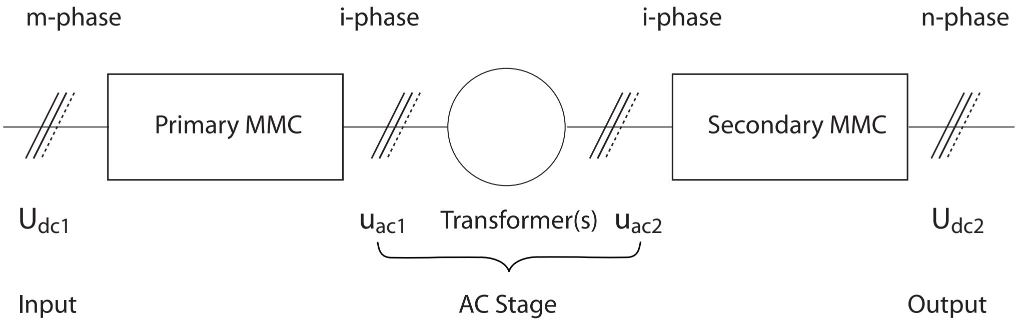

m-phase
i-phase
i-phase
n-phase
Primary MMC
Secondary MMC
U_{dc1}
u_{ac1}
Transformer(s)
u_{ac2}
U_{dc2}
Input
AC Stage
Output

Figure 5.3: General concept

A multitude of input and output configurations with a variable number of phases can be considered: AC/DC, AC/AC (Fig. 5.4) and DC/DC (Fig. 5.6) conversion is possible. The submodules within one MMC are identical, but submodules from the primary MMC don't need to be identical to the submodules of the secondary MMC. For example, bipolar submodules can be used for the primary MMC and unipolar submodules for the secondary MMC and vice versa. The capacitors in the primary MMC do not need to be charged to the same voltage as the capacitors of the secondary MMC. The number of submodules in a branch can be different for the primary and the secondary MMC. The decision on whether to use full-bridge submodules or half-bridge submodules basically depends on two conditions:

- An AC input/output is desired (AC/AC transformation)
- Boosting capability is needed (The transformer voltage is higher than the output voltage)

For example bipolar submodules are indispensable if a structure such as the AC/AC matrix converter in Fig. 5.4 is desired. Bipolar submodules allow a more flexible control, a higher voltage boosting capacity and lower current stress on the capacitors and semiconductors, but they produce also more losses.

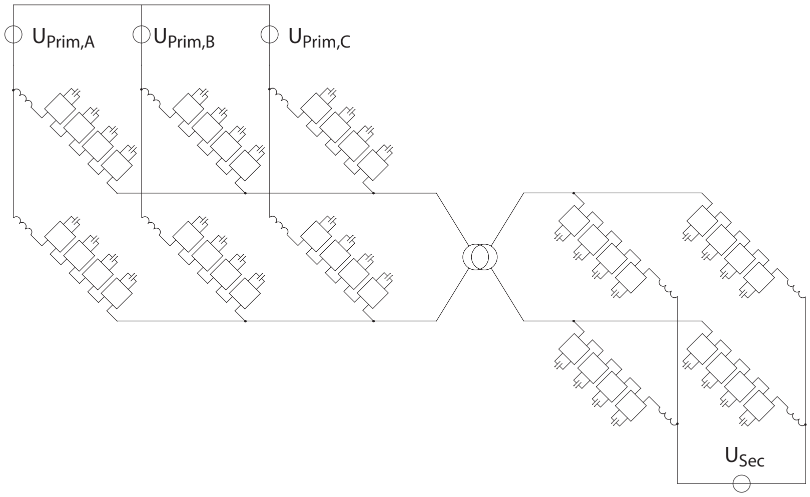


Figure 5.4: Three phase to single phase structre

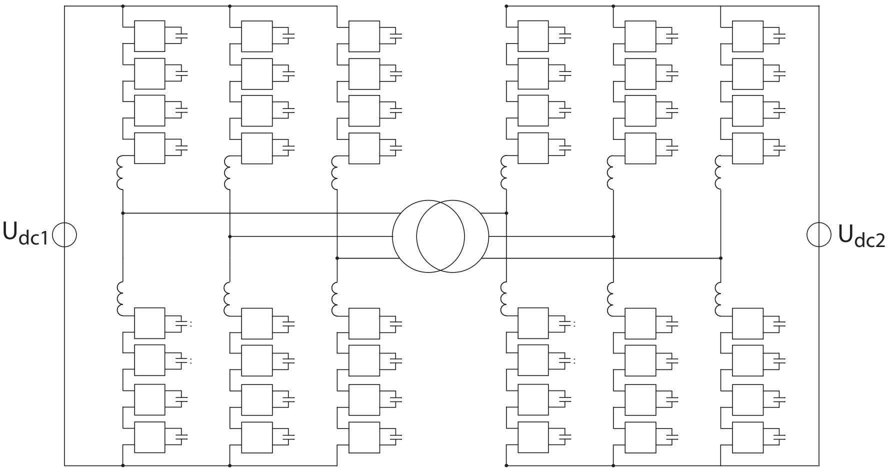


Figure 5.5: DC/DC with a 3 phase transformer

The main advantage of this structure is the possibility to use higher frequencies at the level of the transformer. The passive components within the converter are proportional to the frequency, therefore a higher operation frequency decrease the transformer, the capacitors and the branch inductances. A second advantage is the protection, which will be addressed in section 6.3.

In the frame of this thesis, the focus will be set on a DC/DC conversion with a single phase AC stage, depicted in Fig. 5.6.

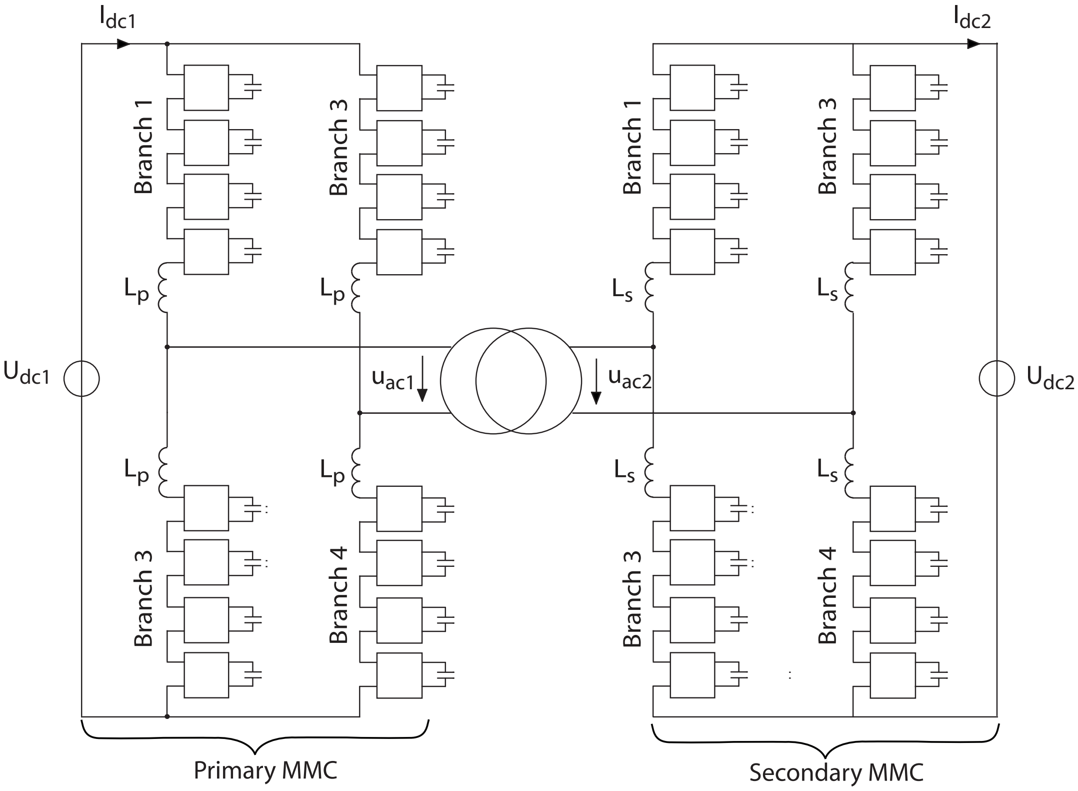

I_{dc1}
I_{dc2}
Branch 1
Branch 3
Branch 1
Branch 3
L_p
L_p
L_s
L_s
U_{dc1}
u_{ac1}
u_{ac2}
U_{dc2}
L_p
L_p
L_s
L_s
Branch 3
Branch 4
Branch 3
Branch 4
Primary MMC
Secondary MMC

Figure 5.6: Single phase converter with single phase AC stage

5.1 Mathematical Description

5.1.1 Steady-State Analysis

The following assumptions have been made in order to derive a model for the MMC:

- The input voltage U_{dc1} and output voltage U_{dc2} are considered constant
- The capacitor voltages of the submodule are equally fixed and the submodules act as controllable voltage sources
- Only the fundamental frequency component of the AC quantities is considered in the design
- The current and the voltage are identical in opposed branches, i.e. the references for the voltage and the resulting current are the same in branch 1 and 4, respectively in branch 2 and 3.

According to section 4.2.1, it can be assumed that the arm currents of the converter in Fig. 5.7 behave as in (5.1) to 5.4). The DC respectively AC currents are supplied by the

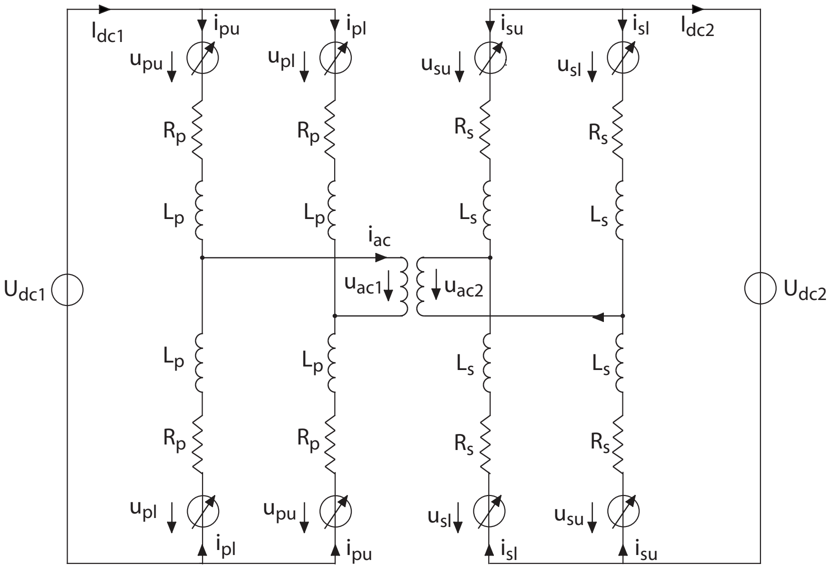

Idc1
ipu
ipl
isu
isl
Idc2
upu
upl
usu
usl
Rp
Rs
Lp
Ls
iac
uac1
uac2
Udc1
Udc2
upl
upu
usl
usu
ipl
ipu
isl
isu

Figure 5.7: Detailed model of the DC/DC converter

branch currents in equal parts.

$$i_{pu} = \frac{i_{ac}}{2} + \frac{I_{dc1}}{2} \tag{5.1}$$

$$i_{pl} = -\frac{i_{ac}}{2} + \frac{I_{dc1}}{2} \tag{5.2}$$

$$i_{su} = -\frac{i_{ac}}{2} - \frac{I_{dc2}}{2} \tag{5.3}$$

$$i_{sl} = \frac{i_{ac}}{2} - \frac{I_{dc2}}{2} \tag{5.4}$$

In (5.5) to (5.8), the references for the branch voltages are defined, where $\hat{U}_p$ is the amplitude of the AC voltage on the transformer primary terminals and $\hat{U}_s$ the amplitude of the AC voltage on the transformer secondary terminals, without the voltage drop on the branch inductances.

$$u_{pu} = \frac{1}{2}(U_{dc1} + \hat{U}_p \sin(\omega t)) \tag{5.5}$$

$$u_{pl} = \frac{1}{2}(U_{dc1} - \hat{U}_p \sin(\omega t)) \tag{5.6}$$

$$u_{su} = \frac{1}{2}(U_{dc2} + \hat{U}_s \sin(\omega t + \delta)) \tag{5.7}$$

$$u_{sl} = \frac{1}{2}(U_{dc2} - \hat{U}_s \sin(\omega t + \delta)) \tag{5.8}$$

Considering the Kirchhoff loops formed by the upper or lower branches and the transformer for the primary and secondary MMC, the relation for the transformer voltage u_{ac1} and u_{ac2} is found.

$$\begin{aligned}
u_{ac1} &= -R_p i_{pu} - L_p \frac{\mathrm{d}i_{pu}}{\mathrm{d}t} - u_{pu} + u_{pl} + R_p i_{pl} + L_p \frac{\mathrm{d}i_{pl}}{\mathrm{d}t} \\
&= -R_p i_{ac} - L_p \frac{\mathrm{d}i_{ac}}{\mathrm{d}t} - (u_{pu} - u_{pl}) \\
u_{ac2} &= -R_s i_{su} - L_s \frac{\mathrm{d}i_{su}}{\mathrm{d}t} - u_{su} + u_{sl} + R_s i_{sl} + L_s \frac{\mathrm{d}i_{sl}}{\mathrm{d}t} \\
&= -R_s i_{ac} - L_s \frac{\mathrm{d}i_{ac}}{\mathrm{d}t} - (u_{su} - u_{sl})
\end{aligned} \tag{5.9}$$

The current i_{ac} in the transformer is determined by the difference of the voltages u_{ac1} and u_{ac2}, where L_σ summarises the leakage inductance of the primary and the secondary side of the transformer $L_\sigma = L_{\sigma 1} + L_{\sigma 2}$:

$$u_{ac2} - u_{ac1} = L_\sigma \frac{\mathrm{d}i_{ac}}{\mathrm{d}t} + R_\sigma i_{ac} \tag{5.10}$$

Finally, by combining the above equations, an expression for the transformer current in dependence on the branch voltages can be found in (5.11).

$$(u_{su} - u_{sl}) - (u_{pu} - u_{pl}) = (L_p + L_s + L_\sigma) \frac{\mathrm{d}i_{ac}}{\mathrm{d}t} + (R_p + R_s + R_\sigma) i_{ac} \tag{5.11}$$

In the following, the sum of the branch inductance and the leakage inductance will be summarised in $L_{tot} = L_p + L_s + L_\sigma$.

Given the amplitudes and the phase of the AC voltages u_{ac1} and u_{ac2}, the current within the transformer can be estimated. Based on the simplified model of Fig. 5.8 [71], relation (5.12) can be established. The resistive part has been neglected to simplify the equations.

$$i_{ac} = \frac{1}{L_{tot}} \int \left(\hat{U}_p sin(\omega t) - \hat{U}_s sin(\omega t + \delta) \right) \mathrm{d}t \tag{5.12}$$

The general solution using the law of cosines for the relation 5.12 is given in (5.14). $\hat{I}_{ac}$ is the peak current and θ is the phase shift of the current in respect to the primary AC voltage u_{ac1}.

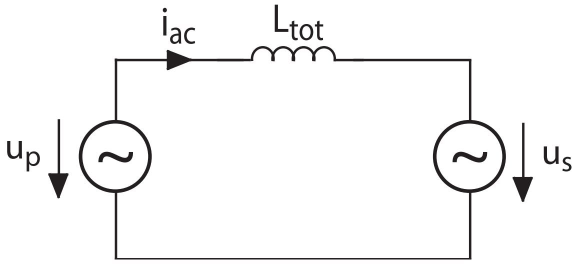


Figure 5.8: Equivalent model of the AC stage [71]

$$\hat{I}_{ac} = \frac{\sqrt{\hat{U}_p^2 + \hat{U}_s^2 - 2\hat{U}_p\hat{U}_s\cos\delta}}{\omega L_{tot}} \tag{5.13}$$

$$\theta = \frac{\pi}{2} - \arccos\frac{\hat{U}_p^2 - \hat{U}_s^2 + (\omega L_{tot}\hat{I}_{ac})^2}{2\hat{U}_p\omega L_{tot}\hat{I}_{ac}} \tag{5.14}$$

However if we suppose that the amplitudes $\hat{U}_p$ and $\hat{U}_s$ are identical and equal to $\hat{U}_{ac}$, a simpler relation can be established:

$$\hat{I}_{ac} = 2\frac{\hat{U}_{ac}}{\omega L_{tot}}\sin(\frac{\delta}{2}) \tag{5.15}$$

$$\theta = \frac{\delta}{2} \tag{5.16}$$

5.1.2 AC Stage Equations

The AC stage can be simplified as in Fig. 5.8, where the series resistance is neglected. The transformer will be represented by its leakage inductance and both converters by their AC voltage u_p and u_s.

The voltages u_p and u_s can represented as phasors, where the parameter δ is the phase shift between the two sinusoidal sources.

$$\underline{u}_p = \hat{U}_p e^{j\omega t} \tag{5.17}$$

$$\underline{u}_s = \hat{U}_s e^{j\omega t+\delta} \tag{5.18}$$

The current phasor $\underline{i}_{ac}$ is given by

$$\underline{i}_{ac} = \frac{\underline{u}_s - \underline{u}_p}{j\omega L_{tot}} \tag{5.19}$$

The active power transported by the transformer is given in relation

$$P_{ac} = Re(\frac{\underline{u}_p \underline{i}_{ac}^*}{2}) = \frac{\hat{U}_p \hat{U}_s \sin\delta}{2\omega L_{tot}} \tag{5.20}$$

The reactive powers Q_p respectively Q_s delivered by the primary respectively the secondary source is defined by

$$Q_p = Im(\frac{\underline{u}_p \underline{i}_{ac}^*}{2}) = \frac{\hat{U}_{ac1}\hat{U}_{ac2}\cos\delta - \hat{U}_{ac1}^2}{2\omega L_{tot}} \tag{5.21}$$

$$Q_s = Im(\frac{\underline{u}_s \underline{i}_{ac}^*}{2}) = \frac{\hat{U}_{ac2}^2 - \hat{U}_{ac1}\hat{U}_{ac2}\cos\delta}{2\omega L_{tot}} \tag{5.22}$$

It is convenient for regulation purposes to have an expression of the phase shift δ as a function of the load current I_{dc2}. The following expression, derived from (5.20), assumes that the transported AC power P_{ac} equals the output power $P_{dc2} = U_{dc2}I_{dc2}$ in steady state conditions.

$$\delta = asin\left(\frac{\omega L_{tot} P_{ac}}{\hat{U}_{apc1}\hat{U}_s}\right) = asin\left(\frac{\omega L_{tot} U_{dc2} I_{dc2}}{\hat{U}_p \hat{U}_s}\right) \tag{5.23}$$

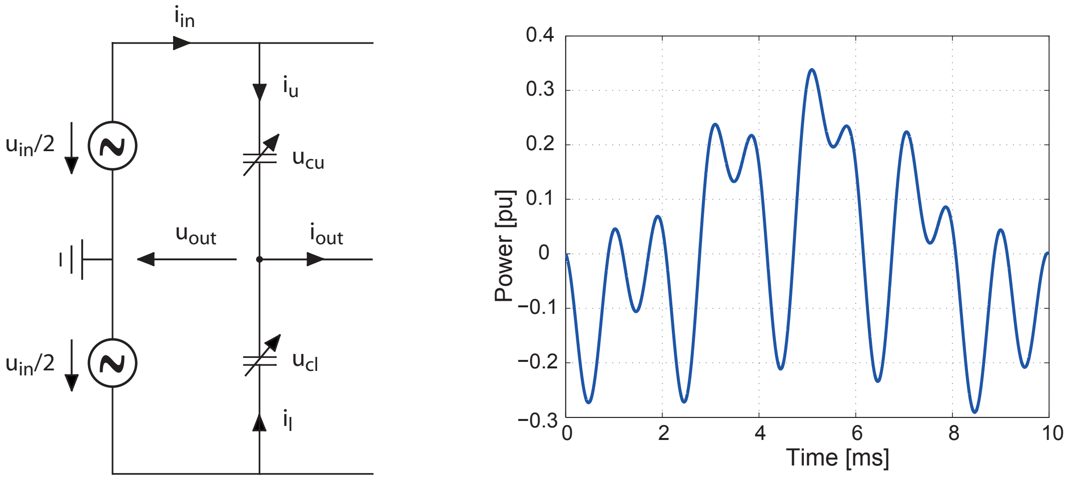
If both AC voltages have similar amplitudes, the reactive power transfer in the transformer is low if the phase shift is low. On the other hand, the active power transfer increases with the phase shift. Generally the phase shift δ should be small to limit the reactive power.

5.2 Parameter Design

The crucial design parameters of this converter is the leakage inductance of the MF transformer, the submodule capacitors and the branch inductances.

5.2.1 General Capacitor Design

The most generic case of an MMC topology can be found in [125], where the MMC is used in a matrix configuration, having an AC input and output. For this example, n_{in} input and n_{out} output phase-legs are considered, with an angular speed ω_{in} for the input and ω_{out} for the output. In Fig. 5.9a) a single phase-leg is represented, where i_u, i_l are the upper and lower branch currents and u_{cu}, u_{cl} the upper and lower branch voltages. The branch impedance is neglected.



a) b)

Figure 5.9: a) Single leg model b) Power P_u of the upper branch for one period $T = 2\pi/\omega_{in}$

The input voltage source u_{in} has been divided in two parts, in order to make the further calculation easier to understand. Assuming that the number of submodules is high enough, the voltages u_{cu} and u_{cl} can be approximated as continuous controllable voltage sources. The phase voltages and currents of the input and the output are defined in (5.24) and (5.25).

$$u_{in} = \hat{U}_{in}\cos(\omega_{in}t) \qquad u_{out} = \hat{U}_{out}\cos(\omega_{out}t) \tag{5.24}$$

$$i_{in} = \hat{I}_{in}\cos(\omega_{in}t + \phi_{in}) \qquad i_{out} = \hat{I}_{out}\cos(\omega_{out}t + \phi_{out}) \tag{5.25}$$

In a symmetrical system with balanced consumption, the upper branch current and voltage can be expressed as in (5.26) and (5.27), depending on the number of phase legs n_{out}.

$$i_u = \frac{i_{in}}{n_{out}} + \frac{i_{out}}{2} \tag{5.26}$$

$$u_{cu} = \frac{u_{in}}{2} - \frac{u_{out}}{2} \tag{5.27}$$

This leads to an instantaneous branch power of $P_u = u_{cu} i_u$, illustrated in Fig. 5.9b) for $\omega_{in} = 314 s^{-1}$, $\omega_{out} = 3141 s^{-1}$, $\phi_{in} = 0°$, $\phi_{out} = 10°$ and $n_{out} = 2$.

The average active input and output power is given in (5.28) and (5.29).

$$P_{in} = \frac{n_{in}}{2} \hat{I}_{in} \hat{U}_{in} \cos(\phi_{in}) \tag{5.28}$$

$$P_{out} = \frac{n_{out}}{2} \hat{I}_{out} \hat{U}_{out} \cos(\phi_{out}) \tag{5.29}$$

The variables m and n are introduced in (5.30) and (5.31) in order to simplify the following development.

$$m = \frac{2\hat{U}_{out}}{\hat{U}_{in}} \tag{5.30}$$

$$n = \frac{n_{out} \hat{I}_{out}}{2\hat{I}_{in}} \tag{5.31}$$

Resuming (5.28) to (5.31) leads to a relation between the variables m and n:

$$n = \frac{n_{in}}{m \cos \phi_{out}} \tag{5.32}$$

Like in [88], a formal capacitor sizing can be derived by calculating the energy variation of the capacitors of a branch between two zero crossings of the branch power P_u. Since it is obviously a difficult task to do so for a system pulsating with two different frequencies, a simpler approach is followed: A coordinate transformation is applied in order to convert the system from AC/AC to DC/AC. Therefore the equations from relation (5.24) and (5.25) can be seen from a synchronous reference frame turning at the angular speed ω_{in}.

$$u_{in}^d = \hat{U}_{in} \qquad u_{out}^d = \hat{U}_{out}\cos((\omega_{out}-\omega_{in})t) \tag{5.33}$$

$$i_{in}^d = \hat{I}_{in}\cos\phi_{in} \qquad i_{out}^d = \hat{I}_{out}\cos((\omega_{out}-\omega_{in})t+\phi_{out}) \tag{5.34}$$

The system has been considerably simplified and now a similar approach for the capacitor design as in [88] can be followed, considering a DC input and an AC output.

The instantaneous power P_u^d in the rotating reference frame is determined in (5.35).

$$P_u^d = (\frac{u_{in}^d}{2} - \frac{u_{out}^d}{2})(\frac{i_{in}^d}{n_{out}} + \frac{i_{out}^d}{2}) \tag{5.35}$$

The integral of the instantaneous power P_u^d between two zeros leads to the energy variation for upper branch [88]:

$$\Delta W_Z = \frac{1}{\omega_{out}-\omega_{in}}\frac{P_{out}}{n_{out}}n(1-\frac{1}{n^2})^{3/2} \tag{5.36}$$

The value of a submodule capacitor C_{sm} is now defined in (5.37), with N the number of submodules per branch, ϵ the tolerated voltage ripple in percent, U_{sm} the capacitor voltage of one submodule and S_{out} the apparent power of the output given by the relation $P_{out} = S_{out}\cos\phi_{out}$. Furthermore the variable n is replaced by relation 5.32.

$$C_{sm} = \frac{\Delta W_Z}{2N\epsilon U_{sm}^2} = \frac{1}{2\epsilon U_{sm}^2}(\frac{n_{in}S_{out}}{mNn_{out}(\omega_{out}-\omega_{in})})(1-(\frac{m\cos\phi_{out}}{n_{in}})^2)^{3/2} \tag{5.37}$$

(5.37) reveals that the capacitor value is inversely proportional to the difference of the frequency between the input and output. The capacitor design can be applied to both modulation methods presented in section 6.1 and section 6.2. The parameters m, n_{in} and n_{out} are chosen according the topology and the elevation factors. For the two-level modulation presented in section 6.2, a high voltage elevation k_p respectively k_s is equivalent to a low modulation index m.

5.2.2 Inductance Design

Generally, the branch inductance has to respect design criteria based on protection and design criteria relative to control as evoked in section 4.4.2. In terms of protection, the branch inductance does limit the $\frac{\mathrm{d}i}{\mathrm{d}t}$ in case of short-circuits. As shown in section 6.3, the proposed topology is able to handle the most severe faults efficiently and in very short time: Measurement delay and reaction time of the command platform, which is in the order of tens of microseconds. Therefore the inductance design in respect to faults is not a limiting factor.

For both modulation methods presented in section 6.1 and 6.2, synchronous switching actions are foreseen. Always the same number of submodules will be connected to the respective DC bus. For the multilevel modulation, this gives place to a N+1 modulation. Also for the two-level operation, the switching actions are synchronous in the upper and lower branch. In steady state conditions, the voltage steps created on the branch inductance are only due to small differences in the switching instants of the submodule. The design criterion regarding the modulation is therefore not a limiting factor.

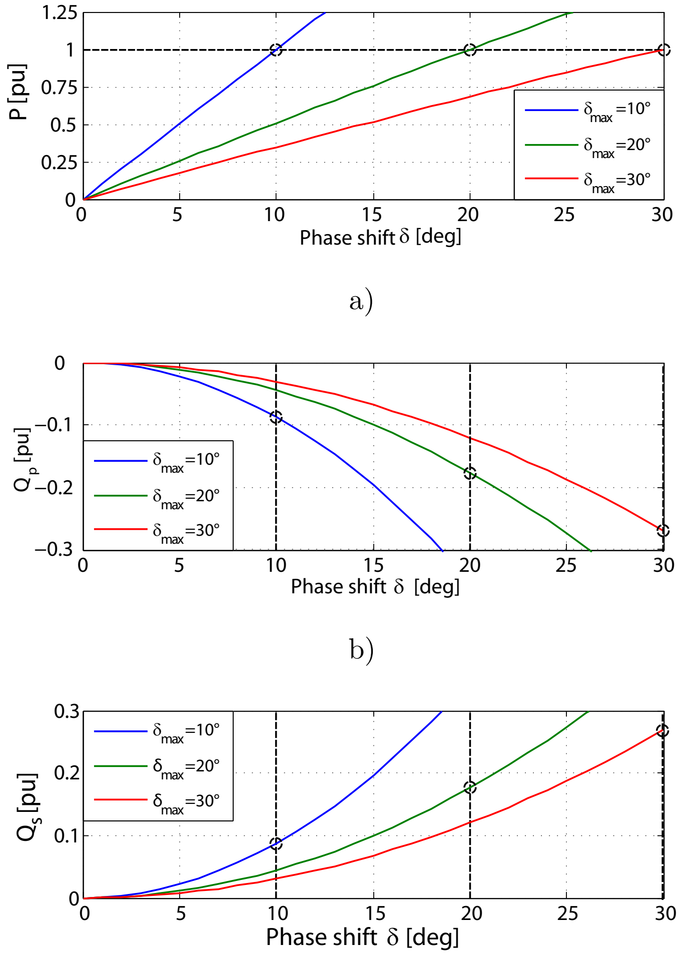
From that point of view the criteria of control is more restrictive. From the analysis of section 5.1, where it has been shown that for control purposes the system can be represented as two voltage sources with an equivalent inductance L_{tot} as in Fig. 5.8, we can set up a criteria for the control based on the total inductance given in (5.38).

$$L_{tot} = L_\sigma + L_p + L_s \tag{5.38}$$

The active power flow through the inductance L_{tot} is given in (5.20) and the reactive power flowing from the primary source to the secondary source in (5.21) respectively in the inverse direction in (5.22). Inverting (5.20) gives the design for the inductance L_{tot}, which depends on the maximum phase shift δ_{max} at nominal power P_{nom}.

$$L_{tot} = \frac{\hat{U}_p \hat{U}_s \sin \delta_{max}}{2\omega P_{nom}} \tag{5.39}$$

From (5.21) and (5.22) it becomes clear that the higher δ_{max}, the higher the reactive power circulation and therefore the current rating of the converter. In Fig. 5.10, the power flow for three values of δ_{max} have been depicted. In 5.10a) the nominal power of 1pu is attained at the respective δ_{max}. In Fig. 5.10b) and 5.10c) the reactive power at the primary and the secondary are shown and it becomes obvious that at 1pu of active power, a higher value of δ_{max} results in a higher reactive power. In Table 5.1 the numerical values of the reactive powers for the three designs are indicated at nominal power.



a)

b)

c)

Figure 5.10: Power flow in the DC/DC modular converter a) Active power P b) Reactive power at the primary source Q_p c) Reactive power at the secondary source Q_s

Therefore a design with little phase shift is more favourable to limit the reactive power circulation within the converter. In general, a $\delta_{max} = 10°$ and below has proven to provide enough controllability even at powers well below the nominal power. However if

Table 5.1: Reactive powers during an active power flow of $P_{nom} = 1pu$

	$\delta_{max} = 10°$	$\delta_{max} = 20°$	$\delta_{max} = 30°$
Q_p	-0.087pu	-0.176pu	-0.267pu
Q_s	0.087pu	0.176pu	0.267pu

the number of levels is low, a higher value of δ_{max} might be needed in order to increase the filtering effect on the otherwise harmonically distorted AC current.

The inductance L_{tot} is defined by (5.39), however the values of the different inductances (branch and leakage inductances) are to be determined: In terms of protection on the DC sides, the leakage inductance of the transformer does not play an important role in contrast to the branch inductances. This is why the leakage inductance is chosen as small as possible in respect to the branch inductances. If unequal characteristics are given for the primary and secondary MMC (different number of levels, different voltage rating), the contribution of the respective branch inductance will depend on the respective MMC ratings of the primary and the secondary, given in (5.40) and (5.41).

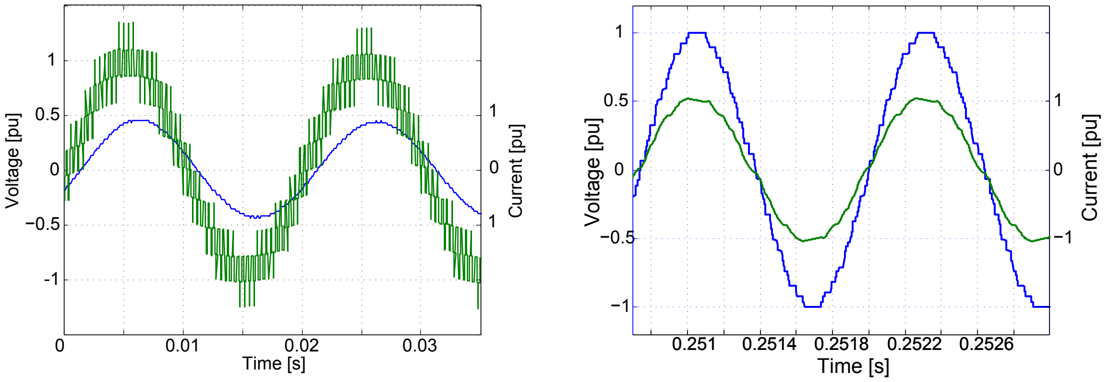
$$L_p = \frac{1}{1 + \frac{U_{dc1}}{U_{dc2}}} L_{tot} \tag{5.40}$$

$$L_s = \frac{\frac{U_{dc1}}{U_{dc2}}}{1 + \frac{U_{dc1}}{U_{dc2}}} L_{tot} \tag{5.41}$$

6 Control and Protection of the Modular DC/DC Converter

6.1 Multilevel Modulation Strategies

The conventional way of operating an MMC is to produce a high resolution AC waveform on the transformer, such as depicted in Fig. 6.1a).



a)

b)

Figure 6.1: a) PWM modulation of a single-phase MMC b) Fundamental switching waveforms of a single-phase MMC

Generally in this kind of modulation the mean average switching frequency of a cell (determined in section 4.1.1) is several times the nominal AC output frequency of 50Hz/60Hz. The "front-to-front" structure presented in chapter 5 however makes it possible to set the AC frequency freely, because it is decoupled from the input/output. If a higher frequency is chosen, it is possible to downsize the passive components within the converter, such as the transformer and the capacitors. On the other hand a higher AC frequency leads to a higher switching frequency, which also has a negative effect on the switching losses. Instead of choosing a PWM modulation, a modulation with fewer switching actions is necessary. Fundamental switching frequency operation, illustrated in

Fig. 6.1b), gives the lowest switching frequencies and will be investigated in more details in section 6.1.1.

6.1.1 Modulation Strategy

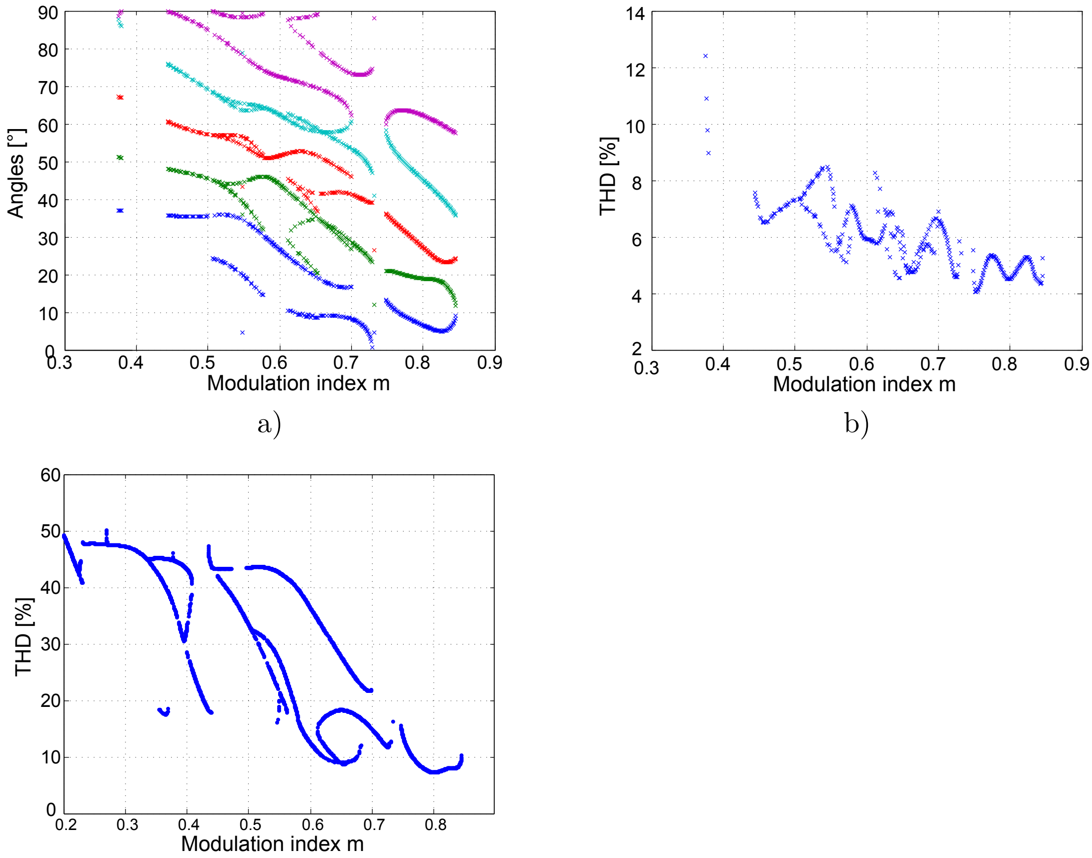
Among the conventional multilevel modulation methods presented in section 4.1, only the modulation methods with low switching frequency will be analysed. In particular two modulation methods are considered, the Nearest Level Control (NLC) and the Selective Harmonic Elimination (SHE). The Space Vector Control (SVC) is aimed at three phase systems, therefore it will not be taken into account.

SHE attempts to decrease the harmonic distortion in the voltage waveform. As it will be seen later, calculating the SHE for an MMC with a high number of levels becomes very difficult and the modulation index will be limited to low values. In contrast, the complexity for the NLC algorithm does not increase with the number of levels and at the same time the harmonic performance increases with a higher number of levels.

Performance Evaluation SHE Using the Newton-Raphson algorithm described in section 4.1.3, the switching angles of a system with 5 submodules are calculated. In a three phase converter, the SHE typically compensates the 5th, 7th, 11th and 13th harmonic. The switching angles in dependence of the modulation index are shown in Fig. 6.2a). Solutions can only be found for a modulation index between $m = 0.376$ and $m = 0.846$ [107]. For some modulation indexes several solutions are possible and if the increment of the modulation index is chosen small enough, the Newton-Raphson algorithm is able to show all of them [110]. The decision on which solution is best depends on the corresponding THD. Fig. 6.2b) shows the THD when the triplen harmonics are taken into account and in Fig. 6.2c) the THD for the same angles considering the triplen harmonics are shown. In the line-to-line voltage in a three-phase system the triplen harmonics are eliminated.

Since the considered system is not a three phase system but a single phase system, the triplen harmonics won't be cancelled out, and therefore all the low harmonics should be cancelled by the SHE, namely the 3rd, 5th, 7th and 9th. Fig. 6.3a) shows the switching angles of such a converter, Fig. 6.3b) shows the THD. The possible solutions are restricted to modulation indexes between 0.643 and 0.686, with a solution at 0.515 and 0.8. The solution range is very limited. One solution for that narrow solution range is for example to introduce more switching actions and apply the SHE-PWM, which offers a wider range of modulation index [96, 128]. This modulation technique however results in a higher number of commutations per period.

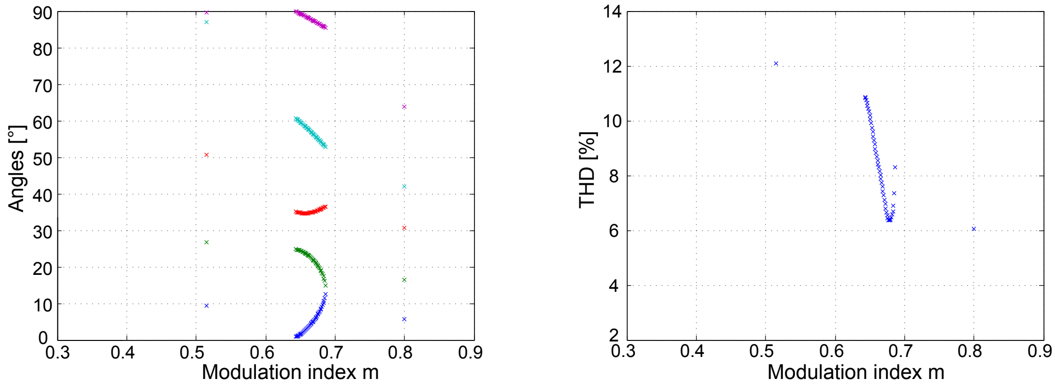
As the number of levels is increased, the convergence of the Newton-Raphson algorithm is not always achieved. Fig. 6.4a) shows the example for a converter with 31 levels. The



a) b)

c)

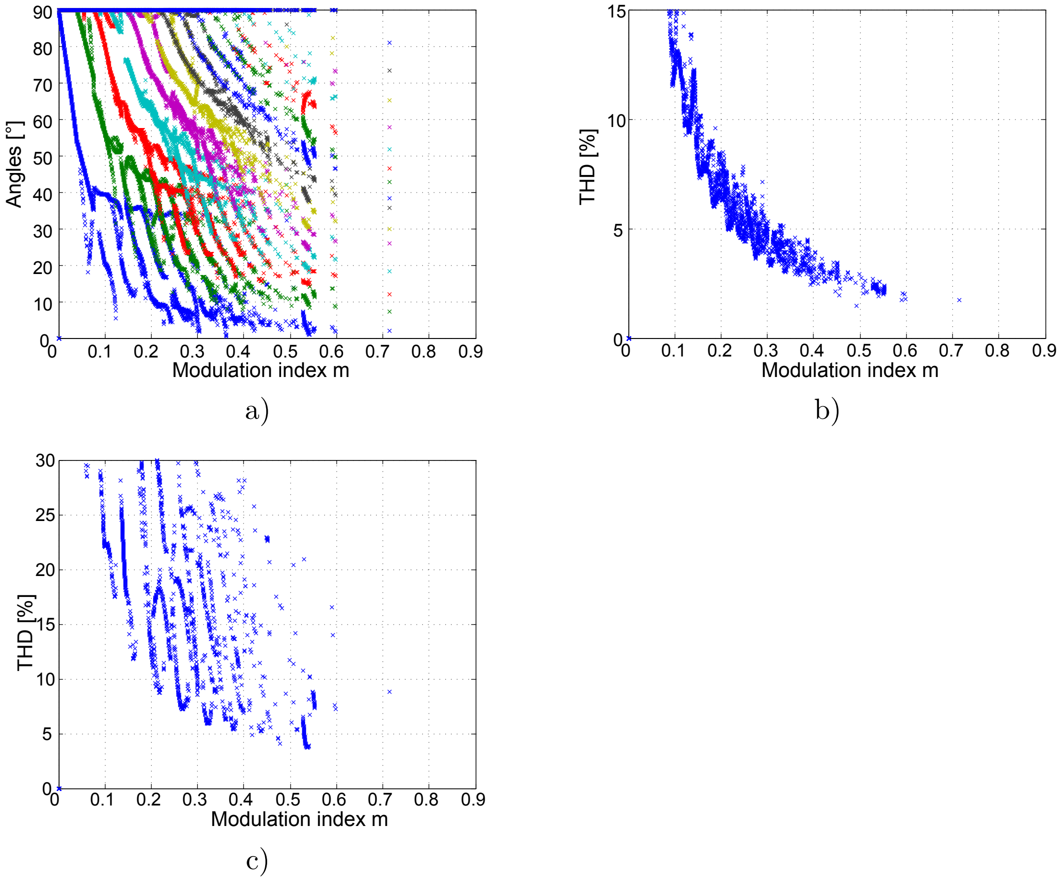
Figure 6.2: 11 level converter a) Switching angles b) THD without triplen harmonics c) THD without triplen harmonics



a) b)

Figure 6.3: Converter with 11 levels with triplen harmonics a) Switching angles b) THD with triplen harmonics

uneven harmonics without the triplen harmonics have been eliminated up to the 43th harmonic. The algorithm is based on an adaptive number of levels: If no convergence is found for a given modulation index and a given number of levels, the number of submodules is decreased by one, until the convergence is obtained or the number of submodules is zero. The equation set is adapted in function of the number of levels, i.e. for a converter with 9 levels only up to the 29th harmonic should be eliminated. In Fig. 6.4a), if the switching angle for a given level is attaining 90°, the submodule is not participating any more in the switching sequence. For a low modulation index, the number of activate levels decreases in consequence. For low modulation indexes $m \leq \frac{5}{15}$, the same solutions are found as in the case with 11 levels, shown in Fig. 6.2a). Fig. 6.4b) shows the corresponding THD, without considering the triplen harmonics. Applying these switching angles to a single phase system yields a higher THD. This is shown in Fig. 6.4c), where the THD contains the triplen harmonics as well.



a)

b)

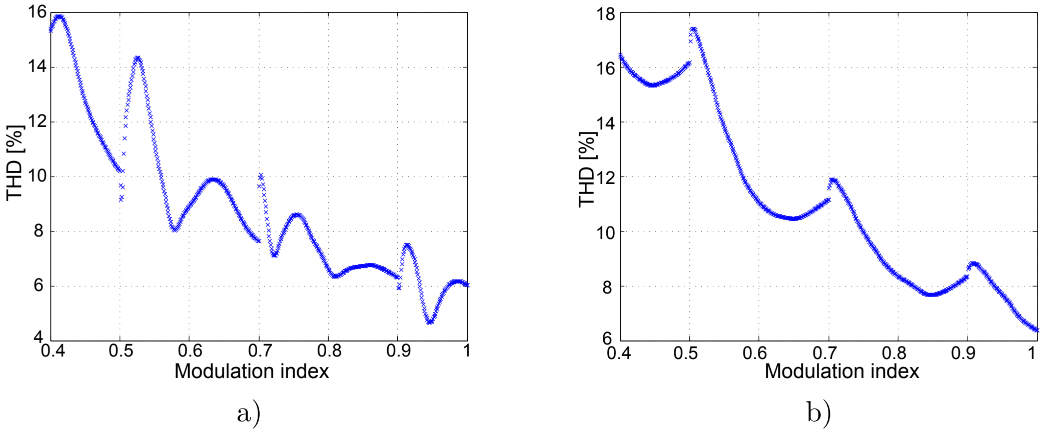
c)

Figure 6.4: 31 level converter with an adaptive number of levels a) Switching angles b) THD without triplen harmonics c) THD with triplen harmonics

If all the harmonics in a single phase circuit will be eliminated, convergence is only given for a relatively narrow range of modulation indexes.

Performance Evaluation NLC The implementation of the NLC is straightforward; however the harmonic performance is inferior to the SHE for a low number of levels.

In this section the THD for different number of submodules will be analysed for their harmonic content. Fig. 6.5a) and 6.5b) show the harmonic content of the 11-level voltage waveform. The harmonic content decreases for higher modulation indexes and unlike the SHE, solutions can be found for modulation indexes higher than 0.8. The THD for 11 levels at a modulation index m=1.0 is below 6% without considering the triplen harmonics (in a three phase system) and slightly above 6% taking into account all harmonics. The solutions for the SHE at the highest modulation index of m=0.8 gives a lower THD of around 5% without triplen harmonics and around 6% taking into account all harmonics.

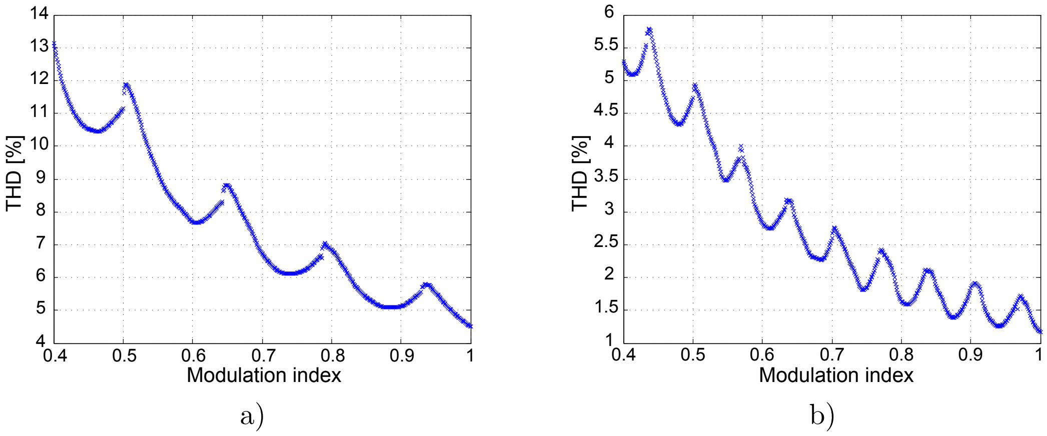


a) b)

Figure 6.5: NLC algorithm: 11 level converter a) THD without triplen harmonics b) THD with triplen harmonics

If the number of levels is increased, the THD is drastically decreasing. Fig. 6.6a) shows the THD for 15 levels, achieving a THD of 4.5% at m=1.0. The THD of a system with 31 levels is shown in Fig. 6.6b), where a THD of around 1.7% is achieved for a modulation index of m=1.0.

Due to the facility of implementation and in regard of the extendibility of the number of submodules, the NLC is more advantageous than the SHE. The limitation of the modulation index of the SHE makes the NLC the modulation of choice and will be implemented in the following. In terms of harmonic content, in particular for high modulation indexes, the NLC is equivalent to the SHE.



a) b)

Figure 6.6: a)THD for 15 levels with triplen harmonics b) THD for 31 levels with triplen harmonics

6.1.2 Control Strategy

In order to cope with the complexity of the MMC, a hierarchical control will be implemented. On the lower level, voltage balancing within a branch must be guaranteed, on the intermediate level the energy balance between the upper and lower branch within a phase leg has the be assured and finally on the highest level the power flow and the input/output characteristics have to be controlled. This control structure is summarised in Fig. 6.7.

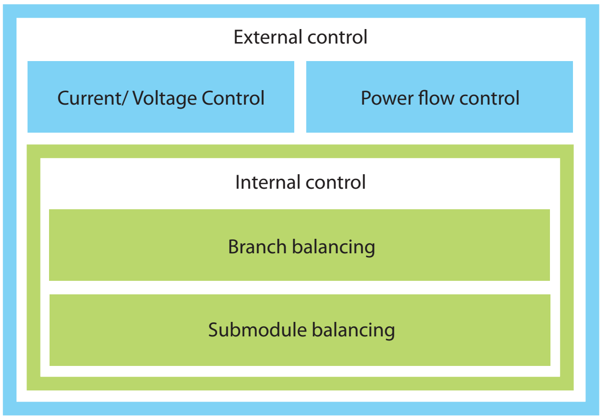

External control
Current/ Voltage Control
Power flow control
Internal control
Branch balancing
Submodule balancing

Figure 6.7: Hierarchical control structure

Inner Control

Balancing of the Branch Submodules The conventional way of assuring balanced submodules within an MMC branch is to measure the capacitor voltages and to establish a ranking of their voltages [88]. In dependence of the current polarity and the established ranking of the submodule voltages, a selection algorithm decides on which submodule to insert or short-circuit in order to maintain the submodule voltages balanced. In order to avoid unnecessary switching actions, only one submodule per switching instant will be inserted or short-circuited. In an MMC branch that is modulated with fundamental switching frequency, each submodule will be inserted and short-circuited once per period of the AC waveform.

Another option is to define a predefined switching pattern that provides a mean of balancing the submodule voltages over several cycles without the need of measuring the different voltages. Depending on the switching pattern, the total energy balance over a complete set of cycles must be assured. The sum of the energies should be zero, i.e. the submodule is charged to the same voltage at the beginning of the cycle and at the end of the cycle.

In [129] a selection method based on a predefined switching sequence is presented. In order to provide zero additional charge of the submodule after the switching sequence, the switching angles have to full-fill two conditions: No additional charge through the active power flow and no additional charge through the reactive power flow. This method requires a N+1-modulation, i.e. synchronous switching in the upper and lower branch of the MMC.

Balancing of the Branches Once the voltages are balanced within a branch, the energy balance between branches has to be assured. This has also been address in section 4.3, where a branch energy controller is assuring the proper energy balance. However, the implementation of a branch energy controller is affecting the output performance in terms of voltage ripple [114].

In order to have a DC link with reduced ripple due to switching actions, the sum of the active submodules in a branch must comply with (6.1).

$$m_u \sum U_{sm,u} + m_l \sum U_{sm,u} = U_{dc} \tag{6.1}$$

m_u respectively m_l are the modulation indexes for the upper respectively the lower branch. This condition is respected if synchronised switching in the upper and the lower branch is given, i.e. every time a submodule is activated in the upper branch, a submodule has to be deactivated in the lower branch. In this case the ripple on the DC link is only due to the branch energy variation. The synchronised operation achieves a voltage resolution of N+1 levels.

However if an inner dynamics controller [111] is used, the condition (6.1) does not hold true and has to be modified according to (6.2). A higher ripple on the DC link can be expected, which has been shown in [114].

$$m_u \sum U_{sm,u} + m_l \sum U_{sm,u} \approx U_{dc} \tag{6.2}$$

The unsynchronised operation allows the branches to work in a completely independent way. The number of activated submodules in the upper branch is not necessarily complementary to the lower branch. This increases the number of output levels to 2N+1 levels.

The difference between the case where an inner dynamics controller is used and the case where a direct modulation is applied lies in the harmonics added by the inner dynamics controller that is controlling the branch energies. Some authors mention [94] that without an intrinsic branch energy control, the capacitor voltages become unstable. It has been shown in section 4.2.2 that the natural tendency of the converter is to balance the energies in the upper and lower branch.

External Control

The power flow in the converter is controlled by phase-shifting the voltage waveforms at the level of the transformer. The phase shift controller of Fig. 6.8 is controlling the output voltage by adjusting the phase-shift of the primary and secondary transformer terminal. This kind of control is preferred, since the number of needed measurements is minimised, only the output voltage and output current needs to be measured to control the power flow.

The phase shift controller supposes that the magnitudes of the voltages at the transformer terminals stay more or less identical and should not vary too much by changing the power flow. A PI based regulator is controlling the DC output voltage and defines the phase shift δ between the AC voltages of the primary and secondary MMC [80].
In Fig. 6.8, the PI controller, represented by G_R, is fed with the voltage error between the DC voltage reference $U_{dc2,ref}$ and the filtered DC voltage measurement $U_{dc2,f}$. The measured load current I_{dc2} is added as a feed-forward component to the PI output I_{reg} and the resulting current I_{ideal} is subject to a limitation block.

The inverse transfer function given in (6.3) of the system MMC-transformer-MMC calculates the phase shift in dependence of the load current I_{out}, issued from the limitation

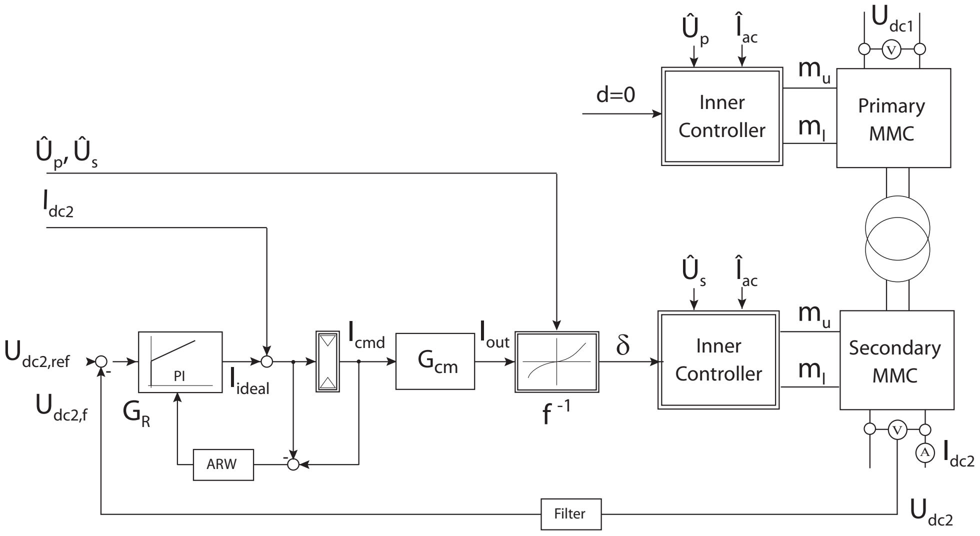

Û_p
Î_ac
U_dc1
d=0
Inner Controller
m_u
m_l
Primary MMC
Û_p, Û_s
I_dc2
Û_s
Î_ac
m_u
m_l
Inner Controller
Secondary MMC
U_dc2,ref
PI
G_R
I_ideal
I_cmd
G_cm
I_out
δ
f^-1
U_dc2,f
ARW
Filter
I_dc2
U_dc2

Figure 6.8: DC output voltage control

block. $\hat{U}_p$ and $\hat{U}_s$ are the amplitudes of the voltage waveforms.

$$\frac{sin\delta}{I_{out}} = \frac{2\omega L_{tot} U_{dc2}}{\hat{U}_p \hat{U}_s} \tag{6.3}$$

The phase shift δ can be positive or negative, depending on the direction of the power flow. An Anti-Reset Windup (ARW) block limits the integral component of the controller, when the command I_{ideal} reaches the maximum admissible value. The system shows an integral behaviour characterised by the equivalent capacitance of the MMC. A total number of N_s submodules per phase-leg is connected permanently to the output terminal. Due to the parallel connection of two phase-legs, the equivalent time constant for the control design is defined by (6.4).

$$T_1 = \frac{2C_{sm}}{N_s} \tag{6.4}$$

The transfer function of the PI controller is defined by $G_R = \frac{1+sT_n}{sT_i}$ using the time constants T_n and T_i defined by (6.5) and (6.6). The PI controller is designed by the "symmetrical criteria" [130] because a good rejection of the perturbation quantity I_{dc2} is required.

$$T_n = 4T_{pE} \tag{6.5}$$

$$T_i = 8\frac{K_{cm}}{T_1}T_{pE}^2 \tag{6.6}$$

The equivalent time constant T_{pE} which summarises the small time constants in the system, such as the sampling time T_E, the modulator delay T_{cm}, the estimated delay inserted by the AD conversion, the calculation delay T_{Calc} and the delay introduced by the filter T_f is defined in (6.7) .

$$T_{pE} = T_E/2 + T_{cm} + T_{Calc} + T_f \tag{6.7}$$

The discontinuous behaviour of any converter with switching actions leads to a delay of the applied voltage in respect to its command signal. This comportment is modelled approximately by a first order transfer function G_{cm}, given in (6.8). The parameter T_{cm} depends on the implemented modulator. For the present case T_{cm} is equal to an average delay given by $T_{cm} = \frac{T_E}{2}$, since the carrier that is compared with the duty cycle is a saw-tooth waveform [130]. The gain K_{cm} between the two currents I_{cmd} and I_{out} is equal to 1.

$$G_{cm} = \frac{K_{cm}}{1 + sTcm} \tag{6.8}$$

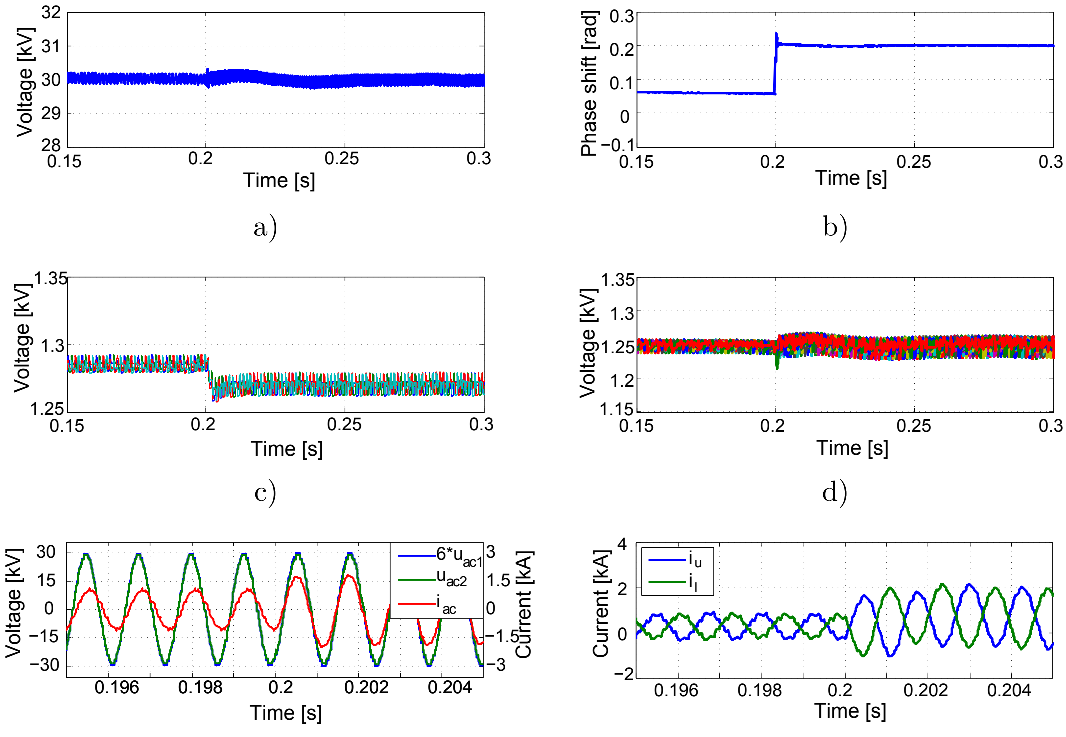
6.1.3 Simulation Results

The single phase structure of Fig. 5.6 has been simulated in MATLAB Simulink using the PLECS library. The converter parameters are based on the values of Table 6.1, where a LV-MV DC transformer is considered of a power of 5 MW. The voltage elevation is done in the transformer with a ratio of 1:6. Since the number of submodules in the primary are rather low, a relatively high phase shift of $\delta_{max} = 15°$ has been chosen.

A load step has been produced from 2.5MW to 5MW at time instant t=0.2s. The secondary DC voltage U_{dc2} in Fig. 6.9a) is slightly affected, but due to the feed forward strategy the overshoot is quickly compensated and steady state is established after 30ms approximately. The controller output δ is shown in Fig. 6.9b), which represents the phase shift between the sinusoidal references of the primary and secondary MMC. Since the output current is measured, a fast response to load steps is given.

Table 6.1: Simulation parameters for the multilevel modulation

Input voltage U_{dc1}	5kV
Output voltage U_{dc2}	30kV
Nominal power P	5MW
Transformer ratio	6:1
AC frequency	800Hz
Primary branch inductance L_p	$1.1e^{-4}H$
Secondary branch inductance L_s	$1.8e^{-5}H$
Number of submodules in the primary	4
Number of submodules in the secondary	24
Rated voltage of 1 submodule	1.25kV
Design criteria δ_{max}	15°



a)

b)

c)

d)

e)

f)

Figure 6.9: Simulation results: a) DC voltage U_{dc2} b) Control parameter δ c) Primary submodule voltages d) Secondary submodule voltages e) AC quantities at the level of the transformer f) Branch currents in the primary MMC

In Fig. 6.9c) and Fig. 6.9d) the submodule voltage of the primary and secondary MMC are depicted. After the load step, the average voltage of the capacitor is decreased, nevertheless they remain balanced at all times. Fig. 6.9e) shows the AC quantities at the level of the transformer. The voltage has the typical multilevel waveform with low harmonic content. In Fig 6.9f) the branch currents of the primary MMC are shown. According to (4.22) and (4.23) the branch current sinusoidal with a DC offset, which can be confirmed here.

6.1.4 Start-Up Strategy

The MMC can be charged from either side, the high voltage or the low voltage side. Basically two steps are necessary, the charge of the first MMC and then the charge of the second MMC, which are described here after.

Charging of the First MMC

Connecting an MMC uncharged directly to a grid would cause high inrush currents that can destroy the semiconductor devices. Therefore putting a charging resistor in series with the converter during the charging of the first converter is indispensable. The following steps have to be followed for the charging:

- A charging resistor has to be connected in series with the first MMC in order to limit the inrush current. The first MMC is in passive state (state "2", Fig. 4.3) and each submodule will be passively charged to $\frac{U_{dc}}{2N}$.

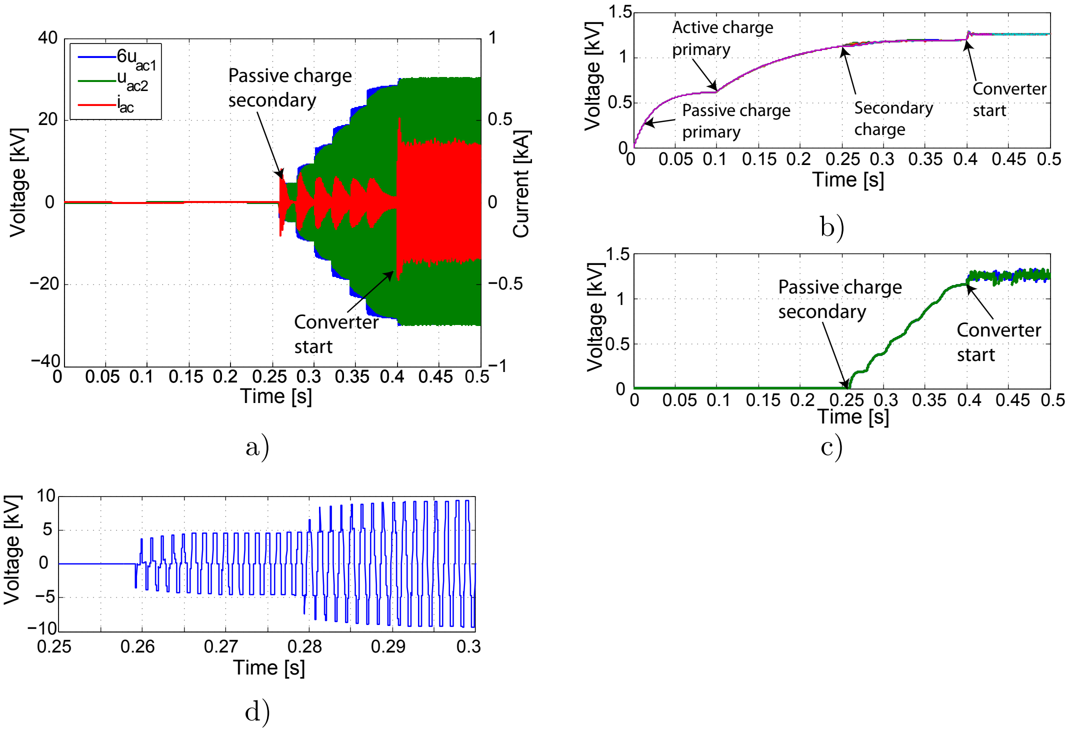
- The first MMC will gradually charge up to its nominal voltage, using the states "0", i.e. short-circuited and "2", i.e. passive mode. The modulation index is chosen in a way to produce zero voltage at the transformer terminals in order not to interfere with the second MMC.

The global modulation index $m(t)$ is zero in the second stage. From (4.63) and (4.64) it becomes clear that the modulation indexes for the upper and lower branch become a constant. The modulation indexes for the upper and lower branch are set to $m_u(t) = m_l(t) = 0.5$. Since the modulation indexes for the upper and lower branch are constants, no AC voltage is produced at the level of the transformer, visible in Fig. 6.10a). The evolution of the primary submodule voltages during the charging procedure is shown in Fig. 6.10b).

Charging of the Second MMC

The charging of the second MMC also follows two steps: First a variable amplitude of the modulation index is applied and than a fixed amplitude of the modulation index. The charging resistor has only been used for the primary and is now disconnected.

Phase 1: Variable Modulation Index Once the first MMC is charged, the secondary MMC can be charged by an initially very low modulation index in order to reduce the inrush currents in the second MMC and the transformer. The second MMC is in passive state and the submodules are charged via the diodes. Gradually the modulation index will be increased, until the secondary MMC is charged up near the nominal voltage. From this point on, the second phase with a fixed modulation index starts.



a)

b)

c)

d)

Figure 6.10: Charging sequence for the primary and secondary MMC a) AC stage quantities b) Primary submodule voltages c) Secondary submodule voltages d) Zoom on the applied transformer voltage during the gradual increase of the duty cycle when starting up the secondary MMC

Phase 2: Fixed Modulation Index Since the difference between the primary and secondary transformer voltage becomes very small, the charging current decreases. At this point, the conventional converter operation can be started and the submodules of the second MMC will be charged up automatically. The amplitude of the modulation index remains constant and the power flow is controlled by the phase shift of the voltage reference between the primary and the secondary MMC.

Fig. 6.10c) shows the submodule voltage of the second MMC. In this example the modulation index is linearly increased, which is illustrated in Fig. 6.10d), where the primary AC voltage is shown. The change from phase 1 to phase 2 where the normal converter operation is started, causes a small transient on the transformer current, visible in Fig. 6.10a).

6.2 Two-Level Modulation Strategies

This section proposes an alternative operation method of the modular DC/DC converter. In contrast to the conventional multilevel operation mode explained in section 6.1, a two-level operation mode is investigated which has important voltage elevation features. This operation mode has been inspired by the DAB [70, 131].

The mathematical developments in section 5.1 derived for sinusoidal references are also valid for the two-level operation if the two-level waveform is approximated by its first harmonic. The harmonic decomposition of a rectangular waveform using the Fourrier series is given in (6.9). $\hat{U}_{rect}$ is the amplitude of the rectangular waveform.

$$u_{ac} = \frac{4}{\pi}\hat{U}_{rect}\left(\sin(\omega t + \delta) + \frac{1}{3}\sin(3\omega t + 3\delta) + \cdots + \frac{1}{k}\sin(k\omega t + k\delta)\right) \tag{6.9}$$

m_{2L} is an equivalent to the modulation index used in AC systems, however here it can only take entire values. The first harmonic is the first term in (6.9):

$$u_{ac}^{1} = \frac{4}{\pi}\hat{U}_{rect}\sin(\omega t + \delta) \tag{6.10}$$

In respect to the development in section 5.1, the only modification is given by the amplitude:

$$\hat{U}_{ac} = \frac{4}{\pi}\hat{U}_{rect} \tag{6.11}$$

The first harmonic of the fundamental square wave is illustrated in Fig. 6.11.

The voltage elevation principle will be explained in section 6.2.1. It is possible to elevate the voltage in the primary and the secondary MMC; the parameter k_p stands for the

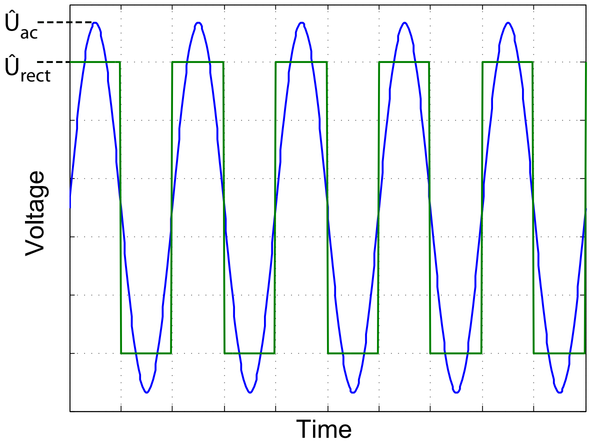


Figure 6.11: Two-level voltage waveform and the first harmonic of the signal

elevation factor of the primary MMC and k_s is the elevation factor of the secondary.

6.2.1 Modulation Strategy

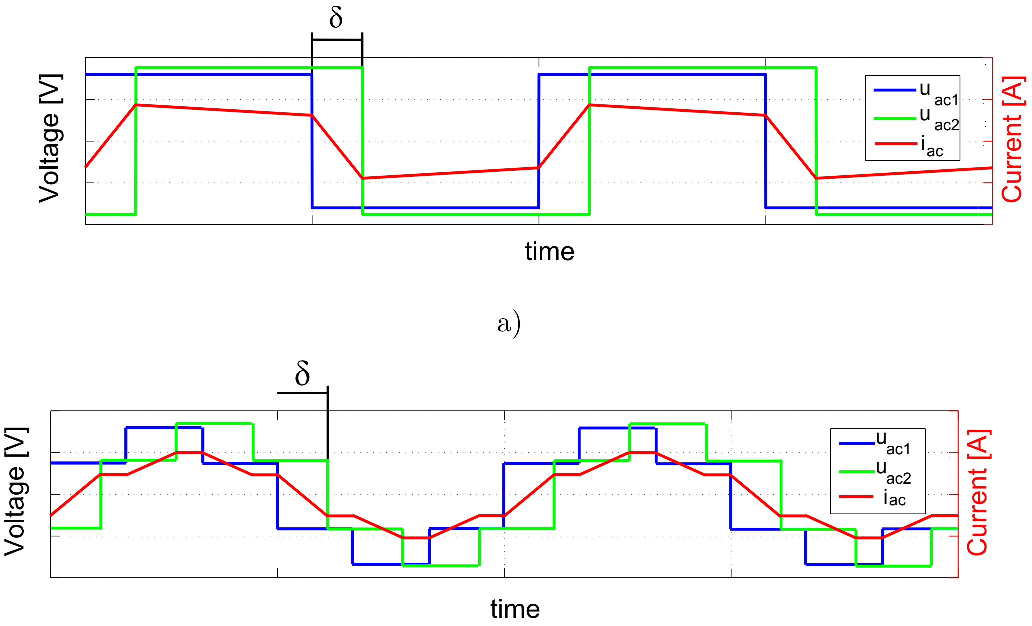
Instead of the multilevel voltage waveform at the level of the transformer, a two-level voltage waveform will be produced. That implies that several switching actions take place at the same time in the MMC converters. Similar to the DAB, the switching actions in the secondary converter are phase shifted in respect to the primary converter.

The two-level modulation provides a mean to elevate an input voltage without necessarily using the transformation ratio of the transformer. For example, choosing a transformer with unitary ratio, the output voltage elevation depends on the number of submodules and the modulation strategy.

As in section 6.1, the converter is working in a fundamental switching mode, which means that the frequency in the transformer is the same as the switching frequency of the submodules. The input of the primary MMC and the output voltage of the secondary MMC can be controlled independently of the AC stage voltages. The modulation of the primary MMC can be distinguished from the modulation of the secondary MMC.

Using a single phase AC stage leads to voltage waveforms as shown in Fig. 6.12a). A three phase AC stage leads to a 4-level voltage waveform, illustrated in Fig. 6.12b). At each voltage step, there are either commutations taking place in the primary MMC or in the secondary MMC. The square wave voltage pattern at the transformer terminals is maintained independently from the DC input or output voltages.

The converter states depicted in the following are only for the positive half-wave of the



a)

b)

Figure 6.12: a) Two-level voltage waveform at the single phase transformer b) Four-level voltage waveform at the three phase transformer

transformer voltage. For the negative half wave, the voltage references for the branches are inverted, that means the references for the upper branch becomes the reference for the lower branch and vice versa.

The Concept of Voltage Elevation

The structure in Fig. 6.13 can be a part of the primary MMC or the secondary MMC. A single phase configuration is considered, but the following explanation can also be applied to a multiphase converter.
There are two cases to differentiate:

1. Considering that the structure from Fig. 6.13 is part of the primary MMC and that a high voltage elevation from the input U_{dc1} to the AC stage u_{ac1} is desired, the voltage u_{ac1} should be as high as possible.

2. If the structure from Fig. 6.13 is part of the secondary MMC, and the aim is to have a high output voltage U_{dc2}, the voltage on the transformer terminal u_{ac2} should be as low as possible.

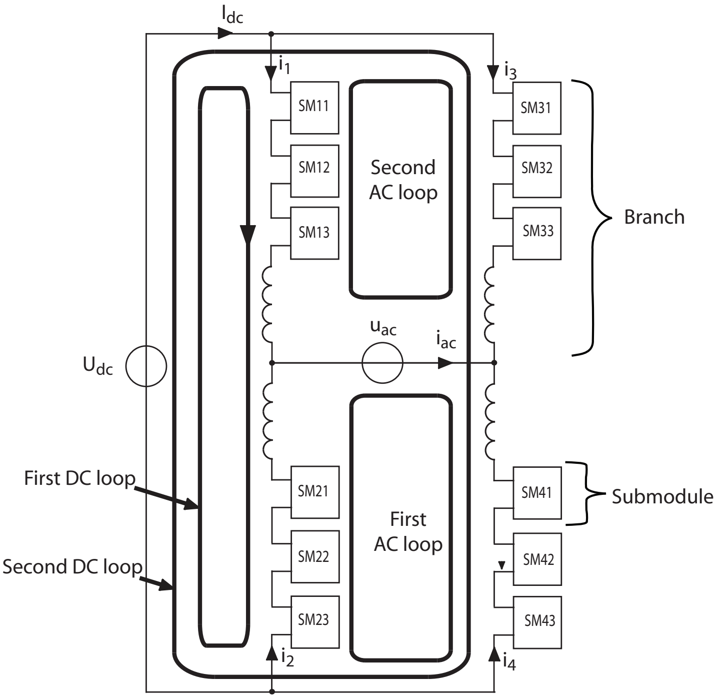

Idc
i1
i3
SM11
SM12
SM13
Second
AC loop
SM31
SM32
SM33
Branch
uac
iac
Udc
SM21
SM22
SM23
First
AC loop
SM41
SM42
SM43
Submodule
First DC loop
Second DC loop
i2
i4

Figure 6.13: Principle of voltage elevation

In Fig. 6.13, a Kirchhoff loop is called "AC-loop", when it forms a closed loop with the transformer AC voltage and two of the MMC branches. There can be several parallel "AC-loops" supplying the AC voltage. If the transformer has several phases, several AC-loops feed the different transformer phases. The "DC-loop" on the other hand is a loop formed with the DC source and two branches. In Fig. 6.13 there are two different "DC-loops". A branch can take part at the same time in the "DC loop" and the "AC-loop".

The voltage elevation of the primary MMC is determined by the ratio of the number of submodules actively connected in the "AC-loops" N_{ac} over the number of submodules connected in the "DC-loops" N_{dc}. If a voltage elevation is desired for the primary side, bipolar submodules are required. The elevation factor k_p of the primary is defined by (6.12).

$$k_p = \frac{N_{ac}}{N_{dc}} \tag{6.12}$$

As for the secondary MMC the elevation is given by the ratio of the number of active submodules in the "DC loops" N_{dc}, over the submodules of cells in the "AC-loops" N_{ac}. u_{ac2} is the low voltage AC input and U_{dc2} is the high voltage DC output, therefore unipolar submodules can be employed. The elevation factor of the secondary MMC is defined by (6.13).

$$k_s = \frac{N_{dc}}{N_{ac}} \tag{6.13}$$

Considering a converter configuration where the branches contain N_p submodules in the primary MMC and N_s submodules in secondary MMC, a maximal voltage elevation of $2N_p$-1 times can be achieved for the primary and $2N_s$-1 voltage elevation for the secondary MMC.

Primary MMC Modulation

The references for the branch voltages in the primary MMC are set in order to achieve a voltage elevation from the input to the AC voltage.

$$u_{pu} = \frac{k_p}{2}\hat{U}_p \sin\omega t + \frac{U_{dc1}}{2} \tag{6.14}$$

$$u_{pl} = -\frac{k_p}{2}\hat{U}_p \sin\omega t + \frac{U_{dc1}}{2} \tag{6.15}$$

Again the voltage u_{pu} respectively u_{pl} represents the voltage of the upper respectively lower branch of the primary MMC and k_p the voltage elevation from the input stage U_{dc1} to the AC voltage u_{ac1}.

Neglecting the voltage drop on the branch impedance, the input voltage U_{dc1} is given by the sum of the two branch voltages u_{pu} and u_{pl} and the AC voltage u_{ac1} by their difference:

$$u_{ac1} = u_{pu} - u_{pl} \tag{6.16}$$

$$U_{dc} = u_{pu} + u_{pl} \tag{6.17}$$

In this section possible modulation strategies for the primary MMC are detailed.

Using Unipolar Circuits in the Submodules Using unipolar submodules in the primary MMC, only a unipolar input voltage can be accepted (typically a DC network or equivalent) and there is no voltage elevation and the amplitude of the AC voltage is either equal or lower than the DC input voltage.

Using Bipolar Circuits in the Submodules The negative terminal voltage of the submodule enhances the degrees of freedom and makes a voltage elevation possible in the primary. To achieve a high voltage elevation, the number of active submodules in the current loop of the input source U_{dc1} should be as low as possible. At least the equivalent of one submodule must be activated, otherwise the source U_{dc1} is shorted-circuited. This can also be achieved by activating submodules (state "1") in series with the inversely connected submodules (state "-1"). At the same time, to achieve high voltage elevation ratios the number of activated submodules (state "1") in the "AC-loop" should be increased. This can be done by connecting the submodules of one branch which are in state "1" in series with the inversely connected submodules (state "-1") of the second branch in the same "AC-loop".

Example for a Voltage Elevation Ratio of 5: As an example, an MMC with 3 submodules per branch is considered with a 3/-2-modulation. In this modulation two "AC-loop" are created, illustrated in Fig. 6.14. The upper "AC-loop" is formed by the AC voltage u_{ac1}, branch 1 and branch 3 and the lower "AC-loop" is formed by the voltage u_{ac1}, branch 2 and branch 4. The sum of the positively and negatively inserted submodules is the same for both "AC-loops" and in this example equal to $N_{ac} = 3 + 2 = 5$ submodules. The sum of the submodule terminal voltage in either "AC-loop" should be maximized if a high voltage elevation ratio is aimed. Two "DC-loops" appear, the first consisting of the input voltage U_{dc1}, branch 1 and branch 2 and the second formed by the input voltage U_{dc1}, branch 3 and branch 4. The equivalent number of activated submodules (in state "1" or "-1") is identical for both "DC-loops" and in this example equal to $N_{dc} = 3 - 2 = 1$ submodule. Again the number of equivalently activated submodules (the difference between directly and inversely connected submodules) should be minimised to increase the voltage elevation ratio. The elevation ratio for this example is therefore $k_p = \frac{N_{ac}}{N_{dc}} = 5$.

The AC current i_{ac} is shared between the two "AC-loops" and the current stress for the submodules is therefore decreased. The input current I_{dc1} is shared between the two "DC-loops", according to section 5.1.

By using bipolar submodules, the input voltage U_{dc1} does not need to be unipolar: Negative and positive input voltages can be created, but the elevation ratio is inverse proportional to the resolution of the input voltage in case a sinusoidal waveform has to be created.

Secondary MMC Modulation

In the secondary MMC the references for the branch voltages u_{su} and u_{sl} are given in (6.18) and (6.19).

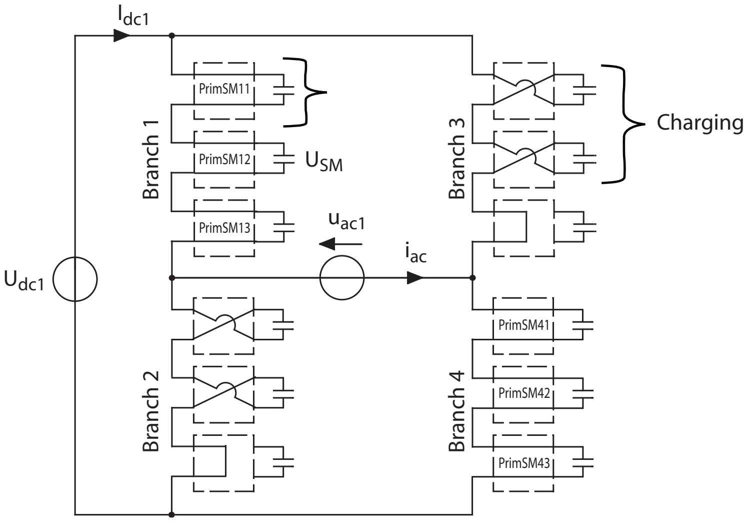


Figure 6.14: Primary modulation strategy for full-bridges with a 3/-2-modulation

$$u_{su} = +\frac{\hat{U}_s}{2}\sin\left(\omega t + \delta\right) + \frac{k_s}{2}U_{dc2} \tag{6.18}$$

$$u_{sl} = -\frac{\hat{U}_s}{2}\sin\left(\omega t + \delta\right) + \frac{k_s}{2}U_{dc2} \tag{6.19}$$

$\hat{U}_s$ is the amplitude of the first harmonic of the reference transformer voltage. k_s is the voltage elevation from the AC voltage u_{ac2} to the output voltage U_{dc2}.

The AC voltage u_{ac2} is given by the difference of the two branch voltages u_{su} and u_{sl}. The output voltage U_{dc2} is defined by the sum of the two voltages u_{su} and u_{sl}.

$$u_{ac2} = u_{su} - u_{sl} \tag{6.20}$$

$$U_{dc2} = u_{su} + u_{sl} \tag{6.21}$$

The modulation of the secondary MMC aims at elevating the AC voltage u_{ac2} at the transformer to the output voltage U_{dc2}. Inversely to the primary MMC modulation, the sum of the submodule terminal voltages in the "AC-loop" should be as low as possible and the sum of the submodule terminal voltages in the "DC loop" as high as possible in order to get a high voltage elevation ratio.

Using Unipolar Circuits in the Submodules Using submodules with a unipolar voltage at their terminals, only unipolar output voltages are possible. Again an MMC with 3 submodules per branch is considered for the example.

Example for a Voltage Elevation Ratio of 5: In this example a 3/2 modulation has been applied. Two "AC-loops" are created, illustrated in Fig. 6.15. The upper "AC-loop" is formed by the AC voltage u_{ac2}, branch 1 and branch 3 and the lower "AC-loop" is formed by the voltage u_{ac2}, branch 2 and branch 4. The sum of the positively inserted submodules is the same for both "AC-loops" and in this example equal to $N_{ac} = 3 - 2 = 1$ submodule. The sum of the submodule terminal voltage in either "AC-loop" should be low if a high voltage elevation ratio is desired.

Two "DC loops" appear, the first consisting of the output voltage U_{dc2}, branch 1 and branch 2 and the second formed by the voltage U_{dc2}, branch 3 and branch 4. The equivalent number of activated submodules is identical for both "DC-loops" and in this example equal to $N_{dc} = 2 + 3 = 5$ submodules. The number of equivalently activated submodules should be high in order to obtain a high voltage elevation ratio. The elevation ratio for this example is therefore $k_s = \frac{N_{dc}}{N_{ac}} = 5$.

The AC current i_{ac} is shared between the two "AC-loops" and the current stress for the submodules is therefore decreased. The current I_{dc2} is shared between the two "DC loops", according to section 5.1.

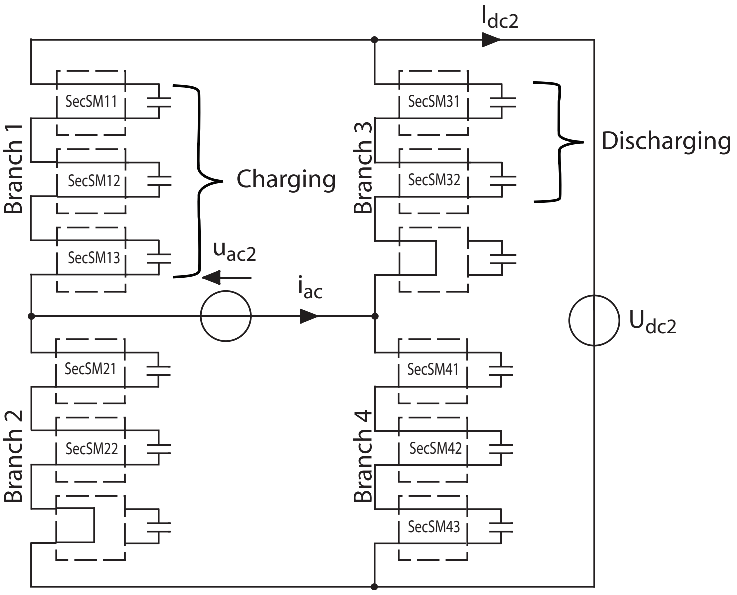
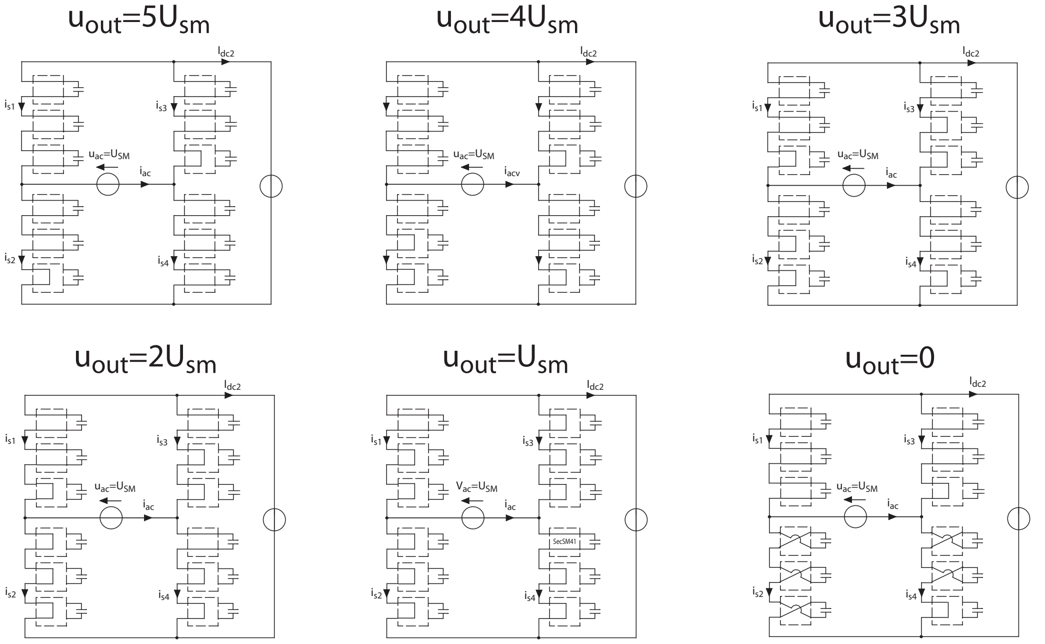


Figure 6.15: Secondary elevation ratio of 5 with a 3/2-modulation

Using Bipolar Circuits in the Submodules If the submodule is a bipolar circuit, the output voltage can be bipolar, an AC output is possible.

Example for Bipolar Output Voltage From a transformer terminal AC voltage peak value of $\hat{U}_{ac} = U_{sm}$ an $4N_s - 1 = 11$ level output voltage can be created. Possible modulation states are depicted for five positive output voltages in Fig. 6.16. For the negative output voltage the polarity of the terminal voltage u_x is inverted.


$u_{out}=5U_{sm}$ $u_{out}=4U_{sm}$ $u_{out}=3U_{sm}$

$u_{out}=2U_{sm}$ $u_{out}=U_{sm}$ $u_{out}=0$

Figure 6.16: Secondary MMC with sinusoidal output.

6.2.2 Control Strategy

Internal Control

On the one hand, also for the two-level modulation the conventional approach for balancing the submodules can be applied, where the submodule voltages are measured and a ranking established.

On the other hand, similar to the multilevel modulation, it is possible to introduce a predefined switching pattern if the energy balance of the submodules is assured. For this predefined switching pattern no measurement is required, which is advantageous for an MMC with a high number of submodules.

Predefined Switching Pattern The main concern is to charge and discharge the different submodules equally over one complete sequence. In the two-level modulation the submodules are connected during a fixed time, which is the same for all the active submodules. A complete cycle defines the number of different states which have to be

run through in order to charge and discharge all the submodule equally. For a converter with N submodules per branch, at least N states are needed for the charging and at least N states are needed for the discharging. Therefore a complete cycle is defined with 2N states, that makes N periods of the AC signal.
Transients may lead to an unbalance in the submodule voltages. However, the energy balance will be restored, as it has been explained in section 4.2.2.

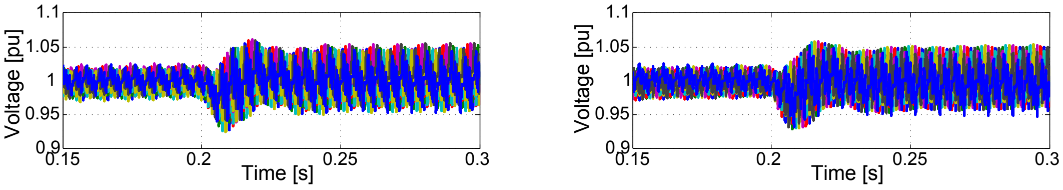
An example will illustrate the problem: The sequence from table 6.2 is applied to the secondary MMC. A converter with 7 submodules per branch realises an elevation of $k_s = 6$ using a 7/5-modulation. During the positive half-wave of the two-level voltage waveform, 7 submodules are connected (which are charged) and during the negative half wave 5 submodules are connected (which are discharged). Table 6.2 defines the insertion order, which for the conventional balancing algorithm is based on measurements and the sorting of the submodule voltages. The letters A-N label 14 different switching patterns and the numbers 1-7 are the numbers identifying each submodule. The submodules that are inserted are framed with gray. Every line corresponds to either the positive or negative half wave of the AC waveform on the level of the transformer.

A	1	2	3	4	5	6	7	Charge
B	1	2	3	4	5	6	7	Discharge
C	2	3	4	5	6	7	1	Charge
D	2	3	4	5	6	7	1	Discharge
E	3	4	5	6	7	1	2	Charge
F	3	4	5	6	7	1	2	Discharge
G	4	5	6	7	1	2	3	Charge
H	4	5	6	7	1	2	3	Discharge
I	5	6	7	1	2	3	4	Charge
J	5	6	7	1	2	3	4	Discharge
K	6	7	1	2	3	4	5	Charge
L	6	7	1	2	3	4	5	Discharge
M	7	1	2	3	4	5	6	Charge
N	7	1	2	3	4	5	6	Discharge

Table 6.2: Fixed balancing scheme

Each submodule is charged 7 times and discharged 5 times. According to (4.22) and (4.23) the branch current is an alternative current with a DC offset, which explains that the discharging current is higher than the charging current.

Simulation results show that the submodule voltages stays perfectly balanced by applying this predefined switching pattern. A converter with 7 submodules in the secondary has been simulated and a load step from 2.5MW to 5MW is produced at time instant t=0.2s. Fig. 6.17a) shows the submodules that are balanced with this predefined switching pattern. In steady state conditions, each submodule has the same voltage again after the whole sequence, that is 7 periods. As a comparison the submodules balanced with the conventional sorting algorithm are shown in Fig. 6.17b).



a) b)

Figure 6.17: Simulation results with a) a predefined switching pattern b) the sorting function

External Control

The control of the power flow and the DC output voltage U_{dc2} is similar to the control strategy presented in section 6.1.2. For the two-level modulation, the controller has to adapt to different set-points, determined by the elevation factors k_p and k_s. The modified control scheme is depicted in Fig. 6.18.

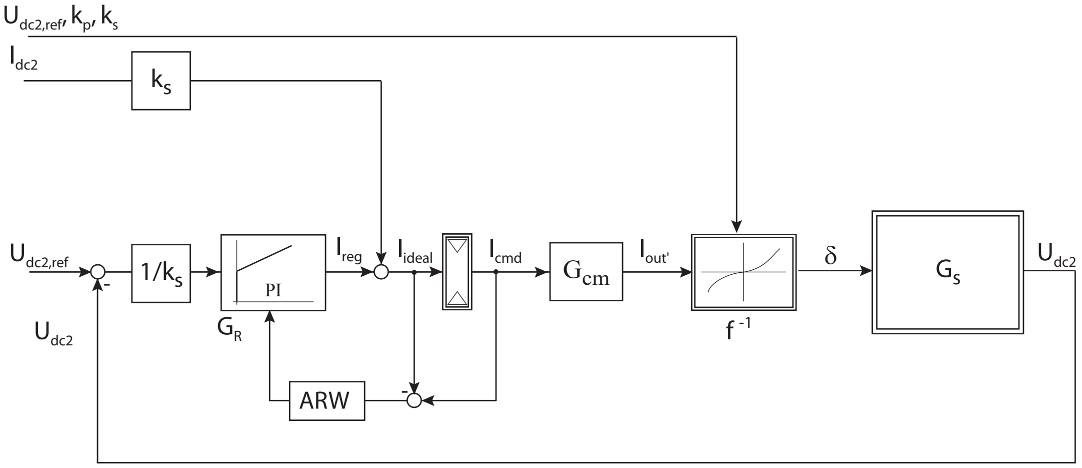


Figure 6.18: Control scheme for the two-level operation

The equivalent time constant T_1 depends on the elevation factor and the number of submodules N_{dc} permanently connected in the "DC-loop". Due to the parallel connection of two phase-legs, the equivalent time constant for the control design is defined by (6.22). When the elevation factor of the secondary MMC k_s changes, the number of submodules in the "DC-loop" N_{dc} changes and therefore also the equivalent time constant T_1.

$$T_1 = \frac{2C_{sm}}{N_{dc}} \tag{6.22}$$

To assure a good response in respect to the perturbation I_{dc2}, the "symmetrical" criteria has been used to determine the PI controller time constants T_i and T_n [130]:

$$T_n = 4T_{pE} \tag{6.23}$$

$$T_i = 8\frac{K_{cm}}{T_1}T_{pE}^2 \tag{6.24}$$

T_{pE} summarises the small time delays, explained in (6.25). f_p is the switching frequency, T_{cm} is the delay regarding the modulator and T_{Calc} is the delay due to calculation and measurement. In average, a command will be executed half a period later, which gives $T_{cm} = \frac{T_s}{2}$ [80].

$$T_{pE} = 0.5/f_p + T_{cm} + T_{Calc} \tag{6.25}$$

The transfer function $G_{cm} = \frac{K_{cm}}{1+sT_{pE}}$ is taking into account the delays between control output and the physical implementation and is modelled as a first order transfer function. The gain K_{cm} between I_{out} and I_{cmd} is 1.

The phase shift that defines the power flow is shown in (6.26). All the control quantities are related to the voltages and currents at the AC stage with the help of the elevation factors k_p and k_s.

$$\delta = asin\left(\frac{2\omega L_{tot}\frac{U_{dc2}}{k_s}I_{out}k_s}{U_{dc1}k_p\frac{U_{dc2}}{k_s}}\right) \tag{6.26}$$

If the entire change in δ is applied, a DC component will be introduced in the transformer current, leading to the demagnetisation of the transformer. Therefore half of the change is applied for the positive half wave and the other half of the change is applied for the negative half wave. The regulator is therefore update only once per period of the AC waveform:

- Positive half wave:
  -Calculation of δ
  -Application of half of the change $\delta_{new} = (\delta + \delta_{old})/2$
- Negative half wave:
  -Application of the full phase shift $\delta_{new} = \delta$

6.2.3 Simulation Results

The following simulation results are based on the parameters of Table 6.3.

In Fig. 6.19a), the AC voltages and current are shown with the predicted two-level waveforms of 1kHz. In the primary MMC an elevation of $k_p = 3$ is achieved with an 2/-1-modulation. Therefore the amplitude of the primary transformer voltage is $\hat{U}_{ac1} = k_p U_{dc1} = 3.6kV$ (without taking into account the voltage drop on the branch inductance and resistance).
The secondary MMC is elevating the voltage with a factor $k_s = 5$, therefore the output voltage is $U_{dc2} = k_p k_s U_{dc1} = 18kV$. A 9/6-modulation has been used, leaving 3 submodules for redundancy reasons. At t=0.2s, a load step from 0.18MW to 0.36MW shows the performance of the DC output voltage regulator, which controls the phase shift between the two-level AC waveforms u_{ac1} and u_{ac2}. Except for a small transient, the output voltage U_{dc2} in Fig. 6.19b) remains unaffected by the load step and the current I_{dc1} respectively I_{dc2} in Fig. 6.19c) receptively in Fig. 6.19d) doubles. In Fig. 6.19e) and Fig. 6.19f) the voltages of the primary and secondary submodules are shown. The voltage ripple on the capacitor increases with a higher load.

At time instant t=0.5s, the elevation factor of the secondary MMC is changed from $k_s = 5$ to $k_s = 7$. The output voltage U_{dc2} rises from 18kV to 25.2kV, shown in Fig. 6.19b). The dissipated power in the load is almost doubled, visible in Fig. 6.19c), however the output current I_{dc2} in Fig.6.19d) increases only to 28A.

As an example, in a second simulation the primary elevation factor k_p is changed from $k_p = 3$ to $k_p = 5$ at t=0.3s. Since the same modulation is maintained in the secondary MMC, the submodules of the secondary converter will be charged due to the higher

Table 6.3: Simulation parameters for the two-level modulation

Input voltage U_{dc1}	1.2kV
Output voltage U_{dc2}	18kV, 25.2kV
Nominal power P	0.36MW
Transformer ratio	1:1
AC frequency	1kHz
Primary branch inductance L_p	$5.5e^{-4}H$
Secondary branch inductance L_s	$3.7e^{-5}H$
Number of submodules in the primary	4
Number of submodules in the secondary	12
Rated voltage of 1 submodule	1.25kV
Design criteria δ_{max}	12°

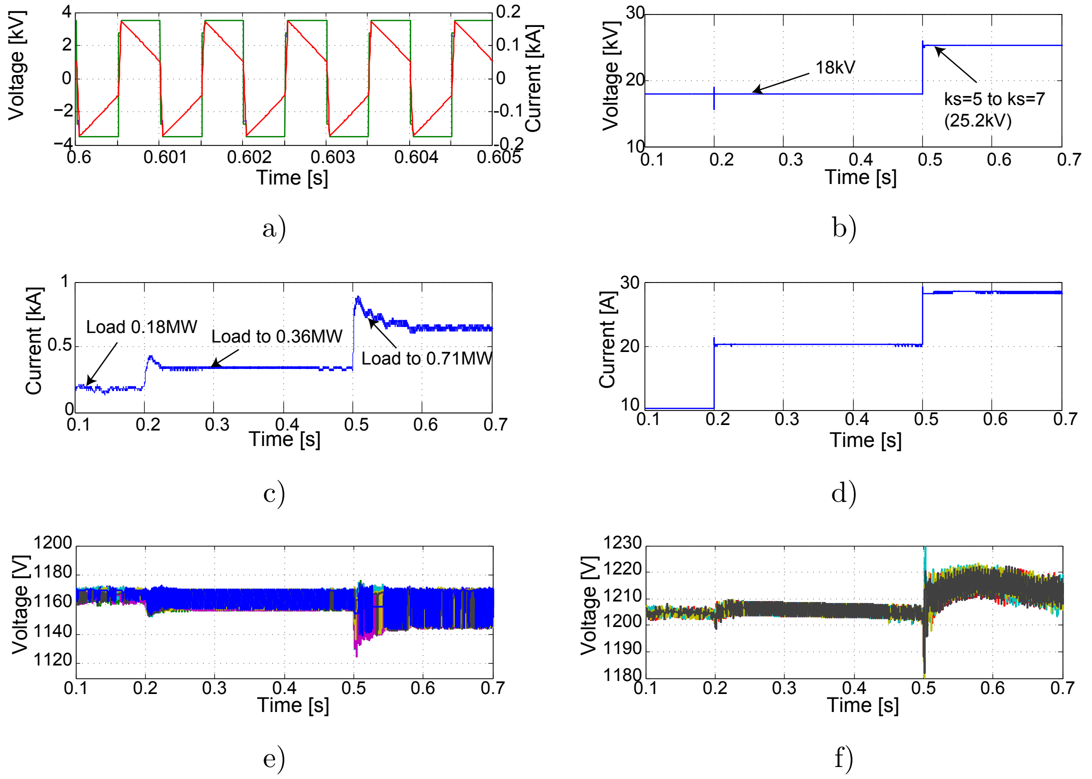
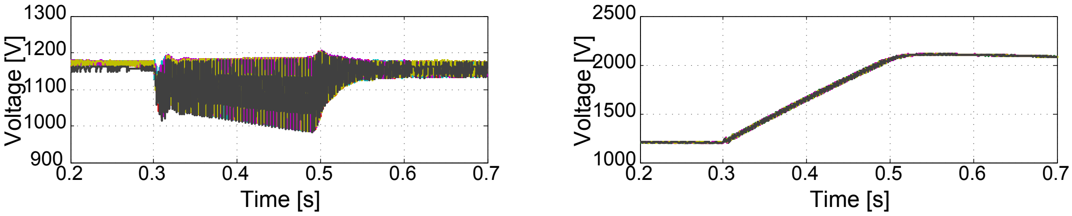


Figure 6.19: Simulation results: a) AC stage quantities u_{ac1}, u_{ac2} and i_{ac} b) Output voltage U_{dc2} c) Input current I_{dc1} d) Output current I_{dc2} e) Primary submodule voltages f) Secondary submodule voltages

transformer voltage. The equivalent number of submodules connected in the "AC-loop" of the secondary with a 9/6-modulation is $N_{ac} = 9 - 6 = 3$. With the initial elevation of $k_p = 3$, the secondary submodules are charged to about 1.2kV. When the elevation factor changes to $k_p = 5$, the amplitude of the primary transformer voltage rises to $\hat{U}_{ac1} = k_p U_{dc1} = 6kV$ and the secondary submodules are therefore gradually charge to $\hat{U}_{ac1}/N_{ac} = 2kV$, which is shown in Fig. 6.20b). The voltage of the primary submodules remain at the same level, however during the charging of the secondary submodules, the voltage ripple increases, as shown in Fig. 6.20a). The output voltage is controlled and the voltage drop on the branch inductances is compensated with a slightly higher submodule voltage.



a) b)

Figure 6.20: Simulation results: a) Output voltage U_{dc2} b) Secondary submodule voltages

6.2.4 Start-Up Strategy

Similar to the charging procedure depicted in section 6.1.4 for the multilevel modulation, the start-up method for the two-level modulation is performed in two steps. First one MMC is charged up and then the second MMC.

Charging of the First Converter

Again a charging resistor is connected in series with the converter to limit the inrush current when the converter is connected to the DC network. After the first stage of passive charge through the diodes, the converter is modulated in a way that the transformer voltage is zero. The secondary MMC that is charged in a second stage is not influenced. According to the number of connected submodules, the primary submodule can be charged to the desired voltage.

Alternatively the first converter can be charged up with the charging method described in [88], where an additional voltage source connected at the DC terminal is used, rated at the submodule voltage. Sequentially all the submodules except one is short-circuited, so that the additional voltage source is charging only one submodule.

Charging of the Second Converter

Charging the secondary MMC is again done in two steps, first with a variable duty cycle and then with a fixed duty cycle [80]. The charging resistor used during the charging process of the primary converter can now be disconnected.

Phase 1: Variable Duty Cycle The voltages of the submodule capacitors are zero at the beginning; a small duty cycle is imposed in order to avoid high inrush currents. This duty cycle is adjusted considering that the voltage of the capacitors is increasing and the inrush current will decrease while maintaining the same duty cycle. In addition to the current limitation, a proper transformer magnetisation needs to be respected. So each change in the duty cycle is applied in two steps, half of the variation during the positive half cycle and the second half of the variation during the negative half cycle.

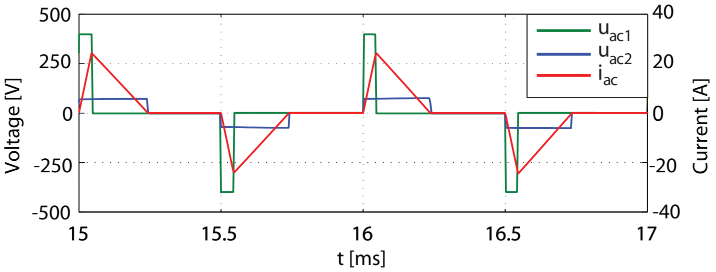


Figure 6.21: Variable duty cycle of the primary AC voltage u_{ac1}, transformer current i_{ac}, secondary transformer voltage u_{ac2}

The second MMC is passive in this phase (state "2"). The secondary submodules are charged sequentially, i.e. the first submodules of a branch are charged first, the second submodules of each branch and so on. The submodule to be charged is deactivated, i.e. in open circuit (state "2"). All other submodules are short-circuited.

In Fig. 6.21, when the voltage u_{ac1} with a low duty cycle is applied at the primary of the transformer, the current is rising, however once the voltage is zero again, the current decreases. The voltage that appears on the transformer secondary u_{ac2} is proportional to the submodule charging state.

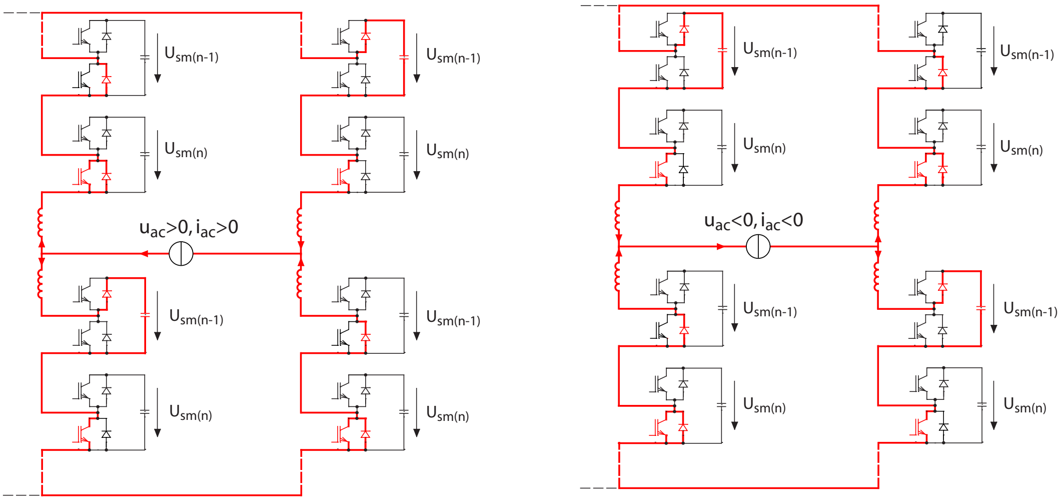
Fig. 6.22 illustrates the state of the secondary MMC during the charging process. During a positive cycle ($u_{ac1} > 0$, Fig. 6.22a)), a submodule from branch 1 and 4 is charged and during a negative cycle ($u_{ac1} < 0$, Fig. 6.22b)) a submodule from branch 2 and 3 is charged.

The transformer inrush current is defined by (6.27). D is the duty cycle of the rectangular waveform.

$$\hat{I}_{ac} = D\frac{U_{dc1} - U_{sm}}{f_p L_{tot}} \tag{6.27}$$

The algorithm for the starting procedure consists of three steps:

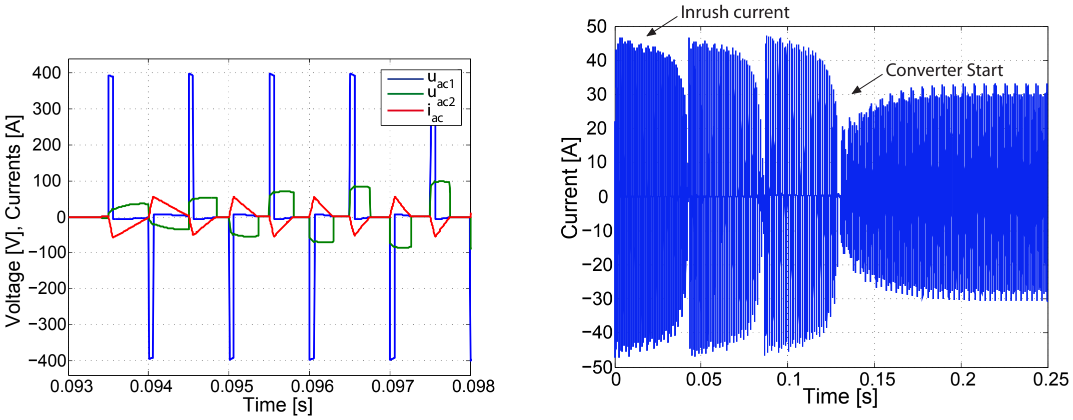
- A new duty cycle is determined: $D_{calc} = \hat{I}_{max} f_p L_{tot} / (U_{dc1} - U_{sm})$
- Only half of the modification is applied: $D = (D + D_{calc})/2$
- Calculation for the negative half-wave, the second half of the variation is applied: $D = D_{calc}$



a) b)

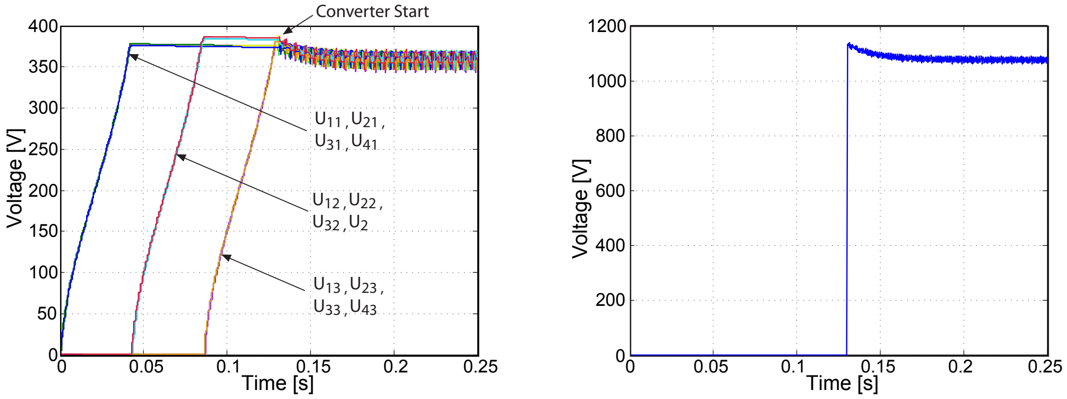
Figure 6.22: Charging sequence for the a) positive half-wave b) negative half-wave

Phase 2: Fixed Duty Cycle The secondary submodules can be charged with the before depicted method, but since the difference of the primary transformer voltage U_{ac1} and the secondary submodule capacitor voltage U_{sm} towards the end gets very small, it is not possible to have the same charging current $\hat{I}_{max}$. A solution is to start the conventional converter operation with a closed loop control. In Fig. 6.23 and Fig. 6.24, the entire charging procedure of the secondary MMC is illustrated. First the secondary MMC is charged up with the variable duty cycle, up to a point where the secondary submodule voltages are around their nominal value. From that point on, the closed loop control is activated.



a) b)

Figure 6.23: Charging of the second MMC in the two-level operation a) Transformer voltages and current with variable duty cycle b) Limited inrush current at the level of the transformer



a) b)

Figure 6.24: Charging of the second MMC in the two-level operation a) Submodule voltage in the second MMC a) DC output voltage

6.3 Protection

Fuses and circuit breakers are required components for the protection of a system during faults. In general DC circuit breakers are not yet as mature as AC breakers and remain costly at high power levels. Many circuit breakers have been proposed [8, 9], but not yet commercialised.

To open a circuit that is carrying a DC current causes an electric arc. In an AC system the arc is extinguished when the current is crossing zero, but for DC systems there is no natural zero for the current.

In [7] several possibilities are described to interrupt a DC current:

- Increasing the distance of the contacts (for the LV region) [132]
- Using the magnetic field to stretch the arc
- Using a resonant circuit which creates a voltage zero so that no arc is created [133]

The use of power semiconductors in a static circuit breaker configuration has opened new possibilities, however the high conduction losses are a serious disadvantage. Hybrid circuit breakers present an interesting alternative using fast mechanical switches and power electronics.

Ideally the grid security is already handled at the level of the DC transformer. In this chapter the fault behaviour or the modular DC/DC converter is analysed and compared to a state of the art DC/DC converter.

6.3.1 Short-Circuit Behaviour

One of the main requirements in the selection of a DC/DC converter for the MV grid is the behaviour of the converter under fault conditions.
At first, faults on the AC sides will be analysed, followed by the analysis of faults on the DC side. Like the DAB, the association of MMC-transformer-MMC builds a single unit, i.e. AC faults are less likely to happen and therefore more focus is set on faults on the DC side.

6.3.2 Fault on the AC Side

A phase-to-ground fault has been depicted in Fig. 6.25a) for the DAB and in Fig. 6.25b) for the modular DC/DC converter. For the DAB, both capacitors on the DC bus on either side are discharged, because a conduction path exists from the neutral point between the capacitors to the fault. A high fault current flows through the whole converter.

The same fault in an MMC does not give place to a high short circuit current, since there is no direct connection to a neutral point [119]. The bipolar output voltage U_{dc2} is not affected; however the voltage potential of the positive respectively negative pole has now a sinusoidal component [119].

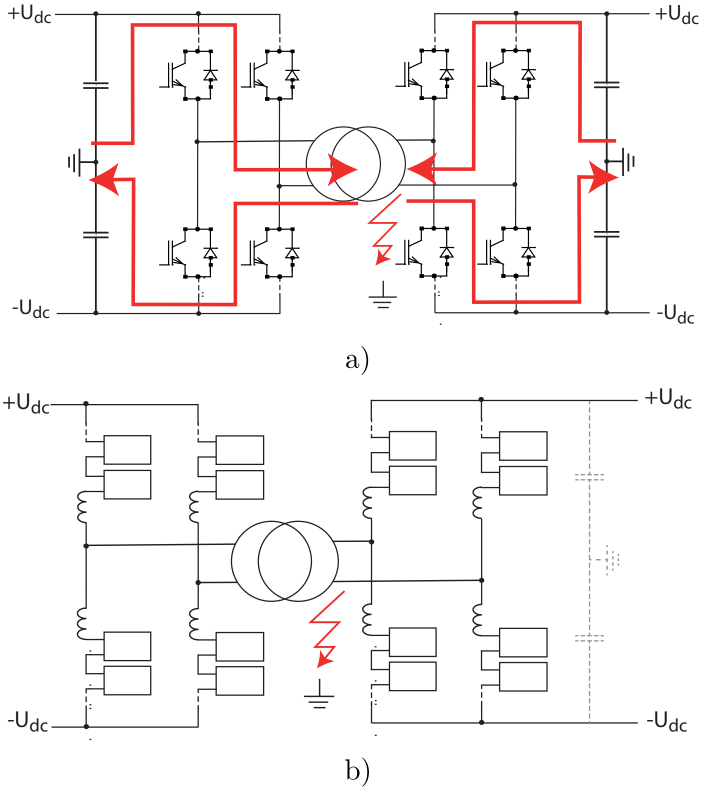
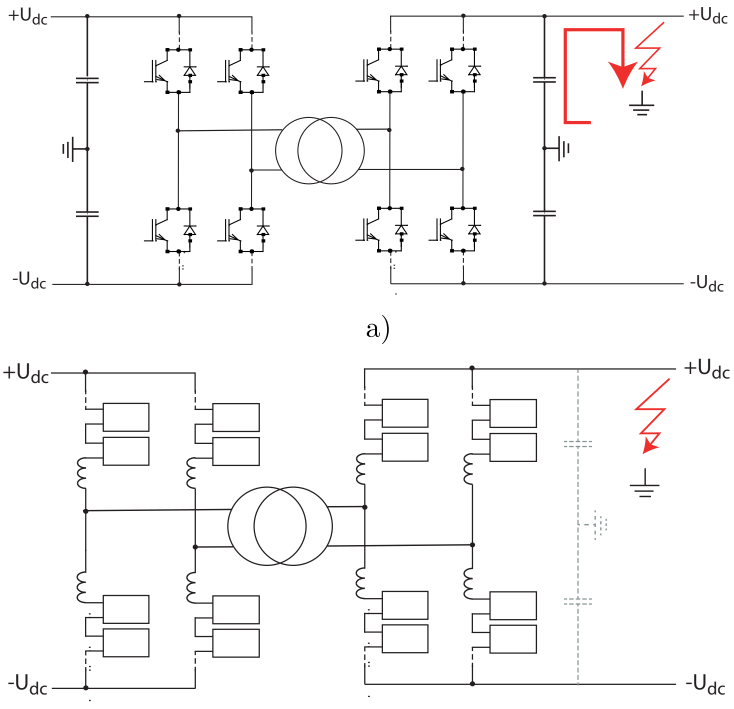


Figure 6.25: AC phase-to-ground faults in a) DAB b) MMC

6.3.3 Fault on the DC Side

Line-to-Ground Fault The most common faults on the DC side are line-to-ground faults, which basically means an isolation failure between a conductor and the ground. In the DAB, the converter has to trip, since the consequence of a short circuit is the discharge of one of the DC line capacitors, illustrated in Fig. 6.26a). If the converter does not trip, the capacitor connected to the faulty line will be discharged and the other capacitor will be charged, which is illustrated in Fig. 6.27a). However even if the fault is cleared, the voltage balance of the two DC link capacitors can still not be restored [134].



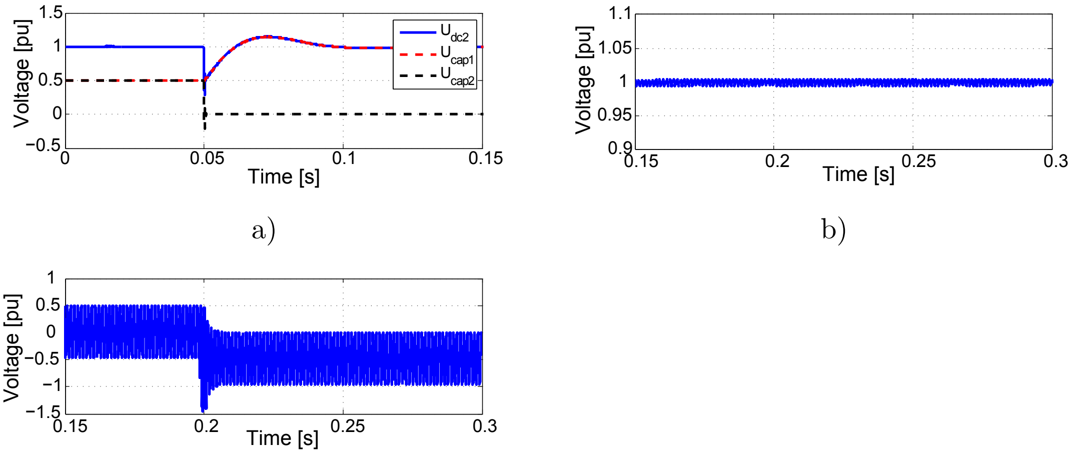
a)

b)

Figure 6.26: DC line-to-ground faults in a a) DAB b) MMC

In an MMC, there is no neutral connection as illustrated in Fig. 6.26b), therefore there is no short-circuit path and only the potential reference changes. The isolation has to be laid out to withstand the increased voltage potential. At time instant t=0.2s, a line-to-ground fault is produced on the MMC based structure. Fig. 6.27b) shows the total DC link voltage which is not affected by the short-circuit. Fig. 6.27c) shows the AC voltage at the level of the transformer where the potential reference has been changed.

This condition holds true if the distance from the MMC to the fault is short. A transmission or distribution line connected to the terminals has some distributed impedance allowing a ground path which affects the short-circuit behaviour. In Fig. 6.28, simulation results show the case of a failure in a transmission line at a distance of 10km. In this case, the DC output voltage and the capacitor voltage of the submodules are transiently



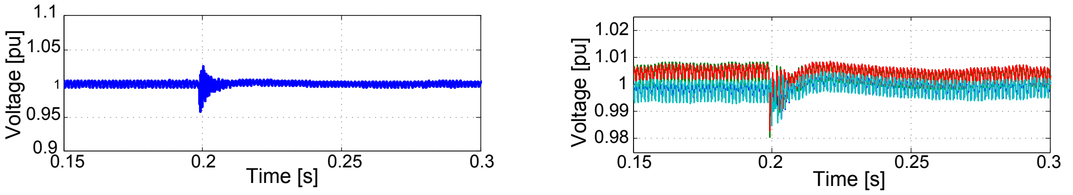
a)

b)

c)

Figure 6.27: DC line-to-ground fault: a) DAB: DC voltages of the capacitors and the line in a DAB, U_{cap1} respectively U_{cap2} are the upper respectively lower capacitor connected to the DC bus; b) MMC: Total DC bus voltage ; c) MMC: AC voltage at the transformer in respect to the ground potential

affected by the short-circuit, however a stable converter behaviour can be guaranteed. Fig. 6.28 shows the effect of the line-to-ground short-circuit on the a) total DC bus voltage and b) the capacitor voltages in the secondary MMC. For the simulation parameters, a conventional 33kV XLPE cable has been considered [135].

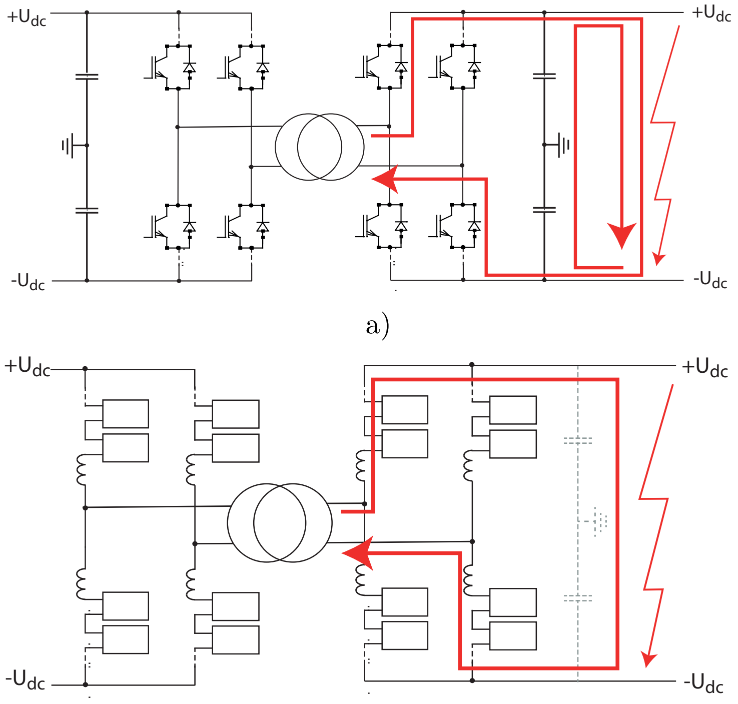


a)

b)

Figure 6.28: MMC: Line-to-ground fault in a DC line at a distance of 10km showing a) the DC bus voltage and b) the capacitor voltages of the secondary MMC

Line-to-Line Fault During a line-to-line fault the capacitors in a DAB on the side of the fault will be discharged immediately and even the AC side is short-circuited through the free-wheeling path of the diodes [134], which is illustrated in Fig. 6.29a). If this happens, the short-circuit current is flowing through the diodes, which have to handle the over-current. In this case the converter should trip, since otherwise the short-circuit is propagated to the primary DC link of the DAB. Fig. 6.30a) shows the evolution of the DC line voltage and the capacitors voltages after a line-to-line fault at time instant t=0.05 s, all of them falling to zero immediately after the fault.

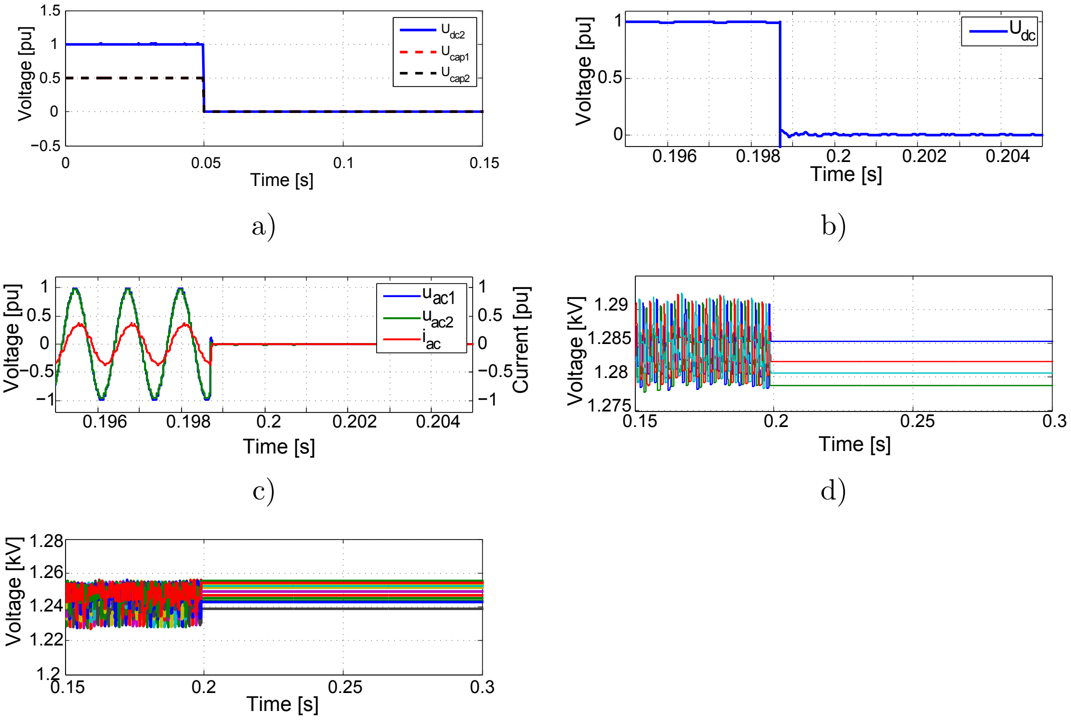


a)

b)

Figure 6.29: DC line-to-line faults in a) DAB b) MMC

In the case of the MMC a line-to-line fault on the DC bus provokes a short-circuit of the transformer shown in Fig. 6.29b). A short-circuit path through the lower diodes of the half-bridge submodules is possible, even if the converter is tripping, since voltage on the capacitors cannot prevent the diodes from conducting. The advantage of the isolated MMC topology is that the primary MMC can be blocked and the short-circuit will not be supplied with any power. Fig. 6.30b) shows the DC link voltage on the side of the fault and Fig. 6.30c) shows the AC quantities at the level of transformer. The submodule capacitors both in the primary and the secondary MMC remain charged, shown in Fig. 6.30d) and 6.30e), which signifies a short down time of the converter. Immediately after the fault clearance, the converter can take up its normal working condition. The blocking time of the converter is short and does not rely on circuit breakers neither at the DC nor on the AC side, which reduces considerable the short-circuit current.



a)

b)

c)

d)

e)

Figure 6.30: DC line-to-line faults a) DAB: Voltage of the capacitor connected to the DC bus and line-to-line voltage; b) MMC: DC link voltage c) MMC: AC quantities of at the level of the transformer; d) Submodule voltages of the primary MMC; e) Submodule voltage of the secondary MMC

7 Efficiency of the Modular DC/DC Converter

One of the most important properties of the Modular DC/DC Converter is its energy efficiency. This performances are dependant on two of the main component categories, namely the electromagnetic voltage transformation in section 7.1 and the semiconductor based converters in section 7.2.

7.1 Influence of the Medium Frequency Transformer

One of the main advantages of the modular DC/DC converter is the fact that the transformer frequency can be chosen freely. In particular when working in the MF range, substantial raw material savings can be achieved. However, more losses can be expected when working at higher frequencies which lead also to an increased operation temperature. The thermal design of a transformer is an optimisation problematic, where a lot of parameters have to be considered. The transformer weight, the cost of the materials or the volume of the transformer can be the optimisation target.

Since transformer design itself can be the topic of a thesis, this chapter will only referred to a transformer design optimisation proposed in [136]. First, the general idea of transformer design is presented, then the results of the design are discussed.

7.1.1 Generalities

The general design equation which helps to understand the relation between the different quantities that characterise a transformer is given in (7.1) [136]. A_w is the cross section of the windings, A_e is the cross section of the core, B_{max} is the maximum flux density in the transformer and S_{rms} is the current density in the windings.

$$A_w A_e \propto \frac{u_{max} i_{max}}{S_{rms} f B_{max}} \tag{7.1}$$

A_e and A_w are both a surface. Assuming that the transformer is a cube with a side length a, the following relation can be established according (7.1):

$$a^4 \propto f^{-1} \tag{7.2}$$

The volume V of the transformer is defined by the side lengths, therefore the volume can now be related to the frequency in (7.3).

$$V \propto a^3 \Rightarrow V \propto f^{-3/4} \tag{7.3}$$

Generally, the losses in a transformer can be separated in three parts:

- Copper losses
- Core losses
- Dielectric losses

Copper Losses Copper losses are the ohmic losses in the windings. The copper losses are influenced negatively by high frequency, since skin and proximity effect increase the equivalent resistance, which is already explained in section 2.1.1. Using Litz wires however reduces greatly their influence and therefore for this approximate analysis skin and proximity effect won't be considered. The equivalent resistance of the windings is proportional to the height of the transformer [137]. The winding losses can therefore also be related to the frequency, shown in (7.4).

$$P_w = R_{ac} i_{rms}^2 \propto a i_{rms}^2 \propto f^{-1/4} \tag{7.4}$$

Core Losses The core losses can be divided in hysteresis losses and eddy current losses. The Steinmetz equation in (7.5) is used to predict the core losses per volume unit V, based on empirical observations [137].

$$\frac{P_{core}}{V} = K f^{\alpha} B_{max}^{b} \tag{7.5}$$

The parameters K, α and b depend on the material characteristic and can be found in the data-sheet of the manufacturer. The Steinmetz equation is specified for sinusoidal flux waveforms. Several methods are proposed for non-sinusoidal waveforms, such as the Modified Steinmetz Equation, the Improved Generalised Steinmetz Equation among others [137]. However, since the dissipated energy per cycle is independent of the voltage shape, the hysteresis losses are not increasing when the voltage shape is non-sinusoidal [67]. Furthermore the eddy current loss is smaller when the voltage shape is a square wave instead of a sinusoidal wave at the same maximum flux density [67].

From (7.5) the relation between the core losses and the frequency is established, which is shown in (7.6).

$$P_{core} \propto f^{\alpha} a^{3} = f^{\alpha - 3/4} \tag{7.6}$$

Dielectric Losses Applying an electrical field to a dielectric material generates heat. The insulation material in a transformer can be represented as an capacitor depending on the geometry of the transformer which is charged and discharged during one cycle. The dielectric losses per unit volume are depicted in (7.7).

$$\frac{P_d}{V} = U^2 \omega \tan \delta C \tag{7.7}$$

where U is the voltage, ω the operation frequency and $\tan \delta$ the loss tangent or dissipation factor, which relates the resistive loss to the reactive power oscillation within the equivalent capacitor C. From (7.7) the relation between the dielectric losses and the frequency is established:

$$P_d \propto f a^3 \propto f f^3 \propto f^{1/4} \tag{7.8}$$

At line frequency, the dielectric losses can be neglected, however with higher frequency these losses can become substantial [67].

Total Losses The sum of the different transformer losses can be summarised using the parameters k_W, k_{core} and k_d, which give a qualitative view of the relation between the different losses:

$$P_{tot} \propto k_W f^{-1/4} + k_{core} f^{1/2} + k_d f^{1/4} \tag{7.9}$$

Depending on the transformer design and the frequency, the core losses are bigger than the windings losses. At higher frequencies, the ratio of the core losses in respect to the winding losses increases.

The transformer temperature is the most critical parameter when it comes to validating the transformer design. Equilibrium is attained when the heat created equals the heat evacuated. The heat increases with higher frequency, according to (7.9). Furthermore if the frequency is increased and the transformer volume decreased, the effective cooling surface is reduced, which causes the temperature to rise. As stated in [136], above a certain transformer frequency the heat production can become too important and reduction of the transformer size does not follow any more the proportionality described in (7.3). A compact transformer design can be maintained if the cooling method is changed. Instead of the natural convection, forced convection or oil cooling can be utilised.

7.1.2 Design Optimisation Procedure

The optimisation procedure described [136] is shown in Fig. 7.1. Based on a given transformer geometry, the winding, core and dielectric losses are determined. The results of the loss analysis are fed to the thermal network model specified in [136]. If any of the temperatures within the transformer exceeds the limits set by T_{max}, the given transformer design is not valid and therefore discarded. The winding temperatures should not exceed 150°C and the core temperatures should remain below 100°C. If the temperatures are respected, the transformer geometry data will be stored and finally compared to other valid solutions to find the optimum regarding the chosen optimisation criteria, which can be cost, volume or weight.

Core Selection

The core material can be classified regarding the operating frequency [137]. The material has a strong impact on the geometry of the transformer. For the modular DC/DC converter, the operation frequency will be below 2kHz, so either silicon-steel or amorphous alloys come into consideration.

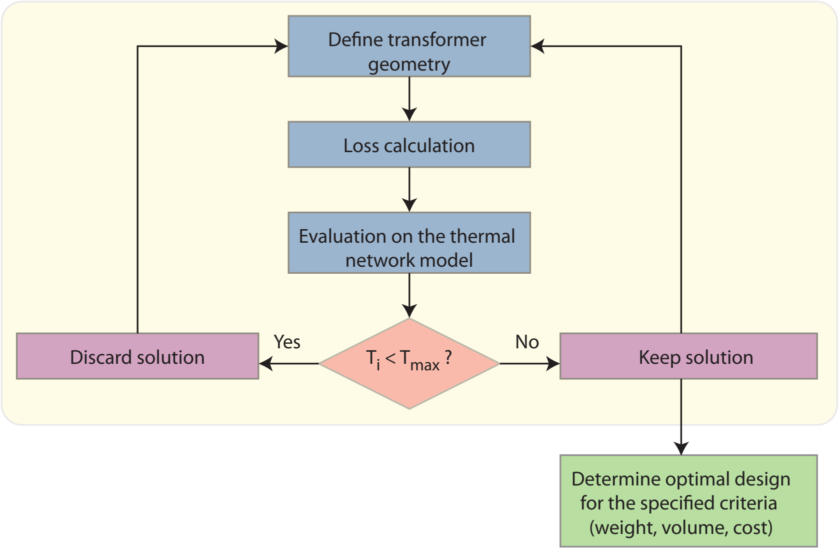

Define transformer geometry
Loss calculation
Evaluation on the thermal network model
$T_i < T_{max}$?
Yes
No
Discard solution
Keep solution
Determine optimal design for the specified criteria (weight, volume, cost)

Figure 7.1: Transformer design methodology

- <1khz : Silicon-Steel (FeSi): Laminated iron cores lead to a high magnetic induction (∼2T) and low cost for high power.

- 1kHz-25kHz : Amorphous and nano-crystalline alloys : At this frequency the losses are to high for Silicon-Steel and amorphous transformer or nano-crystalline alloys are used. Reduced losses and relatively high magnetic induction saturation (∼1.56T) make them the material of choice for this frequency range.

- >25kHz : Ferrites : These materials have low loss densities even at higher frequencies. Due to its low magnetic induction (∼0.5T), these transformers are only suitable for high frequency, because otherwise the size would be a disadvantage in respect to other materials.

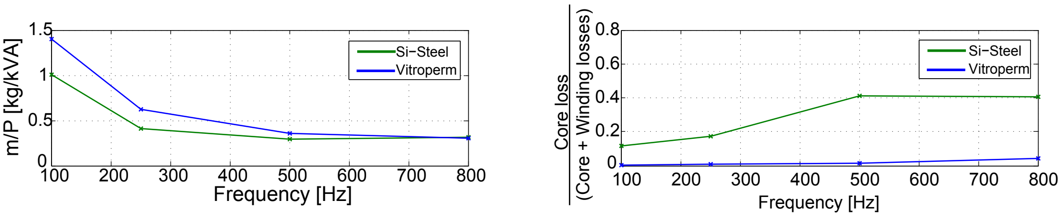
7.1.3 Design Comparison

The designs have been carried out for a core type transformer and Litz-wires. From the loss analysis in section 7.2 it appears clearly that the switching losses are increasing with higher switching frequency. At equal efficiency, the switching frequency in the multilevel configuration is higher than in the two-level operation. Switching frequencies above 1kHz are not advisable, since the efficiency drops below 98% when considering the semiconductor losses. If the total converter size is considered, the two-level operation might be more interesting, because fewer submodules are utilised in comparison to the multilevel operation. In Table 7.1 the parameters for the transformer designs are given. "2L" refers to the two-level modulation and "ML" refers to the multilevel modulation.

Table 7.1: Transformer parameters

Input voltage	5kV
Transformer ratio $N_1/N2$	6 (ML), 1 (2L)
Nominal power	5MVA
Frequency range (ML)	100Hz, 250Hz, 500Hz, 800Hz
Frequency range (2L)	0.5kHz, 0.8kHz, 1kHz, 1.2kHz, 1.6kHz

For the multilevel approach, the results are given in Fig. 7.2. Two different materials are considered, on the one hand SiFe, normally used for lower frequencies and VITROPERM, a nano-crystalline alloy. Fig. 7.2a) shows the normalized mass of the transformer. SiFe is more advantageous in terms of weight at lower frequencies up to 800Hz, where VITROPERM equals the performance in terms of weight. The non-linearity between frequency and mass becomes obvious at higher frequencies. Fig. 7.2b) shows the relation between the core and the winding losses. As stated before, the core losses become more important at higher frequencies. For SiFe the core losses are almost equal to the winding losses, which corresponds to the optimisation criterion specified in [137].

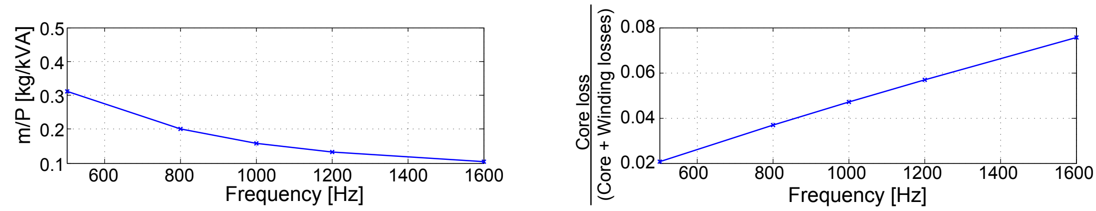


a) b)

Figure 7.2: Transformer design comparison for the multilevel modulation for a SiFe and VITROPERM core a) Normalised mass for different frequencies b) Core loss related to the total loss

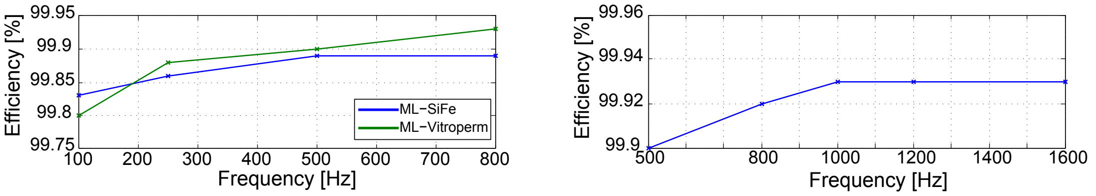
In Fig. 7.3 the design results for the two-level operation is shown. Fig. 7.3a) indicates the normalised mass that decreases with the frequency. At that frequency, the ratio core losses to winding losses is still very small for VITROPERM.

The efficiency for all designs is between 99.8% and 99.93%, shown in Fig. 7.4. In the optimisation procedure only sinusoidal voltage waveforms are considered. For the two-level operation, typically 10% to 15% higher losses have to be expected [136].



a) b)

Figure 7.3: Transformer design comparison for the two-level modulation for a VITROPERM core a) Normalised mass for different frequencies b) Core loss related to the total loss



a) b)

Figure 7.4: Efficiency for the different designs a) Multilevel AC stage b) two-level AC stage

7.2 Semiconductor Loss Evaluation

In this section, a loss analysis of the modular DC/DC converter is made. Switching and conduction losses of the semiconductor devices will be evaluated for a particular case study.

7.2.1 Loss Calculation Model

The loss calculation is based on simulations, which have been done with ideal switches. In a second stage, the switch voltage u_{ce}, the collector current i_C and the command signal provide the necessary information to calculate the conduction and switching losses of the concerning device. This approach makes it possible to analyse the effect of semiconductors from different brands without running the simulation again, which is quite time consuming.

The losses in the transformer, the branch inductances and the capacitors are not considered.

Conduction and switching losses are calculated for several periods of the fundamental AC signal, since not every submodule is necessarily participating during one period of the AC wave, in particular if a certain redundancy is given. This way an average value of the losses is obtained. The parameter κ is introduced, which stands for the number of periods that are considered. The parameter t_s specifies the starting point of the evaluation at a point where the simulation is in steady state. Assuming worst case conditions for the loss calculation, the junction temperature is 125°C.

The conduction losses of the IGBT depend on the transistor currents i_T and the on-state characteristic u_{CE} respectively the diode current i_F and the diode on-state voltage u_F, according (7.10) and (7.11).
When the measured collector current i_C is positive, it flows through the transistor (i_T) and when the current is negative, the current flows through the diode (i_F).

$$P_{con,T} = \frac{\omega}{2\kappa\pi}\int_{t_s}^{t_s+\frac{2\kappa\pi}{\omega}} i_T(\tau)u_{CE}(i_T(\tau))\delta\tau \tag{7.10}$$

$$P_{con,D} = \frac{\omega}{2\kappa\pi}\int_{t_s}^{t_s+\frac{2\kappa\pi}{\omega}} i_F(\tau)u_F(i_F(\tau))\delta\tau \tag{7.11}$$

From the IGBT command, the switch-on instants t_{α_i} and switch-off instants t_{β_i} are determined for the transistor. The turn-off instant of the diode t_{γ_i} coincides with the switch-on instant of the IGBT. The IGBT voltage $u_{CE}(t_{\alpha_i})$ respectively $u_{CE}(t_{\beta_i})$ and current $i_T(t_{\alpha_i})$ respectively $i_T(t_{\beta_i})$ are determined at the switch-on respectively switch-off instants to determine the switching losses $P_{on,T}$ respectively $P_{off,T}$ in (7.12) respectively (7.13). The data-sheet parameters give the typical switching energies for turn-on E_{on} and turn-off E_{off} for the IGBT in dependence of the collector current i_C. To simplify the calculations, the same gate resistor as indicated in the data-sheet is chosen. The switching energy is proportional to the blocking voltage U_{sm} of the device, so the actual switching losses have to be scaled to the test blocking voltage $u_{CE,ref}$ indicated in the data-sheet [138]

$$P_{on,T} = \frac{\omega}{2\kappa\pi}\sum_{i}^{N_\alpha}\left\{\frac{U_{sm}(t_{\alpha i})}{u_{CE,ref}}E_{on}(i_T(t_{\alpha i}))\right\} \tag{7.12}$$

$$P_{off,T} = \frac{\omega}{2\kappa\pi}\sum_{i}^{N_\beta}\left\{\frac{U_{sm}(t_{\beta i})}{u_{CE,ref}}E_{off}(i_T(t_{\beta i}))\right\} \tag{7.13}$$

The turn-on energy of the diode depends mostly on the reverse recovery energy E_{rr}, which is given in the data-sheet of any IGBT device. In a similar manner as the switching energies for the IGBT, the turn-on losses for the diode depend on the current i_F and have to be scaled to the actual blocking voltage. In a simplified manner, the turn-on loss is represented in (7.14).

$$P_{rr,D} = \frac{\omega}{2\kappa\pi} \sum_{i}^{N_\gamma} \left\{ \frac{U_{SM}(t_{\gamma i})}{u_{CE,ref}} E_{rec}(i_F(t_{\gamma i})) \right\} \tag{7.14}$$

The switch-off losses of the diode are in the range of 1% of the switch-on losses and will therefore be neglected.

The blocking state losses will not intervene in the calculation, since they are negligible in respect to the conduction losses.

7.2.2 Case Study

The case study focuses on a wind park with a DC collection, illustrated in Fig. 7.5. Such a configuration has been proposed in [12].

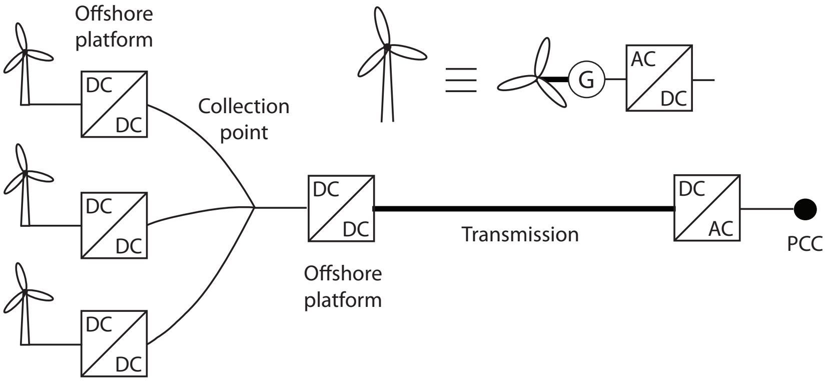


Figure 7.5: Wind park layout for the case study

Wind generator manufacturers propose different turbine output voltages, ranging from 690V, 1kV to 3.3kV and 6.6kV [42, 43]. Generally speaking, it can be expected that turbines with higher output power will use a higher generator voltage [44].

In this case study a generator voltage of 3.3kV will be considered and a low voltage DC bus at 5kV. In Fig. 7.5, a full size active rectifier is connected to the generator and a second converter steps up the intermediate DC bus voltage of 5kV to the collection grid at medium voltage level of 30kV. The case study focuses on the isolated DC/DC converter which steps up the voltage from 5kV to 30kV.

Both the multilevel and two-level modulation will be evaluated in terms of switching losses. The transformer design from section 7.1 has shown that for efficiency considerations the transformer does not have a big influence, since the transformer efficiency is between 99.8% and 99.93%.

The semiconductor model is based on data-sheet parameters. The on-state characteristics $u_{CE}(i_C)$, $u_F(i_C)$ and switching energies $P_{on,T}(i_C)$, $P_{off,T}(i_C)$, $P_{rr,D}(i_C)$ of the device are stored in a table for some discrete values of the collector current i_C.

The selected IGBTs are listed in Table 7.2. The characteristic curves $E_{on}(i_C)$, $E_{off}(i_C)$, $E_{rec}(i_C)$, $V_{CE}(i_C)$ and $V_f(i_f)$ required for the determination of the losses have been stored as a vector in a data-base. In order to determine a particular value for a given current, an interpolation is done.

Table 7.2: Selected IGBT

IGBT code	Rated voltage	Rated current
Infineon FZ400R17KE4	1.7kV	0.4kA
ABB 5SNA 1800E170100	1.7kV	1.8kA
ABB 5SNA 2400E170100	1.7kV	2.4kA
ABB 5SNA 0800N330100	3.3kV	0.80kA
Infineon FZ1500R33HL3	3.3kV	1.5kA
ABB 5SNA 0400J650100	6.5kV	0.4kA

Depending on the modulation half-bridge or full-bridge submodules are used for the primary MMC. For the secondary only half-bridge submodules are used. The denomination of the different switches will follow the same code as in Fig. 7.6.

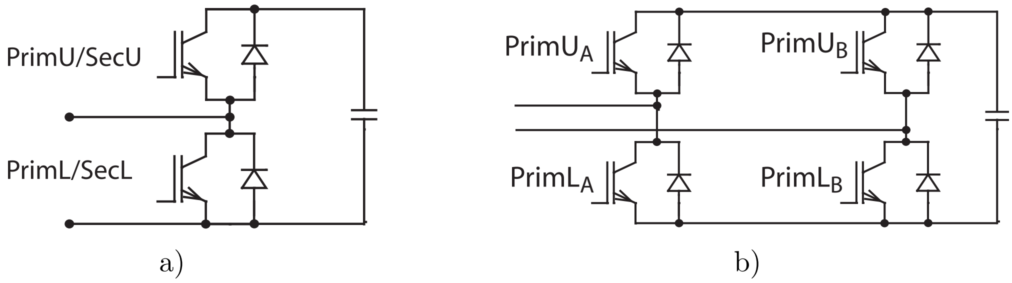


Figure 7.6: a) Half-bridge submodule b) Full-bridge submodule

A first and more detailed loss analysis is performed in section 7.2.2 and a second, shorter analysis for different converter configurations in section 7.2.2.

Converter Analysis A

In order to use similar components for all converter configurations, the nominal submodule voltage is fixed at $U_{sm} = 1250V$ for both the primary and secondary converter. The converter parameters are shown in Table 7.3. N_p receptively N_s are the number of submodules in the primary respectively in the secondary MMC. Three different modulation methods are analysed, the first configuration is using a multilevel modulation (ML) which requires a transformer ratio of 1:6 for the voltage elevation. The second configuration uses a two-level modulation (2L) where the elevation is done in the secondary MMC. The third configuration performs the voltage elevation in the primary and the secondary MMC. From Table 7.3 it becomes obvious that the `ML_4_24`- and the `2L_fb6_16`-configuration require almost double the number of switches in comparison to the `2L_4_14`-configuration.

Table 7.3: Converter configurations A

Denomination	`ML_4_24`	`2L_4_14`	`2L_fb6_16`
Modulation type	ML	2L	2L with FB
Input voltage	5kV		
Output voltage	30kV		
Nominal power	5MW		
Primary submodule voltage	1.25kV		
Secondary submodule voltage	1.25kV		
N_p	4	4	6
N_s	24	14	16
Transformer ratio	1:6	1:1	1:1
Primary voltage elevation k_p	1	1	2
Secondary voltage elevation k_s	1	6	3
IGBT rating of the primary IGBTs	1.7kV, 1.8kA	1.7kV 1.8kA	1.7kV, 2.4kA
IGBT rating of the secondary IGBTs	1.7kV, 0.4kA	1.7kV, 1.8kA	1.7kV, 1.8kA
Number of IGBTs in the primary	32	32	96
Number of IGBTs in the secondary	192	112	128
Total number of IGBTs	224	144	224
Primary switching power [GW]	97.9	97.9	391.7
Secondary switching power [GW]	130.5	342.7	391.6
Total switching power [GW]	228.5	440.6	783.3

- `ML_4_24`-configuration: The NLC algorithm is applied with a fixed modulation index amplitude close to 1. According to section 6.1.1, this is how the lowest harmonic distortion is achieved for the AC waveform of at the level of the transformer. The high modulation index is maintained even for light load conditions, since it is the phase shift that controls the power flow. An N+1 modulation is implemented. Regarding the low number of submodules in the primary MMC and the associated higher harmonic distortion, the design parameter for the inductances has been chosen $\delta_{max} = 15°$, which provides a better filtering of the transformer current.

The nominal voltage of the submodules is given by the relation $U_{sm,p} = \frac{U_{dc1}}{N_p}$ and $U_{sm,s} = \frac{U_{dc2}}{N_s}$.

- `2L_4_14`-configuration: In the primary MMC a 4/0 modulation is chosen, i.e. it is operated as a conventional full-bridge converter either connecting the entire branch or short-circuiting the entire branch in order to produce a two-level waveform at the level of the transformer with an amplitude $\hat{U}_{ac1} = U_{dc1}$. The elevation factor is equal to $k_p = 1$, since the number of submodules connected in the AC-loop and the number of submodules connected in the DC-loop are equal. In the secondary MMC a voltage elevation of 6 is achieved with a 14/10 modulation, i.e. the number of submodules connected per branch varies between 10 and 14. In the DC-loop, $N_{dc} = 10+14 = 24$ submodules are connected and in the AC-loop $N_{ac} = 14-10 = 4$ submodules. The elevation is given by the ratio $k_s = \frac{N_{dc}}{N_{ac}} = 6$. The DC voltage U_{dc2} is distributed on $N_{dc} = 24$ submodules, which gives the nominal voltage of $U_{sm} = 1250V$ per submodule.
- `2L_fb6_16`-configuration: For the primary MMC a 6/-2 modulation is implemented which results in $N_{dc} = 6 + (-2) = 4$ submodules in the DC-loop and $N_{ac} = 6 - (-2) = 8$ submodules in the AC-loop with an elevation of $k_p = \frac{N_{ac}}{N_{dc}} = 2$. The DC voltage U_{dc1} is distributed on $N_{dc} = 4$ submodules which gives a nominal voltage of $U_{SM,p} = 1250V$. In the secondary MMC a 16/8 modulation leads to an elevation factor of $k_s = \frac{N_{dc}}{N_{ac}} = \frac{16+8}{16-8} = 3$.

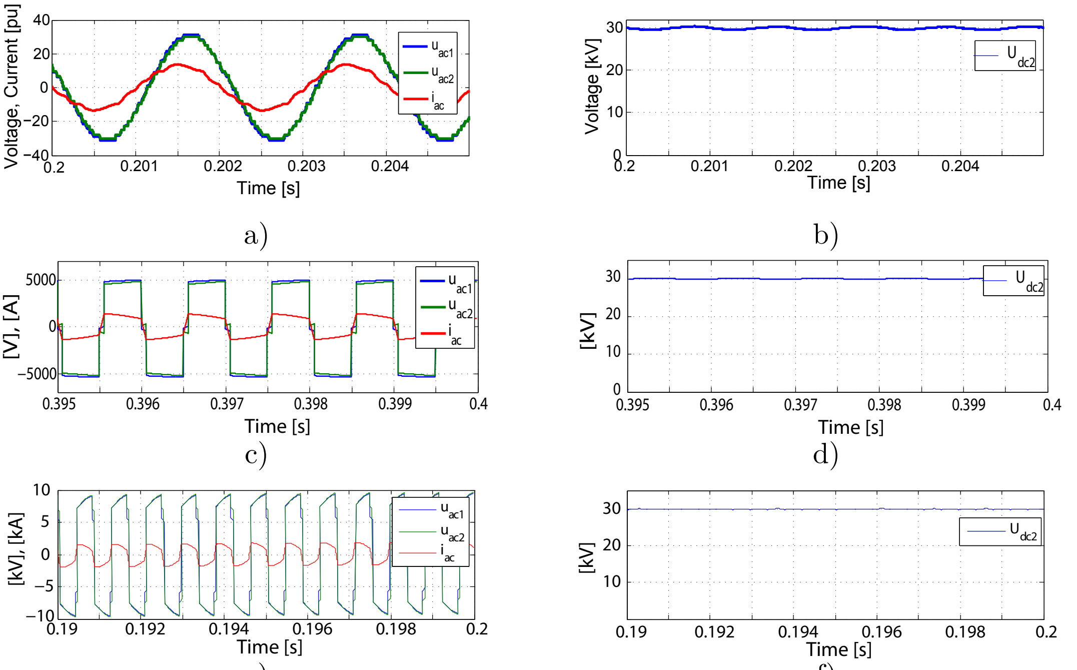
The current rating for the IGBTs can be determined easily according (4.22) and (4.23). For the three configuration the DC input current I_{dc1} and the DC output current is I_{dc2} is the same. In Table 7.4 branch currents are calculated for the three configurations. For this approximate calculation, the reactive power within the converter is not considered and therefore the expected current is higher than the values indicated in Table 7.4. The `ML_4_24`-configuration seems the most promising in terms of current rating.

The basic waveforms of the multilevel and both two-level modulation are shown in Fig. 7.7.

The losses have been evaluated for different frequencies. Since a higher switching frequency is desirable for downsizing the passive components, only switching frequencies higher than 100Hz are considered. The efficiency regarding the semiconductor losses are summarised in Fig. 7.8 for the three configurations. For all of them, there is a clear tendency to decrease the losses when decreasing the switching frequency. Fig. 7.8a) shows the efficiency of the `ML_4_24`-configuration, which shows the best results out of the three configurations. 99% efficiency over a large range of power is achieved at 100Hz. The efficiency is still higher than 98% for a large range with a switching frequency of 1kHz. The efficiency for the `2L_4_14`-configuration, shown in Fig. 7.8b), is only higher than 98% for switching frequencies lower than 800Hz. For the `2L_fb6_16`-configuration, efficiencies

Table 7.4: Branch currents for the different configurations

Denomination	`ML_4_24`	`2L_4_14`	`2L_fb6_16`
Primary transformer voltage $\hat{U}_{ac1}$	5kV	5kV	10kV
Secondary transformer voltage $\hat{U}_{ac2}$	30kV	5kV	10kV
Primary transformer current $\hat{I}_{ac1} = 2\frac{P_{max}}{\hat{U}_{ac1}}$	2kA	2kA	1kA
Secondary transformer current $\hat{I}_{ac2} = 2\frac{P_{max}}{\hat{U}_{ac2}}$	333A	2kA	1kA
Primary input current $I_{dc1} = \frac{P_{max}}{U_{dc1}}$	1kA	1kA	1kA
Secondary output current $I_{dc2} = \frac{P_{max}}{U_{dc2}}$	166A	166A	166A
Expected primary branch current $\hat{I}_p = \frac{I_{dc1}}{2} + \frac{\hat{I}_{ac1}}{2}$	1.5kA	1.5kA	1kA
Expected secondary branch current $\hat{I}_s = \frac{I_{dc2}}{2} + \frac{\hat{I}_{ac2}}{2}$	250A	1083A	583A



a)

b)

c)

d)

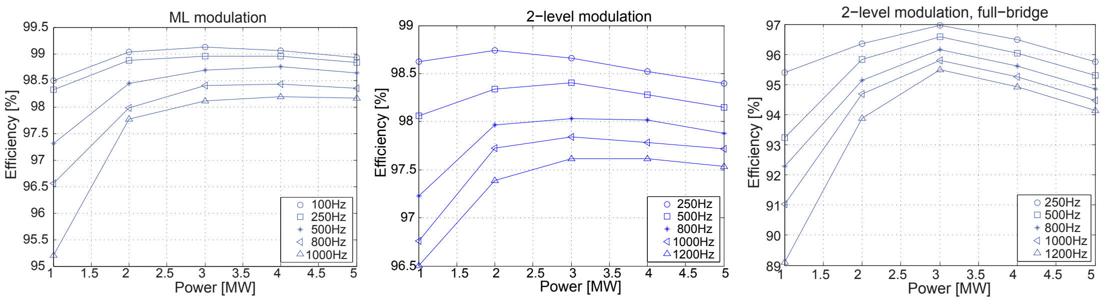
e)

f)

Figure 7.7: Typical waveforms for multilevel modulation at 500Hz a) AC quantities b) DC voltage; typical waveforms for the two-level modulation at 1kHz c) AC quantities d) DC link voltage; typical waveforms for the two-level modulation at 1kHz with full-bridges e) AC quantities f) DC link voltage

are below 97% for switching frequencies above 250Hz.

The selected modulation method has also a strong influence on the installed switching power, which is the product of the current and voltage rating of the semiconductor devices in the converter. The total switching power for the `ML_4_24`-configuration is almost half of the installed switching power of the `2L_4_14`-configuration. Despite the fact that the number of submodules and semiconductors is lower for the `2L_4_14`-configuration in respect to the other configurations, the expected cost for the semiconductor devices is higher.



a) b) c)

Figure 7.8: Efficiency of configurations a) `ML_4_24` b) `2L_4_14` c) `2L_fb6_16`

The energy which is stored in the converter is shown in Fig. 7.9 for the three configurations. Only the energy in the capacitors is taken into account, since the energy stored in the inductances can be neglected. Even if the total number of submodules is higher for the `ML_4_24`-configuration, both the `ML_4_24`-configuration and the `2L_4_14`-configuration have more or less the same energy stored for the different frequencies. Since the voltage elevation is done in the converter, a higher submodule capacitance is required for the `2L_4_14`-configuration, which accounts for the higher energy stored per submodule. This also applies to the `2L_fb6_16`-configuration, where the energy stored in the submodules is even higher for the considered frequency range.

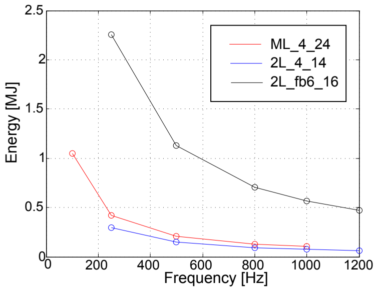
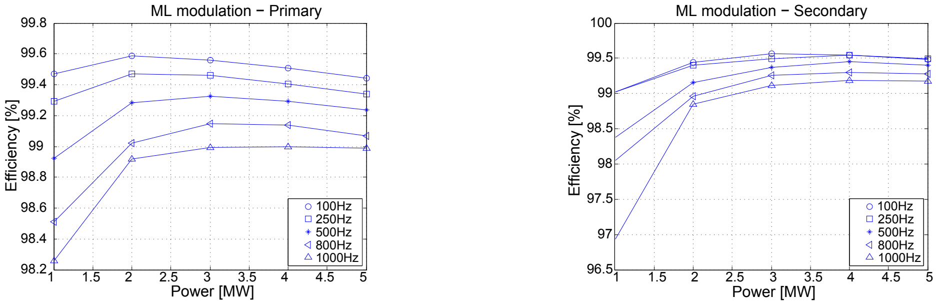


Figure 7.9: Stored energy in the submodule capacitors for the three configurations

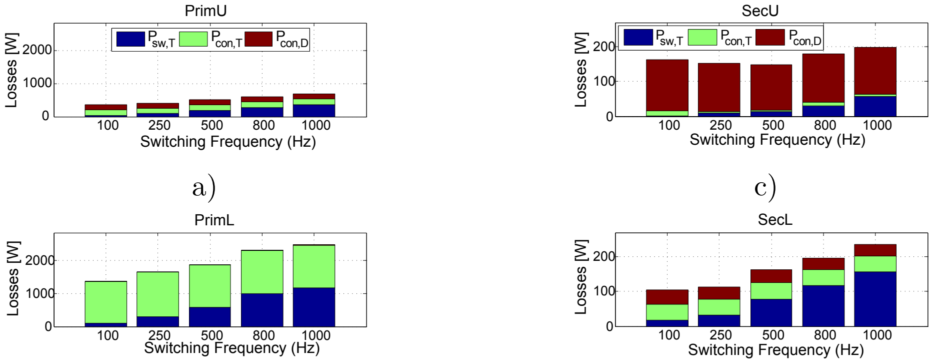
The efficiency of the converter can be divided into the efficiency of the primary and the efficiency of the secondary MMC. Furthermore the loss distribution within the submodules is discussed.

Details on Losses of the `ML_4_24`-Configuration In Fig. 7.10 the efficiencies of the primary and secondary MMC are shown, which are in the same range. Almost for the entire frequency and load range the efficiency is above 99%. Fig. 7.11 gives more details on the loss distribution within a submodule. As it can be expected from the estimated currents in Table 7.4, the losses per submodule are much higher in the primary than in the secondary due to the higher current. In addition, the losses are not distributed equally on the upper and the lower switch within the submodule for the primary MMC. Since the primary converter is in inverter mode, there are almost no conduction losses on the diodes for the lower IGBT of the primary. The secondary MMC is in rectifying mode, therefore the diode of the upper semiconductor is conducting has higher conduction losses in the transistor.



a) b)

Figure 7.10: Efficiencies on the `ML_4_24`-configuration in the a) Primary b) Secondary

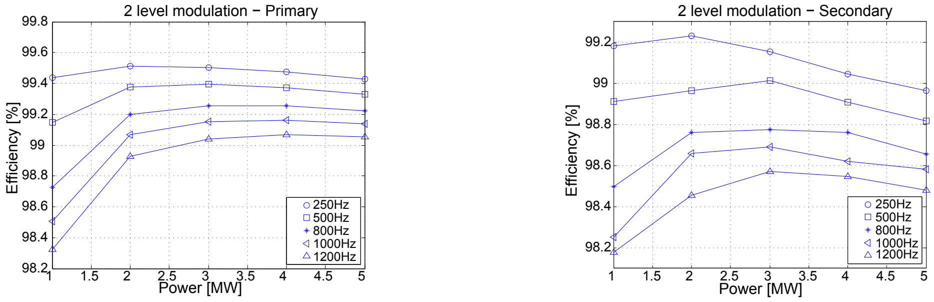


a) c)

b) d)

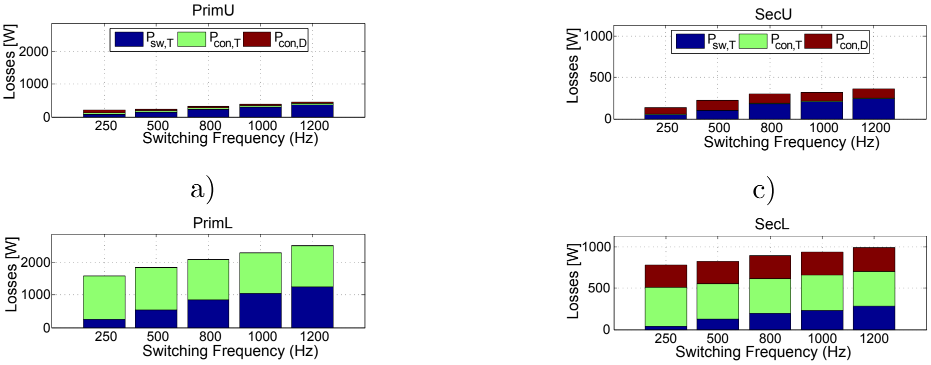
Figure 7.11: Loss distribution in the submodules for the `ML_4_24`-configuration a) Primary: Upper IGBT b) Primary: Lower IGBT c) Secondary: Upper IGBT d) Secondary: Lower IGBT

Details on Losses of the `2L_4_14`-Configuration In Fig. 7.12 the partly efficiencies of the primary are higher than for the secondary, where the voltage elevation takes place. In Fig. 7.13 the losses show a similar distribution as in the `ML_4_24`-configuration. This time the losses are distributed in a even more unequal way between the upper and the lower device of the submodule.



a) b)

Figure 7.12: Efficiencies for the `2L_4_14`-configuration in the a) Primary b) Secondary



a) c)

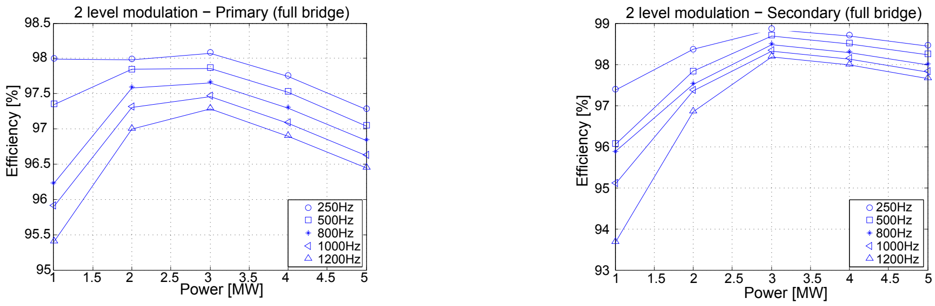
b) d)

Figure 7.13: Loss distribution in the submodules for the `2L_4_14`-configuration a) Primary: Upper IGBT b) Primary: Lower IGBT c) Secondary: Upper IGBT d) Secondary: Lower IGBT

Details on Losses for the `2L_fb6_16`-Configuration The efficiencies for the primary MMC in Fig. 7.14a) are considerably lower than for the secondary MMC and stay below 98%, whereas for the secondary the efficiency is comparable to the one of the `2L_4_14`-configuration. Since there are full-bridge submodules in the primary to achieve the voltage elevation, the losses are more important, in particular because it is the side with the higher current.

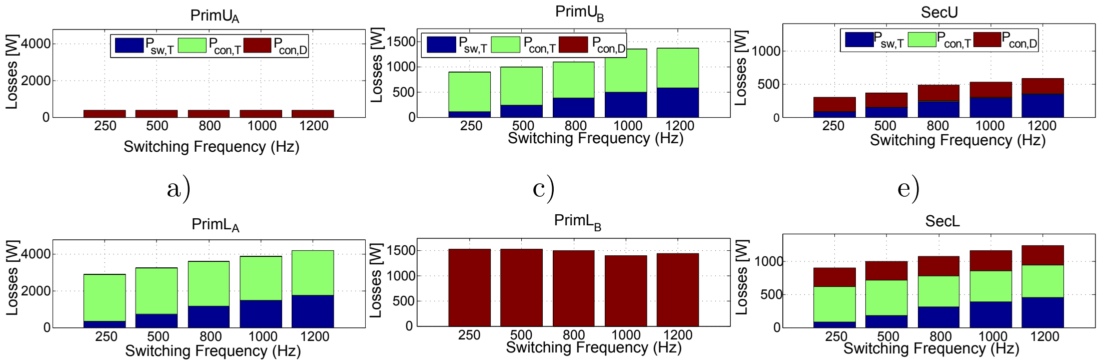
In the submodules of the primary MMC, the losses are not distributed in an balanced manner which is shown in Fig. 7.15a) to Fig. 7.15d).

There are two ways to achieve the submodule state "0" (short-circuit), either using the top two IGBTs or the lower two ones. For this simulation the second option has been implemented, therefore the losses in the lower two IGBTs are considerably higher. In order to obtain a better loss distribution, both ways to achieve the submodule state "0" should be implemented. The losses in the secondary switches in Fig. 7.15e) and 7.15f) are distributed in a similar way as for the `2L_4_14`-configuration.



a) b)

Figure 7.14: Efficiencies for the `2L_fb6_16`-configuration in the a) Primary b) Secondary



a) c) e)

b) d) f)

Figure 7.15: Loss distribution in the submodules for configuration `2L_fb6_16` a) Primary: Upper IGBT A b) Primary: Lower IGBT A c) Primary: Upper IGBT B d) Primary: Lower IGBT B e) Secondary: Upper IGBT f) Secondary: Lower IGBT

Converter Analysis B

Two different configurations are considered in this section, specified in Table 7.5. In comparison to the previous configurations, a higher submodule voltage is tolerated. For the `2L_2_7`-configuration, the elevation is done in the secondary MMC converter. Again the number of switches is almost half in respect to the `ML_6_9`-configuration. For both configurations, the design criteria is $\delta_{max} = 15°$.

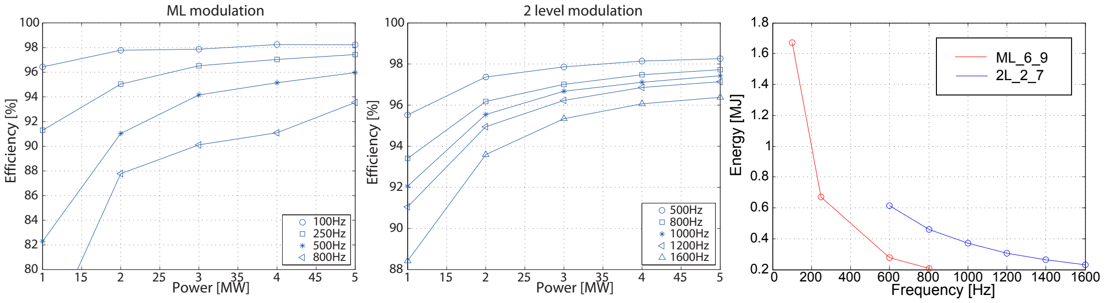
Fig. 7.16a) shows the efficiencies for the `ML_6_9`-configuration and Fig. 7.16b) shows the efficiencies for the `2L_2_7`-configuration for various frequencies. For both modulation methods, it is clearly visible that with decreasing switching frequency, the semiconductor

Table 7.5: Converter configuration B

Denomination	`ML_6_9`	`2L_2_7`
Modulation type	ML Config.	2L Config.
Input voltage	5kV	
Output voltage	30kV	
Nominal power	5MW	
Primary submodule voltage	1kV	2.5kV
Secondary submodule voltage	4kV	2.5kV
N_p	6	2
N_s	9	7
Transformer ratio	1:6	1:1
Primary voltage elevation	1	1
Secondary voltage elevation	1	6
IGBT rating of the primary IGBTs	1.7kV, 2.4kA	3.3kV, 1.5kA
IGBT rating of the secondary IGBTs	6.5kV, 0.4kA	3.3kV, 0.8kA
Number of IGBTs in the primary	48	16
Number of IGBTs in the secondary	72	56
Total number of IGBTs	120	72
Primary switching power [GW]	195.8	79.2
Secondary switching power [GW]	187.2	147.8
Total switching power [GW]	383.0	227.0

losses decrease equally. For equal efficiency, for example 98%, the two-level modulation can operate with a six time higher frequency. In contrast to the configuration studied in section 7.2.2, the `2L_2_7`-configuration is more efficient, even at higher frequencies.

At the level of the energy stored in the converter submodules which is displayed in Fig. 7.16c), for the same frequency less energy has to be stored for the multilevel modulation. Considering the stored energy for equal efficiency on the other hand results in less energy stored for the 2-level modulation.



a) b) c)

Figure 7.16: Efficiencies for various frequencies for the a) `ML_6_9`-configuration b) `2L_2_7`-configuration and c) energy stored for both configurations

7.3 Conclusions

In this chapter, the losses have been determined for a particular case study of a wind farm. Different converter configurations and modulations are compared. Several observations have been made:

- The general tendency of the analysis shows that with higher frequency the switching losses are increasing in respect to the conduction losses.
- The two-level modulation with elevation only in the secondary is advantageous in terms of number of semiconductor devices and submodules. The same tendency has been found in analysis A and B. However, considering the switching energies, the multilevel modulation is more advantageous in the converter configuration A, but not in converter configuration B.
- The energy stored in the submodules for a given frequency is lower for the multilevel modulation, since for the 2-level modulation a more stable voltage and therefore higher capacitance value is needed.
- The two-level modulation with elevation in the primary gives a lower efficiency due to the high current and the high number of semiconductors in the full-bridge submodules.
- A general statement whether to choose the multilevel modulation or the two-level modulation cannot be given, since this decision is not uniquely based on the efficiency of the converter. A converter with a lower number of submodules can be obtained with the two-level operation. However, care has to be taken with the evaluation of the stored power in the converter, since the size of a submodule is mostly depending on the size of the capacitor. Rather than the number of semiconductors, the switching power is better cost indicator.

8 Practical Verification

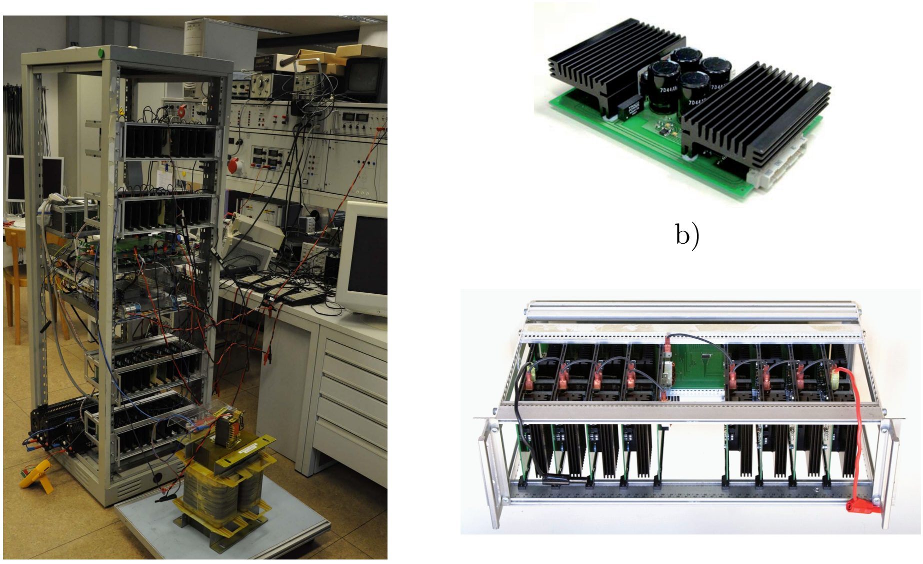
In order to verify the proposed modulation methods, a reduced power prototype has been realised in the laboratory. This chapter describes the prototype and the associated control circuits and shows the experimental results for both the two-level and multilevel operation of the proposed converter structure.

8.1 Prototype Design

The laboratory prototype is illustrated in Fig. 8.1a). Both primary and secondary MMC consist of 4 submodules per branch and each MMC has two phase legs. The submodules are built in a way that both the full bridge and half bridge topology can be realised with the same circuit. A submodule is shown in Fig. 8.1b). The rated current of the submodule is $12A_{rms}$ and the maximum submodule voltage $U_{sm} = 200V$. These submodules have been conceived in the context of a Master Project.

Since the actual prototype is intended for various research projects with a varying number of phase legs, a modular control platform has been conceived for this prototype. The general control structure is depicted in Fig. 8.2. A hierarchical control structure has been adopted, where the Digital Signal Processor (DSP) is the main unit. It handles the communication with two types of Field-Programmable Gate Array (FPGA) cards, the Measurement FPGA and the Control FPGAs. The Measurement FPGA retrieves the external measurements, indicated with a red arrow, such as voltages and currents of the AC stage or the DC input/ output. Up to 12 measurements can be read and handled at the same time. The Control FPGAs control the switches and retrieves internal measurements such as the branch currents and submodule voltages via sequential Serial Peripheral Interface (SPI) measurements. One Control FPGA handles an entire phase leg with 8 submodules and the associated internal measurements.

The details on the functionality are shown in Fig. 8.3. The three main actors of the control are:



b)

a)

c)

Figure 8.1: a) Laboratory prototype b) Submodule c) A phase leg

DSP - TI TMS320C28346 The main state machine which defines the converter behaviour (charging, discharging, steady state, failures) is implemented in the DSP. As it will be explained later, a fast security is also foreseen on a lower level in the FPGAs. The DSP communicates the modulation indexes to the Control FPGAs and checks if the converter experiences any over-voltages on the submodules or over-currents in the branch inductances. The external measurement are retrieved from the Measurement FPGA. All the FPGAs are connected to the same 16bit data and 16bit address bus for the communication.

Control FPGA - Actel (M1)A3P10001 Flash FPGA The Control FPGA is the key element of the control structure and assures at the same time the application of the references given by the DSP, the balancing of the submodule voltages and a fast protection against over-currents. It contains the Modulator, which determines the switching instants of the submodules based on the modulation index given by the DSP. The submodule voltages and branch currents are measured sequentially via a SPI channel. A ranking of the submodule voltages is established in the Sorting block. Knowing the direction of the branch current in addition to the charging states of the submodules, the Selector block decides which submodule has to be connected or disconnected. The IGBT mask is passed to the Dead Time block, which ensures the required delays regarding switch-on and switch-off of the IGBTs.

A fast analogue over-current detection is able to block the FPGA output and the output of the other FPGAs via the communication line "master-stop".

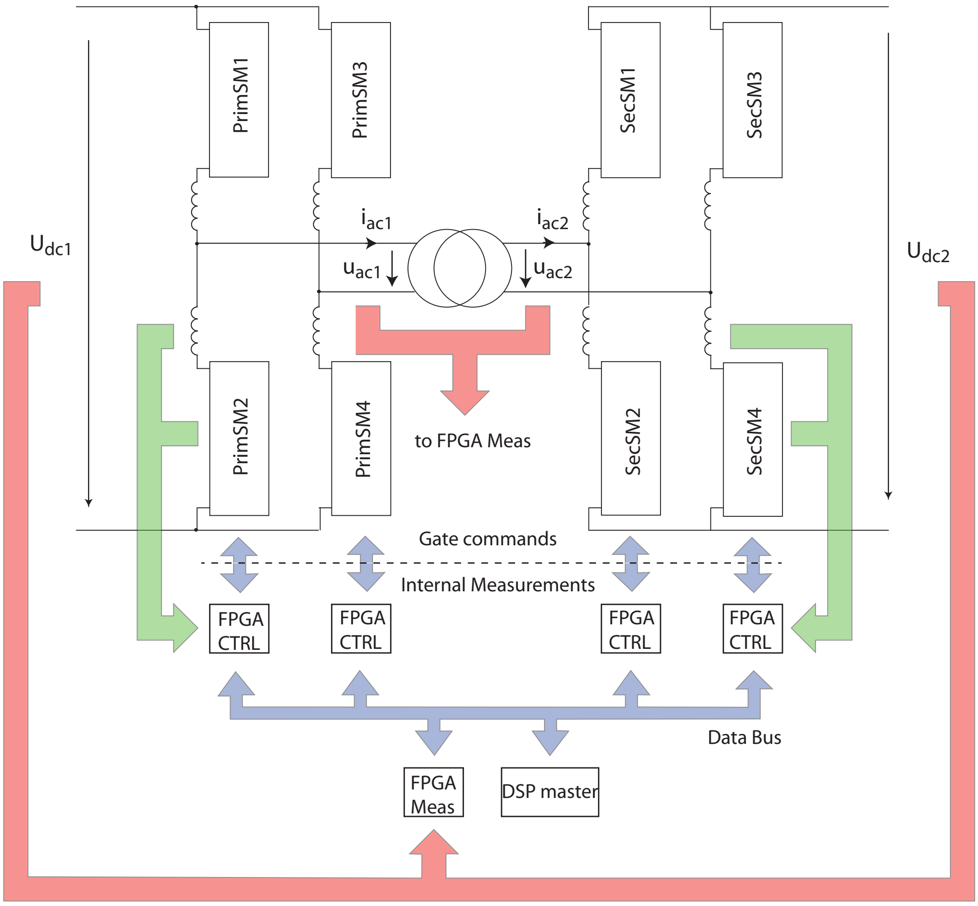

PrimSM1
PrimSM3
SecSM1
SecSM3
U_{dc1}
i_{ac1}
i_{ac2}
u_{ac1}
u_{ac2}
U_{dc2}
PrimSM2
PrimSM4
to FPGA Meas
SecSM2
SecSM4
Gate commands
Internal Measurements
FPGA CTRL
FPGA CTRL
FPGA CTRL
FPGA CTRL
Data Bus
FPGA Meas
DSP master

Figure 8.2: Data-flow between control and converter

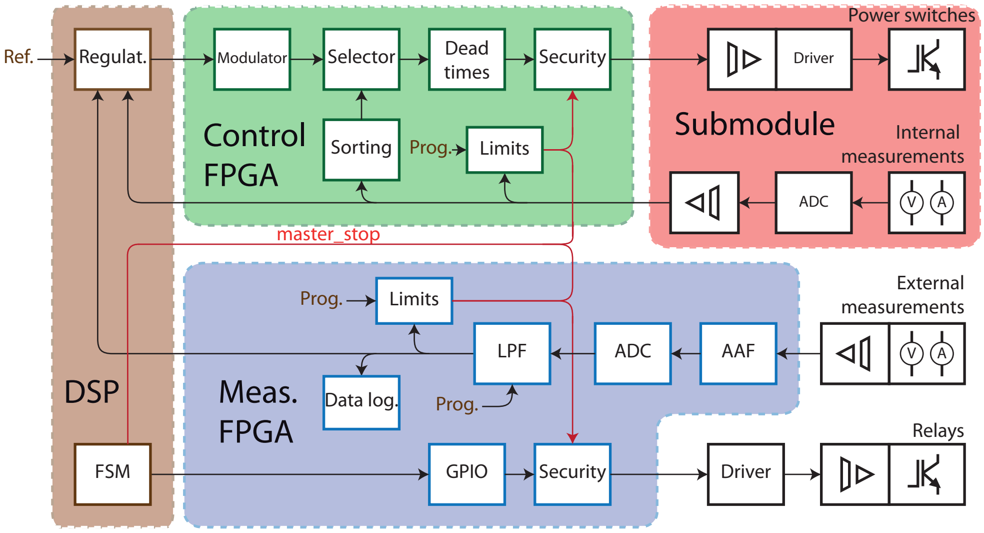

Ref.
Regulat.
Modulator
Selector
Dead times
Security
Power switches
Driver
Control FPGA
Sorting
Prog.
Limits
Submodule
Internal measurements
ADC
V
A
master_stop
External measurements
Prog.
Limits
LPF
ADC
AAF
V
A
DSP
Meas. FPGA
Data log.
Prog.
FSM
GPIO
Security
Driver
Relays

Figure 8.3: Command strategy of the converter

Measurement FPGA - Actel (M1)A3P10001 Flash FPGA All the external measurements are retrieved by the Measurement FPGA. Up to 12 measurements can be treated simultaneously. The data passes first through an Anti-Aliasing filter (AAF). The Analogue-to-Digital Converter (ADC) transforms the analogue measurements to digital data at 100k samples/s, which are low-pass filtered (LPF). The filtered data can now be read by the DSP for control purposes. Internally an over-current and over-voltage check is performed in the Measurement FPGA (Limits block). There is a possibility to save data on the PCB in a Synchronous Dynamic Random-Access Memory (SDRAM) of 256 MB, which can be accessed by the computer.

In addition, the Measurement card handles the control of the relays, used for connecting the converter to the grid or for connecting/disconnecting the charging resistor.

Additional Cards In addition to the control box, several additional cards had to be designed:

- LEM card: Measures up to 7 voltages and 7 currents using LEM LV25-P voltage transducers and LEM LA 55-P current transducers. However only 12 measurements are transmitted to the Measurement FPGA.
- Relay card: Interfaces the relays with the FPGA (Driver)
- Current measurement card: Measures the upper and lower branch currents and communicates the values to the Control FPGA via SPI. An additional analogue security detects over-currents instantly. A separate communication line assures that this information is immediately treated by the Control FPGA, which then takes the necessary measures.

8.2 Transformer

The medium frequency transformer has been built by SEKY International SA and used in the context of a Master Project [80]. The transformer parameters have been measured and are given in Table 8.1. It is a core type transformer.

Table 8.1: Transformer parameters

Frequency	2kHz
Transformer ratio	1:1
Nominal current	20A
Nominal voltage	400V
Leakage inductance L_σ	0.267mH
Transformer winding resistance	0.29Ω
Main transformer inductance L_h	41.9mH
Total weight	76kg

8.3 Multilevel Modulation - Experimental Results

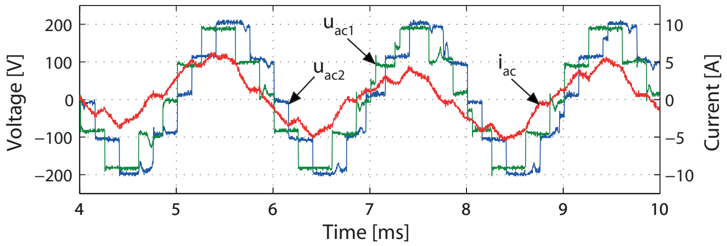
For the multi-level modulation two different test cases are shown, firstly a steady state condition and then a transitory regime produced by a load step. The parameters for the test case are given in Table 8.2.

Table 8.2: Prototype parameters for the ML-modulation

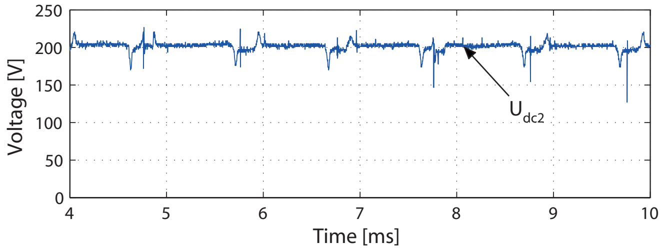
Input voltage U_{dc1}	200V/250V
Output voltage U_{dc2}	200V/250V
Rated Power	1kW
AC frequency	500Hz
Branch inductance L_s, L_p	1mH
Number of submodules in the primary	4
Number of submodules in the secondary	4

Fig. 8.4 describes the steady state results for an output power of 450W at 200Vdc input and output voltage. In Fig. 8.4a), the voltages u_{ac1} and u_{ac2} at the level of the transformer are shown. The implemented N+1 modulation, gives place to a 5 level voltage waveform. The actual frequency of the AC tank is 500Hz which is also the average switching frequency of the different IGBTs. The current i_{ac} is filtered by the leakage inductance of the transformer and the branch inductances of the converter. In Fig. 8.4b) the DC output voltage U_{dc2} is regulated at 200Vdc. The ripple in the DC voltage are on the one hand due to the slightly desynchronised switching of the upper and lower branch (narrow spikes) and on the other hand due to the energy variation of the branches (large oscillation).

Fig. 8.5 shows transient results for a load step produced at a time instant t=0.05s. The power demand has increased from an output power of 337W to 640W visible on the step



a)



b)

Figure 8.4: Experimental results for steady state operation a) AC quantities b) Secondary DC voltage

of the output current I_{dc2}. The DC voltage U_{dc2}, regulated at 250Vdc is hardly affected thanks to the feed-forward control.

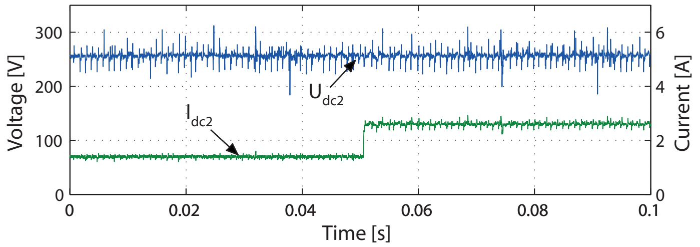


Figure 8.5: Experimental results for a load step at t=0.05s

8.4 Two-Level Modulation - Experimental Results

The parameters for the experimental test of the two-level modulation are given in Table 8.3. The elevation is only performed in the secondary MMC ($k_p = 1$). At time instant t=0.02s a load step is performed from 0W to 200W, visible in Fig. 8.6. Since the phase shift is adapted in two steps, there is no DC component in the transformer current i_{ac}. The current i_{ac} shows the dynamics of an RL-circuit, decreasing asymptotically. The relatively high branch resistance has a negative influence on the gradient and therefore the current decreases quickly.

Table 8.3: Prototype parameters for two-level modulation

Input voltage U_{dc1}	75V
Output voltage U_{dc2}	$k_p k_s U_{dc1} = 225V$
Elevation factor	$k_p = 1,\ k_s = 3$
Rated power	1kW
AC frequency	1kHz
Leakage inductance L_σ	0.267mH
Number of submodules in the primary	4
Number of submodules in the secondary	4

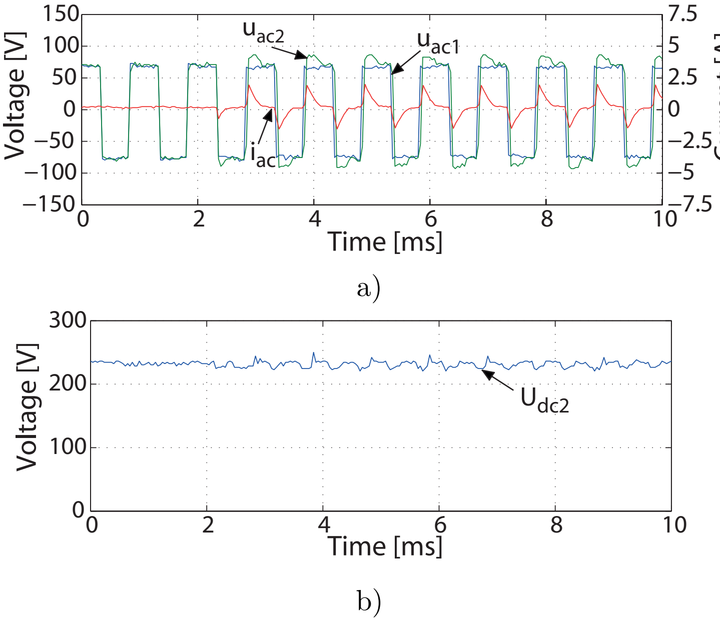
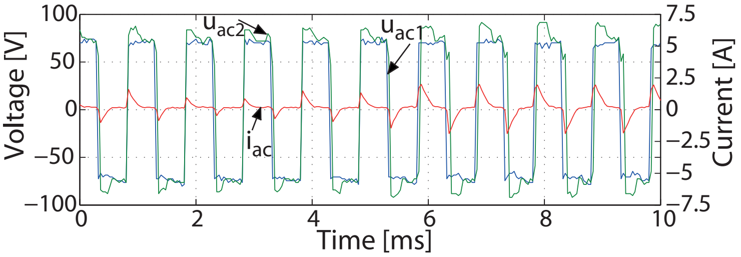
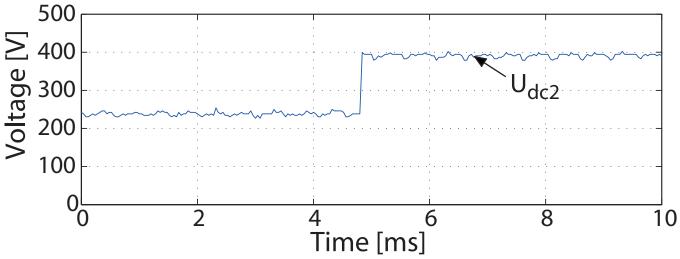


Figure 8.6: Experimental results during a load step a) AC quantities b) Secondary DC voltage

In a second example a step change in the elevation factor from $k_s = 3$ to $k_s = 5$ is produced at time instant t=4.8ms, visible in Fig. 8.7. The controller adapts to the new set-point and regulates the output voltage at $U_{dc2} = k_p k_s U_{dc1} = 375V$. The higher output voltage results in an increased power flow, since the same resistive load is connected. In response to the load step, the transformer current increases.



a)



b)

Figure 8.7: Experimental results during a step change in k_s a) AC quantities b) Secondary DC voltage

9 Conclusions and Future Work

9.1 Summary and Contributions

When classical voltage transformation devices reach their optimal design and the limits of their capacity, new technologies are expected to influence the general concept of power exchange between power generators and users. The well-established AC transmission and distribution network will face several challenges. These include the need for greater use of renewable energies, power quality assurance and reduced use of raw material. Additional problems that will have to be resolved are the need for greater power transport efficiency and reduced space for electrical lines.

New technologies will be needed to address these challenges and to influence the general concept of power exchange between power generators and users. The shift from the traditional AC system to a DC system depends much on the voltage elevation/reduction device. The conventional low-frequency electromagnetic transformer would have to be replaced by an efficient converter topology, which adapts the voltage levels.
The state of the art DC/DC converters listed in the first part of this thesis (Chapter 3) do not provide enough security to be used extensively in a DC grid. Furthermore, the additional protection that the devices require is either costly or not available for any power level.

The modular DC/DC converter topology presented in the second part of this work, overcomes this limitation in terms of protection. The analysis and the control of this isolated DC/DC structure are the main contributions of this thesis. The presented topology can be understood as a power electronic transformer, which adapts the DC voltage levels between LVDC and MVDC or MVDC and HVDC networks. Techniques achieving high voltage elevation ratios were analysed and an innovative solution, the two-level modulation, was presented in section 6.2. In comparison with the conventional multilevel modulation technique presented in section 6.1, the two-level modulation utilised fewer semiconductors for a given application. This was shown in chapter 7 for a concrete case. A general conclusion about the efficiency of the modulation method cannot be drawn because it depends on the converter configuration. Depending on the nominal submodule voltage, different switches have to be chosen, and this influences the loss calculation. For each case, both modulation methods should be assessed. However, with both approaches, efficiencies higher than 98% can be achieved (considering the semiconductor losses and the losses in the transformer).

It can be concluded that with the performance of the Modular DC/DC converter, DC systems may be competitive in comparison with an AC based system. The inferior efficiency of the converter is compensated for by the higher efficiency in transport. Furthermore the protection is handled at the level of the converter, which makes it possible to react quickly to faults.

9.2 Future Work

This thesis focused on the development of the key component of a DC distribution and collection system, the power electronic transformer. Many aspects of the proposed solution can be dealt with in more detail, such as the design of the transformer, an issue that was only lightly touched upon.

Further work includes optimising the proposed structure. A procedure has to be formulated that defines the number of submodules, the voltage levels, the transformer ratio and the modulation method for a given application. The optimisation criteria can be based on weight, volume or cost. Work in this direction has already been done [139], where optimal solutions for given criteria were found for an interleaved DC/DC converter using the Pareto front.

The reliability of a distribution system plays an important role and has not been addressed so far. Applying the Failure Mode and Effects Analysis (FMEA) to the converter, together with redundancy, can be part of another research topic.

The shift from an AC-based system to a DC-based system depends not only on the technology of the power electronic transformer. A stability analysis of a DC grid supported by the modular DC/DC converter is required. The control on the level of the system needs to be defined as well as the global fault behaviour.

A Appendix

A.1 Details on the Branch Energy Balancing

A.1.1 Determination of the Current Coefficient due to an Unbalance of the Branch Energies

The circuit which models the unbalance of the branch voltages is shown in Fig. A.1. Since the two voltage sources are only DC, the current that circulates in the circuit is DC as well. The load has been represented as an slightly ohmic-inductive impedance, however if a DC current is flowing through the impedance only the resistive part is of interest. The value of the resistor can be found by considering the power coming from the DC side is the same as the power consumed on the AC side in steady state conditions:

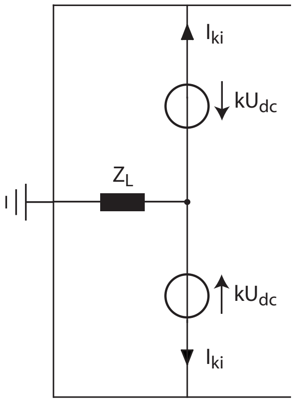


Figure A.1: DC current created by an unbalance of the branch energies

$$P = U_{dc}I_{dc} = \frac{\hat{U}_{ac}\hat{I}_{ac}}{2}\cos\phi \Rightarrow R = \frac{\hat{U}_{ac}^2\cos\phi}{2P} \tag{A.1}$$

The additional DC current I_{ki} in the branch can therefore be calculated and simplified using the relation $m = \frac{2\hat{U}_ac}{U_{dc}}$.

$$I_{ki} = \frac{kU_{dc}}{R} = \frac{8kP}{m^2 \cos\phi U_{dc}} \tag{A.2}$$

Finally the coefficient k_i can be defined by the ratio of the additional DC branch current I_{ki} and the input DC current I_{dc}:

$$k_i = \frac{I_{ki}}{I_{dc}} = \frac{8k}{m^2 \cos\phi} \tag{A.3}$$

A.1.2 Relating AC and DC Quantities

From the analysis of the power flow, the incoming power must be equal to the outgoing power. If no unbalance of the upper and lower branch energies is given, the DC power from the source U_{dc} equals the AC power consumed by the load. If an unbalance takes place, the AC load is biased by a DC component which in turn has to be paid attention to. To the consumed power on the AC side a term regarding the power dissipation due to the unbalance is introduced.

$$P = U_{dc}I_{dc} = \frac{\hat{U}_{ac}\hat{I}_{ac}}{2}\cos\phi + 2I_{ki}kU_{dc} \tag{A.4}$$

By using equation A.2, it is possible to reformulate the power balance

$$P = \frac{\hat{U}_{ac}\hat{I}_{ac}}{2}\cos\phi + 2\frac{8kP}{m^2\cos\phi U_{dc}}kU_{dc} \tag{A.5}$$

Finally with the help of the relation $n = \frac{\hat{I}_ac}{2I_{dc}}$, a relation between m and n can be found:

$$\frac{2}{m\cos\phi}\left(1 - \frac{8k^2}{m^2\cos\phi}\right) = n \tag{A.6}$$

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Curriculum vitae

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Education

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2002–2007 **Master**, *Ecole Polytéchnique Fédérale de Lausanne*, CH.
Electrical Engineering, Speciality in Electrical Energy.

1997–2002 **Matura**, *Kollegium Spiritus Sanctus Brig*, CH.
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Work experience

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Publications

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