# A Sub-$V_T$ 2T Gain-Cell Memory for Biomedical Applications

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## I. Introduction

All state-of-the-art subthreshold (sub-$V_T$) memories are based on static bitcells, while the feasibility and limitations of dynamic bitcells operated in the sub-$V_T$ regime have not been studied yet. For the first time ever, we examine the sub-$V_T$ operation of gain-cells and present a fully functional memory array with data retention times that are $10^4$X higher than access times. The dynamic sub-$V_T$ memory is designed for a mature 0.18µm CMOS node which is typically used to 1) easily fulfill the high reliability requirements of biomedical sensor nodes and implants; 2) reach the highest energy-efficiency of such biomedical systems typically requiring low frequencies and duty cycles [1]; and 3) achieve low manufacturing cost.

## II. 2T Gain-Cell Design and Array Architecture

To counteract the heavily degraded on-to-off current ratios at low supply voltages ($V_{DD}$), the write-access transistor of the considered 2-transistor (2T) gain-cell is implemented with a high-$V_T$ PMOS I/O transistor, exhibiting substantially reduced subthreshold conduction compared to a standard core transistor, in order to achieve data retention times which are at least $10^4$X longer than memory access times. As the bitcell's silicon area is dominated by contacts, the area overhead due to the use of an I/O transistor is small. A standard-$V_T$ NMOS core transistor is used as read transistor providing fast read access times in the order of µs for the sub-$V_T$ domain.

The presented 2 kb two-port word-access memory macro consists of 64 rows and 32 columns. To achieve write-access times of several µs with the I/O devices, an under-drive voltage of -650 mV is applied to the selected write word-line (WWL). Other than the WWL drivers, the entire memory macro is clearly operated in the sub-$V_T$ regime.

## I. Retention Time, Access Time, and Read Margin

The proposed gain-cell memory was evaluated for a sub-$V_T$ $V_{DD}$ of 400 mV at a temperature of 37°C, typically found in biomedical implants. In the considered technology, core and I/O transistors have an average threshold voltage of 500 and 750 mV, respectively. All presented metrics correspond to the worst sample out of 1k Monte Carlo runs accounting for global and local parametric variations.

We simulated retention time according to the worst-case decay of the data levels, assuming that the voltage on the write bit-line (WBL) is always opposite to the voltage on the storage node (SN). The resulting plots, given in Fig. 1, show a retention time of 40 ms, with better protection for the logic 1 level as compared to the logic 0 level. This corresponds to the previously reported behavior in the above-$V_T$ domain [2, 3].

Fig. 2 shows that the proposed gain-cell array retains high read-margins, even with weak data levels that can occur shortly before a refresh operation. Indeed, the distributions of the read bit-line (RBL) voltage when reading a 0 and a 1 are clearly separated and a low-area sense buffer was designed to switch within the corresponding average distribution.

With a read and write time of 2 and 3 µs, respectively, a complete refresh operation takes less than 500µs, meaning that the array is available for W/R operation during more than 98% of the time.

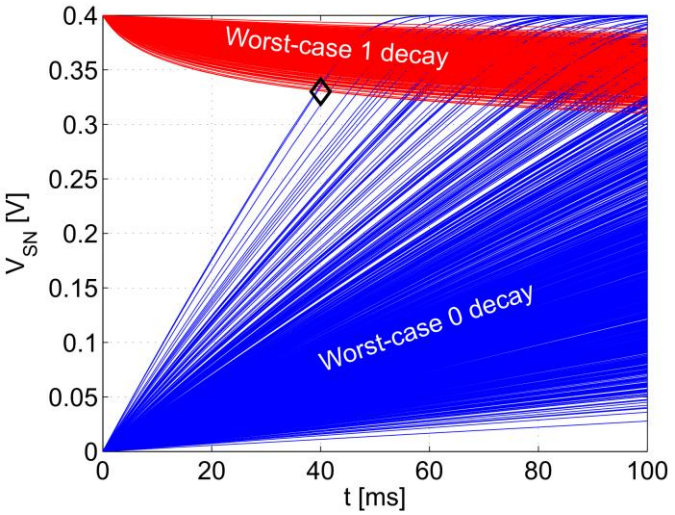


Fig. 1. Worst-case decay of data levels.

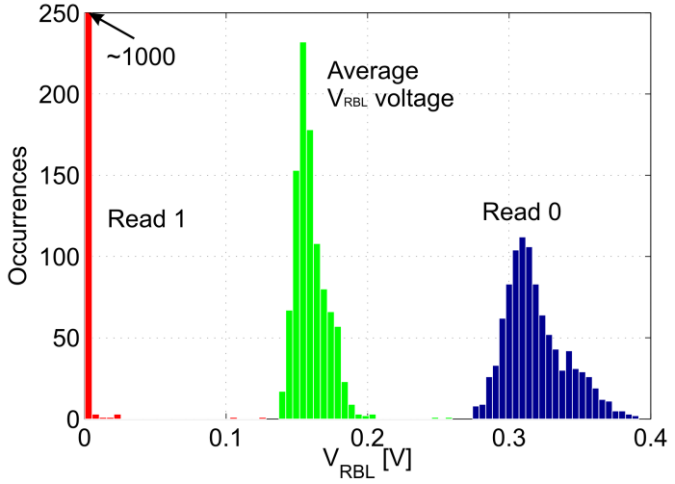


Fig. 2. Distribution of read bit-line (RBL) voltage.

## II. References

[1] M. Seok *et al.*, ISLPED 2008

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[3] K. C. Chun *et al.*, JSSC 2011