Design and Testing Strategies for Modular 3-D-Multiprocessor Systems Using Die-Level Through Silicon Via Technology

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***Abstract*—An innovative modular 3-D stacked multi-processor architecture is presented. The platform is composed of completely identical stacked dies connected together by through-silicon-vias (TSVs). Each die features four 32-bit embedded processors and associated memory modules, interconnected by a 3-D network-on-chip (NoC), which can route packets in the vertical direction. Superimposing identical planar dies minimizes design effort and manufacturing costs, ensuring at the same time high flexibility and reconfigurability. A single die can be used either as a fully testable standalone chip multi-processor (CMP), or integrated in a 3-D stack, increasing the overall core count and consequently the system performance. To demonstrate the feasibility of this architecture, fully functional samples have been fabricated using a conventional UMC 90 nm complementary metal–oxide–semiconductor process and stacked using an in-house, via-last Cu-TSV process. Initial results show that the proposed 3-D-CMP is capable of operating at a target frequency of 400 MHz, supporting a vertical data bandwidth of 3.2 Gb/s.**

***Index Terms*—Multi-core processor architecture, three-dimensional (3-D) integration, through-silicon via (TSV).**

I. Introduction

AS CONVENTIONAL 2-D scaling of device dimensions is increasingly becoming more complicated, three-dimensional integrated circuits (3-D-ICs) are emerging as a promising solution to extend the validity of Moore's Law and to improve performance [1].

In a conventional integrated circuit, hundreds of millions of transistors can be placed on a single chip to increase performance and computing power, but the realization of large dies reduces manufacturing yield. Moreover, long on-chip interconnects increase communication latency due to the impossibility to scale global wire length along with technology [2]. Power consumption is also increased by the higher number of signal repeaters along the lines.

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These scaling challenges can be overcome with a 3-D approach, where multiple dies are stacked on top of each other and interconnected by through-silicon vias (TSVs). In fact, with respect to planar mainstream technologies, 3-D-ICs provide potential performance advances, reducing interconnection delay and ensuring high bandwidth. Moreover, a form factor reduction is achieved thanks to the small chip footprint and the high integration density [3], [4]. 3-D benefits can fit the requirements of the embedded processor market, where emerging parallelization techniques have highlighted the potential of multi core engines [5]. 3-D stacked chip multi-processors (3-D-CMPs) are expected to increase the overall core count, while improving core-to-core communication [6]. With the advent of parallel computing, with its potential [7] and limits [8], the focus is moving rapidly towards the multi-core era [9], [10]. Parallel computing is also the most potent alternative to traditional frequency scaling techniques used extensively throughout the past decades. Concerning the embedded market, recent commercial processor implementations (TILE64 [11]) as well as emerging parallelization techniques for embedded applications highlight the potential for very large number of cores on embedded processors. Latest embedded application implementations [5] demonstrate a very high degree of achievable parallelization thus provide near-optimal "linear" speedup as specified by Amdahl's Law [8]. Furthermore, additional effort is exerted to reduce the inherent level of complexity involving the parallelization of applications, improve the standardization of the flow and reduce the immense fallibility of the parallelization process [12].

Nevertheless, numerous challenges could prevent 3-D-ICs from becoming commercially attractive. In fact, additional effort is required to identify an optimal design partitioning among layers. Moreover, technological processes necessary for creating interconnection among superimposed layers cannot yet be regarded as mature.

This paper presents an innovative and modular multi-processor platform composed of completely identical stacked chips. Each die contains a 3-D connection macro for intra-layer communication, formed by a TSV matrix plus additional circuitry. Each tier features multiple processors, integrated with a 3-D-folded network-on-chip (NoC), enabling data transfer among the processing elements both on the same and on different layers.

The main contribution of this paper relies on the capability of stacking an arbitrary number of layers with a single chip design,

thereby creating a modular 3-D-CMP. The cost-effectiveness is mainly due to the possibility to reduce nonrecurring engineering (NRE) costs, creating a portfolio of architectures with the same mask set. For instance, the standalone die (2-D-CMP) can be directly used as a final product or integrated on top of identical chips with no additional design effort, thereby creating a high performance version of the same device. This homogeneous approach enables to overcome the unique challenges of the prebonding testability of 3-D systems without additional effort and constraints.

The remainder of this paper is organized as follows. Related work on 3-D integration is analyzed in Section II, with a particular attention to the alternative solutions for 3-D-CMPs. Section III demonstrates the architecture features exploiting the proposed homogeneous 3-D design approach. The TSV fabrication process developed in-house is briefly described in Section IV. Section V is focused on the circuit design, detailing 3-D specific macros and modules. Additional architectural features ensuring a pre- and post-bonding testability are presented in Section VI. The experimental results obtained from simulations and measurements on fabricated samples are shown in Section VII and, finally, Section VIII summarizes the more relevant conclusions of this work.

II. Related Work

A significant amount of recent work has been focused on exploring the potential benefits of 3-D stacked processor architectures.

In 2006, Black *et al.* [13] have proposed to arrange the logic modules of an Intel Pentium 4 microprocessor in clusters and reorganized them in two stacked layers, resulting in 15% performance gain and 15% power savings at constant frequency. In the same study, a memory-on-logic solution is also presented, using as a simulation vehicle an Intel Core 2 Duo unit. The implemented architecture aims to increase the cache capacity by stacking a memory layer on top of the dual-core die, highlighting the reduction of both latency and access memory time.

Many other examples of 3-D processors, involving a heterogeneous partitioning, have been presented. An early approach [14] was based on the superimposition of layers containing both cores and cache banks, interconnected by a network-in-memory. A placement algorithm was used for placing the processing units with a 3-D offset to avoid thermal problems.

One of the first solutions implementing multiple memory layers on top of processors was presented by Kgil [15], modeling a web server as a CMP built of four DRAM layers stacked on top of a processing die hosting up to eight parallel cores.

Other CMPs have been designed in later years exploiting multiple 3-D-DRAM layers [16], [17]; these solutions showed the possibility to reorganize modules and interconnections in order to have a significant bandwidth increase, resulting in a relevant speedup in the routine execution. Loh's [18] solution demonstrated an achievable speed-up of 280% with respect to the baseline CMP (an Intel QuadCore) connected to off-chip DRAM. These results are mainly based on architectural simulators, assuming a completely mature and reliable technological process for 3-D integration is available.

Although a number of experimental processes have been proposed for TSV fabrication to construct multiple stacked layers [6], [19], just few industrial examples of memory chips on top of a processor have been demonstrated so far, such as the 3-D-processor system by Tezzaron [20], integrating an Intel 8051-based processing layer with an SRAM layer.

Despite significant latency and bandwidth improvements that are expected [21], the heterogeneous approach requires additional design effort and costs for the realization of different layers to be stacked in the 3-D system. Moreover, in previous proposals, it is extremely challenging to test all the layers before the bonding process, causing a noticeable decrease of the final yield. Recently, a solution is represented by the 3-D-CMP proposed by Healy *et al.* [22], where dummy pads on nonaccessible layers are employed for the prebonding verification and then buried inside the stacked structure [23].

A processor architecture where a baseline micro-architecture can be augmented by vertically stacking additional blocks (e.g., more caches, reservation station, and so on) to target different market segments has been proposed by Loh in [24]. The novelty of this work relies on the capability of stacking multiple samples of the same design realizing a fully modular, testable and highly reusable 3-D-CMP platform with a fairly limited design effort and reduced mask costs.

III. 3-D Modular Multi-Core Architecture Features

The novel and unique architecture has been specifically designed for stacking identical dies in order to form the 3-D system. Fig. 1 presents a basic block diagram of the stacked structure, with a two-layer configuration for the sake of simplicity. Without loss of generality, the proposed architecture can be expanded to include multiple identical layers that can communicate with each other (Fig. 2). Each die can be considered as a planar multi-core architecture, composed by multiple processing elements (PEs), working in parallel. The cores exchange data through a shared memory implemented in the peripheral subsystem (PS) unit; the access of PE to the shared memory is arbitrated by a system of semaphores to avoid contention. The interaction between cores occurs through a specific source-routed NoC, composed of a 36-bit switch, in charge of the effective signals routing to and from six directions (north, south, east, west, up, down), and a network-interface (NI) for each logic block present on the layer. The network system has a 3-D folded architecture in order to enable the management of the signals in both the horizontal and vertical directions.

The intra-layer communication is achieved through the introduction of a 3-D connection macro, exploiting arrays of TSVs as vertical data bus. Additional circuitry is introduced in the macro: a serializer-deserializer module optimizes the trade-off between bandwidth and number of TSVs in the array; a Dual-Clock FIFO enables the data synchronization at the interface of the 3-D structure. In fact, each stacked layer has an independent clock domain, provided with a PLL module to regenerate the transmitted clock signal.

A. Homogeneous and Modular Approach

The homogeneous 3-D integration, obtained by stacking completely identical dies, results in a cost-effective final struc-

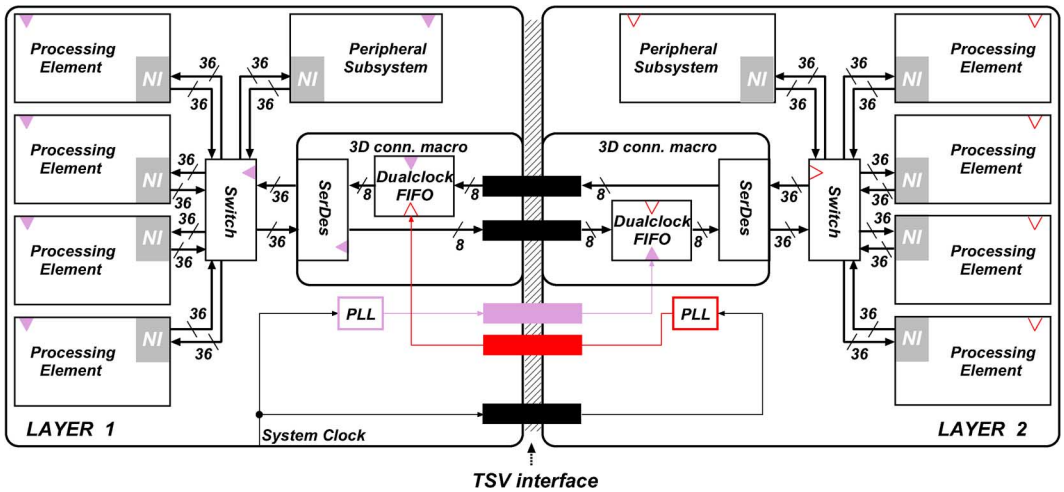

Fig. 1. Proposed architecture for the 3-D-CMP in a two-layer configuration: Four identical PE and a PS are placed in each layer. A 3-D connection macro with TSVs is responsible of inter-layer communication. Only main building blocks and relevant TSVs are shown in the diagram.

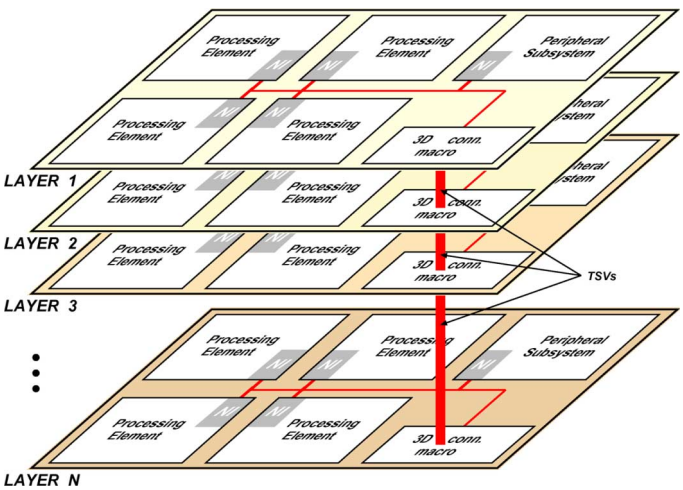

Fig. 2. Generic 3-D connection macro block on each identical layer allows the inter-layer communication among multiple layers, with serial multiplexed TSV arrays.

ture. In fact, the development of a single layer guarantees a reduction in design time and fabrication costs, involving only one set of lithographic masks [6]. A traditional 2-D-IC design flow is employed to design both the multi-processor units and the 3-D connection macro. At this point, it is important to note that each layer is a stand-alone MPSoC IC and can function as a fully testable and operational 2-D-CMP, as shown in Fig. 3(a).

Once the target 3-D structure is decided, known-good-dies (KGDs) are postprocessed. The dies are stacked on top of each other and the Via-last TSVs are fabricated for inter-layer communication, leading to a homogeneous 3-D-CMP structure of identical layers, as shown in Fig. 3(b). With this approach, the overall number of cores in the system is increased, speeding up the parallel workload of the processors and improving the CMP performance. Nevertheless, the proposed design strategy is not limited to homogeneous systems. Different dies can also be integrated in the stacked platform, as long as they share the 3-D connection macro. Fig. 3(c) depicts a possible configuration where a memory layer is placed on top of two CMP dies.

The proposed design approach leads to a reusable platform with high cost-effectiveness: it can target various market segments simply by selecting the appropriate number of layers to be stacked in the system. An important contribution of this work lies in the possibility to configure the stacked dies number after the fabrication: a unique identification signal (LayerID) is provided to each die in order to distinguish identical layers. The LayerID is automatically assigned at the system power-up, after all chips are fully processed and assembled.

However, this postfabrication configurability of the number of layers eventually leads to the need of over-constraining the power I/Os. Before the design phase, a maximum number of layers that can possibly be stacked should be defined in the specs. The designer should then over-constrain in order to guarantee the correct functionality in the case of a system with the maximum number of layers, to avoid PEs starving for power.

The proposed architecture design and the homogeneous stacking solution, as the one depicted in Fig. 3(b), offer the advantage of increasing the overall yield of the assembled structure. Even though the manufacturing yield of small footprint chips can be high, one faulty die can completely ruin the behavior of the entire 3-D system. Identical die integration allows each standalone chip to be fully testable, leading to a higher assembly yield for the final 3-D-CMP structure that is by definition built out of KGDs [25].

The proposed design strategy may introduce challenges concerning the heat dissipation once multiple dies are stacked. As illustrated in the analysis of a 3-D die-stacked microprocessor implementation by Puttaswamy *et al.* [26], stacking identical multi-processor dies may obstruct heat transfer to the heat-sink resulting in a noticeable, yet limited, overall temperature increase of the system. In the extreme case of being unable to provide adequate heat dissipation for a 3-D die-stacked implementation, a number of solutions have been proposed. As an example, Zhou *et al.* [27] proposed an OS-assisted scheduling algorithm performing thermal-aware task migration. The solution ensures the minimization of thermal gradient across the system as well as temperature peaks, with balanced assignments of the workloads to vertically adjacent cores.

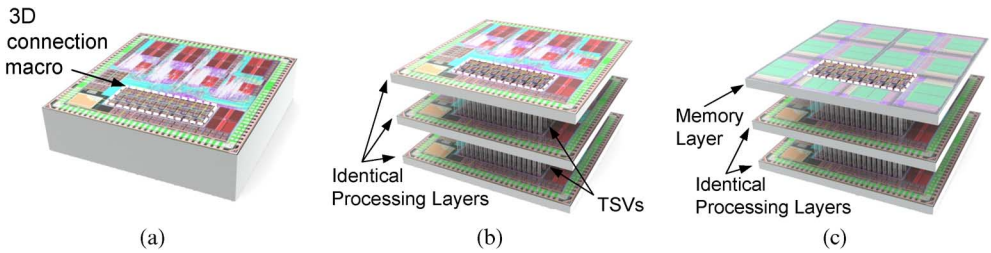

Fig. 3. Modular reusability of the proposed layer architecture. (a) Single die used as standalone 2-D-CMP. (b) Homogeneous stacking for high performance 3-D-CMP. (c) Heterogeneous stacking for 3-D-CMP, integrating additional layers (e.g., a memory die) that shares the same 3-D connection macro.

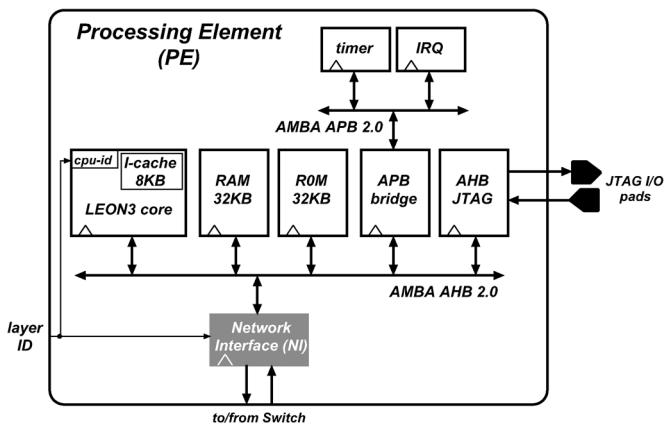

Fig. 4. PE internal architecture, with the LEON3 core and its private modules. Each unit is accessible through JTAG ports for debugging purposes. The NI routes packets from PE to the shared memories in the PSs.

B. Processing Element, Peripherals Subsystem, and Network-on-Chip

Each PE in the CMP architecture hosts a 32-bit RISC processor; the open-source LEON3 unit from Aeroflex Gaisler [28]. It is a general-purpose unit able to perform a wide range of applications, making the designed architecture eligible for several market segments.

In Fig. 4, the main internal blocks of the PE are presented, specifically the core processor and the private slave modules, connected to the AMBA bus. The PE is accessible by off-chip components through a JTAG port for debugging and pre-loading of each core's memories with desired data. Each core utilizes privately addressable memory space, composed of a 32 KB ROM, containing the boot sequence, and a 32 KB RAM, as well as a common memory space composed by the system shared memories. In fact, each layer contains a 32 KB shared memory, placed in the PS, allowing the PE to communicate and exchange data. The access of the cores to the shared space is regulated by a semaphore module present in the PS, able to avoid conflicts in case of simultaneous requests. Multi-core interactions are managed by the NIs implemented both in the PEs and PS. The NIs route data packets to/from the Switch of the 3-D-folded, wormhole-switched NoC. This NoC has been specifically adapted from [29] for the proposed CMP architecture. The 7×7 Switch is characterized by five horizontal interfaces (one for each PEs plus one for the PS) and two vertical ports (for the upper and lower dies), through which 36-bit FLIT (FLow control unITs) packets are transmitted.

IV. In-House Via-Last TSV Process

Throughout this research, a chip-level 3-D integration platform has been developed for KGDs stacking and TSV fabrication [30]. The via-after-bonding (or via-last after BEOL) integration technique [31] is employed for the proposed CMP architecture. Unlike via-first or via-middle techniques [32], where the TSVs are fabricated during the IC fabrication, via-last solution offers the benefit of decoupling the TSV process from the complementary metal–oxide–semiconductor (CMOS) process, allowing the placement of TSVs after the conventional IC fabrication is completed. Moreover, in the proposed approach, the chips are first thinned and bonded, and then the TSVs are fabricated. Therefore, the technique does not require any metal-metal bonding step, which is essential in all via-first approaches. This reduces the complexity of the fabrication process and eliminates the bonding-related reliability issues.

Fig. 5 shows the illustration of the proposed integration approach. The diced chips are tested and KGDs are postprocessed for both layers. The top chip is first etched for the TSV openings and then thinned down to 50 μm by grinding. Compared to the blind-via fabrication techniques where the TSVs are drilled from the backside till the landing metal, this approach is much simpler since it eliminates several fabrication steps, such as metal–metal bonding and passivation layer patterning. On the other hand, the main drawback is that the front-side vias block the BEOL layers; thus, the signal routing on top of the TSVs is not possible. For the bottom chip postprocessing, first a dielectric layer is deposited and patterned, then the redistribution layer (RDL) is fabricated. Since the chips in the stack are identical, RDL is used to reroute the signal to the upper tier. Then, two chips are aligned and bonded with an adhesive bonding technique having a low temperature budget of below 200 °C, to ensure no drift or change on the transistors characteristics. Finally, Cu-TSVs are fabricated by sidewall passivation and Cu electroplating. The electrical connection is realized between the Al pad of the top chip and RDL of the bottom chip. If required, these steps can be repeated for a multilayer stack by using the already-bonded chips as the bottom chip.

The entire TSV process has been developed and experimentally validated at EPFL Center of MicroNano Technology with test chips emulating real CMOS chips. Fig. 6 shows the cross-sections of the lined [30] and fully-filled [33] TSVs developed for the preliminary characterization and verification tests. The

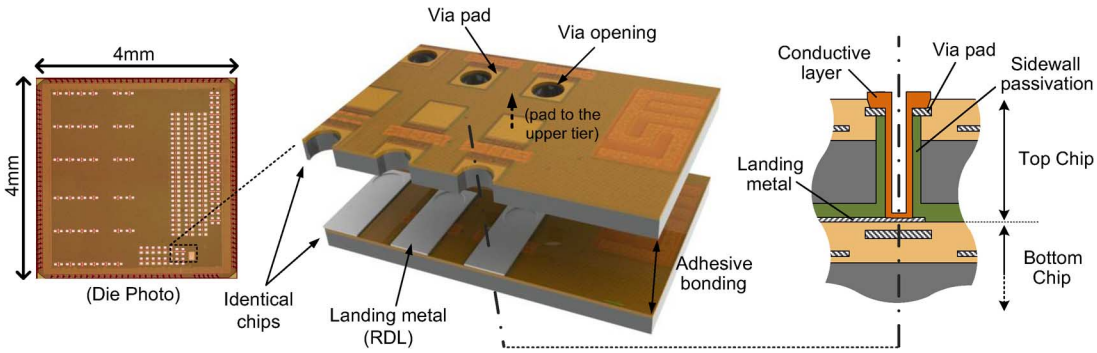

Fig. 5. Schematic cross-section view of the in-house developed copper TSVs with 40 μm diameter, and their placement on the chip.

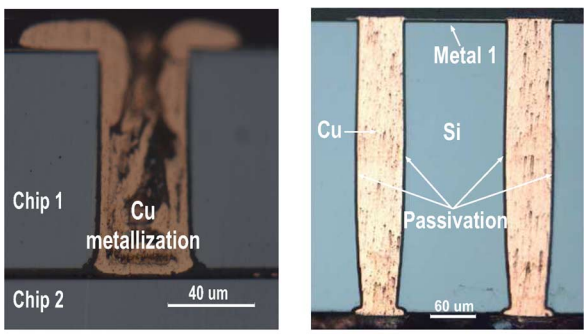

Fig. 6. Cross section of the in-house developed TSVs. (a) Lined TSV connecting two stacked chips. (b) Fully-filled TSV developed for the characterization tests.

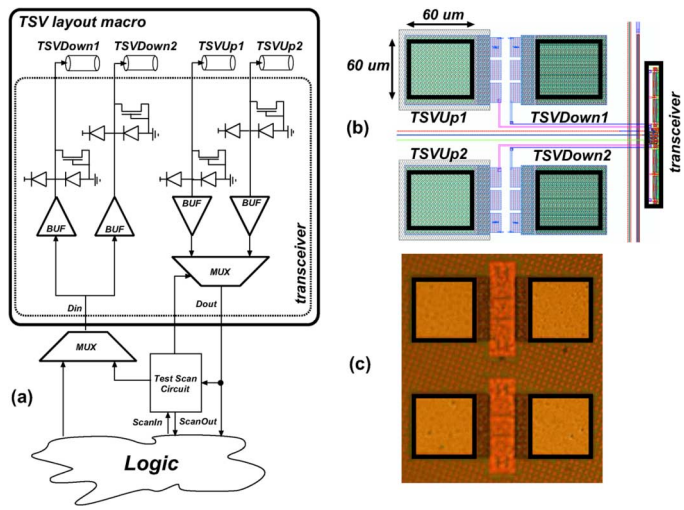

Fig. 7. (a) Circuit schematic of the TSV macro. (b) Layout of the TSV macro, highlighting the main blocks from the corresponding circuit schematic. The effective TSV pad area is put in evidence. (c) Optical microscope image of the TSV macro on the fabricated test vehicle.

daisy-chain resistance measurements demonstrate average TSV resistance of 0.5 Ω.

It is observed that the TSV defects are mostly related to the electroplating step, which is randomly distributed along the chip. Since they do not present any location correlation, the redundant TSVs can be placed as close as possible in order to reduce propagation delay.

V. 3-D Specific Macro Architecture and Circuit Design

A. TSV Redundancy Policy and Circuit Collecting Yield

3-D integration is still a topic of active research. In particular, the nonmature TSV fabrication processes available up to now cannot guarantee, to our best knowledge, the desired yield for the final system. In order to tackle the yield related issues, a redundancy policy has been adopted for the data transmission between layers to ensure reliable communication. Each vertical signal is simultaneously forwarded to the neighbor layer by means of two TSVs, reducing the probability of failure.

Moreover, being able to collect statistics on TSV yield on the final stacked system is desirable. For this purpose, a built-in-self-test (BIST) engine has been implemented. The test is performed at boot time, each TSV is individually tested thanks to a multiplexer inserted in the design to select between the two redundant TSVs. The test pattern is injected through a scan chain; the reader can refer to [29] for a more detailed description of the scan chain design. The statistics are then stored in specific user-visible registers. Additionally, the aforementioned registers provide the selection value to the multiplexers that control, through the redundancy policy, which TSV is used in order to ensure reliable operation of the system. The final TSV-macro is depicted in Fig. 7, presenting the schematic circuit, the layout and a real optical image on a fabricated test chip. For each TSV, two adjacent pads are used, one connected to the TSV of the upper layer and the second one connected to the TSV to the bottom layer. A redistribution layer is used, as shown in the cross section of the TSV macro in Fig. 8. The dimensions of the pad hosting the 40 μm TSV are (60 μm $\times$ 60 μm), in order to avoid alignment problems. The transceiver includes individual ESD protection, a buffer for signal integrity and a weak pull down for each TSV. For data transmission, two different TSV-macros are needed depending on signal direction: a first macro receives the signals coming from the bottom layer and transmits to the top one; the second macro receives the signals from the top layer and transmits to the bottom one. There are three main critical signals in the design that need their integrity to be guaranteed. Hence, additional safety has been incorporated for clock, reset and LayerID signals: they are transmitted over three parallel TSVs and continuously checked during runtime. A glitch-free majority voter is implemented inside each die to

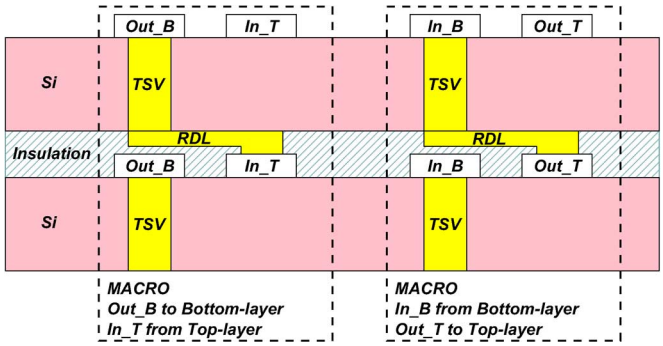

Fig. 8. TSV macro cross-section, highlighting the use of multiple pads and RDL.

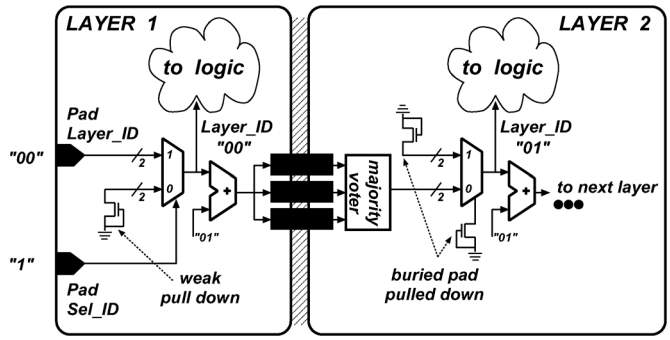

Fig. 9. LayerID generation and propagation between two stacked layers using three redundant TSVs for the signal interface. Schematic of the configured circuit in each layer is shown, unrelated logic is not depicted.

TABLE I
TSVs Features Summary

Overall number of TSVs	120	(95∗)
Total Power TSVs	54	
Total Signal TSVs	66	(31∗)
• Total NoC TSVs	44	(22∗)
• Total JTAG TSVs	10	(5∗)
• Total Control Signal TSVs	12	(4∗)
TSV diameter	40	μm
TSV depth	50	μm
TSV capacitance	1	pF
TSV resistance	0.7	Ω

∗ TSV number without redundancy.

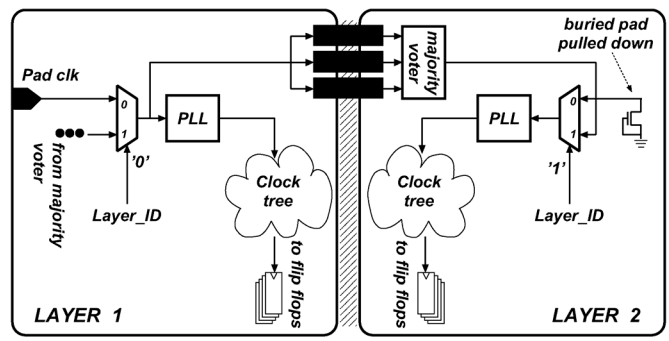

Fig. 10. Clock distribution and propagation between two stacked layers using three redundant TSVs for the signal interface. Schematic of the circuit configured through the LayerID is shown, unrelated logic is not depicted.

ensure the validity of the transmitted bits. A continuous and implicit auto-check of the TSV connection is achieved at the very minor cost of additional area and negligible combinatorial delay, ensuring the correct transmission of the critical signals.

Since only the top-most layer has access to wire-bonded input/output (I/O) and power pads, the power supply (VDD and GND) of all of the bottom layers should also be provided by dedicated TSV. These supply TSVs have a simpler structure and do not incorporate self-check features. A detailed classification of the different purpose TSVs used in this first prototype is presented in Table I, specifying case by case the presence of redundancy with the asterisk.

B. Layer ID Generation Circuit

Once the identical layers are stacked to form a 3-D-IC, they need to operate as a complete system without the need for any further modification or action. Hence, it is necessary to embed specific modules enabling an effective auto-configuration of the layers. For this purpose, a dedicated control signal that provides a different n-bit digital word for each layer has been added, namely the layer identification number (LayerID). Depending on the value of the layerID, each stacked die(layer) knows its position and role in the system and auto-configure itself.

The layerID generation circuit already configured in each layer is depicted in Fig. 9 for a case study of a two-layer system. The starting sequence ("00") is injected through the pads of the top die and is selected by a multiplexer to become the identification value for that layer. The value is also forwarded to a half adder, defining the label for the bottom layer ("01"), to which it is transmitted through three redundant and parallel TSVs. Buried inside the 3-D structure, the pads of the bottom tier are considered inaccessible after stacking; hence they are designed to be internally and automatically pulled-down when no signal is applied to them. As a result, the multiplexer on the second layer is forced to select the LayerID transmitted by the TSV, enabling the identification of the layer's vertical position and the relative self-configuration of the second tier circuitry.

C. Clocking Scheme and Data Transmission

The clock distribution in 3-D-ICs is a complex and challenging task, as presented by Pavlidis *et al.* in [34]. The synchronization of sequential elements located on multiple planes by the same clock signal underlines the importance of controlling the clock skew. With the proposed architecture, each layer has its own clock generation and distribution using a layer-dedicated PLL, hence the obtained clock tree presents minimum skew, high robustness and large tolerance to any timing variation. As depicted in Fig. 10, the clock is injected onto a pad of the top layer, after passing through a PLL module, it is both distributed in the circuit and sent to the three redundant TSVs that propagate it to the next layer. The bottom layer receives the clock from TSVs with triple redundancy which, thanks to the layerID, are selected to enter the PLL module to re-generate the clock signal for maintaining its integrity. This multi-PLL approach results in all layers operating at the same frequency, but being asynchronous from each other due to the unknown phase shift among the clocks.

Transferring signals among different clock domains requires the data to be re-synchronized. For this purpose, data signals are transmitted among layers together with their clock, used by a Dual Clock FIFO to re-synchronize them to the layer clock domain. With this approach the problem of the skew control is intrinsically reduced to a 2-D clock tree synthesis.

In order to reduce the silicon area occupied by the TSVs, data signals are serialized before the transmission through TSVs and successively de-serialized at the receiving layer. The loss in bandwidth due to the serialization can be compensated by increasing the serializer clock frequency, fully exploiting the capability of the sub-micron CMOS processes, as proposed in [35]. However, in the fabricated chip, it has been decided not to implement multi-clock domains, because of the area limitation. Each 32-bit data word that has to be transmitted to the neighboring layer is partitioned into four bytes, and then sent serially through data TSVs that support 8 bits in parallel. The receiving layer reconstructs the original 32-bit word by means of a deserializer after having re-synchronized the data to the layer clock domain. Fig. 1 shows the path of the data transmitted between the dies of a two-layer 3-D system.

D. Physical Design Using Conventional EDA Tools

The design has been implemented in RTL and synthesized with the UMC 90-nm CMOS technology library using Synopsys Design Compiler. The layout has been placed and routed with Cadence Encounter. The functionality has been verified using Mentor Graphics ModelSim. Unfortunately, the current version of Synopsys dc does not support TSVs and 3-D stacking, hence, the synthesis flow has to be performed in several steps. Starting from the synthesizable RTL description, an *ad hoc* set of timing constraints is applied to the TSV macro in order to ensure a correct timing budget between layers. The design is synthesized considering the latencies of the stacked dies. Thanks to the modularity of the design, no additional challenges due to the 3-D target are added to the back-end design. The single die is placed and routed as a traditional 2-D design, following the timing constraints already set up for the synthesis. The TSV macros, designed as full-custom modules with Cadence Virtuoso, are included in the top level design for placement and routing.

VI. 3-D Oriented Testing Policy

The realization of a multi-layer 3-D device poses unique challenges in terms of testability. The proposed architecture enables a complete testing strategy, including both pre- and post-bonding validation, allowing to stack only KGD. Following the fabrication of 2-D samples using a conventional CMOS process, each individual die is fully tested as a single entity, by accessing directly the multi-core processor through the designed frame of 120 I/O pads using a probe card assembly. After this initial testing and validation, functional dies that are destined for 3-D assembly are further processed to manufacture the TSVs. A second pre-bonding validation can be performed to screen dies with non functional TSVs. After postprocessing, a performance test is performed to verify that TSV fabrication induced stress has not altered electrical properties of transistors located nearby

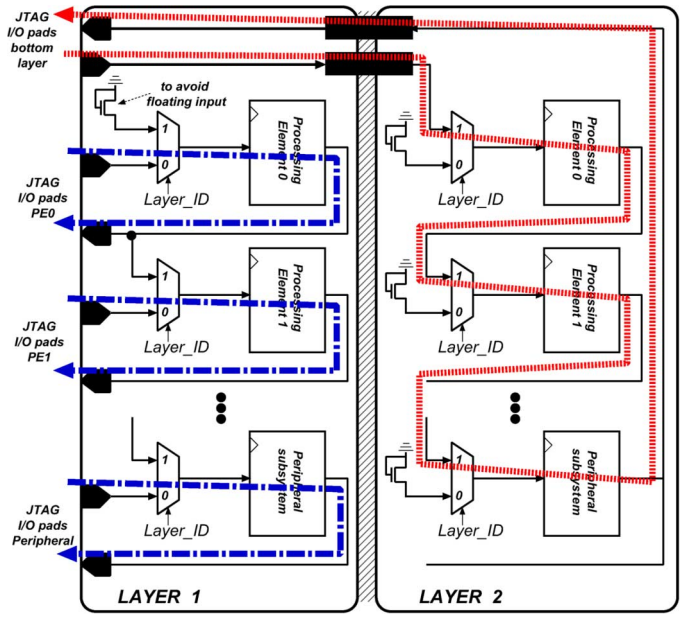

Fig. 11. Block diagram of the multiplexers interface between two stacked layers. The represented circuit is in charge of the scan-chain configurability allowing pre- and post-bonding testability.

the TSVs. Finally, a post-bond test is performed to validate the stacked system. In particular, TSV yield results are determined using the method described in [29]. In future prototypes, sensing circuitry can be integrated in each TSV macro to verify their stand-alone functionality with a capacitance measurement [36]. Once the two layers are assembled, I/O pads are no longer accessible in the bottom tier, therefore a custom testing method based on boundary scan chain has been developed. This requires embedding additional modules, enabling the communication through JTAG signals between an external debugger and the processors. In particular, each layer contains a JTAG interface for the management of the debug signals according to layer position in the stacked structure, defined by the LayerID. The interface is shown in Fig. 11.

For the verification of a stand-alone die, the set of multiplexers is forced to assign the JTAG external signals from the I/O pads to JTAG ports dedicated to each PE. With this approach, each core is accessed in parallel. The top layer of the stacked structure exploits the same configuration. In the bottom layer, the pads are buried during the bonding process, hence the LayerID configures the multiplexers interface to receive the JTAG signals from the upper layer pads through the TSVs. Moreover, the cores are automatically arranged in a chain, that can be accessed serially through the single set of JTAG signal. A representative image of the resulting testing procedure for a two-layer configuration is presented in Fig. 12.

VII. Experimental Results

The features of the novel architecture have been implemented on a test vehicle, in order to explore the benefits of the proposed approach. 2-D-CMPs have been realized using a standard UMC 90-nm CMOS technology. The functional blocks of the test chip

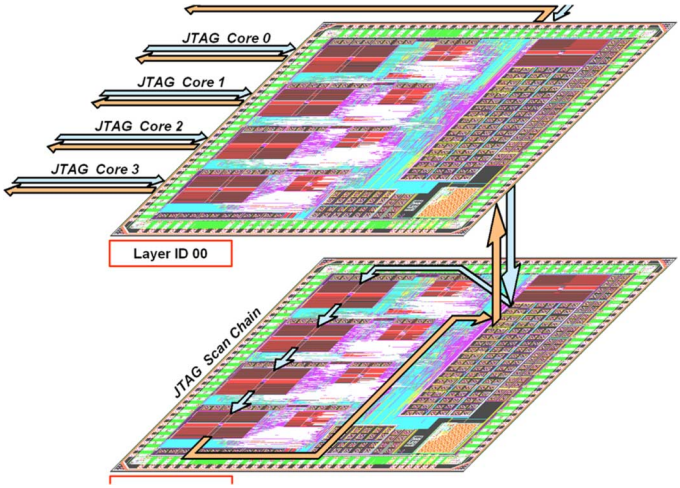

Fig. 12. Auto-configuration for testability. Top layer cores are accessed in parallel from the pads. The processors on bottom layer are configured in a scan chain for the debug procedure: JTAG inputs are transmitted from top to bottom die, the TDO produced on the bottom layer returns up to the top one.

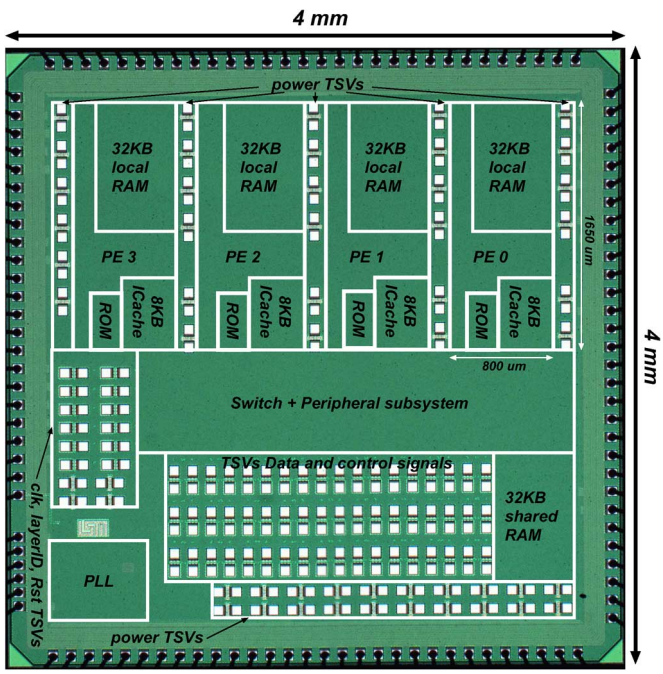

Fig. 13. Single die microphotograph. Pads for signal and power TSVs are visible before the postprocessing. Main blocks are identified in the image (PE, PS, Switch of the NoC, PLL). Size of the full-chip and of the PE footprint are also shown.

are identified in the die micro-graph in Fig. 13. Table II lists the main specifications of a two-layer test prototype.

A. Design Verification

Postlayout simulations in ModelSim verify the correct functionality of the system and extract its performance parameters: each layer has been synthesized with a target operative frequency of 400 MHz, which results in a vertical data bandwidth of 3.2 Gb/s.

Particular attention has been dedicated to the verification of the system behavior at the interface between the two stacked layers. An emblematic case is a core's read/write request to the shared memory of the next layer. Waveforms showing a memory write operation (followed by a read verification) are presented in Fig. 14. JTAG signals are injected requesting core 0 of the top layer to write a 32 bit word, "0XABBAABB0," in the shared memory of the bottom layer [Fig. 14(1)]. Core 0 delivers the request to the NoC [Fig. 14(2)], which encapsulates it in a frame and forwards it to the 3-D interface [Fig. 14(3)]. A serializer divides the encapsulated data in 4 bytes sending them one by one through the TSVs together with a valid signal and the layer clock [Fig. 14(4)]. In the bottom layer, the received data signals are re-synchronized to the local clock domain through a Dual Clock FIFO [Fig. 14(5)]. Then they are de-serialized and sent to the shared memory [Fig. 14(7)]. Further reading of the same location verifies the correctness of the previous operation [Fig. 14(8)], sending out to the JTAG TDO the data packet [Fig. 14(9)].

TABLE II
ARCHITECTURE DETAILS OF 3-D TEST VEHICLE

Process technology	90nm CMOS
Number of layers	2
Die size	4x4 mm
Core footprint	800x1650 μm
Number of cores	8
Total on-chip memory	320 KB
Max operative frequency	400 MHz
Vertical data bandwidth	3.2 Gbps
Number of I/O pads	120

B. FPGA Emulation

The basic functional verification is not sufficient to guarantee the correct behavior of the multi-core structure. Hence, the full 3-D system has been emulated on a Xilinx Virtex5 FPGA board in order to observe the system running. A complete testing procedure, shown in Table III, has been developed in order to debug the device by an external source.

The positive results obtained confirm the correctness of the 3-D multi-processor design, proving the capabilities of interaction among cores located in different layers. In particular, the core's read/write request to the shared memory of the next layer, described in the previous section, has been repeated on the FPGA model, demonstrating the optimal intra-layer communication. Moreover, this procedure is able to verify the correct behavior of the NoC during the packet routing; both the NIs and the switches present a two clock cycles latency. The FPGA emulation enables also the verification of the auto-configuration of the different layers according to their identification signal. The behavior of the self-verification strategy applied to the redundant TSV is validated emulating possible faults causing opens on the TSVs (more frequent problem in TSV technology process).

C. Testing Setup for Prototype Chips

The standalone and modular philosophy of the architecture provides an increased level of testability of the system. It allows the application of a coherent validation procedure both to each of the individual layers and the stacked structure. Both

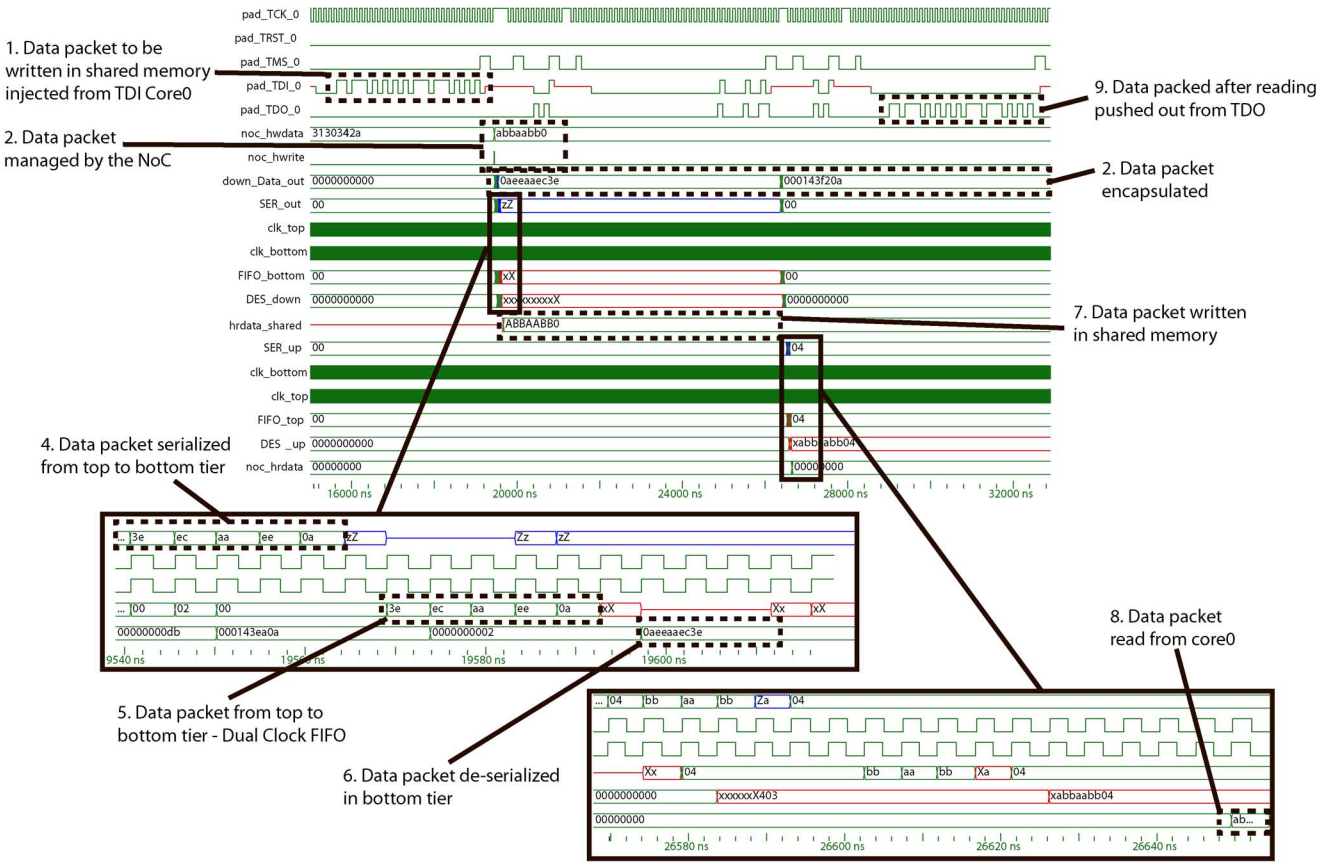

Fig. 14. Postlayout simulation waveforms describing a inter-layer operation: One core is requesting to write a word on the shared memory of the bottom tier, via JTAG.

TABLE III
SUMMARY OF THE TESTED FUNCTIONALITIES

Procedure	Validation
1.	Read own IDcod
2.	Read ROM content
	Read/Write from private RAM
	Read/Write from shared RAM
3.	Binary download & execution
4	TAP controller bypass
	Scan chain of multiple cores
5.	Test of Top and Bottom layer together

components and methodology were chosen so that they could be reused between the different phases. The testing protocol, already shown in Table III, has been applied both to packaged and naked single dies through a specifically designed Probe Card setup, attached to a manual Probe Station (Karl Suss PM8).

The testing source consists of a custom software running on a host computer, able to translate the user commands in input bit vectors. An open-source tool, namely OpenOCD, was chosen as the base of the software debugger infrastructure. After extensive adaptation of the original code, it has been possible to apply the testing procedure previously described.

An USB-to-JTAG converter transmits these vectors to an FPGA board that acts as an interface to the prototype dies. In particular, the programmable unit, integrated on the Probe Station, is in charge of selecting to which cores the test is addressed, setting them in an external scan chain. By utilizing such an approach, it is possible to physically link all cores of all layers with a unique path inside the FPGA board, allowing the same methodology to be used for both individual layer and stacked structure verification.

The processed JTAG debug signals are transmitted through a system of printed circuit boards (PCBs) able to generate all power supplies, clock sources and control signals for the chips. The 120 signals applied to the I/O pins of the device are then transmitted to the Probe Card's needle frame, which is contacting the chip I/O pads.

D. 2-D Prototype Testing

The set of tests applied to the FPGA emulator is then reapplied to the 2-D naked dies of the prototype. Valid response sequences has been registered on the ASIC stand alone multi-core layers ensuring the expected behavior of all the specific functionalities of the single dies, prior to 3-D stacking. It has been possible to access and test each single core validating basic and complex behavior of the processors, including reading and writing from the entire addressable memory space. Checking of the boot sequence inside the ROM, reading/writing operation from both private and shared memories have been verified. Particular effort has been invested for downloading routines inside the private RAM memory of each core; with their execution it has been possible to verify the in-layer multi-core interactions through the shared memory. The complete test procedure has been validated in a wide range of frequencies, starting from 1 MHz and reaching the target frequency of 400 MHz.

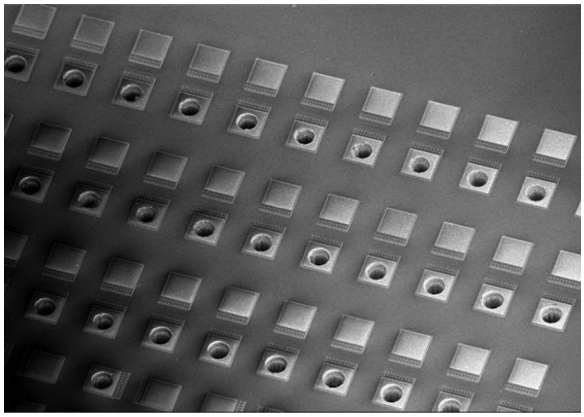

Fig. 15. SEM image of the multi-core die with postprocessed TSV openings.

E. 3-D Prototype

The proposed testing strategy has led to the identification of KGD, that are then postprocessed in the clean-room for the TSV fabrication, exploiting the via-last TSVs presented in Section IV. The technology has already been validated and the fabricated TSVs have been shown to be fully functional by connecting them in a daisy chain on a test wafer. A scanning electron microscope (SEM) image of the actual multi-core die with fabricated TSV openings is shown in Fig. 15.

In order to increase the yield of the final stacked structure, the planned methodology includes the repetition of the same testing procedure to the single chips after the TSV etching process, verifying that no electrical or mechanical damage has occurred during the in-house postprocessing and TSV fabrication.

VIII. Conclusion

This paper presents a modular 3-D stacked multi-processor platform that is composed of identical dies that are interconnected by TSVs. Stacking identical, fully testable multi-processor dies with four processing elements and memory units on each die, leads to an increased yield for the final 3-D system, built out of KGD. Moreover the homogeneous integration approach presented in this work can offer a significant reduction of the nonrecurring engineering cost. Coherent design and testing strategies are proposed and demonstrated to ensure robust operation. A test vehicle, consisting of two layers, has been fabricated using standard UMC 90-nm CMOS process. Single dies have been tested to be functional, and then processed for the in-house TSV fabrication and stacking. The proposed 3-D system can operate at 400 MHz, with a vertical bandwidth of 3.2 Gb/s.

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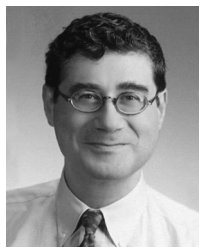

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