Logic-Compatible Multilevel Gain-Cell-Based DRAM for VLSI-SoCs

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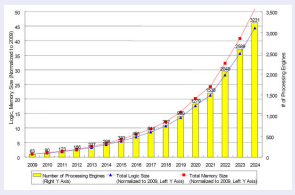
Motivation

Increasing need for **embedded memories** in VLSI SoCs and ASICs

Many systems require only **short retention times**

- Skip refresh cycles
- Compromise retention time for higher storage density



SoC Consumer Portable Design Complexity Trends [ITRS'09].

Major options for embedded memories

SRAM	Large storage cell
eDRAM Multilevel DRAM	Special technologies (expensive)
Gain cell **Multilevel gain cell**	Small and logic-compatible **High storage density for SoCs requiring short retention times**

[ITRS'09] *"International Technology Roadmap for Semiconductors,"* 2009 Edition, http://www.itrs.net

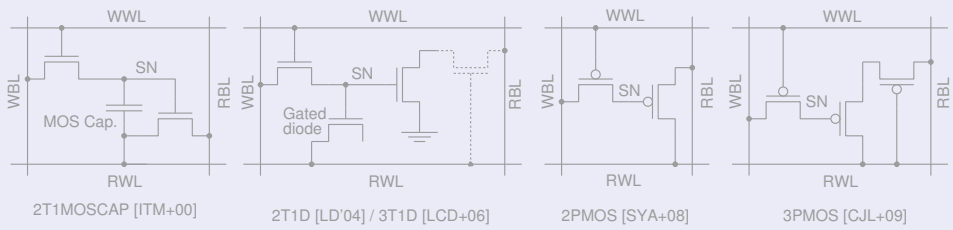
Previously reported single-bit gain cells

Coupling capacitor between *storage node* (SN) and *read word line* (RWL)

- SN boost $\Longrightarrow$ faster read operation

Storage transistor (ST) and *read transistor* (RT) in one device

- Leakage through unselected cells $\Longrightarrow$ limited number of words per *read bit line* (RBL)

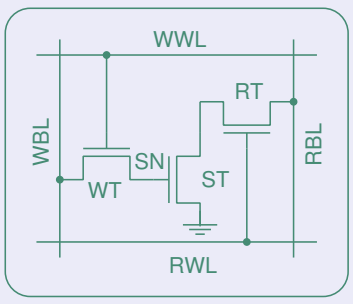


[ITM+00] N. Ikeda et al., *"A Novel Logic Compatible Gain Cell with two Transistors and one Capacitor,"* in Proc. IEEE Symposium on VLSI Technology, 2000
[LD'04] W. Luk et al., *"2T1D Memory Cell with Voltage Gain,"* in Proc. IEEE Symposium on VLSI Circuits, 2004
[LCD+06] W. Luk et al., *"A 3-Transistor DRAM Cell with Gated Diode for Enhanced Speed and Retention Time,"* in Proc. IEEE Symposium on VLSI Circuits, 2006
[SYA+08] D. Somasekhar et al., *"2GHz 2Mb 2T Gain-Cell Memory Macro with 128GB/s Bandwidth in a 65nm Logic Process,"* in Proc. IEEE International Solid-State Circuits Conference, 2008
[CJL+09] K. Chun et al., *"A Sub-0.9 V Logic-compatible Embedded DRAM with Boosted 3T Gain Cell, Regulated Bit-line Write Scheme and PVT-tracking Read Reference Bias,"* in Proc. IEEE Symposium on VLSI Circuits, 2009

Multilevel Gain Cell Design

Requirements for **multilevel** gain cell

- Ease multilevel sensing $\Longrightarrow$ no SN boost
- Must distinguish small differences in sensing current $\Longrightarrow$ separate RT



Best gain cell topology for multilevel storage.

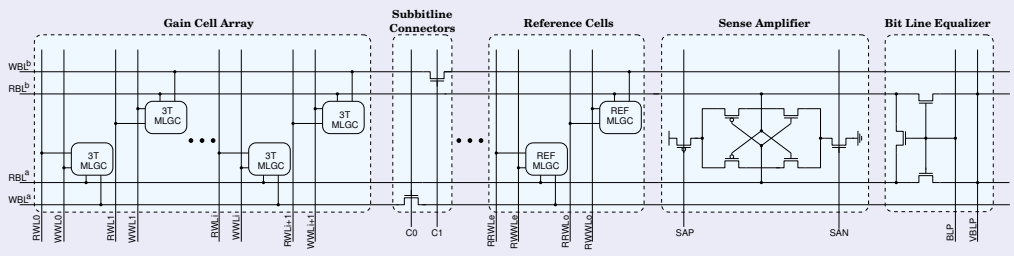
WT	High-V_{th}	Minimum subthreshold leakage
RT	High-V_{th} Low-V_{th}	Maximum number of words per RBL Fast read access
ST	Low-V_{th}	Large useful SN storage range

Write word line (WWL) overdrive and reliability concerns lower bound the SN voltage range

Multilevel Write and Read Operations

Level generation

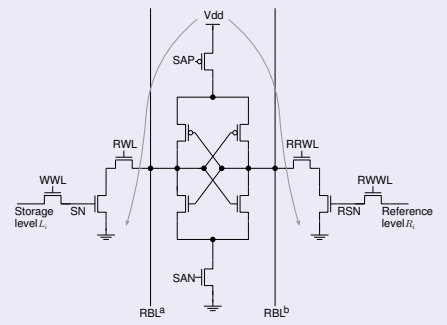
- Charge sharing between bit line segments



Folded bitline architecture.

Multilevel sensing

- Successive approximation algorithm
- Unbalancing the sense amplifier: activate current path through the *gain cell being read* and the *reference gain cell*



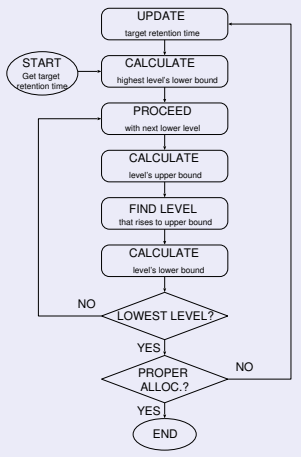
Sensing scheme.

Storage and Reference Level Allocation

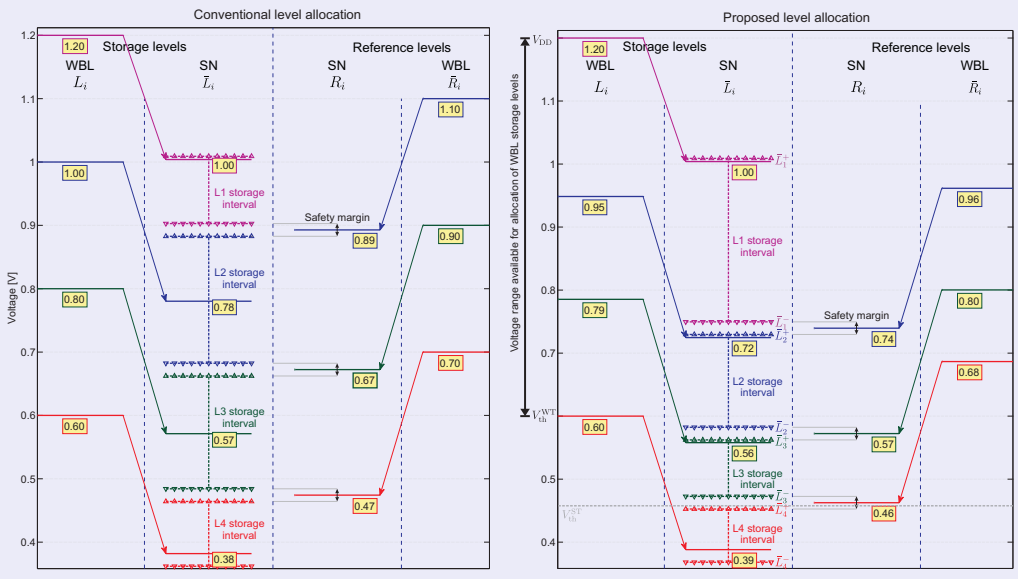
Allocation **optimization algorithm**

- All storage levels reach their upper/lower bound after the same time under the respective worst-case leakage conditions
- In 90-nm CMOS, the leakage mechanisms discharging the SN (GIDL current of the WT and gate tunneling of the ST) dominate over the leakage mechanisms charging the SN (subthreshold conduction of the WT under worst-case WBL state)

Retention time boost of 148 % from 31 µs to 77 µs (@ $85\,^{\circ}\mathrm{C}$, 2 bits per cell)



Optimization algorithm.



Conventional and proposed storage and reference level allocation.

Conclusion

The approach of **storing many bits per cell** has been applied to **gain cells**

A **fully logic-compatible gain-cell-based 2-bit-per-cell DRAM** with **simple level generation technique** and **non-destructive multilevel sensing scheme** has been presented

The proposed **storage and reference level allocation algorithm** can **increase the retention time by 148 %**