Standard-Cell Based Memories (SCMs): from Sub-VT to Error-Resilient Systems

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Motivation & Research Overview

Increasing Need for Embedded Memories (ITRS'09) in ...

<table>
<thead>
<tr>
<th>Robustness</th>
<th>Area priority</th>
<th>Supply Voltage</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Robust</td>
<td>Robust</td>
<td>Very Low</td>
<td>Very Slow</td>
</tr>
<tr>
<td>Secondary</td>
<td>High</td>
<td>High</td>
<td>Fast</td>
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</tbody>
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State of the art

- SRAM with 10T bits [1, 2] vs. 8T bits [2]
- eDRAM: special technology, extra cost
- Gain-cells: logic-compatible

Reliable Sub-VT SCMs

Sub-VT compilation and characterization flow [6]
- Above-VT synthesis, STA, and power analysis
- Analytical sub-VT model [7]
- Ideal for quick design-space exploration

Leakage is dominant, active energy negligible
- Only smallest SCMs reach EMV in sub-VT domain

SCMs guarantee functionality in any system from reliable sub-VT to error-resistant high-performance, at any supply voltage

Best-Practice SCM Implementations

SCM building blocks

- Architectural comparison results true for different technologies, nodes, fabs, and library providers [4]

Key Points

- Functional in any system, at any voltage
- Synthesizable, any size, no power routing
- Faster than sub-VT SRAM, smaller than 6T SRAM

SCMs for Error-Resilient Systems

System tolerates a few errors in memory

- Dynamic latches w.r.t. static latches
  - Smaller
  - Less reliable

SCMs are smaller than SRAM for storage capacities up to 2kb

- Functional in any system, at any voltage
- Synthesizable, any size, no power routing
- Faster than sub-VT SRAM, smaller than 6T SRAM

SCMs are immediately robust in sub-VT domain [3]
- Write & read failures encountered in 6T SRAM are avoided by standard-cell latch
- Still good hold-SNM at \( V_{DD} = 300\text{mV} \)

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>SRAM macro</th>
<th>SCM</th>
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<tr>
<td>( V_{DD} ) [mV]</td>
<td>380</td>
<td>350</td>
</tr>
<tr>
<td>( f_{max} ) [MHz]</td>
<td>475</td>
<td>25</td>
</tr>
<tr>
<td>( f_{SNM} ) [MHz]</td>
<td>65.6</td>
<td>884.4</td>
</tr>
<tr>
<td>Area [um²/bit]</td>
<td>2.9</td>
<td>6.0</td>
</tr>
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</table>