Single-Photon Avalanche Diodes in sub-100nm Standard CMOS Technologies

Mohammad Azim Karami, Hyung-June Yoon, and Edoardo Charbon
Faculty of EEMSC, Delft University of Technology, Netherlands

Tel: (+31) 152783652, Fax: (+31) 152786190, Email: m.a.karami@tudelf.nl

Abstract— **Single-photon avalanche diodes (SPADs) are evaluated in two sub-100nm CMOS technologies. Several geometries are implemented, whereas premature edge breakdown (PEB) prevention is achieved with n-well rings. The octagonal SPADs are implemented in 90nm and 65nm standard CMOS technologies. Full characterization of SPAD performance is carried out as a function of bias and temperature. To the best of our knowledge, this is the first report of SPAD in any 65nm CMOS technology.**

***Index Terms*—Single-Photon Avalanche Diode, Deep-submicron technologies**

I. Introduction

Among solid-state single-photon detectors, Single-Photon Avalanche Diodes (SPADs) have recently emerged as a unique solution. The device consists of a p-n or n-p junction reverse biased above breakdown, thus enabling Geiger mode of operation where the optical gain is virtually infinite [1]. A photon absorption in the multiplication region may cause electron-hole pair generation, which may result in an avalanche of free carriers due to the high electric field present after the breakdown voltage. Upon avalanche triggering, buildup and spread phases follow, while the avalanche is stopped during a quenching phase. During the detection cycle, a current pulse is generated and may be converted to a digital signal [1], [2].

Deep-submicron SPADs could enable in principle smaller pixels, more on pixel functionality, higher speed, and higher fill factors [3]. However, challenges are associated to feature size reduction, namely higher tunneling noise due to high doping, lower photon absorption rates due to thinner depletion regions, thicker optical stacks, and higher surface recombination due to the lower depth of the multiplication regions [4].

Band-to-band and trap-assisted processes are the main tunneling noise sources in SPADs, restricting the noise performance of SPADs in deep-submicron technologies. To maximize the effectiveness of PEB prevention structures and minimize expected band-to-band tunneling effects, the devices were modeled and simulated before fabrication in 65nm and 90nm standard CMOS technologies. To verify the models two "SPAD farms" were designed and fabricated. Families of test structures are built based on n-well guard ring in both 90nm and 65nm technologies. Standard characterization is performed to choose the SPAD topologies with lowest noise and highest quantum efficiency in both technologies.

To the best of our knowledge these are the first SPADs being demonstrated in sub-130nm standard CMOS technologies.

II. SPAD Design and Simulation

A guard ring made out of lightly doped regions, or an oxide layer is necessary to shape the electric field profile, so as to prevent PEB. Figure 1 shows the cross-section of a SPAD with STI/n-well guard ring demonstrating photon counting abilities in 90nm and 65nm technologies.

A shallow-trench isolation (STI) region is used to maximize compactness. While STI is used as an insulation part making the guard ring more compact, it contributes to the noise due to lattice imperfections where free carriers can be temporarily trapped and released to trigger spurious avalanches [5]. The photon absorption takes place in the depletion region below n+ and the generated electron-holes travel to the multiplication region which is located at the interface between n+ and p-substrate.

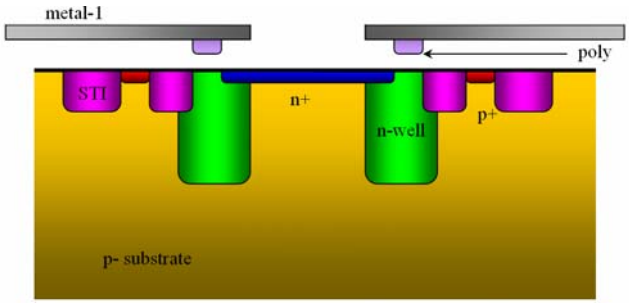

Fig. 1. Cross-section of SPAD using an n-well based guard ring. Note that the STI delimits the SPAD, while the guard ring ensures that the electric field be maximized in the center of the device.

The SPAD structures are simulated to minimize dark count noise and to maximize photon detection probability. Figure 2a and b show a simulation of the electric field on the p-n junction surrounding the 90nm and 65nm SPAD areas, respectively. The simulation was carried out with the SPECTRA [6] imaging device simulator at 0.2 V above

breakdown (i.e. the excess bias voltage). The figures show that the maximum electric field is confined to the active region of the SPAD, with an electric field below critical everywhere else. This condition is necessary to achieve PEB prevention.

The simulation results were confirmed by imaging the SPAD photoluminescence while avalanching. This technique enables one to identify which areas of the device do develop avalanches [7]. The photoluminescence images of both 90nm and 65nm SPADs demonstrate the avalanche occurrence only in the active region and not in the guard rings, thus confirming a successful PEB prevention.

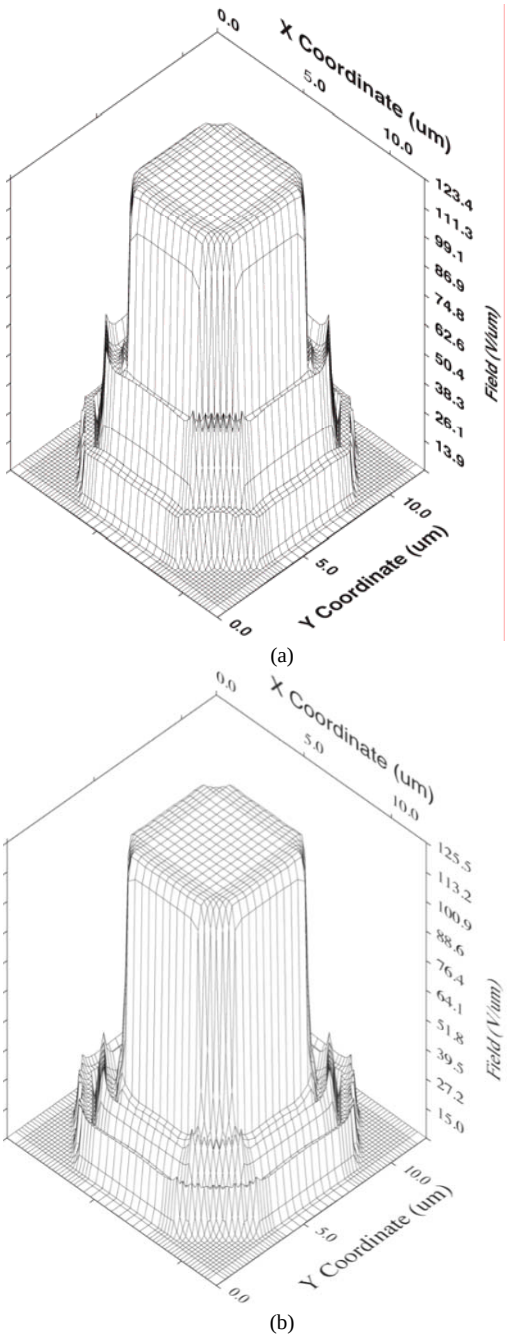

Fig. 2. (a) SPECTRA simulation of the electric field distribution of 90nm SPAD with an excess bias voltage V_e=0.2 (b) SPECTRA simulation of the electric field distribution of the designed 65nm SPAD under the same conditions.

While circular shaped SPADs are generally preferred due to the lack of sharp edges [8], octagonal shaped SPADs were implemented due to the technology restrictions. Figure 3 shows the photomicrograph of the octagonal SPAD implemented in 90nm and 65nm technologies. The guard rings of both SPADs are covered with metal to prevent photon absorption in the guard ring region, which can result in higher noise and higher afterpulsing probability.

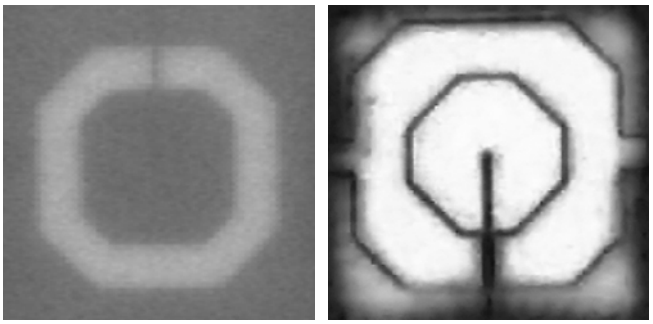

Fig. 3. SPAD photomicrograph in 90nm technology (left), and 65nm technology (right). The edge of each structure measures 8μm.

Figure 4 shows the I-V characteristic measurement in 90nm and 65nm technologies performed at room temperature. The breakdown voltage of the SPAD is decreased from 10.4V in 90nm technology SPAD to 9.5V in 65nm technology SPAD. Lower breakdown voltage for 65nm technology is in agreement with the simulations, due to higher doping profiles.

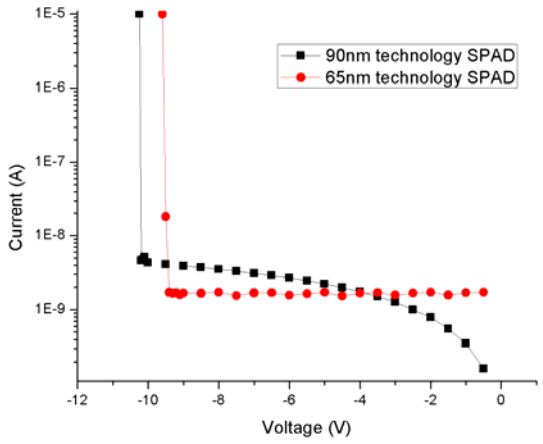

Fig. 4. I-V characteristic of 90nm and 65nm technology SPAD at room temperature.

Figure 5 shows the dark count rate (DCR) measurement of 90nm, and 65nm SPADs for different excess bias voltages and temperatures. The main sources of DCR are Shockley-Read-Hall generation, band-to-band tunneling and trap-assisted tunneling or generation. The 65nm SPAD shows higher DCR

levels and lower dependency of DCR from temperature.

While at low excess bias voltage the DCR is mainly caused by SRH generation, at higher bias voltages tunneling becomes dominant [9]. This behavior is in line with expectations, however, lower levels of DCR are desirable in several applications involving photon-starved imaging. To achieve these goals, further device optimization is required.

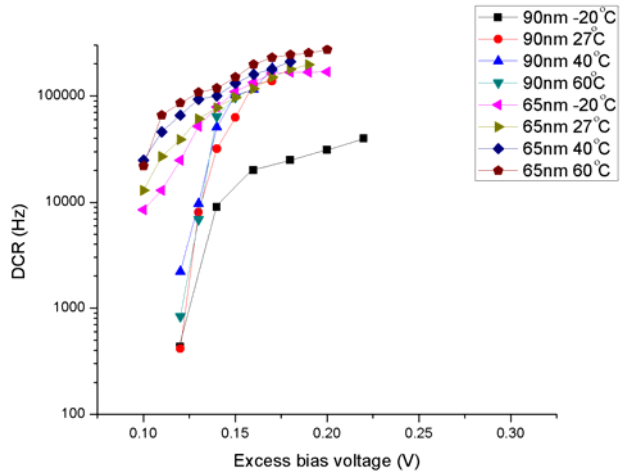

Fig. 5. DCR of 90nm and 65nm SPAD at different bias voltages and at different temperatures.

Figure 6, shows the Photon Detection Probability (PDP) of the 90nm SPAD in different wavelengths range. The PDP measurement is performed at 0.17 V of excess bias voltage. The peak of PDP is 16% at 520nm of wavelength. Lower PDP in deep-submicron technologies, if compared with older processes, is due to thinner multiplication regions, and thicker and more complex optical stacks. The higher doping profiles and shallower junctions also result in higher PDP in blue and UV regions.

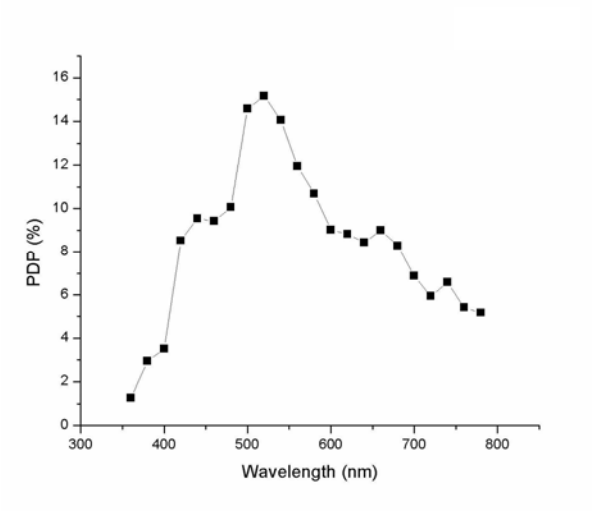

Fig. 6. PDP of 90nm SPAD in different wavelengths at the room temperature.

The jitter measurements, shown in Figure 7, were performed with two 40MHz laser sources at 405nm and 637nm wavelength. The figure shows a histogram of a TCSPC experiment on the SPAD. The Full Width Half Maximum (FWHM) uncertainty of the response is reported in Table 1.

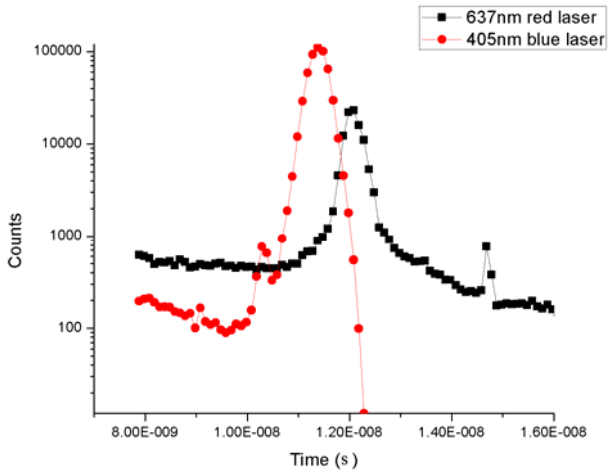

Fig. 7. Histogram of the timing response of the 90nm SPAD.

Afterpulsing was characterized using discrete autocorrelation measurements of SPAD output signals. The resulted value of 32 % at the nominal dead time is being reported while the dead time is higher in these technologies because of the off-chip quenching being performed for the first SPAD farms.

III. Results and Discussion

Standard characterization of the 90nm and 65nm SPAD was performed at different temperatures and excess bias voltages. Table -1 shows the summary of characterization results.

Performance	90nm SPAD	65nm SPAD	Unit	Comments
Diameter	8	8	µm	Octagonal shape
DCR	8.1	61	kHz	V_e=0.13V, T=293K
Timing jitter	398	-	ps	FWHM at 637nm wavelength
	435	-	ps	FWHM at 405nm wavelength
PDP	12	-	%	V_e=0.15V
Afterpulse probability	32	-	%	At nominal dead time
Breakdown voltage	10.4	9.5	V	Different guard ring
Spectrum	360-800	-	nm	

Table -1. Performance summary. All measurements were conducted a room temperature, unless otherwise stated.

IV. Conclusions

Solid-state detectors capable of resolving single photons are useful in a number of applications, from lifetime imaging to 3D vision, from gamma detection to fluorescence correlation spectroscopy. Increasingly, these applications are requiring complex functionality and high operating speed. In this paper a new family of Single-Photon Avalanche Diodes (SPADs) was designed, simulated, and implemented in sub-100 nm standard CMOS technologies. The paper presents a complete characterization of two SPADs designed in 90nm and 65nm technologies. The SPAD performance is compared and discussed with respect to the technology in which the devices were implemented. To the best of our knowledge, the 65nm SPAD is the first device implemented in this feature size.

References

[1] S. Cova, M.Ghioni, A. Lotito, I. Rech, and F. Zappa, "Evolution and prospects for single-photon avalanche diodes and quenching circuits", Journal of modern optics, **51**, 1267-1288 (2004).

[2] A. Rochas, M. Gani, B. Furrer, P. A. Besse, R. S. Popovic, G. Ribordy, and N. Gisin, "Single photon detector fabricated in complementary metal-oxide-semiconductor high voltage technology, "Review of Scientific Instruments, **74**, 3263-3270 (2003).

[3] M. Gersbach, J. Richardson, E. Mazaleyrat, S. Hardilier, C. Niclass, R. Henderson, L. Grant, and E. Charbon, "A low noise single photon detector implemented in a 130nm CMOS imaging process", Solid state Electronics, **53**(7), 803-808 (2009).

[4] N. Faramarzpour, M.J. Deen, S. Shirani, and Q. Fang, "Fully integrated single photon avalanche diode detector in standard CMOS 0.18 um technology", IEEE Transaction on electron devices, **53**(3), 760-767 (2008).

[5] H. Finkelstein, M. J. Hsu, and S. C. Esener, "STI-bounded single-photon avalanche diode in a deep-submicrometer CMOS technology", IEEE Electron Device Letters, **27**, 887-890 (2006).

[6] Link Research Corporation, Japan, Spectra 3-d device simulator, Release 5.4 (2009).

[7] M. Gersbach, "Single-photon detector arrays for time-resolved fluorescence imaging", PhD thesis, EPFL (2009).

[8] M. A. Karami, M. Gersbach, E. Charbon, "A new single-photon avalanche diode fabricated in 90nm CMOS standard technology", SPIE Optics and Photonics (2010).

[9] M.A. Karami, L. Carrara, C. Niclass, M. Fishburn, E. Charbon, "RTS noise characterization in single photon avalanche diodes", Electron device letters, **31**(7), 692-694 (2010).

[10] M. A. Karami, M. Gersbach, H. J. Yoon, E. Charbon, "A new single-photon avalanche diode in 90nm standard CMOS technology", Optics Express, **18**(21), 22158-22166 (2010).