A GSM-GPRS/UMTS FDD-TDD/WLAN 802.11a-b-g Multi-Standard Carrier Generation System

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***Abstract*—A compact carrier generation system enabling proper interoperability among quad-band GSM, WCDMA (FDD and TDD), and WLAN (802.11a/b/g) standards is developed. The implementation is achieved in 0.25-μm BiCMOS-SiGe process. The measured tuning range is higher that 1 GHz (3.05 to 4.1 GHz) exceeding the specifications by 25%. The voltage-controlled oscillator (VCO) exhibits a phase noise of −118 and −125 dBc/Hz measured, respectively, at 400 kHz and 1 MHz offsets while drawing 2.5 mA from 2.5 V supply. The measured phase noise at 400 kHz offset of the PCS/DCS output local-oscillator (LO) signal and the GSM output LO signal is, respectively, −124 dBc/Hz and −130 dBc/Hz.**

***Index Terms*—Analog front-end (AFE), frequency synthesizer, GSM, multi-standard, phase noise, phase-locked loop (PLL), UMTS, voltage-controlled oscillator (VCO), wireless communications, WLAN.**

I. Introduction

THE fundamental requirements driving the wireless communication market today are the global mobility and the wide range of the proposed services. These two forces have resulted in two complementary mature technologies: WLAN (IEEE 802.11a/b/g) for high bandwidth, hot spot local coverage; and cellular handset for voice communication with wide area coverage. Both of them have recently experienced a shift from single system connectivity to multi-system connectivity. Single chip systems fully compliant with the IEEE 802.11a/b/g standards were recently presented [1]–[3]. In the case of cellular systems, the interoperability is motivated by the fact that the 3G (UMTS) will coexist with 2–2.5G (GSM/GPRS). Various solutions were proposed to integrate these standards in the same chip [4], [5]. On the other hand, the modern handsets are designed to handle more and more high-data-rate applications such as games, graphics, audio and video, etc. These requirements can be fulfilled by the convergence of cellular 2G–3G standards and WLAN technology in the same handset [6]. However, without an intensive innovation effort, the processing complexity, memory and power consumption of such systems will be so huge that they will never result in a viable commercial product. One of the challenging blocks to design in such transceivers is the multi-standard carrier generation sub-system [7]. These frequency synthesizers should enable proper interoperability and seamless connectivity among the various standards considered.

In the first section of this paper, we discuss potential synthesizer architectures for a multi-mode quad-band GSM (GSM 850, GSM 900, DCS1800 PCS 1900), WCDMA (FDD and TDD) transceiver. Afterward, the extension to the WLAN (802.11a/b/g) is introduced and a compact, flexible, cost-effective and low-power topology is presented. The prototypes were manufactured in 0.25-μm BiCMOS-SiGe process. Since the RF parts of such multi-mode system concentrate the majority of challenges and aggressive design specifications, the focus will be on this part. Circuit design techniques for both active and passive parts of the voltage-controlled oscillator (VCO), buffers, quadrature mixer and high-frequency dividers are discussed. Experimental results are summarized in the last section.

II. Architectural Options and Frequency Planning

The frequencies of the local-oscillator (LO) signals and thus the design of the synthesizer are strongly correlated with the adopted topology for the multi-mode transceiver. Zero-IF and Low-IF are the most promising architectures for 3G and 4G mobile terminals [6]–[8], since they lend themselves to monolithic integration much more easily than the other architectural candidates. For instance, superheterodyne architecture requires an off-chip high Q channel select filter (e.g., SAW) at a relatively high frequency. In Zero-IF and Low-IF, the requirements on the channel select filter as well as on the sampling frequency of the analog-to-digital converter (ADC) are significantly relaxed, making a low-power and single-chip integration of the transceiver more realistic. In general, the choice between Zero-IF and Low-IF architecture is conditioned by the tradeoff, for each standard, between the impact of the I/Q phase and amplitude imbalance (more severe in Low-IF) and the 1/f noise and DC- offset (more severe in Zero-IF). Moreover, a reconfigurable Low/Zero IF architecture seems also a very promising option to enhance the interoperability of the transceiver [8]. The present carrier generation system will be designed to enable both Low-IF and Zero-IF multi-mode transceiver. The challenging specifications in terms of frequency tuning range and phase noise that should be fulfilled are summarized in Table I. For all these modes, the same synthesizer will be used to cover the transmitter (TX) bands as well as the receiver (RX) bands. For WCDMA FDD,

Manuscript received November 15, 2005; revised January 31, 2006. This work was supported in part by the Swiss Office Fédérale de l'Education et de la Science within the European ST project MuMor under contract IST-2001-3461.

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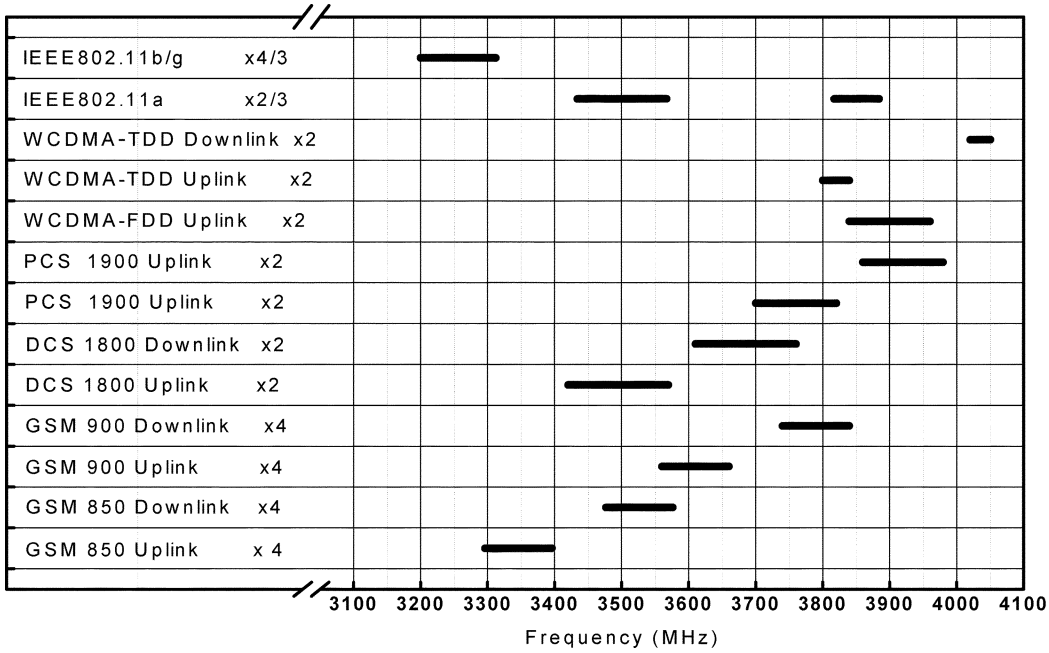
Digital Object Identifier 10.1109/JSSC.2006.873928

TABLE I
BRIEF DESCRIPTION OF THE TARGETED STANDARDS

Standards		F[min-max] (MHz)	Channel (MHz)	PN (dBc/Hz)	Modulation	Suitable Architect.
GSM	850-900 DCS PCS	824-960 1710-1880 1850-1990	200KHz	-141@3MHz	GMSK	Z-IF L-IF
UMTS	FDD-TX TDD	1920-1980 1900-2025	5MHz	-120@3MHz -145@20MHz	QPSK	Z-IF
WLAN 802.11	a b g	5015-5850 2400-2484 2400-2484	16.6MHz 14MHz 14MHz	-102@1MHz	QPSK/QAM	Z-IF/L-IF Z-IF Z-IF

TABLE II
FREQUENCY PLANNING



where TX and RX are active at the same time, only the TX band will be covered by the LO.

Frequency planning and optimization is necessary to enable proper interoperability between such heterogeneous standards. The first obvious optimization constraints are the phase noise and the tuning range, summarized in Table I. In addition, the cost in terms of power consumption, area, and complexity of the final multi-standard system should be optimized to a minimum level. This objective can be achieved only if the standards share a maximum of functionalities and components inside the carrier generation system. The final constraint that should be introduced is a precise generation of the quadrature I/Q signals for each standard. In fact, since Zero-IF and/or Low-IF architectures are considered as the optimal choices, quadrature paths are necessary for the complex processing. The quadrature signals can be generated directly by a quadrature VCO (QVCO), by a polyphase filter or by a frequency divider circuit (prescaler).

The prescaler is the most optimal choice for low power and high precision, even if this solution requires a higher VCO frequency (two times the frequency of the I/Q signals). In fact, doubling the VCO frequency is also an advantage since it helps to avoid frequency pulling and pushing, and decrease the self-mixing and DC-offset phenomena. In the case of the QVCO solution, the major drawback is the cost in terms of area and power consumption. QVCO is constituted by cross coupling two differential VCOs, thus doubling the required area. Its power dissipation is also, in general, huge compared to a single-stage oscillator. Similar weaknesses characterize the polyphase filter solution. In fact, since the topology is based on the classical *RC-RC* phase-shifter network, the quadrature shift precision is strongly dependent on the process variation and mismatches. On the other hand, the order of the polyphase filter should be increased to broaden the frequency band where the quadrature shift is achieved. Increasing the number of stages increases the resistive loss and thus requires more buffering and more power consumption. For wideband applications, such as 802.11.a where the quadrature generation should be ensured over more than 800 MHz, the power consumption of the polyphase filters can become prohibitive [9].

From this preliminary analysis, the ideal solution would use only one wideband VCO and employ frequency dividers to cover the desired standards as well as to generate the precise

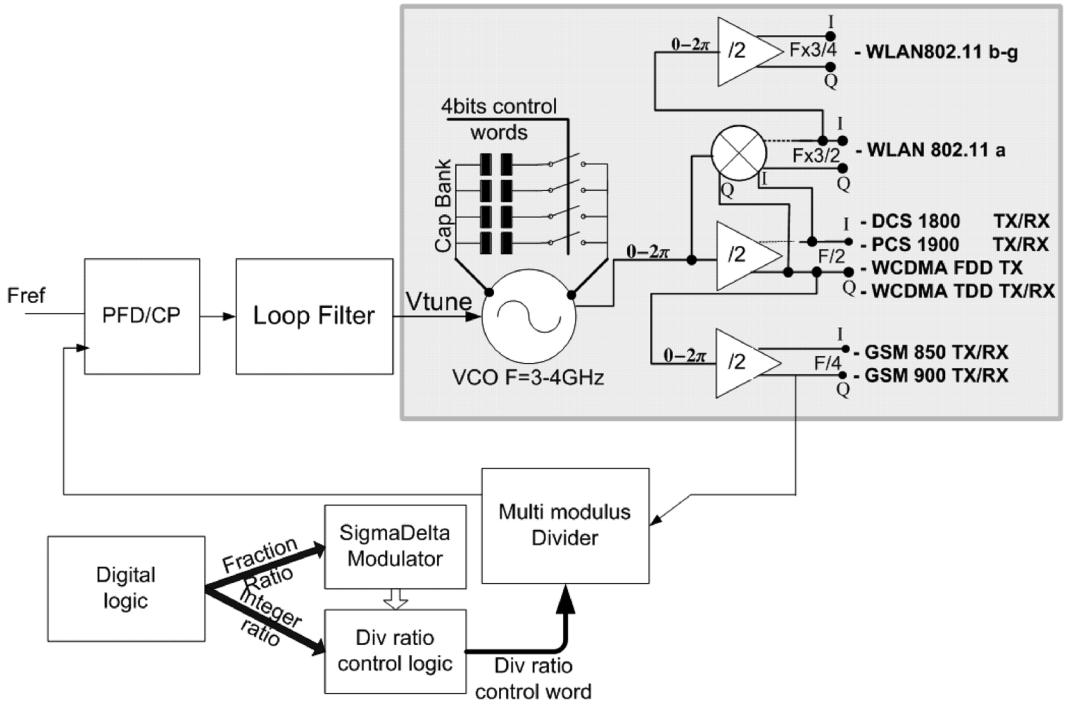


Fig. 1. Multi-mode frequency synthesizer architecture.

quadrature I and Q signals. This approach, however, is only possible if we can design a VCO covering a frequency band from 824 MHz $\times$ 8 (i.e., 6.5 GHz) to 5850 MHz $\times$ 2 (i.e., 11.7 GHz) (see Table I). We should add to this tuning range a margin of at least $\pm 10\%$ to cover the process and temperature variation. Moreover, this VCO should fulfill the most challenging phase noise specification imposed by the GSM standards. Obviously, an on-chip VCO with such tuning range and fulfilling the stringent GSM phase noise specifications is practically impossible to design.

The alternative solution developed to meet these requirements, without leading to an unrealistic design, is shown in Table II. As illustrated in the table, only a VCO with a frequency tuning of 754 MHz, that is from 3296 MHz (4xGSM850) to 4050 MHz (2xWCDMA-TDD downlink), is necessary to cover the whole of the desired spectrum. This planning has also the advantage of setting the VCO frequencies out of the bands of the standards considered. The silicon implementation of this frequency planning results in a compact and cost-effective carrier generation system as illustrated in the next section. It will enable the generation of a precise quadrature signal for all the standards at a minimum cost, i.e., using neither QVCO nor polyphase filters.

III. Implementation

A. System Topology

The architecture implementing the frequency plan of Table II is illustrated in Fig. 1. The interoperability between such heterogeneous standards will cost only few additional blocks, typically a quadrature balanced mixer and a prescaler for the 802.11a-b-g. GSM, PCS, DCS, and UMTS frequencies are generated by two successive divide-by-2 prescalers. The complexity, cost, and power dissipation will be comparable to a single standard synthesizer. The I and Q signals will be generated by dividers for all the standards considered.

B. VCO Design

The VCO is the most critical block to design in the synthesizer. Several parameters impact the phase noise of the VCO as illustrated by the widely used Leeson formula [10]

$$\mathrm{Ph}(\omega_o) = \frac{2kTR_{eq}F}{A_o^2}\left(\frac{\omega_c}{2Q\omega_o}\right)^2\left(1+\frac{\Delta\omega_{\left(\frac{1}{\omega}\right)^3}}{\omega_o}\right). \quad (1)$$

This equation suggests that the phase noise Ph at a frequency offset ω_o depends on the voltage swing A_o, the oscillation frequency ω_c, the tank impedance at the resonance r_{eq}, the quality factor of the tank Q, the excess noise factor F. $\Delta\omega^3_{(1/\omega)}$ is the frequency of the corner between the $(1/\omega)^3$ and $(1/\omega)^2$ regions in the Ph noise spectrum. The GSM mode requires a phase noise significantly low compared to the other standards. The worst condition is set by the -23 dBm@3 MHz blocker in e-GSM RX and gives a phase noise limit of -141 dBc/Hz@3 MHz [6]. The first intuitive way to achieve this noise level is to increase the oscillation swing A_o [see (1)] and so to increase the VCO power consumption. This solution, however, leads to a significant waste of power when the VCO works for the standards that tolerate a higher noise such as WLAN and UMTS. Therefore, a particular effort should be made to design a reconfigurable multi-mode VCO with not only a high tuning range but also good phase-noise performances and low power dissipation.

The optimization process of the tradeoffs between tuning range, phase noise, and power consumption has lead to the hybrid MOS-BJT topology shown in Fig. 2. To form the negative resistance, the complementary cross-coupled nMOS–pMOS

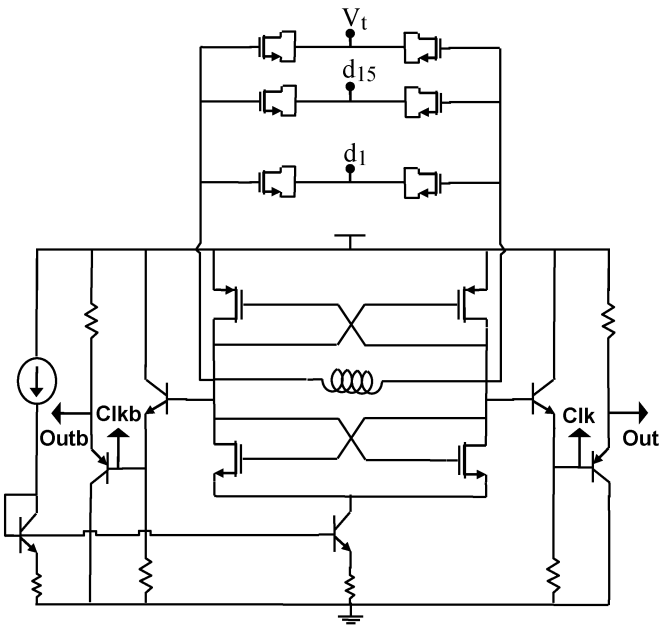


Fig. 2. VCO and buffers schematic.

structure was preferred to a BJT implementation. In fact, even if the BJT has a higher g_m per unit current and lower flicker noise corner than CMOS transistors, the finite base resistance r_b severely limits the maximum attainable oscillation frequency for a given power budget [11]. At high frequency, the impedance corresponding to the base-emitter capacitance C_{be} becomes comparable to r_b, decreasing the portion of the base voltage that will appear across C_{be} and thus degrading the negative resistance of the BJT pair.

Another major drawback in BJT-VCOs is the fact that the DC value of their output signal is close to $V_{\rm dd}$. This specification limits seriously the tuning range of the VCO. In fact, the middle of the tuning range of practically all the varactors (nMOS, pMOS, or PN diode) is reached when the tuning voltage is close to the VCO DC value by typically ± 0.5 V. The varactors can be AC-coupled to the tank via MIM capacitors and their gates biased at $V_{\rm dd}/2$ to avoid this problem. However, the cost of this solution in terms of area and parasitic capacitance becomes prohibitive when a switched-varactors network is used for digital tuning.

In the case of the MOS-based VCO, the gate resistance can be significantly reduced by using a multiple-finger layout, preserving a low negative resistance at high frequency. Moreover, in the complementary nMOS–pMOS configuration of Fig. 2, the current is used twice for amplification [12] and the DC value of the output signal can easily be tuned to $V_{\rm dd}/2$. This structure is thus particularly suitable to achieve low power, low noise, and high tuning range design.

The cross coupled pairs of the VCO act as a mixer and down-converts the low-frequency noise and flicker noise of the active parts near the carrier, leading mainly to AM noise [13]. This noise is amplified by the positive feedback, shaped by the tank and finally translated to phase noise by AM–PM conversion. The tail current is generally considered as the most significant source of flicker noise in differential *LC* VCOs [14]. This is why the low flicker noise BJT was preferred to the noisy MOS transistor in the current-mirror implementation (Fig. 2). A configuration with a 4-bit switched-capacitor network for coarse tuning followed by a small varactor for fine tuning was preferred to a single large varactor. Large varactors are characterized by a steep and nonlinear $C(V)$ characteristic and so increase the harmonic distortion of the signal and the AM–PM noise conversion [14]. The gate overdrive $(V_{gs} - V_t)$ as well as the transistor cut-off frequencies (f_t) was maximized to increase the linearity of the MOS differential pairs. As illustrated by (2) and (3), the optimal choice to minimize the distortion and so the AM–PM noise conversion will be the lowest transistor widths. At the same time, these widths should be large enough to assure a sufficient g_m margin to ensure the oscillation. The current is preferably fixed at the edge of the current-limited regime [15] to guarantee a maximum voltage swing without an excessive waste of power.

$$f_t = \frac{g_m}{C_{gs}} = \frac{\sqrt{2I_D \mu C_{ox} \frac{W}{L}}}{C_{gs}} \alpha\, 1/\sqrt{W} \tag{2}$$

$$V_{gs} - V_t = \sqrt{\frac{I_D L}{\mu C_{ox} W}} \alpha\, 1/\sqrt{W} \tag{3}$$

The buffers used to drive prescaler and to drive output amplifiers, package, PCB parasitics, bias tees and spectrum analyzer are shown in Fig. 2. NPN and PNP BJT emitter-follower topologies were used due to their high input impedance and wide bandwidth. These buffers enable a transfer of the VCO signal to the prescaler without any attenuation.

C. Prescaler and Mixer

The prescaler schematic is illustrated in Fig. 3. A high-speed topology similar to the standard master/slave ECL D-flip-flop but without current sources was used. Removing the current sources increases the maximum toggle frequency and reduces power consumption [16]. However, omitting the current source implies that, in order to drive the input transistors sufficiently into and out of saturation, the input signal swing must be large enough. This condition is satisfied thanks to the buffers (Fig. 2) and the output swing of the VCO which was originally maximized for low phase noise.

To generate the quadrature WLAN carriers, the output differential signals I and Q of the prescaler are mixed with the VCO outputs using the Gilbert-type circuit (Fig. 4). This method has the advantage of requiring only a quadrature mixer and no QVCO, saving in this way significant area and power. The quadrature mixer is designed to consume only 2x1.4 mA@ 2.5 V and the single-stage VCO 2.5 mA@2.5 V. Obviously, this advantage is realized at the cost of a strong sideband at the half of the VCO frequency that is between 1.5 and 2 GHz. Therefore, an image reject filter in RX and TX paths in conjunction preferably with an *LC* filter at the WLAN output of the LO will be necessary to overcome image problem and spurious emission. The fact that the spurs are situated far—more than 3 GHz—from the desired 5 GHz signals makes the integration of such filters much easier [17], [18].

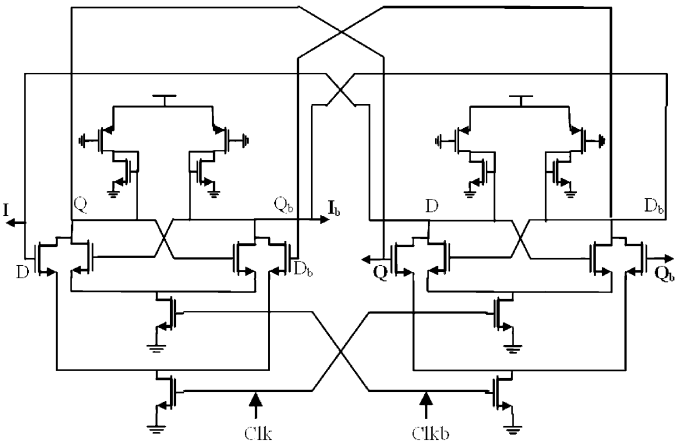


Fig. 3. High-frequency prescaler.

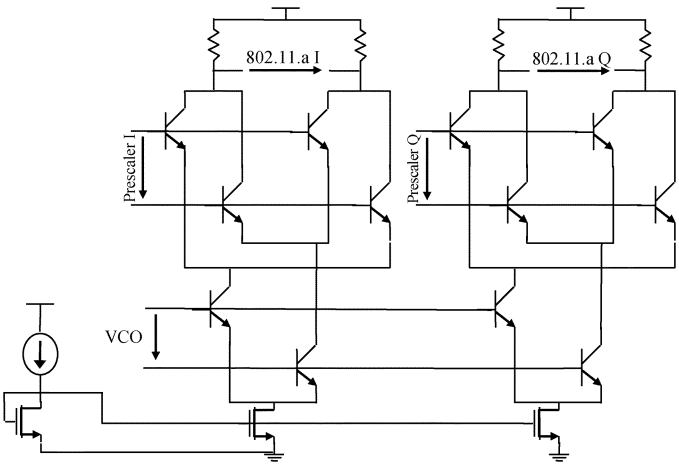


Fig. 4. Quadrature balanced mixer schematic.

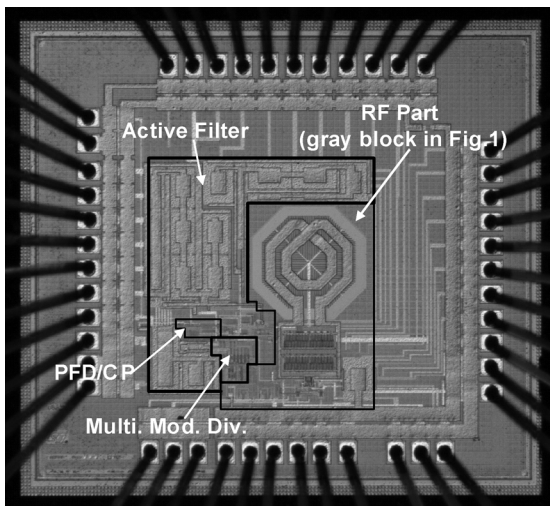


Fig. 5. Microphotograph of the manufactured synthesizer.

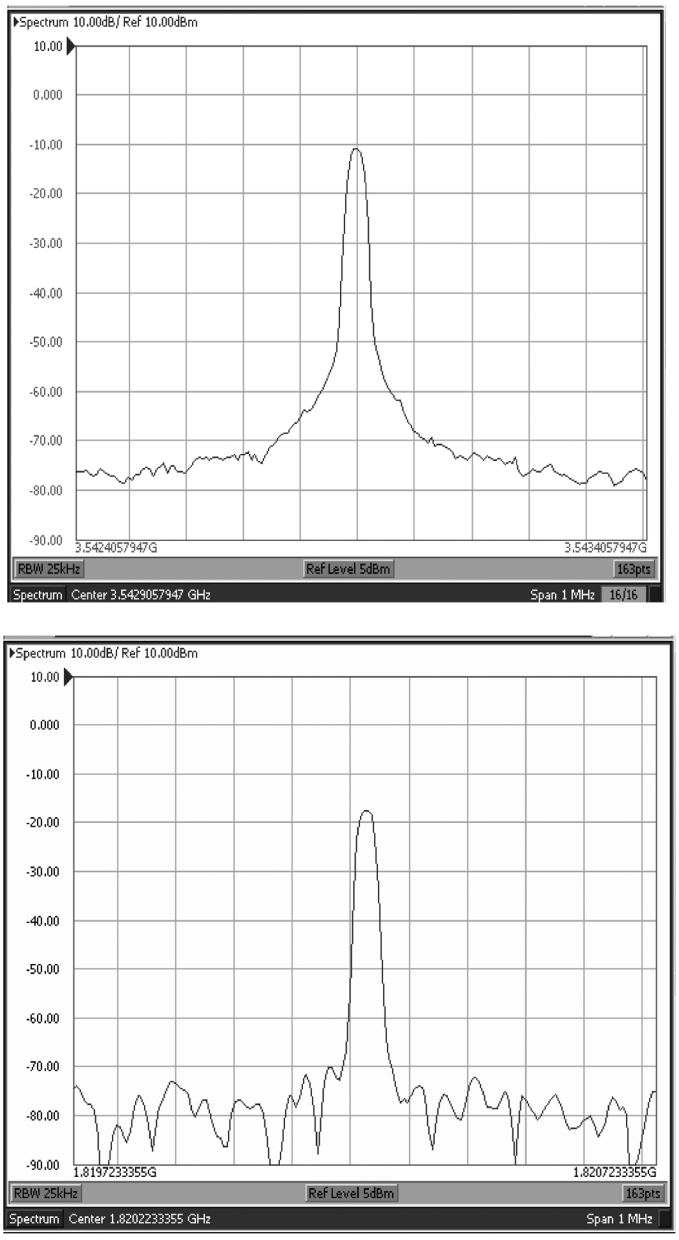


Fig. 6. Typical spectrums at the output of the VCO and the prescaler (span 1 MHz).

An alternative would be the implementation of a QVCO with four mixers to realize an effective single side band up-conversion. This solution comes however at the cost of double the VCO area. In addition, the current consumption of QVCO is in general very high compared to a single VCO (well more than the double) [19]. Several solutions were proposed in de literature to improve these drawbacks. However, the power consumptions generally reported are typically higher than 22 mW. These weakness are illustrated by the figure-of-merit (FOM) comparison studies reported in [20]–[22]. In fact, the switching operation of the transistors that couple the two single-stage VCO blocks up-converts severely the 1/f noise, leading to serious phase noise degradation. Higher current is thus necessary to compensate this side effect. In addition, the size of these transistors should be significantly high to attenuate parasitic mismatches and to save phase accuracy. This condition leads to a higher parasitic capacitance, lower tuning range, lower voltage swing, worse phase noise, and higher power consumption. Therefore, in the actual state of the art, the QVCO seems unsuitable for the considered multi-mode system where stringent phase noise, high tuning range, and low power consumption are required.

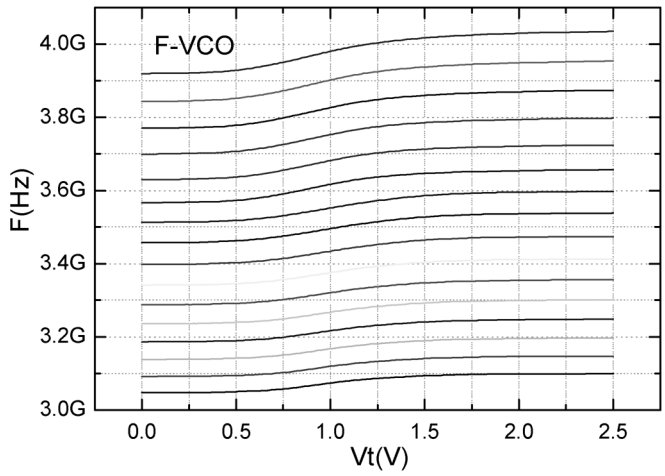


Fig. 7. Measured frequency versus tuning voltage of the VCO, for various digital controls.

IV. Experimental Results

The multi-mode frequency synthesizer was fabricated in a 0.25-μm BiCMOS-SiGe technology. The microphotograph of the chip is illustrated in Fig. 5. The die area of the prototype measures 1.7 mm×1.5 mm. To be conservative and to ensure the success of this first silicon implementation, the carrier generation system (dark gray block in Fig. 1) was designed to enable three working configurations: free running configuration; under the control of an on-chip phase-locked loop (PLL) with an active filter; and under the control of an off-chip PLL with a passive filter. As shown in Fig. 5, the on-chip PLL includes a multi-modulus divider (continuous division range from 64 to 127), phase frequency detector (PFD), charge pump, and active loop filter.

Typical power spectrums measured at the output of the VCO (in free running) and at the output of the first prescaler are shown in Fig. 6 with a span of 1 MHz. The VCO tuning approach consists in breaking the wide range tuning curve into 16 (4 bits) narrower-range sections. A 4-bit digital calibration of a switched-capacitor array (SCA) is used to choose the appropriate narrow-range section before starting the fine frequency tuning over this curve.

The first measurements show that the VCO starts to oscillate with a current as low as 1.3 mA under 2.5 V. The power consumption of the high-frequency prescalers including the buffers is only 1 mA@2.5 V. This value excludes the consumption of the buffers dedicated to the measurements [i.e., the buffers driving the printed circuit board (PCB) parasitic elements, bias tees, and the spectrum analyzer].

Fig. 7 shows the measured frequency versus continuous tuning voltage and digital words controlling the SCA. The frequency variation corresponds to a tuning range of about 1 GHz. The minimum frequency is about 3.05 GHz (0000 SCA digital input) and the maximum frequency is about 4.05 GHz (1111 SCA digital input). This tuning range covers the desired 754 MHz spectrum of Table II with a comfortable margin (250 MHz). We can see in Fig. 7 that the overlaps are sufficient to continuously cover the frequency spectrum. In general, process variations and mismatch inside the SCA can result in significant spectrum discontinuities, especially between the digital words using different SCA units such as 0111 and 1000. To avoid this problem, a thermo encoder switching the SCA units one by one is used. Fig. 8 shows the measured frequency characteristics at the output of the first prescaler (F/2) and second prescaler (F/4). The frequencies after mixing the output of the VCO and the output of the first prescaler (F3/2) and the frequencies at the output of the third prescaler (F3/4) are also illustrated in Fig. 8. As expected, the spectrums of the considered standards are covered with a sufficient margin to compensate temperature and process variations.

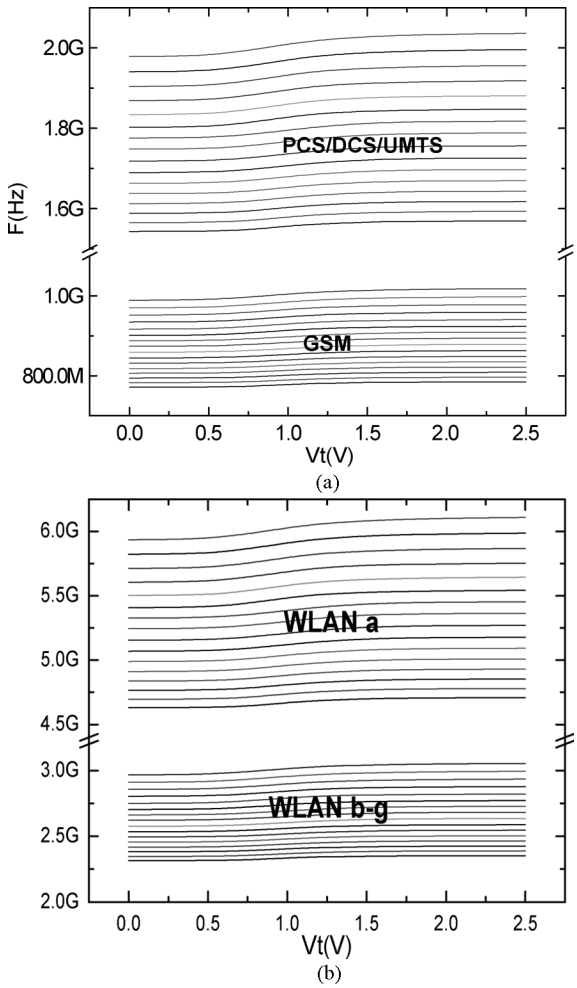


Fig. 8. (a) Measured frequencies at the output of the first and the second prescaler. (b) Frequencies after mixing (F3/2) and dividing (F3/4) operations.

Fig. 9 shows the phase noise measured at the output of the VCO around the middle of its frequency range (SCA digital input = 1000, $V_{\rm tune}$ ∼1.163 V and $F = 3.51$ GHz) and for power dissipation of 6 mW (2.5 mA@2.5 V). Table III shows in more detail the variation of the measured phase noise with the VCO dissipation at various offsets. The phase noise measured at the output of the first and the second prescaler is, as expected, lower by about 6 and 12 dBc/Hz, respectively, than the phase noise measured at the output of the VCO.

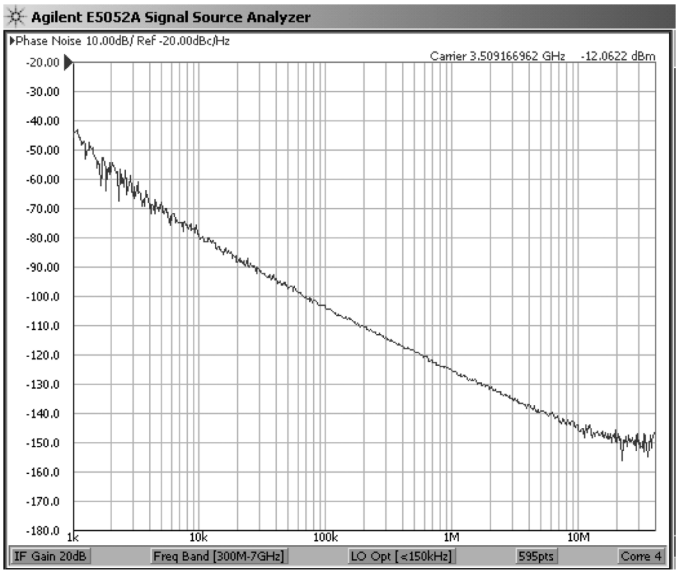


Fig. 9. VCO phase noise with $V_t = 1.163\,\mathrm{V}$ and digital control $= 1000$.

TABLE III
MEASURED PHASE NOISE VERSUS VCO CONSUMPTION

Frequency Offset	2.5mA@2.5V	1.7mA@2.5V
100 KHz	-104 dBc/Hz	-100 dBc/Hz
400 KHz	-118 dBc/Hz	-113 dBc/Hz
1MHz	-125 dBc/Hz	-119.5 dBc/Hz
3MHz	-135 dBc/Hz	-129 dBc/Hz
10MHz	-145 dBc/Hz	-139.5 dBc/Hz

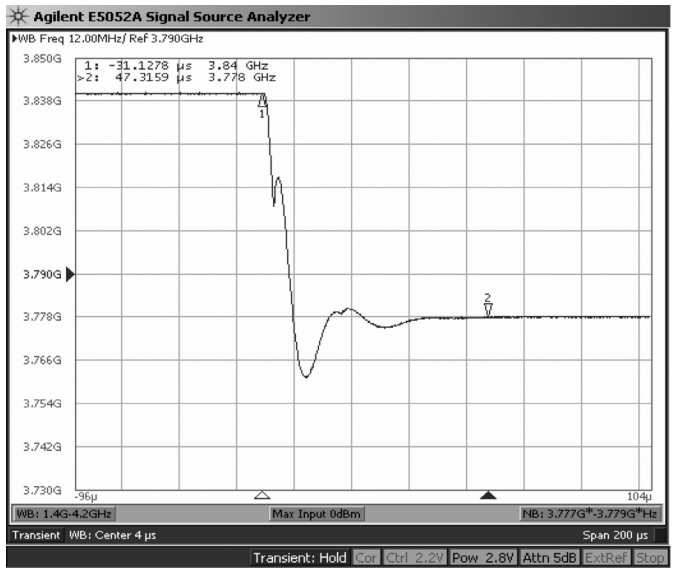
TABLE IV
COMPARISON OF THE NORMALIZED FOM

Freq(GHz)	Power (mW)	Pn(dBc/Hz)	NFOM	Ref
5.3	13.5	-124	-187.1	[13]
4.4	21.6	-119	-178.5	[23]
5.5	5	-116	-183.8	[24]
5.6	2	-114.6	-186.6	[25]
5.8	8.1	-110	-176.2	[26]
4.39	3.5	-117.8	-179	[27]
5	3	-120.42	-189.6	[28]
4	6	-124	-189.25	This Work

Table IV shows a comparative study between the designed VCO and the recently published ones by using the widely used normalized FOM [29]:

$$\begin{aligned}\mathrm{FOM} &= \mathrm{Ph}(1\ \mathrm{MHz}) - 20\log(\omega_c/\Delta\omega) + 10\log(P_{dis}/1\ \mathrm{mW}) \\ &= -189.25\ \mathrm{dBc/Hz/mW}. \end{aligned} \quad (4)$$

The calculated FOM for our VCO from the measured data is −189.25 dBc/Hz/mW. Among the circuits that have been compared, this VCO exhibits one of the best FOMs, confirming the excellent phase noise/power consumption tradeoffs achieved. Moreover, this figure is realized without sacrificing the tuning range (around 30% of the center frequency).



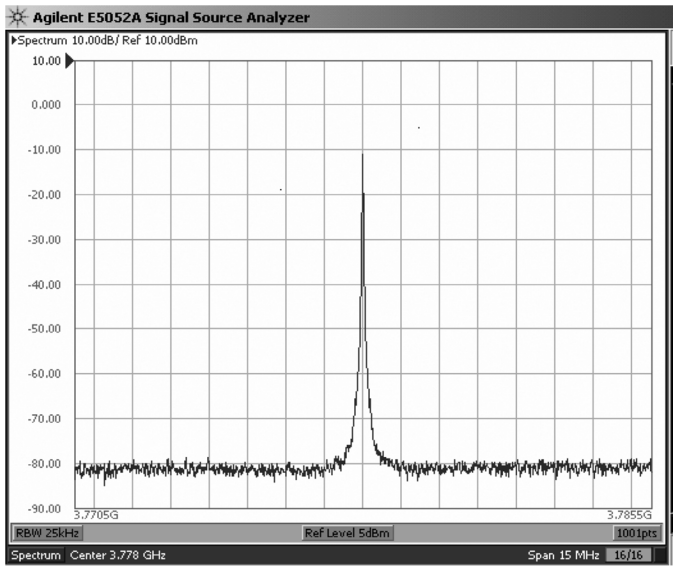


Fig. 10. Typical settling time and spectrum of the synthesizer.

An additional set of measurements of the carrier generation system under a PLL control were achieved. The prototype with the off-chip PLL enables the optimization of the passive filter; its performances are thus higher compared to the fully integrated version. Fig. 10 illustrates a typical measured settling time during the fine tuning with an SCA digital word of 1101. The bandwidth of the PLL is 20 kHz, the reference frequency is supplied by a 16.38 MHz crystal oscillator, and the passive filter is a second-order type with $r_z = 330\ \Omega$, $C_z = 56$ nF, and $C_p = 12$ nF. In this configuration, the PLL is locked from 3.84 to 3.778 GHz within 1 kHz tolerance in 80 μs. Fig. 10 shows also the measured spectrum of the PLL after locking (span 15 MHz). The measured phase noise of the frequency synthesizer after the fine tuning is illustrated in Fig. 11.

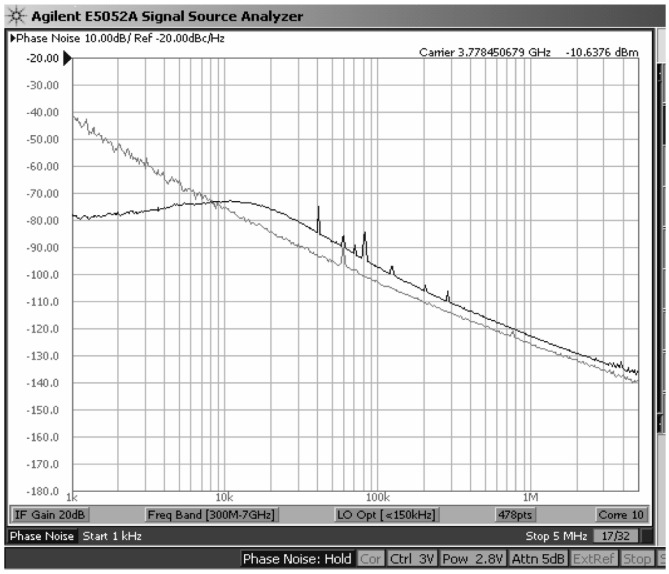


Fig. 11. Phase noise of the VCO in free running and under the PLL control.

V. Conclusion

A compact and cost-effective frequency synthesizer architecture enabling the convergence of such heterogeneous standards as quad-band GSM (GSM 850, GSM 900, DCS1800 PCS 1900), WCDMA (FDD and TDD), and WLAN (802.11a/b/g) in the same terminal has been developed. The design and manufacturing has been achieved with 0.25-μm BiCMOS SiGe process. The experimental results show that the tuning range is about 1 GHz (3.05–4.05 GHz) exceeding the specification by 25% (Table I). A hybrid nMOS–pMOS–Bipolar VCO topology representing an optimal tradeoff between phase noise, power consumption, tuning range, and sensitivity to noise has been presented. This VCO exhibits a phase noise of -125 dBc/Hz measured at 1 MHz offset while drawing only 2.5 mA from 2.5 V supply. The measured phase noise at 400 kHz offset of the PCS/DCS signal (output of the first prescaler) and the GSM signal (output the second prescaler) is, respectively, -124 dBc/Hz and -130 dBc/Hz. The circuit exhibits an FOM of -189.25 dBc/Hz/mW, confirming the excellent phase noise/power consumption tradeoffs achieved.

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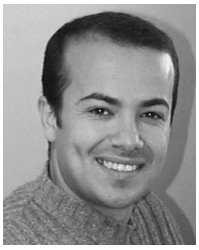

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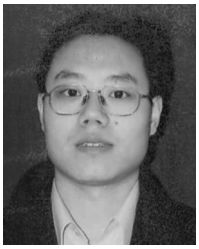

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