Reactive Power Imbalances in *LC* VCOs and Their Influence on Phase-Noise Mechanisms

Adil Koukab, *Member, IEEE*

***Abstract*—Phase-noise mechanisms in cross-coupled *LC* voltage-controlled oscillators (VCOs) are reviewed based on a physical understanding of reactive power imbalances in the tank and in the active part. These phenomena are proven to be the predominant phase-noise degradation mechanism in relatively low- and high-current operations. Based on this analysis, a technique to suppress these detrimental effects is developed and implemented in an *LC* VCO design. The measured results confirm the dependencies predicted by the analysis, and the usefulness of the proposed technique to simultaneously optimize the phase noise at high and low offset frequencies. The measured VCO tuning range is 600 MHz, ranging from 2.4 to 3 GHz. The VCO-prescaler circuit exhibits a phase noise from −88 to −92 dBc/Hz at 15 kHz and from −155 to −160 dBc/Hz at 10 MHz, when the power consumption is 6 and 10 mA for the VCO and 2 mA for the prescaler, and the power supply is 2 V.**

***Index Terms*—Flicker noise, phase noise, power supply rejection (PSR), thermal noise, voltage-controlled oscillator (VCO).**

I. Introduction

THE voltage-controlled oscillator (VCO) is an important RF building block of a transceiver, and its specifications directly impact key system performances such as bit error rate (BER), error vector magnitude (EVM), and sensitivity. This role is even more crucial in emerging broadband technologies, where unprecedented and stringent constraints on frequency precision, near carrier phase noise, and quadrature I-Q mismatch are imposed. For instance, in long-term evolution (LTE), the targeted standard in this design, up to 1024 sub-carriers with narrow bands of 15 kHz are spread over a 1.5–20-MHz scalable bandwidth to generate the orthogonal frequency-division multiple access (OFDMA) signals. Phase noise at low-frequency offsets makes the sub-carriers wider than the actual 15 kHz. Thus, adjacent carriers can spread over each other, resulting in inter-carrier interference [1]. Moreover, in order to limit the out-of-band noise, stringent high-frequency offset phase noise is also required [2].

In this context, improving the performance of VCOs, quadrature VCOs, and prescalers is still a topic that motivates significant research activities. Due to their exceptional noise performance, cross-coupled *LC* VCOs have become the most widely used topologies in RF design. In order to analyze and compare the noise properties of these topologies, the linear time-varying (LTV) model is usually used [3]. For instance, the application of the LTV model to an oscillator where the noise sources are mainly active at the minimum or maximum output voltage results only in amplitude perturbations, and thus, in superior phase-noise performances [4]. This analysis is appropriate for high-frequency thermal noise. For low-frequency noise, the negative and positive frequency parts of the spectrum are correlated, which results only in AM, whatever the oscillator topology or the noise source is [5]. On the other hand, in CMOS VCOs, high-frequency thermal noise is usually less critical than low-frequency flicker noise and it can be easily filtered out. For the bias noise, which is usually identified as the dominant noise contributor in a VCO, high-frequency noise can be filtered out using a simple decoupling capacitor in parallel with the current mirror. Therefore, in spite of their importance, the mechanisms of flicker noise up-conversion are still not fully understood.

A complementary analysis of the phase-noise mechanisms in *LC* VCOs is proposed in this paper. The analysis is developed for classical cross coupled topology, but can be applied also to the other types of CMOS VCOs, such as Colpitts, Hartley, or dual-G_m VCO [4], [6]. It highlights the detrimental role of reactive power in the active part of the VCO. This effect is exacerbated in relatively low- and high-current operations. More specifically, it results in a severe tradeoff between the optimization of the phase noise at the low offset frequencies and high-offset frequencies. The effect of the second (HD2) and third current harmonic (HD3) on the phase noise is also clarified. Based on this analysis, a technique is developed to compensate the reactive parasitics of the switching pair, and thus, to limit their detrimental effect. A VCO topology is proposed that optimizes the phase noise at low- and high-offset frequencies in order to simultaneously avoid inter-sub-carrier interference [1] and ensure a negligible out-of-band radiation.

This paper is organized as follows. In Sections II and III, phase-noise mechanisms in differential cross-coupled VCOs are reviewed and the detrimental effects of reactive power imbalances in the tank and the active part are clarified. An enhanced VCO topology enabling the suppression of these detrimental effects is presented in Section IV. The experimental results are then illustrated in Section IV.

II. Frequency Conversion of the Noise in *LC* VCO

There are many sources of noise in a VCO. The noise of each source is generated at different frequencies, and thus, can affect the carrier directly or after up or down conversion. The conversion is made by switching activity of the cross-coupled transistors [5] and by the nonlinear varactors [7]. This complexity

Manuscript received February 28, 2011; revised August 19, 2011; accepted August 29, 2011. Date of publication October 24, 2011; date of current version December 14, 2011.

The author is with the Swiss Federal Institute of Technology Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: adil.koukab@epfl.ch).

Digital Object Identifier 10.1109/TMTT.2011.2169496

makes it difficult to discern which mechanism impacts the phase noise and which one is dominant. Such information is crucial for optimizing the topology of the VCO. To deal with this difficulty, a methodology based on a step-by-step topology evolution, in conjunction with comparative analysis, is used. Our analysis starts with the VCO1 shown in Fig. 1. This classical cross-coupled VCO is designed with nonvariable capacitors in the first stage. Varactors are intentionally avoided in order to simplify the comparisons and focus on the noise contribution and optimization of the active parts of the VCO. The varactors can be optimized in a second stage, by decreasing their sizes, and thus, their sensitivity. Afterwards, a digitally controlled bank of capacitors, and if necessary, a set of dividers and mixers [8], can be added to meet the tuning range specification. The equivalent parallel resistance, representing the loss in the tank, is shown in the figure.

Referring to VCO1 in Fig. 1, the main sources of noise are the cross-coupled transistors and the tail current mirror. At low frequency, the switching transistors see low impedance $(L\omega)$ at their drain terminals. Approximating this impedance as a short circuit, we can redraw their low-frequency current noise in parallel with the mirror transistor (M_{C2}). Consequently, low-frequency thermal and flicker noise of switching transistors is up-converted via the same phenomena that up-converts low-frequency bias noise. This is why we will focus on the tail current noise $i^2_{n,mr}$. $i^2_{n,mr}$ is composed of thermal- and flicker-noise contributions of M_{c1} and M_{c2} and can be described by the following equation:

$$\overline{i^2_{n,mr}} = N^2 g^2_{m1}\left(\left(4kT\Gamma g_{m1} + \frac{K_f}{f}\frac{g^2_{m1}}{WLC^2_{\text{ox}}}\right)\left(\frac{1}{g_{m1}}\right)^2\right) + \left(4kT\Gamma N g_{m1} + \frac{K_f}{f}\frac{(Ng_{m1})^2}{NWLC^2_{\text{ox}}}\right) \quad (1)$$

where g_{m1} and $N \cdot g_{m1}$ are the transconductances of M_{c1} and M_{c2}. The current ratio N between the oscillator and bias circuits has a significant impact on the value of $i^2_{n,mr}$. The optimal choice for N, in order to minimize the noise, is around 1 [9]. In this case, however, only half of the current is used for oscillation and the other half is wasted in the bias circuit. To save power, a value of 5 is chosen for VCO1 (Fig. 1), and thus, only 1/6 of the total current is consumed by the bias circuit.

The process by which the tail current noise is shaped and converted in frequency is detailed in Fig. 2. First we represent the noise per unit bandwidth as a sinusoid (e.g., $i_{n,mr}(t)$ in Fig. 2) with the same average power. For clarity, we have supposed that the frequency of the RF signal is only ten times the frequency of the injected noise. The spectrum of the low-frequency noise, as well as the filtering action of the decoupling capacitor (Cc in Fig. 1), are illustrated in the same figure. Since the noise sidebands at ω_n and $-\omega_n$ are correlated, they will result only in an amplitude modulation [5].

After the switching action of the cross-coupled pair, the noise signal $(i_{n,mr}(t))$ of Fig. 2(a) is transformed in $(i_{n,mr}(t))_p$ of Fig. 2(b). As illustrated, the noise signal is not modulated as usually stated in the literature, but sampled by a square

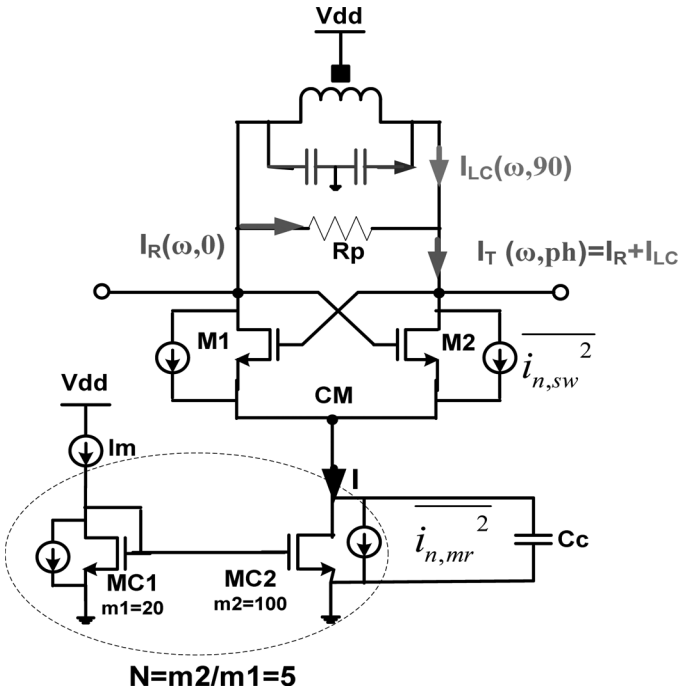

Fig. 1. Conventional cross-coupled VCO (VCO1).

signal at carrier frequency (ω_c) and with a duty cycle of about 50%. The current noise is thus up-converted to ω_c and their multiple values as usually explained [5], [10]. However by applying fast Fourier transform (FFT) to the time-domain signal $(i_{n,mr}(t))_p$ we can demonstrate that this noise also appears in the baseband. Moreover, this analysis reveals that the spectrum at $2\omega_c$ and beyond is significantly attenuated. The attenuation beyond $2\omega_c$ is due to the fact that the sampling signal has a duty cycle of about 50%. As will be detailed in Section III, the baseband part of the sampled current noise plays a fundamental role in the modulation of the frequency (FM), and thus, in the phase noise.

III. Phase-Noise Generation

A. Frequency Modulation

VCO1 used to study the phase-noise mechanisms is designed with 0.25-μm MOS transistors and 2-V power supply. The switching transistors are sized $(\text{W/L} = 50\ \mu\text{m}/0.35\ \mu\text{m})$ to have a negative g_m with enough margin $(g_m \sim 2/Rp \sim 12\,\text{mS})$ in order to ensure proper startup of the oscillator. The value of the inductor is 0.8 nH and its quality factor at 3 GHz is 15.

In order to gain an insight into how the baseband noise is converted to phase noise, we will first consider the variation of the frequency with the current. The results, illustrated in Fig. 3, show a significant sensitivity of the frequency to current variations. In fact, the analysis of the currents circulation in VCO1 reveals that the current flowing into the inductor is not equal to the one flowing into the capacitor of the tank. The difference is equal to $I_{LC}(\omega, 90)$, as shown in Fig. 1. This current is mainly supplied by the lower capacitive impedance of the tank, and thus, it is shifted by 90°, compared to the fundamental $I_R(\omega, 0)$. In this

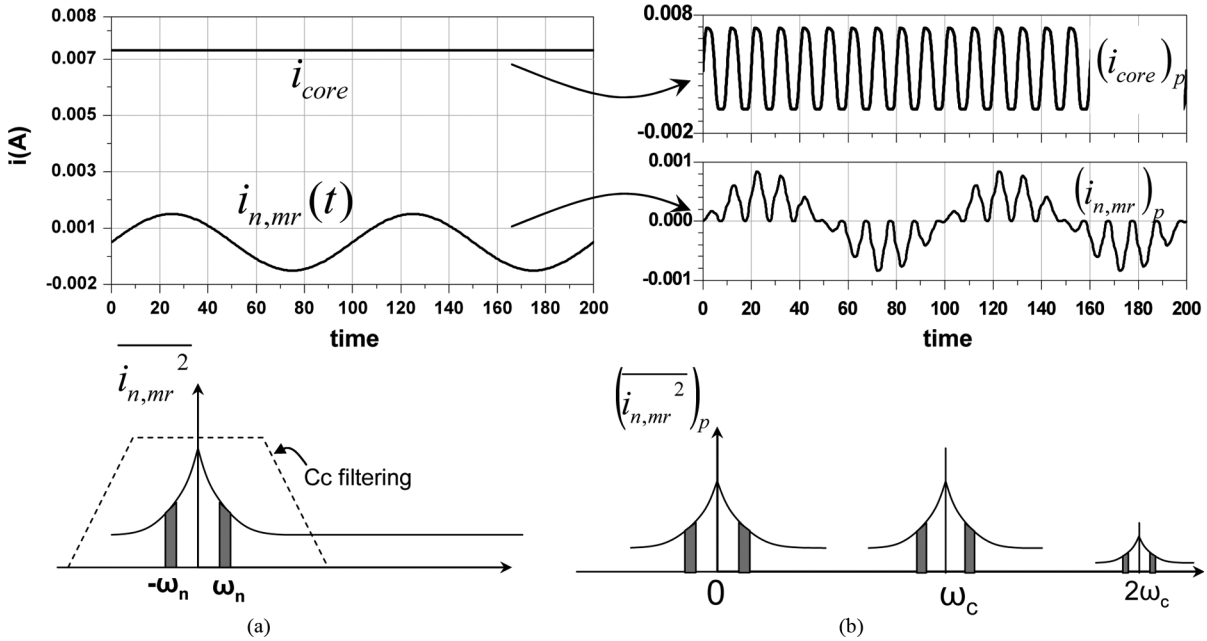

Fig. 2. Sampling and frequency conversion of the bias noise.

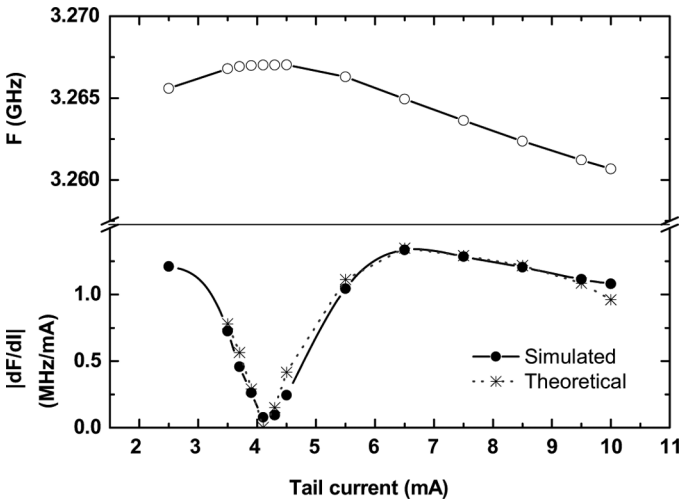

Fig. 3. Frequency and its derivative versus tail current.

case, the frequency ω is no longer equal to $(LC)^{-0.5}$, but given by the following equations:

$$\frac{|Vo^+(\omega)|}{L\omega} - \left|Vo^+(\omega)\right| \cdot C\omega = |I_{LC}(\omega)| \tag{2}$$

$$\omega_{th} = \frac{-|A| + \sqrt{|A|^2 + 4\frac{C}{4}}}{2C}, \qquad \text{with } A = \frac{I_{LC}(\omega)}{V_o^+(\omega)}. \tag{3}$$

$Vo^+(\omega)$ is the voltage at the output of the VCO. The theoretical frequency sensitivity to current variations (dF/dI) calculated using this equation is in good agreement with the simulation results, as shown in Fig. 3. This sensitivity is significant at low and high current, while it is very small for intermediate currents (around 4–4.5 mA). Consequently, the baseband part of the sampled noise [see Fig. 2(b)] that modulates the current will result in a frequency modulation, and thus, a phase noise with a similar variation. The resulting phase noise can be calculated by applying the following equation to the results of Fig. 3:

$$L(\omega_n) = \frac{1}{2}\left|\frac{\partial\omega}{\partial I}\right|^2 \frac{\overline{i_n^2}(\omega_n)}{(\omega_n)^2}. \tag{4}$$

SpectreRF is used to simulate the phase noise and to confirm this analysis. Fig. 4 shows the phase noise at 15 kHz and at 10 MHz versus current. At 15 kHz, the bias transistors are the major noise contributors (more than 80%). As expected, the phase noise at low offset frequencies (e.g., 15 kHz) is significant at low and high currents and reaches its minimum between 4–4.5 mA. Since the sensitivity of the frequency in this region drops to zero, we can assume that this noise is the minimum noise that we can have if we cancel the frequency modulation. At high frequency offset, the main noise contributor is the high-frequency thermal noise of the switching transistors and the series resistance of the inductor. The high-frequency noises located at $\omega_c - \omega_n$ and at $\omega_c + \omega_n$ are not correlated, and thus, directly generate phase noise, independently of the sensitivity of the frequency to the variation of the current. This is why the phase noise at 10 MHz continues to decrease when the current, and consequently, the voltage amplitude increase, as illustrated in Fig. 4. These curves also illustrate the well-known close-in noise degradation at high currents [11], [12], and thus, the tradeoff between the optimization of the noise at low- and high-frequency offsets.

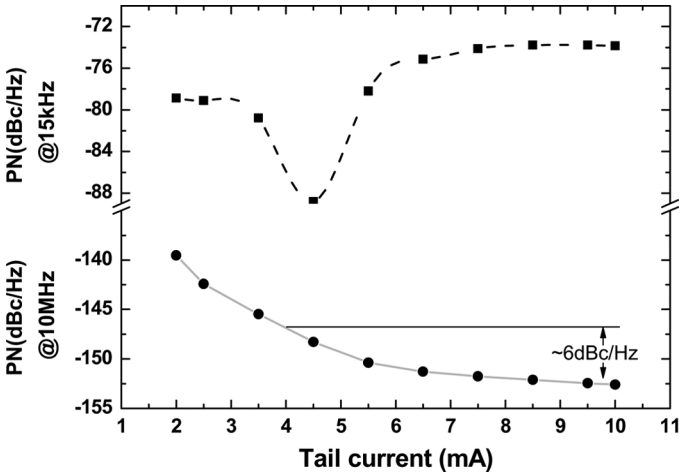

Fig. 4. Phase noise at 15 kHz and 10 MHz versus tail current.

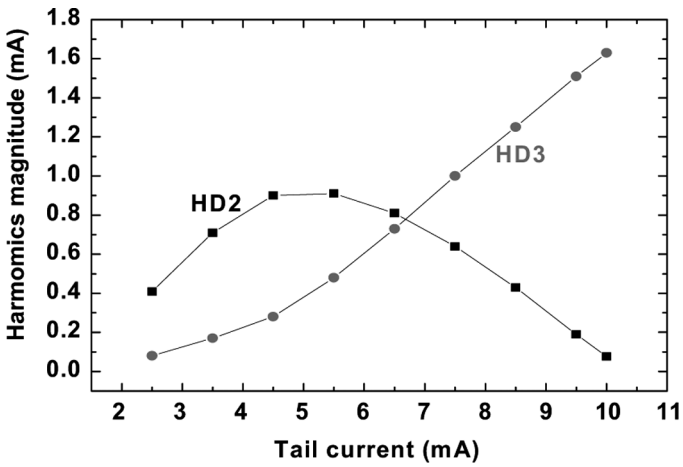

Fig. 5. Second and third harmonics of the current.

B. Reactive Power in the Tank

Since the switching transistors periodically enter the triode region, they generate distorted currents with significant harmonics. This is why the harmonic distortions were usually considered as mainly responsible for the sensitivity of the frequency to the variation of the current. The interdependence between frequency variation and harmonic distortion was first revealed by Groszkowski [13] and reused in [5] and [10] to explain the indirect FM in *LC* VCOs. In fact, the second and third harmonics of the fundamental current (HD2 and HD3) generated by the switching transistors will flow into the lower capacitive impedance of the tank. This will result in an imbalance in reactive power between the inductor and capacitor of the tank. The oscillator compensates for this imbalance by slowing down the frequency until the reactive power in the inductor reaches the level of reactive power in the capacitor.

The variations of HD2 and HD3 versus core current are shown in Fig. 5. Below 4.5 mA, both HD2 and HD3 increase with the current and flow into the lower capacitive impedance of the tank. Consequently, the reactive power in the capacitor of the tank increases compared to the inductor. The oscillator should compensate for this imbalance by slowing down the frequency until the reactive power in the inductor reaches the level of reactive power in the capacitor. This expected trend is in contradiction with the results of Fig. 3 since the VCO frequency increases with the current below 4.5 mA. This is a first indication that the role of HD2 and HD3 in the indirect FM is negligible for low currents. Beyond 6 mA, the HD2 component starts to vanish while the HD3 becomes dominant. Moreover, the variation of HD3 for high currents matches with the variation of the frequency. Therefore, the impact of HD3 on the frequency sensitivity would be more important. A quantitative estimation of HD2 and HD3 effects will be done in Section III-C.

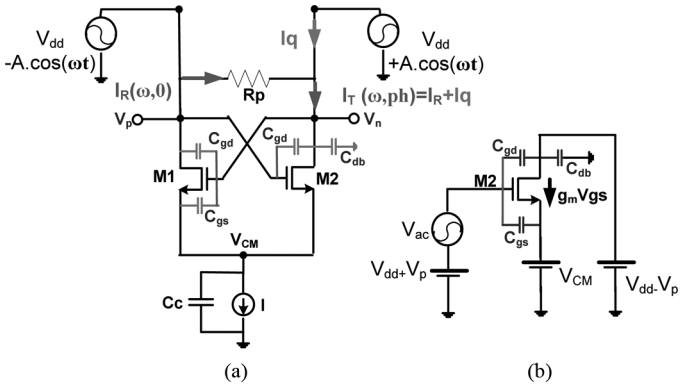

Fig. 6. Test circuits proposed to: (a) discern the reactive power effects in VCO active part and (b) to estimate the variation of their parasitic capacitances.

C. Reactive Power in the Active Part

The reactive power in the active part of the VCO can also make the frequency of the VCO sensitive to current variations. To understand this process, we propose to isolate it and to cancel the effect of the reactive power imbalance in the tank. For this, the test circuit shown in Fig. 6 is proposed.

In this circuit, the *LC* resonator, and thus, its reactive power imbalance effect, are removed and only the active part of the VCO is considered. The circuit is driven by differential voltage sources having exactly the same amplitude and the same dc value as the output signals generated by the VCO (Fig. 1). Ideally, the active part compensates the loss in R_p, and thus, the current I_T flowing into the switching pair should be in-phase and exactly equal to the current I_R. The simulations, however, show a phase shift between I_T and I_R that varies with the tail current. In fact, the MOS transistors exhibits an important reactive part composed of intrinsic and extrinsic parasitics [14]. All these parasitics create a reactive power and result in the phase shift (ph) between $I_T(\omega, \mathrm{ph})$ and $I_R(\omega, 0)$. Consequently, the time-domain signals $I_T(t)$ and $I_R(t)$ cannot be exactly equal. The difference (i.e., I_q) will be supplied by the voltage source in the circuit of Fig. 6. Since I_q is exclusively due to the reactive power in the VCO active part, it will enable to quantify this effect. In contrast, I_{LC} in Fig. 1 is due to both reactive power effects in the tank and in the switching transistors.

Therefore, by simulating I_{LC} and I_q using the schematics of Figs. 1 and 6 and using this values in (3), we can estimate the frequency sensitivities with and without an *LC* reactive power

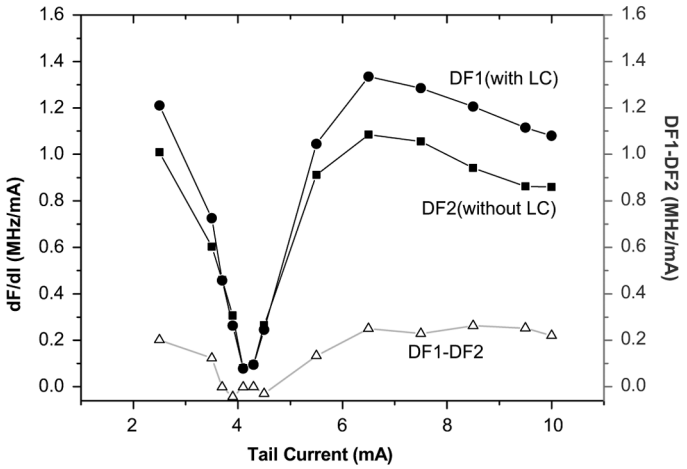

Fig. 7. Simulated frequency sensitivities with and without *LC* reactive power imbalance effect (DF1 and DF2) and the difference (DF1–DF2).

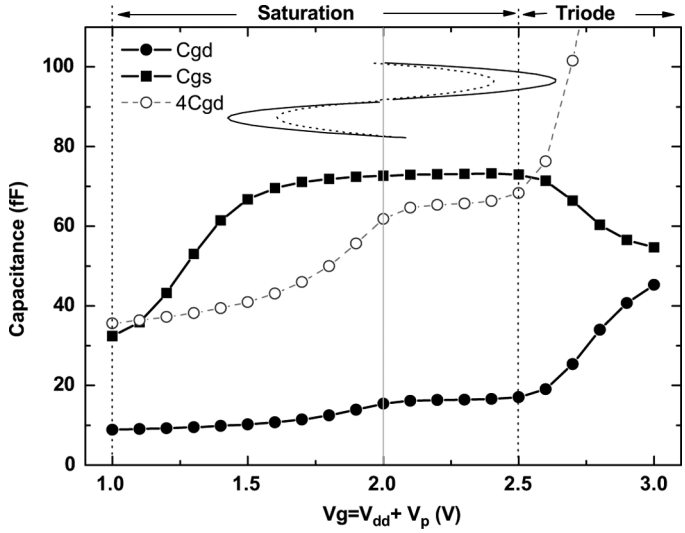

Fig. 8. Variation of the capacitances of the switching transistors simulated using the small-signal analysis of circuit (b) of Fig. 6.

imbalance effect. The results are shown in Fig. 7. As illustrated, the difference between the two curves is smaller than 20% (e.g., at 6.5 mA, DF2 $=$ 1.1 MHz/mA and DF2 $=$ 1.34 MHz/mA). Since the relation between the phase noise and dF/dI is quadratic (4), the difference in terms of phase noise contribution is slightly higher (around 35%). Globally, we can conclude from this analysis that the effect of reactive power in the switching pair is dominant and its contribution to the phase noise is at least two times higher than the contribution of the power imbalance in the tank.

D. Origin of Reactive Power

As illustrated in Fig. 6, the main parasitic capacitances that generate the reactive power of the active part are the gate to drain, gate to source, and drain to bulk capacitances ($C_{\rm gd}$, $C_{\rm gs}$, and $C_{\rm db}$) [14], [16]. Circuit (b) of Fig. 6 is proposed to simulate the variations of these capacitances. The transistor is submitted to the same bias conditions as in the VCO. The gate and drain nodes are submitted $Vdd \pm Vp$ with Vdd equal to 2 V and Vp varying from -1 to 1 V. The small-signal analysis of the drain and source current is used to simulate $C_{\rm gd}$ and $C_{\rm gs}$. The results, shown in Fig. 8, are similar the well-known behavior of the MOS parasitic capacitance in the different modes of operation (i.e., off, saturation, and triode).

At first sight, the value of $C_{\rm gs}$ is much higher than $C_{\rm gd}$ and would dominate the total parasitic capacitance. However, the analysis of the parasitic capacitances inside the VCO [see Fig. 6(a)] reveals that both $C_{\rm gd}$ of M_1 and M_2 contribute to the capacitance seen at the output node V_n (or Vp). In addition, these capacitances are differentially driven by the VCO output signals. In contrast, only the single-ended $C_{\rm gs}$ of M_1 appears at the node V_n. The effective capacitance seen at each output nodes of the VCO is thus $C_{\rm gs} + 4C_{\rm gd}$. The magnitude of $4C_{\rm gd}$ at Vg equal to 2 V is similar to $C_{\rm gs}$. However, its variation is much higher, as illustrated in Fig. 8. In fact, M_1 exhibits a $C_{\rm gd}$ of roughly $WC_{\rm ov}$ in saturation ($C_{\rm ov}$ is the overlap capacitance). When $V_{\rm gd}$ is positive (i.e., $Vg > 2$ V in Fig. 8), the overlap region of the drain is in accumulation and $C_{\rm ov}$ is

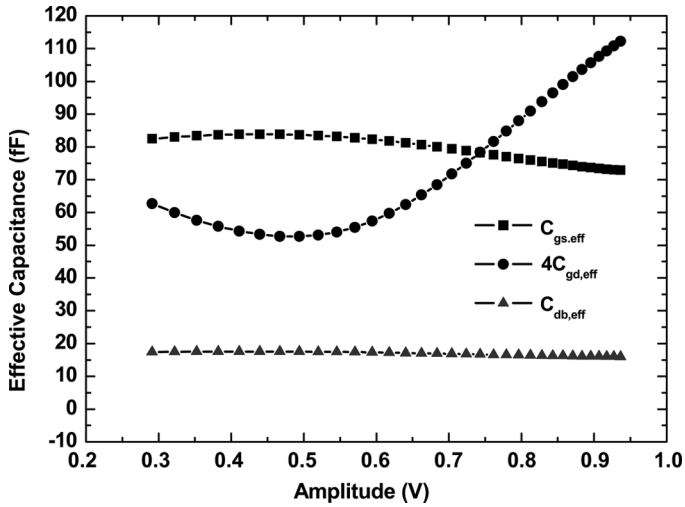

Fig. 9. Variation of the effective capacitance of the switching transistors versus amplitude of the output signal, simulated using the large-signal analysis of circuit (a) of Fig. 6.

at its maximum value. For negative $V_{\rm gd}$, the overlap region of the drain is in depletion and $C_{\rm ov}$ is at its minimum value. This explains the variability of $C_{\rm gd}$ across the saturation mode. In the triode region, $C_{\rm gd}$ and $C_{\rm gs}$ converge toward the same value that is $WLC_{\rm ox}/2$.

The output sinusoidal signal is also shown in Fig. 8. The effective parasitic capacitance seen at the output terminals is the average value of the part of the curves $C_{\rm gs}$ and $4C_{\rm gd}$ covered by the signal. Since the amplitude of this signal increases with the core current, the effective capacitance, as well as the frequency, will change with the current. In the saturation mode, $C_{\rm gs}$ is practically constant, and consequently, the total effective parasitic capacitance variation is governed by the variation of the $4C_{\rm gd}$ curve. More precisely, the average value of $4C_{\rm gd}$ decreases when the amplitude of the signal increases. This explains the frequency growing for small current range (i.e., from 2 to 4.5 mA) illustrated in Fig. 3. When the amplitude of the

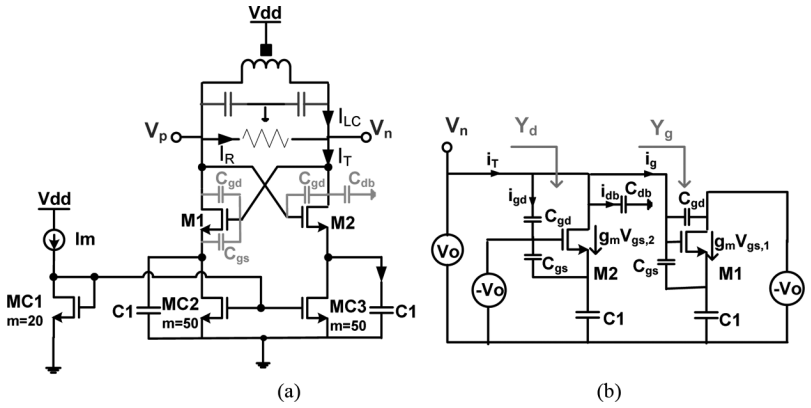

Fig. 10. (a) VCO2 topology with reactive power cancellation technique and (b) its one-port representation.

signal is high enough to push the transistors in the triode region, $C_{\rm gs}$ starts to decreases while $4C_{\rm gd}$ increases abruptly (Fig. 8). Since the $4C_{\rm gd}$ curve increases more quickly, it will dominate the total effective capacitance variation in this mode also. The increase of $4C_{\rm gd}$ will result in a diminution of the frequency for high current range (i.e., beyond 4.5 mA), as shown in Fig. 3.

Effective parasitic capacitances can be determined directly by the large signal analysis of circuit (a) of Fig. 6 and by using the following equations:

$$\frac{|\mathrm{Im}\,[i_{d,2}(\omega)]|}{A} = \omega(2C_{\rm gd,eff} + C_{\rm db,eff}) \tag{5}$$

$$\frac{|\mathrm{Im}\,[i_{g,1}(\omega)]|}{A} = \omega(2C_{\rm gd,eff} + C_{\rm gs,eff}) \tag{6}$$

where $\mathrm{Im}[i_{d,2}]$ and $\mathrm{Im}[i_{g,1}]$ are the imaginary parts of the fundamental harmonic of the drain current of M2 and gate current of M1. A is the amplitude of the output signal. The simulated results of $4C_{\rm gd,eff}$, $C_{\rm gs,eff}$, and $C_{\rm db,eff}$ are shown in Fig. 9. As expected, $C_{\rm db,eff}$ and $C_{\rm gs,eff}$ are practically constant and the total effective capacitance variation is dominated by $4C_{\rm gd,eff}$. The variation of $4C_{\rm gd,eff}$ matches with the variation of the frequency illustrated in Fig. 3.

E. Cancellation of the Reactive Power Effect

As illustrated in previous sections, the reactive power effects in the tank and in the active part of the VCO contribute to the phase noise by making the frequency sensitive to current variations. The variation of the frequency is only possible through the creation of the variable quadratic current I_{LC} at the output of the tank, as shown by (2). A suitable topology to solve this problem should create a negative feedback to counterbalance the current I_{LC}. An example of a topology suitable for this is illustrated by VCO2 in Fig. 10. In this circuit, the common mode node is removed and the current sources of the two differential parts are separated. A simple representation of the MOS parasitics responsible for reactive power is also represented. In this topology, the capacitors C_1 (including the parasitic capacitors of the mirror transistors), play a major role in the oscillation. Principally, these capacitors give the fundamental and the harmonics

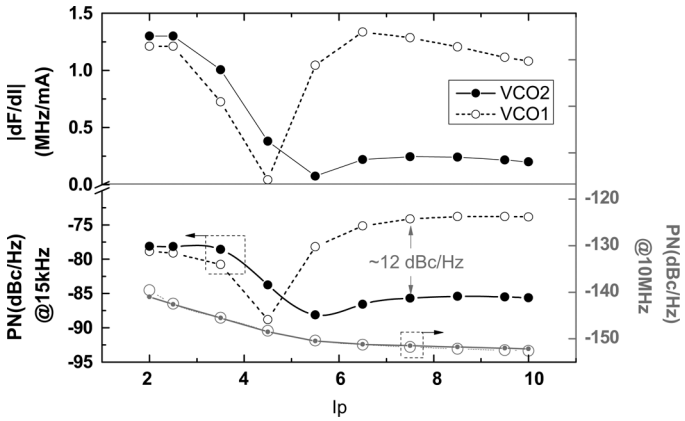

Fig. 11. Simulated frequency sensitivity and phase noise at 15 kHz for VCO2 and VCO1.

of the current the necessary paths to circulate. The objective of this change is to create a quadratic voltage at the sources of the switching transistors due to the current flowing into the capacitor C_1 and, thus, to counterbalance the tank quadratic current responsible for the frequency variation (i.e., I_{LC}).

The capacitor C_1 is optimized to avoid the tradeoff in the optimization of the phase noise at low offset frequency and at high-offset frequency. We are therefore more interested by the improvement of the close-in phase noise for intermediate and high currents. Fig. 11 shows the variation of the frequency with the current for VCO2. The size chosen for C_1 is 3 pF, while the dimensions of all the other components of VCO2 are the same as for VCO1. The frequency sensitivity dF/dI is very small beyond 4.5 mA for VCO2 compared to VCO1. Consequently, the low-frequency current noise will result in a significantly lower frequency modulation and a negligible phase noise. The phase noise at 15 kHz is presented in the same figure. As expected, practically no degradation in the close-in phase noise (e.g., at 15 kHz) is obtained beyond 4.5 mA for VCO2. The improvement, in comparison to VCO1, is 12 dBc/Hz. At high-frequency offset (e.g., 10 MHz), the phase noise of the VCO1 and VCO2 are practically similar (Fig. 4). This analysis demonstrates that the VCO2 topology is particularly suitable to avoid the tradeoff in the optimization of the phase noise at low-offset frequency and at high-offset frequency phase noise. In many cases, the

low-offset frequency noise is as important as the high-offset frequency noise. In OFDM-based systems, for instance, stringent flicker noise specifications are required to avoid inter-sub-carrier interference [1]. At the same time, a strict phase noise maximum level is also imposed at high-frequency offset in order to ensure negligible out-of-band radiation and to respect the modulation mask.

In order to understand more precisely the origin of this improvement, consider the one-port representation of the active part shown in Fig. 10(b). By using this circuit, we can write the admittance Y_d and Y_g seen from the drain and gate terminal of the transistors M2 and M1 as

$$Y_d = \frac{i_{\rm gd} + i_{db} + g_m V_{\rm gs,2}}{V_o} = \frac{g_m V_{\rm gs,2}}{V_o} + j\omega\left(2C_{\rm gd} + C_{db}\right) \tag{7}$$

and

$$Y_g = \frac{i_{\rm gd} + i_{\rm gs,1}}{V_o} = j\omega 2C_{\rm gd} + \frac{i_{\rm gs,1}}{V_o}. \tag{8}$$

By supposing that the current through $C_{\rm gs}$ is negligible compared to $g_m V_{\rm gs}$ (easily verified by simulation), we can demonstrate that

$$\frac{V_{\rm gs,2}}{V_o} = -\frac{V_{\rm gs,1}}{V_o} = -\frac{j\omega C_1}{g_m + j\omega C_1} \tag{9}$$

and

$$Y_d = -g_m \frac{\omega^2 C_1^2}{g_m^2 + \omega^2 C_1^2} + j\omega\left((2C_{\rm gd} + C_{db}) - \underbrace{\frac{g_m^2 C_1}{g_m^2 + \omega^2 C_1^2}}_{Cdo}\right) \tag{10}$$

$$Y_g = -g_m \frac{\omega^2 C_1 C_{\rm gs}}{g_m^2 + \omega^2 C_1^2} + j\omega\left(2C_{\rm gd} + \underbrace{\frac{\omega^2 C_1^2 C_{\rm gs}}{g_m^2 + \omega^2 C_1^2}}_{Cgo}\right). \tag{11}$$

Equations (10) and (11) reveal that the topology modification in Fig. 10 transforms both Y_d and Y_g. The modifications of Y_g are, however, negligible. In fact, $(\omega C_1)^2$ is very high compared to g_m^2. Consequently, the term Cgo is practically equal to $C_{\rm gs}$ and the real part of Y_g is negligible. Y_g of VCO2 and VCO1 are thus practically equal. In contrast, the introduction of the new negative term $(-Cdo)$ in the reactive part of Y_d, makes the impact of the modification more important. This term explains the negative feedback imposed by C_1. In fact, both $2C_{\rm gd,eff}$ and $Cdo_{\rm eff}$ increases with the current beyond 4.5 mA and can even totally cancel each other if we choose the right value of C_1. The subscript (eff) is added to discern the effective value of the capacitances submitted to the large signals of the VCO.

The variation of $Cdo_{\rm eff}$ with the tail current can be determined by using the test circuit of Fig. 6(a). For this, two versions of this circuit are used, one with a single-current sources, as in VCO1, and a second with two current sources, as in VCO2. The imaginary part of Y_d is equal to $2C_{\rm gd,eff} + C_{\rm db,eff}$ in the first case and $2C_{\rm gd,eff} + C_{\rm db,eff} - Co_{\rm eff}$ in the second case. The imaginary part of Y_d versus current is simulated in the two cases and the difference is used to determine directly $Co_{\rm eff}$. The results are shown in Fig. 12 for different values of C_1.

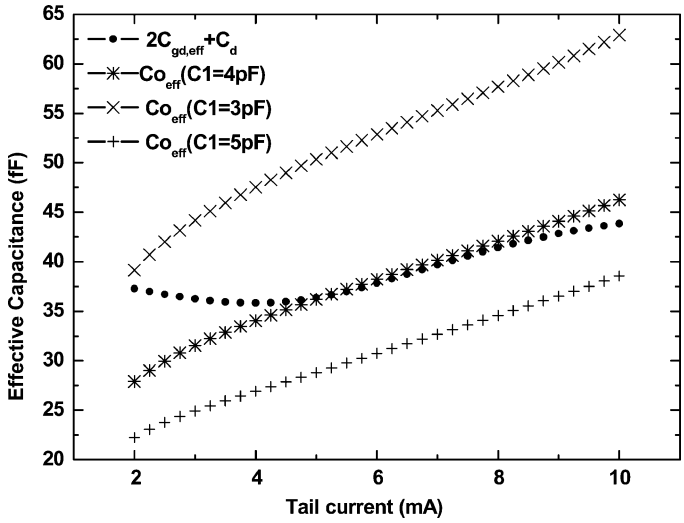

Fig. 12. Variation of the effective capacitance terms of Y_d of VCO2 [(10) for different value of $C1$].

As we see, the two curves increases with the current beyond 4.5 mA and have practically the same values if we choose $C1$ equal to 4 pF. Therefore, they will cancel each other in (10), and consequently decrease the sensitivity of the frequency to current variations. We recall that in a differential VCO, it is $4C_{\rm gd,eff}$ and not $2C_{\rm gd,eff}$ that should be compensated. A higher value of $Co_{\rm eff}$ with a higher slope is thus required. Higher values of $Co_{\rm eff}$ are obtained by decreasing $C1$ (e.g., $C1 = 3$ pF), as shown in Fig. 12. This explains why the optimal value of C_1 to improve the phase noise of the VCO2 is 3 pF (Fig. 12).

Another alternative to limit the effect of the parasitic capacitance of the switching transistors is to decrease their sizes. This solution results, however, in a smaller negative g_m. To compensate this diminution, we have to increase the equivalent parallel resistance of the tank, which can be achieved by increasing the value of the inductor ($R_p = (L\omega)^2/R_s$). In addition, higher R_p results in an output signal with higher amplitude, and thus, a phase-noise improvement. The simulated amplitude, as well as phase noise at 15 kHz for VCO1 and VCO2 designed with L equal to 1.6 nH and W/L of the switching transistors equal to 30 μm/0.35 μm are shown in Fig. 13. For comparison, the results for L equal to 0.8 nH are shown in the same figure. As expected, a significant improvement in the phase noise is achieved for all the current values when we increase L. The benefit of adopting the VCO2 topology is less impressive in this case, but still significant. The major drawback of increasing L, however, is that the capacitor of the tank, and thus, the tuning range should be decreased by the same coefficient (i.e., by two for the results of Fig. 13).

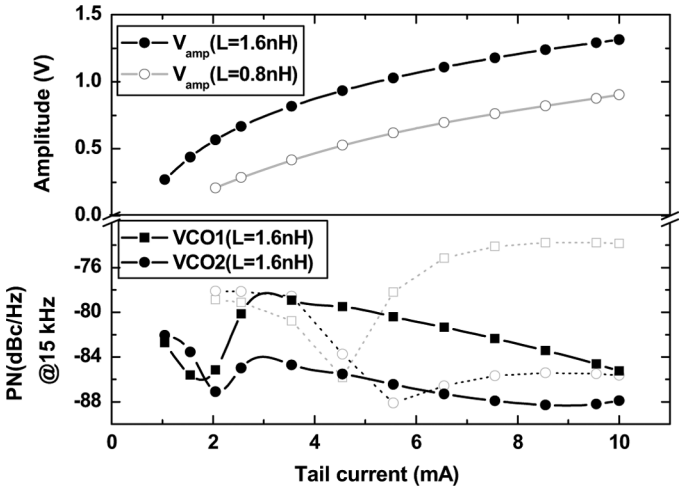

Fig. 13. Simulated amplitude of the output signal and phase noise at 15 kHz for VCO1 and VCO2 designed with ($L = 1.6$ nH, $\mathrm{W/L} = 30\ \mu\mathrm{m}/0.35\ \mu\mathrm{m}$) and ($L = 0.8$ nH and $\mathrm{W/L} = 50\ \mu\mathrm{m}/0.35\ \mu\mathrm{m}$).

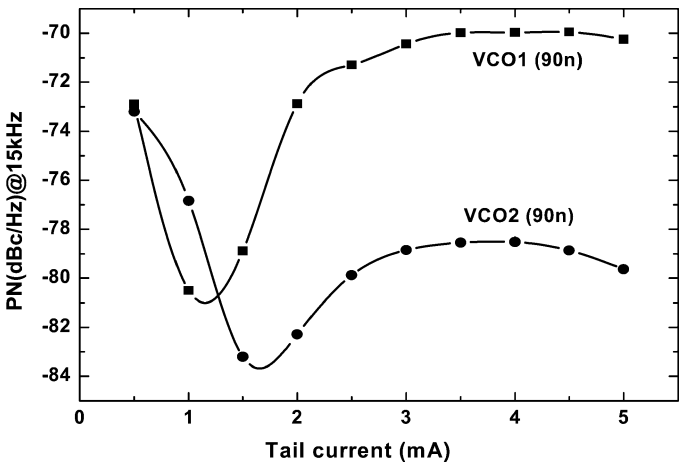

Fig. 14. Simulated phase noise of VCO1 and VCO2 designed with 90-nm transistors and 1-V power supply.

In order to verify the validity of the proposed solution in deep submicrometer (DSM) CMOS technology, a second version of VCO1 and VCO2 are designed with 90-nm transistors and 1-V power supply. The phase-noise performances at 15 kHz, shown in Fig. 14, demonstrates that the superior noise performance of the proposed topology is also valid for low-voltage DSM CMOS implementations.

IV. Experimental Results

Fig. 15 shows a die photograph of the test chip. The prototype VCO was fabricated in BiCMOS-SiGe process, but only the CMOS $(0.25\ \mu\mathrm{m})$ transistors were used. The VCO was designed for a center frequency of 3 GHz, and adopted the cancellation technique of the reactive power effect, described in Section V (Fig. 16).

To test the driving capabilities of the VCO, a true-single-phase-clock (TSPC) prescaler and inverter-based buffer were implemented at its output.

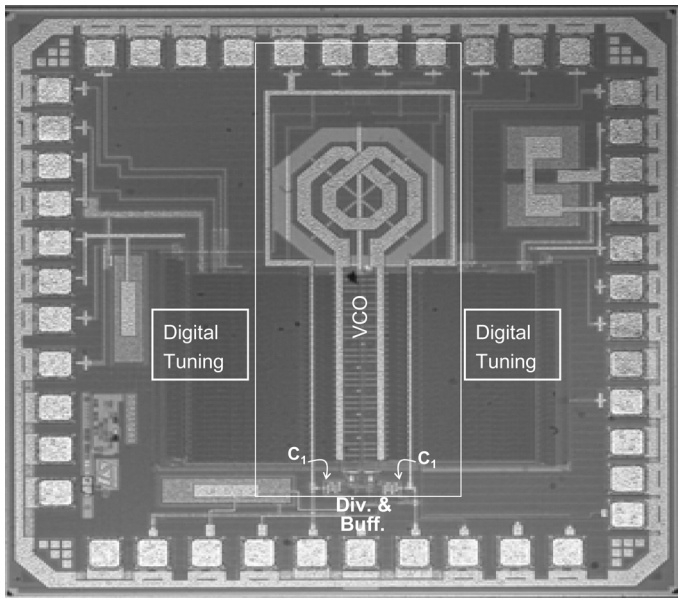

Fig. 15. Microphotograph of the test chip.

The VCO included a 6-bit digitally controlled bank of MOS varactors, as well as their automatic tuning circuits. The tuning circuit shown in Fig. 16(b) is a flash analog-to-digital frequency converter. It enables to tune the capacitance, and thus, the frequency of the VCO in an analog mode by varying the continuously voltage at the node Vt and switch the bank of the varactors to a digital mode by turning the control path Ctr to zero.

The VCO also includes a 10-bit digitally controlled bank of smaller MOS varactors with the same topology as shown in Fig. 16(b). This circuit can be activated optionally if a very fine digital tuning is required. The parasitic capacitors of these complex circuits limit severely the tuning range. To deal with this problem, a small inductor of about 0.8 nH is used in the tank, even if it is not the optimal choice for phase-noise performances, as previously shown in Fig. 13.

The measured tuning range at the output of the prescaler achieved with the bank of varactors in analog mode $(\mathrm{Ctr} = 1)$ is shown in Fig. 17. The voltage frequency transfer function of the VCO prescaler was quite linear over around 300 MHz (600 MHz for the VCO alone), which corresponded to a VCO frequency range from 2.4 to 3 GHz.

The VCO prescaler phase noise was measured using an Agilent E5052A signal source analyzer after digitally switching all the varactors to 0 or 1. The measured and simulated results are summarized in Figs. 18 and 19. The VCO prescaler exhibited a phase noise of -88 and -92 dBc/Hz at 10 kHz and -155 to -60 dBc/Hz at 10 MHz, when the VCO consume respectively 6 and 10 mA with a 2-V power supply circuit. As expected, the proposed VCO did not suffer from the well-known degradation of the close-in phase noise at high current [11], [12], [16]. This property enables to achieve an ultra low phase noise at high-frequency offsets (e.g., -160 dBc/Hz beyond 10 MHz) by increasing the current without any deterioration of the close-in phase noise, as shown in Fig. 18. The measured phase noise at maximum and minimum frequency exhibits a significant

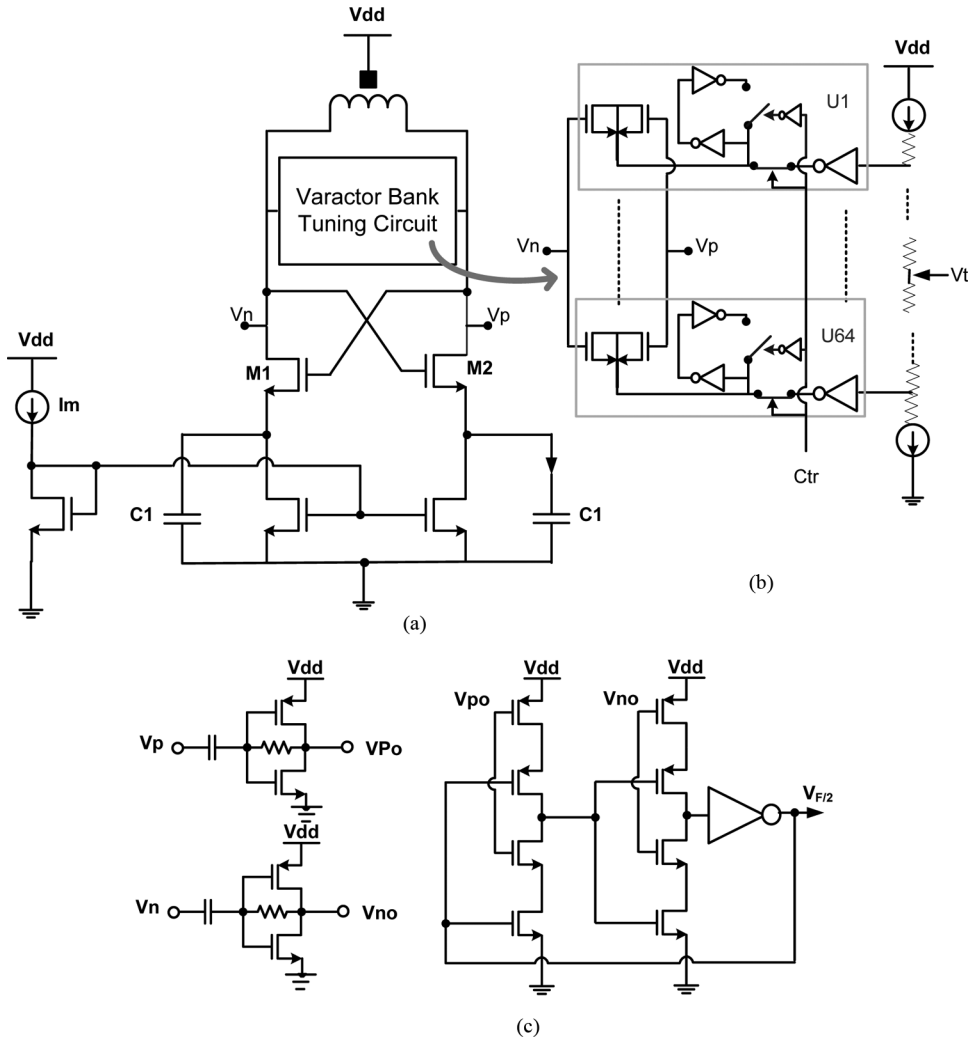

Fig. 16. Schematics of the implemented circuits. (a) VCO. (b) 6-bit frequency tuning and its bank of varactors. (c) Buffers and the TSPC prescaler.

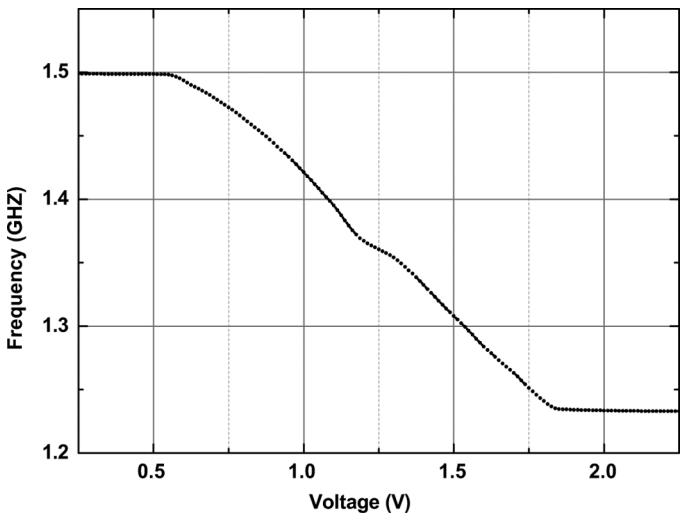

Fig. 17. Measured frequency tuning of the VCO prescaler.

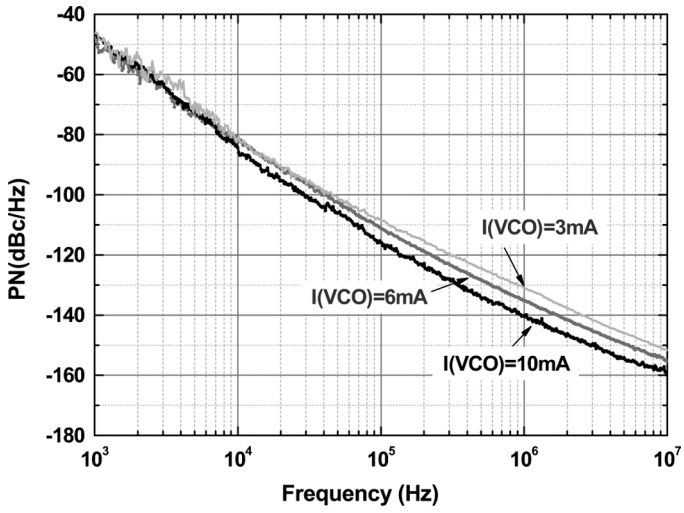

Fig. 18. Measured phase noise of the VCO prescaler circuit for a VCO current of 3, 6, and 10 mA. The precaler consumes 2 mA.

difference only at low offset frequencies, as illustrated by Fig. 19.

The measured phase noise at 15 kHz versus VCO bias current is shown in Fig. 20. A minimum of −93.8 dBc/Hz was obtained

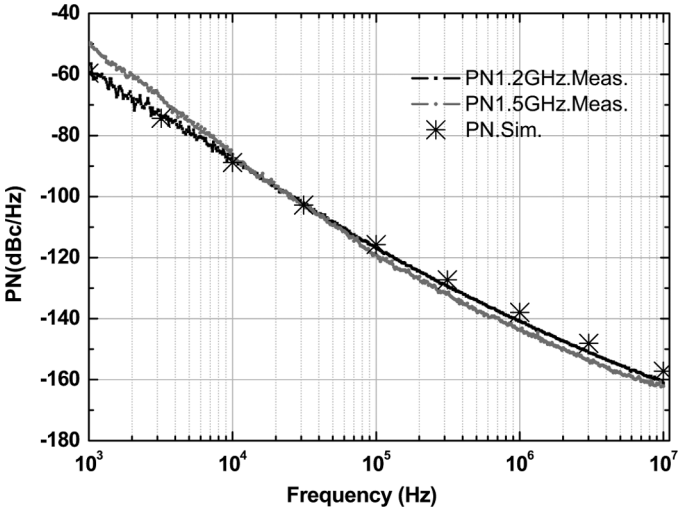

Fig. 19. Simulated phase noise the VCO prescaler at 1.5 GHz and measured phase noise at 1.5 and 1.2 GHz for comparison.

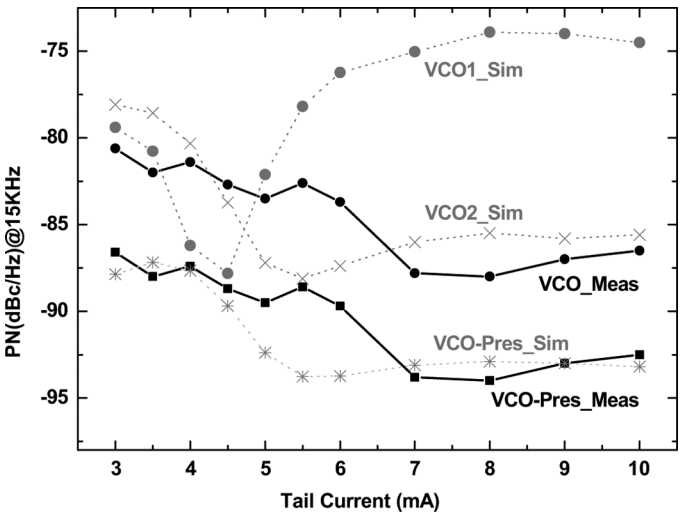

Fig. 20. Measured and simulated phase noise at 15 kHz of the VCO alone and the VCO with its prescaler.

TABLE I
COMPARISON WITH THE PREVIOUSLY REPORTED VCOs

Ref	Pdc mW	F GHz	PN 1MHz	FOM 1MHz	PN 10MHz
[7]	7.25	5	-123	-188.4	-135
[8]	6	4	-125	-189.3	-145
[10]	13.5	5.3	-124	-187.2	-
[15]	7.2	1.8	-128	-184.5	-140
This work	12	3	-130	-188.8	-149
	20	3	-133	-189.5	-154

for a VCO current consumption of 7 mA. For comparison, the simulated phase noise at the same offset frequency for a conventional cross coupled (VCO1) and the adopted topology (VCO2) is also shown in the same figure. This comparison illustrates the contrast between the classical cross-coupled topology where the close-in phase noise is deteriorated at high current and the proposed topology where this deterioration did not occur.

For a more general comparison to the previously reported cross-coupled VCOs, the commonly used figure-of-merit (FOM), which considers phase noise (PN), power consumption ($P_{\rm dc}$), and frequency (f_c) is used

$$\mathrm{FOM} = -20\log\left(\frac{f_c}{\Delta f}\right) + \mathrm{PN}(\Delta f) + 10\log\left(\frac{P_{dc}}{1\ \mathrm{mW}}\right). \tag{12}$$

A selection of VCOs with outstanding FOM is reported in Table I. In spite of its complex tuning circuits and small inductor, the proposed VCO exhibits an FOM of -189.5 at 1 MHz. This FOM can be improved if we reduce the tuning range by using a smaller bank of varactors and a larger inductor (as explained in Fig. 13). The phase noise of the VCO at 10 MHz is also reported in this Table I. At this offset frequency, the proposed VCO exhibits a phase noise -154 dBc/Hz (-160 dBc/Hz at the output of the prescaler), which is at least 9 dB better then all the reported VCOs.

V. CONCLUSION

A complementary analysis of the phase-noise mechanisms in the cross-coupled *LC* VCO was presented. This revealed the importance of the reactive power imbalances in the tank and in the active part. An enhanced VCO topology is proposed that enables the variation of the frequency with the current to be avoided and simultaneously optimizes the phase noise at high- and low-offset frequencies. A fabricated VCO prescaler circuit exhibiting a phase noise -92 dBc/Hz at 10 kHz and -160 dBc/Hz at 10 MHz was presented. The FOM achieved was -189.5 dBc/Hz/mW at 1-MHz offset.

REFERENCES

[1] E. Costa and S. Pupolin, "M-QAM-OFDM system performance in the presence of a nonlinear amplifier and phase noise," *IEEE Trans. Commun.*, vol. 50, no. 3, pp. 462–472, Mar. 2002.

[2] J. Mehta and R. B. Staszewski, "A 0.8 mm^2 all-digital SAW-less polar transmitter in 65 nm EDGE SoC," in *IEEE Int. Solid-State Circuits Conf.*, 2010, pp. 58–59.

[3] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[4] R. Aparicio and A. Hajimiri, "A noise-shifting differential Colpitts VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1728–1736, Dec. 2002.

[5] J. J. Rael and A. A. Abidi, "Physical processes of phase noise in differential *LC* oscillator," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2000, pp. 569–571.

[6] A. Koukab, "LC-VCO design with dual-G_m, boosted for RF oscillation and attenuated for LF noise," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 12, pp. 675–677, Dec. 2010.

[7] S. Levantino, C. Samori, A. Bonfanti, S. L. J. Gierkink, A. L. Lacaita, and V. Boccuzzi, "Frequency dependence on bias current in 5-GHz CMOS VCOs: Impact on tuning range and flicker noise upconversion," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1003–1011, Aug. 2002.

[8] A. Koukab, Y. Lei, and M. Declercq, "A GSM-GPRS/UMTS FDD-TDD/WLAN 802.11 a-b-g multi-standard carrier generation system," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1513–1521, Jul. 2006.

[9] Y. Ku and S. Cho, "An optimum current mirror ratio for low phase noise *LC*-VCO," *IEEE Micow. Wireless Compon. Lett.*, vol. 18, no. 12, pp. 809–811, Dec. 2008.

[10] A. Jerng and C. G. Sodini, "The impact of device type and sizing on phase noise mechanisms," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 360–369, Feb. 2005.

[11] C. Samori, A. L. Lacaita, A. Zanchi, S. Levantino, and G. Cali, "Phase noise degradation at high oscillation amplitude in *LC*-tuned VCO's," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 96–99, Jan. 2000.

[12] F. Svelto and R. Castello, "A bond-wire inductor-MOS varactor VCO tunable from 1.8 to 2.4 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 403–407, Jan. 2002.
[13] J. Groszkowski, "The interdependence of frequency variation and harmonic content, and the problem of constant-frequency oscillators," *Proc. IRE*, vol. 21, no. 7, pp. 958–981, Jul. 1934.
[14] C. Enz, "An MOS transistor model for RF IC design valid in all regions of operation," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 342–359, Jan. 2002.
[15] X. Li, S. Shekhar, and D. J. Allstot, "G_m-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-_m CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.
[16] B. Soltanian and P. Kinget, "AM–FM conversion by the active devices in MOS *LC*-VCOS and its effect on the optimal amplitude," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2006, pp. 108–112.

Adil Koukab (M'10) received the M.S. degree (DEA d'Opto-Electronique) from the University of Nancy, Nancy, France, in 1993, and the Ph.D. degree in electrical engineering from the Metz University, and Supélec, Metz, France, in 1997.

Since 1999, he has been with the Department of Electrical Engineering, Swiss Federal Institute of Technology Lausane (EPFL), Lausane, Lausane, Switzerland, where he is currently a Member of the Scientists Group. His current research interests include design, modeling and electronic design automation (EDA) development for RF, analog, and mixed-signal integrated circuits (ICs), physical parasitic effects, crosstalk, and substrate noise in mixed-signal system-on-chip (MS-SOC) designs