

## Experimental study of flat light-scattering substrates in thin-film silicon solar cells

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### ABSTRACT

In this work, a novel type of substrate for thin-film silicon solar cells is studied. The substrate has the advantage of being physically flat to allow the growth of cells with excellent material quality while being optically rough for enhanced light trapping that leads to high short-circuit current density. The substrate is made of rough zinc oxide (ZnO) which is grown on a flat silver reflector. The ZnO is then covered with amorphous silicon and the stack is polished to expose the tips of the pyramidal ZnO surface. The ZnO embedded in the amorphous matrix provides the desirable scattering of light while the surface onto which the cell is deposited is flat and allows for the growth of good-quality material. We present results of  $\sim 4 \mu\text{m}$  thick microcrystalline silicon solar cells prepared on such substrates with high open-circuit voltages of 520 mV. We also demonstrate a large relative efficiency gain of 10% compared to a state-of-the-art cell which is grown directly on an optimized textured substrate.

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### 1. Introduction

Thin-film silicon solar cells are promising candidates to meet the future demand for clean energy at a large scale, as they require minute amounts of an abundant material [1]. A small thickness of the active layer is needed in thin-film silicon solar cells to ensure satisfactory collection of the photogenerated carriers. The small thickness is advantageous in terms of raw material consumption but results in poor light absorption at long wavelengths, and consequently low short-circuit current density ( $J_{sc}$ ). Nowadays, light scattering at textured interfaces is the most successfully used approach to enhance the  $J_{sc}$  [2]; all recent certified efficiency records reported for thin-film silicon solar cells [3] were achieved on a textured surface. In the meantime, other more exotic approaches with high potential using elongated architectures [4–8], photonic crystals [9,10] or plasmonic effects [11–13] are under development.

Traditional light-path enhancement based on light scattering relies on textured interfaces between two media with different refractive indices  $n$ . Unfortunately, thin-film silicon deposition on textured interfaces leads to the growth of defective absorber material with porous areas that limit cell efficiency by decreasing both the open-circuit voltage ( $V_{oc}$ ), and the fill factor (FF) compared to reference cells deposited on flat electrodes. The appearance of

defective areas in active layers grown on rough substrates was observed both for microcrystalline silicon ( $\mu\text{c-Si:H}$ ) [14–16] as well as for amorphous silicon (a-Si:H) [17] materials. These porous areas also deteriorate the materials' long-term stability as reported recently for  $\mu\text{c-Si:H}$  solar cells by Boccard et al. [18].

Nevertheless, it has been shown that device sensitivity to textured interfaces can be reduced by careful tuning of the cell architecture. As an example, the introduction of resistive doped layers in the cell has recently been used to limit the negative impact of localized defective parts of the cell on the electrical properties of the device [19,20]. Still, these layers may not be sufficient to recover fully the  $V_{oc}$  and FF of a cell grown on a flat surface as follows: (1) the texturing increases the interface area, leading to higher carrier recombination which may affect the  $V_{oc}$ ; (2) the implementation of such a resistive contact layer may lead to increased serial resistance and therefore to a decrease of the device FF; (3) the growth-induced defects at V-shaped areas of the contact may not be fully passivated and (4) the material's long-term stability may remain affected by the porosity in the active layer.

To overcome the problem of growth on physically textured interfaces, while keeping optically rough interfaces, it was proposed to separate the light-scattering interface (interface 1) from the growth interface (interface 2) [21–23]. With this new approach, light scattering is promoted by a textured layer with a low index of refraction filled with a material with a higher refractive index. This stack is then polished to obtain a flat substrate. The choice of materials for this stack is crucial for several reasons. Firstly, the difference between their refractive indices should be large enough

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for efficient scattering at high angles. Secondly, the filling material should have the same refractive index as the cell grown on top. In this case, light that is scattered at interface 1 can re-enter the active layer of the solar cell at interface 2 under high angles without being refracted towards the normal surface. Thirdly, the filling material is an inactive part of the cell and should be non-absorbing.

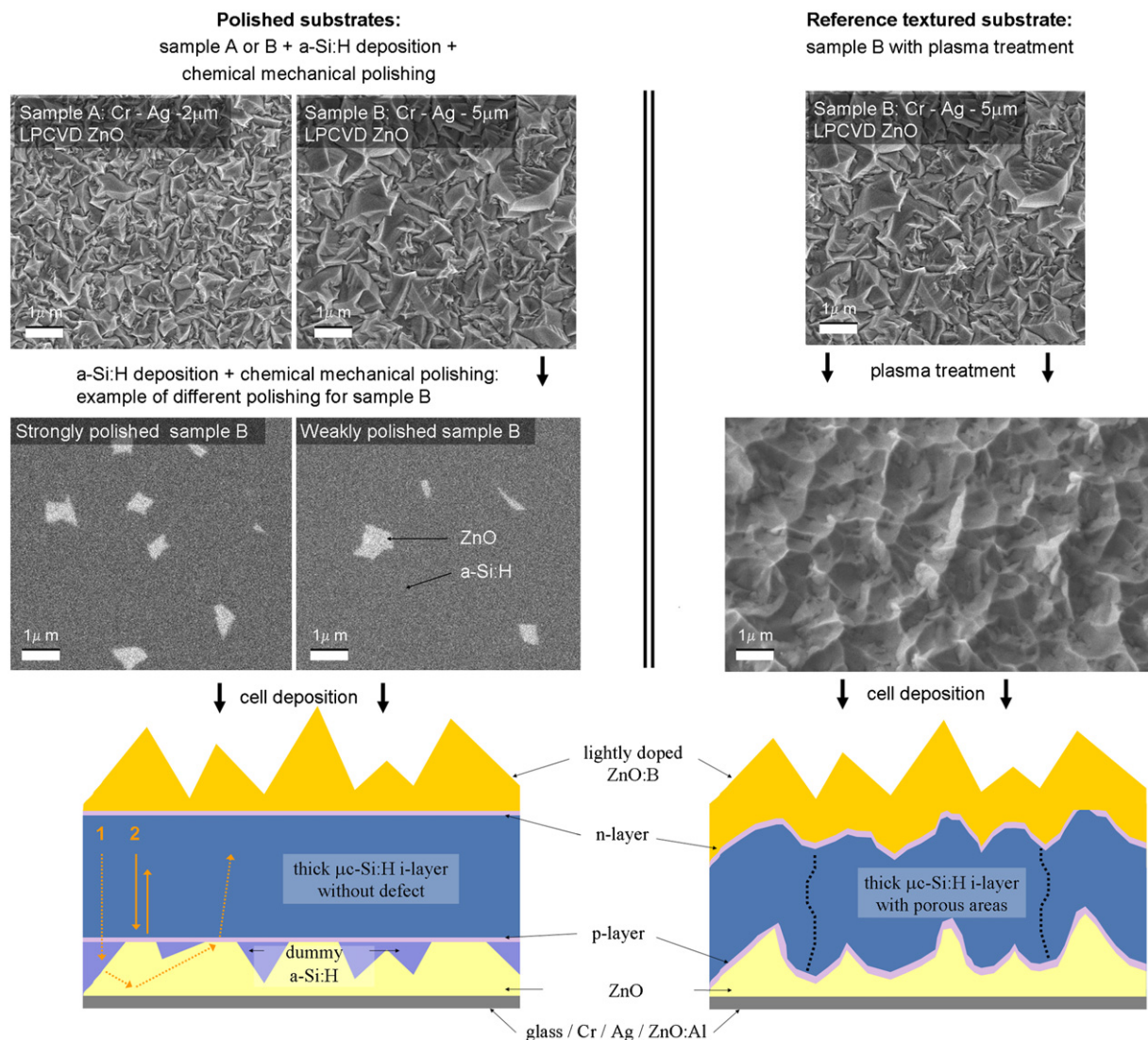
In order to fulfill these requirements, zinc oxide (ZnO) grown by low-pressure chemical vapor deposition (LPCVD) was chosen as the material with low index of refraction ( $n_{\text{ZnO}} \approx 2$ ), as its pyramidal shape is known for its excellent light-trapping properties [24,25]. A ZnO film was deposited without doping to reduce parasitic free-carrier absorption. It was grown on a flat silver (Ag) layer which has high reflection and ensures a good conductivity of the Ag/ZnO contact stack. Intrinsic a-Si:H was chosen as the filling material because its index of refraction ( $n_{\text{a-Si:H}} \approx 4$ ) is similar to that of the  $\mu\text{-Si:H}$  cells in the wavelength range of interest and because it does not absorb light above 800 nm. However, a significant amount of light below this wavelength should be absorbed in a single pass through the active layer, else it would be lost in this “dummy” inactive layer. Therefore, we believe that these substrates will be best used in multiple-junction thin film silicon solar cells such as triple-junction a-Si:H/a-SiGe:H/ $\mu\text{-Si:H}$

cells. In this case, the optical thickness is large for a single light pass through the cell for light below 800 nm, while longer wavelengths benefit from the light scattering given by the back reflector.

In order to mimic thick triple-junction solar cells, we studied the introduction of these substrates in thick  $\mu\text{-Si:H}$  solar cells ( $\sim 3.8 \mu\text{m}$  of intrinsic layer). This allowed us to investigate the potential total current that can be obtained with these substrates and the light-trapping properties compared to a state-of-the-art reference cell grown on a textured substrate. We show a large relative efficiency gain for the solar cell on the polished substrate compared to our reference cell when both cells are optimized independently for each substrate. A high  $V_{\text{oc}}$  of 520 mV was obtained for a cell grown on the polished substrate, while only 490 mV could be obtained for the reference cell grown on a textured surface with features that were smoothed and optimized by plasma treatment for high-efficiency cell growth.

### 1.1. Experimental details

In Fig. 1, scanning electron microscopy (SEM) images for both types of substrates as well as schematic drawings of the typical



**Fig. 1.** SEM images of (left) polished substrates and (right) reference textured substrate during fabrication. Schematic drawings of cells grown on both types of substrates appear below. The colored arrows in the lower left panel illustrate loss in light trapping due to the flat ZnO/Si zones. The dashed lines in the lower right panel illustrate porous areas due to defective  $\mu\text{-Si:H}$  growth. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

cell structures studied in this work are shown. The starting point for both flattened and reference textured substrates is a stack of chromium (Cr,  $\sim 10$  nm)/Ag ( $\sim 180$  nm)/aluminum-doped ZnO (ZnO:Al,  $\sim 20$  nm) that was deposited by sputtering at room temperature (Univex 450B, Leybold) on flat glass (Schott AF45). Two different thicknesses (sample A with thickness  $t_A \approx 2$   $\mu\text{m}$  and sample B with thickness  $t_B \approx 5$   $\mu\text{m}$ ) of LPCVD ZnO were then deposited.

The left hand side of Fig. 1 presents the flattened substrates. Dummy a-Si:H layers were deposited to entirely cover the ZnO pyramids. This stack was then flattened using a chemical mechanical polishing process. Stronger polishing removes more material from the sample, which increases the area of ZnO contact because of its underlying pyramidal shape. The right hand side of Fig. 1 shows the reference textured substrate made by treating sample B with a plasma to smoothen the sharp ZnO features [15,26].

On top of these substrates, p-i-n  $\mu\text{c-Si:H}$  solar cells were deposited by plasma-enhanced chemical vapor deposition. They consisted of a 35 nm thick p-( $\mu\text{c-Si:H}$ ) doped layer, an intrinsic layer (i-layer) of 3.8  $\mu\text{m}$  and 50 nm thick n-silicon oxide ( $\text{SiO}_x\text{:H}$ ) doped layer. As a front electrode a lightly boron-doped LPCVD ZnO layer of 5  $\mu\text{m}$  was deposited.

The  $V_{oc}$  and FF of the solar cells ( $\approx 0.25$   $\text{cm}^2$ ) were characterized by current–voltage ( $I$ – $V$ ) measurement using a dual-lamp solar simulator (Wacom WXS-220 S-L2) in standard test conditions (STC, 25  $^\circ\text{C}$ , AM 1.5 G spectra and 1000  $\text{W}/\text{m}^2$ ). The  $J_{sc}$  was calculated by the convolution of the external quantum efficiency (EQE) and the AM 1.5 G solar spectrum. For better understanding of the light trapping, total absorption (TA) of the cells was studied using a dual-beam spectrophotometer equipped with an integrating sphere (Lambda 900, Perkin Elmer). As no light is transmitted through the device, the absorption is defined as  $\text{TA} = 1 - \text{TR}$ , where TR is the measured total reflectance.

## 2. Results and discussion

### 2.1. Effect of dummy a-si:h layer and its polishing

Fig. 2 presents cell results (EQE, TA and electrical parameters) measured on flattened sample A and B substrates with the polishing state that yielded the most efficient cells. The EQEs of cells on both substrates exhibit a drop between 600 nm and 800 nm. This is ascribed to the fact that, at these wavelengths, light is not fully absorbed in a single pass and gets absorbed in the a-Si:H dummy layer instead. The drop is less and less pronounced near 800 nm where the absorption coefficient of the a-Si:H intrinsic layer approaches zero. Two main differences can be observed between the two polished substrates. The drop due to the a-Si:H parasitic absorption is more pronounced in flattened sample B. This is ascribed to the thicker dummy layer that was needed on sample B to completely fill the pyramidal features that are larger than those of sample A. However, this  $J_{sc}$  loss is counterbalanced by a gain in the long wavelength range which is related to more efficient light scattering on the substrate with larger feature size, as was observed in other studies [27]. The total currents as well as the electrical parameters are similar for both substrates.

The effect of polishing intensity is shown in Fig. 3 for flattened sample A. LP stands for low polishing, MP for medium or intermediate polishing and SP for strong polishing. The EQE is affected by the polishing in two ways: first, the drop due to parasitic absorption in the dummy a-Si:H layer tends to be smaller with increased polishing because a larger part of this layer is removed. More interestingly, the EQE and the TA between 750 nm and 1100 nm for MP and LP substrates are similar.

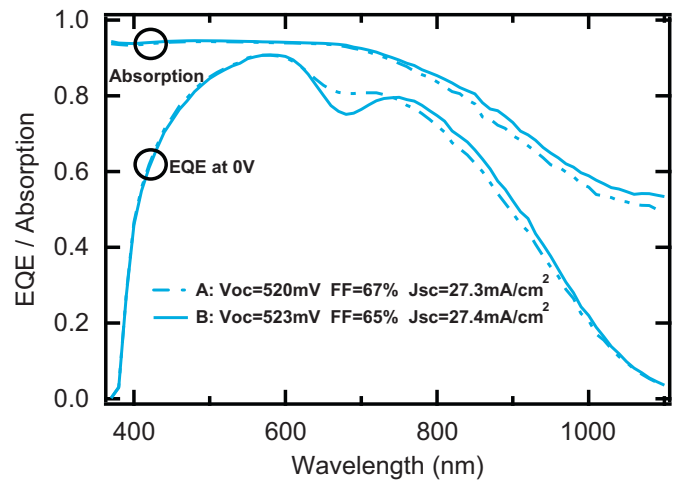


Fig. 2. EQE and TA of cells deposited on sample A and B polished substrates.

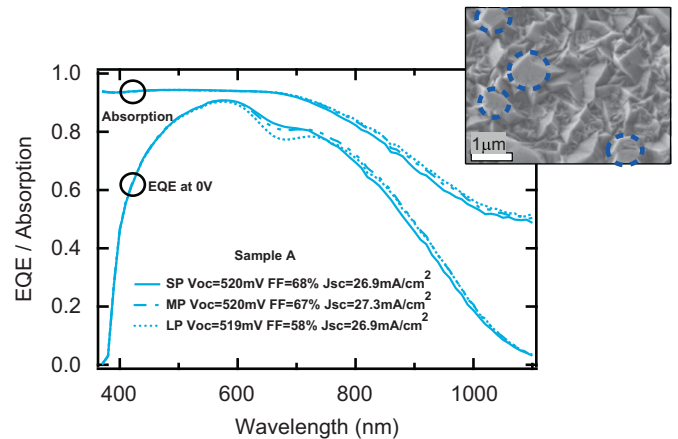


Fig. 3. EQE and TA of cells with different polishing on flattened sample A (LP stands for low polishing, MP for medium polishing and SP for strong polishing). The inset presents a SEM image of an MP sample A after removing all Si layers. Circles mark polished pyramids.

The SEM image shown in Fig. 3 helps us to understand why there is almost no change in light trapping between LP and MP substrates. It presents an image of MP sample A after removing all silicon layers by  $\text{SF}_6$ – $\text{O}_2$  plasma etching. It is observed that only the big pyramids are trimmed in this polished state, allowing all the other smaller pyramids to continue to efficiently scatter the light, as in LP sample A. Still, Fig. 3 also shows that a loss of light trapping in the solar cell occurs for SP. This loss in light trapping can be explained by the increased flat area of the ZnO/Si interface when too many pyramids are trimmed. There are two major paths of losses in light trapping due to the flat ZnO/Si zones which are illustrated by the colored arrows in Fig. 1: the first path (1) shows that the light which goes through the back reflector stack and which is efficiently scattered into a high angle, will be refracted toward the normal when impinging on a flat ZnO/Si zone. The second path (2) shows that a significant part of the light will be directly reflected when impinging on a flat ZnO/Si zone after one single path in the active layer.

The effect of polishing intensity on FF is opposite that on  $J_{sc}$ . When substrate A is less polished (LP), a low FF is observed. A high FF is recovered for higher polishing (MP), but further polishing (SP) does not improve FF any more. The FF trend is expected and can be explained as being an effect of the serial resistance, which decreases as more points of contact are opened



between the cell p-( $\mu\text{c-Si:H}$ ) contact layer and the ZnO with increased polishing. Therefore, the carriers have a smaller distance to travel laterally through the p-layer before being collected by the ZnO back contact, leading to lower resistive losses. The  $V_{oc}$  is affected mainly by material quality and surface recombination. In this set of experiments the  $V_{oc}$  is stable because of the similarly low roughness of the substrates. In this case, the material quality is same as the cells are co-deposited, and the surface recombination should also be similar.

It has to be emphasized that the dependencies of  $V_{oc}$  and FF on the polishing state strongly depend on the type of p-layer used for the cell. Indeed, a p-( $\text{SiO}_x\text{:H}$ ) doped layer which has been proven to drastically enhance cell performance on rough substrates [20] will be highly detrimental to the FF of a cell grown on a polished substrate because of its low lateral conductivity. In addition, such a p-( $\text{SiO}_x\text{:H}$ ) doped layer has a significantly different refractive index from an oxygen-free Si layer, which would introduce undesired refraction at the flat interfaces. Thus the optimum state of polishing for  $V_{oc}$ , FF and  $J_{sc}$  depends on the device architecture.

In a third experiment, the effect of an a-Si:H doped dummy layer on the EQE is compared to an intrinsic dummy layer for substrates of type A. Fig. 4 shows that doping the dummy layer affects the EQE at long wavelengths and decreases the  $J_{sc}$  by  $1.3 \text{ mA/cm}^2$ . It is concluded that there is larger parasitic absorption (compared with the undoped case) due to the dopant. However, the addition of dopant in the dummy layer could allow for better transport of the carriers and therefore improve the cell FF. Still, we believe that it is more beneficial for the cell efficiency to carefully tune the ZnO areas of contact and the mean distance between them, while using a highly conductive p-layer with an undoped dummy layer, than to design a cell with a doped dummy layer and a thinner conductive layer on top. Indeed, from the results of different polishing states for samples A shown in Fig. 3, it was observed that a good FF can be reached without current losses with medium polishing. By increasing the density of contact points (higher polishing SP), the FF did not improve significantly (only 1%). Thus, we suppose that the FF of 67–68% obtained in this experiment is the highest we could get for such thick cells.

Of course this discussion on the addition of dopant depends on the thickness of the dummy layer that is needed to cover the ZnO features. If shallow features are sufficient for efficient light confinement, and if a dummy layer thinner than 100 nm is sufficient to fill the ZnO, then a doped material may not significantly deteriorate

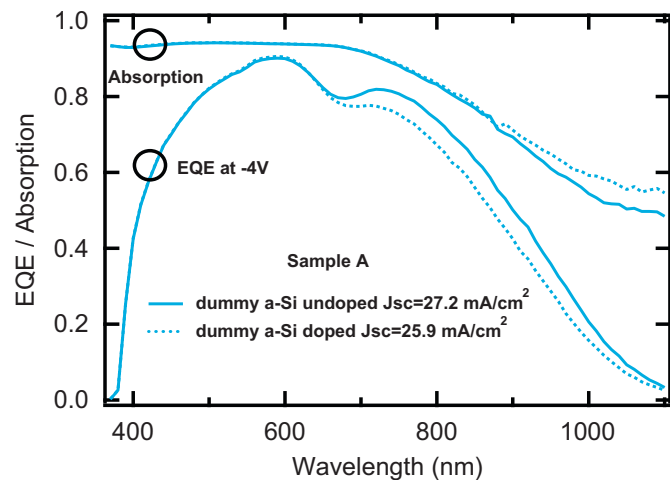


Fig. 4. EQE and TA of cells deposited on flattened sample A filled with doped or intrinsic dummy layers.

the cell EQE. In the case of MP sample A used in this experiment, several hundreds of nanometers of a-Si:H dummy layer remained on the substrates after polishing, substantially reducing the cell EQE.

## 2.2. Potential of polished substrates: comparison with a reference textured cell

In this section, we study the potential and issues of the polished substrates. Firstly, to compare light trapping, the cell with the highest current grown on the polished sample is compared to a cell grown on a textured reference substrate. Secondly, the reference cell and the best cell on a polished substrate are compared in terms of  $V_{oc}$ , FF and overall efficiency. The reference cell is grown on a state-of-the-art textured substrate designed for  $\mu\text{c-Si:H}$  solar cells with high efficiencies. As Fig. 1 shows it consists of a type B sample which ZnO is treated by plasma to render its surface smoother leading to high  $V_{oc}$  and FF [26]. However, the plasma treatment is known to decrease the light-trapping properties of the LPCVD ZnO pyramidal shape [15,16,28]. Here, the length of the plasma treatment is adapted to obtain a substrate that optimizes the cell efficiency by making compromises between the  $V_{oc}$ , FF and  $J_{sc}$  values. With this length of treatment, the quality of material deposited on it is already good but it will be observed that the polished substrates lead to  $\mu\text{c-Si:H}$  material with higher quality.

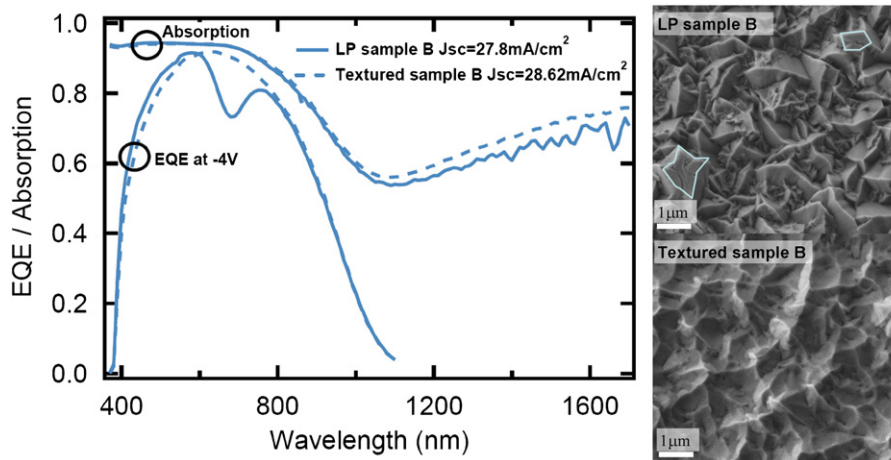
### 2.2.1. Light-trapping performance of the polished substrates

The highest current at long wavelength (800–1100 nm) on a polished substrate was obtained on a flattened type B sample with low polishing. This is expected, as (1) the feature size of sample B is more adapted for light trapping in  $\mu\text{c-Si:H}$  cells than the feature size of sample A [27]; (2) the low polishing ensures the smallest flat ZnO/Si area and (3) the thick layer of a-Si:H deposited on sample B to bury its features does not affect the EQE above 800 nm. In Fig. 5, the EQE and TA of LP flattened sample B are compared with those of the reference cell grown on the textured substrate.

When comparing the EQE curves with a bias of  $-4 \text{ V}$  and without bias, no difference is observed below 550 nm for the polished substrate, whereas the textured substrate shows a gap between these two curves (not shown). Thus, the EQE difference in the blue region is attributed to collection losses in the reference cell. This difference does not affect the light-trapping properties in the long wavelength range. The drop in the EQE curve around 700 nm for the polished substrate was already explained as being due to absorption in the dummy layer. However, above 800 nm the dummy a-Si:H layer does not absorb, and light trapping can be compared for these two substrates.

We might have expected higher light-trapping capabilities with the lowly polished substrate. Indeed, its textured buried interface corresponds to an untreated LPCVD ZnO sample, except for a few trimmed pyramids as the SEM image in Fig. 5 shows. The textured substrate has similar feature sizes to the polished substrate but is highly smoothed by the plasma treatment (see SEM images in Fig. 5), which is known to significantly decrease light trapping compared to an untreated sample [15,18,25,27]. Thus, the result shown in Fig. 5, where both EQE and TA are similar between 800 nm and 1100 nm, was not anticipated. Indeed a slight advantage in light trapping is observed for the cell grown on the textured reference substrate.

The slightly lower light trapping of the polished substrate is attributed to the flat ZnO/ $\mu\text{c-Si:H}$  areas created by the polishing process. This is corroborated by oscillation fringes in the polished cell absorption curve above 1200 nm shown in Fig. 5. These oscillations are attributed to interference fringes due to flat



**Fig. 5.** (Left) EQE and TA of cells grown on a flattened sample B with low polishing (LP) and on a reference textured cell on sample B treated by plasma. The indicated  $J_{sc}$  were calculated from the EQE measured at  $-4$  V. (Right) SEM images of both substrates after removal of all Si layers. The outlines drawn in LP sample B mark polished pyramids.

interfaces and are not observed in the absorption curve of the textured cell. Furthermore, the higher absorption of the textured cell above 1100 nm also indicates better light confinement for these wavelengths. To conclude, this experiment shows that flat interfaces remain optically visible even in LP samples with limited flat ZnO/Si areas and are detrimental to light trapping.

### 2.2.2. Electrical cell performance on polished substrates

The last results showed that light scattering of polished substrates is not as good as anticipated. Yet the light confinement is comparable to the textured substrate at long wavelengths. The potential of these substrates to lead to high cell efficiency due to the physically flat interface for cell growth will now be presented.

Table 1 presents the parameters of solar cells made in two independent depositions. The first two rows correspond co-deposited cells on our best polished substrate and the reference textured substrate, made using a p-( $\mu$ c-Si:H) doped layer that is optimized for the architecture of the polished substrate. The third row corresponds to an identical cell, but with an oxygen-containing p-doped layer that is optimized for textured substrates. This allows a fair comparison between the polished and the textured substrates, since this cell is not hampered by layers that are designed for other cell architectures.

The improvement of cell performance thanks to the polished substrate is clear in the co-deposited cells with a p-( $\mu$ c-Si:H) doped layer. As the cells are co-deposited, the higher FF and  $V_{oc}$  values obtained on the polished substrate are directly attributable to the improved quality of the  $\mu$ c-Si:H material grown on the flat interface. The lower current is due to absorption in the dummy layer and to lower light trapping as explained previously. However this loss is more than compensated by the improved FF and  $V_{oc}$  values. Finally, an overall relative efficiency gain of almost 20% is realized by using the polished substrate. This result is also interesting because p-( $\mu$ c-Si:H) doped layers are commonly used and can be implemented in the simplest cell designs.

As discussed previously, the effect of electronically poor material grown on textured surfaces can be mitigated by using well-designed cell architectures. The use of a p-(SiO<sub>x</sub>:H) doped layer helps the cell to be less sensitive to locally porous material, which leads to an increase of the reference cell FF, as expected. Nevertheless, the cell on the polished substrate with a p-( $\mu$ c-Si:H) doped layer outperforms the reference cell in  $V_{oc}$  and FF. The

**Table 1**

Results for two co-deposited cells with a p-( $\mu$ c-Si:H) doped layer optimized for polished substrates, and for a cell with a p-doped layer optimized for textured substrates.

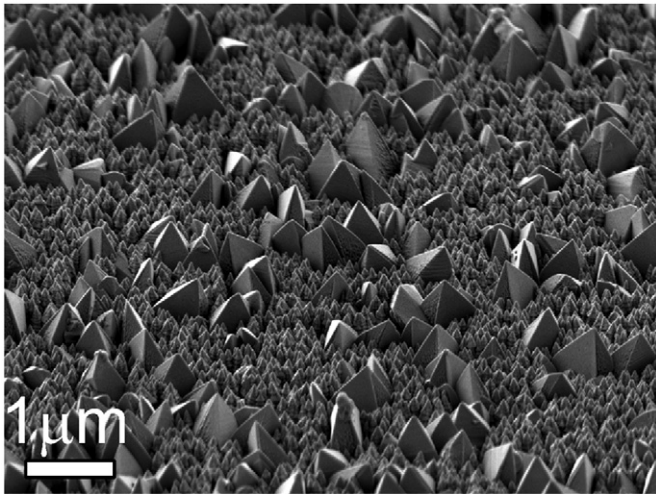
Type of substrate/p-doped layer	FF (%)	$V_{oc}$ (mV)	$J_{sc}$ (mA/cm <sup>2</sup> )	Efficiency (%)
Textured/p-( $\mu$ c-Si:H)	58	494	28	8
MP sample A/p-( $\mu$ c-Si:H)	67	520	27.3	9.5
Textured/p-(SiO <sub>x</sub> :H)	62	491	28.3	8.6

efficiency of the cell grown on the polished substrate with an ordinary p-( $\mu$ c-Si:H) doped layer exhibits a 10% relative gain compared to the cell grown on the textured substrate with an optimized p-(SiO<sub>x</sub>:H) doped layer.

### 2.3. Perspectives

Previously we could fabricated cells with efficiencies greater than 10% on the plasma-treated textured sample B with a cell thickness of 1.2  $\mu$ m, whereas with the same substrate the  $\sim 4$   $\mu$ m thick cell shown in Table 1 reached only 8.6%. This indicates that a  $\sim 4$   $\mu$ m thick single-junction  $\mu$ c-Si:H cell is not an optimal structure for these substrates. Thick  $\mu$ c-Si:H cells were used here to mimic absorption in an optically thick cell, allowing us to assess the substrate potential with regard to  $J_{sc}$  as well as  $V_{oc}$  and FF. As the dummy layer is absorbing below 800 nm, the incorporation of these substrates in triple-junction cells (a-Si:H/a-SiGe:H/ $\mu$ c-Si:H), which absorb a substantial amount of light in a single pass through the cell, should be preferred to reach high efficiencies.

In addition, better control of the mean distance between the polished ZnO areas that act as contacts is desirable. In this regard, the approach of Sai et al. [21,22] to use periodic arrays may be promising. Another improvement would be optimized ZnO texture for enhanced light trapping. It was shown that a wide range of different ZnO morphologies can be obtained by modifying the LPCVD deposition conditions of ZnO [29,30]. A promising texture to solve both previous issues (better control of the density of contact and of light trapping) consists of ZnO films containing features with multiple scales, as shown in Fig. 6. It consists of large, tall pyramids surrounded by smaller ones. The growth conditions allow one to tune the tall-pyramid density, which



**Fig. 6.** SEM image of an adapted ZnO morphology for further improving the polished back reflector substrates presented in this contribution.

determines the density of electrical contact after polishing. The smaller pyramids would remain untouched by polishing and their size should be optimized for light trapping.

An additional improvement would be to address absorption in the dummy layer material. Alloying with oxygen or carbon, for example, increases the silicon bandgap, hence reducing absorption losses close to 800 nm. However, such alloying is accompanied by a lowering of the refractive index, which would lead to stronger undesirable refraction at the interface between the filler material and the  $\mu\text{-Si:H}$  cell. It will thus require a careful trade-off between these two effects (less parasitic absorption vs. more reflection losses) to boost cell efficiency.

### 3. Conclusion

A concept for physically flat back reflectors that ensure the deposition of good material quality, but that are optically rough for enhanced  $J_{sc}$ , was discussed. LPCVD ZnO with pyramidal texture was covered with a dummy  $\text{a-Si:H}$  layer which was then polished to reveal the ZnO contact and to obtain a flat substrate. Scattering occurs at the interface between the ZnO pyramidal texture and the  $\text{a-Si:H}$  dummy layer and allows for impressive light confinement. The flat interface allows for the growth of  $\mu\text{-Si:H}$  material with few structural defects as indicated by the high  $V_{oc}$  (520 mV) and FF (67%) of the cells grown on top. The effect of polishing on light trapping as well as on  $V_{oc}$  and FF was discussed. Finally, the efficiency of the best cell obtained on the polished substrate with a  $\text{p-(}\mu\text{-Si:H)}$  doped layer was compared with an optimized  $\mu\text{-Si:H}$  reference cell with a  $\text{p-(}\mu\text{-SiO}_x\text{:H)}$  doped layer on an optimized textured substrate. A 10% relative efficiency gain was observed, showing that polished substrates have the potential to be successfully applied in high-efficiency multi-junction solar cells.

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