Design of a Discrete-Component Impulse-Radio Ultra Wide-Band (IR-UWB) Testbed and Design of a Very Low-Power IR-UWB Transmitter in CMOS Technology

PAR

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Abstract

This work presents, in a first part, a testbed for Impulse-Radio Ultra-Wideband (IR-UWB) communication for validating the possibility to do such radio communications. The UWB radio is a radio technique that consists to send extremely short impulses (few nano-seconds) which have a rich spectral content over several hundreds of MHz. The UWB radio we consider here works in the 4.0 to 4.5 GHz frequency range.

The IR-UWB radio allows high datarates and small power consumption. In addition, it allows localising precisely a mobile transmitter because UWB signal are similar to those of radar.

As UWB radio is different than conventional narrow-band radio, the algorithms used for communication and synchronisation between UWB devices need to be reconsidered. The UWB testbed presented here allows validating and experimenting these algorithms in order to improve and publish them with significant results.

There are several already published UWB testbed but few of them are described with enough details to be rebuilt as they are by other researchers or scientists in order to reproduce an experiment. In addition, building such a testbed requires an advanced knowledge not only in electronics and microwave theory but also on practical aspects of building such devices. However, many researchers have not this knowledge because they work on another field and thus, we provide a detailed description about the design and construction of the parts of the testbed in order to help anyone who wants to build the testbed. It is also possible to modify the design of the testbed in order that it works in another frequency range by following the methodology of design we used. The testbed is entirely designed with off-the-shelf discrete components and can be built at a relatively low price. We begin our work by presenting first a very simple but viable UWB testbed in order to understand the principles of UWB radio and to justify further design consideration made later in the work. We also present a mathematical

study of UWB signals that allows to rapidly determine their specifications in order to generate a true well shaped UWB signal.

This work presents, in a second part, the design and construction of an integrated low-power UWB transmitter in CMOS 0.18um technology. As UWB radio is by nature low-power, we present a novel architecture for generating an arbitrary signal by consuming the smaller as possible amount of energy. We use this architecture for generating the UWB impulse that we determined mathematically in order to have a shape that optimize the spread of energy in the available frequency range (4.0 to 4.5 GHz as for the testbed). We present three prototypes of the architecture where one is patented.

Abrégé

Cette thèse présente, dans un premier temps, une plate-forme de test pour radio impulsionnelle à très large bande (ULB) afin de valider expérimentalement la faisabilité d'un tel type de communication. La radio impulsionnelle ULB est une technique radio qui consiste à envoyer des signaux impulsionnels très courts (quelques nano-secondes) ayant un contenu spectral riche et large de plusieurs centaines de MHz. La radio considérée ici émet dans la bande 4.0 à 4.5 GHz.

La radio ULB permet d'obtenir des débits élevés avec une faible consommation d'énergie. Elle permet en outre, la possibilité de localiser précisément la position de l'émetteur car la nature de ses signaux est proche de ceux du radar.

Comme la radio ULB est de nature différente de la radio conventionnelle à bande étroite centrée sur une porteuse, les algorithmes utilisés pour communiquer et synchroniser les émetteurs et récepteurs de ce type de radio doivent être entièrement revisités. La plate-forme de test que nous présentons ici permet justement de valider et expérimenter ces algorithmes afin de les améliorer et les publier.

De nombreuses plate-formes de test pour radio ULB sont décrites dans les publications mais peu d'entre-elles le sont de manière suffisamment précise pour que d'autres équipes de chercheurs puissent la reconstruire à l'identique afin de refaire ou d'améliorer une expérience. De plus, construire une telle plate-forme demande des connaissances avancées en électronique, et ce également en ce qui concerne la réalisation pratique des éléments de cette plate-forme. Or, à cause de leur spécialisation dans un autre domaine, de nombreux chercheurs n'ont pas forcément l'expertise ni l'équipement pour construire de telles plate-formes, c'est pourquoi nous avons veillé à donner tous les détails relatifs à la conception et la construction de cette plate-forme afin de guider quiconque souhaite la reproduire. Ainsi, il est également possible de

modifier la conception électronique de la plate-forme pour la faire fonctionner dans une autre gamme de fréquences en suivant la méthodologie indiquée. La plate-forme est entièrement conçue avec des composants discrets disponibles dans le commerce et peut être construite pour un coût relativement bas. En préambule, nous présentons un premier prototype de plate-forme de test rudimentaire afin de comprendre les enjeux et difficultés et ainsi de justifier les choix de conception qui ont étés appliqués dans la plate-forme de test définitive. Nous présentons également une étude mathématique des signaux ULB permettant de calculer rapidement les caractéristiques que doit avoir un signal ULB pour être considéré comme tel.

Cette thèse présente, dans second temps, la conception et la réalisation d'un émetteur ULB en technologie intégrée CMOS 0.18um à très basse consommation. La radio ULB étant par nature à basse consommation, nous présentons une architecture originale permettant de générer un signal arbitraire en utilisant le moins possible d'énergie. Nous utilisons cette architecture pour la génération d'un signal ULB que nous avons déterminé mathématiquement pour avoir une forme qui optimise la répartition de la puissance dans le spectre dans la gamme de fréquence considérée (de 4.0 à 4.5 GHz comme pour la plate-forme). Nous présentons trois variantes de l'architecture dont l'une constitue un brevet.

Mots-clé   ULB, Ultra-Large Bande, IR, Radio Impulsionelle, plate-forme de test, composants discrets, émetteur basse consommation, technologie intégrée CMOS 0.18um

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Part I

Introduction to UWB

Chapter 1

Introduction

1.1 Introduction to UWB

The Ultra-Wideband (UWB) technology is very promising and inexpensive technology for communication with high datarate and/or low-power. The main idea is to transmit data on a wide bandwidth spectrum and not on a single tone carrier as done in conventional narrow-band radio. The use of a wide bandwidth allows using smaller amount of power in each frequency band thus reducing the effect of interference on other radio systems. The wide bandwidth makes also the transmission more robust to other radio system interference and the use of frequency hopping is no more required.

According to FCC regulations (2002), Ultra-wide band systems are defined as those systems which occupy a bandwidth of at least 10% of the center frequency or 500 MHz, whichever is lower. UWB can be used for high bandwidth communications at low energy levels by using an available radio spectrum of 7.5 GHz (3.1 to 10.6 GHz) [1]. This allows the UWB systems to coexist with other systems because the power density is sufficiently low to be perceived as noise by the others. The FCC regulations also defines the amount of power that is authorized in each frequency band without disturbing other devices or systems, as shown in Figure 1.1; how to design systems that are compliant with these regulations will be abundantly discussed in this work.

Because of limitations in technology (2002), the increase in complexity and power consumption lead one to conclude that the bandwidth between 3.1 and 4.8 GHz will provide the most effective bandwidth for initial deployments of UWB devices. Given the bandwidth from

NOTE:
1. UWB EMISSION LIMITS ABOVE 960 MHZ ARE BASED ON
EIRP MEASURED USING AN RMS DETECTOR WITH 1 MHZ
RESOLUTION BANDWIDTH.
2. UWB EMISSION LIMITS BELOW 960 ARE BASED ON
MEASUREMENTS USING A CISPR QUASI-PEAK DETECTOR
WITH A 120 KHZ BANDWIDTH AND THEY MUST FOLLOW
EXISTING RADIO FREQUENCY DEVICE LIMITATIONS.
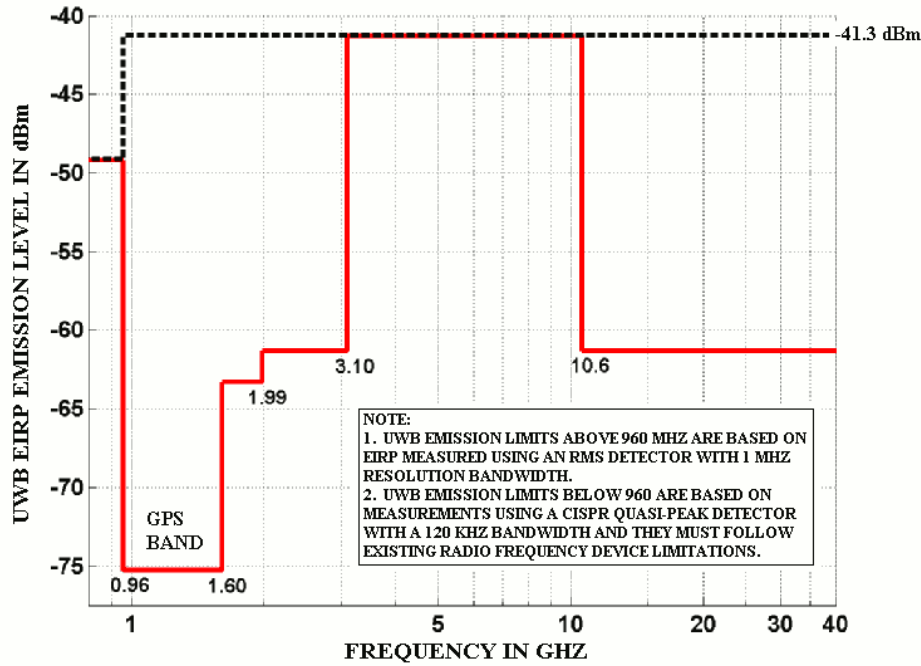
Figure 1.1: The FCC regulations

3.1 to 4.8 GHz, there are several ways to design a UWB communication system. One method is to use the entire 1700 MHz of bandwidth and spread the transmitted information using spread spectrum or code-division multiple access (CDMA) techniques. The main advantage of building UWB communication systems based on spread-spectrum techniques are that these techniques are well understood and have been proven in other commercial technologies like for example wideband CDMA. However, building RF and analog circuits as well as high speed analog-to-digital converters (ADCs) to process this extremely wideband signal is a challenging problem as discussed in this work.

1.1.1 UWB and conventional (narrow-band) Radio

The wide band nature of the signal has advantages over the narrow band signal. To name a few, wide band signals are immune to multi-path fading, the multi-path components are resolved due to short duration of the signals. Due to this, there is a significant reduction in the fading margin leading to a low power operation. In addition, the UWB signals are very useful in localization applications which are also a consequence of its wide band nature.

A major difference between narrowband radio systems and UWB systems is that tradi-

tional systems transmit information by modulating the power level, frequency, and/or phase of the carrier signal whereas UWB transmissions transmit information by generating radio energy at specific time instants and occupying large bandwidth thus enabling a pulse-position or time-modulation. UWB pulses can be sent sporadically at relatively low pulse rates to support time/position modulation, but can also be sent at rates up to the inverse of the UWB pulse bandwidth (see [2]). These are some of the advantages of an UWB signalling system in comparison to narrow band signalling systems:

- High data rate;

- Very precise range measurement for tracking systems;

- Excellent performance in difficult environments such as those with multiple reflective paths and interferers;

- Easily adapted to dynamic data rate systems;

- Ability to track simultaneously a large number of tags because of very short pulse-width;

1.1.2   UWB OFDM

The UWB OFDM (UWB Orthogonal Frequency Division Multiplexing) is based on multi-tone combination for wide-band signals generation (see [3]). The main idea is to generate a pattern of several high frequency tones and to transmit information by changing these tone pattern in order to create a symbol, thus the spectral composition of the transmitted signal evolve in the time according to the modulation of the symbol. The receiver amplifies and filters the UWB signal and calculates the Fourier transform in order to retrieve each pattern and thus the related symbol. The main characteristics of UWB OFDM are the following :

- high power consumption (because of analog multi-tone generation);

- two degrees of freedom on the signal generation : the frequency of the tone and the time they are produced or not;

- multi-carrier (one per tone);

- multi-band (tones can be used in several bands as desired);

- high spectral efficiency : the tones fill the available bandwidth with equal and regular energy spread;

- inherent resilience to RF interference : because tones are dispatched in the spectrum according to a pattern and the shape of these paterns make it more easy to decode even with interference;

- robustness to multi-path : for similar reasons as above;

- proven in commercial technology (ex. IEEE 802.11a/g).

According to [4], the main advantages of OFDM are that it is easier to collect multi-path energy using a single RF chain, it is insensitive to group delay variations, and it is able to deal with narrowband interference at the receiver without having to sacrifice sub-bands or data rate. The only drawback of this type of system is that the transmitter is slightly more complex because it requires an IFFT (inverse Fast Fourier Transform) and the peak-to-average ratio may be slightly higher than that the one of the pulse-based multi-band approaches. Another drawback is the generation of multi-tones that requires a lot of power consumption. The distribution of tones in frequency sub-bands is shown in Figure 1.2.
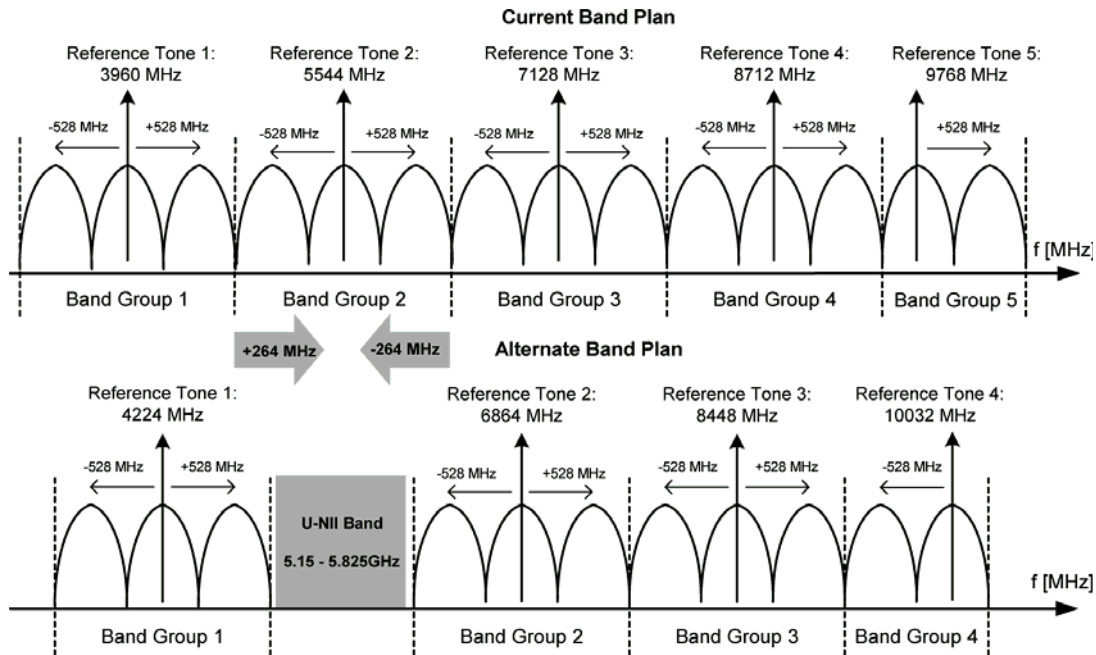
Figure 1.2: The UWB OFDM channels (see [3])

According to [4], increasing the number of tones in an OFDM system decreases the overhead due to Cyclic Prefix, or CP (cyclic prefix is the time between two OFDM symbol). On the other hand, the complexity of the Fast Fourier transform/inverse Fast Fourier transform (FFT/IFFT) block increases and the spacing between adjacent tones decreases. To provide the

best trade-off between the CP overhead and FFT complexity, the multiband OFDM system uses 128 tones. To be compliant with FCC regulations, the 10 dB bandwidth of an UWB signal has to be at least 500 MHz, as mentioned previously. This implies the use of at least 122 tones. Hence, the 128 tones are partitioned into 100 data tones, 22 pilot tones and 6 null tones. Among the 22 pilot tones, 12 are standard-defined pilot tones and 10 are user-defined pilot tones. The 12 standard-defined pilot tones are used to estimate/track phase variations due to carrier/timing frequency mismatch. To relax the specifications on the channel select filter, the tones that are at the edge of the spectrum are either null tones or user-defined pilot tones.

1.1.3   UWB FM

The UWB FM (UWB Frequency Modulation) is based on single-tone with a moving frequency for wide-band signals generation. It was developed mainly at CSEM (Neuchâtel, Switzerland) by Mr. John Gerrits and Dr. John Farserotu (see [5], [6], [7] and [8]). The main idea of UWB FM is to create a wide band signal by changing at a variable speed the working frequency of a VCO (Voltage Controlled Oscillator). The modulation is done by changing the speed of this modulation (see Figure 1.3 for the transmitter principle schematic and Figure 1.4 for the type of signals we have on this circuit) as it is done in conventional FM modulators. The receiver amplifies the UWB signal and demodulates it for obtaining the speed of the FM modulation and a second stage demodulates the symbols by demodulating the speed the initial modulation (see Figure 1.5). In a sense, UWB FM is an extension of conventional FM narrow-band modulation but with a much wider modulation depth. The main characteristics of UWB FM are the following (see [5]):

- Transmitter implementation is straightforward;

- Spectral roll-off of the UWB FM signal is very steep;

- Robustness against narrow-band jamming;

- The system works with a variety of antennas;

- Receiver requires no local oscillator;

- No carrier synchronization (as in Impulse Radio, see thereafter);

- The solution can be fully integrated and does not rely on "exotic" components (like step-recovery diodes (SRD), see Chapter 2) that need individual "tweaking".
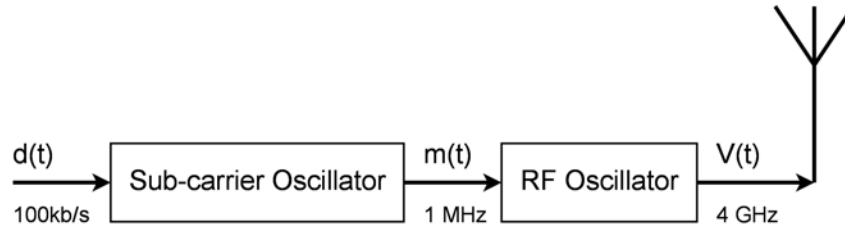
Figure 1.3: The UWB FM transmitter architecture (see [7])
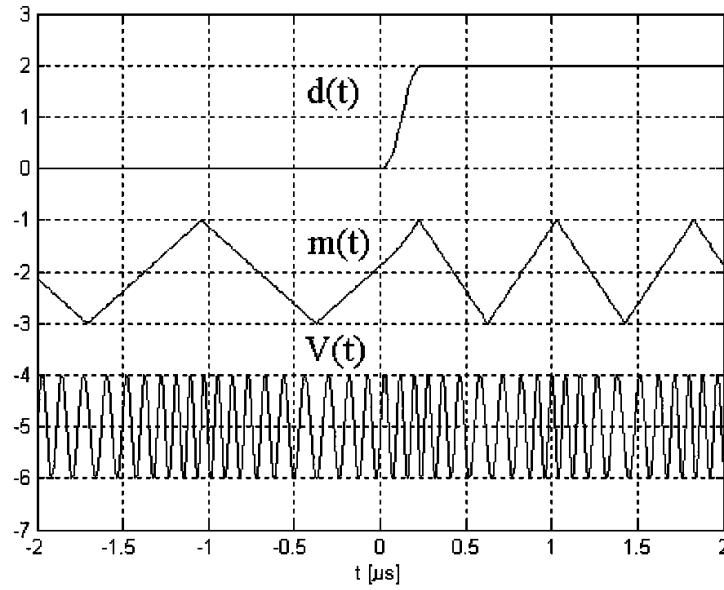
Figure 1.4: The UWB FM signals (see [6])
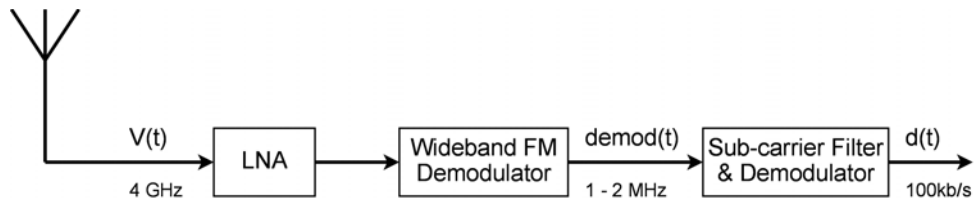
Figure 1.5: The UWB FM receiver architecture (see [5])

The UWB FM is an original way to implement UWB because it uses conventional techniques in a not conventional way. It is also relatively easy to build a UWB FM testbed in comparison to an UWB OFDM one.

1.1.4 UWB IR

UWB IR (UWB Impulse Radio) is based on very short impulse with rich spectral content for wide-band signals generation. The main idea of UWB IR is to generate a very short impulse

(few nanoseconds) that has a rich spectral content. This impulse can be a Gaussian or a square and it could be up-converted by a mixer if needed (see Chapter 3 for a more detailed study of these signals in UWB generation). This works presents three different ways to generate a UWB impulse for IR. The receiver can be a coherent one or not. The main characteristics of UWB IR are the following :

- The signal has a very wide bandwidth (it can be more than 1 GHz) that makes it takes advantage of the available wide bandwidth. The signal is robust against interference because the probability it is overlapped by another signal is weak;

- The signal has a very small power spectral density ($-41, 3$ dBm/MHz according to FCC in [9]). It is thus possible to build very low-power transmitters and to re-use frequency band already used by other narrow-band systems;

- The UWB signal is very similar to a white noise and is low-power, thus, it makes it robust to interception by a hacker;

- The UWB signal has a high temporal resolution. This makes it robust against multipath and is used to do localisation, as explained in [10] for example;

- UWB IR requires a relatively simple and inexpensive architecture for both transmitter and receiver. It is also easier to build a testbed without the need of highly sophisticated equipment.

- The transmission datarate can be easily adapted for either high or low datarate with flexibility.

The impulse radio UWB is investigated in this work because of its low-power properties and also because there are also many challenges to target in comparison to UWB OFDM which is already used in commercial products. The IR-UWB has also a strong potential for the development of ranging and localisation applications.

1.1.5   Physical layer for IR-UWB as done in our system

This section summarizes the physical layer of our future experimental setup (see Chapter 2 and further) which, as described later, would comprise several transmitters and one receiver (we will use two transmitters in Chapter 10 for our experiments). The physical layer signal generated by each transmitter is a classic IR-UWB signal with time-hopping (TH) as in [11]

(see Figure 1.6): Time is divided into frames of duration T_f and there is one pulse of duration T_p transmitted per frame.
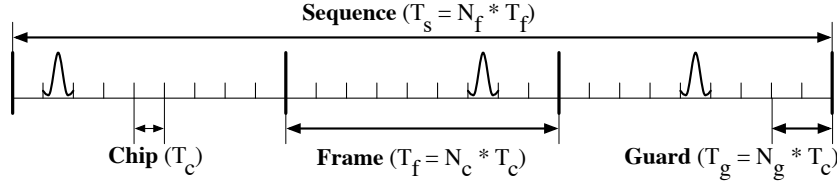
Figure 1.6: Classic IR-UWB signal [11] and its parameters: T_c is the duration of a chip, $T_f = N_c T_c$ is the duration of a frame and $T_s = N_f T_f$ is the duration of a sequence. $T_g = N_g T_c$ is guard time used to prevent ISI.

Because the pulses are sent infrequently, several transmitters can share the medium concurrently. However, the transmission time of each pulse is randomized to avoid catastrophic collisions [11]. Hence, a frame is further subdivided into N_c non-overlapping *chips* of duration T_c, where T_c is generally larger than T_p and $N_c \cdot T_c = T_f$ for each frame, these chips define the possible locations for the transmission of a pulse. To avoid inter-symbol interference (ISI) due to the multipath propagation channel, a guard time of duration T_g reduces the number of effective available positions by N_g chips to $N_c - N_g$. At last, a sequence is subdivided by N_f frames.

A so-called pseudo-random time-hopping sequence (THS) of integers uniformly distributed in $[0, N_c - N_g - 1]$ indicates which position to choose in each frame for the transmission of a pulse. Hence, each transmitter has its own THS, which is independently generated. Information is transmitted thanks to binary pulse position modulation (BPPM), where the position of a pulse carrying a one is shifted by a duration T_m and the position of a pulse carrying a zero is left unchanged. More formally, the baseband IR-UWB signal with BPPM of the n-th transmitter is

$$s^{(n)}(t) = \sum_i p(t - iT_f - c_i^{(n)} T_c - d_i^{(n)} T_m) \tag{1.1}$$

where $p(t)$ is a pulse, $c_i^{(n)}$ is an element of the THS of transmitter n and $d_i^{(n)} \in \{0, 1\}$ is an information-bearing bit.

In practice, the pulses of the IR-UWB signal generated by our transmitters are simply square pulses of duration T_p up-converted at f_c. For time-hopping, for complexity reasons, we do not generate a continuous stream of time-hopping positions. Instead, for each transmitter, we generate a sequence of length N_f of time-hopping positions and use this sequence repeatedly i.e. $c_i^{(n)} = c_{i+N_f}^{(n)}$. The aggregation of N_f frames is a sequence.

Our experimental system (based on the testbed) is packet based (see Figure 1.7). Prior to a payload of length L_{pay} pulse (or equivalently L_{pay} bit because of the binary modulation), there is a preamble of length L_{pre} followed by a so-called preamble delimiter of length L_{del}. The preamble delimiter is used to detect the beginning of the payload once timing acquisition is achieved. Notice that thanks to time-hopping, each transmitter has its own distinct preamble *and* preamble delimiter. Indeed, the preamble delimiter uses another THS than preamble. Hence, a receiver can detect and acquire the timing of the packet from a given transmitter while another transmitter is active.

L_{pre} (32*N$_f$)	L_{del} (8*N$_f$)	L_{pay} (127 bytes)
Preamble	Preamble delimiter	Payload (Binary Pulse Position Modulation)

Figure 1.7: The structure of the packet sent by the transmitter of interest is loosely based on the IEEE 802.15a standard [12]. It contains three parts: (1) a preamble for packet detection and timing acquisition, (2) a preamble delimiter is used to detect the beginning of the payload and (3) the payload. N_f is the length of a sequence.

1.2   About this work

1.2.1   The early beginning

This work describes a research about Ultra-Wide Band Impulse-Radio communications made at EPFL (Ecole Polytechnique Fédérale de Lausanne) with the support of MICS (Mobile Information and Communication Systems). When we started this work in 2006, it was first for designing and realising an UWB testbed during a summer project for helping a research group in UWB communication in the laboratory LCA2 of Prof. Jean-Yves Le Boudec to validate experimentally theoretical results about UWB communications. This summer project evolved to a master diploma project from October 2006 to February 2007 done by the author; this project was to design the UWB LNA described in Chapter 7. The PhD started officially in January 2008 and finished in February 2012. The complete schedule of this work that shows its evolution is shown in Figure 1.8.

1.2.2   Organisation and objectives of the work

As most aspects of UWB are still under development, a lot of work is required to move from laboratory to consumer products. The challenges when we started this work were the following :

- to reduce the size: many UWB devices made of discrete components were huge (in 2006) and very expensive. There was no way for a laboratory to obtain easily them for tests and validation of equipment. More important, it was not possible to know and parameterize the hardware for testing in a general way the UWB transmission. This was a strong motivation to design a UWB testbed;

- carrierless and asynchronous IR-UWB : Because of the wide bandwidth of UWB signals, there is no single carrier as it is only short impulse and/or multitone. This means that there is no possibility to synchronize the reception of the signals on a reference, so we need a kind of modulation that can help for this synchronization;

- to redesign all communication protocol (time-hopping vs. frequency hopping (or pattern hopping in the case of OFDM [13])): In a conventional radio, the frequency hopping technique is used to adapt the transmission to the condition by changing periodically the frequency of the carrier. For example, Bluetooth has about 80 channels around 2.45GHz (see [14]) and, if one is already used or shows a bad transmission quality, it jumps to another channel to find a better one. In UWB, on the contrary, the frequency hopping has no sense and the channels are defined by using different time slots in the occurrence of the signals. This is called time-hopping;

- to be robust to interference : the interference is caused by similar UWB devices and all other radio devices (most of them are narrow-band). Interference caused by similar UWB devices is called *multiuser interference* (or MUI). As the UWB is by nature low-power, it is a challenge to make it robust to narrow-band interferences that are by nature high-power. The UWB communication has to be robust to MUI from other neighbouring UWB transmissions;

- to be reliable: Error detection and correction has a cost in terms of power and datarate. The transmission and detection of the signal and its processing should make it as efficient as possible.

- to manage complexity and flexibility: The UWB network can be complex in case of wireless sensor networks for example and it should adapt easily to the changes of this network. This is mainly the task of communication protocols and algorithms. The flexibility applies also for the hardware architecture as we want to explore and test for the best solution.

- to be secure : as security is a threat in communication, the transmission of data should be safe in order to protect the communication against spy and/or attacks.

Succeeding in these challenges requires a narrow collaboration between telecommunications experts for new protocols designs, algorithms for detection and security conception, performance evaluation of whole systems on one side and electronic and microwave experts for implementing transmitters, receivers and complete integrated systems with low-power, simple, low-cost and reliable circuit designs. This work is motivated by the first point of the list because without any testbed, no research can be done on the further points. When we have a testbed that works and fulfils regulations, we can validate and demonstrate strong results, as presented for example in [15, 16, 10], that focus on the further points of the list, as done in Chapter 10. The results of this part of the work are presented in Part II and partially in Part I.

The second motivation of this work is to design an extremely low-power UWB transmitter in order to be as much as possible close to the market. As a low-power UWB receiver that works very well is described in [17], we focus on a very low-power UWB transmitter that could be compatible with both the testbed and this receiver. The results of this part of the work are presented in Part III.

Finally, when we started to work on UWB communications, in summer 2006, there was (to the best of our knowledge) no publication available about building a complete UWB testbed with only commercial off-the-shelf discrete components or such that anyone could build his/her own testbed with only average knowledge in electronic design. This need concerns mainly several researchers who have a profile strongly oriented to communication theory, mathematics or computing and who want to validate experimentally their research results but who do not necessarily have the knowledge on electronic and microwave techniques to design themselves a testbed. As UWB is a very challenging topic even for experienced electronic and microwave engineers, this work focuses, in addition to present new and original results, to give all information required by anyone to build their own testbed and to modify it with a high probability

of success. This knowledge was gained by working and learning from several of the most experienced and skilled workers and researchers at EPFL who kindly take the time to share their knowledge with the author. This knowledge is essential to anyone who wants to build the testbed because it concerns principles and working rules about practical things that can make a circuit to work perfectly if they are carefully followed or to be deceptively not working if they are not. This knowledge could seem obvious for trained electronic engineers but for researchers from other fields, it is very difficult to know exactly how to do properly things such that they work on the first try. To prevent any difficulty, we give a complete practical guide in Appendix C on how to build all the parts of the testbed.
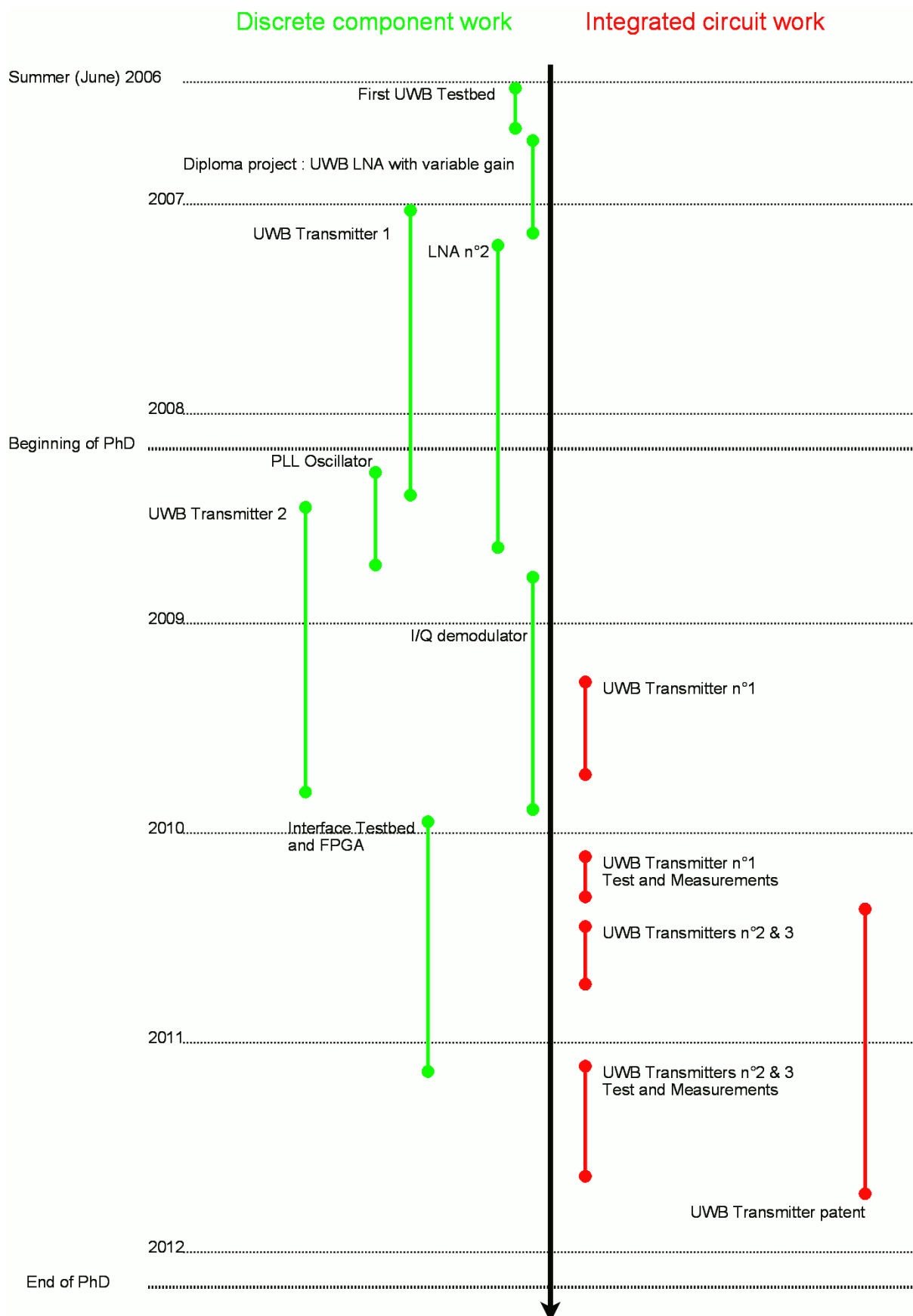
Figure 1.8: The schedule of the work

Chapter 2

A first prototype of UWB testbed

2.1 Introduction

The main objective of our first experimental hardware testbed, as described in this chapter, is extensibility, modularity and flexibility. We want the ability to easily exchange components in the RF chain. We also want full access and control of the parameters of the physical layer, and the possibility to easily implement and test new algorithms at the receiver by simply connecting independent modules. Later, when the testbed architecture will become more mature and according to results obtained until that, we will re-design it by using single modules for transmission and reception. The design of these modules will be described later in Part II. Concerning the signal processing, it should be easy to implement and test new algorithms at the receiver, either by programming an FPGA for real-time processing, or by capturing signal traces that can be then used offline on a separate computer with an algorithm implemented in a high-level programming language. Challenges such as low power consumption or integration are definitely important but are not primary objectives for the testbed. This is why most of the RF elements are either off-the-shelf components or are built with discrete-components. Because it is intended to be used by researchers who work more in telecommunication rather than in electronic engineering, we design the parts of the testbed such that they do a task that can be understood at a system view level without the need to know the electronic detail of the implementation.

An overview of our experimental testbed with its characteristics is shown in Figure 2.1. In this view, we see the digital signal processing part that is given as is on the top and the RF

analog part that we have to design and build on the bottom. We focus only on the RF analog part of the testbed in this work; the FPGA used for generating the physical layer of the UWB and for decoding the received signal is in fact the same device but presented as two different ones for clarity of the figure.
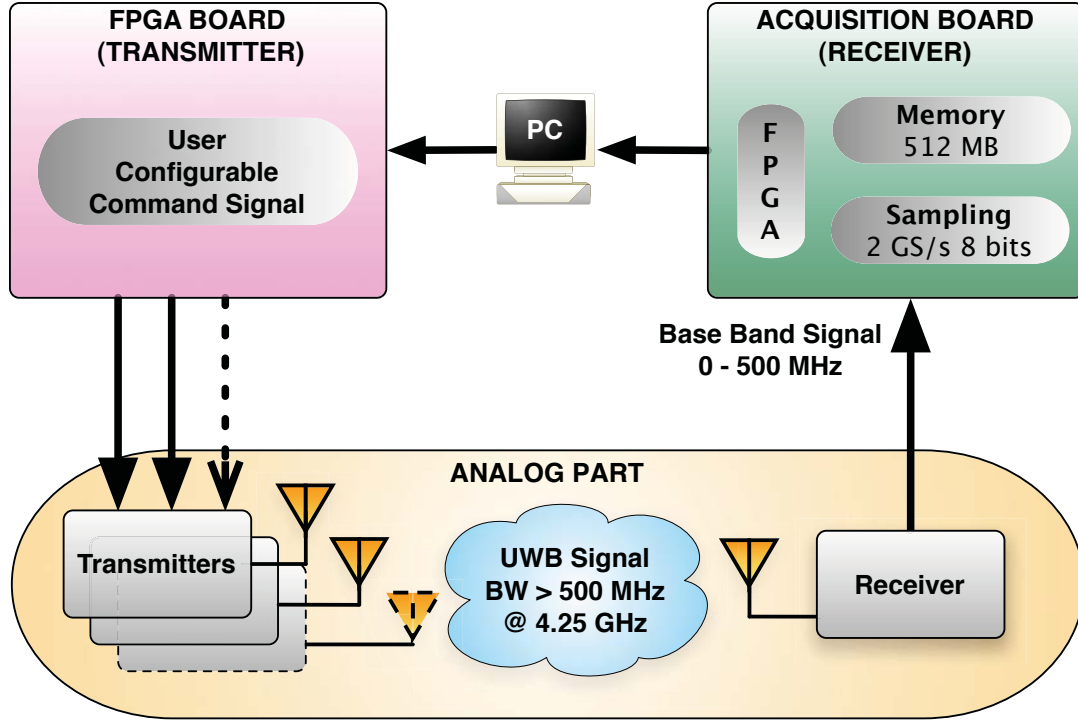
Figure 2.1: Overview of the testbed: an FPGA board controls the transmitters with the desired signal physical layer characteristics (see Section 1.1.5). The receiver amplifies, filters and down-converts the received signal to the baseband. The acquisition board of the receiver samples the baseband signal and stores this signal trace in DRAM on another FPGA. The signal trace is later offloaded to a PC for offline processing.

For implementing the RF analog part of the testbed, we consider the preliminary work made before the beginning of this work in 2006 in our laboratory (LCA-2). This preliminary work includes a master project about SRD-based (Step Recovery Diode) UWB transmitter (see [18]) and preliminary research on available components and UWB receiver architectures (see Appendix I). The prime objective of this first testbed is to be able to transmit and to receive an UWB signal in order to build a simple system on which we can rely for further improvements. We do not focus, at this stage, on power performance or any standard regulations. According to Appendix I, we target initially the frequency range from 4.06 GHz to 4.56 GHz and thus a bandwidth of at least 500 MHz. At the end of this chapter, we expose several conclusions from this initial testbed on which we will build the foundations of our final UWB testbed, presented

in Part II, that we called *U-Lite*.

2.2   UWB Transmitter (or Pulser)

The UWB transmitter (also called "pulser" in this chapter) is the most critical part to design because it has to fulfil several challenging specifications in addition to be compliant to official regulations. Designing a good UWB Transmitter is also a challenge because there are many ways to implement it some of them are easier than other, each of them having its own strength and drawback. In our case, for our first UWB testbed, we decided to focus on the SRD diode technology for UWB impulse generation because of its very low cost and simplicity but also to benefit from already made research and experimentation on this technique in our laboratory.

2.2.1   Working principle - analogy with the engine

The working principle of the pulser is to convert a stream of binary impulses that come from the FPGA board into very short RF impulses - that thus have a very wide bandwidth - which are filtered and radiated by an antenna. The heart of the pulser is a Step Recovery Diode (SRD), a special diode whose behaviour is described in detail in the article [19]. This diode has the ability to accumulate electric charges into its junction when it is conducting. While a conventional diode stops to conduct almost instantaneously when the voltage applied across its terminal vanishes or changes polarity, the SRD diode has to evacuate the accumulated charges in order to stop conducting, which will take a longer time (several nanoseconds) to do. If, during this short time, the voltage across its terminal becomes high, then a reverse current will flow into the diode until it stops conducting. This will create into the circuit a short and powerful impulse with a complex spectral composition that can be used to generate the UWB impulse if it is conveniently shaped by a filter.

An analogy between the SRD pulser and the thermal engine can help to understand better how it works. In this analogy, the inductor plays the role of the intake cam, the capacitor plays the role of the exhaust cam and the SRD diode the role of the piston. The exciting impulse that comes from the FPGA is a square and symmetric signal (in fact we add a small offset in order to compensate the voltage drop across the terminals of the diode and thus to increase the power of the signal) that is shaped by another circuit described later. When the diode stops conducting corresponds to the spark of the light. The pictures come from the book [20].
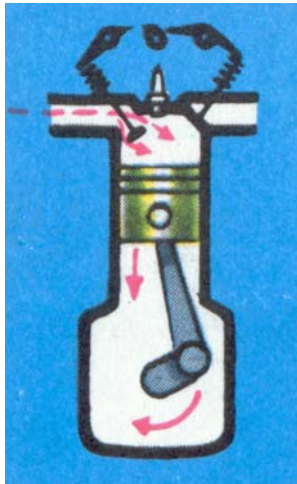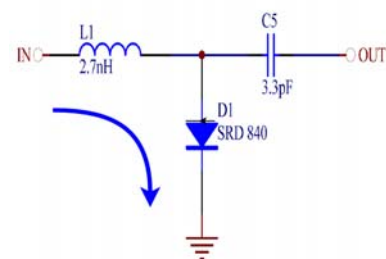
The intake cam opens for bringing the air and petrol mixture into the cylinder.

The positive exciting impulse (low frequency spectrum) goes across the inductor but is blocked by the capacitor. It arrives across the SRD diode which starts to conduct and to accumulate electric charges into its junction.

Table 2.1: Engine analogy : intake
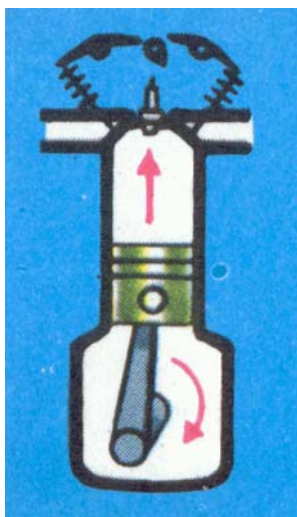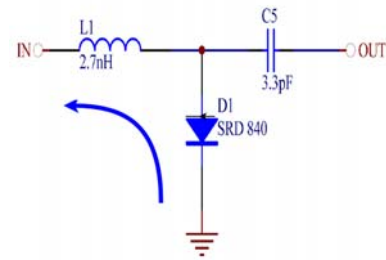
The intake cam closes and the piston rises and compresses the mixture.

When the exciting impulse becomes negative, a current goes across the SRD diode and removes the charges accumulated into the junction. The voltage across diode's terminals rises according to the time constant of the circuit made of the inductor L and the dynamic resistance of the diode and the generator.

Table 2.2: Engine analogy : compression
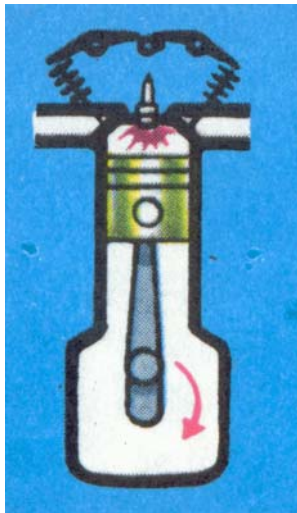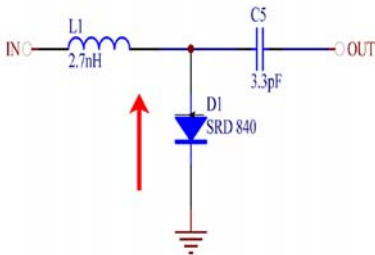
| | When the mixture is compressed, the light produces the spark and the mixture explodes. The piston is violently repelled. The voltage across diode's terminals is high. When the charges that were accumulated into the diode's junction are completely removed, the diode stops suddenly to conduct and a signal with complex and rich spectral components is generated. | |

Table 2.3: Engine analogy : light
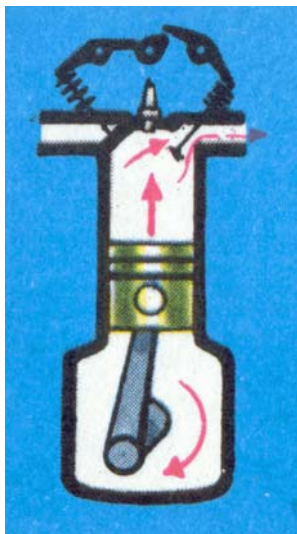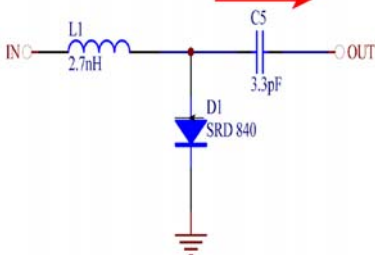
| | The piston rises, the exhaust cam opens and the gases form the burnt mixture are removed from the cylinder. The signal with rich and complex spectral components (high frequency spectrum) goes across the capacitor to the antenna. The inductor stops this signal and avoids it to come back. | |

Table 2.4: Engine analogy : exhaust

When designing the pulser, we focus on the output signal's energy and its spread into the spectrum. We try as much as possible to have energy into the bandwidth from 4.06 to 4.56 GHz. If it is not possible, we can use a mixer to frequency shift the signal but this solution is heavy and should be ideally avoided.

2.2.2   Prototype nᵒ 1

For the first prototype, we consider the articles [19] and [21] that described SRD-based UWB transmitter in addition of the work [18] which made a good introduction to SRD technology. This transmitter is first designed in ADS for further simulations, as shown in Figure 2.2.
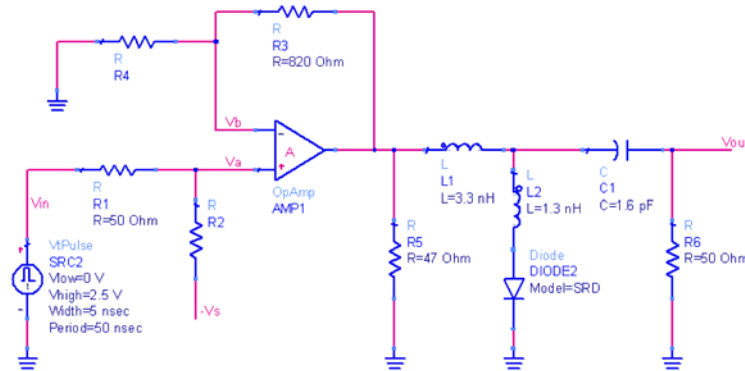
Figure 2.2: The Prototype nᵒ 1 of UWB transmitter based on SRD (see [18])

Although this pulser has on the paper several drawbacks that will be corrected in prototype nᵒ 2, in practice, it works well and is sufficient to do measurements and to test the behaviour of components. The spectrum measured at the output of the pulser is shown in Figure 2.3.
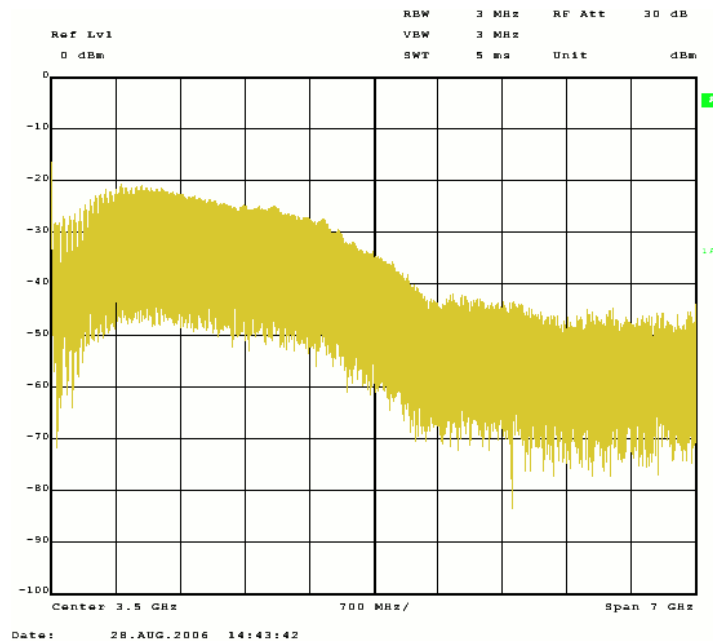
Figure 2.3: The spectrum obtained with SRD Prototype nᵒ 1

We see in this spectrum that most of the power is focused in the 1 to 2 GHz frequency range. The impulse generator emulates the FPGA board; at this stage, the driving impulses last 10 ns and are repeated every 100 ns with the high level at 2.5V (the FPGA board cannot give higher voltage) and the low level at 0 V. We can use a mixer to up-convert the UWB pulses in the 4.0 to 4.5 GHz frequency range, as shown in Figure 2.4.
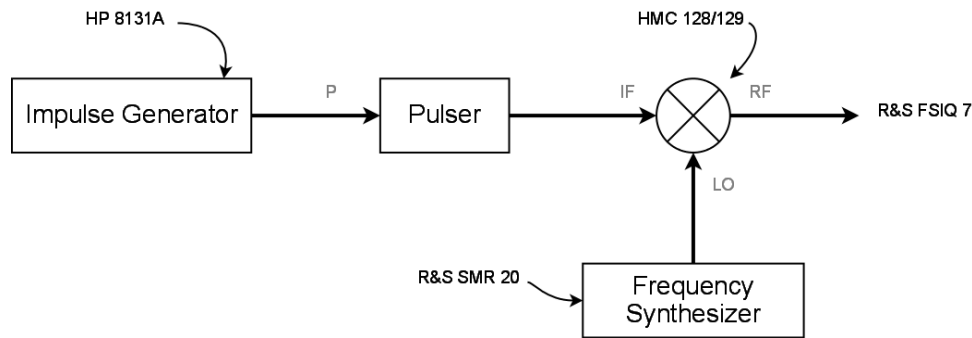
Figure 2.4: SRD Prototype n⁰ 1 with up-conversion

The signals measured in this experiment are shown in Table 2.5.

Mixer	Power [dBm]	Frequency [GHz]	Comments
P	-	-	Impulse signal, see text
IF	-21	$\approx 0,977$	UWB spectrum, maximum value
LO	$+15$	$3,800$	Sine wave
RF	$\approx -32 \, (\approx -29)$	$\approx 4,270 \, (\approx 4,270)$	UWB spectrum, maximum value

Table 2.5: Up-conversion with the mixer HMC 128 (129)

As we have a wide band spectrum, we only show the maximal value in order to have an idea of the power of the signals. This power is approximately constant in neighbouring frequencies. For shifting the frequency of the maximal power in the frequency range of interest, we use a mixer for frequency up-conversion. We use two types of mixers from Hittite Corporation that can work in the 4.0 to 4.5 GHz frequency range: the HMC128 and HMC129; the results of these up-conversions are shown in Figures 2.5 and 2.6 respectively.

In these Figures, we see that the output is almost the same, although there are peaks at -30 dBm for the HMC129 mixer. A more detailed calculation could be made to determine which mixer is the best one but, in practice, it is better to wait on the prototype n⁰ 2 to decide, provided we effectively choose to up-convert the signal.
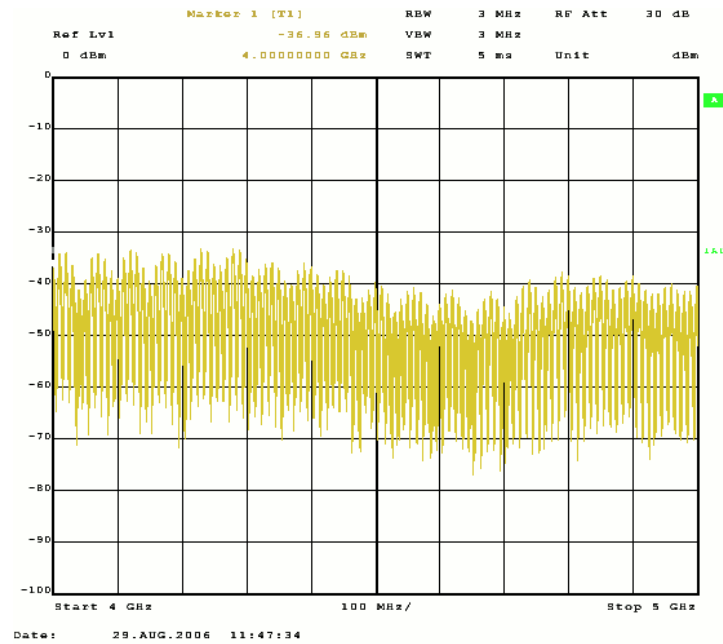
Figure 2.5: Spectrum of SRD Prototype n° 1 with up-conversion with HMC128 mixer
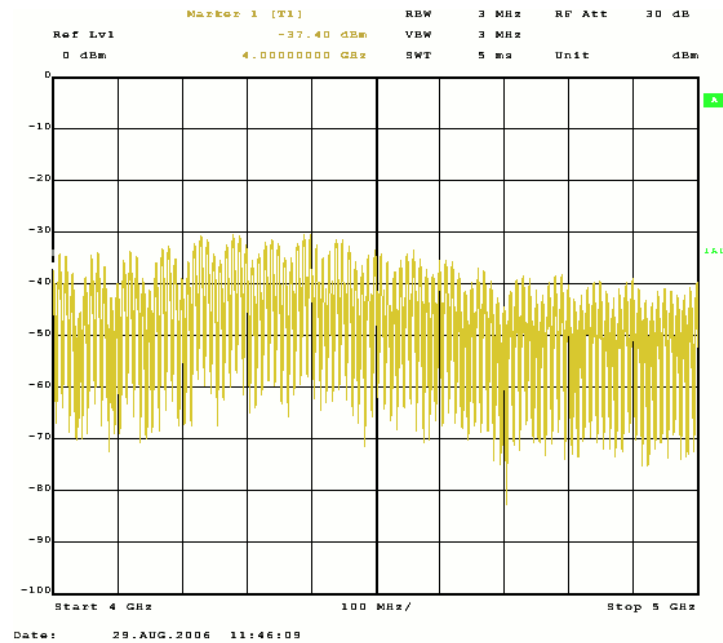
Figure 2.6: Spectrum of SRD Prototype n° 1 with up-conversion with HMC129 mixer

2.2.3   Prototype n° 2

The prototype n° 2 is similar to the prototype n° 1, excepted that the choice of component was revised and the PCB (Printed Circuit Board) layout was optimized for the high frequency sig-

nals of the circuit. In addition, the PCB is electro-chemically gold plated by hand with gold cyanide (a very poisonous product to use with extreme care) in order to protect it against corrosion and to avoid the use of a varnish that could modify the permittivity of the PCB material. In a first step, we simulate the circuit with ADS with almost ideal components. By almost ideal components, we mean that non-ideal components that have a strong influence on the behaviour of the circuit - this means L_1 and $DIODE1$ in Figure 2.7 - have been modelled by ourselves as much as possible with ideal components given in ADS library. In further simulations, we will even use more advanced models that are given by components manufacturers. In a second step, we built the pulser prototype n° 2 and validate experimentally that the UWB impulses corresponds to the simulations. As the pulser will be driven by a FPGA board, we should ensure that the driving signal for the pulser will be close to the ideal signal we used in simulations. This is the role of the driving circuit described thereafter in Section 2.2.8. The model for the SRD diode given by its manufacturer is shown in Figure 2.7.
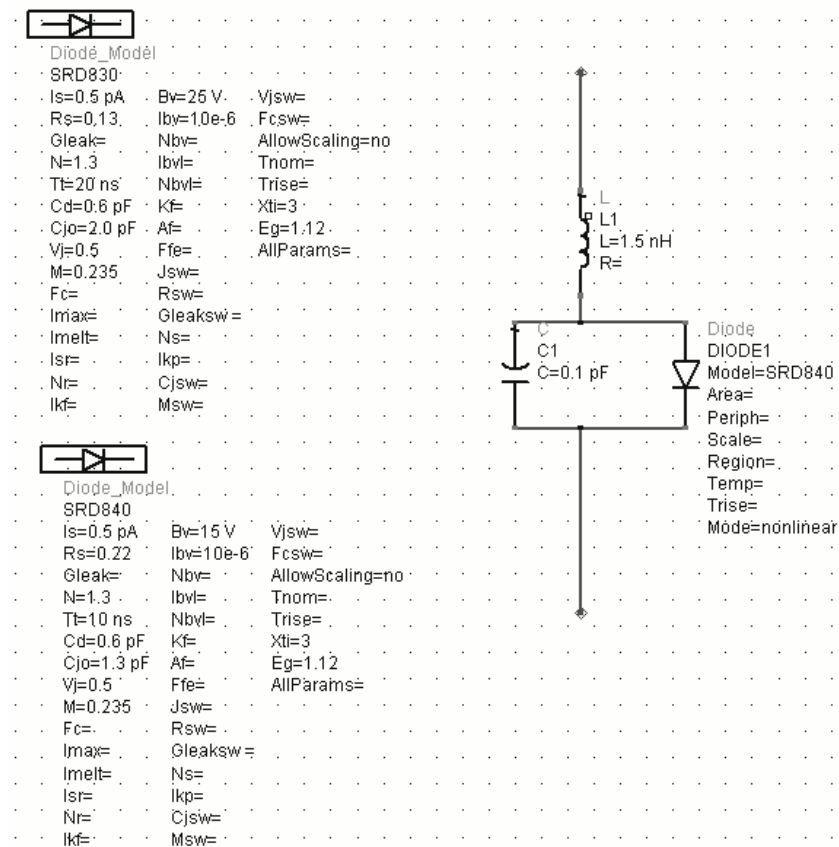
Figure 2.7: ADS model of the SRD diode for Prototype n° 2

2.2.4   Simulations

The ADS simulations take most of the time of the design because the pulser circuit is very sensitive to component value variation. This is also the PCB layout and construction is very important in order to remain close to the ideal scenario we consider in simulation. The schematic in ADS simulation environment is shown in Figure 2.8.

Figure 2.8: ADS simulation of Prototype nº 2

With this configuration, we obtain the spectrum shown in Figure 2.9.

Figure 2.9: Spectrum obtained by ADS simulation of Prototype nº 2

We see that the power available in the 4.0 to 4.5 GHz frequency range is about -35 dBm

for each peak. We should notice that the power emitted in the bandwidth is the integral (or addition if peaks are discrete) of the power carried by each peak in the bandwidth. From simulation results, we modify the schematic for prototype nᵒ 2 as shown in Figure 2.10.
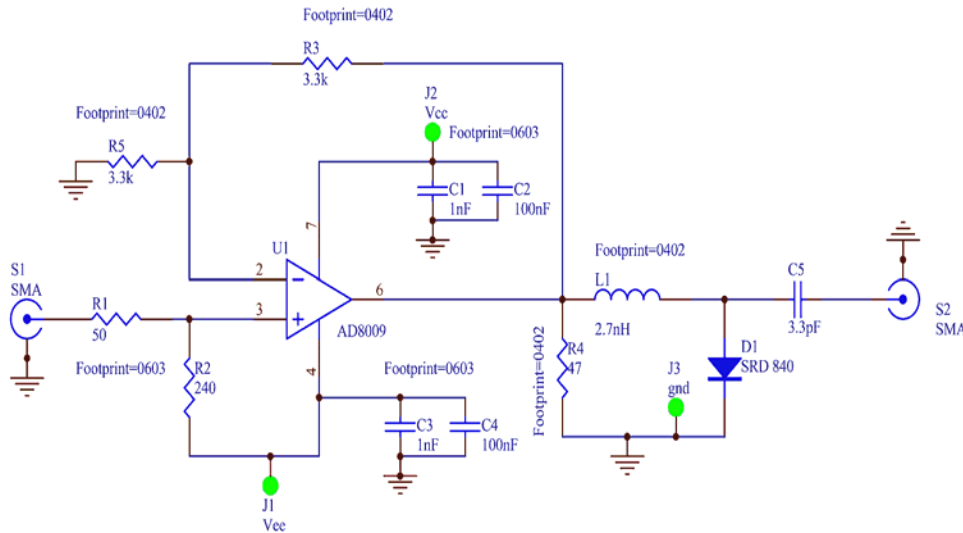
Figure 2.10: Schematic of Prototype nᵒ 2

2.2.5 Choice of components

The components that are on the path of the RF signal (thus L_1, R_3 and R_4) must be of SMD type with a size of 0402 in order to be sure that their resonant frequency is much above the 5 GHz of the output signal (we consider 5 GHz as a safety margin). The specifications of the manufacturer guarantee a resonant frequency of 10.4 GHz. The diode D_1 has a fixed package size (SOD 323). The other components have a more conventional size (0603). The circuit is powered with a symmetric power supply of ± 5 volts that should not be exceeded.

2.2.6 Stripline calculations

The tracks that carry the RF signals are transmission lines of type microstripline with ground plane and matched at 50Ω; the PCB material is Duroid (RO4003B) from Rogers Corporation. The microstripline is designed according to the Matlab file given in Appendix A.1.1. For more detail about theory and design of transmission lines we can refer to the books [22] and [23].

We obtain a width of $w = 48.7$ mils that are rounded to 49 mils, or approximately 1.23 mm.

2.2.7   PCB of the pulser

The PCB of the pulser (prototype nº 2) is shown in Figure 2.11. The PCB is doubled-sided and the bottom side is a ground plane that fills all the surface of the PCB for shielding and for fulfilling microstrip geometry requirements. There are several vias used to connect to ground with the smallest as possible amount of parasitic inductance (in practice, so many vias are not really required but at the time we would exclude any unexpected problem because we have planned a demonstration).
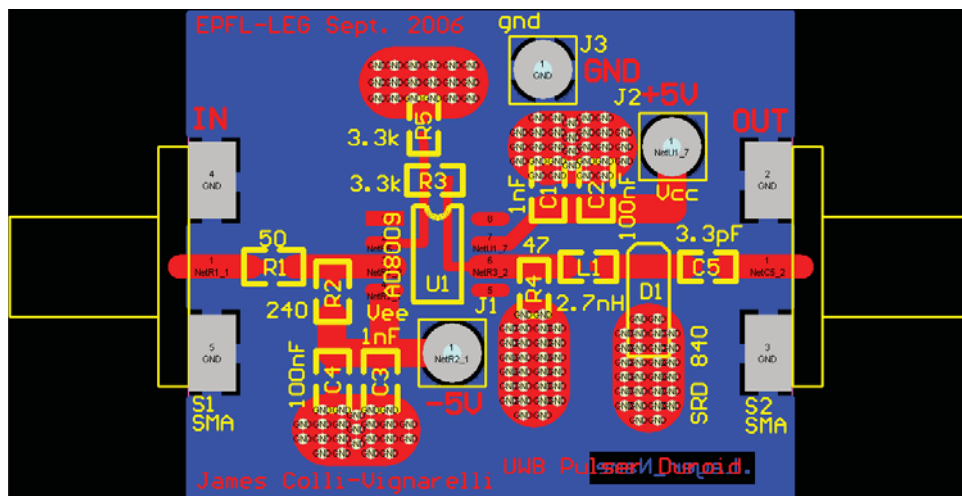
Figure 2.11: The PCB of the pulser on Duroid

The pulser circuit when finished is shown in Figure 2.12
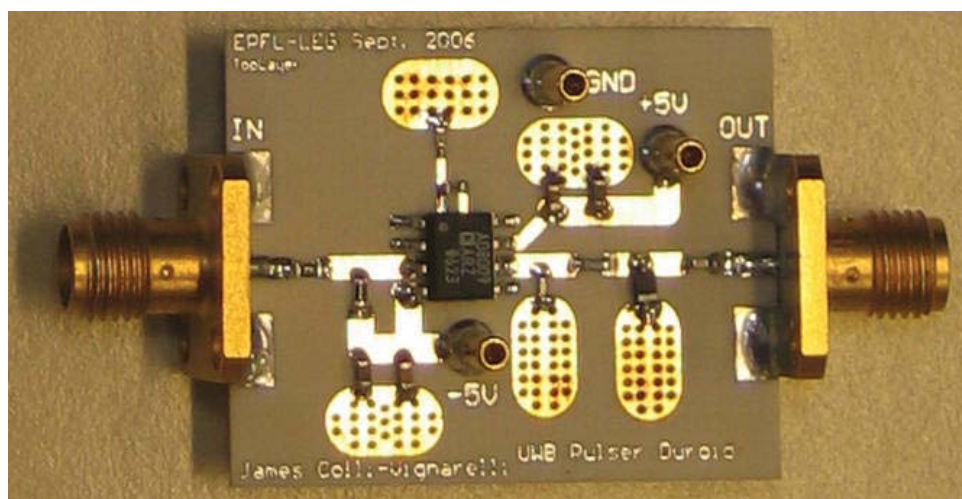
Figure 2.12: The pulser circuit

2.2.8   Driving circuit

The driving circuit is used to amplify and to adjust the level of the bit stream coming from the FPGA board in order to drive the pulser circuit such that the generated UWB impulses are of optimal shape. It is auxiliary board connected to the pulser with an SMA connector and made in FR-4 PCB material. The PCB holds four units for driving four independent UWB channels. The schematic of one channel is given in Figure 2.13.
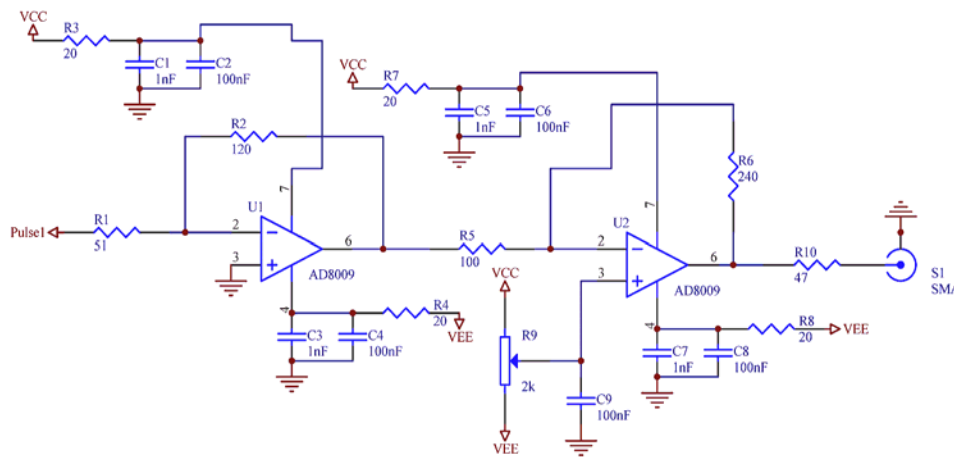
Figure 2.13: Schematic of driving circuit (one unit)

The circuit is made of two inverting amplifiers that have a gain of about 5.7 (this is because the impedance matching resistor introduces a division by 2 of the voltage at the input and at the output); the real gain is thus estimated to be about 1.41. The second amplifier allows to add an offset with R_9 as we noticed that a small offset helps to improve the pulser performance by compensating the voltage drop across the diode.

The power supply in designed with care because the driving circuit can oscillate if they are badly decoupled. The voltage drop on the resistors is small but we can increase the power supply to ± 5.5 volts without any problem. For example, when we designed this circuit on the prototyping board, it started to oscillate only because the decoupling capacitors were not close enough to the integrated circuit pins. The PCB of the Driving circuit is shown in Figure 2.14 with the decoupling problem solved.

When we experiment the driving circuit on the pulser, we noticed that the FPGA board is able to do as well with the driving circuit as without. A measure of the signals from the driving circuit shows that the improvement made with the amplification is penalized by the shape of these signals due to the slew rate of the amplifiers. We thus decided to remove the driving circuit from our experiment and to let the FPGA board to drive directly the pulser as the
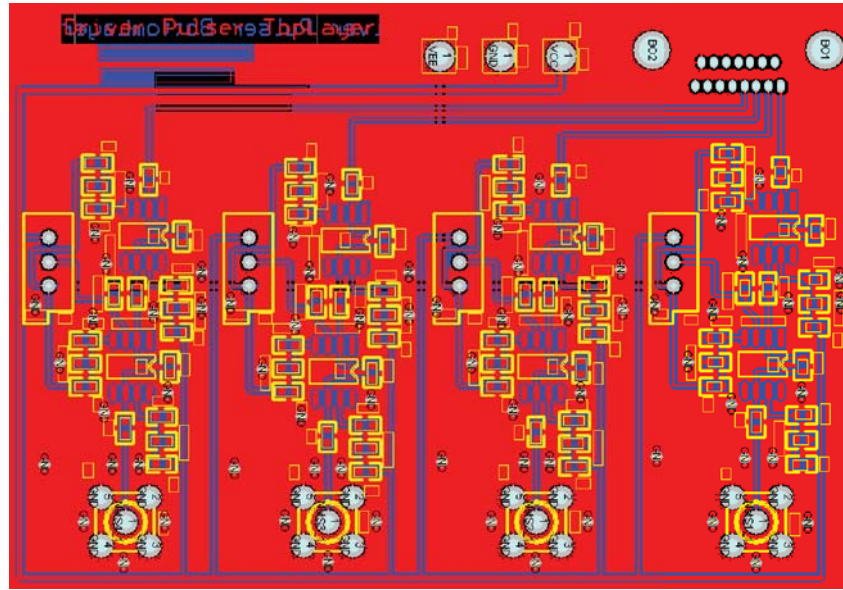
Figure 2.14: PCB of driving circuit (one unit)

driving circuit brings no overall improvement of the UWB generated signal quality. We discuss at the end of this chapter what are the improvements that could be done on the couple driving circuit - pulser.

2.2.9 Measurements

According to what was said previously, the circuits are measured driven directly by the FPGA board without the help of the driving circuit. This is because we want to have final results as they will appear in the testbed at the end of the project for the demonstration. By successive experimentations, we decided to represent a "bit" by sending 5 pulses each of 12 ns of duration every 24 ns to the pulser. These 5 impulses allow the pulser to give the best use of the energy after a long inactive time (about 800 ns) without the need to fill the silent time with undesired signals (see Figure 2.17 for an overview of the timing of UWB signals). The spectrum at the output of the pulser driven by the FPGA board is shown in Figure 2.15.

We see that the spectrum shape is similar to the one obtained with prototype n° 1 and that the power in the frequency range of interest (blue arrow at 4 GHz) is close to the power obtained by simulation. However, we also measured the spectrum of the pulser when it is driven by a continuous stream of driving impulses (in the contrary of the FPGA that has burst driving impulses) in order to see if there is a difference because of this difference of the timing of driving signals due to way the spectrum analyser calculate the power by doing an average. The
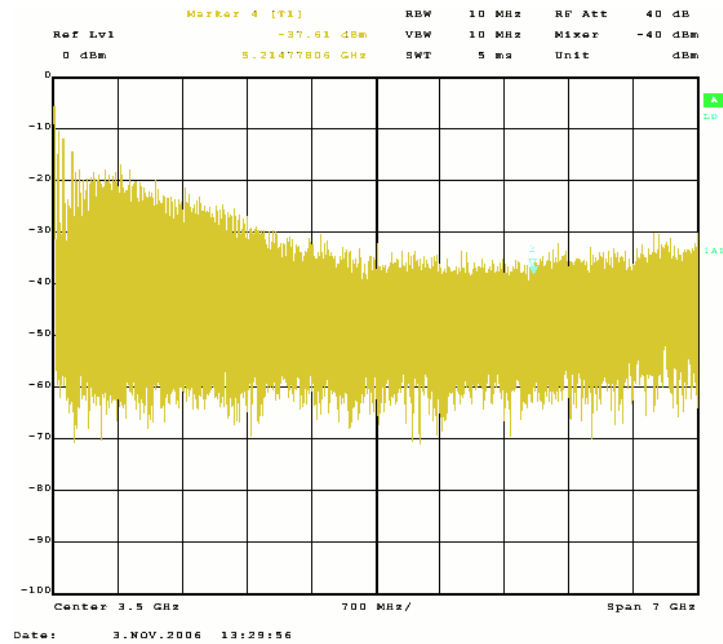
Figure 2.15: Spectrum of prototype nᵒ 2 when driven by the FPGA

spectrum at the output of the pulser driven by the Agilent 33250A function generator is shown in Figure 2.16. We see that the spectrum is almost the same as the one obtained with the FPGA board for driving the pulser.
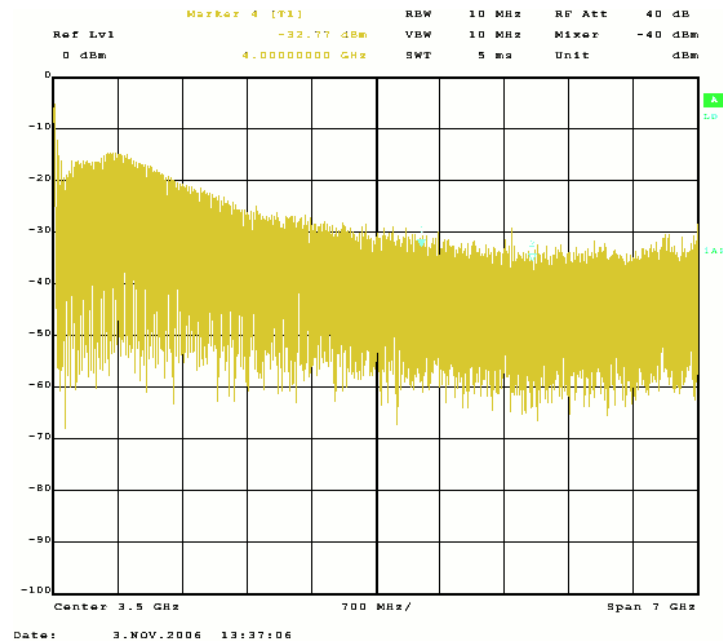
Figure 2.16: Spectrum of prototype nᵒ 2 when driven by the function generator

We validate here the very good quality of the components models used in simulations (which was not given at all in advance), and the correctness of the design calculations. The same signal is shown in time domain in Figure 2.17.
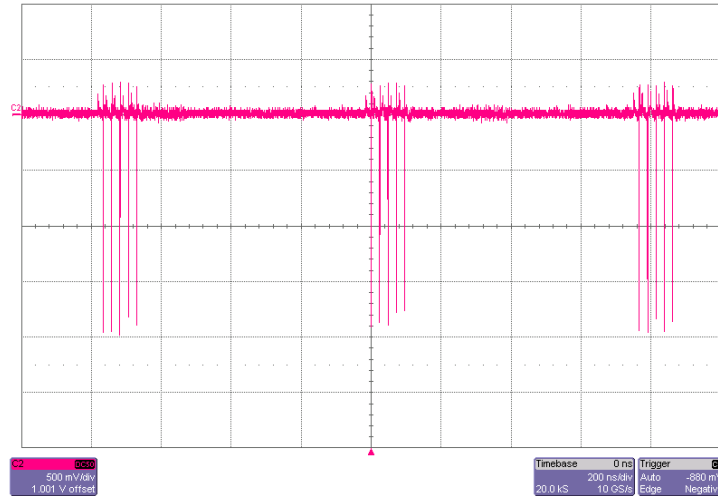
Figure 2.17: Signal of prototype nº 2 when driven by the FPGA

We notice the amplitude of the signal (almost 2 volts) and the short duration of impulses (< 2 ns). This demonstrates why these signals are called *Impulse Radio* and *Ultra-Wide Band*.

Finally, the whole transmitter is shown in Figure 2.18.
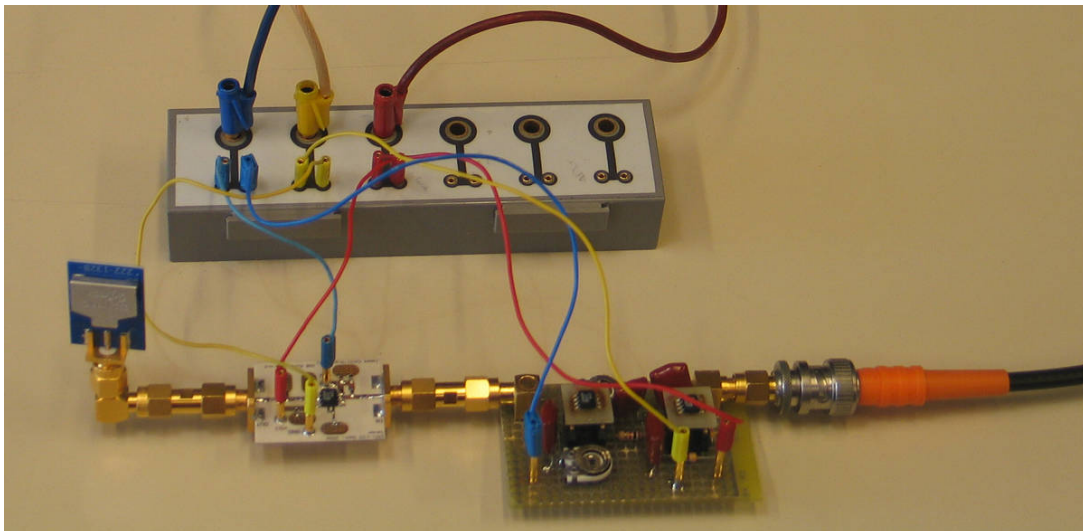
Figure 2.18: The pulser circuit

2.3   UWB receiver

2.3.1   Receiver description

The receiver is essentially made of two parts. One part is dedicated to amplify and filter the received UWB signal from the antenna, the other part is dedicated to down-convert the amplified UWB signal in the base band (from 0 to 1 GHz) for the digital acquisition by the FPGA board ADC. The digital signal processing made on the FPGA takes into account the frequency down-conversion. The architecture of the receiver is shown in Figure 2.19.
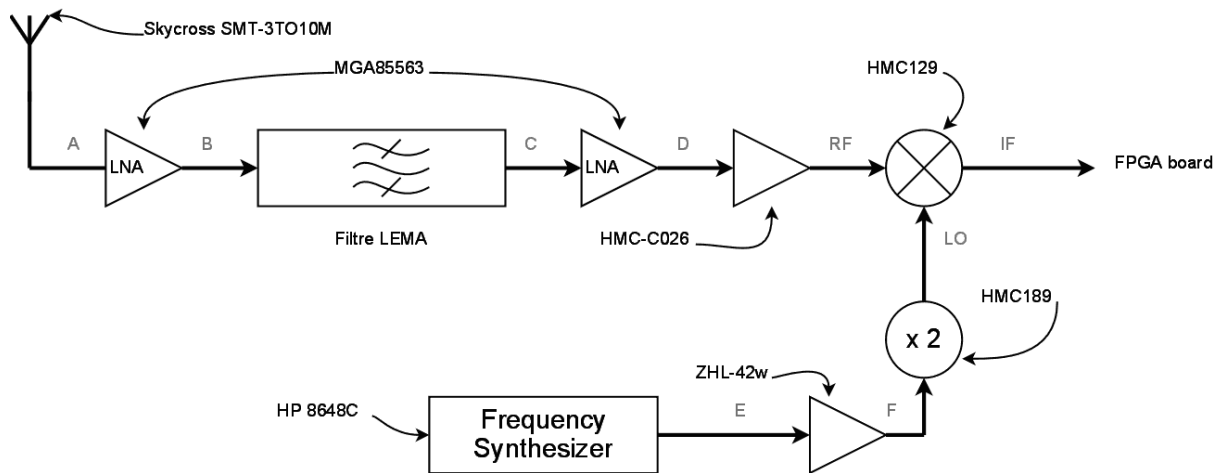
Figure 2.19: Receiver architecture

This architecture, although it works very well, will be improved later according to the experimental results.

Amplification and filtering

The UWB signal is received by the antenna, which is specially designed for wide-band applications. The signal is filtered and amplified by two LNAs. The filter was designed by our colleagues at LEMA (Laboratoire d'Electro-Magnétisme et d'Acoustique). It is a band-pass filter with cutting frequencies at 4.0 and 4.5 GHz. At point C (see Figure 2.19), the signal is powerful enough and the noise small enough by the filters and LNAs for being strongly amplified by a high-gain power amplifier with average noise figure. The input of the mixer requires a signal that is as powerful as possible because the mixer introduces a loss of power (this is a passive mixer). The LNAs have a gain that remains almost constant in the frequency range of interest.

Frequency shifting (down-conversion)

The frequency down-conversion is made with a passive mixer and a local oscillator. The oscillator has to generate a 4.0 GHz sine wave in order to shift the frequency range from 4.0 to 5.0 GHz into the base band from DC to 1.0 GHz. As it was difficult (in 2006) to find on the market a programmable oscillator able to deliver a sine wave at such a frequency with precision, we decided to use an oscillator that generates a 2.0 GHz sine wave and to use a passive frequency doubler. As the mixer requires a high level of power on its LO input and because the doubler is passive, we add a power amplifier with a gain of 30 dB in order to compensate the losses.

Here, we explain mathematically how a signal is shifted in the frequency domain by mixing it with a sine wave of fixed frequency. This process works for down-conversion as well as for up-conversion. Let V_{LO} and V_{RF} be two sinusoidal signals applied on the mixer's inputs that correspond to the local oscillator and RF received signal respectively. We assume that the received signal is a pure sine wave but, by applying the Fourier transform on the UWB signal, the same principle holds.

$$
\begin{aligned}
V_{RF}(t) &= \hat{V}_{RF} \cdot \sin(\omega_{RF}t) \\
V_{LO}(t) &= \hat{V}_{LO} \cdot \sin(\omega_{LO}t)
\end{aligned}
$$

where:

- $\omega_{LO} = 2\pi \cdot f_{LO}$ that represents the operating frequency of the local oscillator and

- $\omega_{RF} = 2\pi \cdot f_{RF}$ that represents the frequency of the received RF signal.

The mixer performs the mathematical multiplication of the input signals as follows :

$$
V_{IF}(t) = V_{RF}(t) \cdot V_{LO}(t)
$$

By using the following trigonometric identity:

$$
\sin(A) \cdot \sin(B) = \frac{1}{2} \cdot [\cos(A - B) - \cos(A + B)]
$$

the voltage at the output of the mixer V_{IF} is expressed as follows :

$$
V_{IF} = \frac{\hat{V}_{RF} \cdot \hat{V}_{LO}}{2} \cdot [\cos(2\pi(f_{RF} - f_{LO})) - \cos(2\pi(f_{RF} + f_{LO}))]
$$

This expression shows that there are two frequency outputs: $f_{RF} - f_{LO}$ and $f_{RF} + f_{LO}$. By only considering the difference (or equivalently by rejecting the sum with a filter), we can down-convert the received signal.

2.3.2   Low Noise Amplifier (LNA)

The LNAs are designed and built by ourselves for this experiment, while the other components are directly available on the market and mounted on evaluation board by the manufacturer (as it is the case for Hittite's circuits). The LNAs are designed with a MMIC from Avago, the MGA85563, as shown in Figure 2.20.
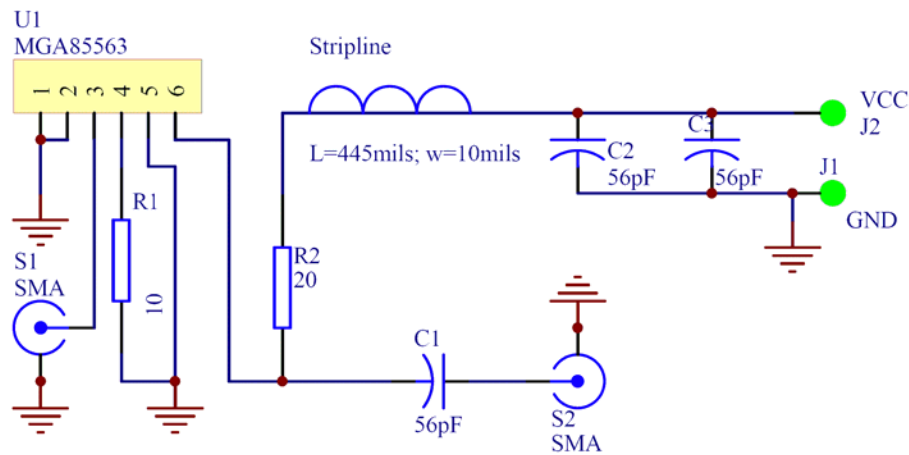
Figure 2.20: LNA schematic

This MMIC has a good gain, a small noise figure and it requires a simple PCB with few external components. Indeed, with very high-frequency designs, it is important to have the minimal amount of components in circuits. Moreover, the circuit is made of double-sided Duroid RO4003 with chemical gold-plating with gold cyanide, as for the pulser. The resistor R_1 is used to set the bias current, which is about 20 mA, that is required to have a good linearity and a small noise figure. The RF tracks are sized as they were for the pulser (w = 49 mils). The new design topic here is the size of RFC (Radio-Frequency Choke) stripline used to power the MMIC and to reject RF into power supply. This RFC stripline is needed because the power supply and the RF output are shared by the same pin of the MMIC. The design of this stripline is detailed in the next section.

Stripline calculations

The working principle of the RFC stripline is simple. The stripline is a thin line that connect, via R_2 the RF to the power supply. The rejection of the RF works because the power supply $J2$ arrives on a wide square of copper and thus the stripline, which is a kind of transmission line, considers it as a very badly matched load and rejects the RF. The size of the stripline has to be a quarter wave length with a short circuit on one end (the big square pad). In fact, the stripline is not a real RFC inductance but a notch filter designed to reject around 4.25 GHz. As we have UWB signals to amplify, the filter would not be well matched in the edge of the bandwidth; a small resistor is placed in series with the stripline in order to decrease the quality factor (de-Q) of the filter and to improve the rejection of the RF signal. Formally, its value should be added to the resistance of the stripline but this one is negligible. The calculations required to size the RFC stripline are implemented in the Matlab code shown in Appendix A.1.3, according to references [22] and [23].

As the resistance of the stripline is negligible, as given by the Matlab code, we choose to de-Q the stripline with $R_2 = 20\Omega$.

PCB of the LNA

The PCB of the MMIC LNA is shown in Figure 2.21. As for the pulser, the PCB is doubled-sided and the bottom side is a ground plane that fills all the surface of the PCB for shielding and for fulfilling microstrip geometry requirements. For the same reason as for the pulser, there a several vias used to connect to ground with the smallest as possible amount of parasitic inductance.
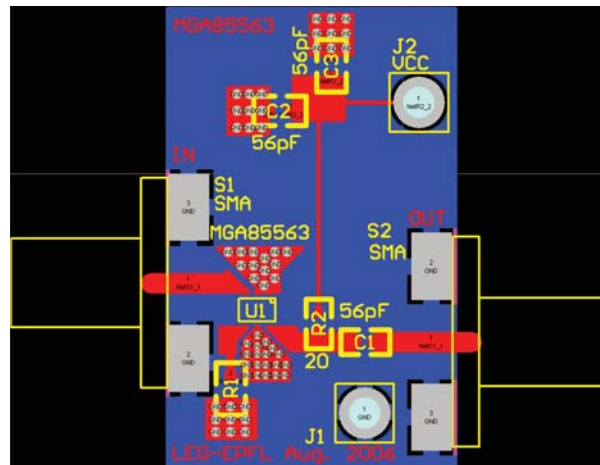
Figure 2.21: The PCB of the LNA on Duroid

2.3.3 Choice of components

The RF parts made of the mixer, the frequency doubler and the power RF amplifier are designed by using integrated circuits form Hittite Corporation, which provides evaluation boards ready to use we just have to assemble with SMA connectors. The programmable VCO, the ADF 4360-2, is provided by Analog Devices. As it is a complex circuit that requires a serial link and a computer for programming the output frequency, we replace it by a function generator (HP 8648C). The frequency doubler is a passive circuit HMC-189; it accepts at its input a signal in the frequency range from 2 to 4 GHz and provides an output signal from 4 to 8 GHz, provided that the power of the input signal is at least of 15 dBm. We choose a passive doubler because it is easy to find in our working considered frequency range. The conversion loss is of 13 dB. The mixer is a passive circuit HMC-129. It is passive for the same reason as for the doubler and it requires an input signal of at least 15 dBm on its LO (Local Oscillator) input to provide a good conversion. The inputs LO and RF (Radio Frequency) accept an input frequency range from 4 to 8 GHz while the IF (Intermediate Frequency) output provides a signal from DC to 3 GHz, thus much more than required for the acquisition board. In our case, we consider RF as an input and IF as an output because we down-convert the signal but their respective function can be exchanged when we do up-conversion with exactly the same characteristics. The conversion loss is of 7 dB as shown further in the measurements. Because of the power level required for both frequency doubler and mixer, we need a power amplifier at the input of the doubler in order to make both of them to work properly. In practice, we amplify the sine wave from the generator to 25 dBm with the power amplifier at the input of the doubler such that we have about 11 dBm at the input of the mixer. Although this power is lower than required for the mixer (according to the manufacturer), we see experimentally that it works well and we accept it like this because we cannot increase the power at the input of the doubler unless we take a higher risk to destroy it.

2.3.4 Measurements

During our experimentations, we saw that the architecture of the receiver previously described needs to be modified at some points. To simplify the study of the receiver, we divided it into two parts each with its own measurement protocol. We combined these two sets of results to show the expected behaviour of the receiver as it will be used in practice. Red letters are used to label the points of the receiver for the budget-link of each part. They also help to refer to parts of the circuits in the following explanations.

Amplification and filtering stage only

Although the care of the LNA design, we saw that two (or more) cascaded LNAs, as shown in Figure 2.19, will oscillate. This is because there are coupling as we do not use shielding box at this stage of the design (see Section 2.4.2 for more details). In addition, the band-pass filter is placed after the power amplifier because it is also a passive element that reduces the available power at its output. For the test, we use the Rohde et Schwarz function generator with the antenna in order to simulate the pulser but with only one frequency with a known power. Indeed, measuring the system with real UWB signals would be too complex and the power level would be wrongly measured because of the spread of power. We use a sine wave signal at 4.54 GHz (we choose this value randomly, any other value in the considered frequency range works as well) for the tests. The antenna are spaced at about 40 cm. The amplification and filtering part is shown in Figure 2.22; this architecture is similar to the one of Figure 2.19 but with only one LNA.
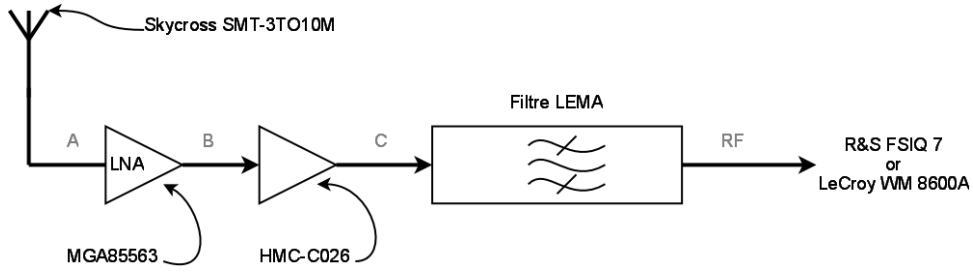
Figure 2.22: Detail of receiving part

The resulting measurement obtained at each point labelled in Figure 2.22 is given in Table 2.6 which gives the budget link of the circuit.

Receiver	Power [dBm]	Frequency [GHz]	Comments
A	−78	4.54	Sine wave
B	−69	4.54	Sine wave
C	−41	4.54	Sine wave
RF	−43	4.54	Sine wave

Table 2.6: Budget-link of LNAs and filter only

These measurements show that the specifications given by the manufacturers of the integrated circuits are exactly met. This means that the quality of the PCB design is good.

Frequency shifting stage only

In this configuration, we want to measure what is obtained from the mixer. For this purpose, we inject into the mixer the sine wave at 4.54 GHz and we measure the spectrum at its output. The architecture of the circuit is shown in Figure 2.23. As we only have sine waves in this scenario, we do not perform measurements in the time domain.
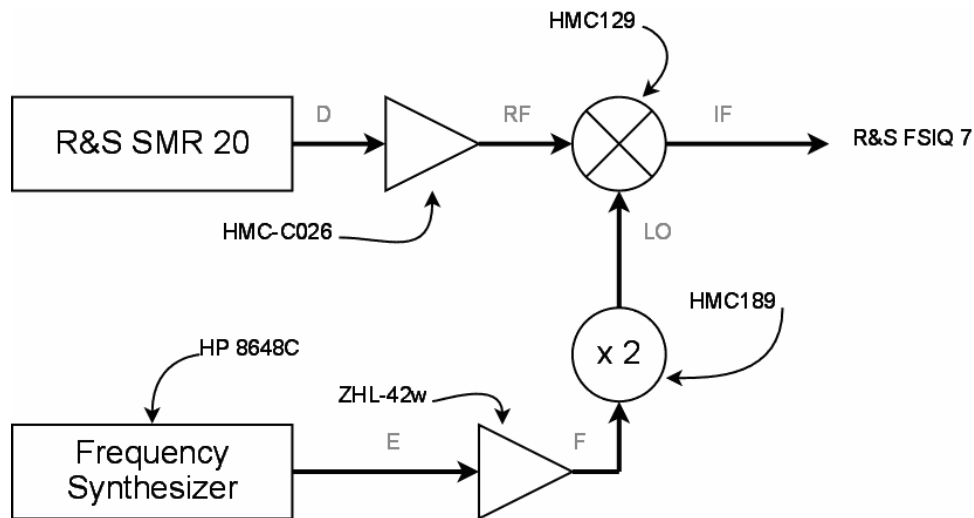
Figure 2.23: Detail of down-converting part

The resulting measurement obtained at each point labelled in Figure 2.23 is given in Table 2.7 which gives the budget link of the circuit. We see the very good quality of the signal at the output of the mixer and the high sensitivity of the system.

Receiver	Power [dBm]	Frequency [GHz]	Comments
D	-63	4.540	Sine wave
E	-10	$2,000$	Sine wave
F	25.8	$2,000$	Sine wave
RF	-33	4.540	Sine wave (+ noise)
LO	10.4	$4,000$	Sine wave (+ harmonics)
IF	-39	$0,540$	Sine wave (0 - 1 GHz)

Table 2.7: Budget-link of down-converting part only

The spectrum on the full range (from 0 to 7 GHz) at the output (point IF) is shown in Figure 2.24.
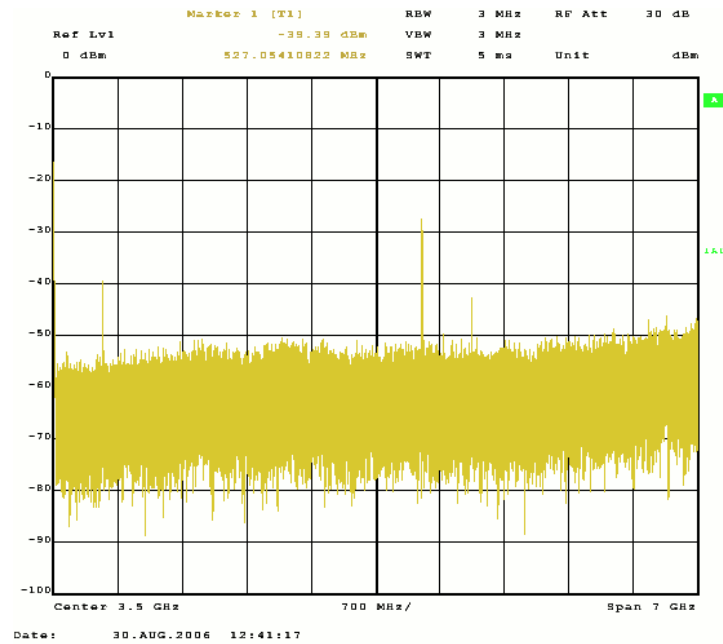
Figure 2.24: Spectrum at the output of the mixer

In the base band (from 0 to 1 GHz) we have at the output (point IF) the spectrum shown in Figure 2.25.
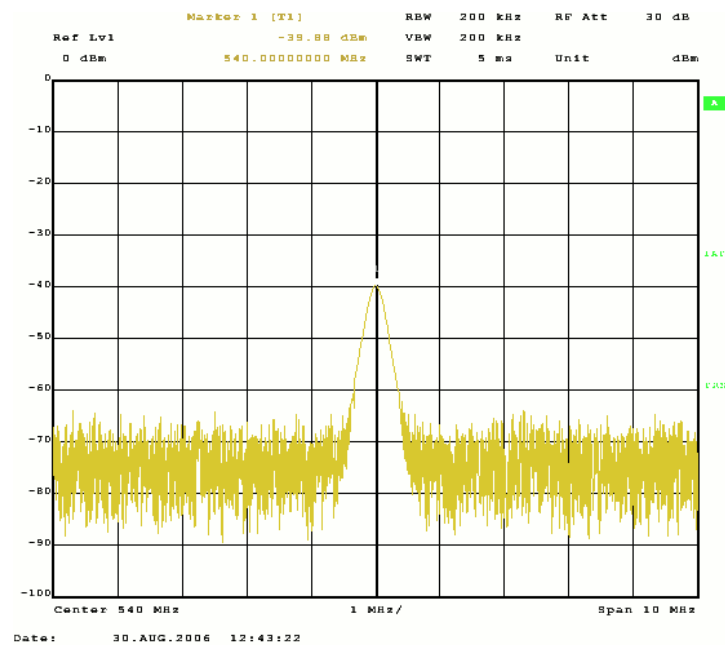
Figure 2.25: detail of the spectrum at the output of the mixer

We clearly see the sine wave at 540 MHz that comes from the down-conversion. We also

estimate the attenuation of the mixer which is approximately 6 dB.

Whole receiver

The complete receiver measurements take the previous results with the level measured at the output, as shown in Figure 2.26. The budget-link is measured by injecting the same 4.54 GHz sine wave as done previously; we show at the end of this section the signal we obtain with a real UWB impulse when the pulser is driven by the FPGA board. These signals are those that are processed by the FPGA in practice.
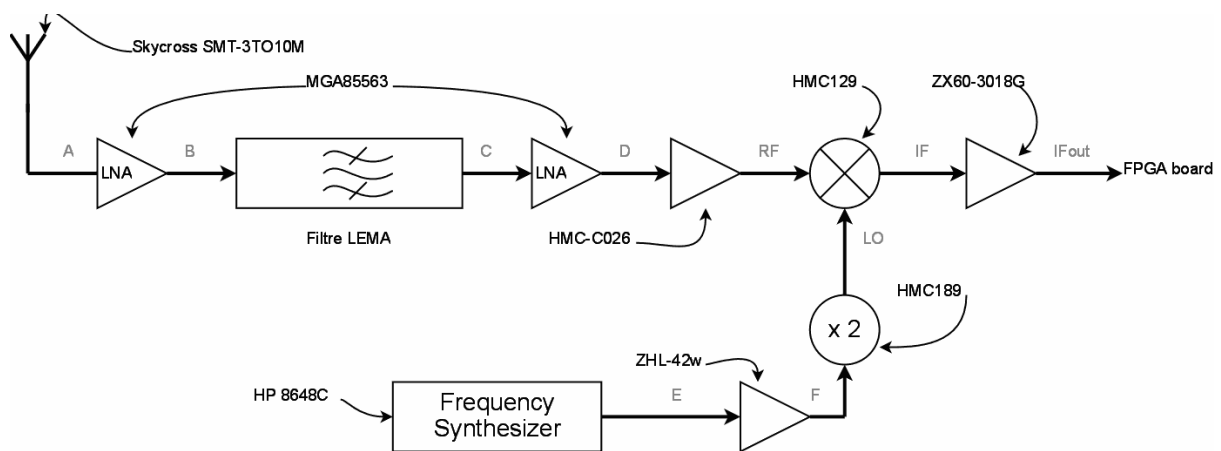
Figure 2.26: Complete receiver

The results of measurement are shown in Table 2.8 thereafter.

Receiver	Power [dBm]	Frequency [GHz]	Comments
A	-78	$4,54$	Sine wave
B	-69	$4,54$	Sine wave
C	-41	$4,54$	Sine wave
E	-10	$2,000$	Sine wave
F	$25,8$	$2,000$	Sine wave
RF	-43	$4,54$	Sine wave
LO	$10,4$	$4,000$	Sine wave (+ harmonics)
IF	-50	$0,54$	Sine wave (+ intermodulation)
IFout	-28	$0,54$	Sine wave (+ intermodulation)

Table 2.8: Budget-link of the complete receiver

As for individual stages, we note the good accuracy between measurements and expectations. The spectrum, shown in Figure 2.27, is similar to those obtained previously with the down-conversion stage only.
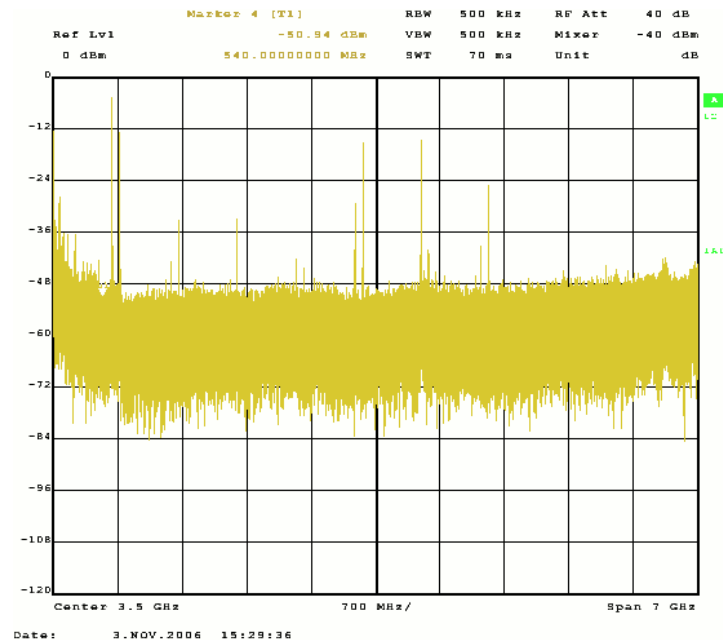
Figure 2.27: Spectrum at the output of the receiver with pulser

We see on the left of the blue arrow the UWB spectrum with a bandwidth of about 500 MHz obtained from the down-conversion of the received signal. As the FPGA has a anti-aliasing low-pass filter that cuts at about 700 MHz, the other harmonic components produced by the down-conversion are removed for the DSP. Figure 2.28 shows the signal in the time domain measured with the LeCroy oscilloscope which has a bandwidth of 6 GHz. The undesired frequencies that correspond to the noise are strongly removed by the anti-aliasing filter on the FPGA board.

This signal is analysed by the FPGA for recovering the synchronization pattern sent by the pulser. The main idea of this analysis is to apply a correlation calculation on the sequence to find the beginning of it; this sequence begins at the point where the correlation is maximal. Finally, the whole receiver is shown in Figure 2.29.
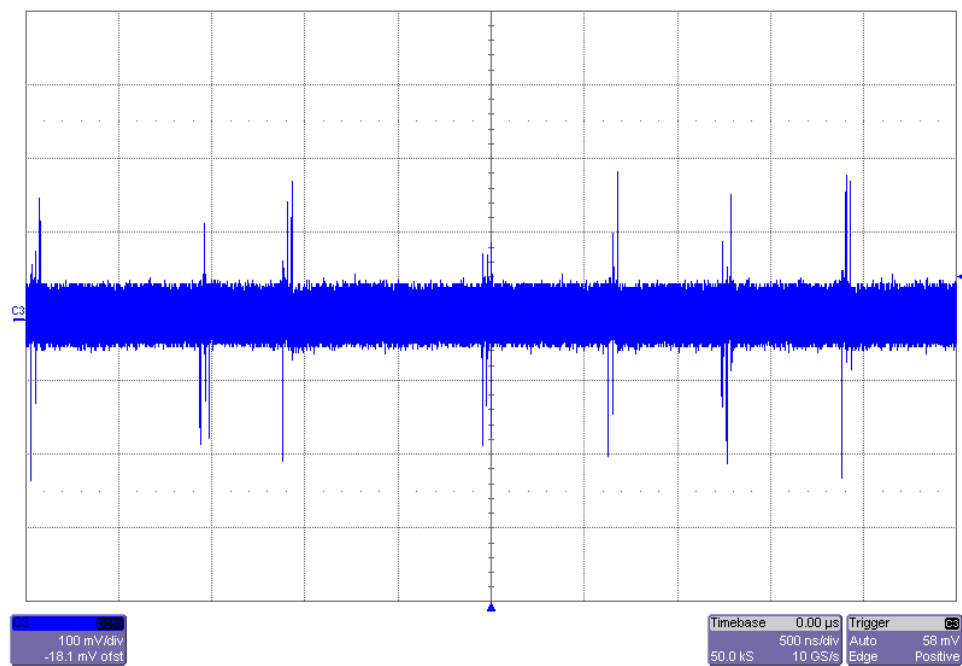
Figure 2.28: Spectrum at the output of the receiver with pulser
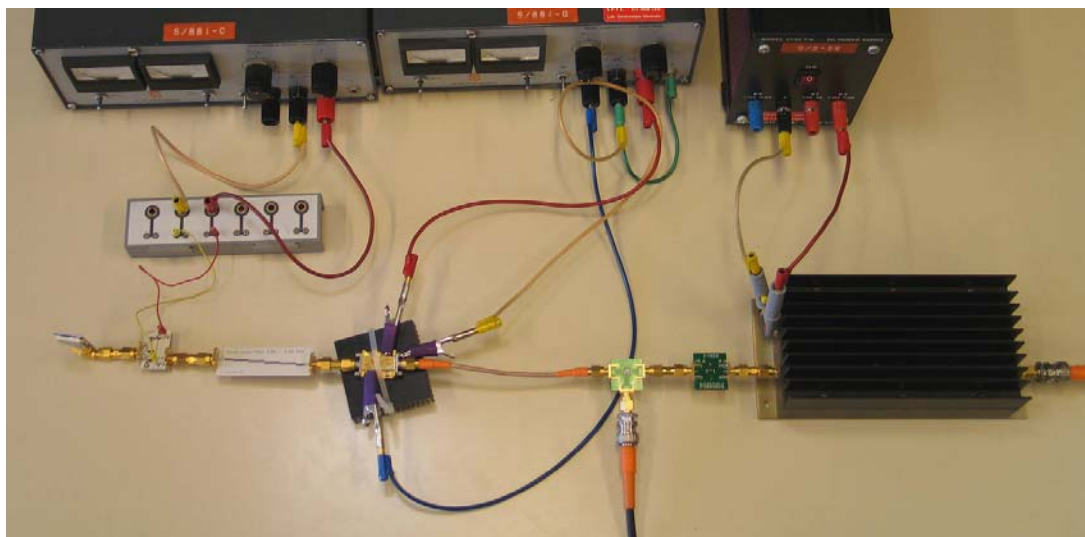
Figure 2.29: The receiver circuit

2.4   Improvements

Although the system (transmitter and receiver) described in this chapter works very well, there are several improvements required to have a small and reliable UWB testbed that can transmit data over large distance. For this purpose, we consider the system as made of smaller parts such that each of them can be improved independently of the others. By combining these improved parts together, we should ideally obtain two boards of conventional size (160 x 100 mm), one for the emitter and the other for the receiver. The improvements described thereafter assume that we still use discrete components or MMIC circuits.

2.4.1   Improvement nº 1

The driver and the pulser need to be on the same board. Comparators are required for reshaping the signal from the FPGA board because measurements show that these signals are strongly degraded depending on the type of load on the circuit and despite of a careful impedance matching. The quality of the obtained UWB impulse depends directly on the shape of the incoming stream form the FPGA and this should not be the case for future designs. The recommended architecture would be the following :

- a comparator reshapes the incoming signal by, first, giving it the correct high and low levels voltages and, second, by ensuring the shortest transition time between high and low levels;

- one or two amplifiers amplify the signal with the correct gain (if required) and add a tuneable offset (also if required);

- the SRD diode (assuming we keep anyway this technology) with its passive surrounding components generate the UWB signal, as usual.

The total amount of amplifiers reduces from 3 to 1 or 2. The reshaping of the incoming signal by the comparator makes the quality of the generated UWB signal completely independent on the connection between the FPGA board and the transmitter. As the set driver-pulser has a small size, we can have more than 4 (for example 8 or 12) that will allow to experimentally validate protocols and algorithms (like these described in the article [24]) with several independent interferers for more realistic scenarios (MUI, see Section 10.1).

Because SRD-based UWB transmitters are too complex and unpredictable (even with many simulation runs) to implement for targeting a given set of specifications, we decided to not consider this technology for our future testbed. We will focus on more conventional architectures such that we have an easier control on the parameters of the UWB signal like power, central frequency and bandwidth in order to have a testbed that is strictly compliant with standard regulations. However, SRD impulse generation remains an active field of research as shown in the article [25].

2.4.2   Improvement nᵒ 2

Two LNAs need to be designed with the filter on the same board. For a first prototype, the same LNAs that were used can be considered but there are other better candidates that could be explored for doing LNAs with voltage controlled gain (see chapters 7 and 8 thereafter). The greatest challenge here is to remove the instability of the receiver when two or more LNAs are cascaded. For this purpose, this part needs to be shielded with a completely sealed metallic box. In addition, we investigate the possibility to improve the stability by modifying the resistor R_1 in the circuit of the MGA85563 MMIC.

2.4.3   Improvement nᵒ 3

Another power amplifier needs to be designed for replacing the very hot HMC-C026 (its temperature rises to more than $80\,°C$ although there is a radiator). This is because this amplifier is designed to amplify signal in a bandwidth from 2 to 20 GHz, which is much more than our needs. Using an amplifier designed to work only in the bandwidth of interest (here from 4.0 to 4.5 GHz) could strongly reduce the power consumption. In addition, if the LNAs give enough gain, there is no more the need to amplify the UWB signal with a so high gain and the power amplifier can be removed. Indeed, the HMC-C026 has a gain of 30 dB while a gain of 20 dB could be enough if the UWB signal is amplified at the output of the mixer (see improvement nᵒ 4 thereafter).

2.4.4   Improvement nᵒ 4

The down-conversion mixer and local oscillator need to be designed on the same board. Designing the local oscillator should not be a problem but it is a whole project in itself because we need a microcontroller for configuring the VCO and to write a software for the microcontroller (see Chapter 5). We suggest at this stage to use the ATtiny13 microcontroller from the

tinyAVR family from ATMEL for its simple instruction set and ease for programming. The crucial point when improving this part is to replace the huge power amplifier ZHL-42w by a cascade of smaller amplifiers for raising the level of the VCO before the frequency doubler and mixer. A similar amplifier design should be used at the output of the mixer in order to have a powerful enough signal for the acquisition board (but the bandwidth of the signal is not the same as we are in the baseband). These amplifiers could be designed on the same principle as those described in improvement nᵒ 3. When all these partial improvements would be made, integration of all the elements on one PCB should be relatively easy to do provided that the power supplies and decoupling capacitors are well designed. We also highly recommend to use a shielding box for isolating the circuits and to avoid parasitic oscillations and cross-coupling.

2.5   Conclusion

The goal we targeted when we started to design and to build this first prototype of testbed was to validate the possibility to transmit and receive UWB impulses and to gain the knowledge required to build later a better one. This testbed works as expected but it requires many improvements as mentioned previously. We experimentally validated the quality of the radio communication by measuring its ability to receive a pattern of bits (a predefined sequence of bits that were sent) with the presence of several interferers. The protocols and algorithms are improved according to these intermediate results in order to prepare the experimental validation of the PID algorithm as done in [26] with the improved testbed described thereafter. In addition, these improvements give a direction in which to focus when designing integrated parts of this testbed, as explained thereafter in this work. Although it requires improvements, this testbed was already working well enough to experimentally validate a simple synchronization algorithm with two transmitters as it was shown in the MICS Workshop that holds in 2006 at Zurich and for which it won the best demonstration award.

We decided for this first prototype of testbed to not consider the FCC regulations because we first focus on designing a testbed that works. It is crucial for further improvements of our testbed to be compliant to these regulations because it is a required condition to produce results that are accepted by the research community and industry and also because it is required by the law.

Chapter 3

UWB Mathematical foundations

The generation of UWB signal is one the most challenging topic when designing circuits (either integrated or discrete) for UWB communications. These challenges include mainly the conformation of the spectrum's shape with official standards, the power required to generate the signal and the possibility to generate this signal with electronic means by maintaining an acceptable level of complexity of the circuit. For these reasons, this chapter presents the mathematical study of UWB signal generation by considering simple waveforms (in the time domain) that can be implemented in a circuit. Although their apparent simplicity in the time domain, these waveforms allow to generate signals whitch have a spectrum that is of high interest in UWB communication; some of these spectra can be very difficult (if not impossible) to calculate and to express with analytical expressions.

The goal of this chapter is to express generic signals in the time domain that are created by combining simple generic waveforms and to calculate the corresponding spectrum in order to express relations between the parameters of the time-domain signals with the parameters of the frequency-domain signals. The parameters of the frequency-domain signals are given by regulation standards and the specifications desired for the circuit; the time-domain signals parameters are then calculated according to the relations obtained in this chapter and the electronic circuit is designed to produce this signal with as the best as possible accuracy. For each type of signal, we provide a numeric application that directly concerns a scenario developed in this work. The sine wave with square envelope is used for the discrete UWB Transmitter presented in Chapter 6, and the sine wave with truncated Gaussian envelope is used for the integrated low-power UWB transmitter presented in Chapters 12 and 13. Because the case of

Gaussian and square enveloppe cannot by solved analytically, we use a numeric simulation oriented to integrated circuit implementation that is presented in Chapter 11. The calculations in this chapter assume that the pulse is alone; for calculating the spectrum of a sequence of pulses, the reader can refer to [27] and [28]. In our case, as the pulses are very short compared to the pulse repetition period, we can assume that the spectrum's shape is not modified, excepted its magnitude.

3.1   Definition of the generic signals

We consider three generic signals that can be combined to produce UWB signal : the sine wave, the Gaussian function and the square window. In order to simplify further calculations, we define these functions such that they are even functions centered at $t = 0$. Assuming the even property makes the functions being symmetric around the origin and thus helps in Fourier transform calculations. These calculations can be made however by considering not even function but with a significant increase of complexity and a loss of understanding of fundamental properties.

3.1.1   The sine wave

The sine wave is in our case a cosine in order to have an even function; it is defined as follows:

$$C(t) = A \cdot \cos(2\pi f_0 t)$$

where A is the amplitude in volts and f_0 is its frequency in Hertz as shown in Figure 3.1.
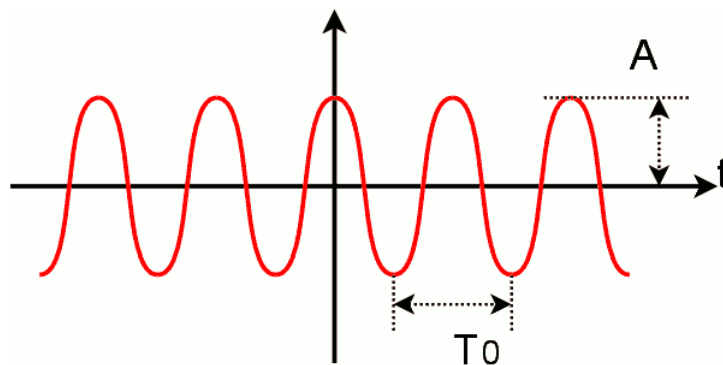
Figure 3.1: The sine wave in the time domain.

3.1.2   The square window

The square window is defined as follows:

$$W_{T_p}(t) = \begin{cases} 1 & \text{if } -\frac{T_p}{2} \leq t \leq \frac{T_p}{2} \\ 0 & \text{else} \end{cases}$$

where T_p is the duration of the window, as shown in Figure 3.2.
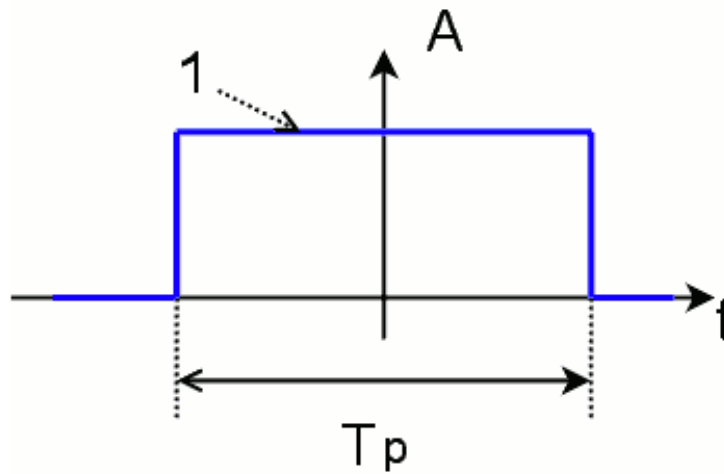
Figure 3.2: The square of duration T_p in the time domain.

The spectrum of the square window is expressed as follows :

$$F(f) = T_p \cdot \text{sinc}(\pi f T_p)$$

3.1.3   The Gaussian function

The Gaussian function is defined as follows in the general case:

$$G_{\mu,\sigma}(t) = \frac{1}{\sqrt{2\pi}\sigma} \cdot e^{\frac{-(t-\mu)^2}{2\sigma^2}}$$

where μ is the mean and σ is the standard deviation, as shown in Figure 3.3

The mean is geometrically interpreted as the position of the center of the Gaussian and the standard deviation represents how the "mass" is spread around the mean. In other words, a Gaussian is sharper with a smaller σ and wider with a bigger one. In order to have an even
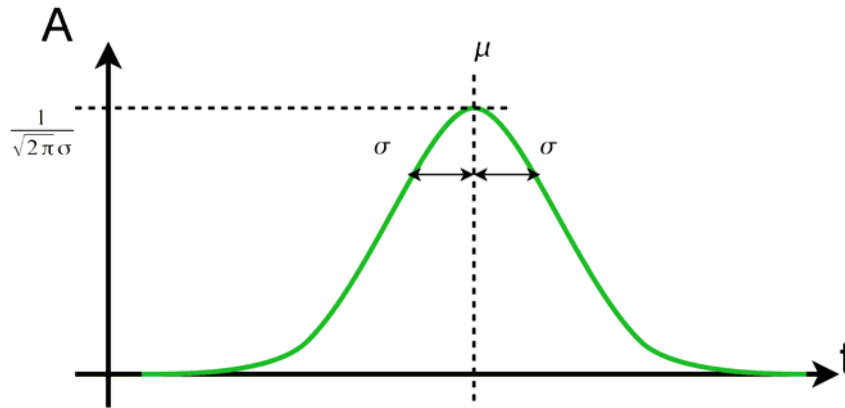
Figure 3.3: The Gaussian centered at μ in the time domain.

function for the Gaussian, we consider the Gaussian centered at $\mu = 0$ as follows :

$$G_\sigma(t) = \frac{1}{\sqrt{2\pi}\sigma} \cdot e^{-\frac{t^2}{2\sigma^2}}$$

The spectrum of the Gaussian function is expressed as follows :

$$F(f) = e^{-\frac{(2\pi\sigma f)^2}{2}}$$

It is remarkable to see that the spectrum of a Gaussian function is also a Gaussian function.

3.2 The sine wave with a square envelope

The sine wave with a squared envelope is one of the easiest UWB signal to generate and it gives an acceptable spectrum according to UWB considerations. It has a finite duration time Tp that determines the bandwidth in the frequency domain. This signal is defined of follows :

$$P_{UWB}(t) = W_{T_p}(t) \cdot A \cdot \cos(2\pi f_0 t)$$

where

$$W_{T_p}(t) = \begin{cases} 1 & \text{if } -\frac{T_p}{2} \leq t \leq \frac{T_p}{2} \\ 0 & \text{else} \end{cases}$$

and f_0 is the central frequency and A is the amplitude in volts. The signal is shown in Figure 3.4.
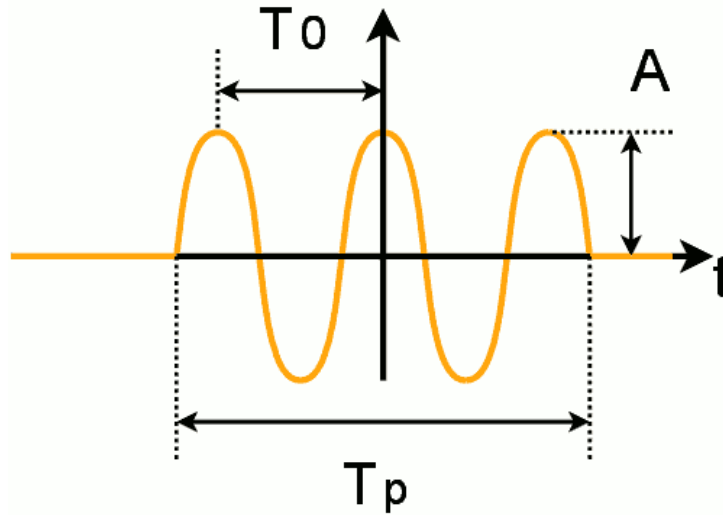
Figure 3.4: The sine wave with square envelope in the time domain.

3.2.1   Spectrum calculation

Let

$$F(f) = \mathfrak{F}\left(P_{UWB}(t)\right) = \int_{-\infty}^{\infty} P_{UWB}(t) \cdot e^{-j2\pi ft} dt$$

be the Fourier transform of this impulse. By applying Euler's identity and changing integration boundaries, we obtain :

$$
\begin{aligned}
F(f) &= \int_{-\infty}^{\infty} P_{UWB}(t) \cdot \left[\cos(-2\pi ft) + j\sin(-2\pi ft)\right] dt \\[2mm]
&= \int_{-\infty}^{\infty} W_{T_p}(t) \cdot A \cdot \cos(2\pi f_0 t) \cdot \left[\cos(-2\pi ft) + j\sin(-2\pi ft)\right] dt \\[2mm]
&= A \cdot \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \cos(2\pi f_0 t) \cdot \left[\cos(-2\pi ft) + j\sin(-2\pi ft)\right] dt
\end{aligned}
$$

By applying elementary trigonometric and calculus transformation, the integral is calculated as follows:

$$
\begin{aligned}
F(f) \;=\;& A \cdot \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \cos(2\pi f_0 t) \cdot \cos(-2\pi f t) dt + jA \cdot \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \cos(2\pi f_0 t) \cdot \sin(-2\pi f t) dt \\[2ex]
\;=\;& \frac{A}{2} \cdot \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \left(\cos(2\pi(f_0 - f)t) + \cos(-2\pi(f_0 + f)t) \right) dt \\[2ex]
& + j\frac{A}{2} \cdot \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \left(\sin(2\pi(f_0 - f)t) + \sin(2\pi(f_0 + f)t) \right) dt \\[2ex]
\;=\;& \frac{A}{2} \cdot \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \cos(2\pi(f_0 - f)t) dt + \frac{A}{2} \cdot \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \cos(-2\pi(f_0 + f)t) dt \\[2ex]
& + j\frac{A}{2} \cdot \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \sin(2\pi(f_0 - f)t) dt + j\frac{A}{2} \cdot \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \sin(2\pi(f_0 + f)t) dt \\[2ex]
\;=\;& \frac{A}{2} \cdot \left[\frac{1}{2\pi(f_0 - f)} \sin(2\pi(f_0 - f)t) \right]_{-\frac{T_p}{2}}^{\frac{T_p}{2}} + \frac{A}{2} \cdot \left[\frac{1}{2\pi(f_0 + f)} \sin(2\pi(f_0 + f)t) \right]_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \\[2ex]
& + j\frac{A}{2} \cdot \underbrace{\left[-\frac{1}{2\pi(f_0 - f)} \cos(2\pi(f_0 - f)t) \right]_{-\frac{T_p}{2}}^{\frac{T_p}{2}}}_{=0} + j\frac{A}{2} \cdot \underbrace{\left[-\frac{1}{2\pi(f_0 + f)} \cos(2\pi(f_0 + f)t) \right]_{-\frac{T_p}{2}}^{\frac{T_p}{2}}}_{=0}
\end{aligned}
$$

Evaluating the integral and rearranging terms gives:

$$
\begin{aligned}
F(f) &= \frac{A}{2} \cdot \left(\frac{1}{2\pi(f_0 - f)} \sin(\pi(f_0 - f)T_p) - \frac{1}{2\pi(f_0 - f)} \sin(-\pi(f_0 - f)T_p) \right) \\
&\quad + \frac{A}{2} \cdot \left(\frac{1}{2\pi(f_0 + f)} \sin(\pi(f_0 + f)T_p) - \frac{1}{2\pi(f_0 + f)} \sin(-\pi(f_0 + f)T_p) \right) \\
&= \frac{A}{2} \cdot \left(\frac{1}{2\pi(f_0 - f)} \sin(\pi(f_0 - f)T_p) + \frac{1}{2\pi(f_0 - f)} \sin(\pi(f_0 - f)T_p) \right) \\
&\quad + \frac{A}{2} \cdot \left(\frac{1}{2\pi(f_0 + f)} \sin(\pi(f_0 + f)T_p) + \frac{1}{2\pi(f_0 + f)} \sin(\pi(f_0 + f)T_p) \right) \\
&= A \left(\frac{\sin(\pi(f_0 - f)T_p)}{2\pi(f_0 - f)} + \frac{\sin(\pi(f_0 + f)T_p)}{2\pi(f_0 + f)} \right) \\
&= A \frac{T_p}{2} \left(\frac{\sin(\pi(f_0 - f)T_p)}{\pi(f_0 - f)T_p} + \frac{\sin(\pi(f_0 + f)T_p)}{\pi(f_0 + f)T_p} \right) \\
&= A \frac{T_p}{2} \left(\mathrm{sinc}(\pi(f_0 - f)T_p) + \mathrm{sinc}(\pi(f_0 + f)T_p) \right)
\end{aligned}
$$

The spectrum of the square window is the particular case of $F(f)$ when $f_0 = 0$ and $A = 1$. This gives :

$$
\begin{aligned}
F_{f_0=0, A=1}(f) &= 1 \cdot \frac{T_p}{2} \left(\mathrm{sinc}(\pi(0 - f)T_p) + \mathrm{sinc}(\pi(0 + f)T_p) \right) \\
&= \frac{T_p}{2} \left(\mathrm{sinc}(-\pi f T_p) + \mathrm{sinc}(\pi f T_p) \right) \\
&= T_p \cdot \mathrm{sinc}(\pi f T_p)
\end{aligned}
$$

Assuming that $\mathrm{sinc}(\pi(f_0 + f)T_p) \ll \mathrm{sinc}(\pi(f_0 - f)T_p)$ (see discussion in Section 3.3.1), the spectrum is considered to be maximum in f_0 with a very good approximation and its value at this frequency is given by :

$$
F(f_0) = jA\frac{T_p}{2} \left(\mathrm{sinc}(2\pi f_0 T_p) - 1 \right)
$$

The frequency f_0 corresponds to the central frequency of the UWB spectrum and thus is the

frequency delivered by the sine wave oscillator previously described. By normalizing the spectrum with its maximum value, we define the attenuation as :

$$A(f) = \frac{F(f)}{F(f_0)} = \frac{\mathrm{sinc}(\pi(f_0 + f)T_p) - \mathrm{sinc}(\pi(f_0 - f)T_p)}{\mathrm{sinc}(2\pi f_0 T_p) - 1} \tag{3.1}$$

Because in the UWB domain, the corner frequency is defined at -10 dB of the maximum value instead of -3 dB, as done in usual applications, we have to look for values of f such that $A(f) = \sqrt{0.1} = 0.3162$. The square root is used here because we consider voltage instead of power. For this purpose, we consider the fundamental wave relation $f_0 \cdot T_0 = 1$ and let

$$\begin{aligned} T_p &= \alpha \cdot T_0 \\ f &= \beta \cdot f_0 = f_\beta \end{aligned}$$

where α and β are dimensionless scaling values for the time and the frequency respectively. By inserting this into (3.1), we obtain

$$A(f_\beta) = \frac{\mathrm{sinc}(\pi(1 + \beta)\alpha) - \mathrm{sinc}(\pi(1 - \beta)\alpha)}{\mathrm{sinc}(2\pi\alpha) - 1} \tag{3.2}$$

The bandwidth B is then simply defined as $B = 2f_0(1 - \beta)$ and we thus have the following fundamental relation :

$$B \cdot Tp = 2(1 - \beta)\alpha = K \tag{3.3}$$

where K is a parameter that depends on the quality factor $Q = \frac{f_0}{B} = \frac{1}{2(1-\beta)}$. This dependency between K and Q is better understood by noting that β depends on α from (3.2).

3.2.2   Numeric Application

The IR-UWB transmitter described thereafter works from 4.0 to 4.5 GHz, so $B = 0.5$ GHz and $f_0 = 4.25$ GHz (and thus $T_0 = 0.2353$ ns). Thus, β is given by

$$\beta = 1 - \frac{1}{2Q} = 1 - \frac{B}{2f_0} = 1 - \frac{0.5}{2 \cdot 4.25} = 0.9412$$

Then, we calculate α by solving numerically – by iteration for example as done in Appendix A.2.1 – the equation (3.2) with $A(f) = 0.3162$. We find $\alpha = 12.46$. The pulse duration is given by

$$T_p = \alpha \cdot T_0 = 12.46 \cdot 0.2353 \text{ ns } = 2.932 \text{ ns}$$

and the fundamental relation parameter is

$$K = B \cdot T_p = 2(1 - \beta)\alpha = 2(1 - 0.9412) \cdot 12.46 = 1.47 \tag{3.4}$$

with $Q = 8.5$. In practice, the pulse duration is about 10% greater in order to compensate the envelope that is not perfectly square but trapezoidal (due to the balun) and the spectrum that would consequently be too wide.

3.3   The sine wave with a Gaussian envelope

The sine wave with a Gaussian envelope gives one of the best spectrums according to UWB specification but requires a more complex circuit to be accurately generated. It has an infinite duration time and the spectrum bandwidth can be adjusted by changing the standard deviation of the Gaussian function. Because of its infinite duration, this signal cannot be generated as it is and thus it has mainly a theoretical interest here. In practice, the tails of the Gaussian function can be neglected and truncated to 0; this case will be studied thereafter. The sine wave with Gaussian envelope signal is defined of follows :

$$P_{UWB}(t) = G_\sigma(t) \cdot A \cdot \cos(2\pi f_0 t)$$

where

$$G_\sigma(t) = \frac{1}{\sqrt{2\pi}\sigma} \cdot e^{-\frac{t^2}{2\sigma^2}}$$

is the Gaussian function centered at $t = 0$ with a standard deviation σ, f_0 is the central frequency and A is the amplitude in volts. The signal is shown in Figure 3.5.

3.3.1   Spectrum calculation

Let

$$F(f) = \mathfrak{F}\left(P_{UWB}(t)\right) = \int_{-\infty}^{\infty} P_{UWB}(t) \cdot e^{-j2\pi ft} dt$$
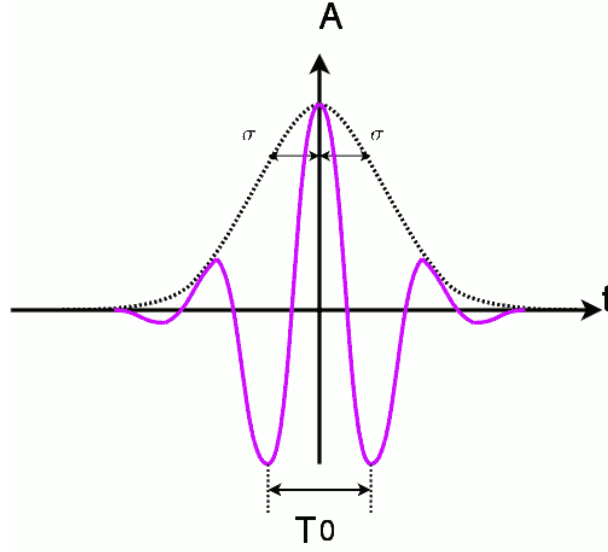
Figure 3.5: The sine wave with gaussian envelope in the time domain.

be the Fourier transform of this impulse. By using the signal definition, applying Euler's identity and integral elementary properties, we obtain :

$$
\begin{aligned}
F(f) &= \int_{-\infty}^{\infty} G_{\sigma}(t) \cdot A \cdot \cos(2\pi f_0 t) \cdot e^{-j2\pi ft} dt \\[2ex]
&= A \cdot \int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi}\sigma} \cdot e^{-\frac{t^2}{2\sigma^2}} \cdot \cos(2\pi f_0 t) \cdot e^{-j2\pi ft} dt \\[2ex]
&= A \cdot \int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi}\sigma} \cdot e^{-\frac{t^2}{2\sigma^2}} \cdot \frac{e^{j2\pi f_0 t} + e^{-j2\pi f_0 t}}{2} \cdot e^{-j2\pi ft} dt \\[2ex]
&= \frac{A}{2} \cdot \frac{1}{\sqrt{2\pi}\sigma} \cdot \int_{-\infty}^{\infty} e^{-\frac{t^2}{2\sigma^2}} \cdot \left(e^{j2\pi f_0 t} + e^{-j2\pi f_0 t}\right) \cdot e^{-j2\pi ft} dt \\[2ex]
&= \frac{A}{2\sqrt{2\pi}\sigma} \cdot \left[\int_{-\infty}^{\infty} e^{-\frac{t^2}{2\sigma^2}} \cdot e^{j2\pi f_0 t} \cdot e^{-j2\pi ft} dt + \int_{-\infty}^{\infty} e^{-\frac{t^2}{2\sigma^2}} \cdot e^{-j2\pi f_0 t} \cdot e^{-j2\pi ft} dt\right] \\[2ex]
&= \frac{A}{2\sqrt{2\pi}\sigma} \cdot \left[\int_{-\infty}^{\infty} e^{-\frac{t^2}{2\sigma^2}+j2\pi f_0 t - j2\pi ft} dt + \int_{-\infty}^{\infty} e^{-\frac{t^2}{2\sigma^2}-j2\pi f_0 t - j2\pi ft} dt\right] \\[2ex]
&= \frac{A}{2\sqrt{2\pi}\sigma} \cdot \left[\int_{-\infty}^{\infty} e^{-\frac{t^2}{2\sigma^2}-j2\pi(f-f_0)t} dt + \int_{-\infty}^{\infty} e^{-\frac{t^2}{2\sigma^2}-j2\pi(f+f_0)t} dt\right] \\[2ex]
&= \frac{A}{2\sqrt{2\pi}\sigma} \cdot \left[\int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}(t^2+j4\pi\sigma^2(f-f_0)t)} dt + \int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}(t^2+j4\pi\sigma^2(f+f_0)t)} dt\right]
\end{aligned}
$$

In order to evaluate the arguments of both exponential functions, we use the technique of the square completion. Let

$$t^2 + j4\pi\sigma^2(f - f_0)t = (t + a)^2 - c = t^2 + 2at + a^2 - c$$

where

$$a = j2\pi\sigma^2(f - f_0)$$

$$c = -4\pi^2\sigma^4(f - f_0)^2$$

and

$$t^2 + j4\pi\sigma^2(f + f_0)t = (t + b)^2 - d = t^2 + 2bt + b^2 - d$$

where

$$b = j2\pi\sigma^2(f + f_0)$$

$$d = -4\pi^2\sigma^4(f + f_0)^2$$

The Fourier transform of this impulse is thus calculated as follows :

$$
\begin{aligned}
F(f) &= \frac{A}{2\sqrt{2\pi}\sigma} \cdot \left[\int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}(t^2 + j4\pi\sigma^2(f - f_0)t)} dt + \int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}(t^2 + j4\pi\sigma^2(f + f_0)t)} dt \right] \\
&= \frac{A}{2\sqrt{2\pi}\sigma} \cdot \int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}\left((t + j2\pi\sigma^2(f - f_0))^2 + 4\pi^2\sigma^4(f - f_0)^2\right)} dt \\
&\quad + \frac{A}{2\sqrt{2\pi}\sigma} \cdot \int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}\left((t + j2\pi\sigma^2(f + f_0))^2 + 4\pi^2\sigma^4(f + f_0)^2\right)} dt
\end{aligned}
$$

Because the expressions $4\pi^2\sigma^4(f \pm f_0)^2$ do not depend on the variable t, they can go out of

the integral symbol and the proposition in Section K.1 holds as follows:

$$
F(f) = \frac{A}{2\sqrt{2\pi}\sigma} \cdot \int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}\left((t+j2\pi\sigma^2(f-f_0))^2+4\pi^2\sigma^4(f-f_0)^2\right)} dt
$$

$$
+\frac{A}{2\sqrt{2\pi}\sigma} \cdot \int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}\left((t+j2\pi\sigma^2(f+f_0))^2+4\pi^2\sigma^4(f+f_0)^2\right)} dt
$$

$$
= \frac{A}{2\sqrt{2\pi}\sigma} \cdot \int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}\left((t+j2\pi\sigma^2(f-f_0))^2\right)} \cdot e^{-\frac{1}{2\sigma^2}\left(4\pi^2\sigma^4(f-f_0)^2\right)} dt
$$

$$
+\frac{A}{2\sqrt{2\pi}\sigma} \cdot \int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}\left((t+j2\pi\sigma^2(f+f_0))^2\right)} \cdot e^{-\frac{1}{2\sigma^2}\left(4\pi^2\sigma^4(f+f_0)^2\right)} dt
$$

$$
= \frac{A}{2\sqrt{2\pi}\sigma} \cdot e^{-2\pi^2\sigma^2(f-f_0)^2} \cdot \underbrace{\int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}\left((t+j2\pi\sigma^2(f-f_0))^2\right)} dt}_{\sqrt{2\pi}\sigma}
$$

$$
+\frac{A}{2\sqrt{2\pi}\sigma} \cdot e^{-2\pi^2\sigma^2(f+f_0)^2} \cdot \underbrace{\int_{-\infty}^{\infty} e^{-\frac{1}{2\sigma^2}\left((t+j2\pi\sigma^2(f+f_0))^2\right)} dt}_{\sqrt{2\pi}\sigma}
$$

$$
= \frac{A}{2\sqrt{2\pi}\sigma} \cdot \sqrt{2\pi}\sigma \cdot \left(e^{-2\pi^2\sigma^2(f-f_0)^2} + e^{-2\pi^2\sigma^2(f+f_0)^2}\right)
$$

$$
= \frac{A}{2} \cdot \left(e^{-\frac{(2\pi\sigma(f-f_0))^2}{2}} + e^{-\frac{(2\pi\sigma(f+f_0))^2}{2}}\right)
$$

The spectrum of the Gaussian function is the particular case of $F(f)$ when $f_0 = 0$ and $A = 1$. This gives :

$$
F_{f_0=0, A=1}(f) = \frac{1}{2} \cdot \left(e^{-\frac{(2\pi\sigma(f-0))^2}{2}} + e^{-\frac{(2\pi\sigma(f+0))^2}{2}}\right)
$$

$$
= \frac{1}{2} \cdot \left(e^{-\frac{(2\pi\sigma f)^2}{2}} + e^{-\frac{(2\pi\sigma f)^2}{2}}\right)
$$

$$
= e^{-\frac{(2\pi\sigma f)^2}{2}}
$$

For determining the value required for σ in order to have a bandwidth $B = 2f$ with a corner frequency at -10 dB, we can translate the spectrum at $f_0 = 0$ in order to consider the original Gaussian function without frequency shift for simplifying the calculations. The question is:

Why do we consider the baseband spectrum for the Gaussian function while we consider the frequency shifted spectrum in the case of the sine with squared window ? The answer is twice. First, the sinc function decreases much more slowly than the Gaussian and this causes the bilateral spectrum of the sinc to be not so negligible in comparison with the Gaussian one. For this reason, the Gaussian shifted at $f_0 = 0$ gives a very accurate expression for σ that remains valid when it is shifted at f_0 while doing the same for the sinc will add a not so negligible error. However, we can neglect some terms in the squared enveloped sine spectrum expression only when we assume that the maximum frequency is at f_0 because the maxima of each of these terms occurs approximately at f_0; excepted that, we consider the full expression for the attenuation. The other reason is also that considering the baseband Gaussian is much easier for expressing a relation between σ and the bandwidth B than the complete expression for the frequency-shifted Gaussian. We consider thus the original Gaussian spectrum for the remaining calculation according to the previous justification. The spectrum is thus maximum at $f = 0$ and we have:

$$F(0) = e^{-\frac{(2\pi\sigma 0)^2}{2}} = 1$$

As its maximum value is 1, the attenuation is trivially defined as :

$$A(f) = \frac{F_{f_0=0}(f)}{F_{f_0=0}(f_0)} = e^{-\frac{(2\pi\sigma f)^2}{2}} \tag{3.5}$$

As previously done for the squared enveloped sine, the corner frequency is defined at -10 dB of the maximum value instead of -3 dB and we have to look for values of f such that $A(f) = \sqrt{0.1}$. The reader should keep in mind that although this equation is obtained at $f_0 = 0$, it is true at any central frequency f_0. The relation between the bandwidth B and σ is obtained as follows :

$$A(f) = e^{-\frac{(2\pi\sigma f)^2}{2}} = \sqrt{0.1}$$

$$\frac{(2\pi\sigma f)^2}{2} = -\ln\sqrt{0.1} = \ln\frac{1}{\sqrt{0.1}} = \frac{1}{2}\ln 10$$

$$(2\pi\sigma f)^2 = \ln 10$$

$$\sigma = \frac{\sqrt{\ln 10}}{2\pi f} = \frac{\sqrt{\ln 10}}{\pi B} \approx 0.483 \cdot \frac{1}{B}$$

Unlike with the squared enveloped sine, and because of the justification given above, this relation shows that with a Gaussian envelope, the central frequency f_0 has no effect on the bandwidth. The standard deviation σ is an equivalent way to express the bandwidth in this case.

3.3.2   Numeric Application

The IR-UWB transmitter described thereafter works from 4.0 to 4.5 GHz, so $B = 0.5$ GHz and thus $\sigma = 0.966$ ns. If we consider - for example - that 98% of the signal lies in the $\pm 2\sigma$ zone, we thus have 98% of the power during $t = 4\sigma \approx 3.86$ ns.

3.4   The sine wave with a Gaussian and a squared envelope

The sine wave with a Gaussian and squared envelope is one of the most difficult UWB signal to generate and to calculate. It corresponds to a sine wave with a Gaussian envelope that is truncated by a square window in order to have a finite duration time Tp. This signal is defined of follows :

$$P_{UWB}(t) = W_{T_p}(t) \cdot G_{\sigma}(t) \cdot A \cdot \cos(2\pi f_0 t)$$

where

$$W_{T_p}(t) = \begin{cases} 1 & \text{if } -\frac{T_p}{2} \le t \le \frac{T_p}{2} \\ 0 & \text{else} \end{cases}$$

with a duration T_p and

$$G_{\sigma}(t) = \frac{1}{\sqrt{2\pi}\sigma} \cdot e^{-\frac{t^2}{2\sigma^2}}$$

with a standard deviation σ; f_0 is the central frequency and A is the amplitude in volts. The signal is shown in Figure 3.6.

3.4.1   Spectrum calculation

In the case of sine wave with a Gaussian and a squared envelope, the calculation of the spectrum by applying the definition of a Fourier transform as done previously leads to a complex integral that cannot be solved analytically. We target to express the spectrum such that we can normalize all parameters like central frequency and impulse duration. By doing these normalization, we can express in a simple and meaningful way the relations between the physical
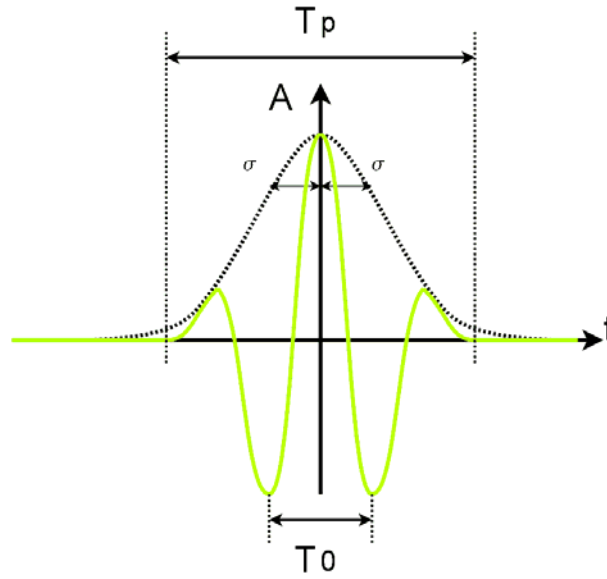
Figure 3.6: The sine wave with square and Gaussian envelope in the time domain.

parameters of the signal in the time domain (like amplitude, frequency, duration and shape) and its mathematical properties in the frequency domain (like power and bandwidth).

For all these reasons, we calculate the spectrum in a different way for the Gaussian and squared envelope. We saw previously that considering the signal in the base band is enough in the case of a Gaussian envelope because the Gaussian expression decreases so fast that the two bilateral spectra do almost not interfere to each other. Doing the same with the squared envelope is also possible but is much less accurate and it was why we did all calculation by considering the central frequency f_0. In the case of a Gaussian and squared envelope, both envelope shapes are multiplied together so the property of having a strong decrease far from the central frequency is preserved. Because of this, we can calculate the spectrum by considering the signal in the base band only, as it was done previously for the Gaussian envelope, which simplifies considerably the calculations. As we already know the spectra for the Gaussian and squared envelope in the base band, we use the convolution theorem; this gives a much simpler way to calculate the spectrum of both envelope shapes multiplied together.

Let

$$p(t) = W_{T_p}(t) \cdot G_\sigma(t)$$

be the envelope of the signal - or in a equivalent way, let it be the $P_{UWB}(t)$ signal in the

base band. We already know from previous calculation that :

$$\mathfrak{F}\left(W_{T_p}(t)\right) = T_p \cdot \mathrm{sinc}(\pi f T_p)$$

$$\mathfrak{F}\left(G_\sigma(t)\right) = e^{-\frac{(2\pi\sigma f)^2}{2}}$$

Applying the convolution theorem (see Section K.3) gives :

$$\mathfrak{F}\left(p(t)\right) = \mathfrak{F}\left(G_\sigma(t)\right) \star \mathfrak{F}\left(W_{T_p}(t)\right) = \int_{-\infty}^{\infty} e^{-\frac{(2\pi\sigma\hat{f})^2}{2}} \cdot T_p \cdot \mathrm{sinc}(\pi(f-\hat{f})T_p)d\hat{f} \qquad (3.6)$$

This integral cannot be solved analytically (to the best of our knowledge); we apply normalization as done previously for the square envelope. For this purpose, we consider the fundamental wave relation $f_0 \cdot T_0 = 1$ and let

$$
\begin{aligned}
T_p &= \alpha \cdot T_0 \\
f &= \beta \cdot f_0 = f_\beta \\
\sigma &= \gamma \cdot \frac{1}{f_0} \\
\hat{f} &= \epsilon \cdot f_0 \qquad \rightarrow \qquad d\hat{f} = d\epsilon \cdot f_0
\end{aligned}
$$

where α, β, γ and ϵ are dimensionless scaling values for the time and the frequency variables. The variables α and β play exactly the same role as for the case of the square envelope; the variable γ plays exactly the same role as for the Gaussian envelope. The variable ϵ is the integration variable for the frequency. By inserting this into (3.6), we obtain :

$$
\begin{aligned}
\mathfrak{F}\left(p(t)\right) &= T_p \cdot \int_{-\infty}^{\infty} e^{-\frac{(2\pi\sigma\hat{f})^2}{2}} \cdot \mathrm{sinc}(\pi(f-\hat{f})T_p) \cdot d\hat{f} \\
&= \alpha \cdot T_0 \cdot \int_{-\infty}^{\infty} e^{-\frac{(2\pi(\gamma\cdot\frac{1}{f_0})\cdot\epsilon\cdot f_0)^2}{2}} \cdot \mathrm{sinc}(\pi(\beta\cdot f_0 - \epsilon\cdot f_0)\alpha\cdot T_0) \cdot d\hat{\epsilon}\cdot f_0 \\
&= \alpha \cdot T_0 \cdot f_0 \cdot \int_{-\infty}^{\infty} e^{-\frac{(2\pi\gamma\epsilon\cdot f_0\cdot\frac{1}{f_0})^2}{2}} \cdot \mathrm{sinc}(\pi(\beta-\epsilon)\cdot\alpha\cdot T_0\cdot f_0) \cdot d\hat{\epsilon} \\
&= \alpha \cdot \int_{-\infty}^{\infty} e^{-\frac{(2\pi\gamma\epsilon)^2}{2}} \cdot \mathrm{sinc}(\pi(\beta-\epsilon)\alpha) \cdot d\hat{\epsilon}
\end{aligned}
$$

3.4.2 Numeric Application and Design Procedure

As the expression for the sine wave with a Gaussian and a squared envelope cannot be solved analytically (to the best of our knowledge), we need numeric analysis for expressing a link between the parameters of the signal. We make such an analysis in Chapter 11 where we use this type of signal for our integrated low-power UWB transmitter. The Matlab codes for this analysis are given in Appendix A.

Part II

Design and realisation of discrete-component IR-UWB testbed - The U-Lite Testbed

Chapter 4

Presentation of the discrete-components UWB Testbed

This chapter presents the discrete-components UWB testbed we developed during this work and the structure which it is presented in Part II. As already mentioned, the testbed we presented in Chapter 2 suffers from several drawbacks. The first testbed was more an experimental approach to Ultra Wideband communication rather than a true testbed. The testbed presented here is a much more advanced testbed which was called *U-Lite* testbed; its first description is made in the article [26].

The design and construction of the U-Lite testbed took approximately three years to be completed. In further separate chapters, we present all the fundamental elements of the testbed but in practice, many decisions and design considerations were made by considering the testbed as a whole. The further chapters present the circuits that constitute the testbed in details so that anyone can rebuild their own testbed and/or modify it with ease. Depending on the context, we focus more or less on several points that play a key role in the design and the construction of a given part. Because designing a whole circuit has a cost, considering we need to take care of the RF design and with the shielding box machining process, we use laboratory equipment and small evaluation parts of the components we target to use in order to have an easy way of building the architecture of the device. This explains why in [26] we could present the architecture of the U-Lite testbed although it was finished practically in 2010 (see Figures 4.3 and 4.4 for example).

We focus to design a Testbed that is relatively simple to build and to duplicate if desired, and so that anyone can build the same system for UWB experimentation. When we started this

work, there were already many publications about UWB testbed (see [29], [30], [31], [32] and [33]) but many of them are intended for integrated circuit designs or are not detailed enough to be reproduced with the assurance that they are exactly the same than the original.

The UWB testbed is a central part of this work because it is used for many experimentations that were subject to several publications ([34], [35], [10]), [36], [26], [16] and [15]). These publications are also a way to show that the U-Lite testbed is mature enough for being used in a wide range of experimental high level applications. It is also intended to be used in this work for testing the UWB low-power transmitters presented thereafter in Chapters 12 and 13, provided that these transmitters can work at the required frequency range.

4.1   Organisation of Part II

The realm of Part II is the presentation of the U-Lite UWB testbed and its use in several research applications. The design and construction of this testbed was made in a highly iterative way with several parallel improvements of its parts. The presentation of the elements of the testbed is presented in a linear way but in practice they should be considered as a whole where all the elements are closely related to each other (see Figure 1.8 in Section 1.2.1).

The first element required to build the testbed is a high frequency oscillator that can generate a 4.25 GHz sine wave for the UWB signal generation on the transmitter side, and, further, for the frequency down-conversion at the receiver side. The oscillator is presented in Chapter 5; its design was straightforward and only one prototype was enough to have a a circuit that works as expected. With the oscillator, the design of the transmitter was made with the focus on the generation of the impulse envelope that modulates the 4.25 GHz sine wave. This envelope generation requires several prototypes before having a circuit that fulfils exactly the expectations. We present the early prototypes in Section 6.1 and the final one in Section 6.2. This UWB transmitter is described also in the article [37].

The receiver is made of an amplification and filtering stage followed by a frequency down-conversion stage. The amplification is made by a Low-Noise Amplifier (LNA) designed to have a wide bandwidth and a voltage-controlled gain. The design and construction of the LNA was one of the greatest challenges of this work and it requires many experimental prototypes. We present a complete LNA circuit theory and all the preliminary prototypes of LNAs in Chapter 7 and the final device is described in detail in Chapter 8. This LNA device is also presented

in the article [38]. The frequency down-conversion requires, as mentioned earlier, an oscillator and a mixer but experimentations show that this is not enough in the case of asynchronous UWB short impulses. For this reason, we designed a novel architecture of UWB frequency down-converter based on I/Q mixer for doing the down-conversion and the energy detection in one step. This leads to the I/Q down-converter (or I/Q demodulator) presented in Chapter 9 and described in the article [39].

Part II ends with Chapter 10 that presents the experiments made with the U-Lite testbed. The testbed was used in several experimentations such that ranging, data transfer and security and all of these experiments were presented in articles or PhD works.

4.2   Overview of the *U-Lite* Testbed

In this section, we give a brief overview of the U-Lite testbed (see Figure 4.2). On the transmitter side, we can generate several concurrent IR-UWB signals with a bandwidth of at least 500 MHz. For this purpose, an FPGA creates several command signals that each drives an IR-UWB transmitter. Each command signal is a simple low voltage digitally controlled impedance (LVDCI) signal where rising edges correspond to a pulse transmission. The maximum clock frequency of our FPGA is 166 MHz. This translates to a minimum chip duration T_c of 6 ns (see section 1.1.5). We have the ability to fully control each parameter of the transmitted signal (see Equation (1.1) in section 1.1.5) and they can be configured by the computer through registers. An FPGA was chosen because it can manage high speed signals and a very flexible internal processing unit can be implemented easily, depending on the kind of experiment that is targeted. It is also easier to parameterize completely the physical layer of the UWB signal.

The FPGA is connected to each IR-UWB transmitter through a Micro DB connector. Hence, our analog IR-UWB transmitter was built to be robust to distortions of the command signal. Its architecture is depicted in Figure 4.1(a). An integrated PLL sine wave oscillator running at 4.25 GHz is connected to the antenna through a mixer. The mixer behaves like a switch when driven by a square signal. The output of the PLL is amplified before the mixer. An important part of the transmitter is the square impulse generator. Indeed, driven by a possibly degraded FPGA command signal, it has to reliably generate short squared impulses of 3 ns to drive the mixer. The duration of the pulse can be finely tuned with a trimmer. The receiver is a direct-conversion circuit (see Figure 4.1(b)) but with an I/Q mixer driven by a 4.25 GHz sine wave for managing the phase error between transmitter and receiver local oscillator that
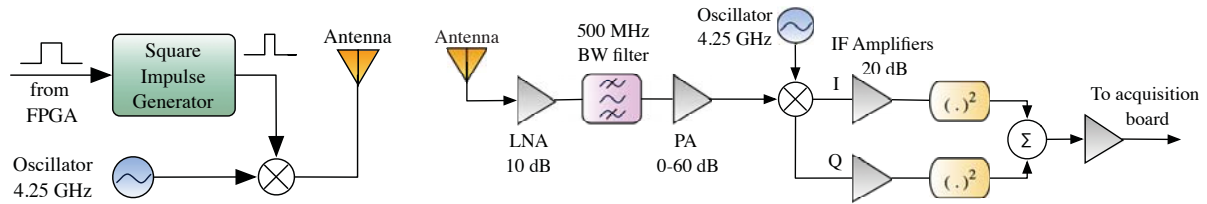
(a) The impulse generator generates a square impulse of about 3 ns. This signal drives the mixer that switches on and off the oscillator sine wave and produce the IR-UWB signal.

(b) The received signal is amplified and filtered before being down-converted by an I/Q-mixer. The mixer has its local oscillator frequency at 4.25 GHz. The baseband signal is amplified and sent to the FPGA for sampling.

Figure 4.1: Overview of the RF part of our experimental testbed.

Figure 4.2: A view on the U-Lite testbed (version 2009)

is inherent to asynchronous transmission. The signal from the antenna is amplified by two (or more) LNAs that include a power amplifier with a voltage-controlled gain. The signal is additionally band-pass filtered inside the LNA. The design of the antennas is described in [40]
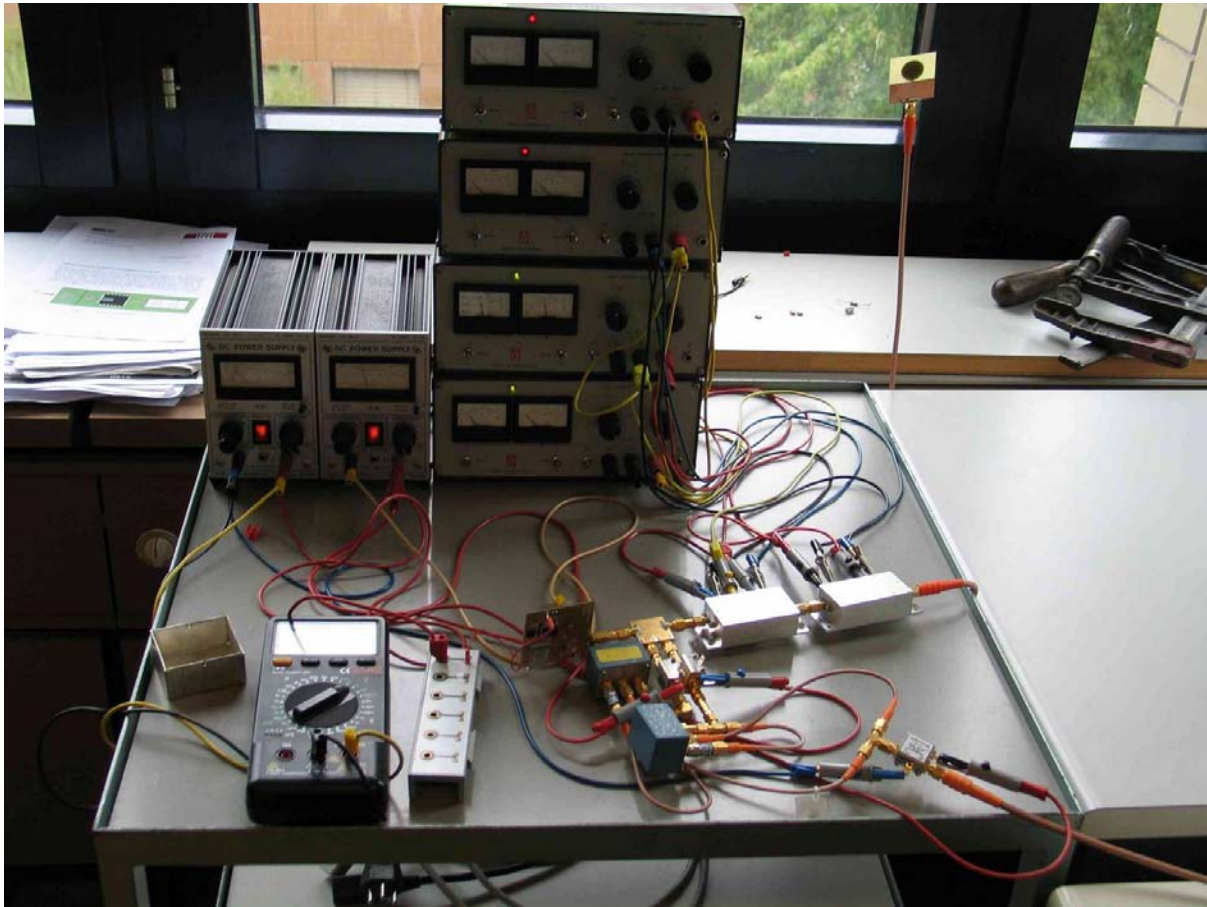
Figure 4.3: A view on the U-Lite Receiver part (version 2009)

and [41]. Most of our receiver is built around discrete components with off-the-shelf integrated circuits. Hence, we carefully designed them to avoid any undesired interferences and spurious coupling between components. We made sure to shield components whenever necessary to preserve the integrity of the received signal. The components used for the testbed as it was in 2009 are listed in Table 4.1. The U-Lite testbed is shown in Figure 4.2 and a closer view of the receiver of U-Lite is shown in Figure 4.3. At the beginning of the work (2009), the receiver was implemented with off-the-shelf RF modules such that amplifiers and conventional or I/Q mixers. The U-Lite testbed was completely finished in 2011 and is shown in Figure 4.4; the size is strongly reduced as is the reliability that is increased by the use of RF shielding boxes. The components required to build all the U-Lite testbed are listed in Tables 4.2, 4.3, and 4.4.
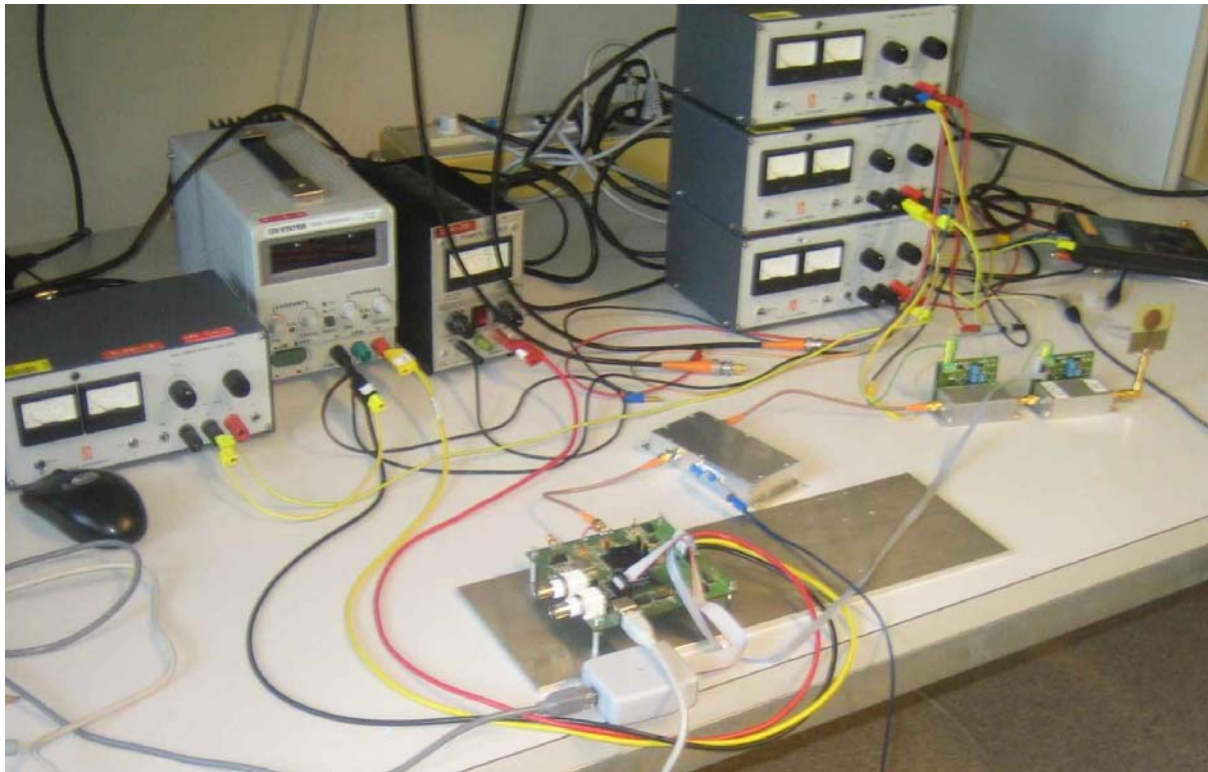
Figure 4.4: A view on the U-Lite Receiver part (version 2011)

FPGA	Virtex II Pro XC2VP70, Xilinx
Acquisition board	AC-240 (512 MB SDRAM), Acqiris
PLL oscillator	PCA 4260C-LF, Z-Comm
Switching mixer	HMC128, Hittite Corporation
LNA transistor	NESG2030M04, NEC
Power amplifier	MMIC MGA-85563, Agilent
I/Q mixer	HMC525, Hittite Corporation
Squaring mixer	ZLW-11, Mini-Circuits
IF amplifier	ZX60-3018G, Mini-Circuits
Duroid substrate	RO4003B, Rogers Corporation

Table 4.1: List of components used for the original (2009) Testbed

Miscellaneous passives	0402 case, $f_0 = 6$ GHz, Vishay
pHEMT Transistor	HMC128, ATF-35143 Avago Technologies
Power amplifier MMIC	MGA-86576, Agilent
Duroid substrate	RO4003C, Rogers Corporation
Aluminium case	ZG2-2-TR, Telemeter

Table 4.2: List of components used for the UWB Low Noise Amplifier (2011).

PLL oscillator	PCA 4260C-LF, Z-Comm
Microcontroller	ATTiny13, Atmel Corporation
"Slow" Comparator	ADCMP601, Analog Devices
"Fast" Comparator	ADCMP553, Analog Devices
Schmitt trigger inverter	NC7S14, Fairchild Semiconductor
Balun Transformer	CX2024, Pulse
Reference Oscillator	VX3@50MHz, Jauch Quartz
Switching mixer	HMC128, Hittite Corporation
Power amplifier MMIC	MGA-85576, Agilent
Duroid substrate	RO4003C, Rogers Corporation
Aluminium case	ZG3-2, Telemeter

Table 4.3: List of components used for the UWB Transmitter (2011).

3 - 7 GHZ I/Q mixer	HMC620LC4, Hittite Corporation
DC - 1 GHz amplifier	MAR-8ASM+, Mini Circuits Corporation
2 - 1000 GHz Mixer	ADE-R2ASK+, Mini Circuits Corporation
Duroid substrate	RO4003C, Rogers Corporation
Aluminium case	ZG4-2, Telemeter

Table 4.4: List of components used for the UWB I/Q Demodulator (2011).

Chapter 5

Oscillator

This chapter presents the oscillator used for both transmitter and receiver parts of the UWB testbed. This oscillator was designed in 2008 by Ms Jasmine Akhertouz Moreno during her Master semester project under the supervision of the author. This oscillator is an important component of the testbed because it plays a fundamental role in the impulse generation as explained later in Chapter 6. It plays also an essential role in the receiver for the demodulation of the high frequency UWB signal in order to acquire it digitally, as explained in Chapter 9. Because the specifications of such an oscillator are the same on both sides of the system, we decided to design one type of oscillator that is used on both UWB transmitter and I/Q demodulator, each one having its own local oscillator. These specifications, at this stage of the design, are the following :

- The working frequency is 4.25 GHz as the frequency band from 4.0 to 4.5 GHz is chosen.

- The precision and the stability of this frequency is important, although we work in a wide bandwidth, because of beats that could appear if precautions are not taken; this is widely explained in Chapter 9.

- The power consumption is not a key factor in this design because we target to fulfil the FCC regulations with a high accuracy for laboratory equipment and not for mobile devices. We can accept higher power consumption if this helps to reach accurately the FCC regulations.

- The oscillator should be small and use components easily available on the market. As for the power consumption, we can accept a higher price if this helps to reach accurately the FCC regulations.

For all these reasons, and after an extensive research on the market of components for building an accurate oscillator (see Appendix F.1), we decided to implement a PLL-based architecture.

5.1   The PLL synthesizer

This section focuses on explaining concisely the principle of a PLL-based oscillator and its advantages over other oscillator architecture in the context of our design. We do not intend to explain widely the fundamentals of PLL in this chapter, but only the essentials we need. The reader who wants to learn more on Phase-Locked Loop circuits can read the book [42]. Our device is based on a conventional PLL architecture that consists of the following elements, as shown in Figure 5.1:

- A Phase Comparator.

- A low pass Filter.

- A Voltage Controlled Oscillator VCO.
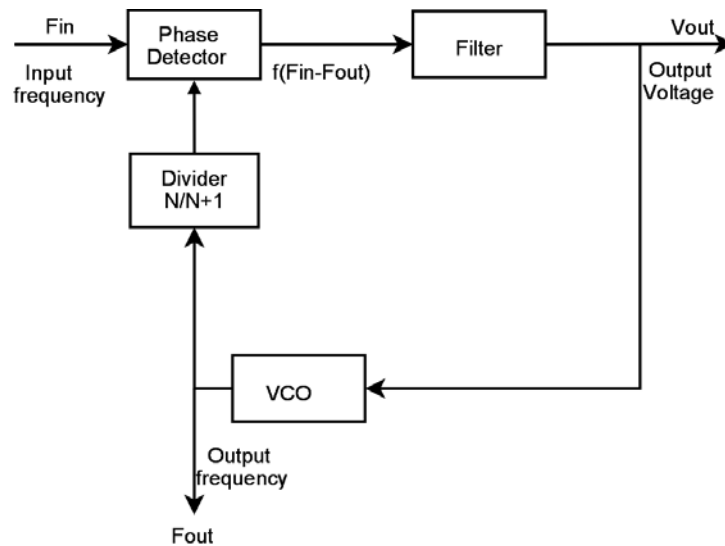
Figure 5.1: Phase-Locked Loop architecture

The circuit is fed with an input signal F_{in} that is the reference frequency, and the phase detector compares the phase of this incoming reference signal with the one that comes from

the VCO. The phase comparator gives an output voltage that is proportional to the phase difference (the phase error). The low pass filter is used to soften the phase error by eliminating the harmonic frequencies that are present in this signal, and let only the very low frequency part of the signal on the output. Basically, the idea is to generate a voltage that can drive the VCO frequency with the help of the feed-back in order to reduce the phase difference. Once the phase difference is equal to $0\,^\circ$ or $90\,^\circ$, the loop is locked and the frequency is stabilised. By incorporating a frequency divider, the frequency can be multiplied for generating signals at very high frequency with a high precision. This technique is used in the oscillator we use for the UWB testbed. In general, the frequency divider is a programmable logic circuit that allows the PLL oscillator to work in several frequency ranges. The PLL oscillator we designed fulfils the following specifications:

- Maximum power supply voltage of 5V.

- Output power higher than 10dBm for the passive mixer (see chapters 6 and 9).

- Working frequency of 4.25 GHz.

- Maximum circuit size of 50mm in order to be placed in a shielding box.

- Minimum current consumption but it is not a key factor.

According to this, we did an extensive market research for finding the best available components (see Appendix F.1) on the market. This research was made in 2009 and it is given for helping and guiding the reader who wants to implement the testbed with other specification than ours. From this research, we decided to implement a PLL-based oscillator with a PLL synthesizer PSA4260C-LF from the company Z-Comm. This synthesizer incorporates all the elements of the PLL and requires a microcontroller for programming its settings on the power up of the circuit. The synthesizer needs an external reference oscillator and a RF amplifier for producing the sine wave with the required power. These components are briefly described in thereafter.

5.1.1 The microcontroller

The chosen PLL synthesizer needs a microcontroller to set the correct values into its internal registers. A simple, easy to program and inexpensive circuit is enough, because it only loads once the PLL parameters into its registers. The best device found in the market is the Atmel microcontroller ATtiny13, which has the following specifications.

- 8-Bits Microcontroller

- 32x8 General Purpose Working Registers

- 1KByte of In-System Programmable Program Memory Flash

- Internal Calibrated Oscillator (no need of an external crystal)

- 8-pin PDI/SOIC: six Programmable I/O Lines (enough for the synthesizer)

- Operating Voltage: 2.7-5.5V (in the allowed range)

- Low Power Consumption (always good)

- Case: SO-8W (very small)

5.1.2   The reference oscillator

As explained before, the device needs an external reference clock for generating the RF frequency. This reference clock is a crystal oscillator with its own electronic control, and the choice of its value depends on the desired output frequency. The value of the frequency step R that the PLL synthesizer can follow is expressed in the following equation:

$$R = \frac{\text{Reference Frequency}}{\text{Step Size}} = \frac{50MHz}{10MHz} = 5$$

The value of 50 MHz is a good choice because it exactly divides the frequency of the output (4.25 GHz) and it is one of the highest available value, which ensures a good phase noise. This value fulfils also the limitation imposed on the R value given in the datasheet of the synthesizer, and it will be loaded in the R counter PLL register. The way this register is set will be explained later in Appendix B. The most suitable crystal oscillator found in the market that works at 50MHz is the VX3MH-5000 from Jauch. At this frequency, the current consumption is 15mA and it is a SMD device, which is ideal for the design.

5.1.3   The RF amplifier

The PSA4260C-LF offers an output power smaller than 10dBm. Because of this and also because a resistive network is required to exactly match the output of the synthesizer, an amplifier is required to increase the output power, such that the power specification is met. The amplifier we chose is the MGA86576 MMIC from Hewlett Packard. The RF amplifier and its passive

network add another degree of freedom in our design that would be useful later for fulfilling the FCC standards regulations.

5.1.4 Summary

We use a PLL-based synthesizer for designing the oscillator because it is easy to design, it deliver a stable frequency and it can easily be programmed to work at another frequency, if required. The use of an additional amplifier helps to determine precisely the output power in order to be FCC compliant. In addition, the synthesizer has reasonable power consumption. However, the chip needs an external reference clock to generate the output RF sine wave, and a microcontroller to configure the internal registers of the synthesizers. An overview of the oscillator's architecture we thus obtain is shown in Figure 5.2 :
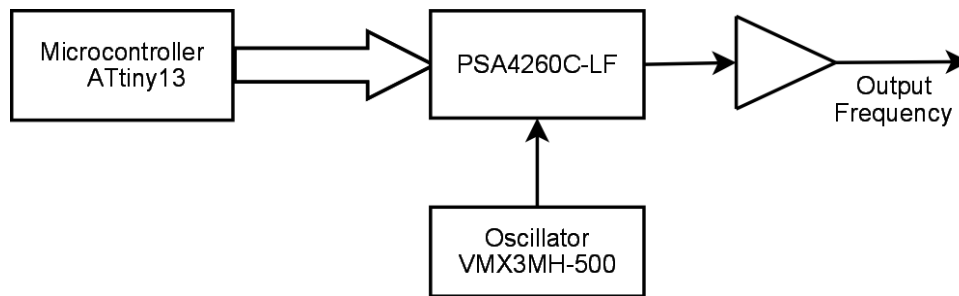
Figure 5.2: Functional block diagram of an oscillator based on a PLL

5.2 The schematic

The following section describes the schematic of the oscillator and explains how components are used and chosen. The function of all components used in the design is explained in detail. The schematic is given in Figure 5.3 thereafter. The schematic is divided in two main parts: the first part that we called the digital part, works at low frequency and consists of the ATtiny13, the switch, the crystal oscillator and the microcontroller's connector. The second part, that we called the RF part, works at high frequency and includes the synthesizer PSA4260C-LF, the RF amplifier and the SMA connector. Their functionality are explained in detail thereafter.

Figure 5.3: The schematic of the oscillator

The digital part

In this part, the ATtiny13 (U_1) is programmed through a dedicated connector (J_2) with a dongle and a computer. The dongle is the interface between the computer's serial port and the ports of the microcontroller dedicated to programming of its internal flash memory. More detail on how the dongle is made are given in [43] in case the reader needs to build one. A switch (U_2) is used between the microcontroller and the programming connector because the pins dedicated for the programming are also used for normal use for communicating with the synthesizer. The function of the switch is to disconnect the synthesizer (U_4) when the microcontroller is flashed because the synthesizer is an expensive component and we would avoid to destroy it in case the dongle has a failure. Once the programme is loaded in the microcontroller, the dongle is removed and the switches are turned on to allow the connection between the microcontroller and the synthesizer. This connection requires only three lines; we used the fourth switch available to force a reset of the controller in prevision of future debugging.

The RF part

The central element of this part is obviously the synthesizer PSA4260C-LF (U_4). The synthesizer RF output requires a resistive network in order to guarantee an exact impedance matching of 50Ω. This is due to the internal oscillator that is of LC type and which cannot oscillate if the mismatch is too high. The resistive network recommended by the manufacturer of the synthesizer is a cross pad attenuator that is studied in detail in Appendix E. According to the datasheet of the synthesizer and to our own study of the cross attenuator we chose $R_2 = R_5 = 27\Omega$ and $R_3 = R_4 = 68\Omega$ for which the attenuation is 10 dB. The output of the cross pad attenuator is thus amplified with the MMIC amplifier (U_5) which gives approximately 20 dB of gain, thus reaching the 10 dBm power we target. The MMIC amplifier's input is coupled through the capacitor C_7 while its output is coupled the SMA connector J_1 through the capacitor C_{10}.The MMIC amplifier is powered with a high impedance microstrip line that rejects the 4.25 GHz RF signal. The resistor R_6 is used to de-Q the microstrip line and the capacitors C_8 and C_9 are used for decoupling the power supply.

The reference oscillator U_3 gives directly the 50 MHz reference to the synthesizer. It is supplied with a voltage of 3.3V while the power supply voltage of the circuit is 5 V. As the reference oscillator works constantly, its consumed current is constant and we can use a simple resistor to produce the required voltage drop instead of a complete voltage divider. Assuming a

load of 15 pF and a working frequency of 50 MHz, it consumes a current of 15 mA according to its datasheet. Then, R_1 is calculated as follows:

$$R1 = \frac{Vcc - Vosc}{Icc} = \frac{5 - 3.3}{0.015} = 113\Omega$$

We chose $R_1 = 120\Omega$. However, with this value for R_1, the voltage is measured at about 4 V at the Vcc pin of the reference oscillator. The main reason for this discrepancy is the load introduced by the PLL device, which is much smaller than 15pF we expected. The current consumed by the oscillator is much smaller than 15 mA and R_1 must be higher. We experimentally determined that $R_1 = 180\Omega$ is a good value. The current consumed by the oscillator is:

$$I_{osc} = \frac{Vcc - Vosc}{R1} = \frac{5 - 3.3}{180} = 9.44mA$$

Finally, it is recommended to put the highest value capacitors close the power supply, and the smallest ones near the powered device. The reason for this disposition is that high capacitances attenuate low frequencies, which are more critical near the power supply. Conversely, the smallest ones attenuate high frequencies which disturb more the device.

The RF tracks used for RF signals is designed with a coplanar waveguide topology that is matched to 50Ω. The dimensions of the track are determined as done previously in Appendix A.1.1 and by considering the as smallest as possible width.

Passive elements

The table 5.1 sums up the function of each element.

Passive Element	Function
C_1	- Decouple U_1 (DC Block)
C_2,C_3	- Decouple U_3 - C_2 to attenuate low frequencies - C_3 to attenuate high frequencies
C_4,C_5	- Decouple U_4 - C_4 to attenuate high frequencies - C_5 to attenuate low frequencies

C_7	- DC Block U_5 to prevent accidental application of a voltage from U_4
C_9,C_8	- Bias decoupling network, DC block U_5 - C_8 to attenuate high frequencies - C_9 to attenuate low frequencies
C_{10}	- DC block on the output
R_1	- Voltage drop for U_3 - To filter voltage peak from the supply
R_2,R_3,R_4,R_5	- 10dB attenuation pad
R_6	- Bias decoupling Network - Provide the highest circuit gain over the entire 1.5 to 8 GHz frequency range

Table 5.1: Summary of the passive elements

5.3 The PCB layout

Designing a circuit that works at a 4.25 GHz implies we need to use Duroid$^{\text{TM}}$ as PCB material, which is more suited than FR-4 for very high frequency designs. This special material is intended for RF microwave circuits because it has smaller losses and more finely determined specifications. More generally, microwave circuits require special care in their design and in their construction (see Appendix C). The most important point to be careful of are the following:

- The material chosen to make the PCB is Duroid RO4003 instead of FR-4. Actually, RO4003 offers better characteristics until 10GHz. FR-4 is more suited to work until 2 or 3 GHz .

- Varnish should be avoided to protect the PCB surface in order to not modify the relative permeability of the material. For this reason, tracks should be chemically gold plated for oxidation protection and preservation of the electrical properties of the PCB.

- The PCB must have a wide and continuous ground plane. This ensures a return path for all signals and power supplies, as well as protecting the board from outside parasitic.

- All the elements must be Surface Mounted Device (SMD). The most important reason for this choice is that the circuit will be placed and glued inside a metallic shielding box. Thus, elements soldered through holes would create short-circuit.

- Cross lines should be avoided by getting the track going under the pad.

- Straight angles should be avoided, because, at this frequency, they produce reflections that can causes losses and mismatches.

- To avoid possible losses in copper tracks due to mismatch, the elements must be close as much as possible but by keeping a convenient distance that allows the soldering.

- Vias are essential in such kind of PCB for ground connection. They should be as small as possible, in enough quantity and regularly distributed along the PCB surface. As vias introduce a small inductance, we place several of them in parallel for sensitive circuits

By applying these rules when routing, we obtain the PCB layout as shown in Figure 5.4.
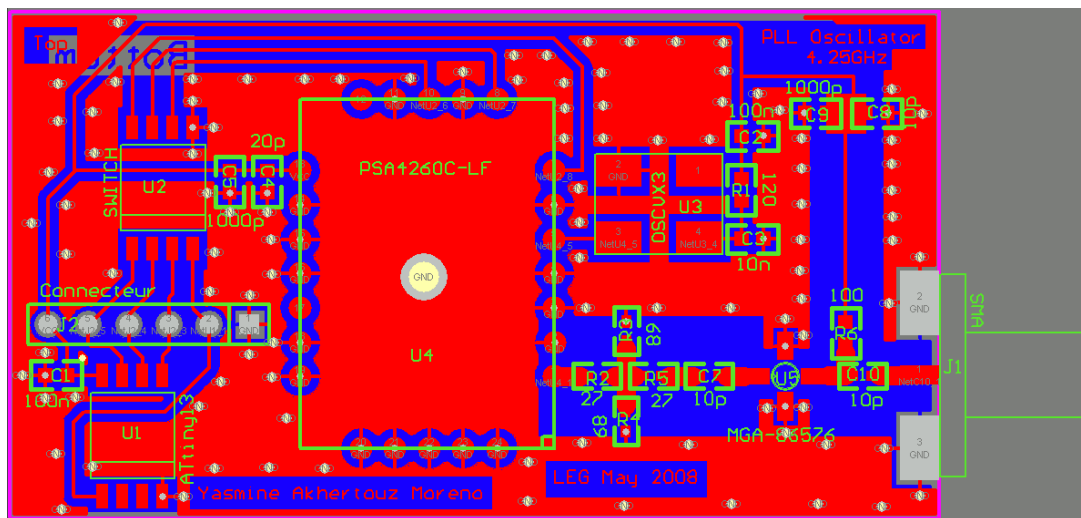
Figure 5.4: PCB layout of the oscillator

Most of the footprints used in the PCB are already defined in footprints library, more particularly:

- The Microcontroller Attiny13 and the switch: case SO8M

- The capacitances and resistances used in the supply: 0603

- The capacitances and resistances used in the RF tracks: 0402

- The connector SMA: SMA_STRIPLINE

- The amplifier: WW76

- Microcontroller's connector: SIP6

The passive elements used for the RF path have a size of 0402 because they offer a high resonant frequency suitable for working at 4.25 GHz. On the other hand, the lumped elements with a size of 0603 have low resonance frequency, so they are not appropriate for the RF tracks, but it is enough for being used in the supply as DC block. The footprint of the PLL chip PSA4260C-LF is made by following exactly its datasheet while the footprint of passive elements are all sligthly enlarged for a better soldering. In the case of the oscillator, we also create a footprint from its datasheet by with enlarge pads for an easier soldering.

5.4 Measurements

This section shows the experimental results and measurements in order to validate that the right frequency, power and spectral purity are achieved. We present improvements for future designs as they will be made in the testbed circuits in order to satisfy even better the specifications.

5.4.1 Time measurement

This measure is done by using a digital oscilloscope. We see in Figure 5.5 that the output frequency corresponds to 4.25 GHz.

The measure shows that the signal takes about 1.2 divisions. So, the measured frequency is:

$$f_{output} = \frac{1}{1.2 \cdot 200 \cdot 10^{-12}} = 4.17 \text{ GHz}$$

It is only a rough estimation because the oscilloscope does not give enough precision. In fact, the sine wave is sharp because the oscilloscope cannot acquire enough points to draw a smooth sine curve for such a frequency, as shown in Figure 5.5,.

5.4.2 Spectrum measurement

This measurement confirms with a high accuracy that the circuit generates the desired frequency at 4.25 GHz. The results are shown in Figures 5.6 and 5.7 .

The measurement shows also that there are no spurs near the working frequency. This PLL oscillator is thus a very good circuit to work with as a precise and clean local oscillator.
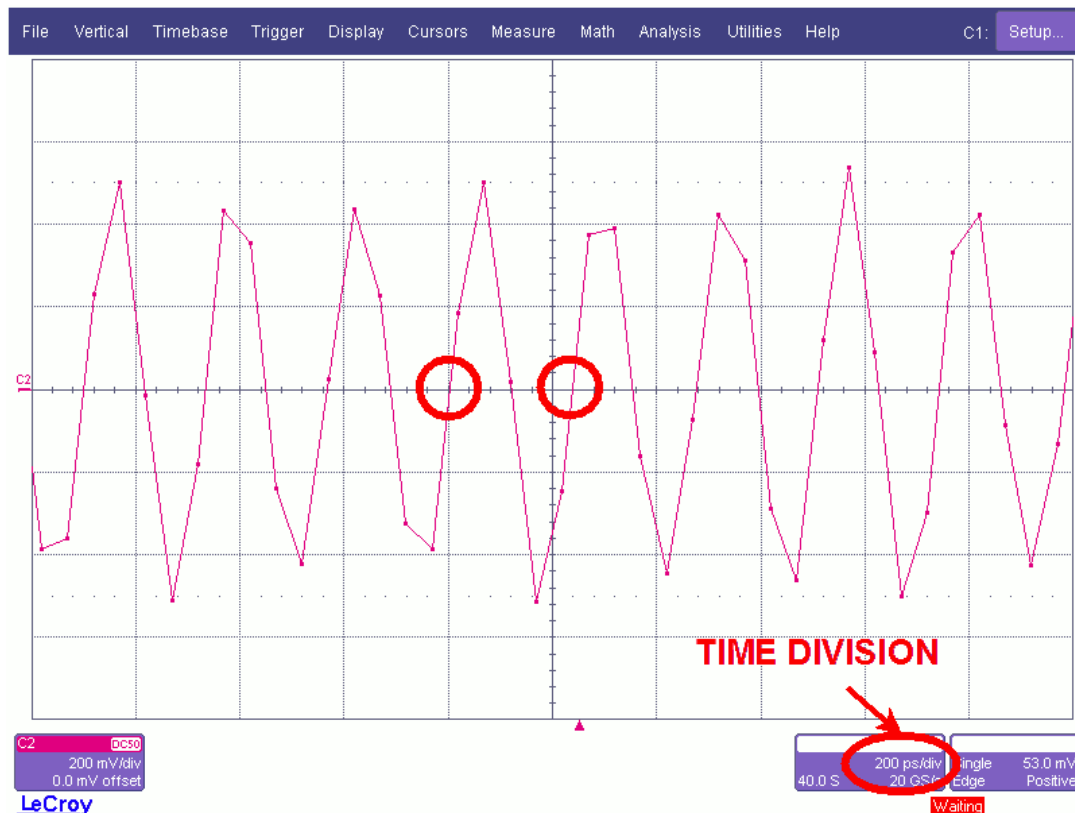
Figure 5.5: Sine wave measured at the output of the oscillator circuit

5.4.3   Noise floor

For this measure, the resolution of the analyser is increased to 20Hz. Figure 5.8 shows that the noise floor is at about to -60 dBm while the output sine wave is at 4.35 dBm.

5.5   Improvements and further implementations

Concerning the frequency, there is nothing to improve as the desired frequency specified in the requirement is reached. Nevertheless, from the previous measurements, the output power is a bit lower than expected but in practice this has no effect on driving a mixer. This is mainly due to some mismatches between the components along the output path that are caused by parasitic capacitances that could appear along the RF path. They can be decreased by moving closer the components of the output path, and also by improving the soldering as done later in final circuits (see Figures 5.9 and 5.10).
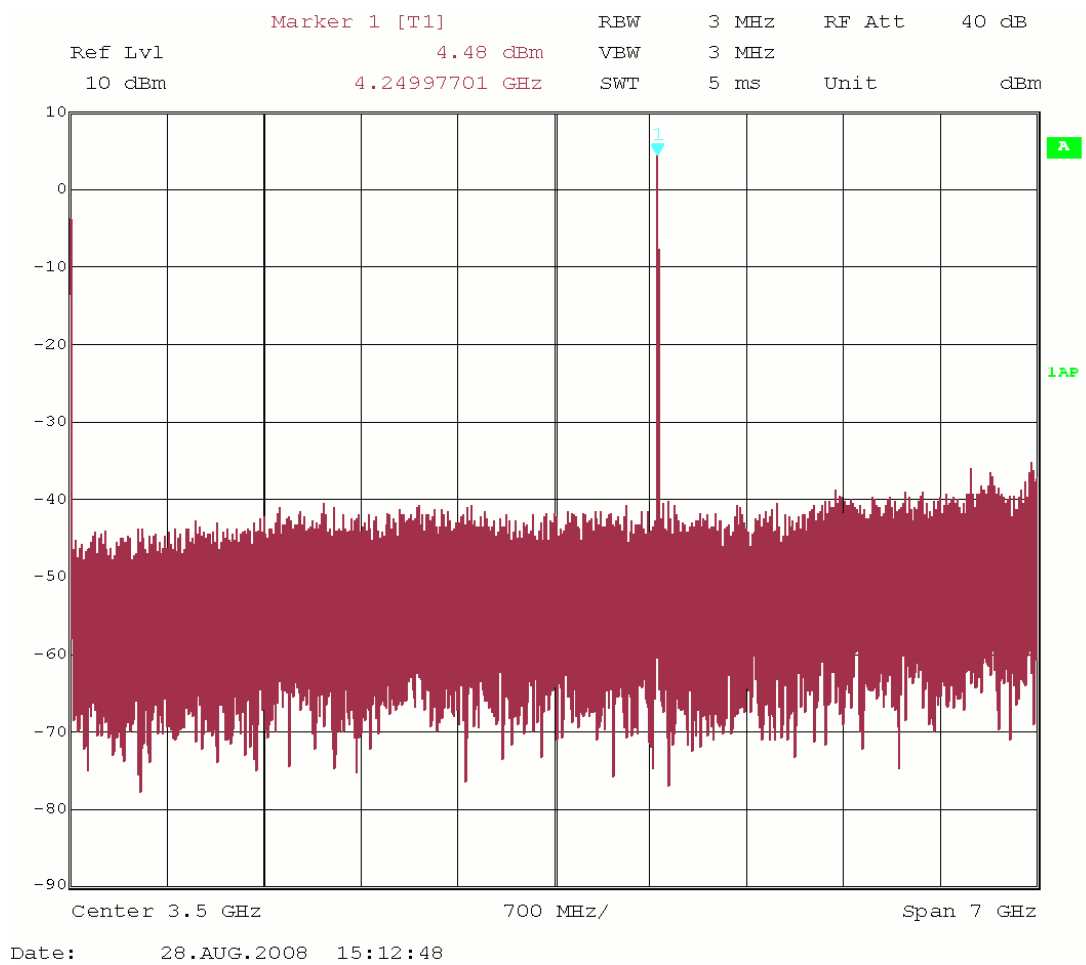
Figure 5.6: Spectrum with a bandwidth of 3MHz
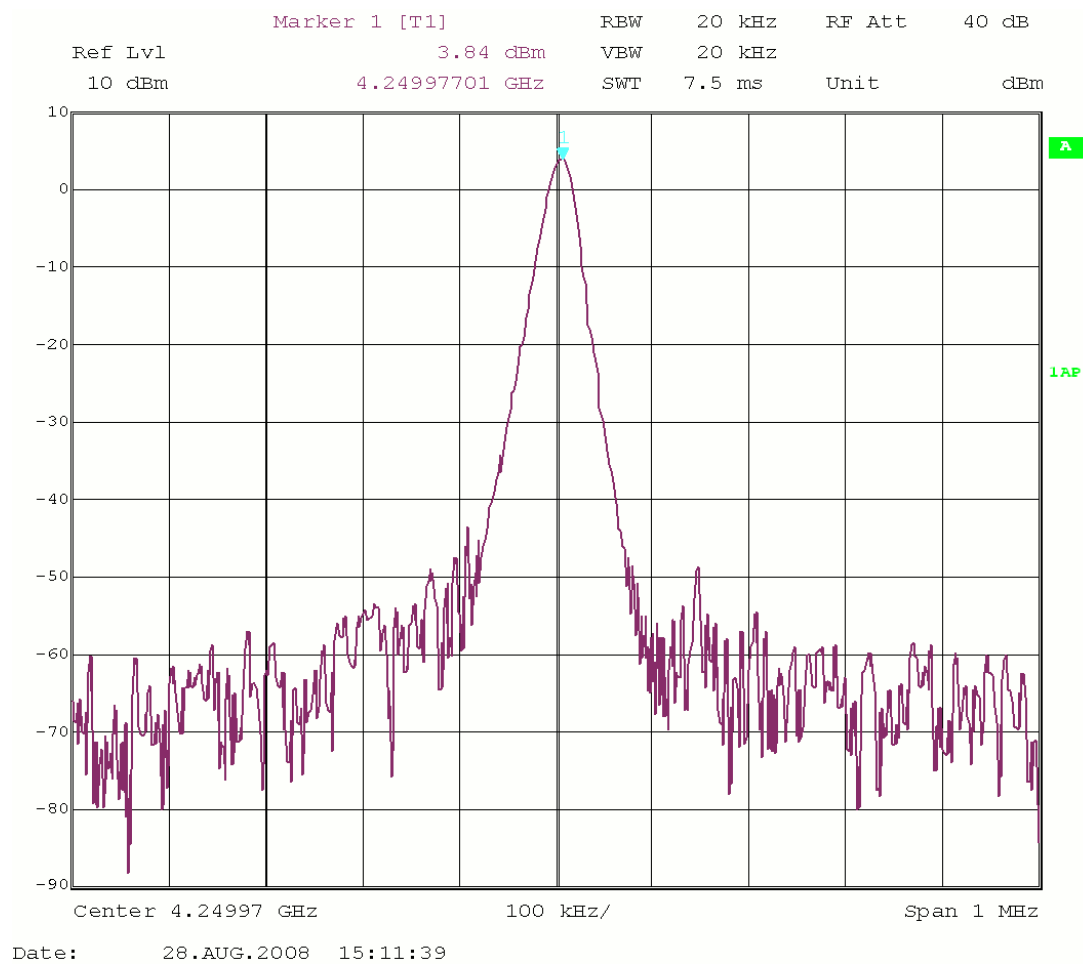
Figure 5.7: Spectrum with a bandwidth of 20KHz
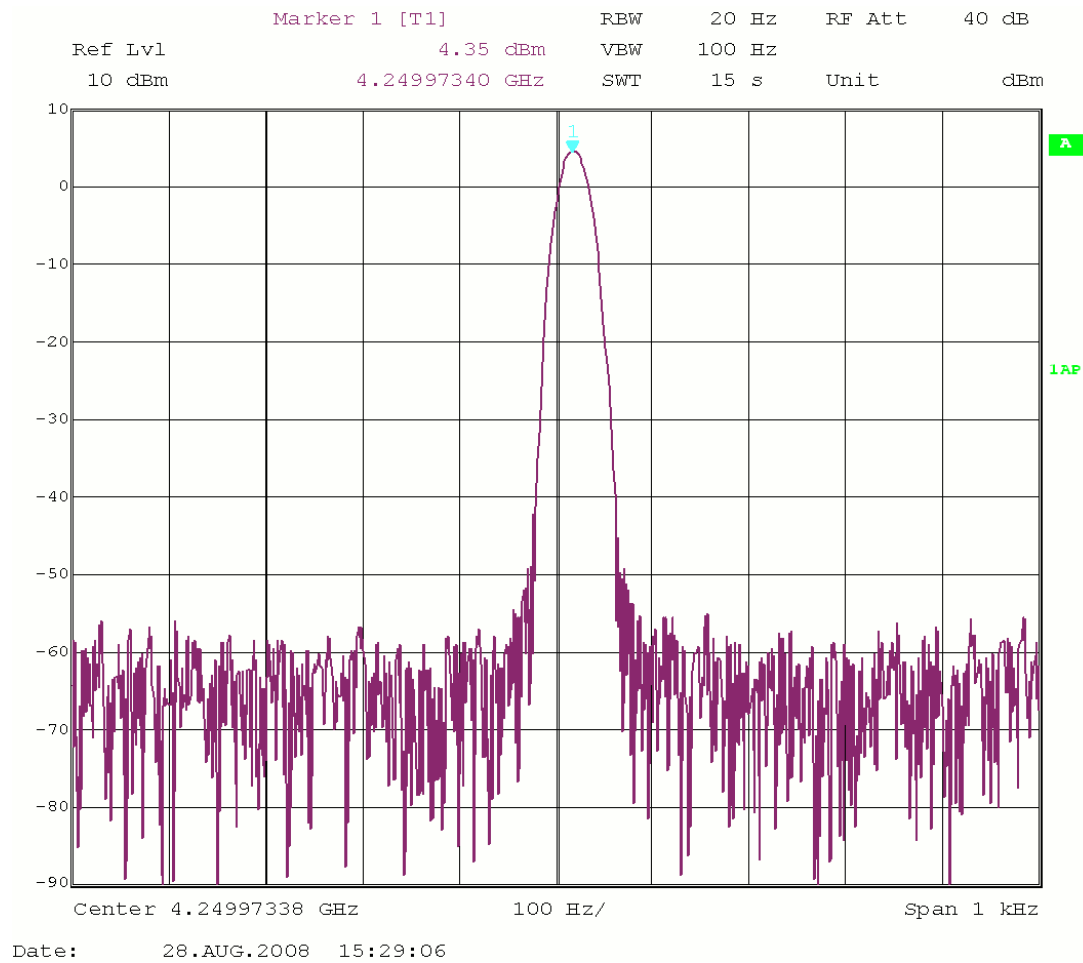
Figure 5.8: Phase noise at 20Hz
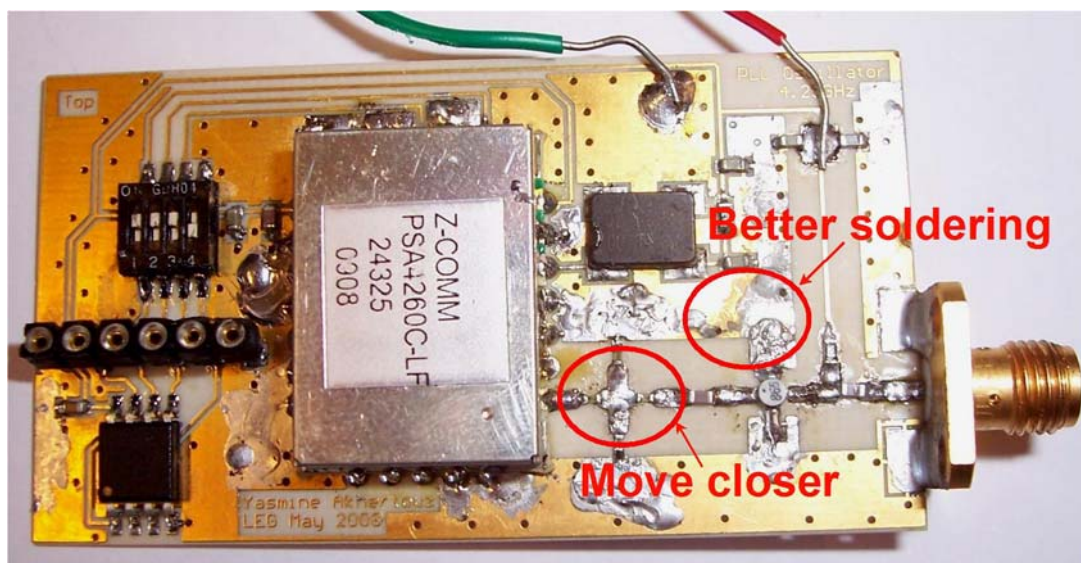
Figure 5.9: Suggested improvements

Figure 5.10: The final oscillator circuit, as it is used in the testbed

Chapter 6

UWB Transmitter

The UWB transmitter described in this chapter is a fundamental part of this testbed, if not the most important one as it has to meet and implement all the IR-UWB specification for making the testbed a "true" UWB system. As usual, as this circuit is specially intended for communication research community, we focus on simplicity and availability of the required components rather than pure technologic performance. In addition, in Chapter 2, we described a UWB transmitter based on SRD diode but it is very difficult to design a flexible and adjustable transmitter with this technique. In our scenarios, we want a UWB transmitter that implements as accurately as possible the official standards of UWB. The objective is thus to make the circuit simple, generic, and to avoid the need for the high-level background and technical infrastructure required in IC design. In order to make our testbed reproducible at reasonable costs, we chose to build it with off-the-shelf discrete components. There are no constraints on the power consumption. The 4.0 to 4.5 GHz band was chosen from the allowed UWB band [9] because there is no other transmission system that sends signals into it. Thanks to its generic architecture, it is easy to modify the transmitter in order to work in another frequency band or with a wider bandwidth, depending on the needs of the users.

For robustness and flexibility, our UWB transmitter is based on a classic architecture (see [44], [45] and [46] for example) as shown in Figures 6.2 and 6.15. An oscillator based on a PLL synthesizer produces a 4.25 GHz sine wave that is switched on during about 3 ns. The duration of the driving impulse is adjustable, as explained later. The mixer, when driven by a digital impulse, behaves like a switch. The square impulse generator is driven by a rectangular signal coming from a FPGA and converts each incoming digital impulse into a fast switching

impulse. The FPGA board is the model AC-240 from Aquiris and belongs to the specifications. The maximal clock frequency of the FPGA is 166 MHz, hence the chip time (the duration of a bit, see Section 1.1.5 and [26]) is limited to a minimum of 6 ns. The output UWB signal is sent to an omnidirectional antenna (not described in this work but in [41]) that has a 50Ω impedance.

The design and development of the UWB transmitter followed an incremental process, as it is the case for the LNA described later in this work. We started from the measurements of the SRD diode pulser and we try to do better. The starting point is to take a mixer, an oscillator as the one of Chapter 5, and a laboratory impulse generator, the HP8131A we already used for driving the SRD pulser. By setting the impulse generator to deliver a pulse that lasts about 3 ns, we obtain the UWB signal shown in Figure 6.1. The duration of the pulse is obtained empirically here but we demonstrate in Chapter 3 that this duration gives the expected spectrum shape.
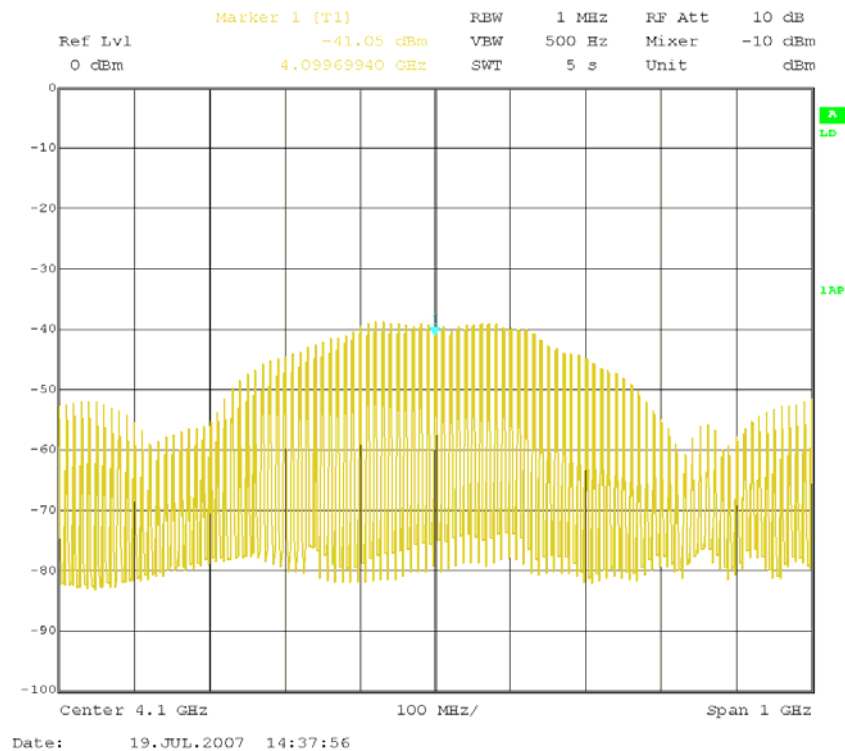
Figure 6.1: The ideal pulse obtained with laboratory equipment (HP8131A, oscillator and HMC128 mixer)

According to this result, the challenge here is to replace only the HP8131A impulse generator by our own one made with discrete off-the-shelf components, and that can be driven directly by the FPGA board (or any equivalent digital equipment that implements the IR-UWB

physical layer), as the mixer and the oscillator are already available. Replacing this heavy and costly equipment is a challenge in itself because our own circuit has to generate extremely short impulses (about 3 ns) without the use of exotic components like, for example, the SRD diode we used for the pulser. This means we need to design a new architecture of circuit and to investigate technologies of logic circuits that could be able to manage so short impulse durations. For this purpose, we developed two kind of prototypes: the first one, presented in Section 6.1, is based on two concurrent impulses that are delayed by a slightly different delay and combined by a logic gate; the second one, presented in Section 6.2, is based on one impulse that is shorten by comparators and a tunable trimmer capacitor that adjust the weight of the capacitive load seen by a gate. Our final UWB transmitter is designed by using this last approach that showed better results.

6.1   UWB Transmitter prototype n° 1

As mentioned previously, the working principle of the prototype n° 1 is to delay the incoming signal and to combine it with a AND gate, as shown in Figure 6.2. We consider this approach because we target to generate very short impulses with conventional general purpose components from the market. When we started to design the transmitter (in 2007), very high speed component were more difficult to find as nowadays so we intended to generate very short impulse of 3 ns with lower speed but more easily available components.
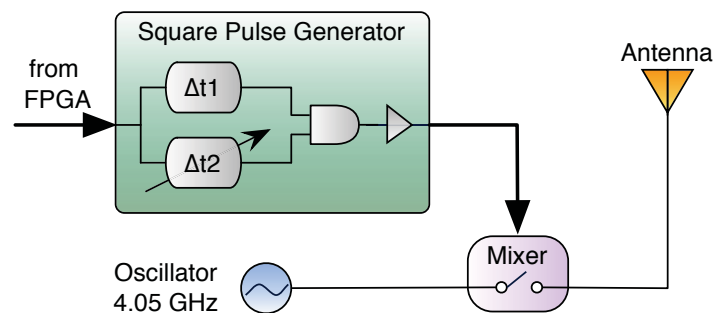
Figure 6.2: The principle of generating very short impulses

6.1.1   UWB Transmitter prototype n° 1, version 1

The first version of prototype n° 1 (version 1.1 for short) is probably one of the simplest we can imagine. We use an EXOR gate that is fed-back by its own output (see Figure 6.3). An EXOR gate can be understood as an inverter for which we can activate or not the inverting function. In

other words, according to the level at one of its input, the other input is duplicated to its output by being inverted or not. According to that, if the incoming signal is low, the output is low and the other input is also low, thus nothing happens because it is a stable state. When the incoming signal becomes high, the EXOR starts to become an inverter and its output oscillates between low and high level. We expect that, as the incoming signal from the FPGA lasts at most 6ns, the output has only the time to rise and fall once but no more. At this point of the development, we are aware that the pulse will last about 4.5ns (i.e. the propagation delay of the gate) and could hardly be shorter but we target to validate the principle and to test the effect of an adjustable capacitor at the output of the EXOR gate. The remaining part of the schematic is made of an amplifier for adjusting the output voltage for the mixer; it is almost the same as it was already made with SRD pulser.
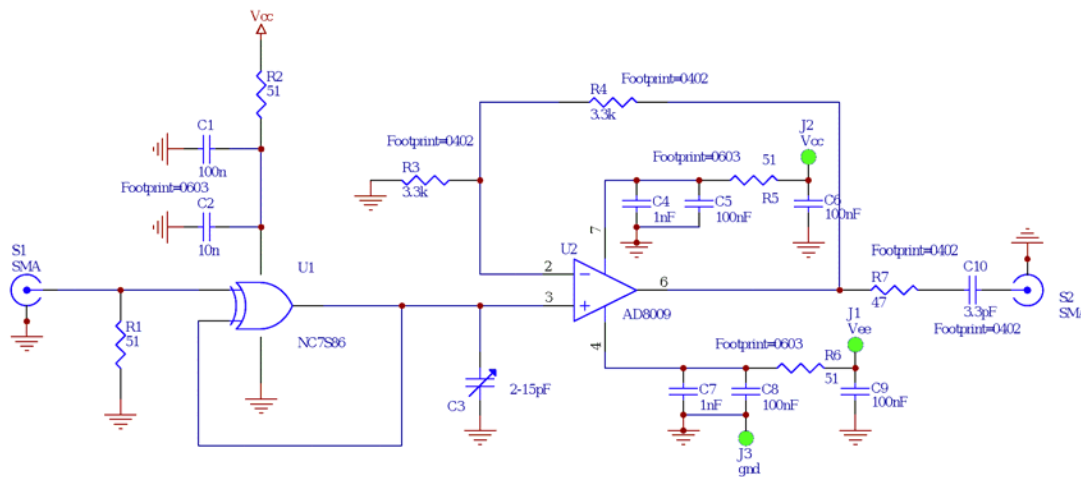
Figure 6.3: Schematic of UWB Transmitter prototype nº 1, version 1

The PCB of prototype version 1.1 is shown in Figure 6.4. We use several decoupling capacitors and SMA connectors for an easy connection with mixer evaluation board. The power supply voltage should never go above 6 volts.

The measurements of the prototype version 1.1 are shown in Figures 6.5 and 6.6. These measurements are made by connecting the prototype to the HMC128 mixer on IF input, a 4.05 GHz sine wave (we did not have the 4.25 GHz oscillator at that time) on the LO input and measuring at the RF output of the mixer. Figure 6.5 shows a surprising very well shaped UWB spectrum that could be used for more advanced UWB experimentations. However, Figure 6.6 shows that in the time domain the signal lasts much longer than expected and thus it does not comply with our specifications. In fact, the first two nanoseconds of the signal are excellent but there is the tail that comes from the second triggering cycle of the EXOR gate. Unfortunately,
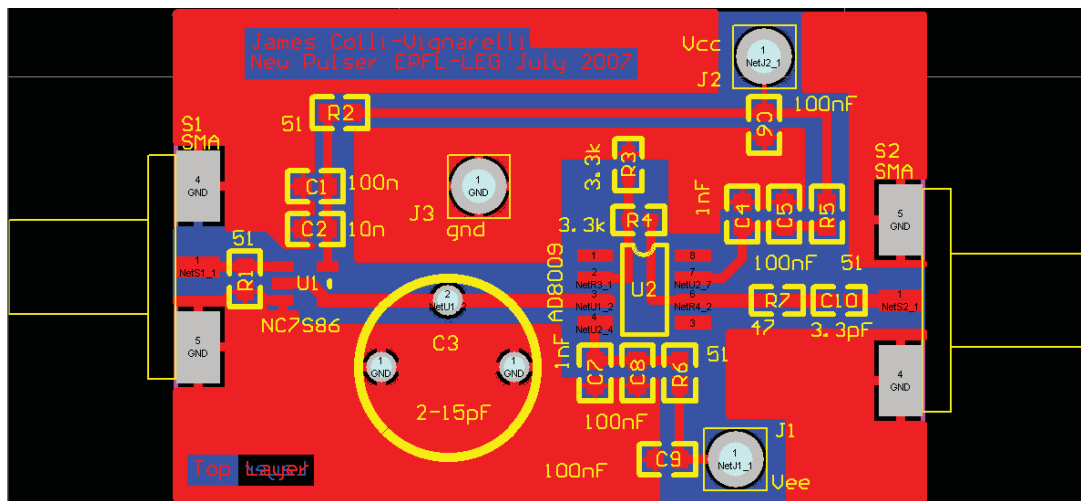
Figure 6.4: PCB of UWB Transmitter prototype nº 1, version 1

it is not possible to decrease or remove this tail with the trimmer, even with a bigger or smaller capacitance value.

Figure 6.5: Signal of UWB Transmitter prototype nº 1, version 1, in frequency domain

The prototype version 1.1 shows encouraging results but is too simple for our target. We can hardly adjust the duration and the control on the width of the spectrum is poor because of
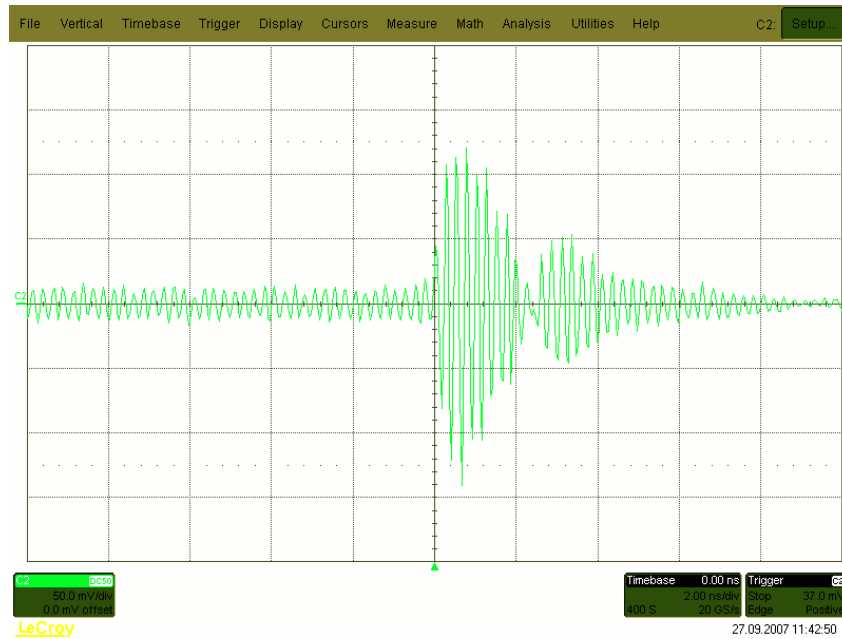
Figure 6.6: Signal of UWB Transmitter prototype nº 1, version 1, in time domain

the tail. However, the gate is able to generate a very short impulse although is has a longer propagation delay the duration of the pulse itself. This shows that the mixer does not need to see the output of the gate to reach the logic high level voltage. We consider the delayed signal combination for our further prototypes.

6.1.2   UWB Transmitter prototype nº 1, version 2

For the version 2 of prototype nº 1, we use the principle described in Figure 6.2 (see Figure 6.7 and Figure 6.8 for the timings). The incoming signal is sent to two cascades of two inverters each. The two inverters are required to compensate the inversion function and the two cascades are almost the same, excepted one that has a much higher capacitive load than the other in order to delay by few nanoseconds the signal. The AND gate triggers only when both signals are high and thus, a longer delay decreases the duration of the impulse at the output of the AND gate. This approach has the advantage to work even with gates that have a propagation delay longer than the pulse we want to generate (this propagation delay is of 4.5 ns, depending on the power supply voltage for the logic family we consider here). This consideration applies also for the AND gate because the propagation delay is defined in order to reach one logic level in comparison with the opposite one but our circuit is designed to drive a mixer that is much more sensitive than similar other logic gates. This means that, even if the propagation delay

is longer, we expect to have a small output impulse anyway that would be able to trigger the mixer for about 3 ns. An adjustable trimmer capacitor is largely enough for modifying the load of the inverter and to provide a fine adjustment of the duration of the pulse.
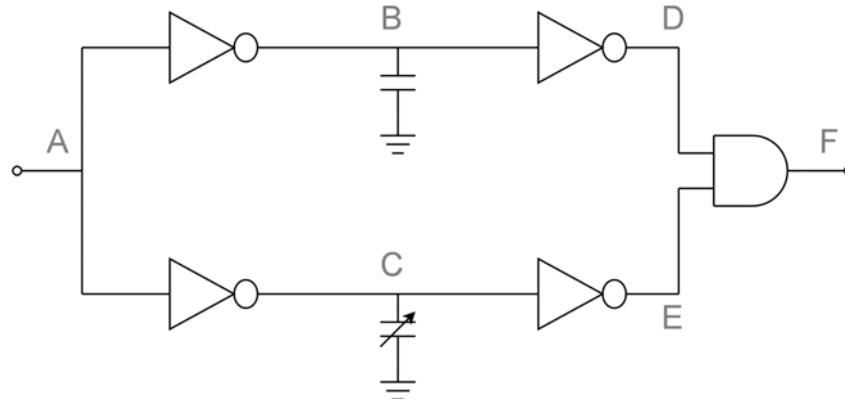
Figure 6.7: The principle schematic of the prototype nº 1, version 2 square impulse generator circuit.

The schematic of the transmitter version 1.2 is shown in Figure 6.9. This Figure implements exactly the principle described in Figure 6.7 and the operational amplifier remains the same as for version 1.1. The constant capacitor is chosen to 1 pF and the trimmer has a range from 5 to 60 pF.

The PCB layout of the transmitter version 1.2 is shown in Figure 6.10; the same observations as for version 1.1 hold.

The measurements of the prototype version 1.2 are shown in Figures 6.11 and 6.12. These measurements are made by connecting the prototype to the HMC128 mixer on IF input, a 4.05 GHz sine wave (we did not have the 4.25 GHz oscillator at that time) on the LO input and measuring at the RF output of the mixer. As for version 1.1, Figure 6.11 shows a surprising very well shaped UWB spectrum that could be used for more advanced UWB experimentations. However, Figure 6.12 shows that in the time domain the signal lasts much longer than expected and thus it does not comply with our specifications. This version 1.2 of the transmitter shows no improvement of that point and, unfortunately, it is not possible to decrease or remove this tail with the trimmer, even with a bigger or smaller capacitance value.

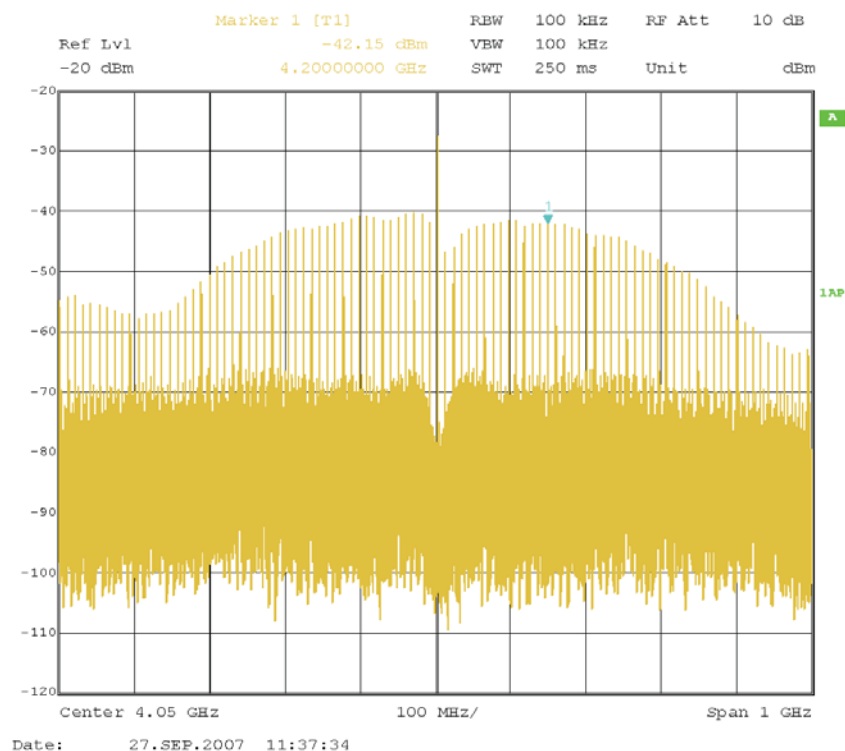The prototype version 1.2 shows no improvement on version 1.1 and we still have the tail in the time domain. We can hardly adjust the duration and the control on the width of the spectrum is poor because of the tail. We assume that the tail occurs because the mixer is coupled in a capacitive way to the output of the operational amplifier (see C_{19} in Figure 6.9). This capacitor is required because the amplifier delivers a DC voltage that could destroy the mixer if it is not
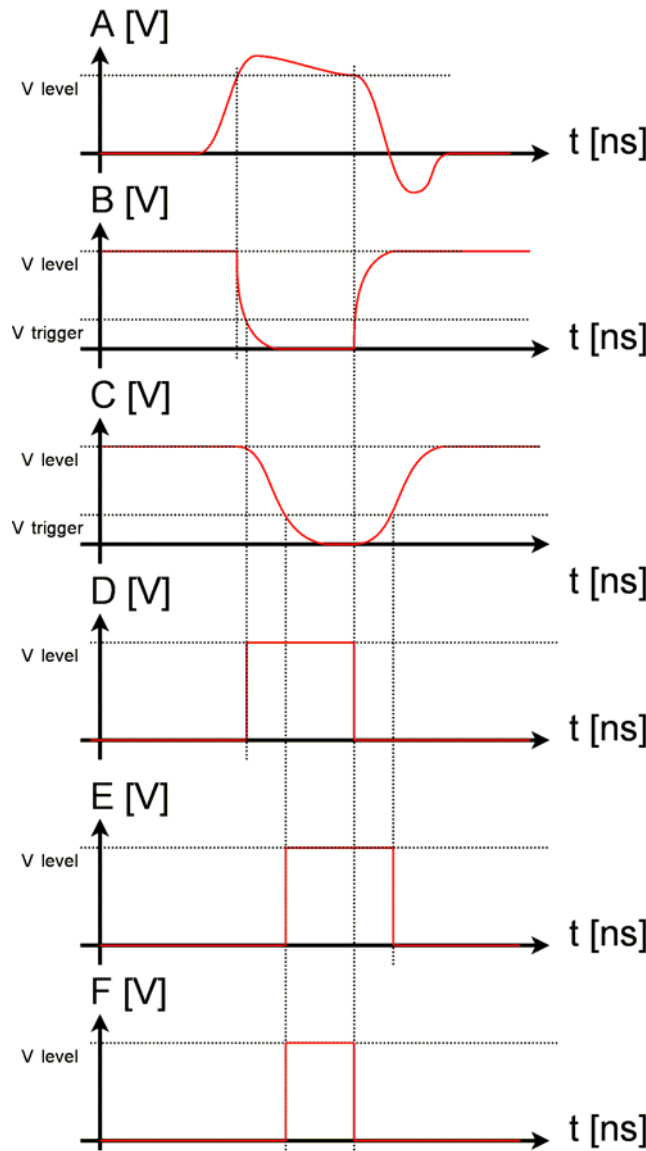
Figure 6.8: The signals involved into the prototype nº 1, version 2 square impulse generator circuit.

removed. However, it is possibe that the capacitor is too small and when the impulse goes down, it produces a negative impulse that triggers on the mixer and thus causes the tail. The duration of the tail is the time required for the capacitor to completely discharge.

6.1.3   UWB Transmitter prototype nº 1, version 3

In version 1.3, we add a DC voltage on the input such that the inverters are close to their metastable point in order to have an extremely short impulse that lasts about 3 ns with the tail
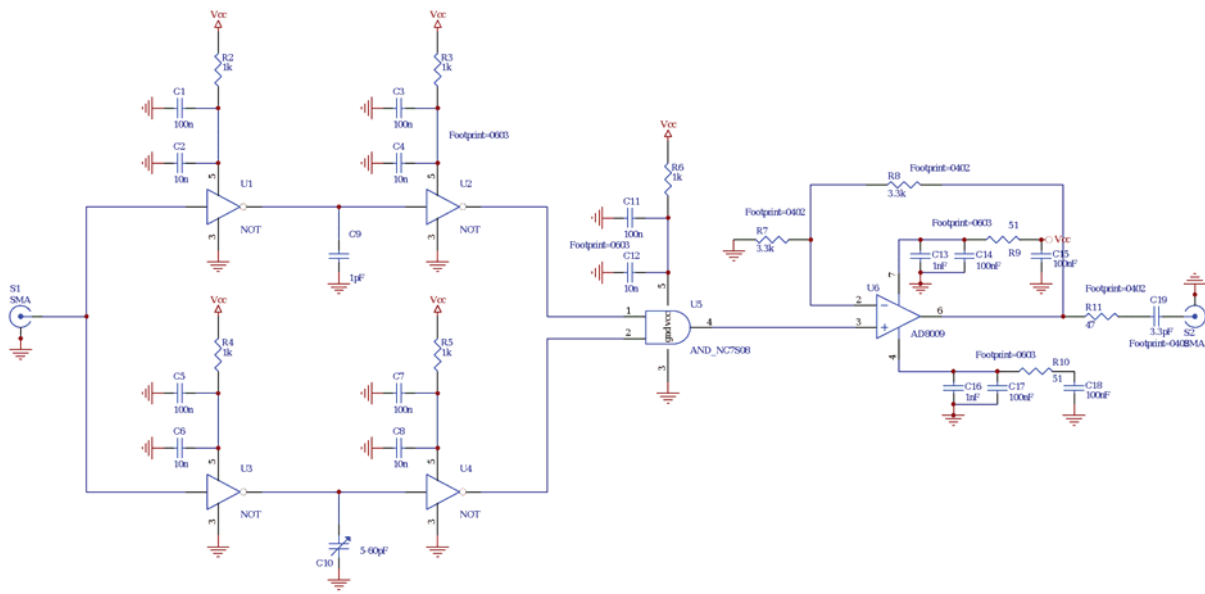
Figure 6.9: Schematic of UWB Transmitter prototype nº 1, version 2
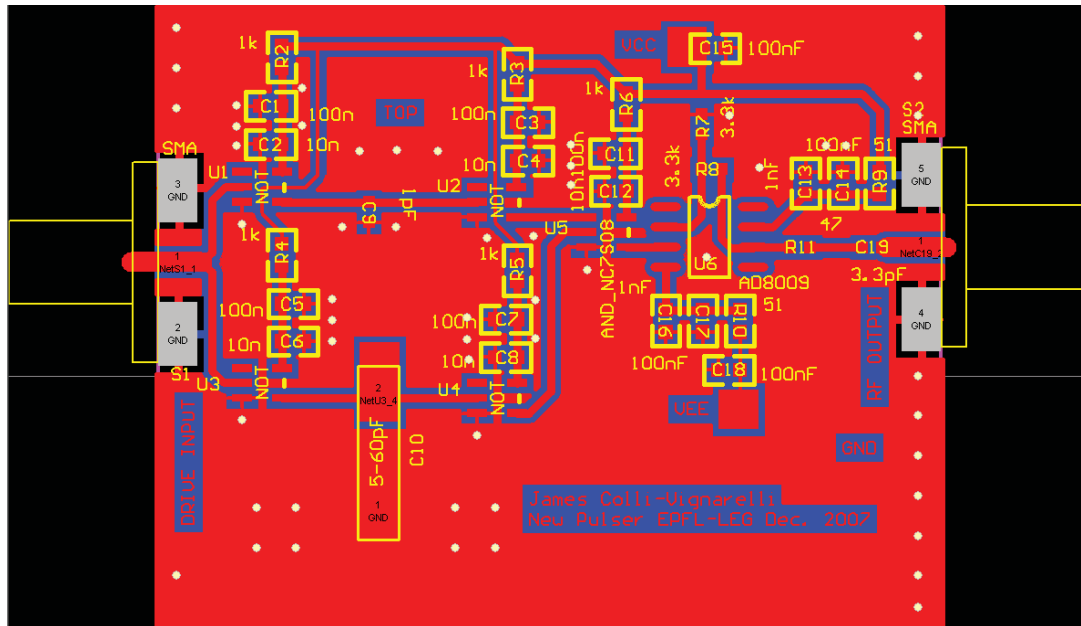
Figure 6.10: PCB of UWB Transmitter prototype nº 1, version 2

included. We also increase C_{19} to 33pF. We try this approach as an experimental one for taking advantage of the tail that we can hardly be removed with this architecture. The schematic and PCB layout of the prototype version 1.3 are shown in Figures 6.13 and 6.14 respectively. Unfortunately, the measurements show no improvement on the previous prototypes (they are similar to Figures 6.11 and 6.12).
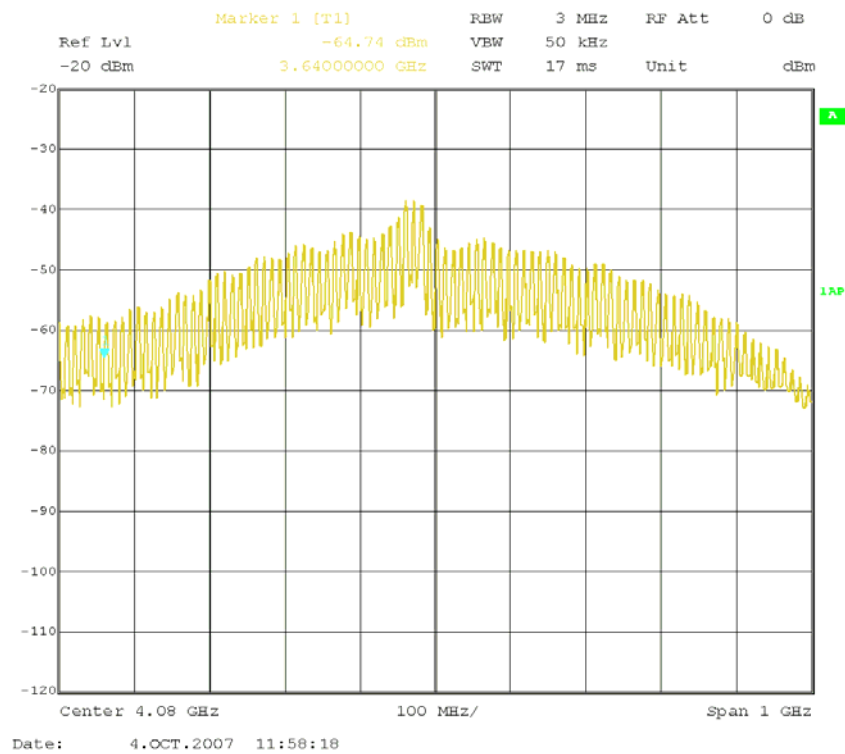
Figure 6.11: Signal of UWB Transmitter prototype nº 1, version 2, in frequency domain
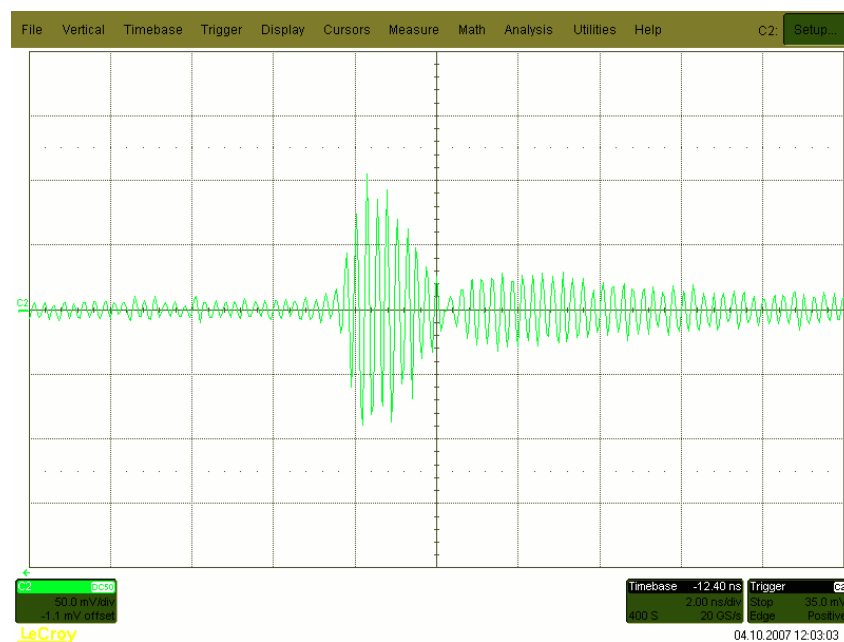
Figure 6.12: Signal of UWB Transmitter prototype nº 1, version 2, in time domain

6.1.4   Conclusion about Prototype nº 1

The prototype nº 1 looks like a good idea at the beginning but it has the drawback of the tail that would be an interesting approach if the tail would be removed. At this point, we focus on
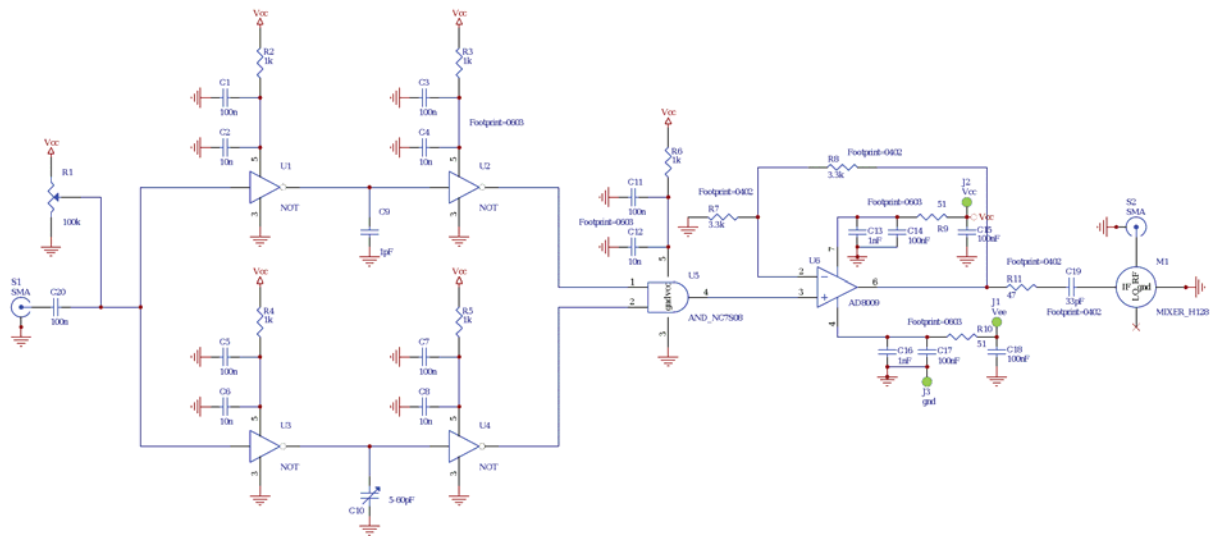
Figure 6.13: Schematic of UWB Transmitter prototype nº 1, version 3
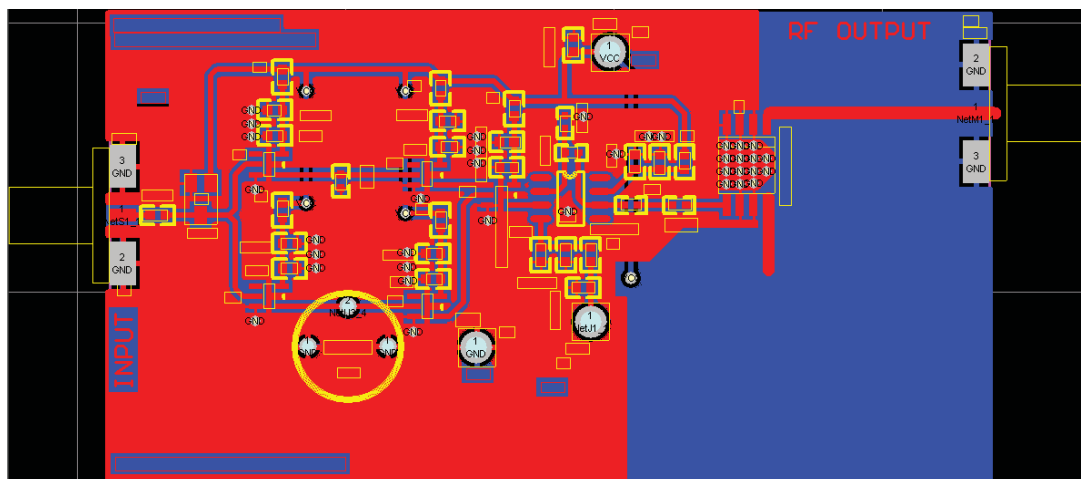
Figure 6.14: PCB of UWB Transmitter prototype nº 1, version 3. The blue zone on the bottom left corner is dedicated for the oscillator that is on another board.

removing completely the coupling capacitor in order to send to the mixer exactly a rectangular impulse without distortion. We also focus on finding much better and faster logic gates.

6.2   UWB Transmitter prototype nº 2

As prototype nº 1 was not good enough for producing the expected UWB signal, we developed another alternative approach, based on comparators for shaping the incoming signal instead of logic gates. The prototype nº 2 of the transmitter is based on very fast comparators that use PECL (Positive Emitter Coupled Logic) logic elements. This logic family is differential and needs a DC biasing for working properly. A balun is used to transform the differential signal into a unipolar one without any DC voltage, as we targeted to do with the prototype nº 1. The architecture of this prototype is summarized in Figure 6.15 and more precisely in Figure 6.16.
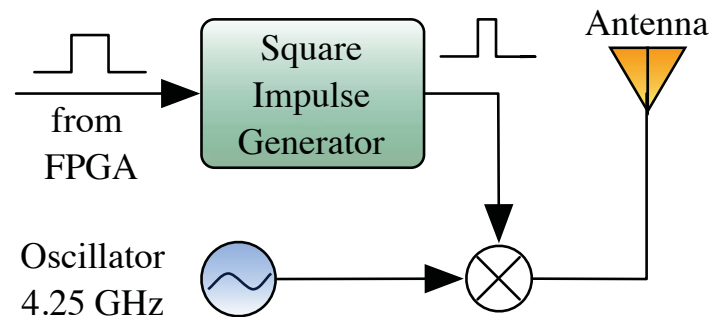
Figure 6.15: *Overview of the Transmitter.* The transmitter is made around a PLL synthesizer that creates the 4.25 GHz sine wave. This signal is switched on during about 3 ns by the mixer driven by the impulse generator. This makes the radiated signal to have a UWB spectrum. These impulses are produced from the bitstream of the FPGA board (not shown in Figure) every time a logic one is sent. The duration of a bit from the FPGA (chip time) is 6 ns. The antenna does not belong to the transmitter and is connected outside.

6.2.1   Schematic of the Transmitter

Overview of the Circuit

The complete schematic of the UWB transmitter is shown in Figure 6.16. The upper part is dedicated to the PLL synthesizer and the lower part is dedicated to the square impulse generator. Many decoupling capacitors are required because almost every integrated circuit has its own power supply voltage; these voltages are obtained by inserting resistors between their corresponding circuits and the main power supply. This is possible because the circuits have a constant current consumption (we can neglect current transients, thanks to the 10 nF decoupling capacitors).

Figure 6.16: *The complete schematic of the UWB Transmitter.*

The PLL Synthesizer
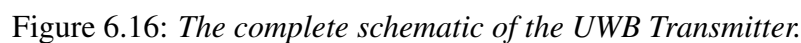
The PLL synthesizer is the one described in Chapter 5.

Description of the Square Impulse Generator

The square impulse generator takes the pulse coming from the FPGA board and reshapes it in order to obtain a very short impulse of approximately 3 ns that drives the mixer. As the FPGA board connections have poor impedance matching characteristics (point A in Figure 6.16), the signal first has to be squared by a comparator in order to obtain the original rectangular signal (point B). The comparator triggers at V_{tune1} level and a Schmitt-trigger inverter is then used as a buffer for driving a capacitive load (point C), which produces a triangular signal that is made of arcs of exponentials. The capacitance is variable, and this is how the pulse duration is adjusted (in conjunction with V_{tune2}). A fast PECL logic-based comparator triggers this signal at the V_{tune2} level to produce the short impulse (points D and E). As the PECL logic defines the low level at 1.3 volts and the high level at 2 volts and uses balanced signals, a balun transformer is required to obtain the same signal with unbalanced polarity and no DC voltage level. In the

schematic, the DC voltage is obtained with a resistive divider, which gives 1.3 volts with a 50Ω impedance. As the balun, like the divider, has an impedance of 50Ω, the total impedance seen by the output of the PECL is 25Ω, which is in the driving range of the circuit. The typical signals involved in this circuit are shown in Figure 6.17.
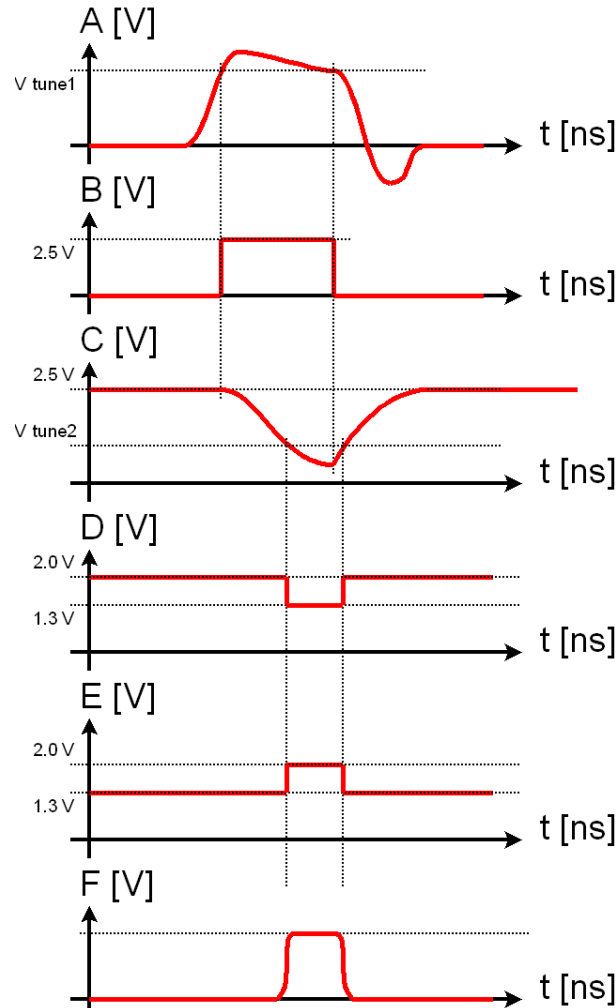
Figure 6.17: *The signals involved into the square impulse generator circuit.* See figure 6.16 for the corresponding circuit.

Mixer and Correction of the Feed-through

When we designed the first prototypes of the UWB transmitter, there was a high feed-through from the mixer between the local PLL synthesizer and the RF UWB output. This feed-through made a high peak (measured at about -30 dBm) in the spectrum at 4.25 GHz, which made the transmitter initially not compliant with the FCC regulations. To solve this, we use a trans-

mission line coupler in order to create destructive interference between the oscillator and the RF output (see Figure 6.16). Physically, the coupler is simply made with a wire soldered at one end of the resistive attenuator pad and it passes above the mixer and the RF output track while its other end stays in the air. By experimentally giving it by hand an appropriate shape (see Figure 9.11), it it possible to strongly decrease the effect of the feed-through and to remain FCC compliant. Each device requires thus a tailor-made adjustment of the coupler in order to remove the effect of the feed-through.

Complete schematic

The complete schematic of the UWB transmitter, including the oscillator is shown in Figure 6.18.

6.2.2   Construction of the IR-UWB Transmitter

The UWB Transmitter is made in Duroid RO4003C, which is better suited than FR4 for high frequency designs; its dielectric constant is $\varepsilon_r = 3.38$. The thickness h of the board is 0.508 mm (20 mils) and the thickness of the copper t is $35\mu m$ after etching and gold plating. The transmission lines have the *Shielded Microstrip* (or *Coplanar Waveground with Ground* as in [47]) configuration (see Figure 6.19) because it gives good protection against RF radiation and is also easy to include in the layout by simply drawing a ground plane around all RF tracks. For this configuration, the lines are sized by using the following formula (refer to [47] and Appendix A.1.2 for more details) :

$$Z_0 = \frac{\eta_0}{2\sqrt{\varepsilon_{eff}}\left(\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k_1')}\right)}$$

$$\text{with} \qquad k = \frac{a}{b} \qquad k' = \sqrt{1 - k^2} \qquad k_1' = \sqrt{1 - k_1^2}$$

$$\text{and} \qquad k_1 = \frac{\tanh\left(\frac{\pi a}{4h}\right)}{\tanh\left(\frac{\pi b}{4h}\right)} \qquad \varepsilon_{eff} = \frac{1 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}{1 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}$$

where K is the complete elliptic integral of the first kind. The calculation gives (after several iterations) a width for the signal track of $a = 1.25$ mm and, by considering a gap between tracks of $120\mu m$ that is the smallest resolution that can be achieved by our PCB workshop, a distance between grounds of $b = 1.25 + 2 \cdot 0.12 = 1.49$ mm in order to have a matching impedance of 50Ω. Although a good design of the transmission lines and ground planes reduces significantly
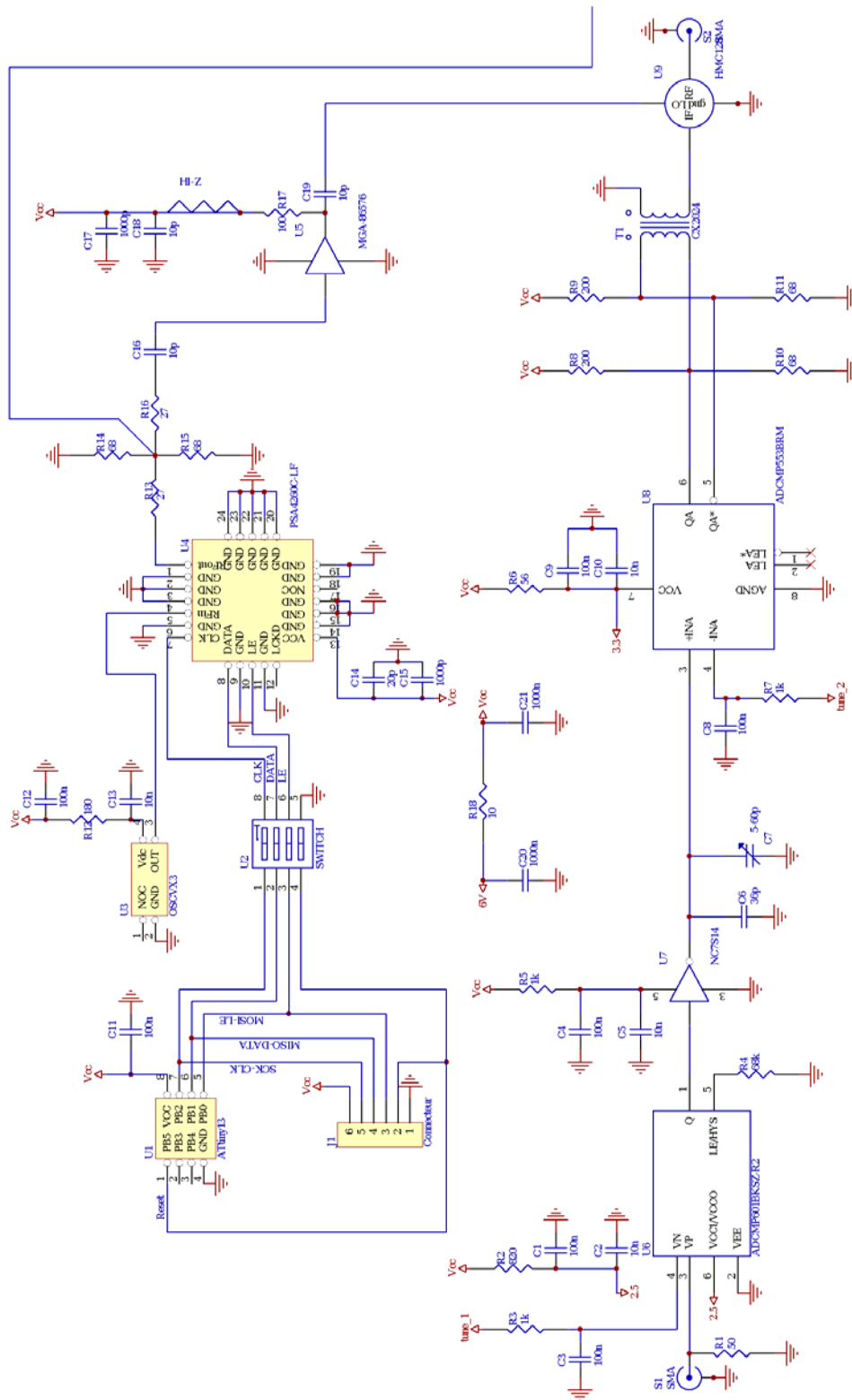
Figure 6.18: *The complete schematic of the UWB transmitter*
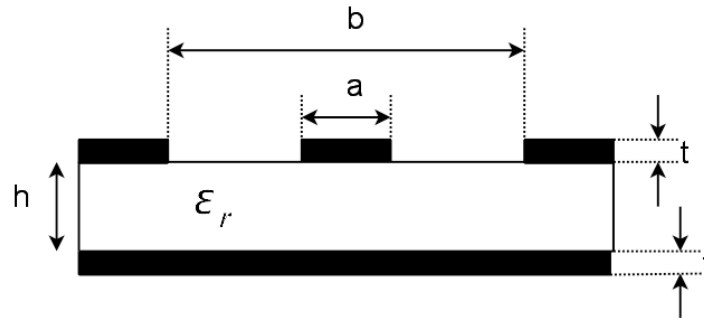
Figure 6.19: *The shielded microstrip configuration.*

the radiated power of the circuit, the PCB should be packaged in a metal case with a screwed cover in order to completely shield the environment against the radiation coming mainly from the PLL synthesizer. It is important to use many vias to connect both top and bottom ground planes in order to have the least amount of parasitic inductance, especially near high frequency signal tracks. The circuit is gold-plated by electro-chemical means in order to avoid corrosion of the copper that would rapidly degrade the performance. When components are soldered, the circuit is placed in the aluminium case and glued with a conductive glue (with silver) and placed in an oven for polymerisation for 3 hours at $70°$ C. The connection between the UWB transmitter and the outside world is made with SMA connectors for RF signals and through DC filters that are screwed into the shielding case for a DC power supply and tuning voltages. The microcontroller is then flashed with its software. The resulting PCB layout is shown in Figure 6.20 and the finished circuit is shown in Figure 9.11.
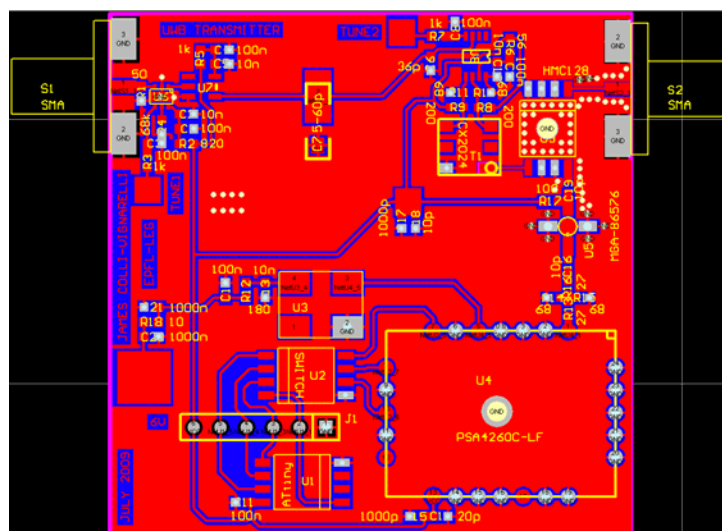
Figure 6.20: The PCB layout of the UWB transmitter
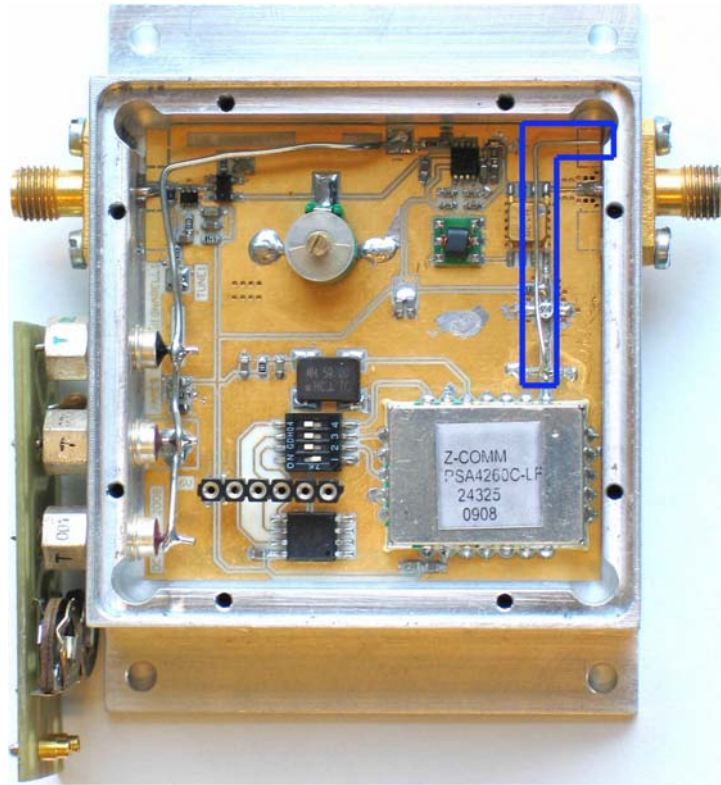
Figure 6.21: *Close view on the transmitter.* The transmitter is made using Duroid RO4003C material. The square shape makes the circuit fit the RF shielding case in aluminium. The blue line shows the transmission line coupler used to cancel the feed-through; its shape is obtained by experimentation.

6.2.3 Measurement on the IR-UWB Transmitter

The signal produced by the UWB transmitter is shown in frequency (see Figure 6.22 and 6.23) and time (see Figure 6.24) domains with a 1 MHz pseudo-random signal at the input. The signal has a power density of about -42.7 dBm/MHz at around 4.25 GHz and -51.3 dBm/MHz at 4.0 and 4.5 GHz, thus making the UWB transmitter compliant with the FCC rules (see Figure 6.23). In the time domain, we see that the signal lasts approximately 3.2 ns and has an amplitude of around 400mV_{pp}. We also see that the envelope of the signal is trapezoidal because of the balun. This trapezoidal shape increases the width of the UWB signal and decreases the intensity of the secondary lobes that would be higher with a pure rectangular envelope. The circuit is supplied with 5 volts and has a current consumption of 132 mA; thus it has a power consumption of 660 mW, most of it used by the PLL, local oscillator, MMIC amplifier and biasing resistors. This power consumption, although high, is acceptable in our case because the transmitter is intended
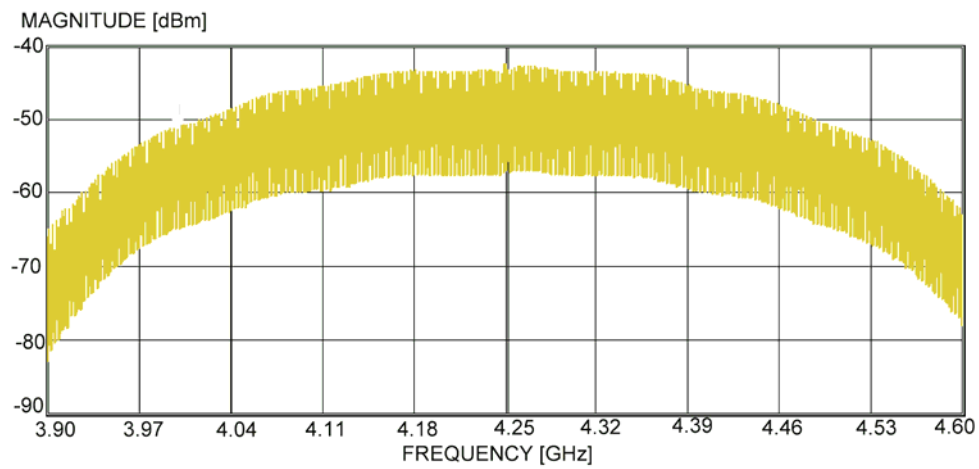
Figure 6.22: *The spectrum of the signal at the output of the UWB transmitter from* 3.9 *GHz to* 4.6 *GHz.*
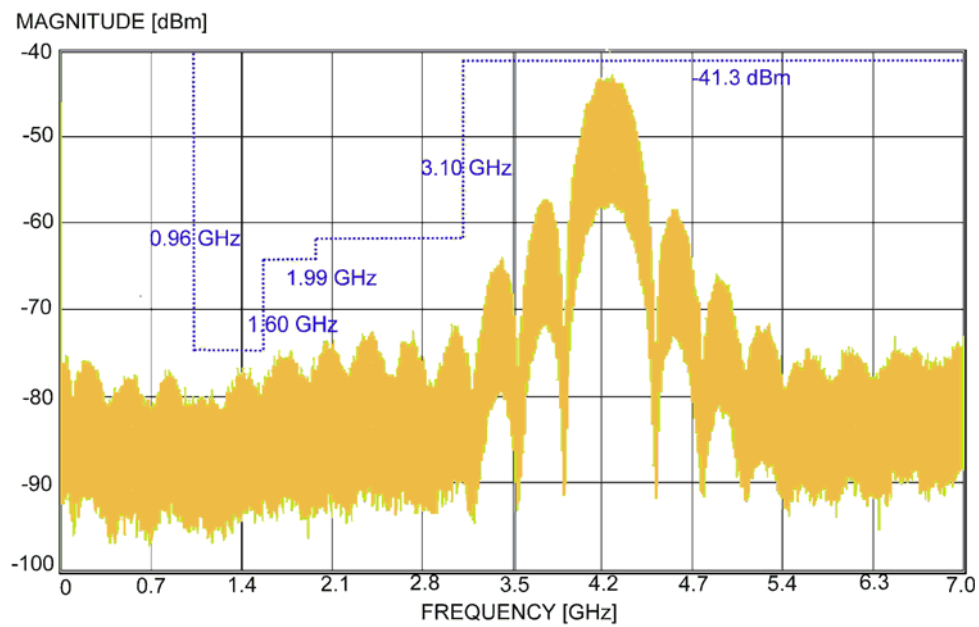
Figure 6.23: *The spectrum of the signal at the output of the UWB transmitter from DC to* 7 *GHz with the FCC regulations mask [9].*

to be used for measuring and testing purposes and not for real mobile low-power applications. We estimate that the consumption can be decreased to 570 mW - and thus save 90 mW - by using a switching power supply, instead of voltage drops across resistors, for delivering all the voltages required by the components of the transmitter.
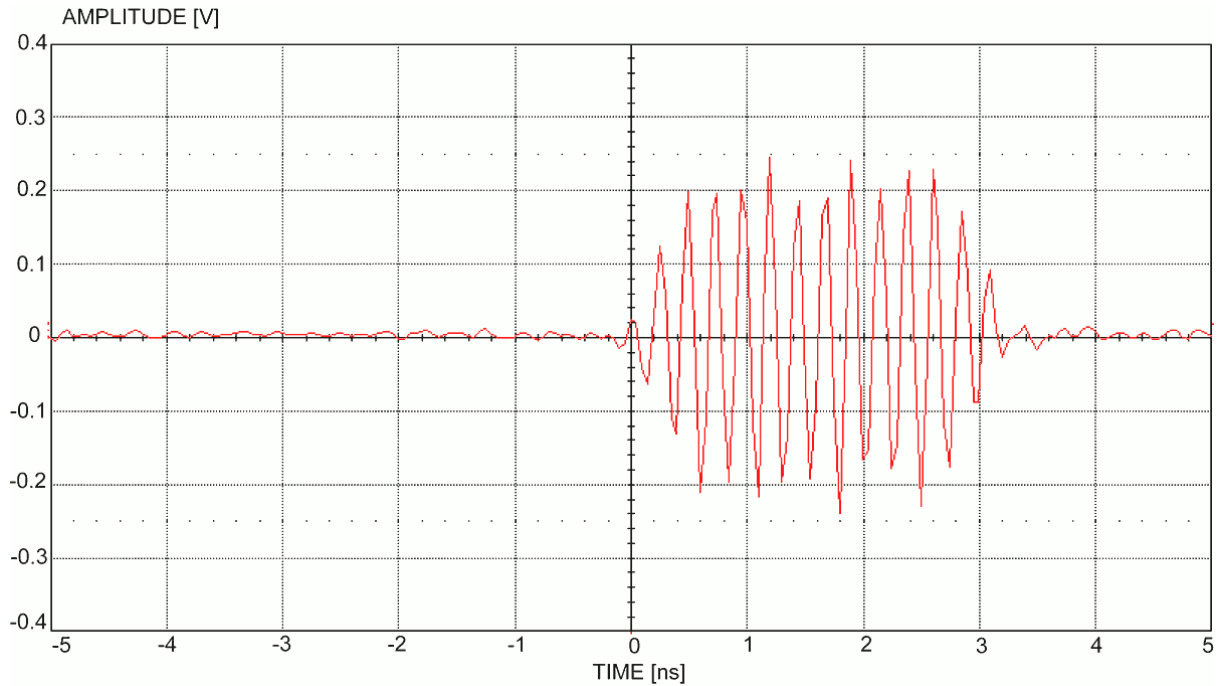
Figure 6.24: *The signal at the output of the UWB transmitter in the time domain.*

6.3   Conclusion

We have developed a generic UWB transmitter that is easy to use and to build for demonstrating and validating experimentally protocols and synchronization algorithms; its architecture is easy to modify for different central frequencies or bandwidths. The UWB transmitter described in this chapter is able to produce very high quality UWB signals by fulfilling very accurately the FCC standards specifications. It produces a well-shaped UWB signal with a square window; in fact the window is slightly trapezoidal because of the balun. The power consumption is high but acceptable for a non-mobile testbed for experimental validation purposes. In case the power consumption remains a problem, we estimate it is also possible to decrease it by at least 14 % by using switching power supply ICs in place of resistors. In our case, the results of the experimental demonstration and validation of the IR-UWB transmitter completely fulfils the expectations and regulations, thanks to its tuning facilities.

Chapter 7

LNA prototype n° 1

This chapter presents the research made for designing a complete Low-Noise Amplifier (LNA) for UWB signals (from 4.0 to 4.5 GHz) and, if possible, a voltage controlled gain. A narrow-band LNA can be designed by considering results from Section 7.1 but a wide-band LNA requires much more care by making it as much as possible insensitive to wide frequency variations around a central frequency. The challenges for this LNA are summarized as follows:

- The LNA has to be impedance-matched to 50Ω on the whole bandwidth.

- The gain has to be constant on the whole bandwidth.

- The LNA has to show a small noise figure on the whole bandwidth.

- The LNA has to have a voltage-controlled gain for AGC (Automatic Gain Control) purpose.

At the early beginning of the study of the LNA design (diploma project of the author), it was intended to design a circuit that meets all the specifications mentioned above and that could be cascaded as much as desired. However, according to experimentations and improved knowledge we gain on this type of circuit, we gave up this idea and focus instead on a cascade of specialised circuits, each circuit having its own specialised function. It is not possible, as shown experimentally in this chapter, to fulfil completely all these challenges with one circuit because they are in some case mutually exclusive. The best that can be done it to find an acceptable trade-off between these target specifications such that they approximately compensate each other their own influence on the transfer function of the LNA. The strategy considered for this purpose is to design the LNA as if it would be used in a narrow-band system (here : 4.25 GHz)

and to experimentally determine the surrounding component values that are the less sensitive to wide frequency variations. According to the results we obtain like this, we propose an acceptable LNA circuit with one transistor and how to improve it in a more advanced two-stage LNA system. This chapter presents the work made on one circuit that targets as much as possible to meet all the specifications mentioned previously and based around one transistor. Chapter 8 presents the LNA as done finally in the testbed and based on a two-stage system, each one being designed to meet one or two specification targets only but such that the whole system fulfils all of them.

7.1   Principles of LNAs with MOS transistor

The aim of this section is to give a deeper insight into how LNAs with MOS transistor are designed. The following developments are normally used when designing integrated circuits since all value of the components involved in the circuit can be finely adjusted with the shape and dimensions of the layout mask. In the case of a discrete circuit design, so many details are not necessary in themselves because the margin on the component values is large and there are considerable out-of-control parasitic elements that make a purely theoretic design almost useless. However, a good understanding of the underlying principles on MOS-transistor-based LNAs will help to achieve a good architecture that works and achieve the given constraints by highlighting the points to focus on. Then, some simulations will confirm whether the design works as expected or not.

In this section, we assume that the reader has basic knowledge of noise theory, circuit analysis and MOS transistor technology. This section is based mainly on the course book [48] and will follow the same approach; similar developments are made in reference [49] for the MOS and [50] for the SiGe transistor. In order to fully understand the underlying principles of LNAs, five circuits will be explained and analysed fully in detail. Some hypotheses were made in all this section in order to simplify the calculations and to focus only on the amplifier performance:

- First, the biasing circuit and its corresponding noise is neglected; the calculations focus mainly on the input signal path and transistor performance;

- Only the gate-source capacitance C_{GS} will be considered because of its importance in the impedance matching network and its effect on the noise figure; the Miller capacitance,

the drain-source and the source bulk capacitances are neglected;

- The output path is not considered here. This is because it was supposed that the noise has a lower effect on the signal quality when it was amplified. For this reason, the output of the amplifier will be grounded in the equivalent small signal schematics.

- The amplifiers are assumed to be narrow band (here).

All these circuits work in A-class. The first is a very simple circuit that has poor low-noise characteristic but is easy to analyse; this will make simple to understand the procedure of calculating noise in a circuit. The further circuits will show a progressive improvement of the noise figure; the last gives the best results and will, in fact, be used in this project to design the voltage controlled LNA.

7.1.1   LNA nᵒ 1 : Common source without matching network

The amplifier is a common source MOS transistor whose input has to be matched to the 50Ω of source input voltage. This means that the real part of the input impedance has to be 50Ω while its imaginary part has to be near 0Ω; in other words, the matching network has to be able to cancel the parasitic capacitance C_{GS} of the MOS transistor while showing purely resistive 50Ω at its input to the source generator. For this purpose, a shunt inductor L_S and a shunt resistor R_P are added between the gate of the transistor and the ground. If the shunt resonant circuit L_S-C_{GS} is tuned to the working frequency ω_0 , the imaginary part of the impedance vanishes and only resistive components remain in the circuit, as shown in Figure 7.1.
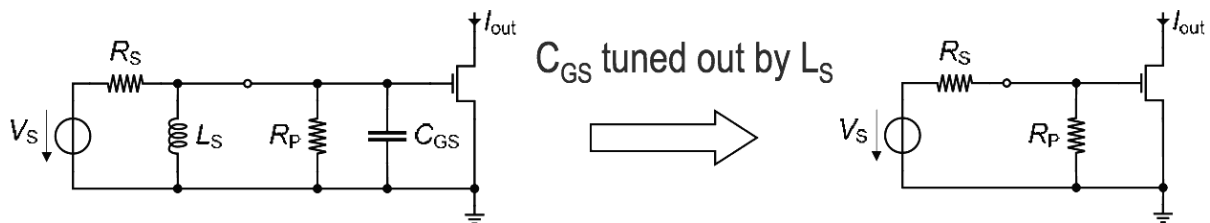
Figure 7.1: Schematic of the common source LNA (see [48]).

The small-signal equivalent circuit at ω_0 is shown in Figure 7.2. All further calculations assume that the circuit works at this frequency. This figure helps to understand how the equivalent transconductance G_{meq} is obtained, which will be very useful when calculating the total noise obtained in the whole circuit.
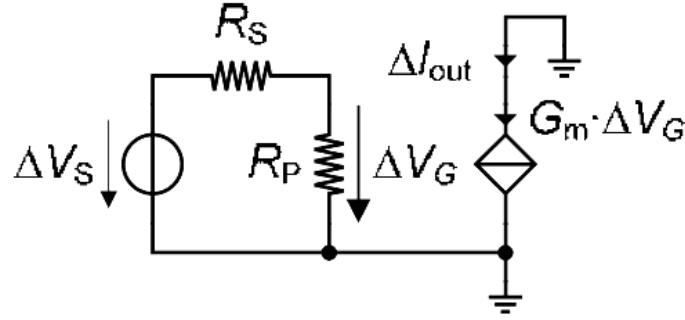
Figure 7.2: Small-signal schematic of common source LNA without matching (see [48]).

Equivalent transconductance calculation

The equivalent transconductance is defined by the ratio between the output current and the input voltage; thus taking into account the presence of the other components around the MOS transistor.

$$G_{meq} = \frac{\Delta I_{out}}{\Delta V_s}$$

Any variation of the output current is linked to the input voltage by :

$$\Delta I_{out} = G_m \cdot \Delta V_G = G_m \cdot \frac{R_P}{R_P + R_S} \cdot \Delta V_S$$

Thus, replacing this expression in the definition of equivalent transconductance gives :

$$G_{meq} = \frac{\Delta I_{out}}{\Delta V_s} = G_m \cdot \frac{R_P}{R_P + R_S}$$

Noise calculation

The noise small-signal equivalent schematic is obtained by adding a shunt current source across each resistor; the same applies for modelling the transistor noise, as shown in Figure 7.3.

It is then easy to determine the noise voltage seen between the gate and the ground :

$$\Delta V_G = (I_{nRs} + I_{nRp}) \cdot \frac{R_S \cdot R_P}{R_S + R_P}$$

The corresponding output noise current is thus given by :

$$\Delta I_{nout} = I_{nD} + G_m \cdot \Delta V_G = I_{nD} + G_m \cdot (I_{nRs} + I_{nRp}) \cdot \frac{R_S \cdot R_P}{R_S + R_P}$$
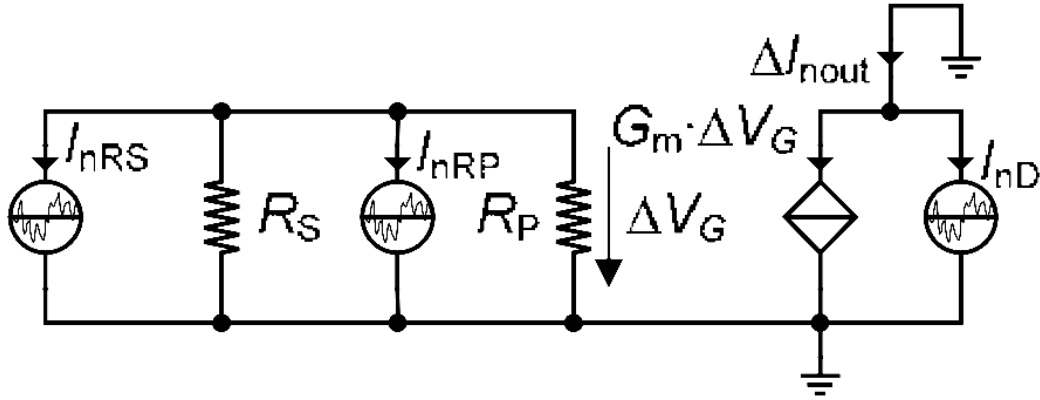
Figure 7.3: Noise small-signal schematic of common source LNA (see [48]).

The equivalent noise voltage source is then obtained by replacing the corresponding values in the following equation :

$$V_{neq} = \frac{\Delta I_{nout}}{G_{meq}} = I_{nD} \cdot \left(\frac{R_P + R_S}{R_P}\right) \cdot \frac{1}{G_m} + (I_{nRs} + I_{nRp}) \cdot R_S$$

$$= I_{nD} \cdot \left(1 + \frac{R_S}{R_P}\right) \cdot \frac{1}{G_m} + (I_{nRs} + I_{nRp}) \cdot R_S$$

Since noise is expressed in terms of power spectral density, the equivalent noise resistance is obtained first by replacing the noise current sources by their corresponding resistance and transconductance, and then by squaring their corresponding scaling factor as shown below :

$$R_{neq} = G_{nD} \cdot \left(1 + \frac{R_S}{R_P}\right)^2 \cdot \left(\frac{1}{G_m}\right)^2 + \left(\frac{1}{R_S} + \frac{1}{R_P}\right) \cdot R_S^2$$

As in MOST, the drain noise is linked to the mutual transconductance $G_{nD} = \gamma_{nD} \cdot G_m$, where γ_{nD} is the thermal noise excess factor which shows how much noise is generated at the drain for a given G_m, then, inserting this equation in the previous one obtained for the equivalent noise resistance gives :

$$R_{neq} = \frac{\gamma_{nD}}{G_m} \cdot \left(1 + \frac{R_S}{R_P}\right)^2 + R_S + \frac{R_S^2}{R_P}$$

The noise factor is simply obtained by normalising the equivalent noise resistance by the input resistance as shown below. This expresses the total noise obtained in the whole circuit as

if the noise was only produced by resistor R_S.

$$F = \frac{R_{neq}}{R_S} = \frac{\gamma_{nD}}{G_m \cdot R_S} \cdot \left(1 + \frac{R_S}{R_P}\right)^2 + 1 + \frac{R_S}{R_P}$$

Although there is no matching network, but assuming all the same that the input impedance is matched with the source impedance – i.e. $R_S = R_P$, the noise factor becomes :

$$F = 2 + \frac{4 \cdot \gamma_{nD}}{G_m \cdot R_S}$$

This equation shows that, ideally, the noise figure can never be smaller than 2 (or 3 dB); however a careful design is required for approaching this asymptotic value.

7.1.2   LNA nº 2 : Common source with matching network

The previous LNA can be considerably improved by adding an impedance matching network that is independent from the resistance R_P. This one can thus be made larger in order to reduce its noise contribution. The impedance matching network is a high-pass because the series capacitor works as a block the DC bias while the inductor works as an RF choke for the bias voltage. It is important to note that in order to decrease the noise of a resistor, its value has to be small when it is in a series circuit and large when it is in a shunt circuit.

Such an impedance matching network has to reduce the impedance seen from the source so that it matches the source resistance as shown in Figure 7.4.
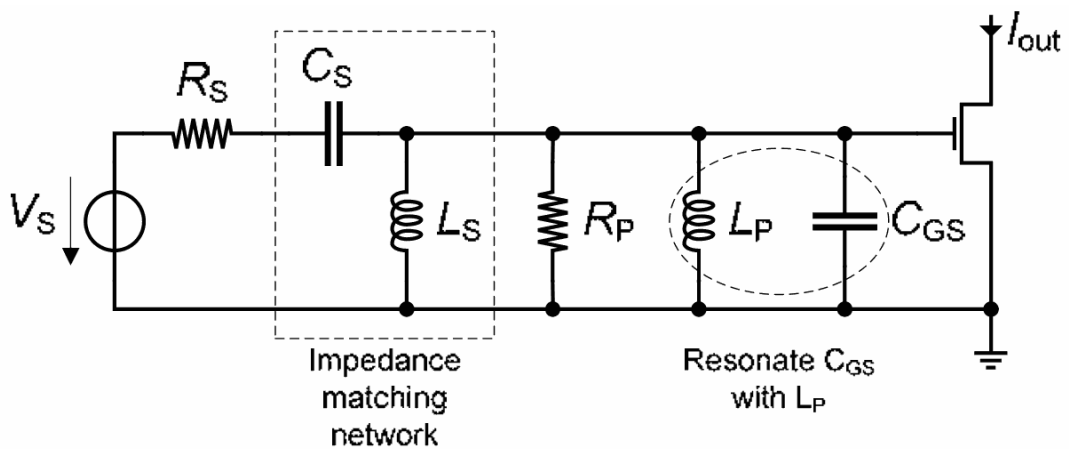
Figure 7.4: Schematic of the common source LNA with matching network (see [48]).

The following formulæ will be very useful for further calculations. There are detailed in reference [48].

$$Q = \frac{X_S}{R_S} = \frac{R_P}{X_P} = \sqrt{\frac{R_P}{R_S} - 1}$$

$$X_P = \omega_0 \cdot L_S = \frac{R_P}{Q}$$

$$X_S = \frac{1}{\omega_0 \cdot C_S} = Q \cdot R_S$$

$$R_P = (1 + Q^2) \cdot R_S$$

As previously, the resonant circuit L_P and C_{GS} vanishes at resonance frequency ω_0 and the equivalent small-signal circuit is as shown in Figure 7.5.
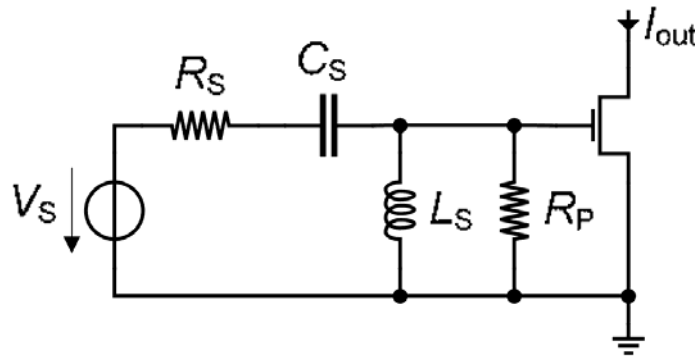
Figure 7.5: Schematic of the common source LNA at resonant frequency (see [48]).

Equivalent transconductance calculation

The series and shunt branches of the circuit shown in Figure 7.5 form a voltage divider that affects the total transconductance of the whole circuit. At resonance, their respective impedance are given by the following equations :

$$Z_1 = R_s + Z_{C_S} = R_S + \frac{1}{j\omega_0 \cdot C_S} = R_S + \frac{1}{j\frac{1}{Q \cdot R_S}} = R_S(1 - jQ)$$

$$Z_2 = R_P \parallel Z_{L_S} = \frac{j\omega_0 \cdot L_S \cdot R_P}{j\omega_0 \cdot L_S + R_P} = \frac{jR_P \frac{R_P}{Q}}{j\frac{R_P}{Q} + R_P} = j\frac{R_P}{Q + j}$$

The gain of the voltage divider is then obtained by replacing the impedance values in the definition:

$$
\begin{aligned}
A_v = \frac{V_G}{V_S} &= \frac{Z_2}{Z_1 + Z_2} = \frac{j\frac{R_P}{Q+j}}{R_S(1-jQ) + j\frac{R_P}{Q+j}} = \frac{jR_P}{R_S(1-jQ)\cdot(Q+j) + jR_P} \\
&= \frac{j(1+Q^2)R_S}{R_S(1-jQ)\cdot(Q+j) + j(1+Q^2)R_S} = \frac{j(1+jQ)}{Q+j+j(1+jQ)} \\
&= \frac{j(1+jQ)}{Q+j+j-Q} = \frac{j(1+jQ)}{2j} \\
&= \frac{1+jQ}{2}
\end{aligned}
$$

The equivalent transconductance is thus simply expressed as :

$$
G_{meq} = A_v \cdot G_m = (1+jQ)\cdot\frac{G_m}{2}
$$

Noise calculation

As previously, the noise small-signal equivalent schematic is obtained by adding a shunt current source across each resistor and also across the drain and source of the transistor as in Figure 7.3. The noise contribution of the resistor at the gate is given by :

$$
\Delta V_G = V_{nRs} \cdot A_v + V_{nRp} \cdot \frac{Z_2'}{Z_1' + Z_2'}
$$

where the Z_1' and Z_2' form a current divider. Their values are given by the following equations:

$$
Z_1' = R_P
$$

$$
\begin{aligned}
Z_2' &= Z_1 \parallel Z_{L_S} = \frac{R_S(1-jQ)\cdot j\frac{R_P}{Q}}{R_S(1-jQ) + j\frac{R_P}{Q}} = \frac{jR_P R_S(1-jQ)}{jR_P + R_S Q(1-jQ)} = \frac{jR_P\cdot(1-jQ)}{j\frac{R_P}{R_S} + Q(1-jQ)} \\
&= \frac{jR_P\cdot(1-jQ)}{j(1+Q^2) + Q(1-jQ)} = \frac{jR_P}{j(1+jQ)+Q} = \frac{jR_P}{j-Q+Q} \\
&= R_P
\end{aligned}
$$

By inserting this in the gate voltage expression, there is:

$$
\begin{aligned}
\Delta V_G &= V_{nRs} \cdot A_v + V_{nRp} \cdot \frac{Z_1'}{Z_1' + Z_2'} \\
&= V_{nRs} \cdot \frac{1 + jQ}{2} + V_{nRp} \cdot \frac{R_P}{R_P + R_P} \\
&= V_{nRs} \cdot \frac{1 + jQ}{2} + V_{nRp} \cdot \frac{1}{2}
\end{aligned}
$$

The corresponding output noise current is given by:

$$
I_{nout} = I_{nD} + G_m \cdot \left(V_{nRs} \cdot \frac{1 + jQ}{2} + V_{nRp} \cdot \frac{1}{2} \right)
$$

The equivalent noise voltage source is then obtained by replacing the corresponding values in the following equation:

$$
V_{neq} = \frac{I_{nout}}{G_{meq}} = I_{nD} \cdot \frac{2}{G_m(1 + jQ)} + V_{nRs} + V_{nRp} \frac{1}{1 + jQ}
$$

The equivalent noise resistor is obtained by replacing the noise sources by their value and by squaring their scale factor; the noise source that models the noise in the transistor is replaced as previously. It is important to note that the j symbol vanishes without leaving a minus sign when squared. The fundamental reason why this happens is the fact that it is assumed that all noise sources are uncorrelated, so since only the noise power is relevant here, it is the magnitude (absolute value) of the noise terms that is added.

$$
R_{neq} = G_{nD} \cdot \frac{4}{G_m^2(1 + Q^2)} + R_S + R_P \cdot \frac{1}{1 + Q^2} = \frac{4\gamma_{nD}}{G_m(1 + Q^2)} + 2R_S
$$

The noise factor is thus expressed as :

$$
F = \frac{R_{neq}}{R_S} = 2 + \frac{4\gamma_{nD}}{G_m R_S(1 + Q^2)}
$$

This equation shows that, as for the LNA nº 1, the noise figure can never be smaller than 2 (or 3 dB); however it is easier here to reach this ideal value because the quality factor can decrease greatly the second term of the noise figure.

7.1.3   LNA nº 3 : Common gate without matching network

Since the gate has a purely reactive impedance, it is interesting to see what happens if the transistor is used in a common gate configuration, where the signal enters by the source, which has a resistive impedance as it will be shown further. Therefore, the number of external components is very small, so it should improve the noise factor of the amplifier. This gives the schematic shown in Figure 7.6.
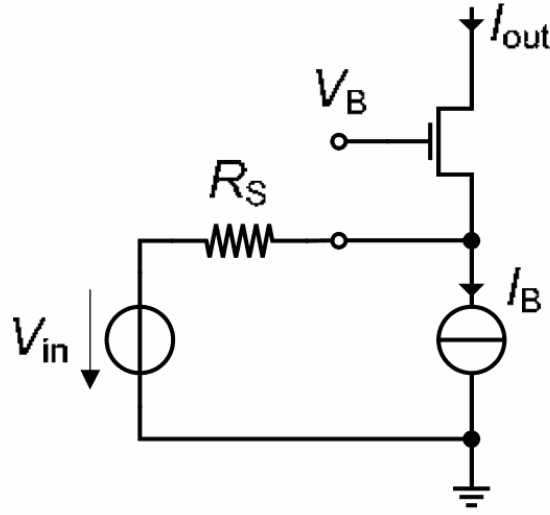
Figure 7.6: Schematic of common gate LNA without matching network (see [48]).

Input impedance calculation

The input impedance is very simple to calculate with the help of the equivalent small-signal schematic shown in Figure 7.7, where the drain is shortened to the ground and the current source I_B is opened. Its value is given by :

$$Z_{in} = \frac{\Delta V_S}{\Delta I_{in}} = \frac{\Delta V_S}{G_{ms} \cdot \Delta V_S} = \frac{1}{G_{ms}}$$
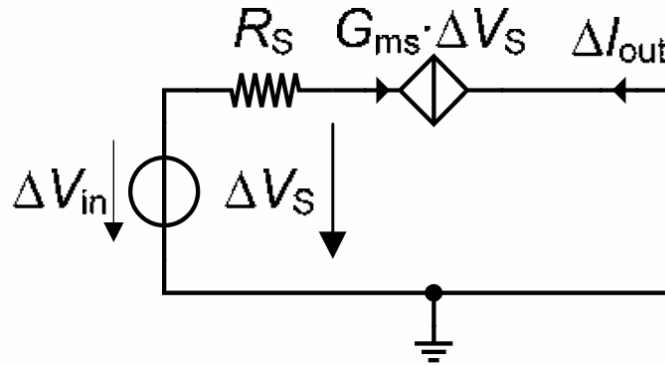
Figure 7.7: Small-signal schematic of common gate LNA (see [48]).

Equivalent transconductance calculation

From the small-signal schematic shown in Figure 7.7, the output current variation and the input voltage variation are given by the following expressions:

$$\Delta V_S = \Delta V_{in} - R_S \cdot G_{ms} \cdot \Delta V_S \Leftrightarrow \Delta V_S(1 + G_{ms} \cdot R_S) = \Delta V_{in}$$

$$\Delta I_{nout} = -G_{ms} \cdot \Delta V_S = -G_{ms} \cdot \frac{\Delta V_{in}}{1 + G_{ms} \cdot R_S}$$

It is thus very easy to calculate the equivalent transconductance :

$$G_{meq} = \frac{\Delta I_{nout}}{\Delta V_{in}} = -\frac{G_{ms}}{1 + G_{ms} R_S}$$

The impedance is matched when :

$$R_S = Z_{in} = \frac{1}{G_{ms}}$$

So, the equivalent transconductance becomes :

$$G_{meq} = -\frac{G_{ms}}{2}$$

Noise calculation

The noise small-signal equivalent schematic is obtained as usual, as shown in Figure 7.8.
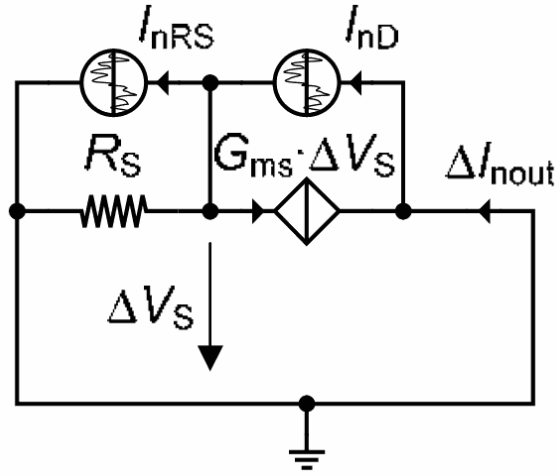
Figure 7.8: Noise small-signal schematic of common gate LNA (see [48]).

The noise voltage seen at the source (input) is given by :

$$\Delta V_S \quad = \quad R_S \cdot (I_{nD} - I_{nRs} - G_{ms} \cdot \Delta V_s)$$

$$\Rightarrow \quad \Delta V_s(1 + R_S \cdot G_{ms}) = R_S(I_{nD} - I_{nRS})$$

$$\Rightarrow \quad \Delta V_S = \frac{R_S(I_{nD} - I_{nRS})}{1 + R_S \cdot G_{ms}}$$

and the noise current seen at the drain (output) is given by :

$$\Delta I_{nout} = I_{nD} - G_{ms} \cdot \Delta V_s = I_{nD} - G_{ms} \cdot \frac{R_S(I_{nD} - I_{nRS})}{1 + R_S \cdot G_{ms}}$$

Since the impedance is matched, this value simplifies to :

$$\Delta I_{nout} = I_{nD} - \frac{1}{2}(I_{nD} - I_{nRS}) = \frac{I_{nD}}{2} + \frac{I_{nRS}}{2}$$

The equivalent noise voltage source is then obtained by replacing the corresponding values in the following equation :

$$V_{neq} = \frac{\Delta I_{nout}}{G_{meq}} = I_{nD} \cdot \frac{-1}{G_{ms}} + I_{nRS} \cdot \frac{-1}{G_{ms}}$$

The equivalent noise resistor is obtained by replacing the noise sources by their value and

squaring their scale factor; the noise source that models the noise in the transistor is replaced as previously. The impedance is always assumed to be matched.

$$R_{neq} = G_{nD} \cdot \frac{1}{G_{ms}^2} + \underbrace{\left(\frac{1}{R_S}\right)}_{G_{ms}} \cdot \frac{1}{G_{ms}^2} = \frac{G_{nD}}{G_{ms}^2} + \frac{1}{\underbrace{G_{ms}}_{R_S}} = \frac{G_{nD}}{G_{ms}^2} + R_S$$

Finally, the noise factor is given by :

$$F = \frac{R_{neq}}{R_S} = \frac{G_{nD}}{G_{ms}^2 \cdot R_S} + 1 = 1 + \frac{G_{nD}}{G_{ms}} = 1 + \delta_{nD}$$

where δ_{nD} is drain thermal noise excess factor which shows how much noise is generated at the drain for a given G_{ms}; its value is 0.5 when in weak inversion and saturation, which gives its smallest value. The best noise figure that can be achieved with the LNA nº 3 is thus 1.5 or 1.76 dB, which corresponds to a great improvement from the previous architecture.

7.1.4   LNA nº 4 : Common gate with matching network

Like the LNA nº 2 towards the LNA nº 1, the previous LNA can be improved in the same way by adding an impedance matching network between the source generator and the transistor, as shown in Figure 7.9. As for LNA nº 2, the impedance matching network is a high-pass because the series capacitor works as a block the DC bias while the inductor works as an RF choke for the bias voltage.
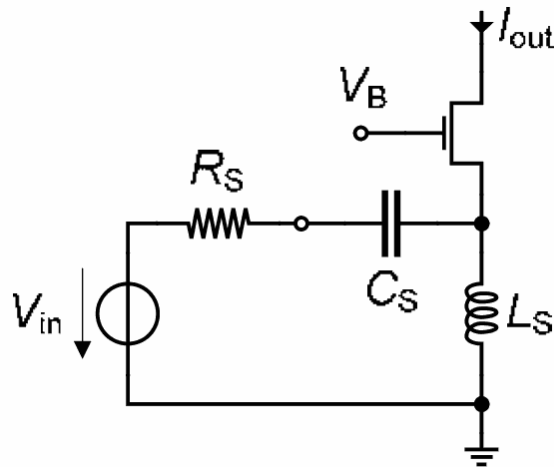
Figure 7.9: Schematic of common gate LNA with matching network (see [48]).

The equivalent small-signal schematic of the corresponding impedance matching network

is shown in Figure 7.10. This schematic is obtained mainly by shortening the drain to the ground, thus letting the current source G_{ms} in shunt with the inductor. The similarity with the case of the LNA n$^{\text{o}}$ 2 is quite obvious, so the results obtained before can be re-used here without any additional condition. However, it is important to keep in mind that this schematic is only valid at the resonant frequency.
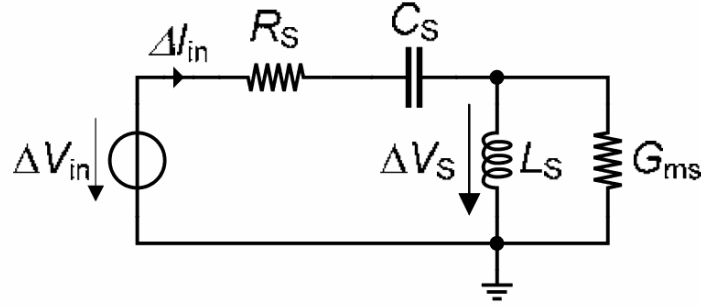
Figure 7.10: Small-signal schematic of common gate LNA (see [48]).

The same formulæ as for the LNA n$^{\text{o}}$ 2 will be useful for further calculations; they are valid only at ω_0 .

$$Q \;=\; \frac{X_S}{R_S} = \frac{R_P}{X_P} = \sqrt{\frac{R_P}{R_S} - 1}$$

$$X_P \;=\; \omega_0 \cdot L_S = \frac{R_P}{Q}$$

$$X_S \;=\; \frac{1}{\omega_0 \cdot C_S} = Q \cdot R_S$$

$$R_P \;=\; (1 + Q^2) \cdot R_S$$

Input impedance calculation

By comparing Figures 7.5 and 7.10, it is obvious that R_P and G_{ms} play exactly the same role in both circuits, thus it gives:

$$Z_{\text{in\_LNA n°4}} \underbrace{=}_{\text{matching network}} \frac{1}{1+Q^2} \cdot Z_{\text{in\_LNA n°3}} \underbrace{=}_{Z_{\text{in\_LNA n°3}} = \frac{1}{G_{ms}}} \frac{1}{(1+Q^2)} \cdot \frac{1}{G_{ms}} \underbrace{=}_{G_{ms} = \frac{1}{R_P}} \frac{R_P}{1+Q^2} = R_s$$

This equation is a complicated one and needs explanations; it has however the advantage

to re-use the previous calculations. For the first equality, the LNA n° 4 is the same as the LNA n° 3 in exception that there is a matching network that decreases the impedance seen from the source by a factor $\frac{1}{(1+Q^2)}$. The second equality is obtained by calculating the value of Z_{in} for the LNA n° 3 as in the corresponding section. The third equality is obtained by comparing the role played by G_{ms} in the LNA n° 4 and R_P in the LNA n° 2 that is exactly the same because of the impedance matching - it is only a symbolic transformation. Then, the last equality is obtained just by applying the rule from the reference [51] which gives the final result.

Equivalent transconductance calculation

As shown in Figures 7.5 and 7.10 and assuming that the impedances are matched, i.e. $R_P = \frac{1}{G_{ms}}$, the small-signal schematic of the impedance matching network of LNA n° 4 has exactly the same topology as that of LNA n° 2, thus the equivalent transconductance is the same, with the exception that G_m is now replaced by G_{ms}:

$$G_{meq} = (1 + jQ) \cdot \frac{G_{ms}}{2}$$

Noise calculation

The noise small-signal equivalent schematic is obtained as usual, as shown in Figure 7.11.
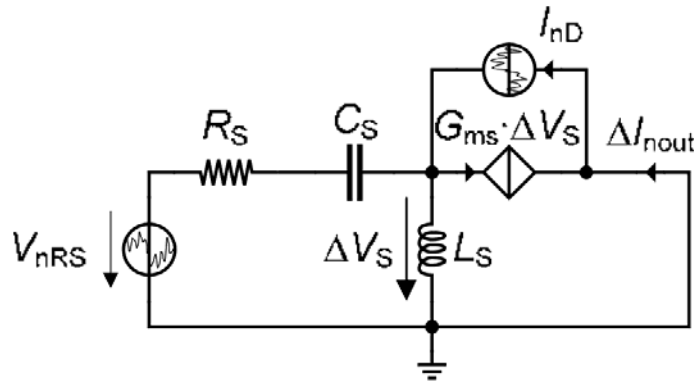
Figure 7.11: Noise small-signal schematic of common gate LNA (see [48]).

The voltage seen from the source of the transistor is given by :

$$\Delta V_S = V_{nRS} \cdot A_v + I_{nD} \cdot Z_{tot}$$

where A_v is the gain of the voltage divider formed by the series branch R_S - C_S and the

shunt branch $L_S \, G_{ms}$, and Z_{tot} is the total impedance seen from the noise current source I_{nD}. These expressions are detailed below:

$$A_v \quad = \quad \frac{G_{meq}}{G_{ms}} = \frac{1+jQ}{2}$$

$$Z_{tot} \quad = \quad R_P \parallel (L_s \parallel (R_S + C_S)) \underbrace{=}_{\text{cf. LNA n°2}} R_P \parallel Z_2' = R_P \parallel R_P = \frac{R_P}{2} = \frac{1}{2G_{ms}}$$

The voltage seen from the source of the transistor thus becomes :

$$\Delta V_S = V_{nRS} \cdot \frac{1+jQ}{2} + I_{nD} \cdot \frac{1}{2G_{ms}}$$

The corresponding output noise current is then given by :

$$\Delta I_{nout} \quad = \quad I_{nD} - G_{ms} \cdot \Delta V_S$$

$$= \quad I_{nD} - G_{ms} \cdot \left(V_{nRS} \cdot \frac{1+jQ}{2} + I_{nD} \cdot \frac{1}{2G_{ms}} \right)$$

$$= \quad I_{nD} - \frac{I_{nD}}{2} - G_{ms} \cdot V_{nRS} \cdot \frac{1+jQ}{2}$$

$$= \quad \frac{I_{nD}}{2} - V_{nRS} \cdot G_{ms} \cdot \frac{1+jQ}{2}$$

The equivalent noise voltage source is then obtained by replacing the corresponding values in the following equation :

$$V_{neq} = \frac{\Delta I_{nout}}{G_{meq}} = I_{nD} \cdot \frac{1}{(1+jQ)G_{ms}} - V_{nRS}$$

The equivalent noise resistor is obtained by replacing the noise sources by their value and squaring their scale factor; the noise source that models the noise in the transistor is replaced as previously. The impedance is always assumed to be matched. The minus sign that is expected when squaring j does not appear for the same reason as explained previously.

$$R_{neq} = \delta_{nD} \cdot G_{ms} \cdot \left(\frac{1}{(1+jQ) \cdot G_{ms}} \right)^2 + R_S = R_S + \frac{\delta_{nD}}{(1+Q^2)G_{ms}}$$

Finally, the noise factor is then given by :

$$F = \frac{R_{neq}}{R_S} = 1 + \frac{\delta_{nD}}{\underbrace{(1+Q^2)R_S}_{R_P} G_{ms}} = 1 + \frac{\delta_{nD}}{\underbrace{R_P}_{\frac{1}{G_{ms}}} \cdot G_{ms}} = 1 + \delta_{nD}$$

where δ_{nD} is, as explained previously, the drain thermal noise excess factor which shows how much noise is generated at the drain for a given G_{ms}; its value is 0.5 when in weak inversion and saturation, which gives its smallest value. The best noise figure that can be achieved with this LNA is thus 1.5 or 1.76 dB, as for the previous LNA but with an improvement concerning the matching network.

7.1.5   LNA nº 5 : Common source inductively degenerated

The last architecture is the best of all. It combines the advantages of the others by allowing the impedance matching and the gate capacitance cancelling by the mean of two independent parameters, as shown further. In addition, all the components are purely reactive so in theory they add no noise, so only the transistor contributes to the noise figure. The schematic of this LNA in given in Figure 7.12. The L_s inductor is for the source degeneration and L_G is for cancelling the gate capacitance (in conjunction with L_s).
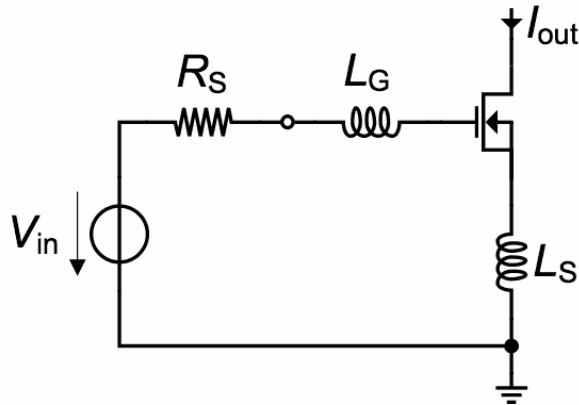
Figure 7.12: Schematic of Common source LNA with inductance degeneration (see [48]).

Input impedance calculation

This section will show that the input impedance is purely resistive at the resonant frequency. For this purpose, the small-signal schematic in Figure 7.13 will help to set the correct equations.
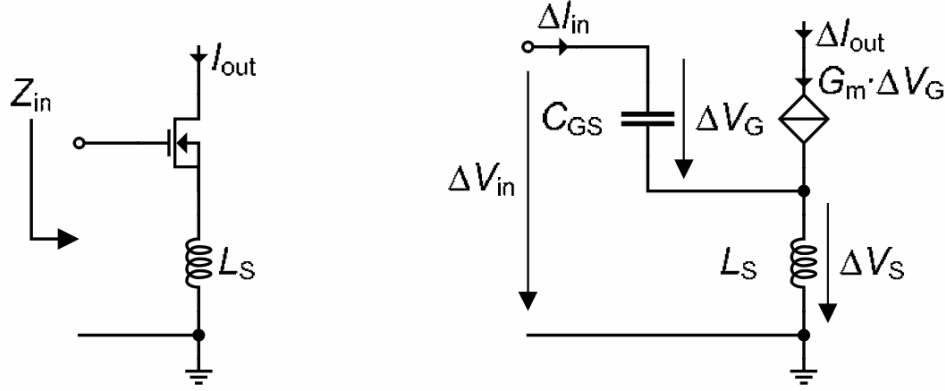
Figure 7.13: Small-signal equivalent schematic for input impedance (see [48]).

The input impedance is given by :

$$Z_{in} = \frac{\Delta V_{in}}{\Delta I_{in}} = \frac{\Delta V_G + \Delta V_S}{\Delta I_{in}} = \frac{\Delta V_G}{\Delta I_{in}} + \frac{\Delta V_S}{\Delta I_{in}} = \frac{1}{sC_{GS}} + \frac{\Delta V_S}{\Delta I_{in}}$$

Since $\Delta V_S = sL_S(\Delta I_{in} + \Delta I_{out})$ and $\Delta I_{out} = G_m \cdot \Delta V_G$ then :

$$
\begin{aligned}
Z_{in}(s) &= \frac{1}{sC_{GS}} + \frac{sL_s(\Delta I_{in} + \Delta I_{out})}{\Delta I_{in}} \\[2mm]
&= \frac{1}{sC_{GS}} + sL_s\left(1 + G_m \cdot \frac{\Delta V_G}{\Delta I_{in}}\right) \\[2mm]
&= \frac{1}{sC_{GS}} + sL_s + G_m \cdot sL_S \cdot \underbrace{\frac{\Delta V_G}{\Delta I_{in}}}_{\frac{1}{sC_{GS}}} \\[2mm]
&= \frac{1}{sC_{GS}} + sL_s + \frac{G_m \cdot L_S}{C_{GS}}
\end{aligned}
$$

The same equation expressed with $j\omega$ gives, at resonance :

$$Z_{in}(j\omega) = \frac{G_m \cdot L_S}{C_{GS}} + j\frac{\omega^2 \cdot L_S \cdot C_{GS} - 1}{\omega \cdot C_{GS}} \underbrace{=}_{\omega=\omega_0=\frac{1}{\sqrt{L_S \cdot C_{GS}}}} \frac{G_m \cdot L_S}{C_{GS}}$$

Since L_S is used at the same time for tuning C_{GS} and for matching the source resistance R_S, an additional degree of freedom is required. For this purpose, another inductor, L_G is added in series with R_S in order to eliminate the remaining imaginary part.

Equivalent transconductance calculation

This section explains how to calculate the equivalent transconductance of the whole circuit using the small-signal schematic in Figure 7.14.
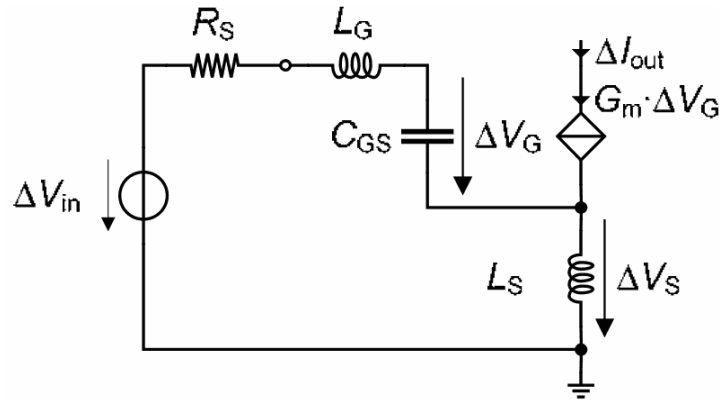
Figure 7.14: Small-signal of common source LNA with inductance degeneration (see [48]).

The following simple formulæ will be useful in further algebraic transformations, where ΔI_{in} is the current flowing across the series branch made by R_S, L_G and C_{GS} :

$$\Delta I_{out} = G_m \cdot \Delta V_G$$

$$\Delta V_G = \Delta I_{in} \cdot \frac{1}{sC_{GS}} \Leftrightarrow \Delta I_{in} = sC_{GS} \cdot \Delta V_G$$

Here the voltage across L_S is calculated with two independent equations. The first one is obtained by considering the total current flowing through L_S while the second is obtained by considering the voltage loop passing through the source generator and L_S.

$$(1) \quad \Delta V_S = sL_S(\Delta I_{in} + \Delta I_{out})$$

$$= sL_S(sC_{GS} + G_m) \cdot \Delta V_G$$

$$(2) \quad \Delta V_S = \Delta V_{in} - \Delta V_G - (R_S + sL_G) \cdot \Delta I_{in}$$

$$= \Delta V_{in} - \Delta V_G - (R_S + sL_G) \cdot sC_{GS} \cdot \Delta V_G$$

Since they are independent, these equations can be matched together :

$$\Delta V_S = \Delta V_{in} - \Delta V_G - (R_S + sL_G) \cdot sC_{GS} \cdot \Delta V_G = sL_S(sC_{GS} + G_m) \cdot \Delta V_G$$

Hence, it is easy here to separate ΔV_{in} and ΔV_G in order to express one toward the other :

$$
\begin{aligned}
\Delta V_{in} &= \Delta V_G + (R_S + sL_G) \cdot sC_{GS} \cdot \Delta V_G + (sC_{GS} + G_m) \cdot sL_S \cdot \Delta V_G \\
&= \Delta V_G \cdot (1 + sR_SC_{GS} + s^2L_GC_{GS} + s^2L_SC_{GS} + sG_mL_S)
\end{aligned}
$$

The voltage gain at the gate is thus obtained by replacing by previous results in its definition as shown below. The quality factor and the resonance frequency are simply obtained by identifying the corresponding terms with those of the standard form of the transfer function of any LC resonant circuit as shown below.

$$
\begin{aligned}
A_\nu(s) = \frac{\Delta V_G}{\Delta V_{in}}(s) &= \frac{1}{1 + (R_SC_{GS} + G_mL_S) \cdot s + ((L_G + L_S)C_{GS}) \cdot s^2} \\[2mm]
&= \frac{1}{1 + \frac{s}{\omega_0 Q} + \left(\frac{s}{\omega_0}\right)^2} \\[2mm]
\Rightarrow \omega_0 &= \frac{1}{\sqrt{(L_G + L_S) \cdot C_{GS}}} \\[2mm]
\Rightarrow Q &= \frac{1}{(G_mL_S + R_SC_{GS}) \cdot \omega_0}
\end{aligned}
$$

Since the gain of a series resonant circuit is maximum at ω_0, it gives :

$$A_{\nu\_\max} = A_\nu(s = j\omega_0) = \frac{1}{1 + \frac{j\omega_0}{\omega_0 Q} + \left(\frac{j\omega_0}{\omega_0}\right)^2} = \frac{1}{1 + \frac{j}{Q} - 1} = \frac{Q}{j}$$

The equivalent transconductance at any frequency is given by :

$$G_{meq}(s) = A_\nu(s) \cdot G_m = \frac{G_m}{1 + (R_SC_{GS} + G_mL_S) \cdot s + ((L_G + L_S)C_{GS}) \cdot s^2}$$

Hence, the equivalent transconductance at resonance is :

$$G_{meq0} = G_{meq@\omega_0} = A_{\nu\_max} \cdot G_m = \frac{G_m}{j\omega_0 \cdot (G_m L_S + R_S C_{GS})}$$

Since the input is impedance matched, the following condition holds :

$$R_S = \frac{G_m L_S}{C_{GS}} \Leftrightarrow R_S C_{GS} = G_m L_S$$

Assuming that $\omega_t \approx \frac{G_m}{C_{GS}}$ (see [48]) which is the transition frequency or, in other words, the frequency at which the gain of the transistor equals 1, the equivalent transconductance becomes:

$$G_{meq0} = \frac{G_m}{j\omega_0 \cdot (\underbrace{G_m L_S + R_S C_{GS}}_{R_S C_{GS}})} = \frac{G_m}{j\omega_0 \cdot 2R_S C_{GS}} \approx \frac{\omega_t}{j\omega_0 \cdot 2R_S}$$

In the case of matched impedance, the equivalent transconductance is independent on G_m.

Noise calculation

The noise small-signal equivalent schematic is obtained as previously, as shown in Figure 7.15.
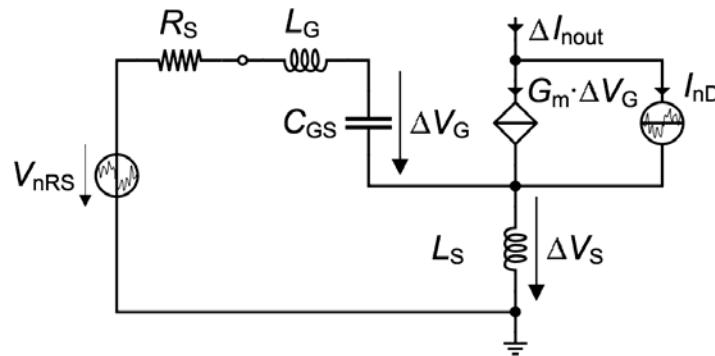
Figure 7.15: Noise small-signal common source LNA with inductance degeneration (see [48]).

The output noise current is given below by applying the superposition principle. It is important to note that it depends on s.

$$I_{nout}(s) = \underbrace{G_{meq} \cdot V_{nRS}}_{I_{nD} \text{ is removed}} + \underbrace{(I_{nD} + G_m \cdot \Delta V_G)}_{V_{nRS} \text{ is removed}}$$

When V_{nRS} is removed, the condition $G_m \cdot \Delta V_G = -\Delta V_S \cdot G_{meq} = -G_{meq} \cdot sL_S \cdot I_{nD}$

holds because the voltage across L_S drives the controlled source (see Figure 7.15). Hence, it gives :

$$I_{nout} = G_{meq} \cdot V_{nRS} + (1 - sL_S \cdot G_{meq})I_{nD}$$

The corresponding equivalent noise voltage is given by applying its definition using the obtained values :

$$
\begin{aligned}
V_{neq}(s) &= \frac{I_{nout}}{G_{meq}}(s) = V_{nRS} + \left(\frac{1}{G_{meq}} - sL_S\right)I_{nD} \\
&= V_{nRS} + \left(\frac{1 + (G_m \cdot L_S + R_S \cdot C_{GS}) \cdot s + ((L_G + L_S) \cdot C_{GS}) \cdot s^2}{G_m} - sL_S\right)I_{nD} \\
&= V_{nRS} + \left(\frac{1 + (G_m \cdot L_S + R_S \cdot C_{GS}) \cdot s + ((L_G + L_S) \cdot C_{GS}) \cdot s^2 - sG_m \cdot L_S}{G_m}\right)I_{nD} \\
&= V_{nRS} + \frac{1 + R_S \cdot C_{GS} \cdot s + ((L_G + L_S) \cdot C_{GS}) \cdot s^2}{G_m}I_{nD}
\end{aligned}
$$

At resonant frequency, this equation simplifies to :

$$V_{neq}(s = \omega_0) = V_{nRS} + j\frac{R_S C_{GS} \cdot \omega_0}{G_m} \cdot I_{nD}$$

The equivalent noise resistance is obtained as previously. Again, the minus sign that should appear when squaring j vanishes for the same reason as explained previously.

$$
\begin{aligned}
R_{neq}(s = \omega_0) &= R_S + \left(j\frac{R_S C_{GS} \cdot \omega_0}{G_m}\right)^2 \cdot G_{nD} \\
&= R_S + \left(\frac{R_S C_{GS} \cdot \omega_0}{G_m}\right)^2 \cdot \gamma_{nD} \cdot G_m \\
&= R_S + \frac{(R_S C_{GS} \cdot \omega_0)^2 \cdot \gamma_{nD}}{G_m}
\end{aligned}
$$

Finally, assuming that $Q_L = \frac{1}{\omega_0 \cdot R_S C_{GS}}$ is the quality factor of C_{GS} and of L_G at resonant

frequency, the noise figure is given by :

$$
\begin{aligned}
F(s = \omega_0) = \frac{R_{neq}(\omega_0)}{R_S} &\approx 1 + \frac{\gamma_{nD} \cdot R_S {C_{GS}}^2 \cdot {\omega_0}^2}{G_m} \\[2em]
&= 1 + \frac{\gamma_{nD} \cdot R_S C_{GS} \cdot {\omega_0}^2}{\omega_t} \\[2em]
&= 1 + \frac{\gamma_{nD} \cdot \omega_0}{Q_L \cdot \omega_t}
\end{aligned}
$$

In theory, there is no limit to the transition frequency, so the noise figure can be made as close as possible to 1 (or 0 dB !) with the source degenerated LNA. Since in practice it is not possible to have an infinite transition frequency, there is always some noise in the circuit; however, the noise figure can also be greatly reduced by using a high quality input impedance matching network. In other words, it means that the noise figure is determined only by the transistor characteristics and the quality of the surrounding components.

7.1.6 Conclusion on LNA architectures

The first two architectures were based on the common source configuration and showed a moderate noise figure that can never be smaller than 3 dB; however, the input impedance matching network of the LNA nº 2 allows to reach more easily this limit. The two following LNA architectures were based on common gate configuration and showed a great improvement on the noise figure which can be close to 1.76 dB here. However, the LNA nº 4 is better than the LNA nº 3 concerning the input impedance matching. The gate capacitance cancellation circuit depends directly on the input impedance matching network for these four LNA architectures.

The last LNA was based on common source with inductive degeneration and showed the noise figure which can be made as small as possible with the theoretic possibility to reach 0 dB. Although in practice it is not possible to have an infinite transition frequency, the noise figure can be greatly reduced by using a high Q input impedance matching network in addition with a high transition frequency transistor. This LNA architecture allows also to design the input impedance matching network independently of the gate capacitance cancellation circuit.

The results of the previous calculations are summarized in Figure 7.16.

In conclusion, the LNA nº 5 combines all of the characteristics that are required for a LNA

	LNA1	LNA2	LNA3	LNA4	LNA5
R_{in}	R_P	$\dfrac{R_P}{\left(1+Q^2\right)}$	$\dfrac{1}{G_{ms}}$	$\dfrac{1}{G_{ms}\left(1+Q^2\right)}$	$\dfrac{G_m L_S}{C_{GS}}$
G_{meq} (matched)	$\dfrac{G_m}{2}$	$\left(1+jQ\right)\dfrac{G_m}{2}$	$-\dfrac{G_{ms}}{2}$	$\left(1+jQ\right)\dfrac{G_{ms}}{2}$	$\dfrac{\omega_t}{2R_S\omega_0}$
F	$2+\dfrac{4\gamma_{nD}}{G_m R_S}$	$2+\dfrac{4\gamma_{nD}}{\left(1+Q^2\right)G_m R_S}$	$1+\delta_{nD}$	$1+\delta_{nD}$	$1+\dfrac{\gamma_{nD}\omega_0}{Q_L\omega_t}$

Figure 7.16: Summary of the five LNA architectures performance (see [48]).

and it will be consequently the architecture used for the design of this project.

7.2   Bipolar transistor LNA

At the very beginning of this project, there were a lot of discussions about which kind of transistor should be used to build the LNA. This section explains how the LNA design begins and why bipolar transistors were used first. It seems perhaps unusual to develop first the theory on LNA based on MOS transistor when beginning to design a LNA based on bipolar transistor. The main reason is that during the preliminary study of the project, it seems more reasonable to design a bipolar-based LNA because such a transistor shows usually better noise figure than MOS; it is specially the case with a circuit that has so much constraints on its performance. Another reason to choose the bipolar is a document found on the Web (see [52]) that describes a LNA made by a student during a scholar project which is very close to that is expected to be obtained here. His LNA is based on bipolar transistor and operates in the same band of frequency that the present one but without having a variable gain. In this section, the basics on how a bipolar LNA has to be designed are first explained; then, some possible architecture will be simulated in order to compare and improve the design.

The retained approach in the design of the LNA is to first design a single LNA with only one transistor and to test it until it gives at least a good impedance matching and a good gain. At this point, a gain of 5 dB is acceptable and more than 10 dB would be excellent. When

this will be done, the single LNA will be modified in order to make its gain adjustable but by taking care not to lose the impedance matching previously obtained. In every case, the noise is expected to be minimised by using the lowest resistor value as possible, as explained further.

The next step is to cascade the obtained single LNAs and to check whether they interfere to each other not only in terms of impedance matching but particularly in terms of stability. The simplest architecture that is expected to arise is to have four independant cascaded LNAs where everyone is controlled by a voltage that set their respective gain to – for example – 0 dB and 10 dB. Figure 7.17 shows the structure of such a LNA.
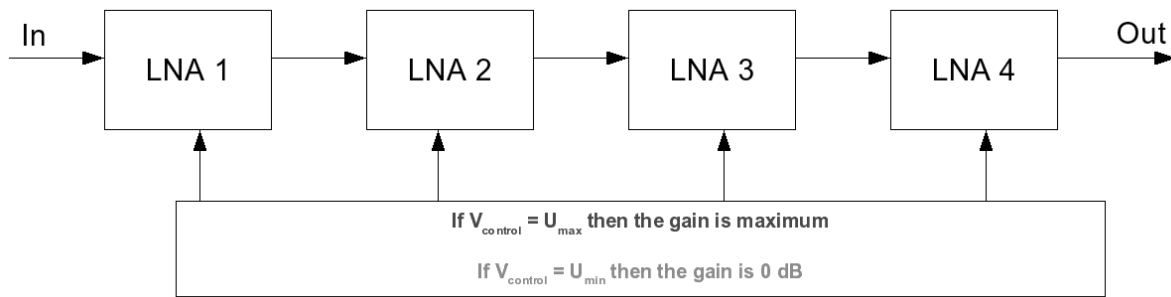
Figure 7.17: Synoptic view of the complete LNA made with four independent single LNAs

The gain of the whole chain is made adjustable by setting the correct voltage to every single LNA, hence, a 0 dB gain is obtained by setting all the single LNAs to 0 dB gain, where a 40 dB is reached by setting all of them to 10 dB gain. The intermediate gains (10 dB, 20 dB and 30 dB) are naturally obtained by setting to 0 or 10 dB the corresponding LNAs. In order to maintain the noise figure as small as possible, it is important to consider where the gain needs to be maximum or minimum. For this purpose, the Friis formula which gives the total noise figure obtained by cascading several amplifiers is of great interest. It is given below in the case of four amplifiers.

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 \cdot G_2} + \frac{NF_4 - 1}{G_1 \cdot G_2 \cdot G_3}$$

It explains that the noise figure is mainly determined by the noise figure of the first LNA since further LNA noise figures have progressively lower importance. There are thus two conclusions to this formula. The first is that the input LNA should have the lowest noise figure as possible and the second is that the gain of first stages must be the highest as possible in order to decrease the total noise figure. For this reason, when intermediate gain will be required, the

first LNAs will have the high gain and the further will have no gain. This would be done inside the FPGA or some external electronic devices.

7.2.1   The basic principles of bipolar-based LNA

Overview

The theory on bipolar-based LNA is much simpler than that on MOS because there is no gate capacitance to cancel. However, there are some resistors that are needed for biasing. The most generic architecture of a RF amplifier is given in Figure 7.18 (see [53]). Since impedance seen from input and output of the transistor can vary drastically, an input and output matching network is needed in order to avoid power loss. A more concrete example is given in Figure 7.19 that shows two possible RF amplifiers.
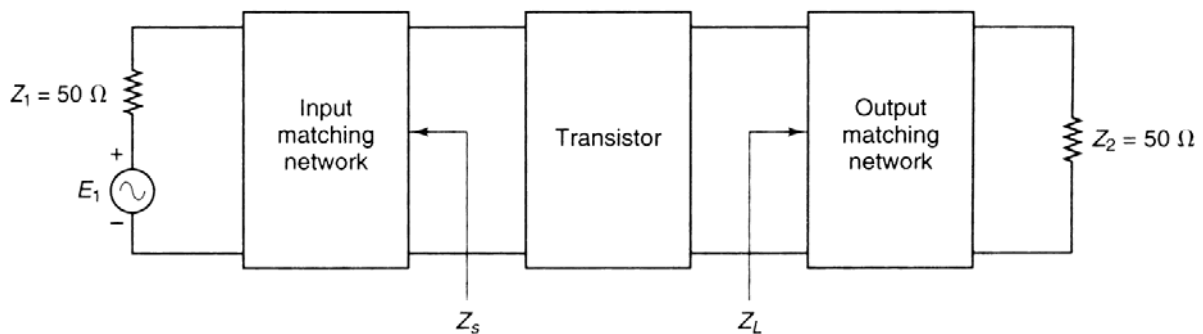
Figure 7.18: Structure of a microwave amplifier with either bipolar or MOS transistor (see [53])

These two amplifiers are designed to operate at 500 MHz [53]. The left one has four resistors that have a low value and that are in shunt towards the signal path. Thus, this amplifier will add much more noise than the right one that has only two resistors having quite high value. For this reason, the right architecture is an excellent candidate for the initial design of the LNA. The main rule in LNA design is to have as less resistor as possible and when resistors are needed, to try to make their value as low as possible when they are in series or, similarly, high when they are in shunt with the RF signal path.
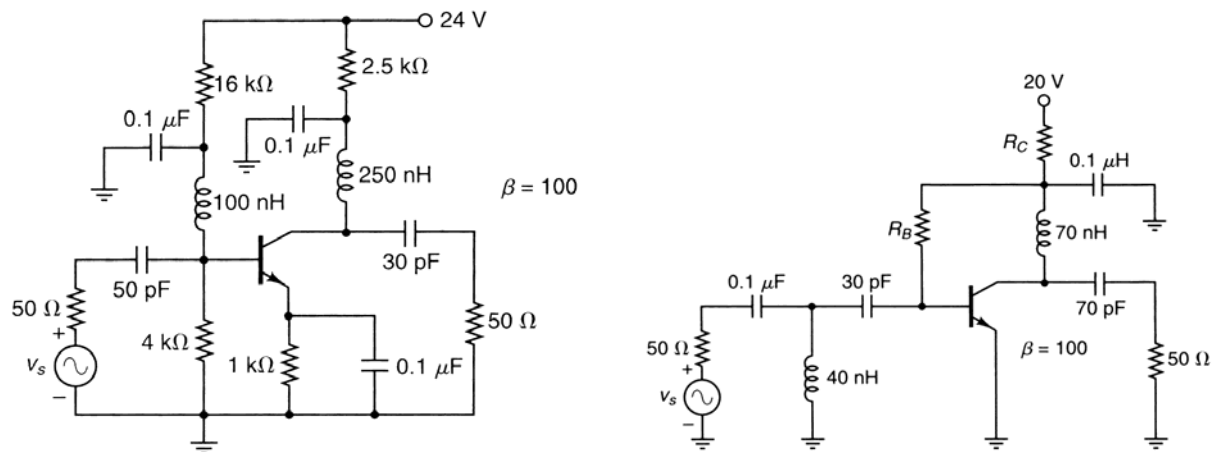
Figure 7.19: Two examples of RF amplifiers from [53] with bipolar transistor that operates at 500 MHz. The left one has 4 resistors used for biasing that add a lot of noise. The right one has only two resistors and is a good candidate for designing a LNA.

Practical considerations

The designs that were experimented in this section will be based on such "simple" circuit. Since the frequencies involved in the LNA are very high, it is quite impossible to calculate the circuit by hand because there are many parasitic effects that are too heavy and complex to model. For this reason, a simulation tool is needed. One of the most appropriate software for RF design is the Agilent ADS, for which models are given by most transistor manufacturers. The approach in this chapter is to start from the circuit given in reference [53] and to study the behaviour of the obtained amplifier around different transistor configurations until the desired characteristics are hopefully reached. For each case, there is a discussion on what was gained and what are the remaining problems to solve.

Another important aspect that can modify considerably the results is the choice of the transistor. The transistors were mainly chosen according to their characteristics but also to their availability on the market. The realm of RF transistors is huge, so it is important to choose finely what transistor would be able to be used to achieve the expected result. The main constraints are to be low noise and to be able to operate conveniently at 5 GHz at least; this reduces drastically the spread of the choice. In spite of its importance in most RF circuits, the current consumption is not a vital constraint in this project (a consumption in the range of 100 mA is acceptable provided that the circuit works as expected). Some searches on the Web at most RF components manufacturer and suppliers sites give a list of possible candidates for the transistor.

Since some components are sometimes difficult to buy - because they are obsolete or simply because they are only sold for large quantities, it is wise to select other types of transistor from different suppliers in case one is not available. According to that search, the following transistor were retained :

- MT3S35T, from Toshiba : NF = 1.4 dB @ 2 GHz, gain = 13 dB

- BFG424F, from Philips : NF = 1.2 dB @ 2 GHz, gain = 18.5 dB

- NESG2030M04 (aka 2sc5761), from NEC : NF = 0.9 dB @ 2 GHz, gain = 20 dB

Since the NESG2030M04 shows the most impressive characteristics, it was chosen for the simulations and design although it was not immediately available, because there was a good probability to find it from other suppliers and also because waiting for being sure it was available would induce too much time lost. Anyway, the other transistor were finally not available at all and during simulations, another transistor based on pHEMT technology and having outstanding characteristics, was found and was easily available.

7.2.2   Architecture n° 1 : The common emitter

The first architecture described in this section is the common emitter, which is an almost straightforward copy of the right schematic shown in Figure 7.19. The common emitter configuration is better than common base because in this configuration, the input and output are more independent thus improving the S_{12} value. The common collector is not discussed since is gives no gain at all. The schematic shown in Figure 7.20 gives the simplest form of the common emitter amplifier configuration based on the NESG2030M04 transistor without impedance matching network, which will be designed further. The bias of the transistor is made with only two resistors according to the following criteria as explained in the transistor datasheet : the collector-emitter current I_{CE} is set to 5 mA because it gives the best noise figure and it allows also a Gain-BandWidth of approximately 18 GHz, and V_{CE}, the voltage across the collector and the emitter, is set to approximately 2 volts. The current gain β of the transistor equals approximately 250 assuming an I_B of 5 mA. Assuming a power supply voltage of 5 volts, the value of the resistors is thus given by the following equations :

$$R_c = \frac{V_{CC} - V_{CE}}{I_{CE}} = \frac{5V - 2V}{5mA} = 600\Omega$$

$$R_B = \frac{V_{CE} - U_j}{I_B} = \frac{V_{CE} - U_j}{I_{CE} \cdot \frac{1}{\beta+1}} \approx \beta \cdot \frac{V_{CE} - U_j}{I_{CE}}$$

$$= 250 \cdot \frac{2V - 0.7V}{0.005mA} = 65k\Omega$$

The resistor values are rounded to the nearest normalised standard value, i.e. 620Ω and 68 kΩ respectively. The inductor L1 acts as a RFC to avoid the RF signal to be short-circuited through the power supply.
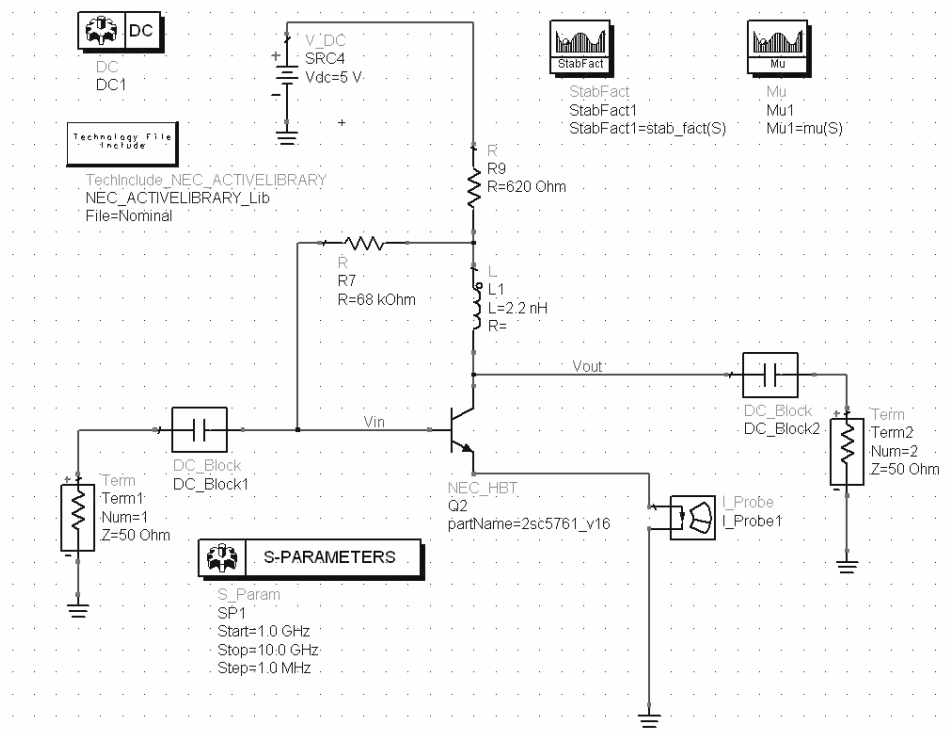

Figure 7.20: The simplest form of common emitter (without impedance matching network here)

The simulation results of this circuit are given in Figure 7.21. The bias point is near the calculated one; the junction drop voltage U_j is bigger than the 0.7 volts that are commonly found with traditional transistors and equals approximately 0.82 volts. The input and output
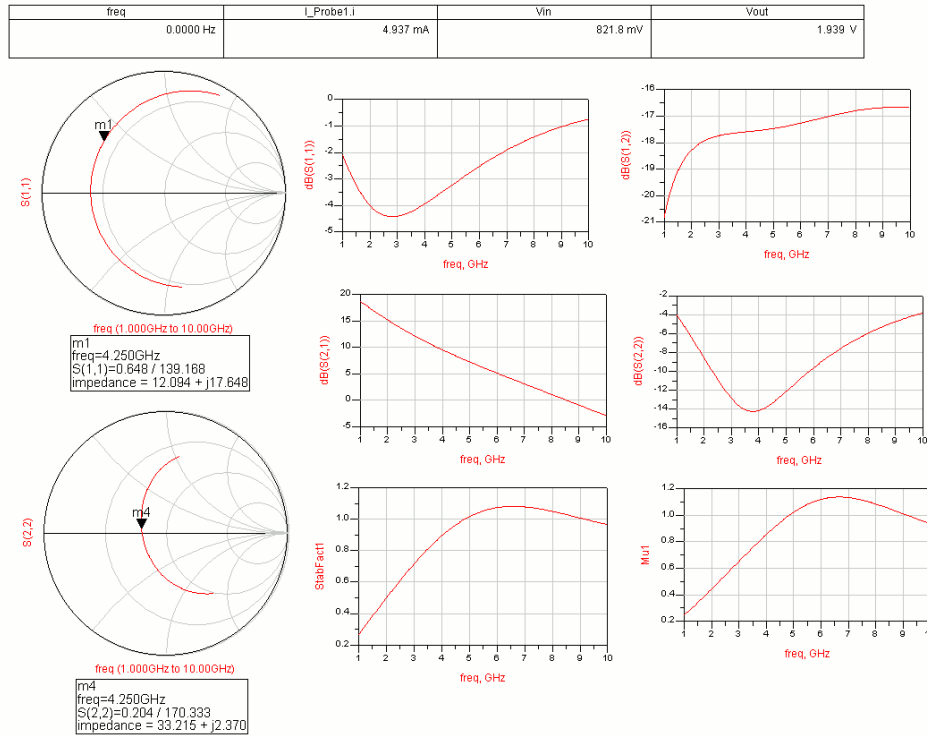
Figure 7.21: Simulation results of the simple common emitter amplifier

are not matched to 50 Ω and need consequently an impedance matching network. Although the circuit is not unconditionaly stable because the K stability factor – or Rollett's factor – is smaller or roughly equal to 1 (see [54]), it does not oscillate. One reason is the fact that the S_{11} and S_{22} parameters are smaller than 0 dB, so the impedance mismatch does not add positive feedback. The other reason is the feedback resistor which is too high in comparison with the Miller capacitance that lies intrinsically between the base and the collector of the transistor. In addition, the S-parameters are very close to those given in the transistor datasheet.

The ADS software allows to design impedance matching network with the help of a Smith chart (see Figure 7.22). By setting the working frequency at 4.25 GHz and the normalisation impedance to 50Ω, it is possible to design very simply such a network. The input impedance seen from the source is $12.1 + j17.6\Omega$. So, by moving the point on the chart until it reaches the center which corresponds to the 50Ω, gives immediately the components and their value that are needed for the matching network.

This matching network is then included in the amplifier schematic as shown in Figure 7.23
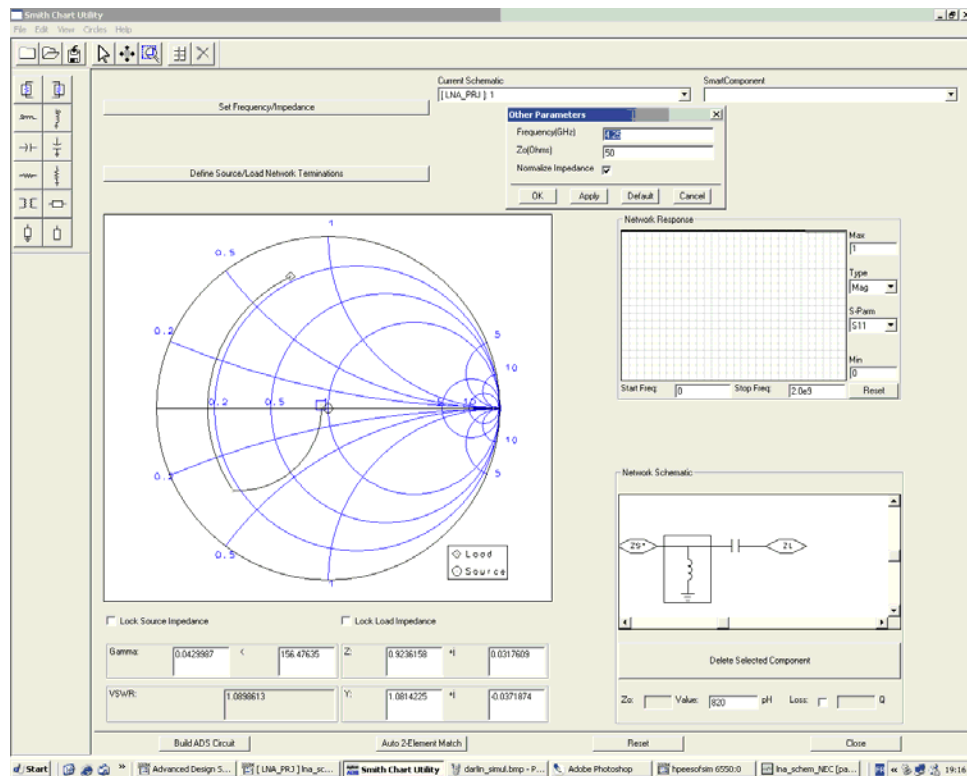
Figure 7.22: Smith chart for the input impedance matching network. The matching network is a high-pass because the series capacitor works also as a DC block.

and the circuit thus obtained is simulated in order to check whether the input impedance matching is effective.

The simulations of the input matched circuit are shown in Figure 7.24. The input matching is excellent as shown by the S_{11} value near 4.25 GHz and the gain of the amplifier, shown by S_{21}, is greatly improved.

The next step is to design the output impedance matching network; the process is exactly the same as what was done for the input. The corresponding Smith chart is shown in Figure 7.25.

The corresponding output matching network is then included in the schematic of the amplifier as shown in Figure 7.26. This ends the design of the common emitter amplifier.

The simulation results of the complete amplifier are shown in Figure 7.27. At this point

Figure 7.23: Common emitter amplifier with the input impedance matching network

the output impedance is outstandingly matched as shown by S_{22} which is near -50 dB. The gain is not significantly modified. However, the input impedance is now degraded because of the S_{12} that is not sma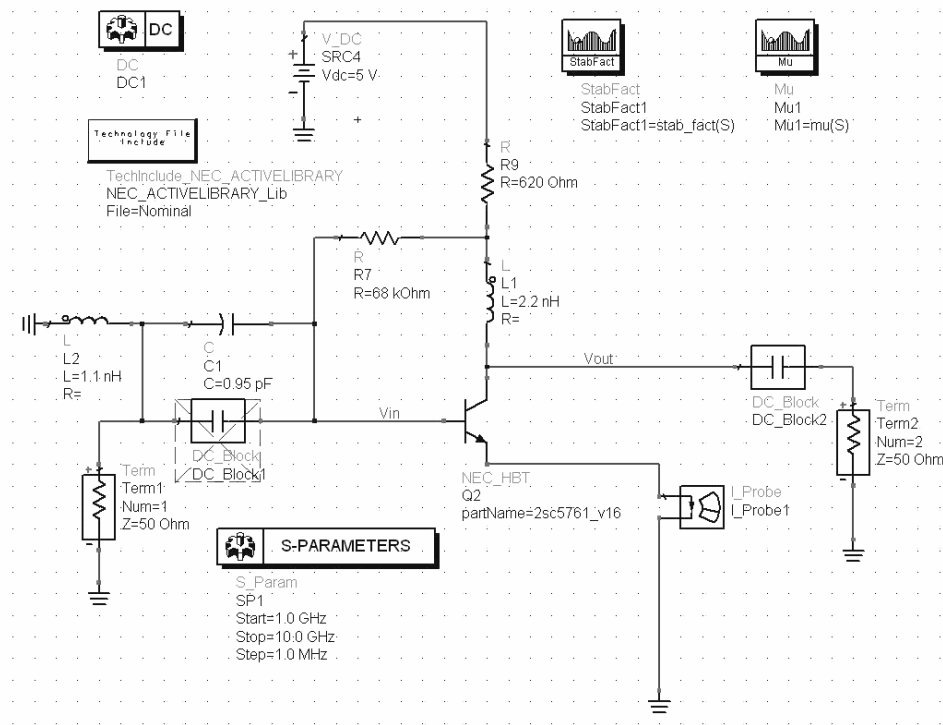ll enough to make both input and output impedance matching network designs independent. This is caused by the Miller capacitance, which has a high effect at such frequency, and leads to a problem because the input impedance needs a particularly good impedance matching since it is connected to the antenna.

It is not possible to re-design the input impedance matching network again because it will change the output impedance matching conversely. In addition, when the bias current is changed in order to experiment some gain variation, the matching of both input and output changes drastically. A possible approach to solve this problem is to reconsider the complete amplifier architecture. Since the impedance matching is needed for optimising the power transfer of the signal at high frequency, it is perhaps possible (but not verified experimentally) to give up the impedance matching of every stage and to consider only the voltage amplification provided that the connection between two successive stages is smaller than one tenth of the wavelength. If this assumption is true, it might be possible to design a first input amplifier which is conveniently matched to the antenna and then, to design intermediate amplifiers with
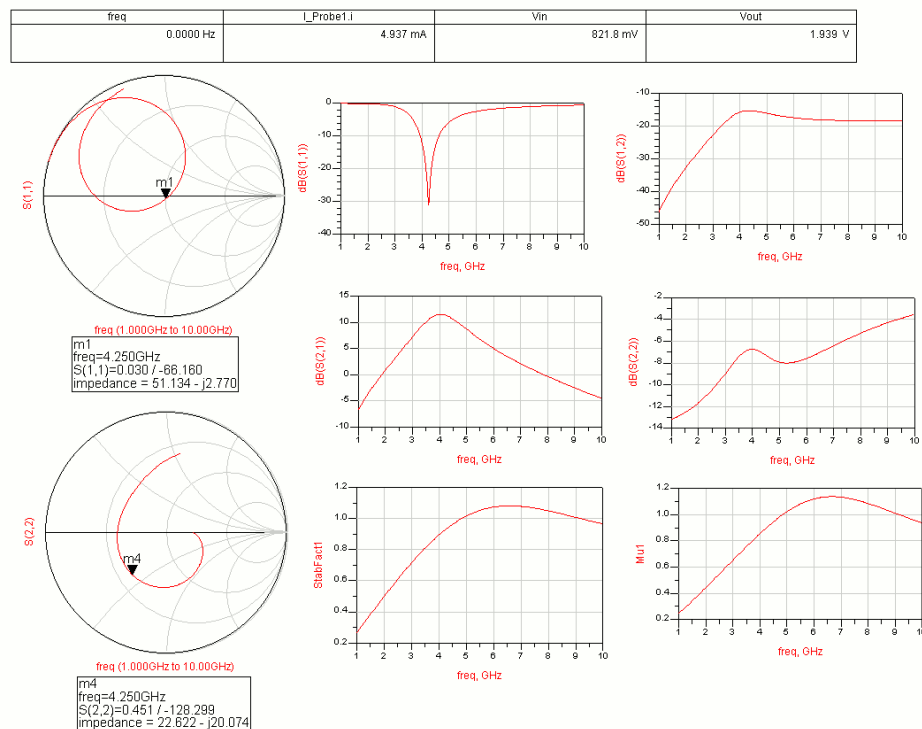
Figure 7.24: Simulation of the common emitter amplifier with input impedance matching network

adjustable gain where the impedance matching is not critical itself, and lastly to design an output amplifier with an output impedance matched again for the further devices. The remaining part of this section will assume that this hypothesis might be true in order to limit the complexity of the problem.
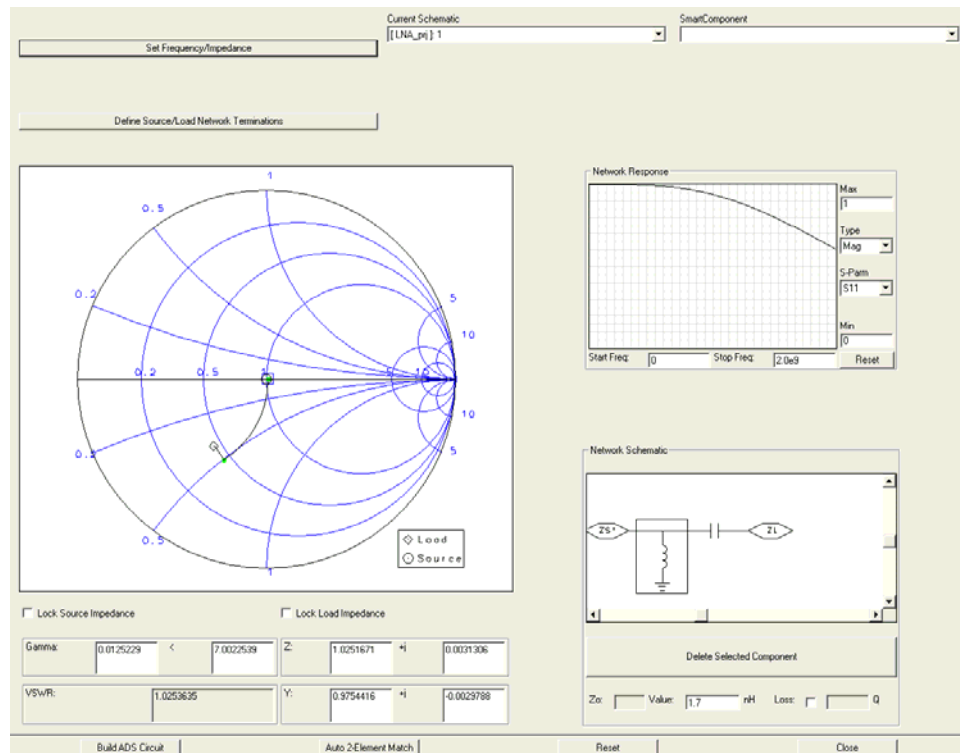
Figure 7.25: Smith chart of the output impedance matching network
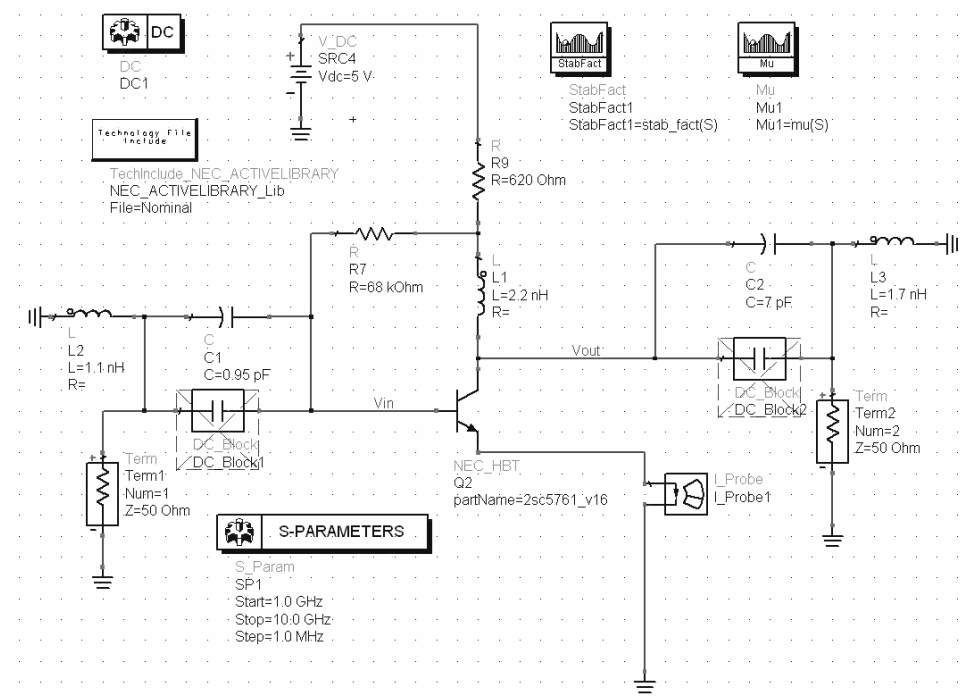
Figure 7.26: Common emitter amplifier with both input and output impedance matching networks
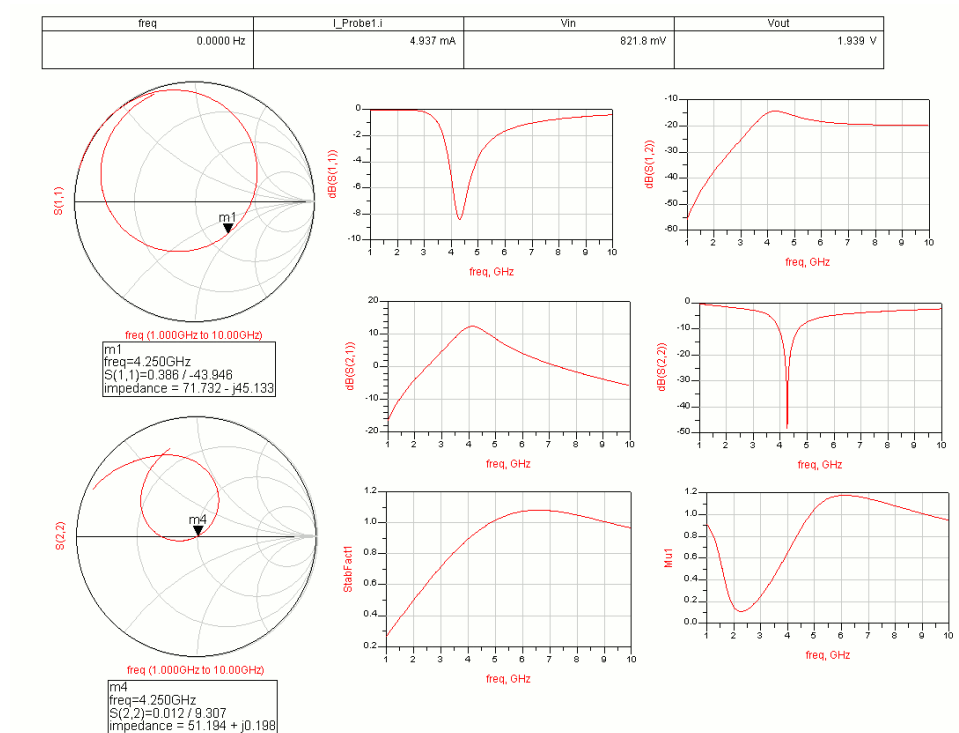
Figure 7.27: Simulation results of the common emitter amplifier with both input and output matching networks

7.2.3   Architecture n° 2 : The cascode amplifier

The second architecture that was experimented is the cascode amplifier. Since the mismatch that occurs with the previous circuit is mainly caused by a too bad S_{12}, improving this S parameter will normally allow to match both sides of the amplifier almost independently. In the case where the idea to match only the input and then to amplify the voltage is applied, such an improvement will be very useful because the designer have not to determine with a high precision that are the input and output impedance of the intermediate amplifiers. He or she has only to ensure roughly that the output impedance is low and the input impedance is high. The cascode amplifier can strongly improve the S_{12} parameter by virtually decreasing the Miller capacitance of the amplifying transistor. This is done by adding a second transistor in common base configuration which has a very high input impedance, as shown in Figure 7.28 below.
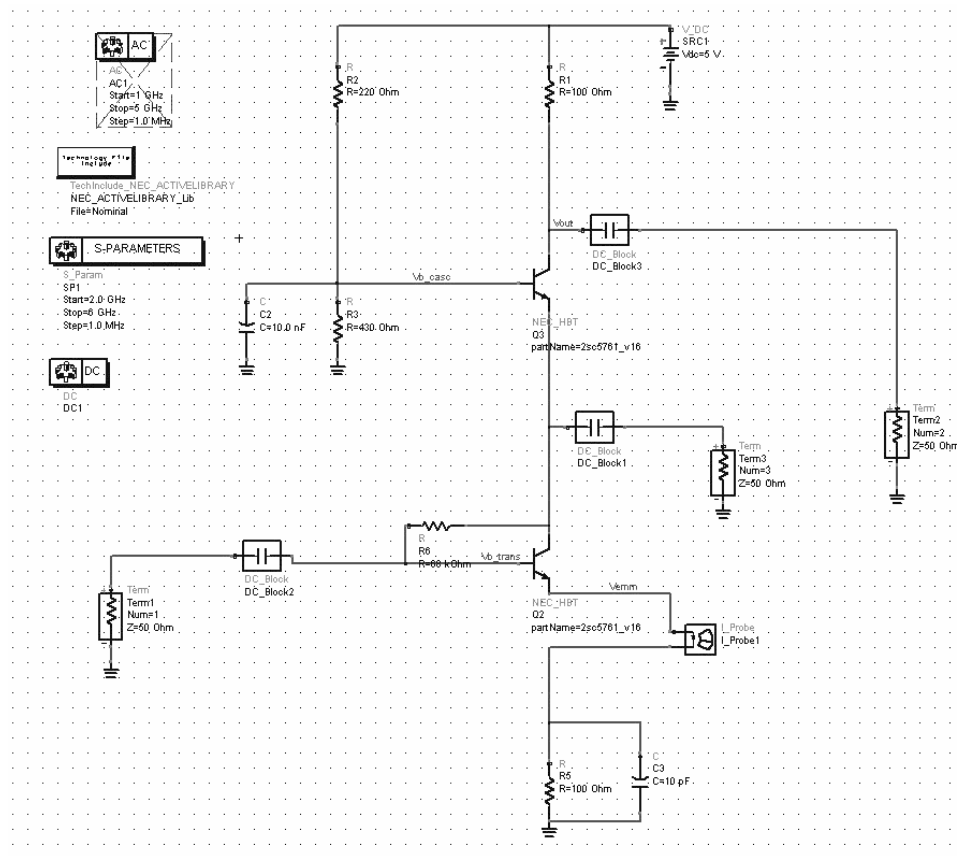
Figure 7.28: The schematic of the cascode LNA

The amplifier transistor is biased as previously done with the common emitter with a feedback resistor and an emitter degeneration resistor. The I_{CE} current and V_{CE} voltage of both

transistors are the same, for the same reasons as previously explained. The Vb_{casc} voltage is set to 3.2 V. The emitter of the cascode transistor is thus approximately equal to 2.5 V. The Vem voltage is 0.5 volts.

The simulation results of the cascode amplifier are given in Figure 7.29.
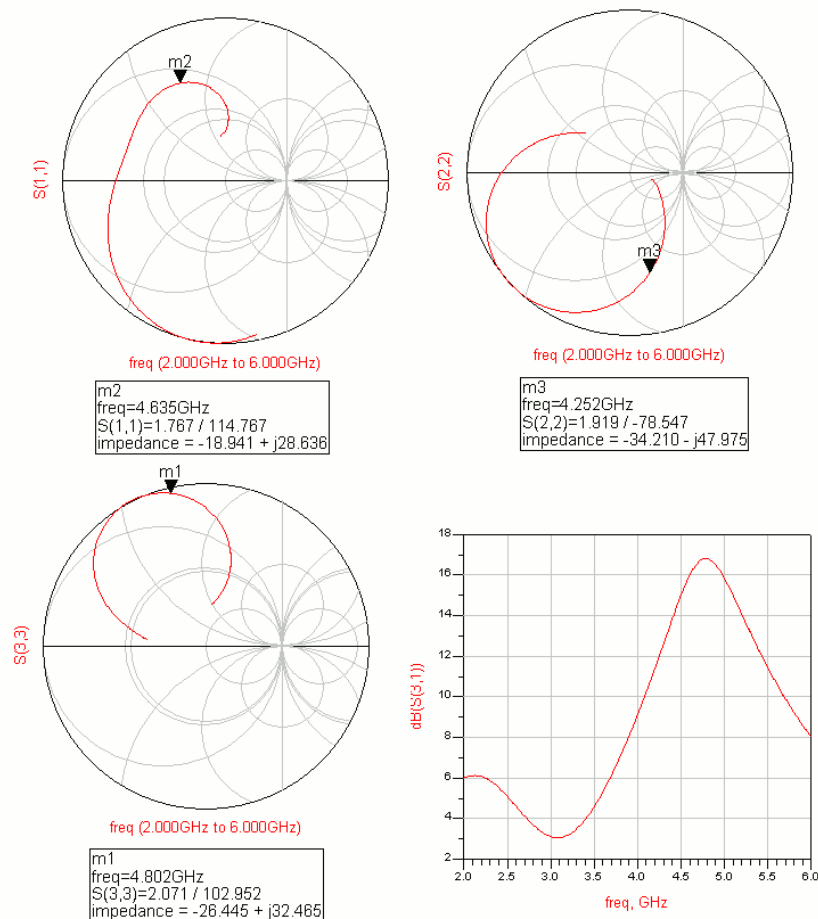
Figure 7.29: The simulation results of the cascode LNA

The simulation shows that this circuit oscillates strongly. The reason of this is because the transistor is modelled as a 2-ports with its own S-parameters. When two transistors are connected in a cascode configuration, the simulator interprets the collector of the one and the emitter of the other as two impedances that need to be matched in order to have a good RF behaviour. Since the impedances of the transistor are all different, the S-parameter simulation shows an important mismatch that induces oscillations in the circuit. In practice, such oscillations will seldom occur if the circuit is well designed because the transistors will be mounted

as close as possible in order to make the apparent mismatch negligible toward the wavelength. It is however not possible to indicate to the simulator that the mismatch between transistor is not relevant in this circuit, so it is impossible to take an advantage of S-parameters simulation in the case of a RF cascode. For all these reasons, the gain shown in the fourth chart is not representative of the reality.

It is easy to show that the circuit does not oscillate in itself by performing an AC analysis whose results are shown in Figure 7.31. For this purpose, the schematic of the cascode amplifier is modified as shown in Figure 7.30 in order to perform the AC simulation.
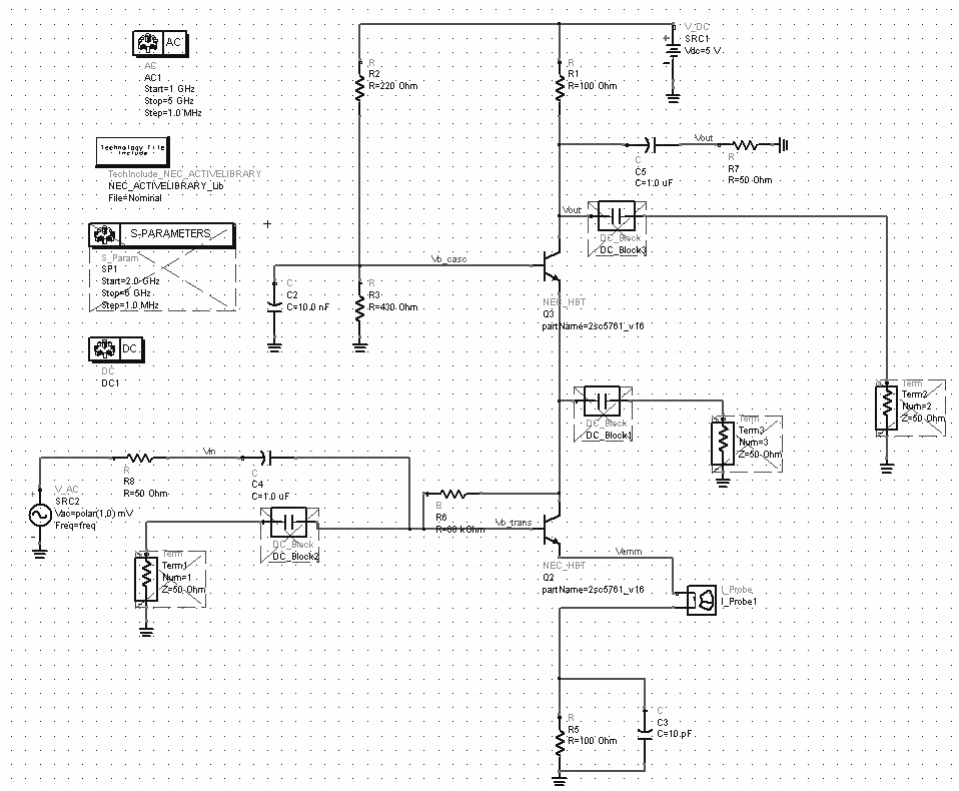
Figure 7.30: The same schematic as in figure 21 but for AC simulation

Although this simulation confirms that the circuit is in fact stable, it is not possible to design a convenient matching network by performing only an AC analysis. Thus, a dilemma arises : either performing an AC analysis in order to simulate and check with a good accuracy that the circuit has some gain without oscillating but this makes impedance matching impossible due to theoretical limitations of the AC analysis, or either performing the S-parameters analysis that
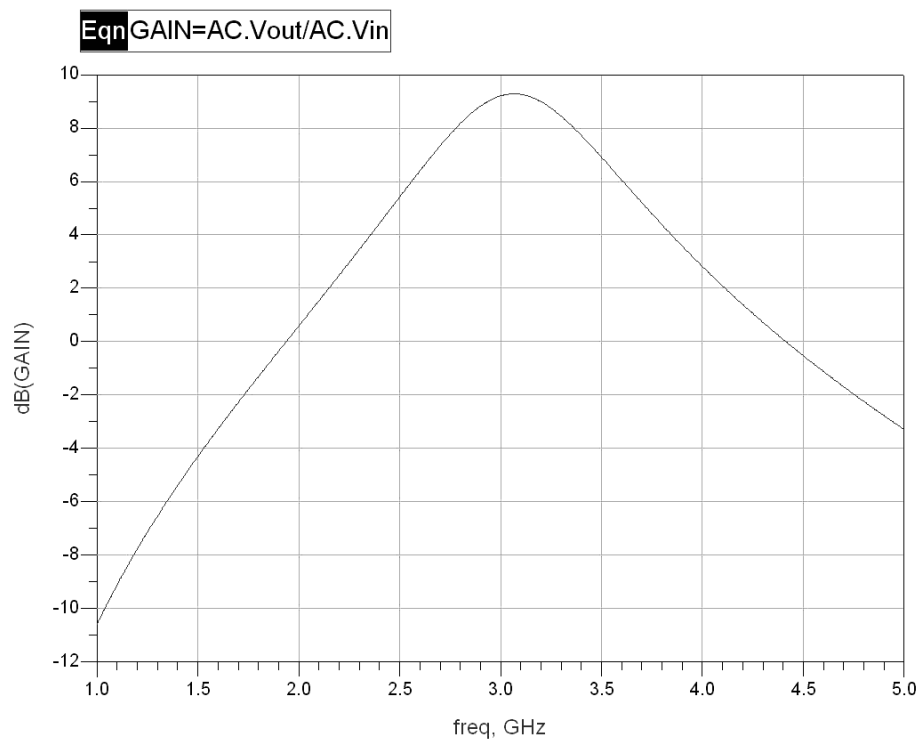
Figure 7.31: AC simulation of the cascode gain

allows theoretically to design the impedance matching but, here, oscillations happen because of the apparent mismatch between both transistors. Ideally, this circuit needs an intermediate kind of analysis that would be based on S-parameters analysis for the input and output in order to model the circuit as a 2-ports but that would in fact perform internally an AC analysis between components of the circuit.

7.2.4   Architecture n° 3 : The Darlington amplifier

The Darlington amplifier gives, like the cascode, an outstanding S_{12} that ensures a good separation between input and output that allows the independence of the impedance matching networks. The schematic of this amplifier is given in Figure 7.32. As explained previously, the output impedance matching is not critical in itself because it is assumed that intermediate amplifiers perform a voltage amplification only, so output impedance matching is not of high importance here.
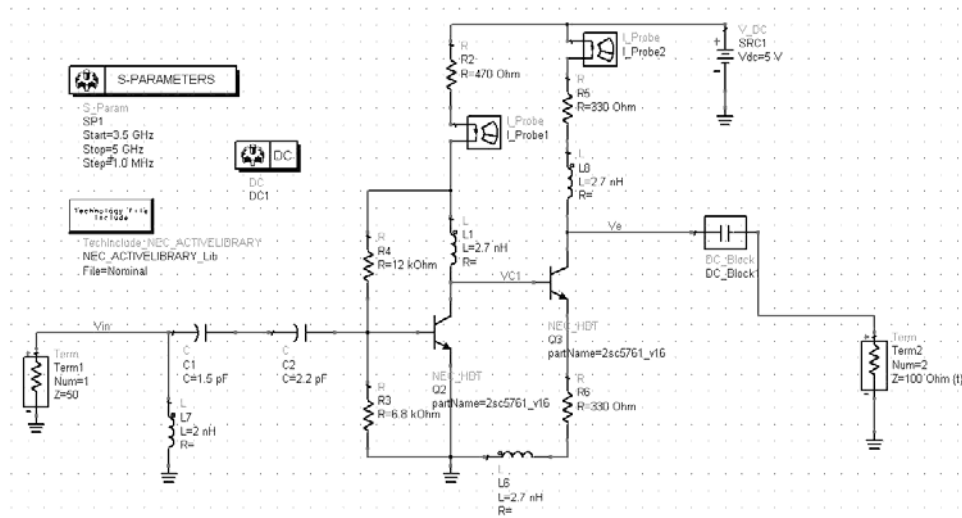
Figure 7.32: The schematic of the Darlington LNA

The first transistor is a common emitter whose base voltage is 1.8 V and collector-emitter current is 5.35 mA. The $VC1$ point is around 2.5 V. The second transistor is also a common emitter amplifier with emitter degeneration. Its emitter voltage is at 1.65 V (as seen previously, the U_J voltage drop is not equal to 0.7 volts with these transistors, it rather lies between 0.8 and 0.9 volts depending on the bias), thus the collector-emitter current is 5 mA. The simulation results are shown in Figure 7.33.

The gain is excellent (more than 10 dB) as well as the input impedance matching (S_{11} is close to -25 dB in the middle of the frequency band of interest. The S_{12} is so low that the unilateral 2-ports hypothesis holds naturally. The output impedance is roughly matched (S_{22} is approximately -4 dB) but this is less important since it is expected to amplify the voltage further. The noise figure (1.76 dB) is excellent as well as the noise matching in general. This circuit is thus a very good candidate for an input amplifier but its gain is not yet adjustable.
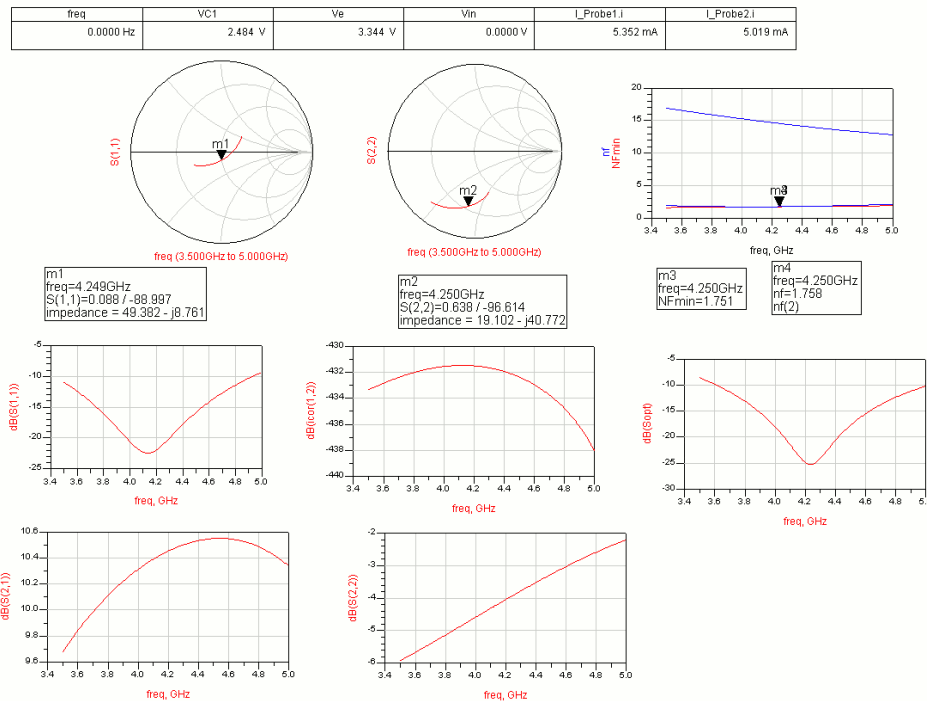
Figure 7.33: The simulation results of the Darlington LNA

7.2.5 Conclusion on bipolar transistor

The two first simulations show very poor results when designing an Ultra-Wide Band LNA with a bipolar transistor. The Darlington circuit was the best that was obtained on all the simulations made with the bipolar transistor, although it was only in the case of a constant gain. For this reason, it is an excellent choice for the input amplifier in the case where a chain is made with several amplifier cells. The question of designing the intermediate voltage amplifiers and the output amplifier stays open at this point of the project. This is mainly due to the finding of another transistor, based on the pHEMT technology, and that shows outstanding characteristics particularly towards the noise and input/output impedance, for designing the LNA as explained in detail in the next section. Actually, it seems more reasonable to use bipolar transistor mainly for narrow-band C-class amplification at such frequency range since it is the most common use of bipolar transistors in RF applications. In addition, general knowledge articles about bipolar-based LNA made with discrete components are rather scarce because most applications are today integrated and thus use MOS rather than bipolar transistors. In conclusion, simulating such a LNA with bipolar transistor was an excellent exercise in itself and was a good introduction to what are the difficulties that have to be solved further in this project.

7.3   pHEMT transistor LNA

This section will describe the pHEMT transistor based LNA with its outstanding RF characteristics. The existence of this transistor was discovered during a casual discussion about RF designs and amplifiers. Its performance was so high that the bipolar simulations were given up in favour of this new transistor. The model chosen for designing the LNA was the ATF35143 from Avago technologies. Here are some of its characteristics :

- a working frequency range from 450 MHz until 10 GHz;

- a noise figure of 0.4 dB at 2 GHz and 0.5 dB at 4 GHz;

- a gain that can reach more than 13 dB at 4 GHz and a current drain of 30 mA;

- a very easy to match input and output, as explained further;

- a gain that can be, like any other FET, be adjusted with the gate voltage.

In addition, the manufacturer gives many excellent application notes and a datasheet that explains in detail how to use the transistor and how to make designs with many examples and case studies. The following sub-section will describe what a pHEMT transistor is and how it works; then, the next sub-section will describe the design of the LNA with corresponding simulations.

7.3.1   What is a pHEMT transistor

This section describes the pHEMT technology, which is an improvement of the MOS transistor in the field of radio-frequency design. Since it is not the purpose of this document to explain all details on this kind of transistors, only relevant information that is needed to understand the design will be explained (see Figure 7.34).

A simple and intuitive explanation on the pHEMT transistor is given in [55] while a formal and complete description is given in [56].

Ordinarily, the two different materials used for a heterojunction must have the same lattice constant (spacing between the atoms). An analogy - imagine pushing together two plastic combs with a slightly different spacing- at regular intervals, you'll see two teeth clump together. In semiconductors, these discontinuities are a kind of "trap", and greatly reduce device performance. A HEMT where this rule is violated is called a pHEMT or pseudomorphic HEMT. This
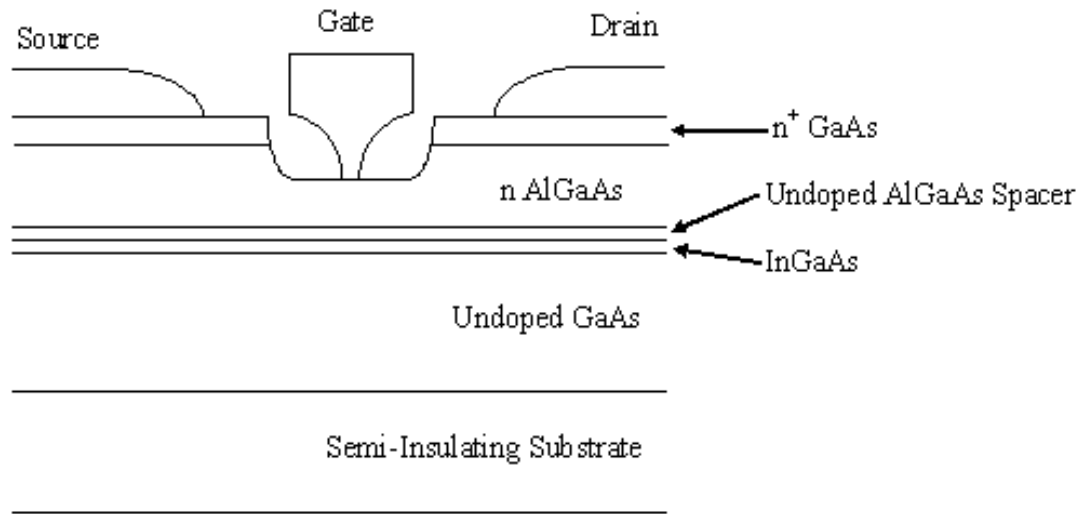
Figure 7.34: Cross view of a pHEMT transistor

feat is achieved by using an extremely thin layer of one of the materials - so thin that it simply stretches to fit the other material. This technique allows the construction of transistors with bigger bandgap differences than otherwise possible. This gives them better performance.

Another way to use materials of different lattice constants is to place a buffer layer between them. This is done in the mHEMT or metamorphic HEMT, an advancement of the PHEMT developed in recent years. In the buffer layer made of AlInAs, the indium concentration is graded, so that it can match the lattice constant of both the GaAs substrate and the GaInAs channel. This brings the advantage that practically any Indium concentration in the channel can be realized, so the devices can be optimized for different applications (low indium concentration provides low noise, high indium concentration gives high gain).

In spite of the fact that pHEMT transistors are based on high technology achievements, they can be seen and modelled like classical MOS transistors. For this reason, the theory explained in Section 7.1 can be applied straightforwardly in the design of the pHEMT-based LNA described here. In addition, the manufacturer of the transistor gives the ADS model of its electrical behaviour, so there is almost nothing to calculate directly since the ADS simulator will provide accurate results on what happens with real circuit.

7.3.2 The single LNA

It was said previously that the manufacturer has prepared many excellent documents on its transistor. One of this document is an Application Note (see [57]) that describes in detail a LNA which works at 3.5 GHz. Its schematic is reproduced in Figure 7.35 below. It was then not very difficult to modify it a little in order to have a LNA working in the 4.0 to 5 GHz frequency range. The components value in the circuit were first these given in the application notes, as shown in Figure 7.36, and the circuit was simulated in order to see how it behaves like this; then, depending on the obtained results, the components values were adapted until an optimum was reached.

The transistor is in common source with inductance degeneration configuration. The degeneration is made with two microstrip inductances LL1 and LL2, since the transistor has two source pads which need to be degenerated both in the same way. Simulations show that 1 nH is a good value for these both inductances. C1 and L1 are an impedance matching network for the input. R2 is used for in-band stability, as C2 and C4. L2 and L3 are RFC used for biasing the transistor; their Q are very important from the point of circuit loss and hence the noise figure. R1 and R3 are decoupling resistors and they also de-Q the RFC; they provide low frequency stability by providing a resistive termination.
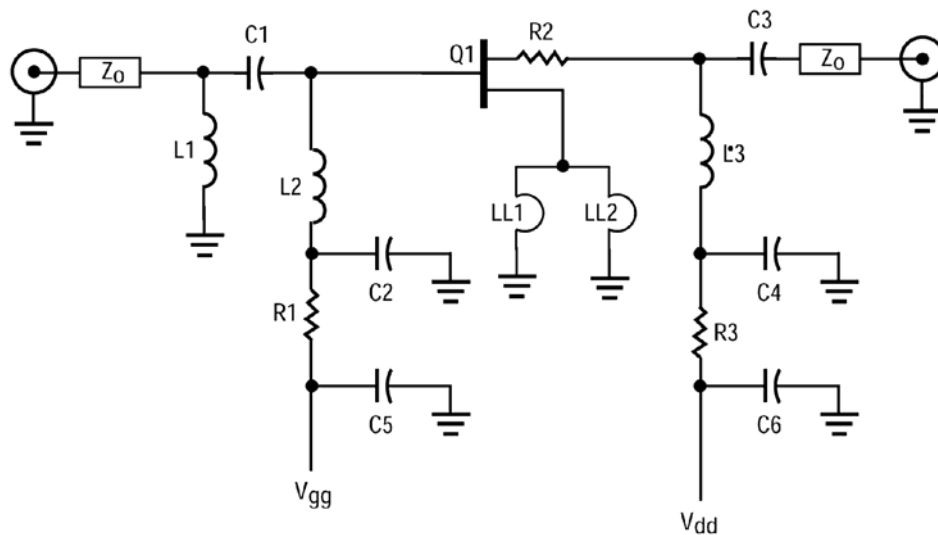

Figure 7.35: Suggested amplifier for 3.5 GHz given in the Application Note (see [57])

The component values suggested by the manufacturer are shown in Figure 7.36.

C1	1.5 pF chip capacitor (C1005COG1H1R5C)
C2, C4	4.0 pF chip capacitor (C1005COG1H040C)
C3	2.0 pF chip capacitor (C1005COG1H020C)
C5, C6	1000 pF chip capacitor
L1	2.2 nH inductor (Toko LL1005-FH2N2S)
L2, L3	3.3 nH inductor (Toko LL1005-FH3N3)
LL1, LL2	Strap each source pad to the ground pad with 0.030" wide etch. The jumpered etch is placed a distance of 0.037" away from the point where each source lead contacts the source pad.
Q1	Agilent Technologies ATF-35143 PHEMT
R1	47 Ω chip resistor
R2	10 Ω chip resistor (Murata CR05-10RJ)
R3	53 Ω chip resistor
Zo	50 Ω Microstripline

Figure 7.36: Values suggested in [57] for the LNA

By performing many simulations form the original schematic, the LNA was modified in order to achieve excellent results in the 4.0 and 4.5 GHz frequency range. The obtained circuit is shown in Figure 7.37.

This circuit topology is very close to to the original, with exception of L1 and C4 in Figure 7.35 that were removed in Figure 7.37 because they introduce instability and gain loss with the new frequency range. The other component values were somewhere slightly modified in order to achieve a good trade-off between stability and high gain. The simulation results are shown in Figure 7.38. They show that with a source degeneration of 1 nH, the K stability factor is 1.7 on average and the gain is 8 dB with an almost flat magnitude of the transfer function. The impedance matching is very good for the output and outstandingly good for the input. In addition, the noise factor is smaller than 0.9 dB. These results were obtained with a gate voltage of -0.2 volts. It is possible to change the drain current of the transistor, and thus the gain of the amplifier, by changing the gate voltage as shown by the following equation :

$$V_{GS} = V_P \left(1 - \sqrt{\frac{I_d}{I_{dss}}} \right)$$

where V_P is the pinch off voltage and I_{dss} is the saturation drain current. By changing the
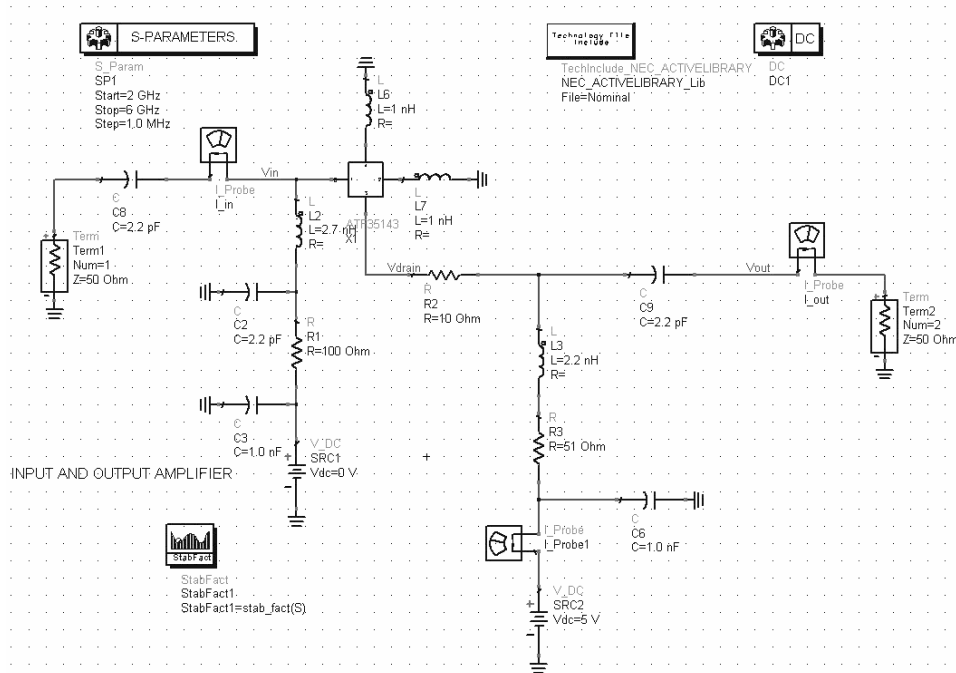
Figure 7.37: Schematic of the LNA with 1 nH of source degeneration

gate voltage to -0.9 volts, the gain can be reduced until near 0 dB as shown in Figure 7.39. The impedance matching is of course modified but the corresponding S parameters stay below 0 dB, so the circuit is stable. The noise figure becomes higher and reaches 2 and 2.5 dB. This confirms that was explained with the Friis formula about the importance of having high gain in the first stages of the LNA cascade. For all these reasons, it is this design that will be used for designing the single LNA which will be made for testing first how it behaves in practice and to decide whether it will be kept for the complete LNA. Further sections will explain how it was made and show its measured characteristics which are excellent.

There is a last point to simulate with the single LNA which is the minimum source inductance required for ensuring the amplifier stability. This is shown in Figure 7.40 by setting the source inductance to 0.3 nH which is the lowest acceptable value, with a small safety margin, before the circuit becomes unstable.

The simulation results are shown in Figure 7.41. The gain is higher but the impedance matching is worse. The noise figure is a bit higher than with 1 nH but it still stays in an acceptable range near 1.1 dB. Of course, the K factor is close to 1 and the S_{11} and S_{22} parameters are close to 0 dB, thus the circuit is close to the instability. In practice, as explained later, there are
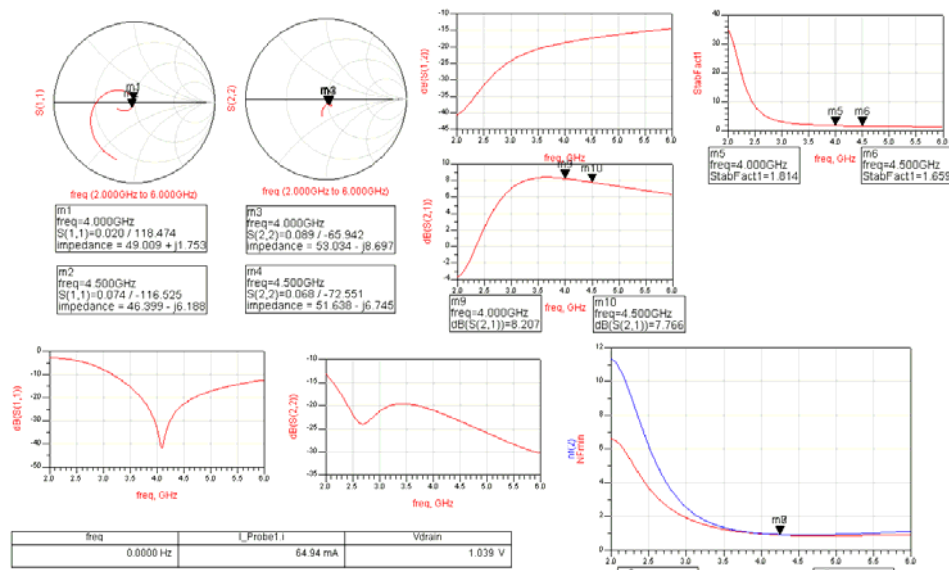
Figure 7.38: Simulation results of the LNA with 1 nH source degeneration and V_G at -0.2 volts

Figure 7.39: Simulation results of the LNA with 1 nH source degeneration and V_G at -0.9 volts

some parasitic inductances on the PCB that make this circuit not so bad for a first realisation. There are now enough elements for discussing the case of the complete LNA.
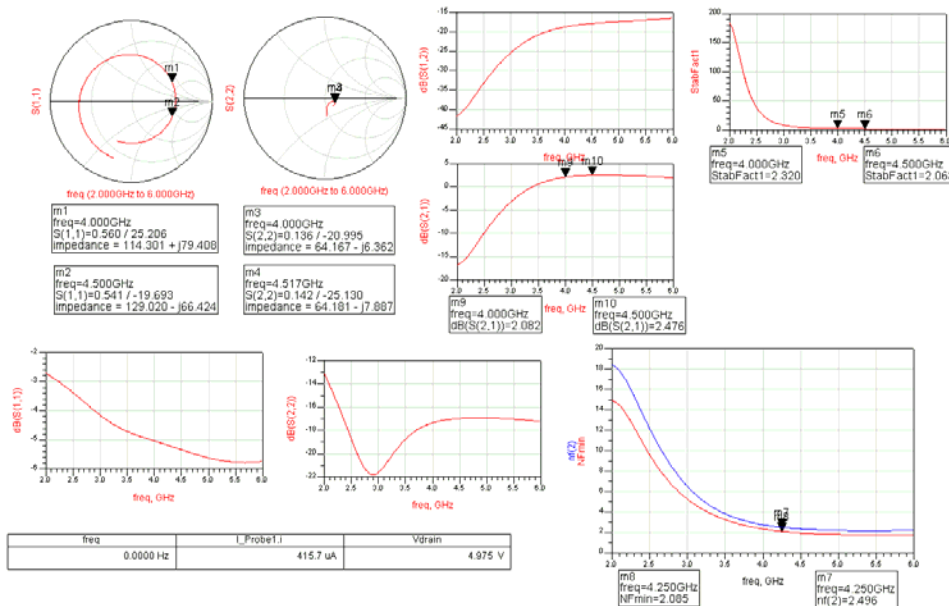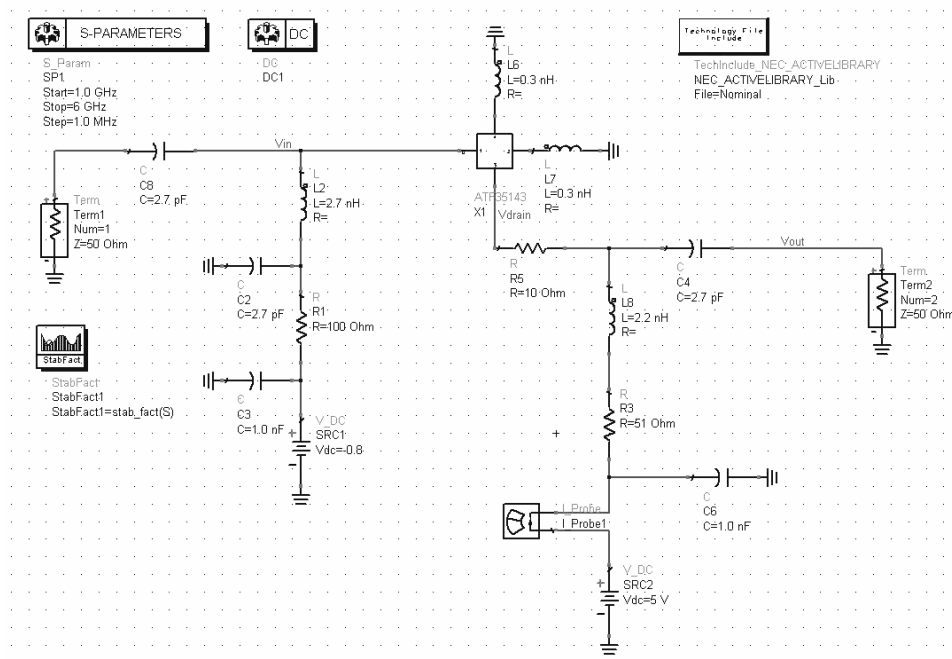
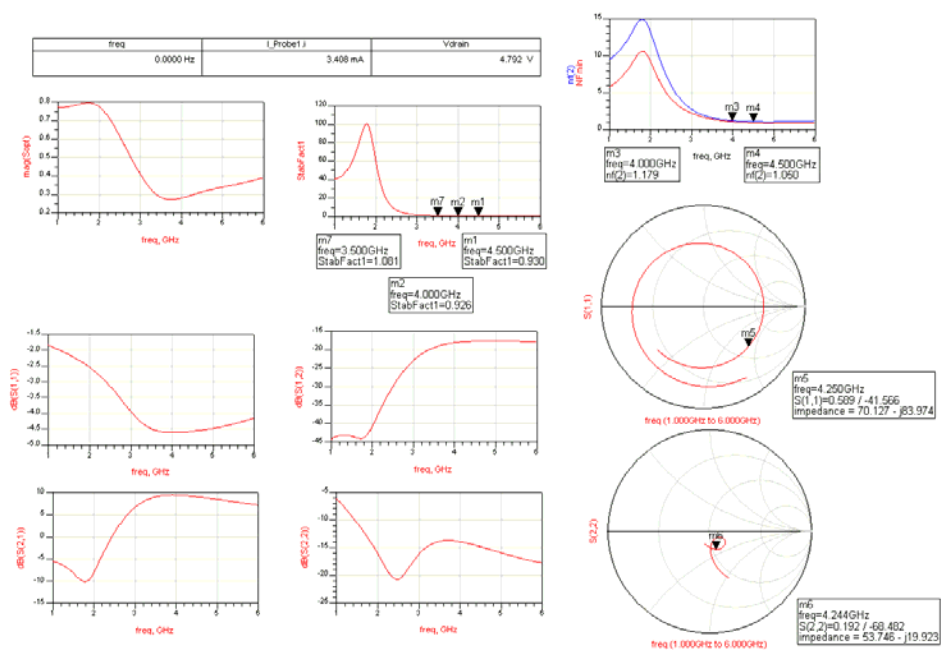Figure 7.40: Schematic of the LNA with 0.3 nH of source degeneration

Figure 7.41: Simulation results of the LNA with 0.3 nH source degeneration

7.3.3   The complete LNA

The complete LNA is simply made by cascading several single LNAs as explained previously in this document. This sub-section will describe its simulation results that will be very useful for the real design explained in the next section. This LNA is shown in Figure 7.42.
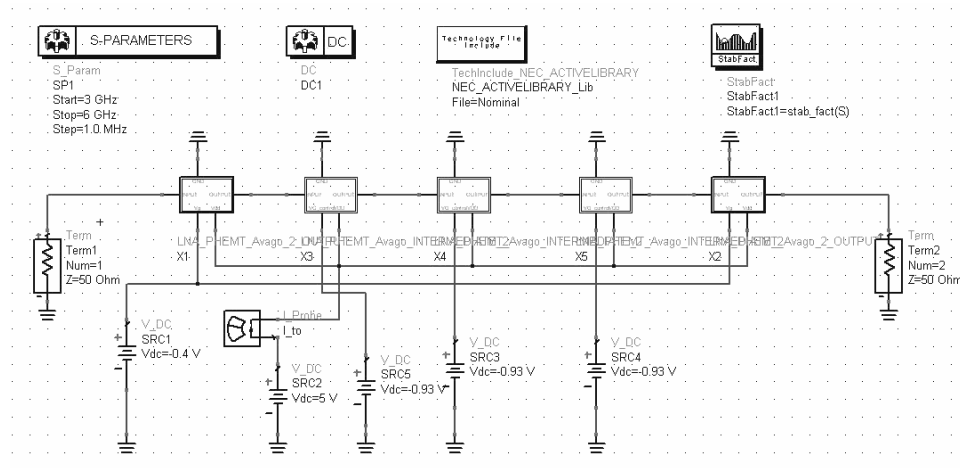
Figure 7.42: Schematic of the complete LNA

As for the bipolar LNA, the LNA described here is built with two input and output LNA made with a 1 nH source degeneration for insuring the stability and the impedance matching, while the intermediate LNA are made with a 0.2 nH source degeneration for insuring a high gain although there is a lower impedance matching and a closer instability. The input and output amplifiers have a fixed gain, while the intermediate amplifiers have an adjustable one. The reason for using 0.2 nH in place of 0.3 or 1 nH is the fact that when the LNA are cascaded, they interact with each other and thus the global behaviour of the whole circuit is not exactly the same as the combination of every LNA considered separately. In practice, things will be slightly different as explained further.

The detailed schematic of these LNA circuits are shown in Figures 7.43 and 7.44 for the input/output amplifiers and the intermediate amplifiers, respectively. It is important to notice that the capacitor that couples two successive stages was removed on the left of the intermediate amplifier because in the compound circuit it is connected directly to the previous stage; it avoids thus to have two capacitors in series that will probably change the simulation results.

The simulation results when the gain is maximum, i.e. when all gate voltages are set to
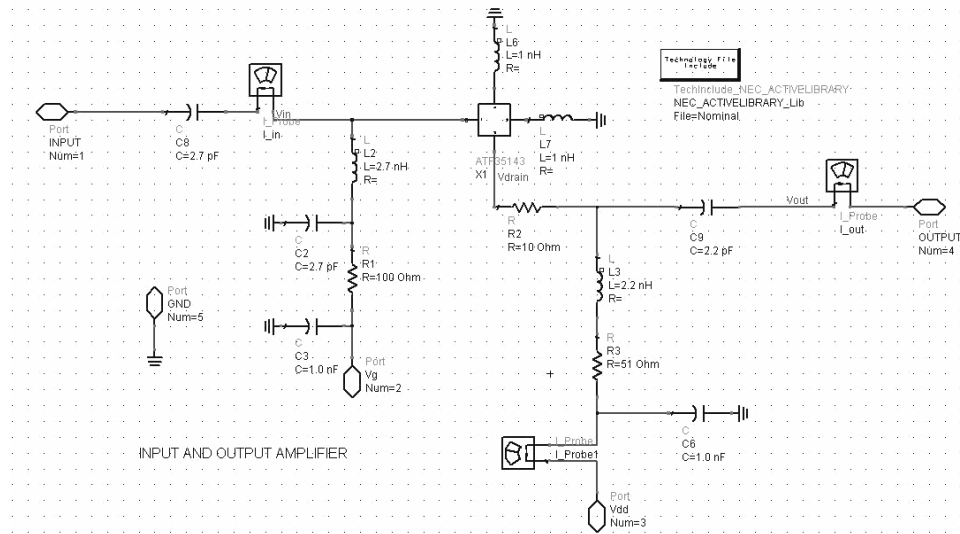
Figure 7.43: Detail of the input/output amplifier
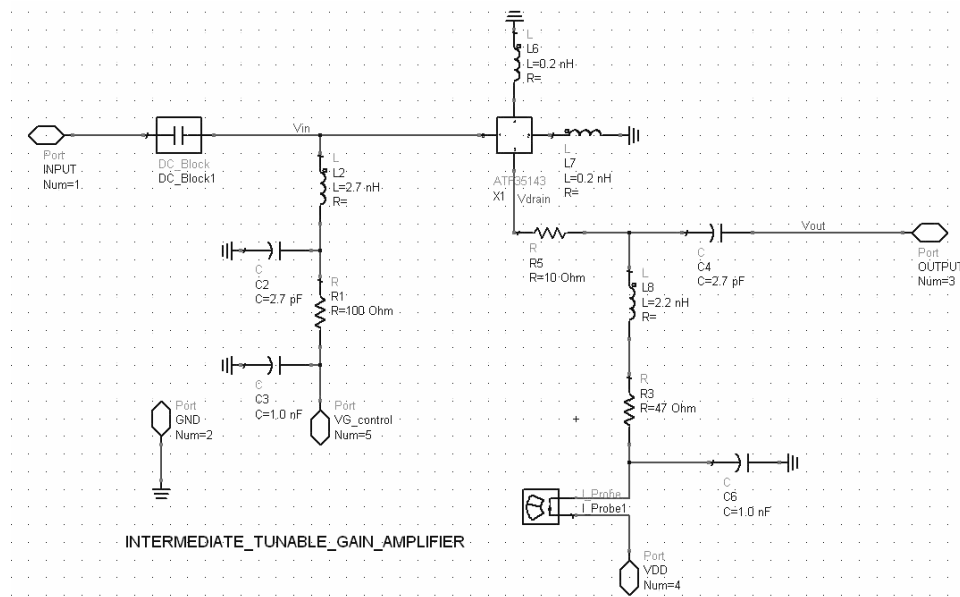
Figure 7.44: Detail of the intermediate amplifier

-0.2 volts as shown in Figure 7.45.

The gain reaches 55 dB in average and the input and output impedance matching is still out-standingly good. The noise figure lies near 0.9 dB that is very good for such an amplifier. The stability factor is so high that it needs some experimentation to see if there is any simulation artefact which gives such a value.
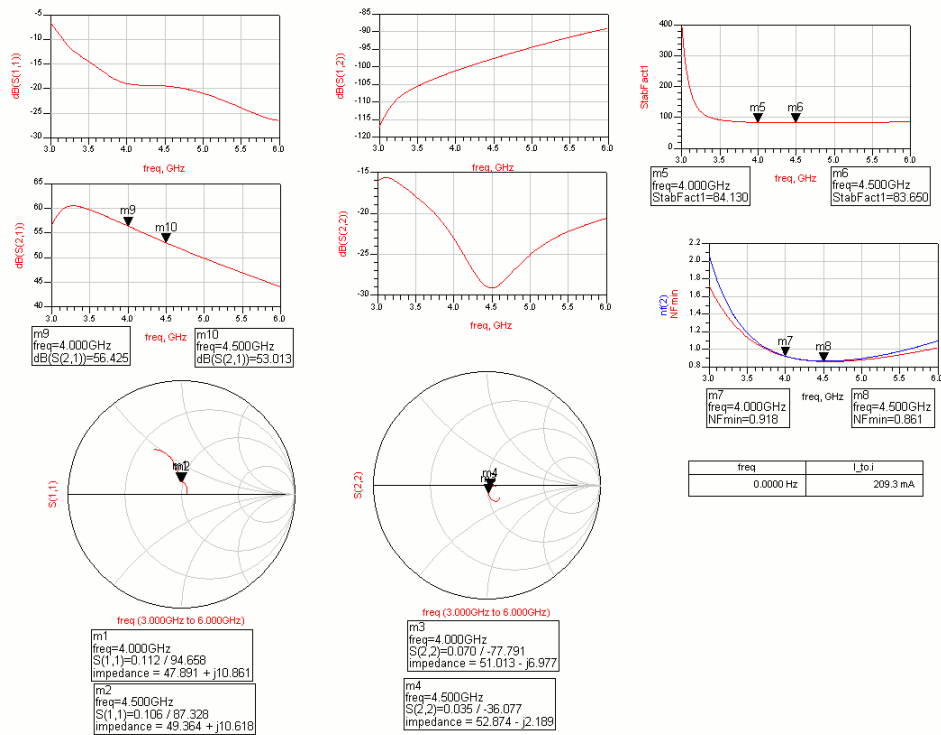
Figure 7.45: Simulation results of the complete LNA when the gain is maximum, i.e. all V_G are -0.2 volts

The same simulation is made but here with all gate voltage at -0.93 volts in order to see how the circuit behaves when it is "transparent" (see Figure 7.46). The input impedance matching is degraded and the noise figure increases greatly until 7 dB; however this is not so important because the circuit is made transparent only for strong signals that are quite insensitive to higher noise. The output impedance stays however in a good range.

In conclusion, the pHEMT transistor gives an excellent design for building an Ultra Wide-Band LNA with an adjustable gain. The next section will describe how it was made in practice.

Details on the LNA nº 1 prototype construction and schematics are given in Appendix D.1.
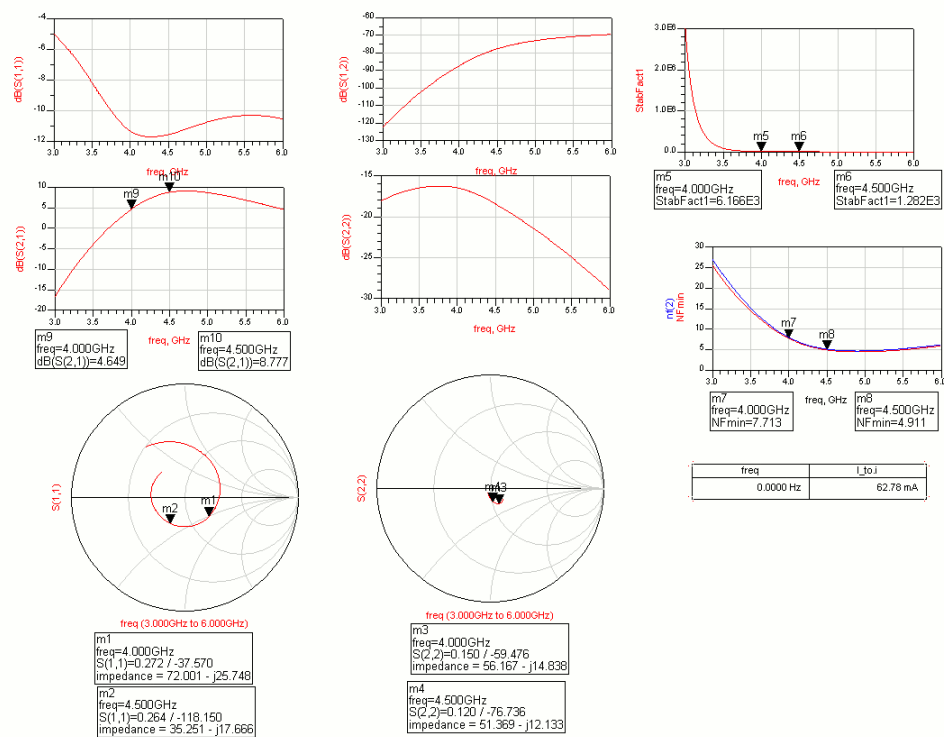
Figure 7.46: Simulation results of the complete LNA when the gain is almost 0, i.e. when all V_G are -0.93 volts

7.4   Measurements and improvements

The aim of this section is to show experimental results and measures, and to discuss the ways to improve the design and the realisation of the LNA. The results concerning the single LNA will be given first, these concerning the complete LNA will come next.

7.4.1   Single LNA

The following measurements will be made with the single LNA: the spectrum analysis, which will make possible the measure of the gain and of the 1 dB compression point. Then, the noise figure will be measured as the S-parameters and the current consumption.

Spectrum

The spectrum of the single LNA is shown in Figure 7.47 with an input signal at -60 dBm with a frequency spread of 7 GHz. This shows that the LNA does not oscillate and that the sine wave is correctly amplified.
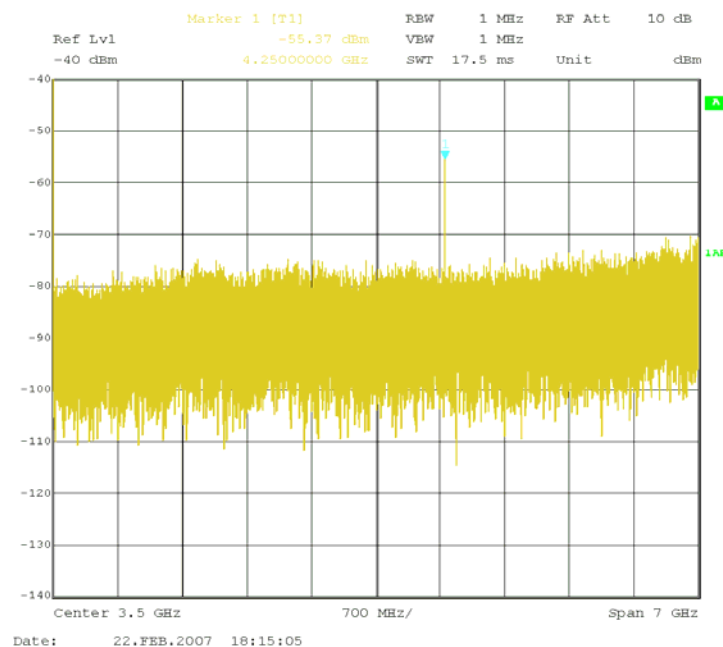
Figure 7.47: Spectrum of the single LNA with input signal at -60 dBm

Gain

The gain is obtained with a detail view of the spectrum that shows the power measured where the marker is positioned as shown in Figure 7.48. The gate voltage is -0.33 volts.
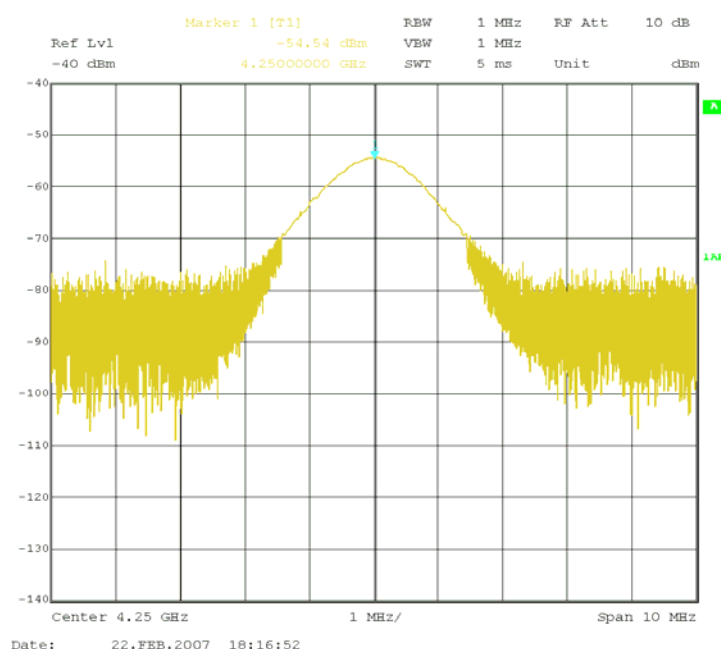
Figure 7.48: Detailed view on the amplified sine wave with the marker for measuring the gain

Since the input signal power is -60 dBm, the gain is 5.46 dB. It should be noted here that there is a loss of about 2 dB in the cables (measured by connecting a through connector) that were used for the measurement, so the gain can be estimated to be around 7.5 dB.

Compression Point (linearity)

The input compression point measures the linearity of the amplifier. It is obtained by increasing the power of the input signal until the gain decreases of one dB as shown in Figure 7.49. This happens for an input signal of -33 dBm.

Noise Figure

The noise figure was measured first with gate voltage that gives the minimum noise figure and secondly with the gate voltage that gives the maximum gain as shown in Figures 7.50 and 7.51.

This shows that the noise figure is 1.42 dB in the optimal case, where the simulated noise figure was 1.2 dB in the case of 0.3 nH source inductance. The gain is a bit higher here (6.5 dB) because other cables were used for the measurement.
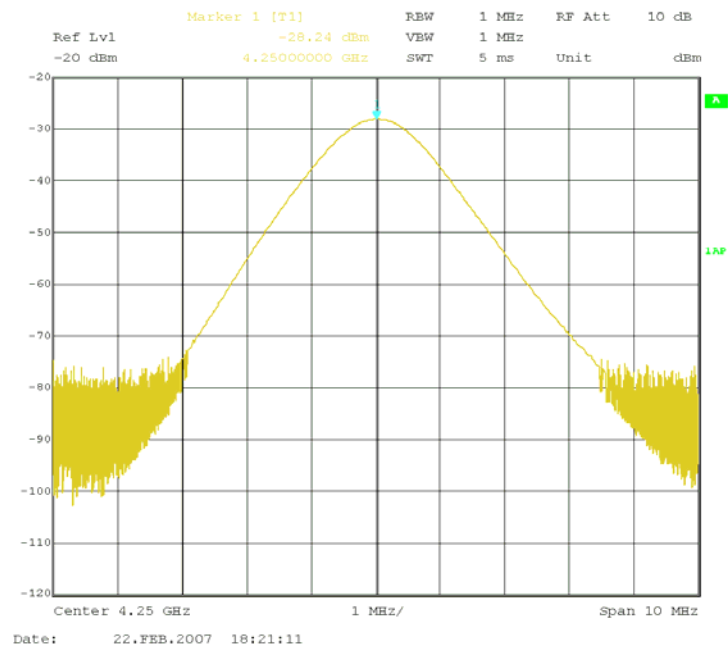
Figure 7.49: Output of the LNA at the compression point
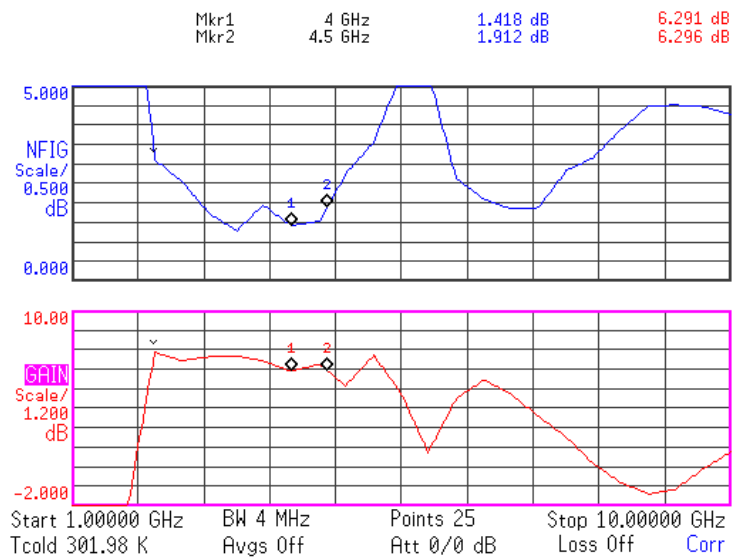
Figure 7.50: Noise figure and gain of the single LNA with minimal noise figure

S-parameters

The S-parameters of the single LNA are shown in Figures 7.52, 7.53, 7.54 and 7.55.

These measures show that the S_{11} is not so good as expected and need an improvement, the S_{12} is excellent, the S_{21} is in the range of expectations and last, the S_{22} needs an improvement. The impedance matching is not very good and need to be corrected. There are some
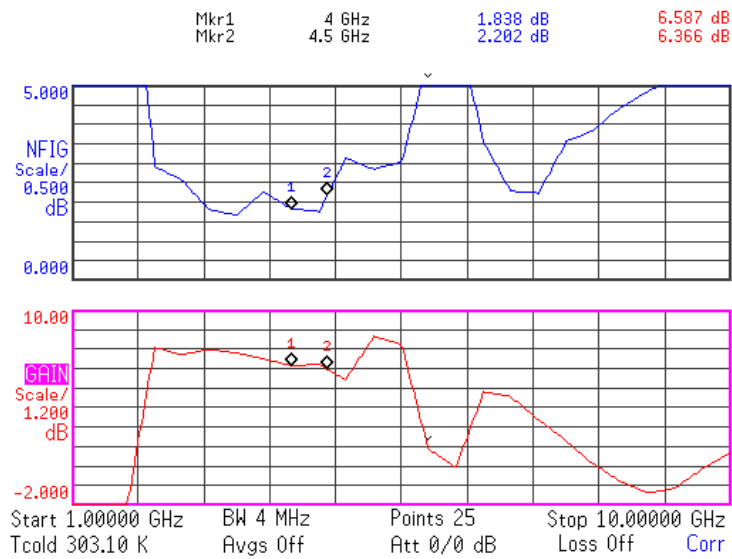
Figure 7.51: Noise figure and gain of the single LNAwith maximal gain
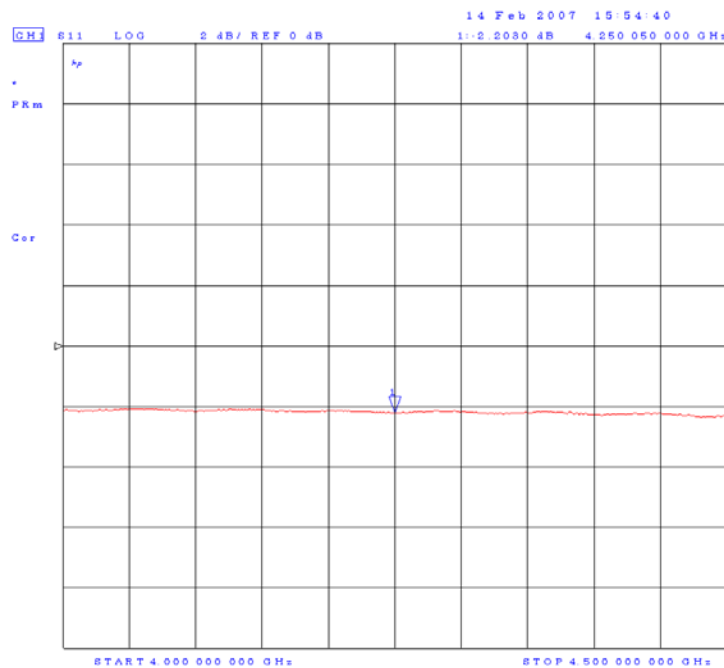
Figure 7.52: S_{11} of the single LNA

improvements that will be given further.

Current and power consumption

The current consumption was measured to 58.3 mA. As the power supply is 7 volts, the power is 400 mW. This is in the range of expectations.
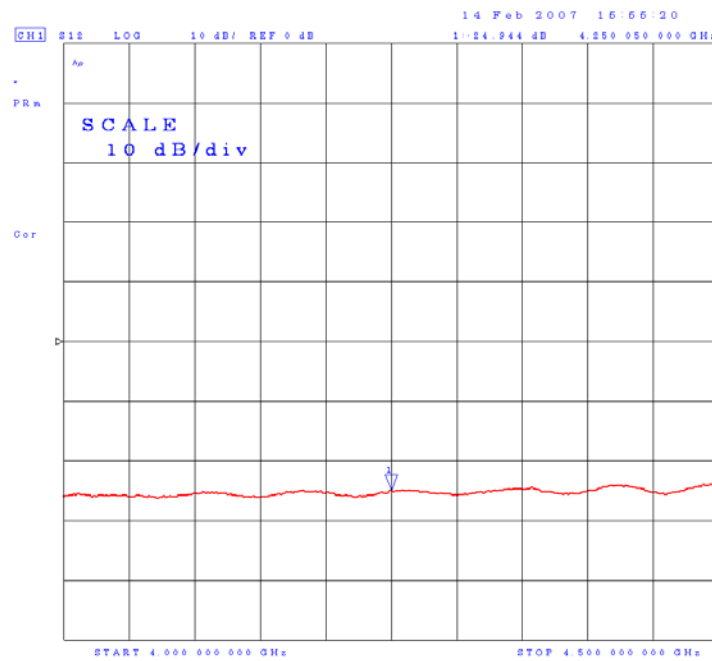
Figure 7.53: S_{12} of the single LNA
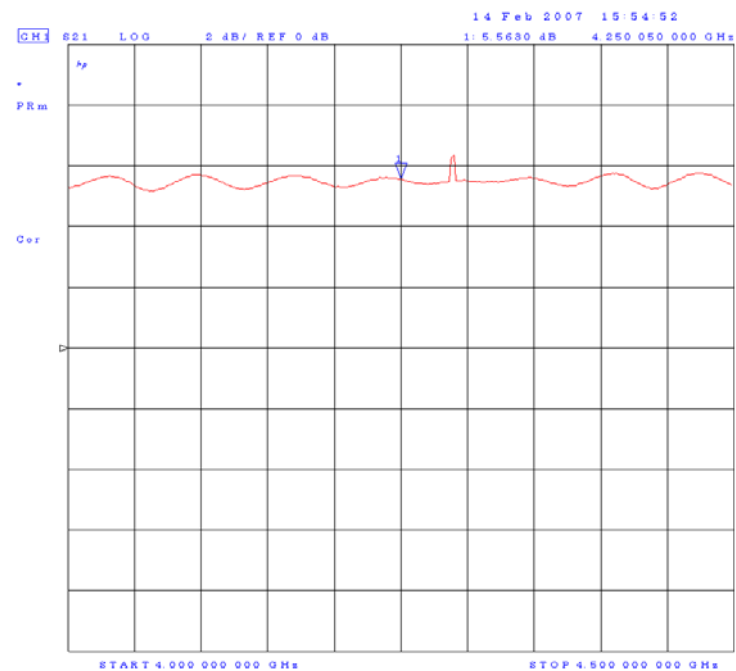
Figure 7.54: S_{21} of the single LNA
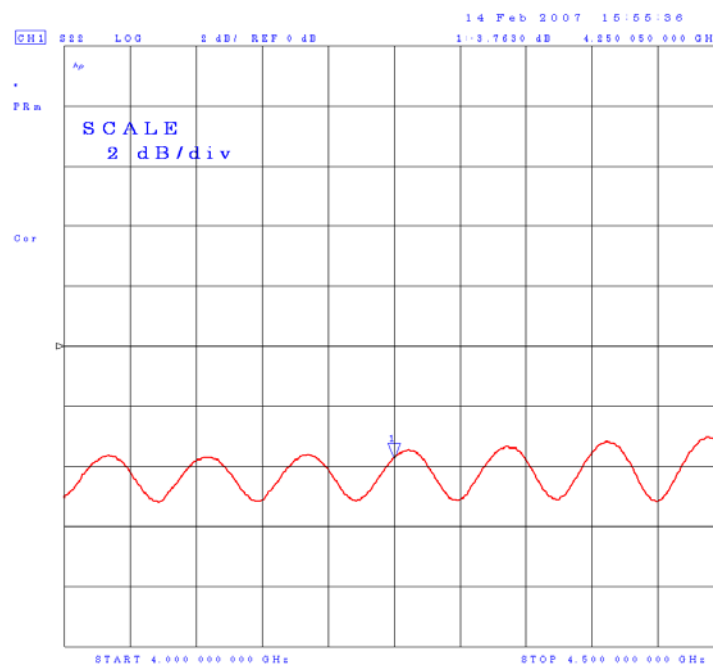
Figure 7.55: S_{22} of the single LNA

7.4.2 Complete LNA

This section describes the measurements made on the complete LNA. They are almost similar to those made on the single LNA.

Spectrum

The spectrum of the single LNA is shown in Figure 7.56 with an input signal at -60 dBm with a frequency spread of 7 GHz.
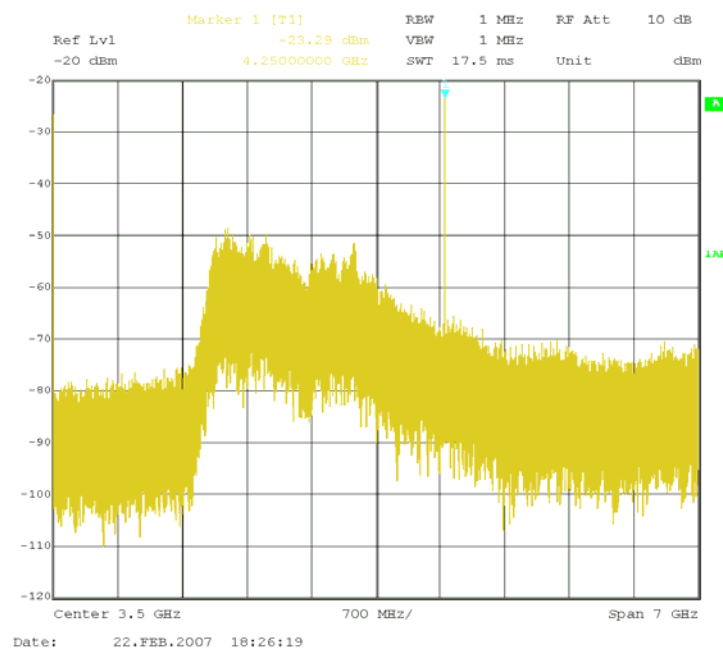
Figure 7.56: Spectrum of the complete LNA with input signal at -60 dBm

This spectrum shows that the complete LNA oscillates greatly in the 2 GHz and 3 GHz frequency range. However it does not avoid it to give a very fine gain in the frequency range of interest, as explained below.

Gain

The gain is given in Figure 7.57 which shows a closer view on the sine wave. Since the input signal power is -60 dBm, the gain is approximately equal to 37 dB, which reaches the expectations. It is interesting to see that even it oscillates, the LNA can achieve such a gain with only four single LNAs. The gate voltage is -0.31 volts.
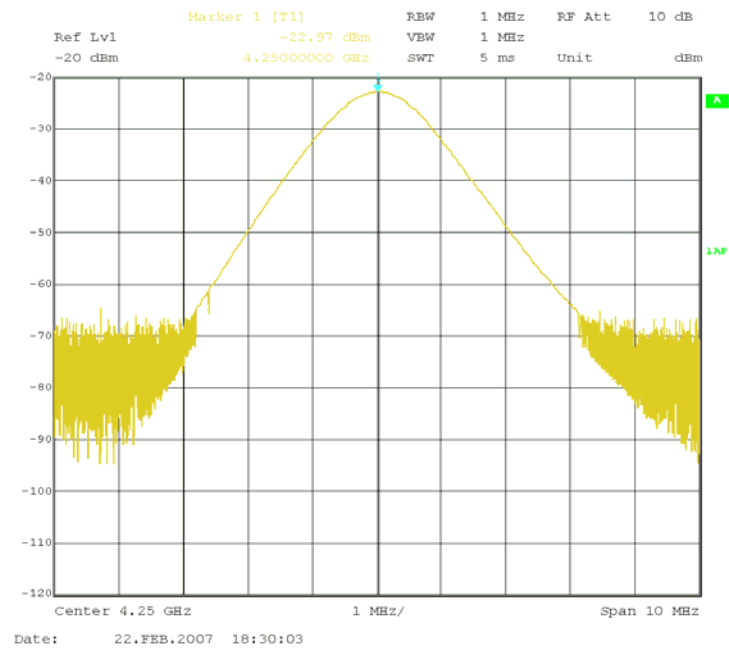
Figure 7.57: Detailed view on the amplified sine wave with the marker for measuring the gain

S-parameters

The S-parameters of the single LNA are shown in Figures 7.58, 7.59, 7.60 and 7.61.
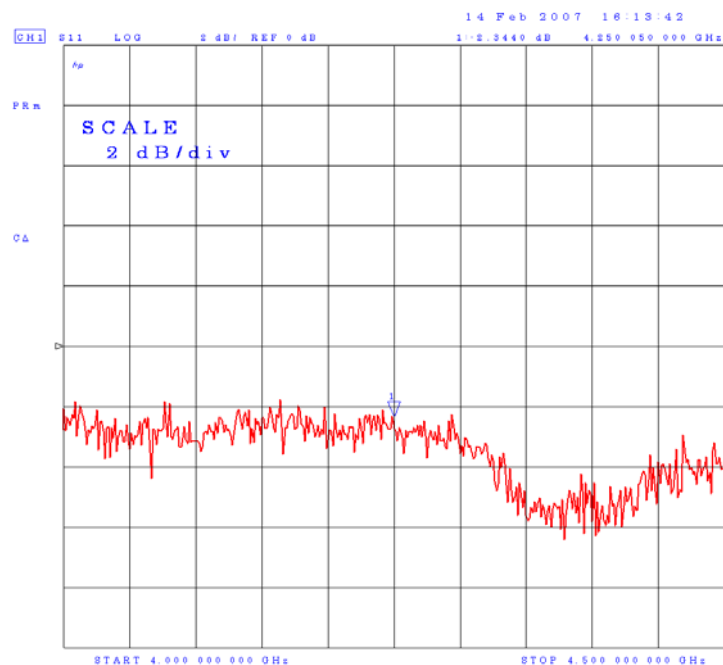
Figure 7.58: S_{11} of the complete LNA
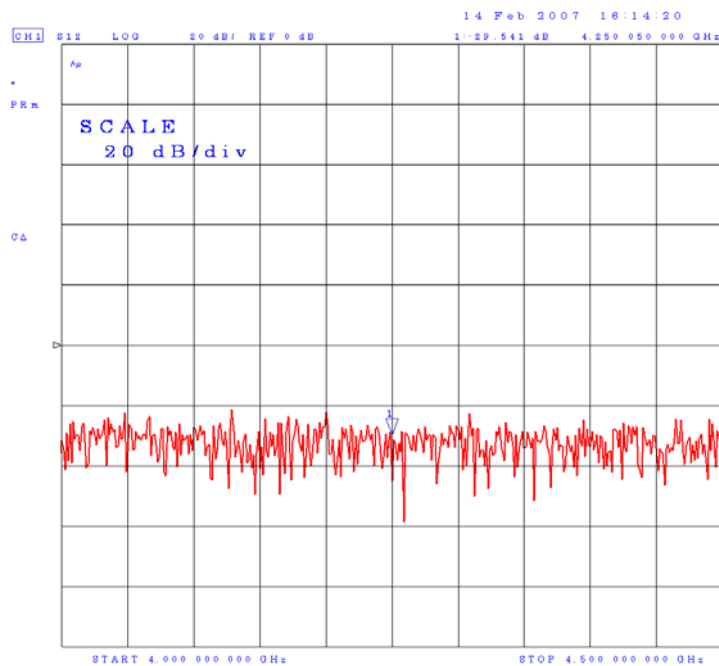
Figure 7.59: S_{12} of the complete LNA
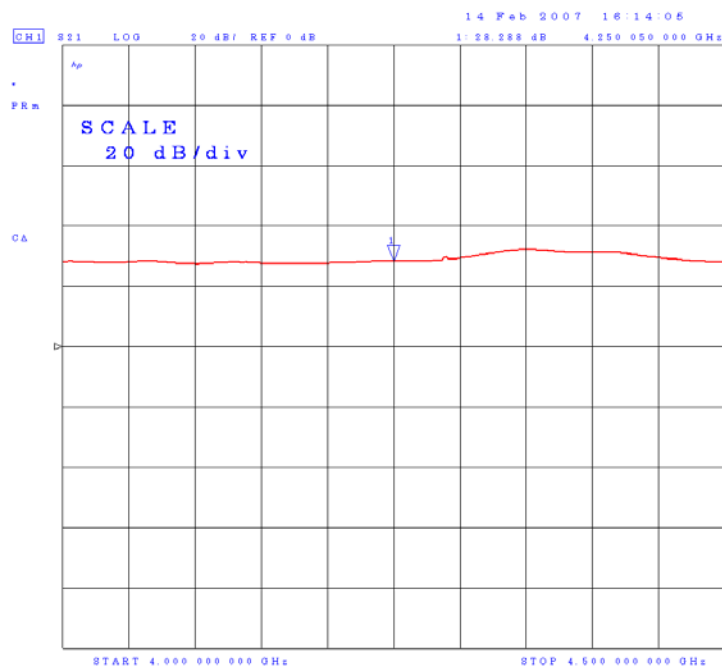
Figure 7.60: S_{21} of the complete LNA

The S_{11} parameter is very close to 1 and thus the circuit is near to be unstable. In fact, in the 2 GHz to 3 GHz frequency range, and because it is greater than one, so it explains why there are oscillations. These measures are not shown here because it is complicated to save results from
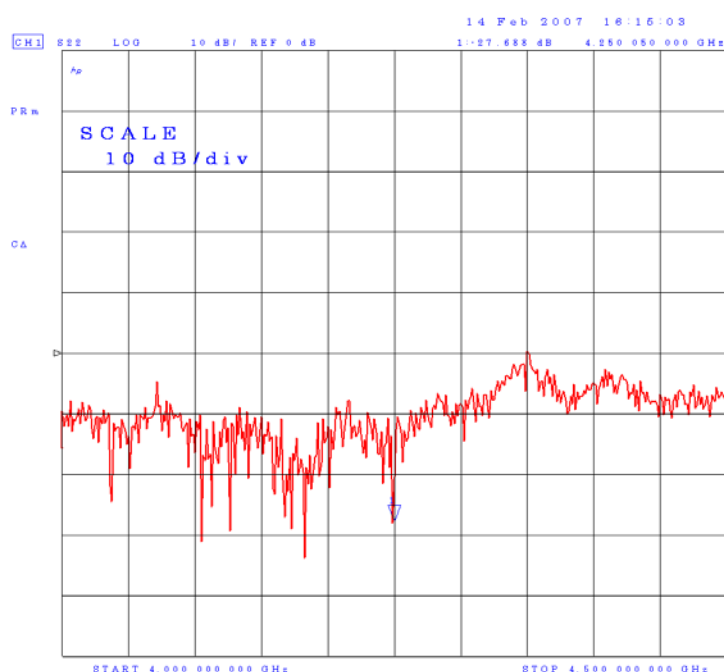
Figure 7.61: S_{22} of the complete LNA

the network analyser and it takes a long time that was not available at the end of this project. However, there are some possible improvements of the LNA behaviour. The other parameters are as expected; the S_{22} can however be also improved in order to give a good circuit.

Compression Point (linearity)

The input compression point happens for an input signal of -28 dBm as shown in Figure 7.62. The gain is 37 dB so the compression point happens when it is 36 dB. This measure should be made with care because the output power is near the upper power limit of the transistor which is 14 dBm and it is easy here to reach this point and to destroy the transistor.

Current and power consumption

The current consumption was measured to 115.8 mA. As the power supply is 7 volts, the power is 810 mW. This is in the range of expectations.

7.4.3   Improvements

The single and complete LNA circuits give good results in terms of amplification; however they still have some drawbacks that need to be improved in order to have a correct amplifier,
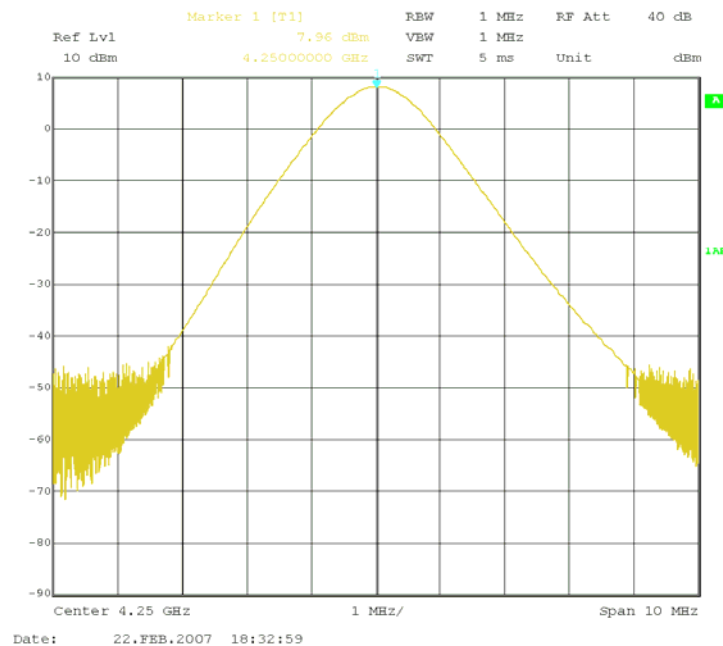
Figure 7.62: Compression point of the complete LNA

especially concerning the impedance matching and the stability. This section will give some possible approaches for improving the design for the future.

- First of all, the source inductance should be modified in order to be closer to 1 nH and not 0.33 nH as made previously. It was initially believed that 0.33 nH would give better results according to some simulations and experimentations with the single LNA. We correct the source inductance value; they are both set to approximately 0.82 nH (after further optimisation) by increasing the microstrip inductance length to 50 mils instead of 30 mils.

- The shielding quality can be greatly improved by enclosing all the circuit in a box without any slot and not only some parts as it was done previously. We build a completely closed shielding of the whole circuit; the shielding is made with beryllium copper instead of FR-4 PCB material.

- Lastly, there are some tracks on the circuit that could be redrawn in order to better decouple the power supply. For example, some capacitors can be made closer to the line to decouple (see Figure D.11). We re-design some tracks and re-arrange some components on the PCB; we also shrink the design in order to avoid too long tracks between two consecutive single LNA cells.

By improving the LNA, we can see and discuss whether these improvements are helpful for reducing or eliminating the parasitic oscillations of the circuit or not. These improvements of the construction of LNA prototype n° 1 are described in Appendix D.2.

7.5   Conclusion

This new design of the complete LNA shows no fundamental improvement on the previous one. However, it is sure now that the shielding and the source inductance were not responsible of the remaining oscillations. The main way to improve the design at this point would be to tune manually the value of the components, especially the coupling capacitors at input, output and between stages, but this would be tedious and the improvement is not guaranted. Although the presence of some oscillations, the LNA shows a very good behaviour in the frequency range of interest and the gain is easy to adjust without introducing any artefact or other oscillations. In addition, a band-pass filter will stop any parasitic oscillation allowing thus a good performance of the UWB reception that will be enough for the purpose of the experimental testbed that was already made.

According to these results, we believe that the single LNA is a very good candidate for a LNA stage but another stage is required for having more power and, eventually, a controlled gain. However, the tuning voltage V_g on the grid that was first intended for gain control would be a very interesting feature to keep but for impedance matching of the input of the LNA in order to have a very good matching with the antenna (which could not be exactly 50Ω) and thus to prevent power loss.

LNA prototype n° 2

8.1 Introduction

This chapter presents the LNA designed for the testbed with a voltage-controlled gain. According to Chapter 7, it is almost not possible to design on one stage a LNA that has a low noise figure, both input and output matched, a variable gain and which is stable. However, Chapter 7 shows a single LNA circuit that has a low noise figure and an adjustable input impedance, which is of high interest in a system where input signal power is extremely low (remember that with UWB signals, the received power is lower than with narrow-band signals).

The challenge here is to design a circuit that implements the remaining functionalities we targeted in chapter 7: a high and voltage-controlled gain. We decided to implement the LNA in this way when we discovered the document shown in Appendix J that relates the possibility to do variable gain by changing a DC voltage on the MMIC amplifier MGA-86576 from Avago (formerly Hewlett-Packard). This document was the *deus ex machina* element we needed to build our LNA because it is impossible to find it anywhere and there is no other clue that let suppose that this MMIC has the possibility to change its gain by applying a voltage on its input.

The UWB LNA described here is a fundamental part of the U-Lite testbed and is described in an article [38]. As this circuit is specially intended for communication research community, we focus on simplicity and availability of required components rather than pure technologic performance. As with other parts of the testbed, the objective is to make it simple and to avoid the need for the high-level background and technical infrastructure required in IC design.

In order to make our testbed reproducible at reasonable costs, we chose to build it with off-the-shelf discrete components with no specific constraints on the power consumption but with performance that are close to those of integrated circuit design, as done in [58] for example. Thanks to its generic architecture, it is easy to modify the transmitter in order to work in another frequency band or with a wider bandwidth, depending on the needs of the users.

8.2   Architecture of the UWB LNA

The UWB LNA is based on three parts, as shown in Figure 8.1. The first part is the LNA that is extensively described in Chapter 7 and which is based on a pHEMT (pseudo High Electron Mobility Transistor), a transistor technology that allows for very high speed signal amplification with low noise. The voltage *Vtune1* is used to finely match the input of the circuit at 50Ω (*Vtune1* becomes the new name of V_G). The second part is a UWB band-pass filter that selects only the band of interest (here form 4.0 GHz to 4.5 GHz). The last part is the power amplification with the variable gain feature (by using the voltage *Vtune2*). The combination of these three parts leads to the device we called *UWB LNA* in this work. The input UWB signal is obtained from an omnidirectional antenna (not described in this work but in [41]) that has a 50Ω impedance.
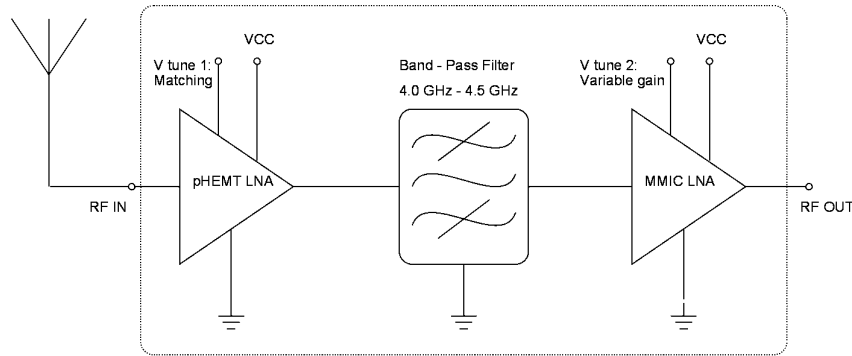
Figure 8.1: *Overview of the LNA circuit*

8.3   Schematic of the UWB LNA

8.3.1   The pHEMT LNA Input Stage

The schematic of the pHEMT LNA stage is based around the transistor ATF-35143, as shown in Figure 8.2 and as explained in Chapter 7. Between the first prototype of LNA circuit shown

in Figure D.1 and the new one we present here in Figure 8.2, we perform additional simulations in order to improve the performance and optimize the inductance value for source degeneration. The circuit presented here is the final one as we used in our publications. The transistor is used in a common source configuration with an inductive degeneration; this allows low-noise amplification by avoiding the presence of too many resistors. The circuit is supplied with a 7-volt source through a network of two 68Ω resistors and 100nF and 1nF capacitors for decoupling. The 1.6nH inductor and 22pF capacitor are used not only for RF and DC decoupling respectively, but also for noise and impedance matching. The 10Ω resistor is used for insuring the stability of the circuit with the cost of a small decrease of the gain. The left part of the circuit is similar, with the same constraints. Because the input current is negligible, the resistors value can be higher ($1k\Omega$) and the effect of the filtering network is increased in order to avoid cross-coupling between input and output, and thus parasitic oscillations. The inductor is also a bit higher at 1.8 nH. All components value are obtained by iterating simulations that use complete models for all components and for PCB material. The part of the circuit that requires much care is the inductive degeneration. The value of the inductors (one for both source pins of the transistor) should lie between 0.3 to 1 nH (higher, the gain vanishes, lower, the circuit oscillates) and ideally be 0.5 nH. As it is hard to obtain a precise value of discrete inductance at so high frequency, the inductive degeneration is made with PCB microstrip lines. The line dimensions are given by the following formulas [59]:

$$Z_0 \text{ (Ohm)} = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \cdot \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$$t_{pd} \text{ (s/m)} = 3.33661417 \cdot 10^{-9} \cdot \sqrt{0.475 \cdot \varepsilon_r + 0.67}$$

$$C_0 \text{ (F/m)} = \frac{t_{pd}}{Z_0} = \frac{2.64322140 \cdot 10^{-11} \cdot (\varepsilon_r + 1.41)}{\ln\left(\frac{5.98h}{0.8w + t}\right)}$$

$$L_0 \text{ (H/m)} = C_0 \cdot Z_0{}^2$$

$$L \text{ (H)} = L_0 \cdot l$$

where

$$l = 8.13 \cdot 10^{-4}\text{m}$$
$$w = 1.27 \cdot 10^{-4}\text{m}$$
$$h = 5.08 \cdot 10^{-4}\text{m}$$
$$t = 35\mu\text{m} = 3.5 \cdot 10^{-5}\text{m}$$
$$\varepsilon_r = 3.38$$

Since our PCB workshop has a resolution of 120μm, this value is assigned to the width of the microstrip line and the other values are given by the PCB material (RO4003C); the length is then determined by iteration. By calculating the inductance L with these formulas gives 0.50443 nH for both source inductances.
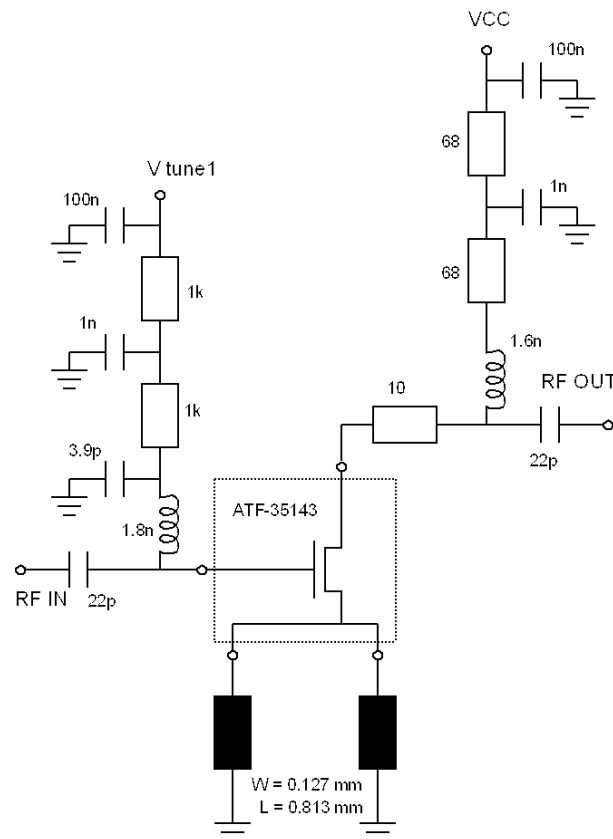
Figure 8.2: *The schematic of the pHEMT LNA input stage*
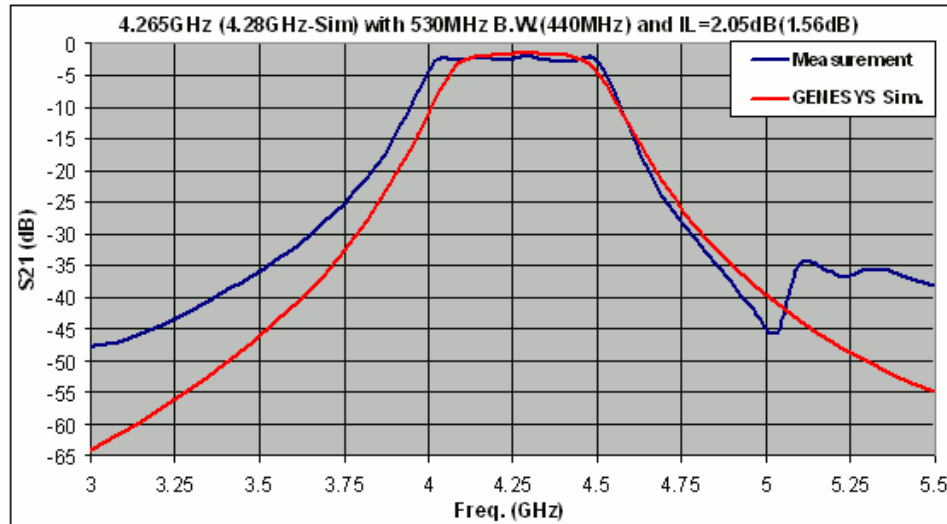
Figure 8.3: *The transfer function of the UWB filter. The red line is the theoretic curve and the blue one is the measured characteristic response.*

8.3.2   The UWB Band-Pass Filter

The band-pass filter is an interdigital filter of the 4th order with cutting frequency boundaries at 4.0 GHz and 4.5 GHz. The transfer function of the filter is shown in Figure 8.3, where the red line is the theoretic response expected from the filter and the blue line is the real response measured from the filter. The filter is designed by our colleague Mr. Altug Oz by using the Agilent GENESYS tool for both RF characterisation and PCB generation. The software generates directly the Gerber files for the PCB manufacture (see Figure 8.4).
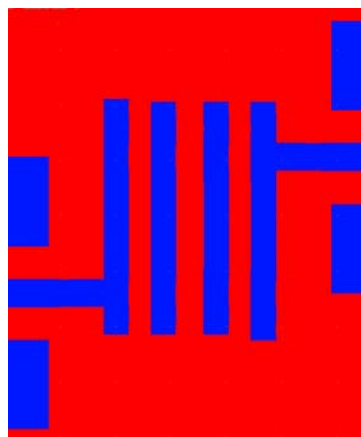
Figure 8.4: *The layout of the band-pass filter generated by the Agilent GENESYS software*

8.3.3 The Variable-Gain Output Power-Stage

The schematic of the variable-gain output power-stage is based around the MMIC MGA-86576 as shown in Figure 8.5. The MMIC is a very common circuit in RF design, but here it is used in a specific way for varying the gain. The gain of the MMIC can be changed by applying a small DC voltage to the input of the MMIC through a high Z microstrip line and a $7.5k\Omega$ resistor (see Appendix J for more details). The gain is nominal - i.e. about 23 dB - when there is no voltage, and it decreases when the voltage becomes positive. Conversely, when a negative voltage is applied to the MMIC's input, the gain increases about 2.7 dB at -93 mV, and then it decreases. The schematic of the variable-gain output stage is straightforward, as shown in Figure 8.5. The main feature of this circuit is the microstrip lines that are used to reject the RF signal from the DC voltage supplies. The idea is to design a quarter wavelength transmission line that ends with another badly matched line (the two big squares in our case, see Figure 8.5). The design of these lines is described in [23] with the following formulas by assuming an average frequency of 4.25 GHz :

$$\varepsilon_{RE} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{1 + \frac{10h}{w}}} - \frac{(\varepsilon_r - 1)t}{4.6h\sqrt{\frac{w}{h}}}$$

$$L = \frac{c_0}{4f_0\sqrt{\varepsilon_{RE}}}$$

where (PCB variables are the same as above)

$$w = 2.54 \cdot 10^{-4} \text{ m}$$

$$f_0 = 4.25 \text{ GHz}$$

$$c_0 = 2.99792485 \cdot 10^8 \text{ m/s}$$

The length is thus $l = 11.4$ mm and the dissipated power in the microstrip line is $P = 54\mu\text{W}$, so the track will easily support the current without blowing. Note that the size of the two squares is not critical as long as it is much wider than the width of the microstrip line. Contrary to the pHEMT inductance, the width is chosen at 0.254 mm because it is a relatively long line and it is more difficult to insure a regular shape with a 0.12 mm width. The remaining components are classic architecture for RF coupling and MMIC biasing and decoupling.
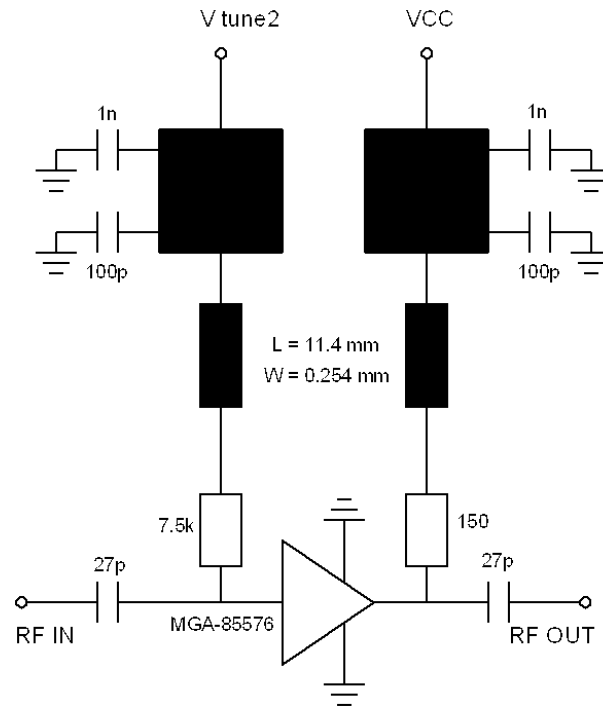
Figure 8.5: *The schematic of the variable-gain output stage*

8.4   Construction of the UWB LNA

The LNA is made in Duroid RO4003C, which is better suited than FR4 for high frequency designs; the thickness of the copper is $35\mu m$ after etching and gold plating. Although a good design of the transmission lines and ground planes reduces significantly the radiated power of the circuit, the PCB should be packaged into a metal case with a screwed cover in order to completely shield the device from external interference while preventing oscillations by decoupling the internal elements. It is important to use many vias in order to connect both top and bottom ground planes with the least amount of parasitic inductance, especially near high frequency signals. The circuit is gold-plated by electro-chemical means, in order to avoid corrosion of the copper that rapidly degrades the performance. When components are soldered, the circuit is placed in the aluminium case and glued with a conductive glue (with silver) and placed into an oven for polymerisation for 3 hours at $70°$ C. The connection between the UWB Transmitter and the outside world is made with SMA connectors for RF signals and through DC filters that are screwed into the shielding case for DC power supply and tuning voltages. The resulting circuit is shown in Figure 8.6. The PCB layout of the LNA and of the power amplifier are shown in Figure 8.7 with the component reference on the footprint for easier mounting.

More detailed explanations on how to build the LNA are given in Appendix C.
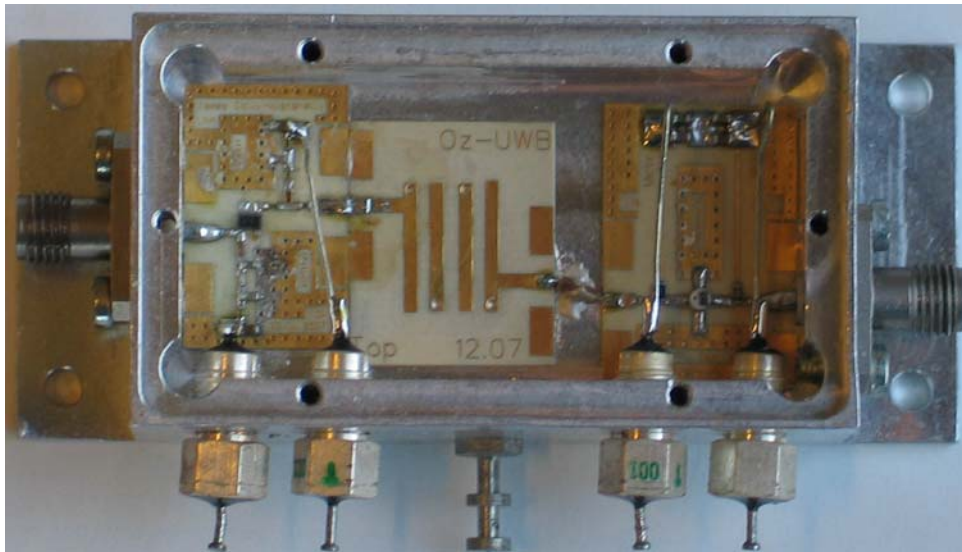
Figure 8.6: *The circuit of the variable-gain UWB LNA*
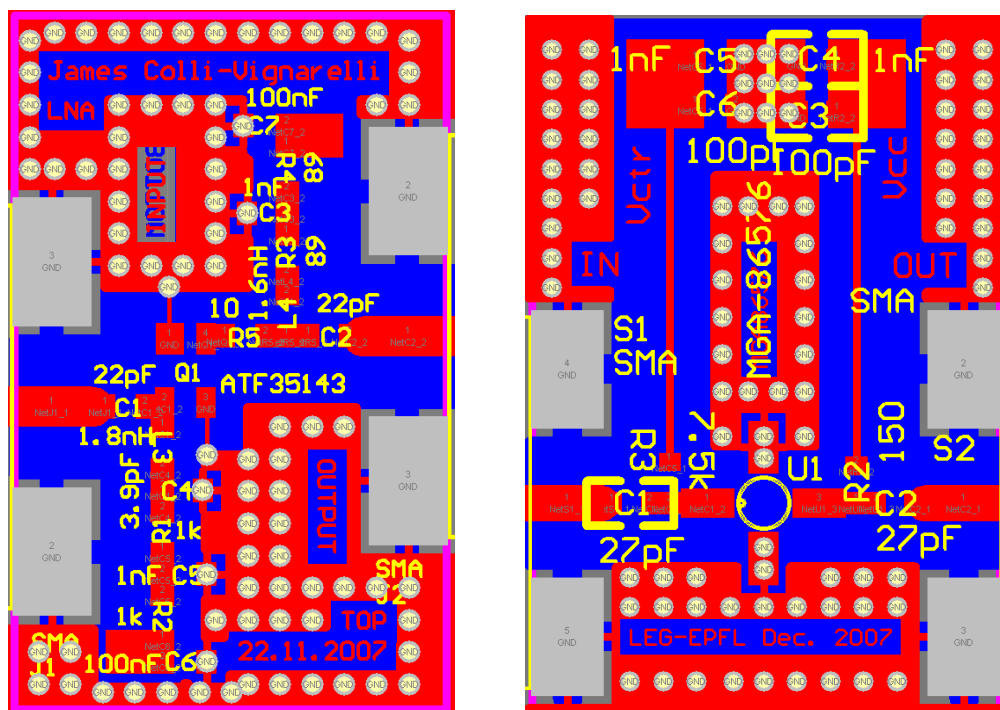
Figure 8.7: *The PCB layout of the variable-gain UWB LNA: The PCB on the left is the one for the LNA and the PCB on the right is the one for the power amplifier with voltage-controlled gain.*

8.5   Measurement on the UWB LNA

The power supply voltage is 7 volts for both circuits (the input LNA stage and the output power stage). During the noise analysis the calibration automatically removes the loss of the cables; however, in the case the 1 dB compression point measurement, the loss of cables was measured at 2.0 dB by using a through connector.

8.5.1   The pHEMT LNA Input Stage

The noise analysis of the pHEMT stage is shown in Figure 8.8. At 4.25 GHz, the gain is 8.821 dB and the noise figure is 1.108 dB which is a very good value (red and blue curve respectively). The 1 dB compression point is at +6.6 dBm and the current consumption is 15.9 mA.
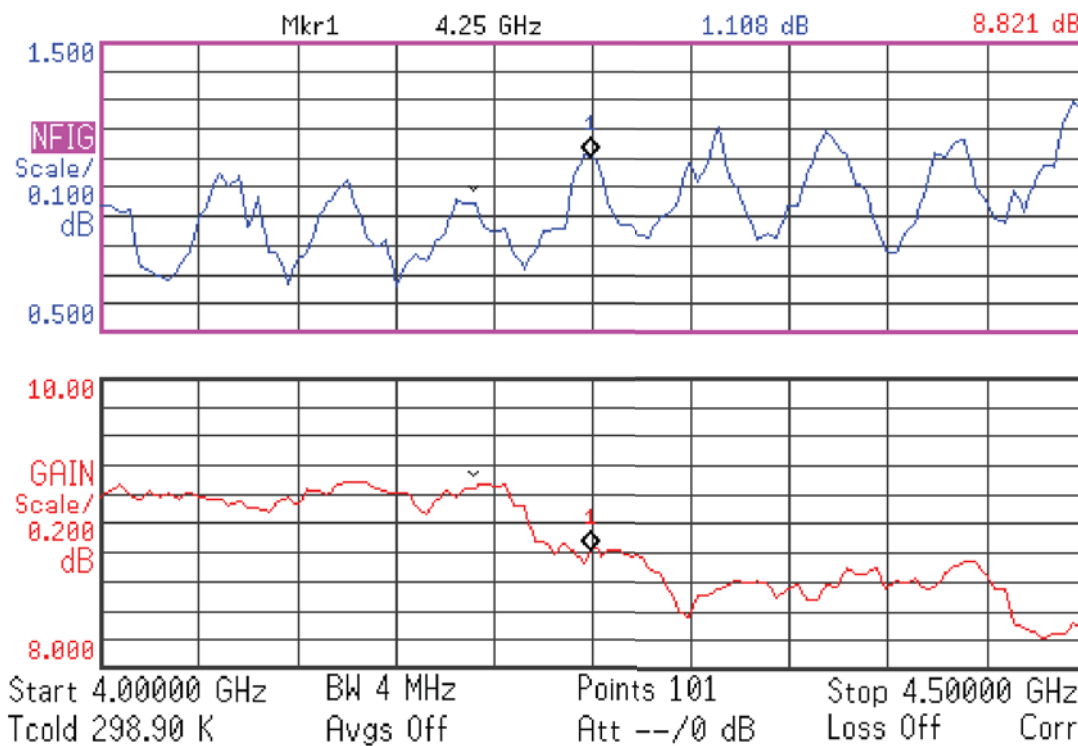
Figure 8.8: *The noise analysis of the input pHEMT stage.*

8.5.2   The UWB Band-Pass Filter

The measurement is already done in Figure 8.3 (blue curve).

8.5.3   The Variable-Gain Output Power-Stage

The noise analysis of the variable gain output stage is shown in Figure 8.9. At 4.25 GHz, the gain is 25.677 dB and the noise figure is 2.788 dB. The 1 dB compression point is at +6.0 dBm and the current consumption is 13.7 mA.
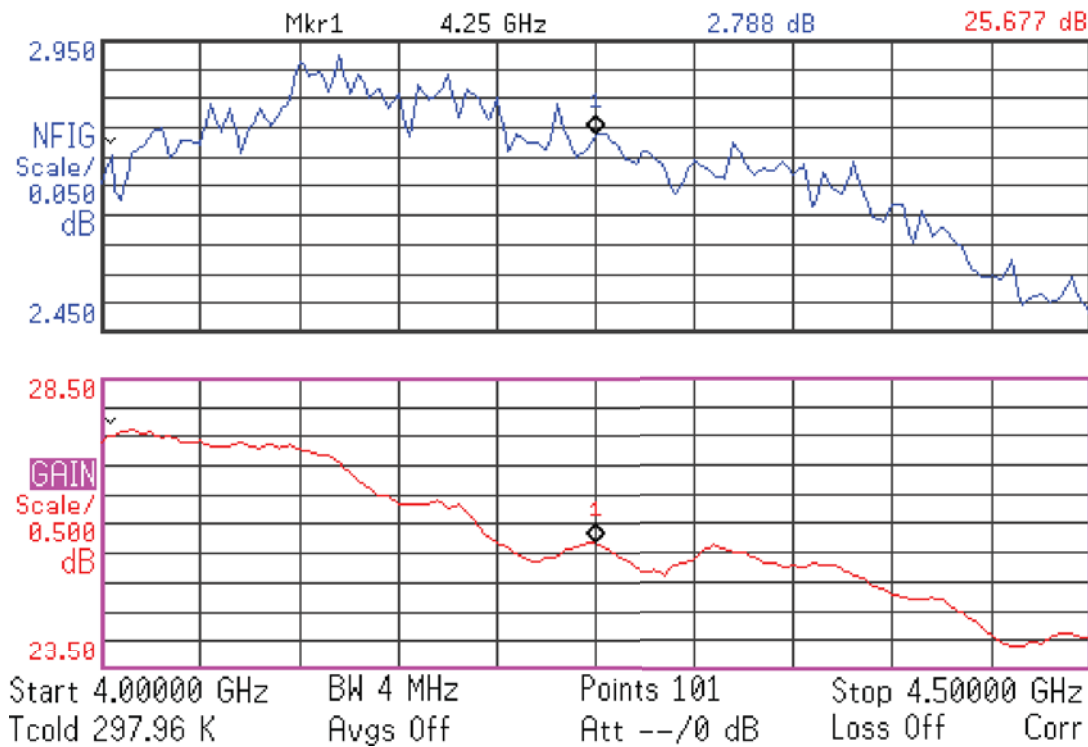
Figure 8.9: *The noise analysis of the output MMIC stage with maximum gain.*

8.5.4   The Whole Chain of the UWB LNA with Variable Gain

The noise analysis of the whole UWB LNA chain is shown in Figure 8.10. At 4.25 GHz, the gain is 29.864 dB and the noise figure is 2.223 dB. The 1 dB compression point is at +3.3 dBm and the current and power consumptions are 29.6 mA and 210 mW respectively. All these results are summarized in Table 8.1. In addition, the LNA supports high input-signal power (up to 0 dBm) that makes it easy to cascade two devices as done in [26] in order to have 60 dB of gain or even more.
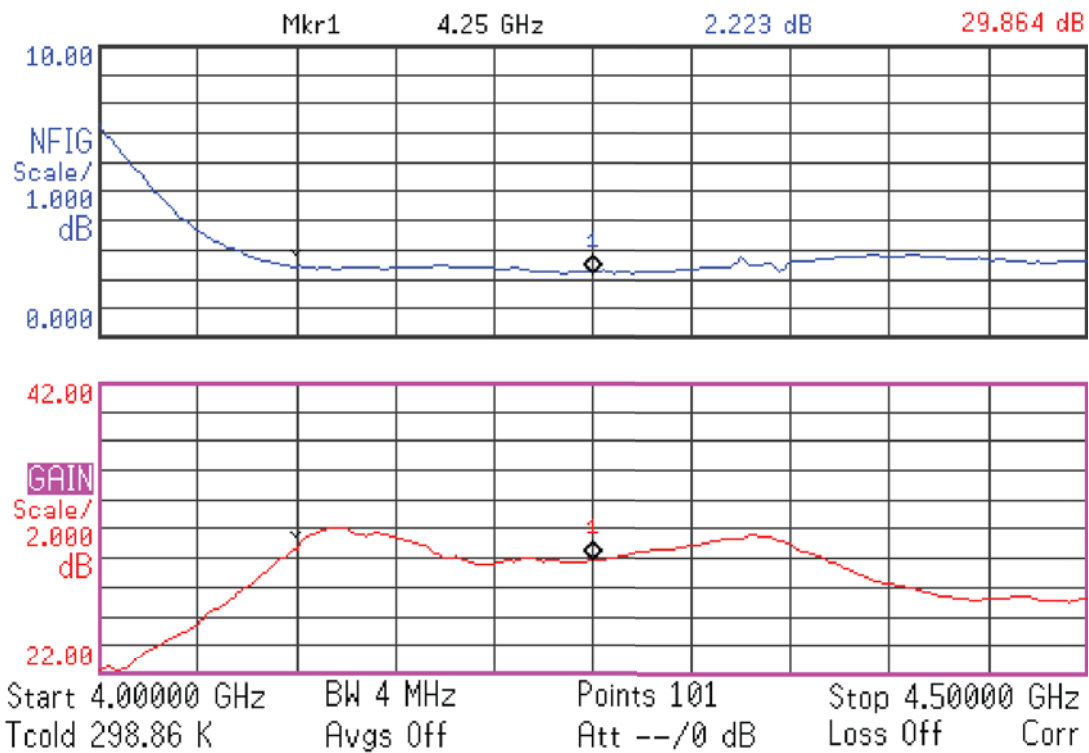
Figure 8.10: *The noise analysis of the complete chain LNA (pHEMT + filter + MMIC) with maximum gain.*

Measurement	pHEMT stage	MMIC stage	complete LNA
1dB CP	+6.6 dBm	+6.0 dBm	+3.3 dBm
Current	15.9 mA	13.7 mA	29.6 mA
$f = 4.0$ GHz :			
Gain	9.2 dB	27.4 dB	22.5 dB
Noise Figure	0.93 dB	2.73 dB	7.0 dB
$f = 4.25$ GHz :			
Gain	8.821 dB	25.677 dB	29.864 dB
Noise Figure	1.108 dB	2.788 dB	2.223 dB
$f = 4.5$ GHz :			
Gain	8.3 dB	24.0 dB	27.5 dB
Noise Figure	1.128 dB	2.48 dB	2.7 dB

Table 8.1: Summary of the UWB LNA measurements results.

8.6   Conclusion

We have developed a IR-UWB LNA that achieves high gain with very low noise figure on the bandwidth of interest. The gain can be adjusted by applying a voltage that comes from a DAC (Digital to analog converter) driven by the FPGA for automatic gain control. The power consumption is acceptable considering the LNA is intended to be used for measuring and testing purposes - as done in [26] for example - and not for mobile low-power applications. The results of the RF measurements and the experimental demonstration of the IR-UWB LNA completely fulfils the expectations and even goes beyond them when we consider publications made on the same subject but with integrated circuits like [60] (with respect to the achieved gain), [61] (with respect to the achieved noise figure), and [62] (with respect to both the achieved gain and noise figure). We thus completely achieve our initial target.

Chapter 9

I/Q Demodulator

9.1   Introduction

This chapter presents the I/Q demodulator used for the receiver part of the UWB testbed. This demodulator was designed by the author and built by Ms Angélique Umuhire in 2010 during her Master Diploma project under the supervision of the author. It was presented at PRIME Conference in the article [39] and the article [63] presents its importance for a good detection accuracy of the pulse positions.

This UWB demodulator is an important part of the testbed because it has to amplify the UWB signal and to down-convert it in a lower frequency band in order to be acquired and processed by digital means at a reasonable cost. In a sense, the I/Q demodulator does exactly the reciprocal of the UWB transmitter in terms of signal processing. The first approach is to amplify the received UWB signal and to down-convert it by using a conventional mixer driven by the local oscillator described in Chapter 5, as shown in Figure 9.1. This is, in fact exactly what was done in Chapter 2 with the SRD pulser as UWB transmitter. We will see later in this chapter that because transmissions are asynchronous, the demodulator needs a more sophisticated architecture with an I/Q mixer to work properly but the principle remains the same. To the best of our knowledge, using an I/Q mixer for frequency down-converting an UWB signal as made here was never made before and this I/Q demodulator is a novel and original architecture of UWB receiver.
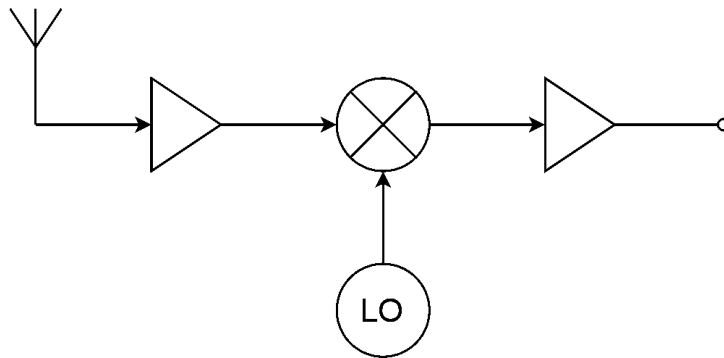
Figure 9.1: The naive approach for UWB demodulation

9.1.1 Frequency down-conversion

The demodulator performs a frequency down-conversion by using a mixer. The down-conversion is required because the cost of fast analog to digital converter is very high in the giga-hertz range and we are only interested in the energy of the UWB impulse and not its exact shape. We already explained in Section 2.3.1 how the down- or up-conversion process works. In its conventional form, the mixer is a passive nonlinear circuit that multiplies two input signals as shown for example in Figures 9.1. The drawback of using a conventional mixer is that the phase is lost. For preventing that, I/Q mixers can be used (see Figure 9.2). An I/Q mixer contains two conventional mixers where one is directly driven by the local oscillator while the other is driven by the local oscillator that is phase-shifted by $90\,°$. Mixing simultaneously signals with an In-phase and a Quadrature reference sine wave (LO) preserve the phase information by representing it with a complex vector. I/Q mixers are thus used in the field of complex modulation (like PSK and QPSK for example); the reader can refer to the book [64] for more information. I/Q mixers has four ports: the Local Oscillator (LO) port and the Radio Frequency (RF) port as in conventional mixers, and the I (In-phase) and Q (Quadrature) ports that both correspond to the IF port in conventional mixers. RF and I/Q can be used either as input or output depending the mixer is used for up- or down-conversion. In this chapter, the oscillator is the same as the one described in Chapter 5.

9.1.2 The importance of I/Q demodulation in our Testbed

As Impulse-Radio UWB transmissions are asynchronous and carrierless, there is a small frequency drift between the local oscillators of the transmitter and the receiver because it is im-
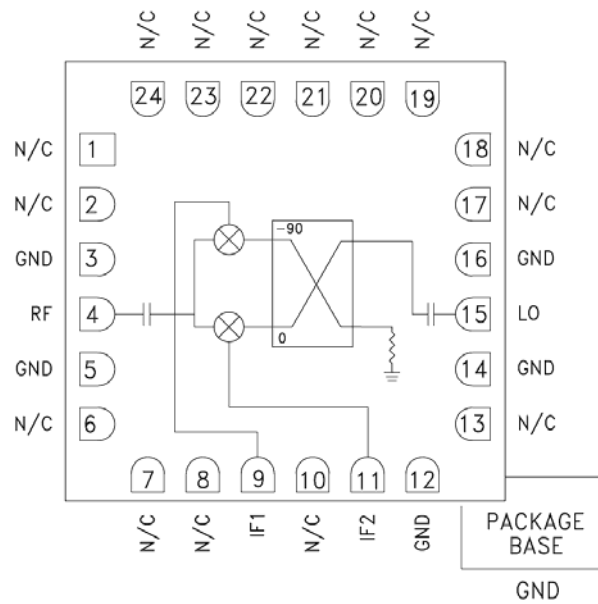
Figure 9.2: The principle of an I/Q mixer (here the HMC620: I and Q are labelled IF1 and IF2).

possible to perfectly synchronise two remote oscillators. When using a conventional mixer for down-conversion as shown in Figure 9.1, this frequency drift produces a beat in the down-converted baseband signal that has a disastrous effect on data integrity and synchronisation algorithm (they do not work at all, see [26]). Figure 9.4(a) shows by simulation the effect of this beat on the baseband signal but in practice, the result is exactly the same. During frequency down-conversion, there are three scenarios that can occur. The first one (Figure 9.3(a)) is the ideal case where both oscillators are perfectly synchronised (frequency and phase); in this scenario, a conventional mixer works perfectly because the phasor of the obtained baseband signal is collinear with the I axis and remains steady. This case happens in practice very rarely and never remains stable long enough to be useful. The second scenario (Figure 9.3(b)) is the case where the oscillators are synchronised in frequency but not in phase. In this scenario, a conventional mixer would work correctly provided that both oscillators are not too much out of phase as we have nothing if they are in quadrature (90 $^\circ$ phase shift). The third scenario (Figure 9.3(c)) is the case when there is a frequency drift between the oscillators; this is the scenario seen in practice. In this scenario, the frequency drift produces a beat that makes the UWB down-converted impulses have an envelope that distort the signal when a conventional mixer is used. This envelope corresponds mathematically to the magnitude of the projection of the rotating phasor on one axis (here I for example). The I/Q demodulator is required to extract the quadrature component Q in addition to the in-phase one in order to preserve the power of the
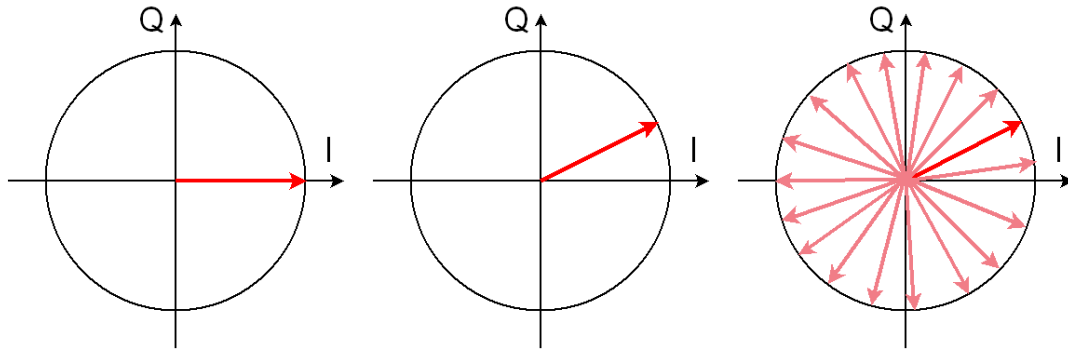
(a) Scenario A: The local os-
cillators of the transmitter and
the receiver are perfectly in
phase; the phasor vector re-
mains steadily aligned with I
axis.   This is an ideal sce-
nario that is obviously not real-
istic in IR-UWB asynchronous
transmission.

(b) Scenario B: The local oscil-
lators of the transmitter and re-
ceiver are synchronised in fre-
quency but not in phase; the
phasor vector remains steady
and has a non-zero projection
component on the I axis be-
cause of the phase shift. This
scenario is not realistic in IR-
UWB asynchronous transmis-
sion.

(c) Scenario C: The local oscil-
lators of the transmitter and the
receiver have approximately the
same working frequency. The
phase error is continuously in-
creasing but the total energy of
the signal is preserved. This is
a realistic scenario in IR-UWB
asynchronous transmission.

Figure 9.3: The three scenarios that occur when the local oscillators of the transmitter and the
receiver are used for UWB generation and down-conversion.

signal and remove the beat. Taking the I and Q components, squaring both of them and adding
them together in order to have the magnitude of the phasor ensures that the average power is
constant, without having any beat (see Figure 9.4(b)).
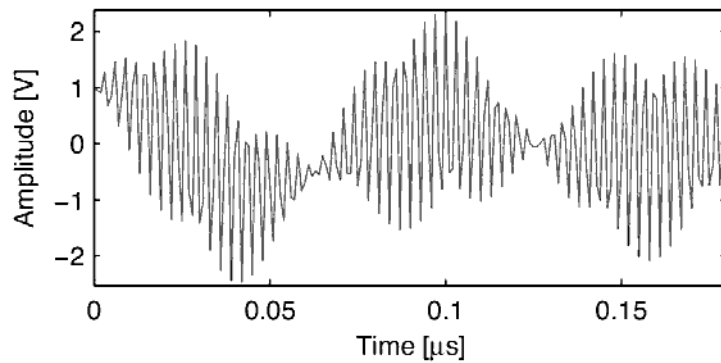
(a) Down-conversion of UWB impulses without I/Q demodulation (signal obtained by simulation that is similar to signals obtained in practice)
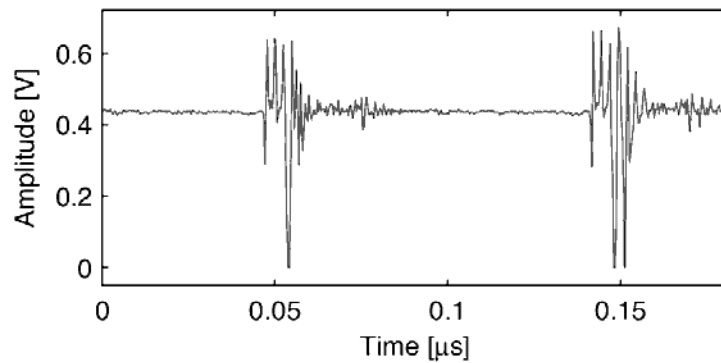
(b) Down-conversion of UWB impulses with I/Q demodulation (signal obtained by acquisition of real UWB data)

Figure 9.4: *The difference between conventional and I/Q demodulation on UWB signal down-conversion.* The envelope in a is produced by the projection of the phasor on the I axis; this phasor represents the phase shift between the oscillators and is characterised by the phase noise of these two oscillators. We notice that the SNR is much better with I/Q demodulation

9.2   I/Q demodulator architecture

This section describes the architecture used to design the I/Q demodulator. The market search of the circuits we use is presented in Appendix F. The off-the-shelf or passive-based circuits we use are the following:

- One I/Q mixer, **HMC620LC4** from Hittite technology;

- Two conventional mixers **ADE-R2ASK+** from Minicircuits;

- Two amplifiers devices, **MAR-1+** and **MAR-8ASM+** from Minicircuits;

- One local oscillator (LO) (presented in Chapter 5);

- Two power-splitter circuits designed by using normalized resistances (see Appendix E for details);

- Two cross attenuator pads designed by using normalized resistances (see Appendix E for details);

- A power combiner designed by using normalized resistances (see Appendix E for details).

In Figure 9.6, the circuit receives a signal from the transmitter (Point 1), with a frequency range from 4.0 to 4.5 GHz. The signal is sent to the I/Q mixer (HMC620LC4) that receives also a signal from the local oscillator (at 4.25 GHz). The I/Q mixer gives the two signal components I and Q. Both of them are amplified by the MAR-8ASM+ amplifier, after which (Point 2) they are split by a power splitter. This is done in the order to be able to square the amplitude of the signal later on. A fraction of the signal is attenuated through the attenuator cross pad (Box 3). Finally, the mixers ADE-R2ASK+ receive the signals from the power splitters and the attenuator pad. The two signals from the mixers are then combined by a power combiner (Box 4) before being amplified again and sent to the FPGA board (Point 5). The estimated budget link of the I/Q demodulator is given in Table 9.1.

Examples	1 (*)	2
Input power [dBm] (Point 1)	-11.000	-16.000
I/Q output [dBm]	-18.500	-23.500
Output amplifier [dBm] (Point 2)	-13.000	8.000

Output mixer [dBm]	-5.000	-10.000
Power combiner output [dBm]	-10.700	-15.700
Amplifier output [dBm] (Point 5)	6.800	-1.800

Table 9.1: Example: Estimated budget-link of the I/Q demodulator. (*): level used in the real circuit.

The architecture of the I/Q demodulator was validated first by using off-the-shelf RF modules (amplifiers, mixers and attenuators); it is this system that is described briefly in the article [26] where the U-Lite testbed is presented for the first time. In this chapter, we intend to build a complete and embedded design of this I/Q demodulator.
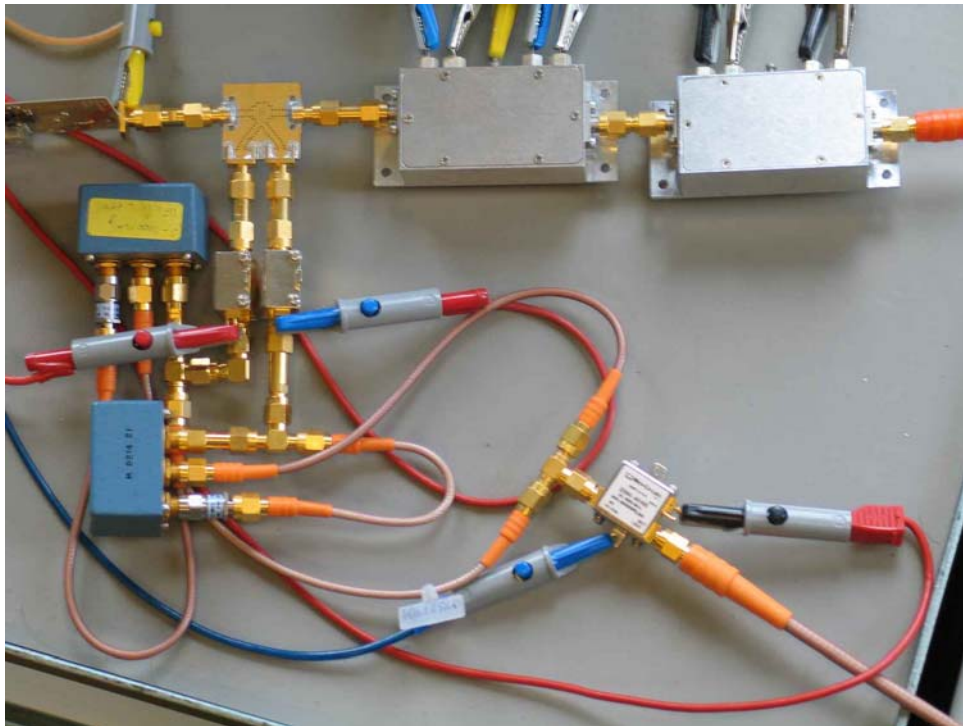
Figure 9.5: The original I/Q demodulator made with off-the-shelf RF modules (we see two LNAs on the top)

Because the components of the I/Q demodulator we present here are not the same as the original ones we used in Figure 9.5, we need to reconsider the design from the beginning and to replace the function of the RF modules by discrete-component versions of them. The two kinds of elements that need further investigation for replacement are power splitter/combiner and cross-pad attenuator (see Appendix E for a complete study of these passive RF architectures).
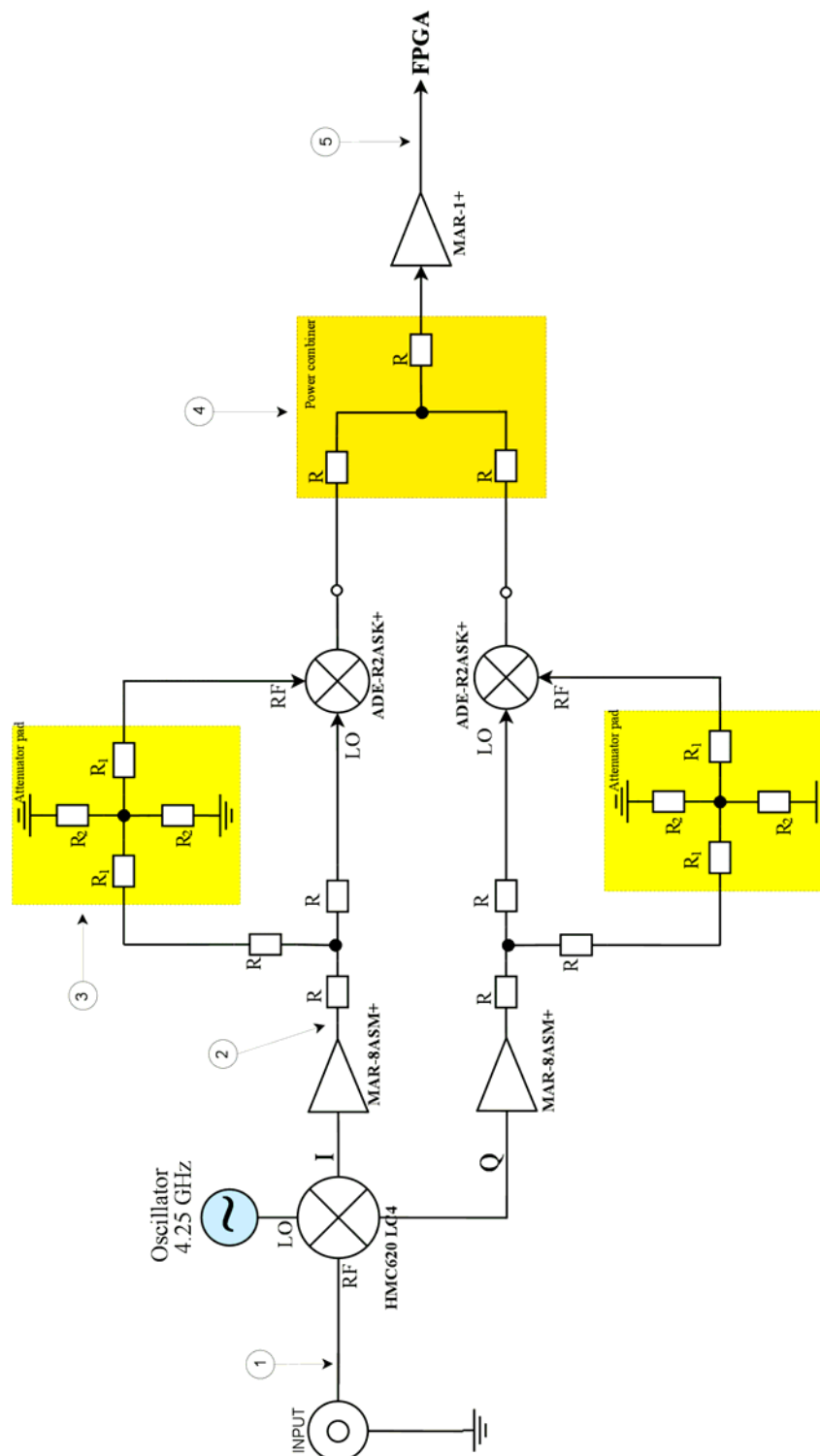
Figure 9.6: The architecture of the I/Q demodulator

9.3   Schematic of the receiver

The schematic of the I/Q demodulator is made of five parts (see Figure 9.7) :

- I/Q mixer;

- amplifiers;

- conventional mixer for squaring the signal;

- resistive networks;

- general purpose passive elements

This section presents the detail on the how the I/Q demodulator is designed with the calculation of the resistive networks. The main part of the circuit is the I/Q mixer. The I and Q components obtained from the mixer are amplified with two Monolithic Microwave Integrated Circuit (MMIC) amplifiers by about 30 dB. Decoupling capacitors are required because of the high frequency and high power of the RF signals. The inductor is used to feed the amplifier without RF leakage; the resistor is used to decrease the quality factor of the inductor because of the wide bandwidth of the signals. The I and Q signals are then squared by using a conventional mixer that is fed with the same signal on its RF and LO inputs.

9.3.1   The I/Q mixer

The I/Q mixer receives the UWB signal that lies in a frequency range from 4.0 GHz to 4.5 GHz. Its local oscillator port is connected to a PLL synthesizer that generates a sine wave at 4.25 GHz. The I/Q mixer we choose (see Appendix F) is the HMC620LC4. Both I and Q signals from the I/Q mixer are amplified before being squared.

9.3.2   Amplifiers

We need three amplifiers: two for the I and Q components and one for the output. As the I/Q mixer has a conversion loss of typically 7.5 dB, an amplifier is required for increasing the level of the signal from the I/Q mixer. Therefore the MAR-8ASM+ amplifier (with a gain of 31.5 dB) is chosen. The signal from the power combiner also needs to be amplified, because the power combiner has a conversion loss (attenuation) of 6 dB (see thereafter). For this, a MAR-1+ amplifier with a gain of typically 17.8 dB is chosen. The power supply of these amplifiers is described thereatfer.
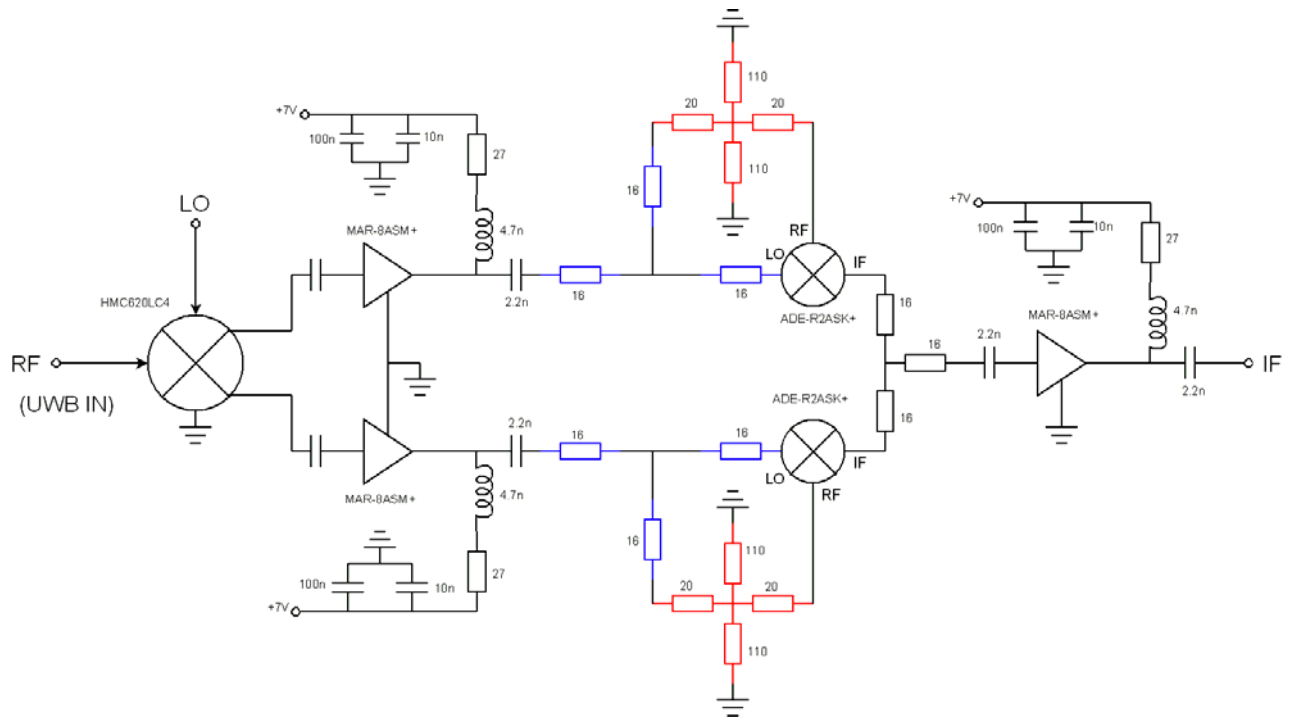
Figure 9.7: *The complete schematic of the UWB I/Q receiver.* The left part is the I/Q mixer with its incoming RF and LO signals. The I and Q components given by the mixer are amplified by about 20 dB and then are squared by using a simple mixer fed with the same signal on its own RF and LO inputs. An RF power splitter is used in order to have the signal available for both inputs of the mixer with impedance matching; in order to respect the power supported by the RF input of the mixer, this part of the signal is attenuated by using an attenuating pad. Finally, the two components are added by using a power combiner (the same network as the power splitter) in order to have the magnitude of the baseband signal; this signal is amplified once again and sent to the acquisition board.

9.3.3 The squaring circuit

The squaring circuit is formed by a mixer that multiplies the signal with itself in order to obtain the square of the signal. The mixer has two input ports: LO and RF. The signal from the amplifier MAR-8ASM+ passes through a power splitter for duplicating the incoming signal by preserving the impedance matching. One path goes directly into the mixer and the other path passes through an attenuator before entering the mixer in order to reduce the power level on this input. As the level of the signal that can be supported by the LO input port has to be smaller or equal to 7 dBm, there is a need of an attenuator too.

9.3.4 Resistive network

Several types of resistive networks are used in the circuit. They are made only of resistances and can implement several functions like power splitter, power combiner and attenuator. The power splitter and power combiner are in fact only one network, the splitting and combining function depends only on the direction of the flow of power. The networks are presented in detail in Appendix E. The power splitter and power combiner have a conversion loss that makes the circuit needs amplification.

Power splitter/combiner

The power splitter/combiner (in dark blue in Figure 9.7) is a three-port network used to split or combine two signals into one or conversely. As a complete study of these networks is presented in Appendix E, we only focus our specific needs here. In this chapter, a power combiner of three ports is used, hence the attenuation A is given by :

$$A = -G = 6 \text{ dB}$$

and thus we have :

$$R = 1.\overline{66}\Omega$$

This power combiner/splitter has a real gain of -5.933 dB; this means that the network has a resistive loss due to thermal dissipation and which is unavoidable. In addition to this, there is an error due to non-ideal resistances' value because of the rounding to a normalised value. Table 9.2 shows the difference between real and ideal scenarios we have with exact and rounded resistance values.

N	3
Ideal resistance [Ω]	16.67
Real resistance [Ω]	16
Real input impedance	49.00
Absolute error on input impedance	1.00
Ideal Gain	0.25
Real Gain	0.26
Ideal Gain [dB]	-6.00
Real Gain [dB]	-5.93

Table 9.2: Comparison between ideal and real scenarios of power splitter/combiner

Cross pad attenuator

The design of the attenuator (in red in Figure 9.7) takes into account the levels of the signals that will be sent or received. According to the budget link (Table 9.1) where the level of the incoming signal is -11 dBm, the level of the signal entering through the mixer at the LO port must have a level of 7 dBm, the attenuator pad can have a real gain of -6.559 dB with:

$$R_1 = 18\Omega \qquad \text{and} \qquad R_2 = 130\Omega$$

or -5.673 dB with:

$$R_1 = 16\Omega \qquad \text{and} \qquad R_2 = 150\Omega$$

In order to minimize losses and mismatch caused by rounding the resistance value, it is necessary to evaluate the effect of this rounding when the exact value falls between two normalized values. We target to have at the amplifier an impedance that is close to 50Ω (see Figure 9.8).

The impedance Z_{in} seen by the amplifier depends on the chosen value of the resistances that form the resistive networks and is expressed as follows:

$$Z_{IN} = R + \frac{(R + K)(R + Z_0)}{2R + K + Z_0}$$
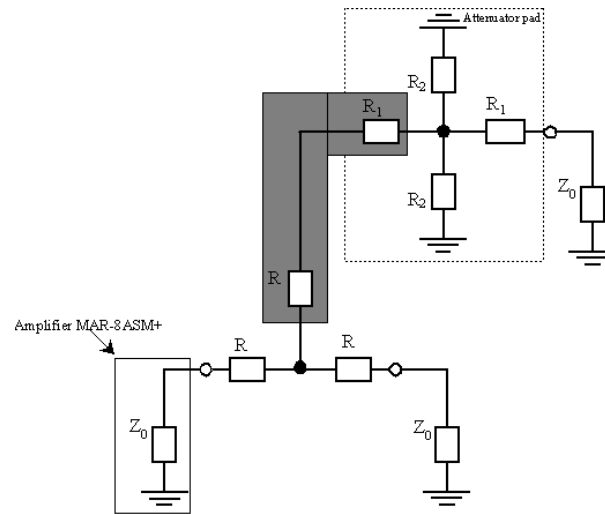
Figure 9.8: Impedance seen by the amplifier MAR-8ASM+

where K is the impedance seen at the attenuator pad :

$$K = R_1 + \frac{R_2(Z_0 + R_1)}{2(Z_0 + R_1) + R_2}$$

The impedance seen by the amplifier, depending on the choice of R values, is shown in Table 9.3. The design of the power splitter is the same as for the power combiner; for the first choice, the value of the resistances R of the power splitter can be done with 16Ω. The other choice is made on the resistances that give an input impedance close to 50Ω:

Z0 [Ω]	R [Ω]	R1 [Ω]	R2 [Ω]	Z IN [Ω]
50.000	16.000	18.000	120.000	48.969
50.000	16.000	16.000	150.000	49.274
50.000	18.000	18.000	120.000	51.969
50.000	18.000	16.000	150.000	52.274

Table 9.3: Input impedance comparisons

This study shows that the choice $R = 16\Omega$, $R1 = 16\Omega$ and $R2 = 150\Omega$ gives an impedance that approaches the best the impedance $Z_0 = 50\Omega$. Therefore, this is the best way to have minimum mismatches in such a design. For a minimum number of components, resistances can be combined, as shown in Figure 9.9.
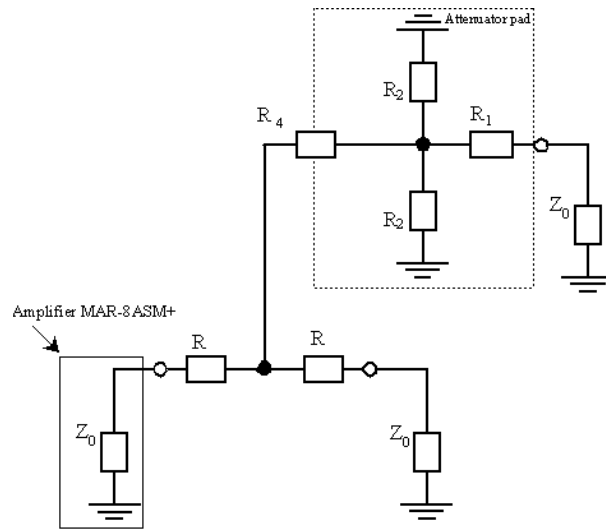
Figure 9.9: Impedance seen by the amplifier MAR-8ASM+ with R_4

In order to decrease the number of components on the circuit, we combine series resistances. The resistances R for the power splitter and R_1 for the attenuator pad (Figure 9.9) are combined. Hence it is necessary to study the impedance seen by the amplifier, with a normalized resistance R_4. The values of R_1 and R_2 are replaced in order to obtain a value that approaches the impedance seen by the amplifier, 50Ω.

R	R_1	R_2	R_4	Z_{in}	R'_4	R'	R'_1	R'_2	Z'_{in}
16	16	150	32	49.274	33	18	15	150	51.955
16	16	150	32	49.274	33	15	18	120	47.468
16	16	150	32	49.274	30	15	15	150	47.455
16	18	120	34	48.969	33	18	15	150	51.955
16	18	120	34	48.969	33	18	18	120	51.969
16	18	120	34	48.969	36	16	20	100	48.790
16	18	120	34	48.969	36	16	20	110	49.199
18	16	150	34	52.274	33	18	15	150	51.955
18	18	120	36	51.969	36	18	18	120	51.969

Table 9.4: Study of combined resistances with $Z_0 = 50\Omega$ (all values are expressed in $[\Omega]$)

The choice for the resistance values is based on the minimum losses and the adaptation of all the circuits to 50Ω. Therefore, the used values for the resistances in the power combiner and

the power splitter were 16Ω for each resistance, and in the attenuator pad 20Ω for R_1 and 110Ω for R_2. Since the resistance R_4 will replace R_1 and R, a resistance value of 36Ω is considered.

9.3.5   Decoupling elements

Generally, we use two decoupling capacitances for high frequency circuit: one of small capacitance value for decoupling high frequency noise and one of higher value for decoupling low frequency noise. The coupling capacitance value is chosen to be transparent with respect to the impedance of the port at 50Ω. For the power supply of the amplifier, we use a RFC inductor (RF Choke) for a better rejection of the RF signal in the path of the power supply. As RFC are more efficient in narrow-band system, we use a resistor to decrease the quality factor of the RFC inductor and thus to increase the bandwidth of the rejected signal. The RFC inductor needs to be carefully chosen with a series resonant frequency much higher than the 4.5 GHz of the RF signal because above this frequency the inductor behaves as a capacitor, as shown in Figure 9.10.
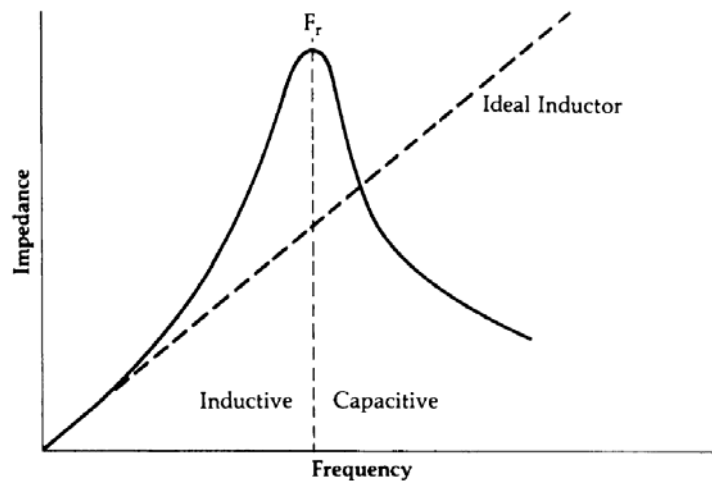
Figure 9.10: Inductance behavior according to the frequency [13]

The role of all passives is summarized in Table 9.5. We will complete this table with definite values after measurements of the I/Q demodulator.

Elements	*Function*
C_2, C_7, C_{11}	Decoupling high frequencies, prevent stray coupling from or to other signal processing components via the DC supply line.
C_1, C_8, C_{10}	Decoupling low frequencies

$R_9, R_{10}, R_{11}, R_{12}, R_{16}, R_{17}$	Bias resistances that are required to decrease the effect of voltage variation on bias current by approximating a current source.
L_1, L_2, L_3	Optional inductances that block the high frequencies to the supply
C_3, C_5, C_9	Coupling capacitor for U_2, U_3, U_6 devices to prevent accidental application of a DC voltage
C_4, C_6, C_{12}	Coupling capacitor for U_2, U_3, U_6 devices to remove DC voltage
$R_1, R_2, R_3, R_4, R_5, R_6, R_7, R_8$	- 6dB attenuation pads
$R_{18}, R_{19}, R_{20}, R_{21}, {}_{R22}, R_{23}$	Power splitter resistive networks
R_{13}, R_{14}, R_{15}	Power combiner resistive network

Table 9.5: Function of passive elements

9.4   PCB layout - Prototype n° 1

The construction of the PCB requires care because we can have undesired parasitics as well as resistive loss at high frequency if it is badly designed. The circuit to design includes elements that work at different working frequencies as the input signal lies in a frequency range from 4.0 to 4.5 GHz while the oscillator works at a frequency of 4.25 GHz and the baseband signal lies from DC and 1 GHz. For these reasons, the design of the PCB is made with the following guidelines:

- The material used for the PCB is Duroid RO4003 instead of FR-4. It offers a better performance than the FR-4 at high frequencies [65] and it has low resistive losses. It can be used for microwave designs until 10 GHz while the FR-4 can work properly only until 2 or 3 GHz.

- The protection of the PCB is done by using electrochemical gold plating instead of varnish in order to preserve the relative permeability of the material.

- Many vias are used on the PCB in order to connect the ground layers with the smallest amount of parasitic inductance. The size of the vias on the PCB is 0.5 mm.

- All the components used are SMD (Surface Mount Devices). This has the advantage to minimize parasitic resistances due to pins and to decrease costs of production because of drilling.

- Components on the PCB must be as close as possible to each other in order to minimize losses.

The construction process of the I/Q demodulator is exactly the same as for the LNA, as explained in detail in Appendix C. The resulting circuit is shown in Figure 9.11.
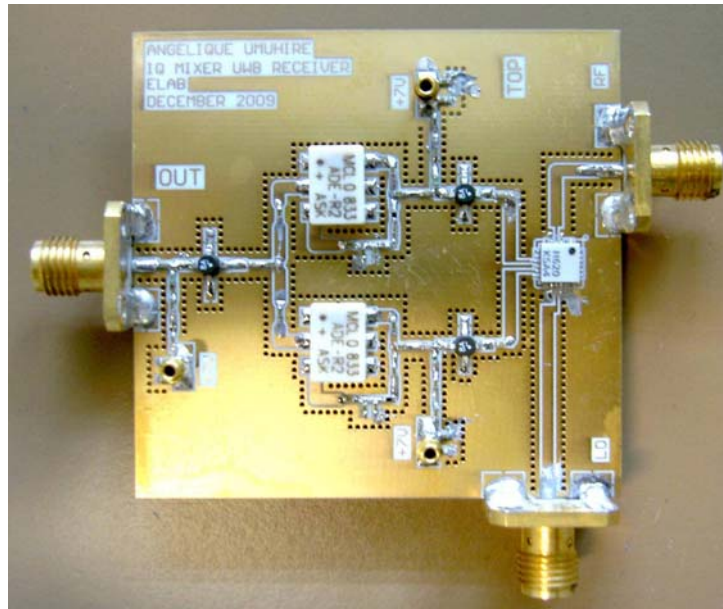
Figure 9.11: Close view of the I/Q receiver.

9.5   Measurements and tests

This section presents the experimental validation of the I/Q demodulator and its measurements. According to these measurements, we design the final prototype of I/Q demodulator, as shown in Section 9.6. A first set of measurements is made on the I/Q demodulator board without the I/Q mixer while the other set is made with the board with the I/Q mixer. We can thus correct our architecture in case we have an unexpected lack of signal power in our budget link.

9.5.1   The receiver board without the I/Q mixer

For these measurements, the HMC525LC4 I/Q mixer available on an evaluation board is used. It is connected to the receiver board with SMA connectors for both the I and Q components. The construction of the receiver without the I/Q mixer is made, first, with only one amplifier MAR-1+ (17.8 dB of gain at the output). Once this is done, and as the FPGA board needs a minimal amount of power for the acquisition, we can determine whether there is enough power at the output or not. Then, we add two amplifiers before the inputs of the receiver circuit (between the I/Q mixer and receiver boards): this shows what was expected, namely there is a too low signal level. This can be solved in three ways:

- The MAR-1+ amplifier with a low gain can be replaced by an amplifier with a higher gain, a MAR-8ASM+ from Minicircuits for example.

- The attenuator pad can be removed, which means that the attenuator pad is replaced by a wire (or a zero-ohm resistor) in order to have no attenuation. As the maximum power authorized for the RF port of the mixer is 17 dBm, the removing of the attenuator is possible (see Table 9.6). The input power from the I/Q mixer must be smaller than -14.5 dBm because of the maximum power level supported by the mixer.

- A cascade of amplifiers can be made to have a higher gain before the ADE-2ASK+ mixer (see Table 9.7). This, however, increases the risk of feed-back coupling and therefore unstability.

Cases	MAR-1+	MAR-8ASM+
Input power [dBm] (Point 1, see Figure 9.6)	-11.000	-11.000
I/Q output [dBm]	-18.500	-18.500
Output amplifier [dBm] (Point 2)	13.000	13.000
Output mixer [dBm]	1.300	1.300
Power combiner output [dBm]	-4.700	-4.700
Amplifier output [dBm] (Point 5)	13.100	26.800
Amplifier output [mW] (Point 5)	20.420	478.630

Table 9.6: Estimated budget link by removing the attenuator

Cases	Two MAR-1+	One MAR-8ASM+
Input power [dBm] (Point 1, see Figure 9.6)	-11.000	-11.000
I/Q output [dBm]	-18.500	-18.500
Amplifier output [dBm] (Point 2)	17.100	13.000
RF Mixer input	5.100	1.000
Output mixer [dBm]	-0.400	-4.700
Power combiner output [dBm]	-6.600	-10.700
Amplifier output [dBm] (Point 5)	24.900	20.800
Amplifier output [mW] (Point 5)	20.420	120.226

Table 9.7: Comparison between the cascade of two ampli-
fiers and one amplifier at the I/Q mixer output.

The gain of two cascaded amplifiers MAR-1+ (35.6 dB) is approximately the same that the gain of one amplifier MAR-8ASM+ (31.5 dB). With two amplifiers MAR-8ASM+, we have too much power on the input of the mixer (its maximum input power is 17 dBm). Thus the choice depends on the power level we have at the input of the I/Q mixer. Figures 9.12, 9.13, 9.14 and 9.15 show the signal measured on the FPGA board for the first solution (two amplifiers) with a scale of 0.1V, 0.05V, 0.2V and 0.5V respectively. The distance between the antennas is 1.20 m. Because of the Friis formula, the power level of the received signal depends mainly on the distance and the level of the transmitted signal.
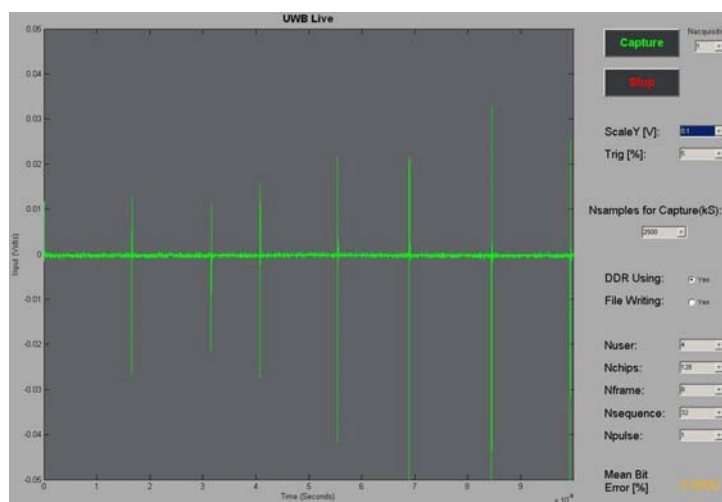

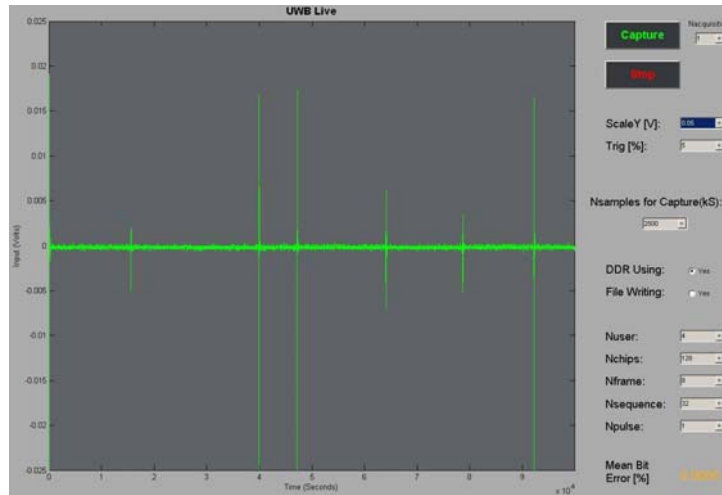Figure 9.12: The FPGA board received signal, scale 0.1V

Figure 9.13: The FPGA board received signal, scale 0.05V
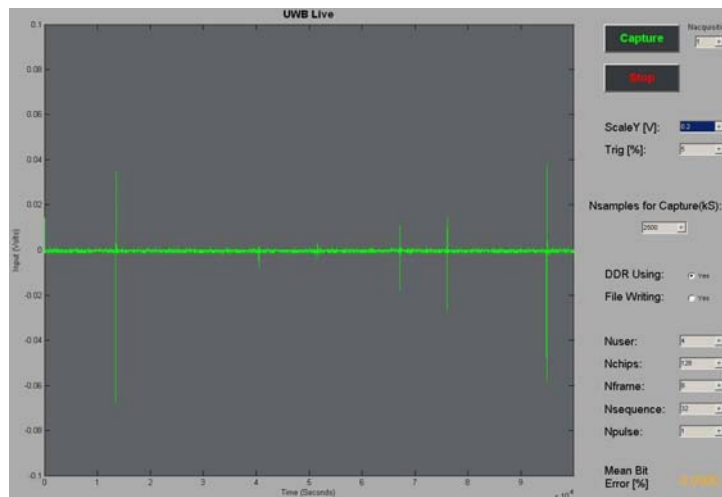
Figure 9.14: The FPGA board received signal, scale 0.2V

Figure 9.16 shows the received signal measured with the spectrum analyser. The frequency span is from DC to 1 GHz and the maximum power level is -68 dBm.

9.5.2 The receiver board with the I/Q mixer

The second set of measurements is made using the I/Q demodulator with the I/Q mixer HMC620LC4 on the same board. The construction of the circuit is made with the same consideration that was made with respect to the circuit without the I/Q mixer (see Section 9.5.1). This means that, instead of using the MAR-1+ amplifier at the output of the power combiner, we use the MAR-8ASM+ amplifier. Hence, the MAR-8ASM+ is used both at the I/Q mixer output and at
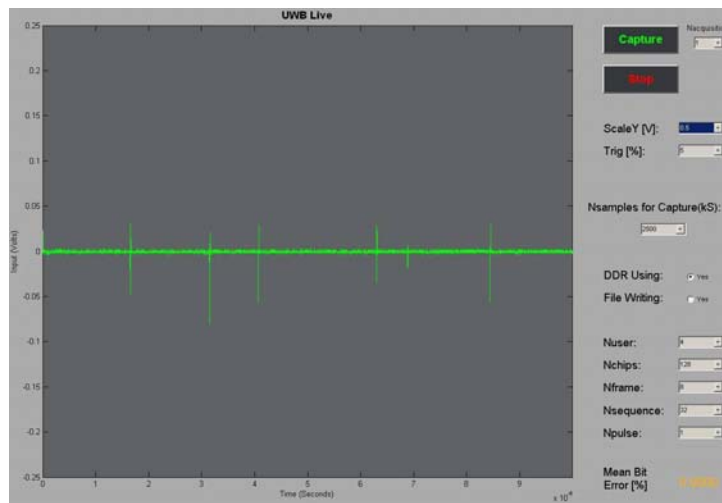
Figure 9.15: The FPGA board received signal, scale 0.5V
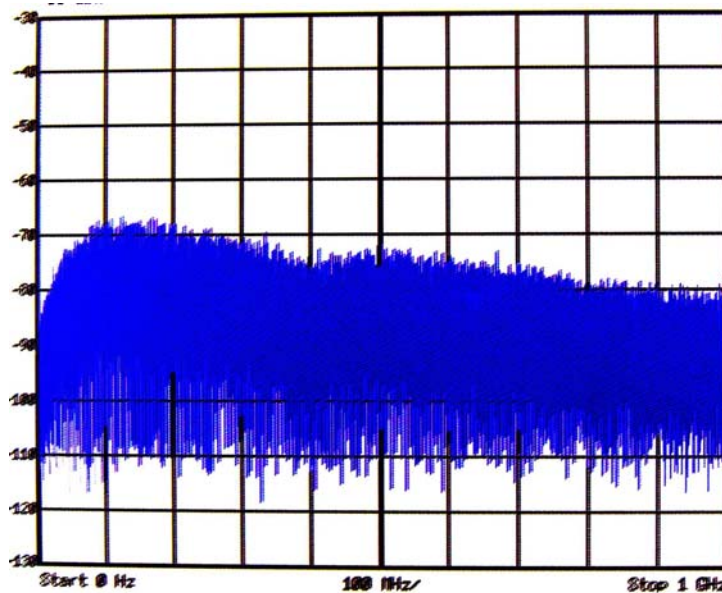
Figure 9.16: The received UWB signal with the board without the I/Q mixer

the output of the power combiner. This gives an acceptable power level to the signal that can be detected in any case by the FPGA board. The results obtained by using this circuit are shown in Figures 9.17, 9.18, 9.19, 9.20, 9.21 and 9.22 with a scale of 0.05V, 0.1V, 0.5V, 0.2V, 1V and 2V respectively. The distance between the antennas that were used to observe the signals was 1.20 m as before.
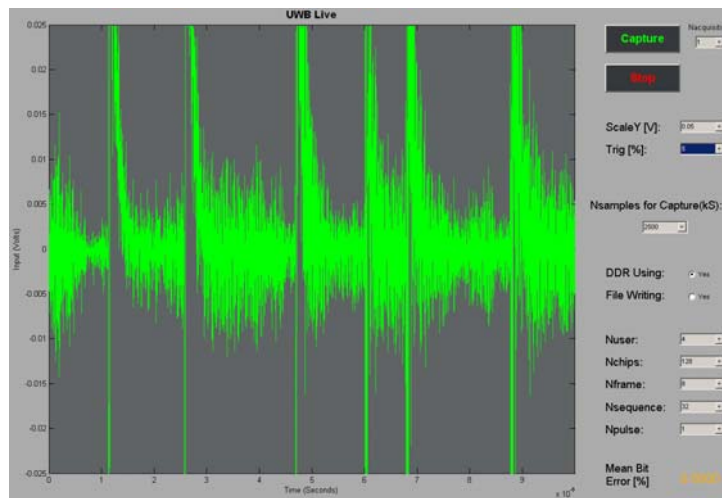
Figure 9.17: The FPGA board received signal, scale 0.05V
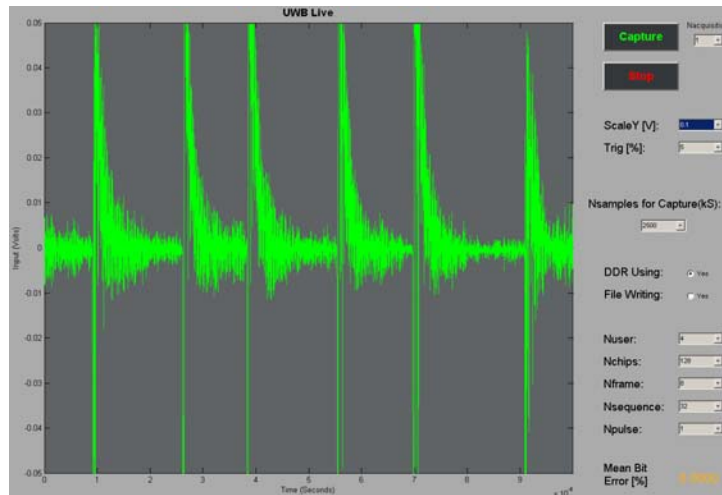
Figure 9.18: The FPGA board received signal, scale 0.1V

We observe that the FPGA board receives a good signal, even for high scales (Figure 9.22). We consider that the signal is correctly amplified here. The spectrum analyser shows the received signal and estimates its level.

The received signal is located around the frequency range from DC to 1GHz, as expected. We see its spectrum in Figure 9.23 and 9.24.

In Figures 9.23 and 9.24, we observe the received signal in a frequency range from DC to 1GHz. The level of the signal in this range is high, as it is estimated to be almost -30 dBm. The level of the signal received by the I/Q mixer is estimated at -60.830 dBm (see Table 9.8).

| *Output level [dBm] (Point 5, see Figure 9.6)* | -30.000 |

Input amplifier [dBm] Box 4	-61.500
Output mixer [dBm]	-55.500
RF Mixer input [dBm]	-50.100
Output power splitter [dBm]	-42.830
Input power splitter [dBm]	-36.830
Input amplifier [dBm]	-68.330
Input I/Q Mixer level [dBm] (Point 1)	-60.830
Input I/Q Mixer level [μW] (Point 1)	826.000

Table 9.8: Estimation of the level at the input of I/Q mixer

We measured the maximal distance for which the signal could be detected and we observe that, for a signal with a sensibility of 0.1V on the FPGA board, the distance between the two antennas is more than 2.50 m.

9.5.3 Conclusion on prototype nº 1

According to the measurements we made, the passive elements values we decided to use are given in Table 9.9 where U_2, U_3 and U_4 correspond to the amplifiers in the circuit.

Elements	*Values*	*Function*
C_2, C_7, C_{11}	10 nF	Decoupling high frequencies, prevent stray coupling from or to other signal processing components via the DC supply line.
C_1, C_8, C_{10}	100 nF	Decoupling low frequencies
R_9, R_{12}, R_{16} R_{10}, R_{11}, R_{17}	62Ω 27Ω	Bias resistances that are required to decrease the effect of voltage variation on bias current by approximating a current source.
L_1, L_2, L_3	4.7 nH	Optional inductances that block the high frequencies to the supply

C_3, C_5, C_9	2.2 nF	Coupling capacitor for U_2, U_3, U_6 devices to prevent accidental application of a DC voltage
C_4, C_6, C_{12}	2.2 nF	Coupling capacitor for U_2, U_3, U_6 devices to remove DC voltage
R_1, R_4, R_8, R_5 R_2, R_3, R_6, R_7	20Ω 110Ω	-6 dB attenuation pads
R_{18}, R_{19}, R_{20}, R_{21}, R_{22}, R_{23}	16Ω	Power splitter resistive networks
R_{13}, R_{14}, R_{15}	16Ω	Power combiner resistive network

Table 9.9: Values of the passive elements

The range of signal levels that can be detected by the circuit depends largely on the maximum power level that the mixer can accept on its RF input. This level is $+7$ dBm, thus the receiver can detect signals with a level lower than $+7$ dBm. Without any attenuator before the RF port, the input level at the RF and LO entries of the mixer have the same value but, because there is an attenuator before the RF port and as the level at the LO port has to be 7 dBm, the maximal admissible level of 17 dBm at the RF port is never be reached.

LO input level of the normal mixer	7dBm
Input power splitter	-1dBm
Input amplifier [dBm]	-30.5dBm
RF input of the I/Q Mixer [dBm]	-23dBm

Table 9.10: Maximum RF input level of the I/Q mixer

The level at the RF input port of the I/Q mixer has to be smaller than -23 dBm, which is equal to 5μW for preventing the destruction of the mixer (see Table 9.10). The input power level must not exceed $+20$ dBm and $+13$ dBm for the HMC620LC4 I/Q mixer and the MAR-8ASM+ amplifier, respectively.
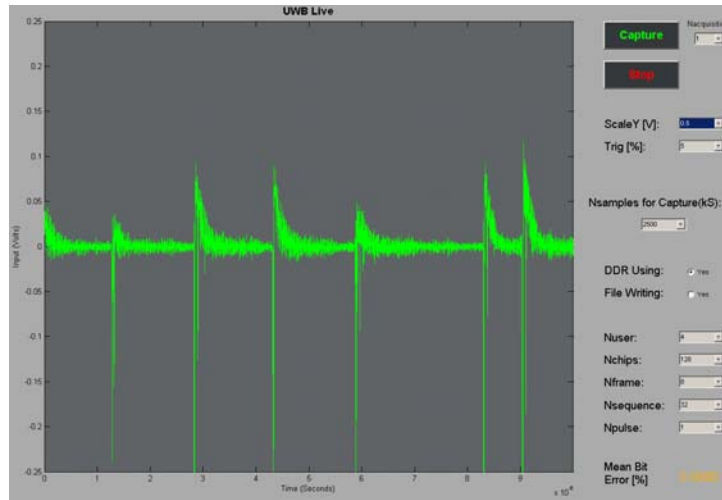
Figure 9.19: The FPGA board received signal, scale 0.5V
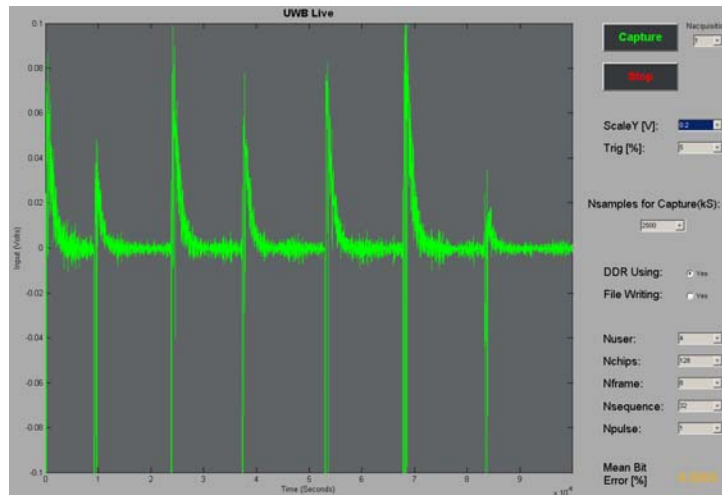
Figure 9.20: The FPGA board received signal, scale 0.2V

9.6   Improvement - Prototype nº 2

According to the measurements, we can design the second prototype of the I/Q demodulator with the local oscillator and a shielding box. The previous prototype achieves all the targeted challenges and only minor modifications are required for this one. The schematic of the prototype nº 2 is shown in figure 9.25 and the corresponding PCB layout is shown in Figure 9.26. The local oscillator is exactly the same as in Chapter 5. The finished I/Q demodulator in its shielding box is shown in Figure 9.27. We add a diode for protecting the circuit in case of polarity mistake in the power supply.
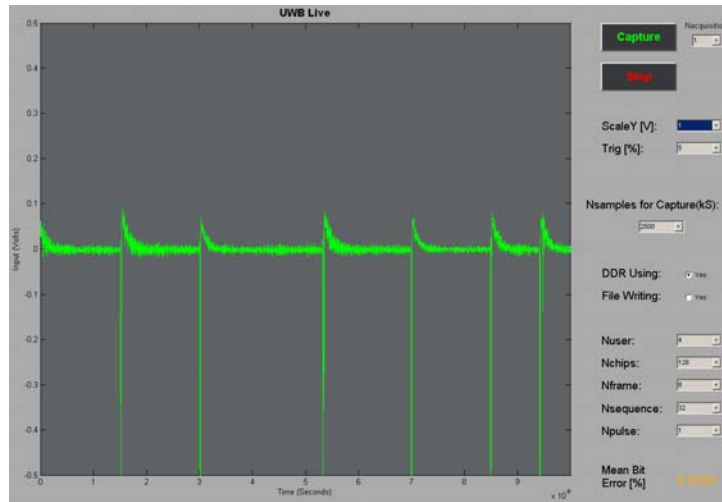
Figure 9.21: Received signal, scale 1V
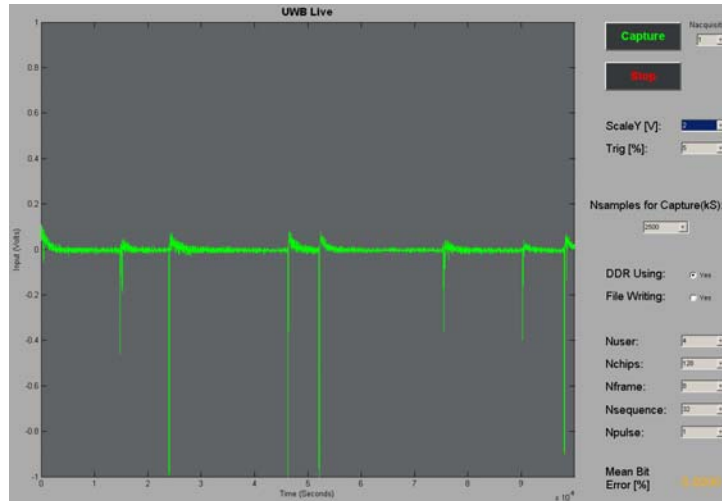
Figure 9.22: Received signal, scale 2V

9.7   Conclusion

In this chapter, we presented a complete UWB I/Q demodulator that can down-convert an incoming UWB signal from the 4.0 to 4.5 GHz frequency range to the DC to 1.0 GHz baseband. We demonstrate that, although UWB signals are not modulated with phase consideration (in IR-UWB), the I/Q approach is required for managing the phase shift between two remote asynchronous local oscillators. We present this architecture as a novel one as, to the best of our knowledge, we found nowhere anything else similar in UWB. The experimental validation of this architecture is exposed in articles [26], [39] and Chapter 10.

Figure 9.23: The received UWB signal, from DC - 0.5GHz

Figure 9.24: The received UWB signal, from DC - 1GHz

Figure 9.25: Schematic of the final UWB I/Q receiver

Figure 9.26: PCB layout of the final UWB I/Q receiver
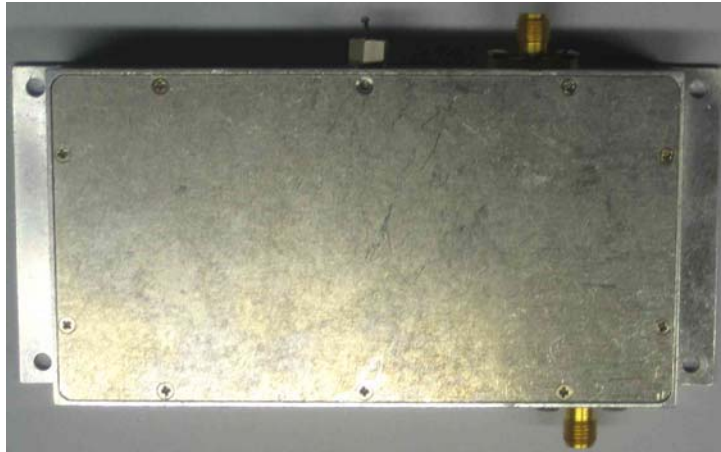
(a) View on the closed box
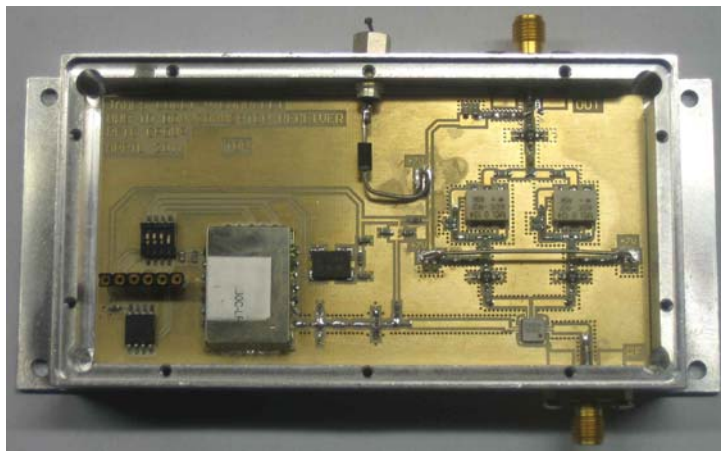
(b) View inside the box

Figure 9.27: *The final prototype of UWB I/Q demodulator.*

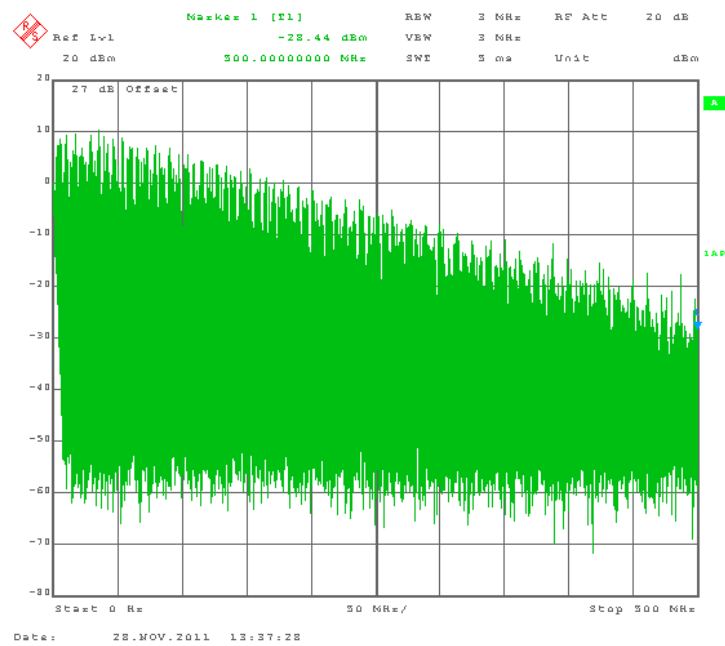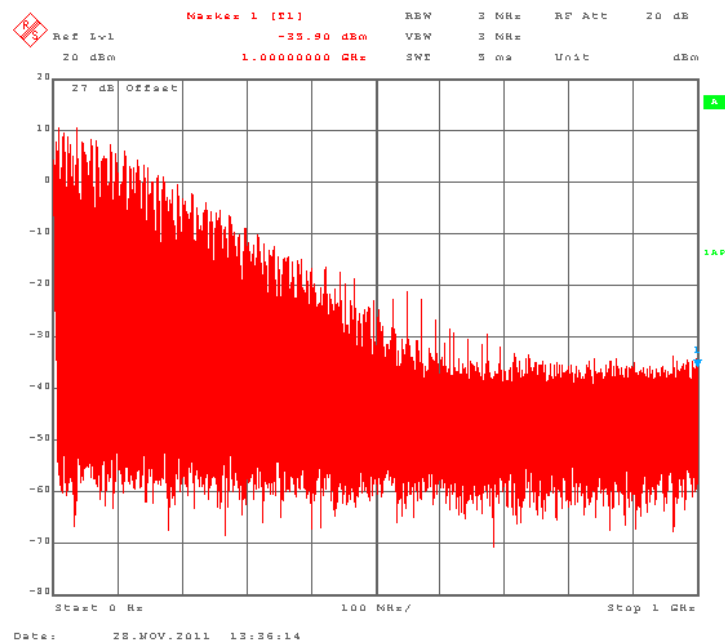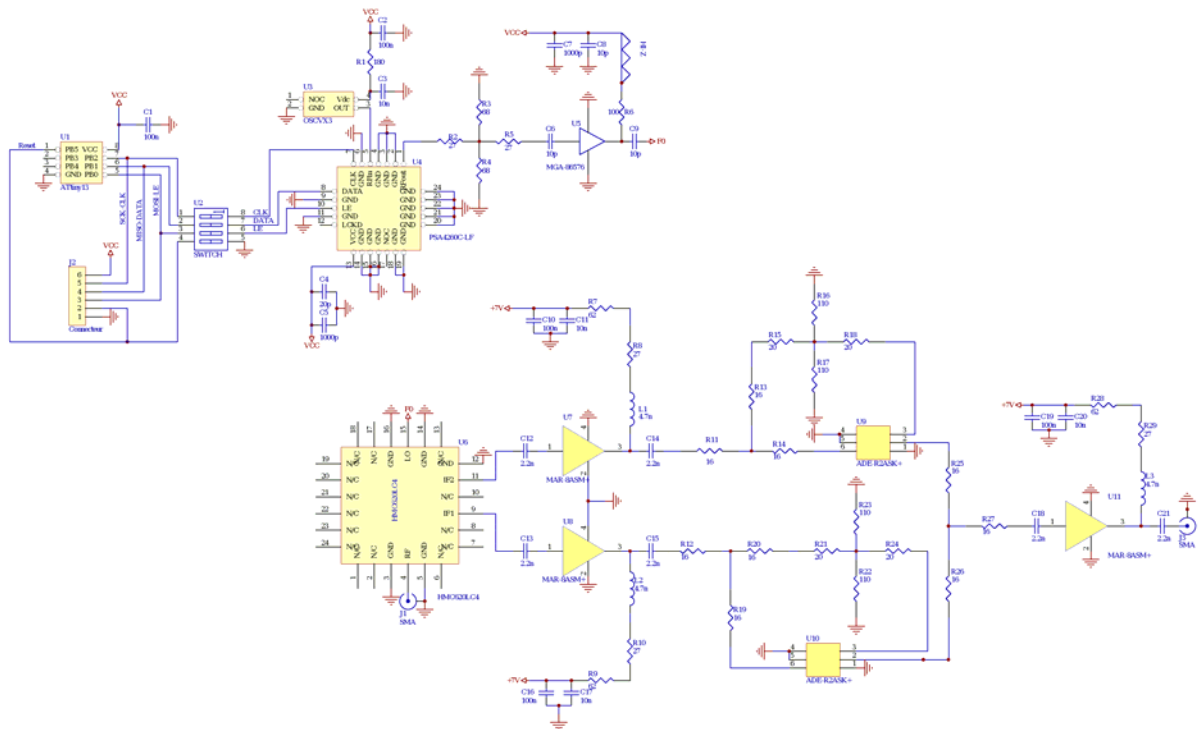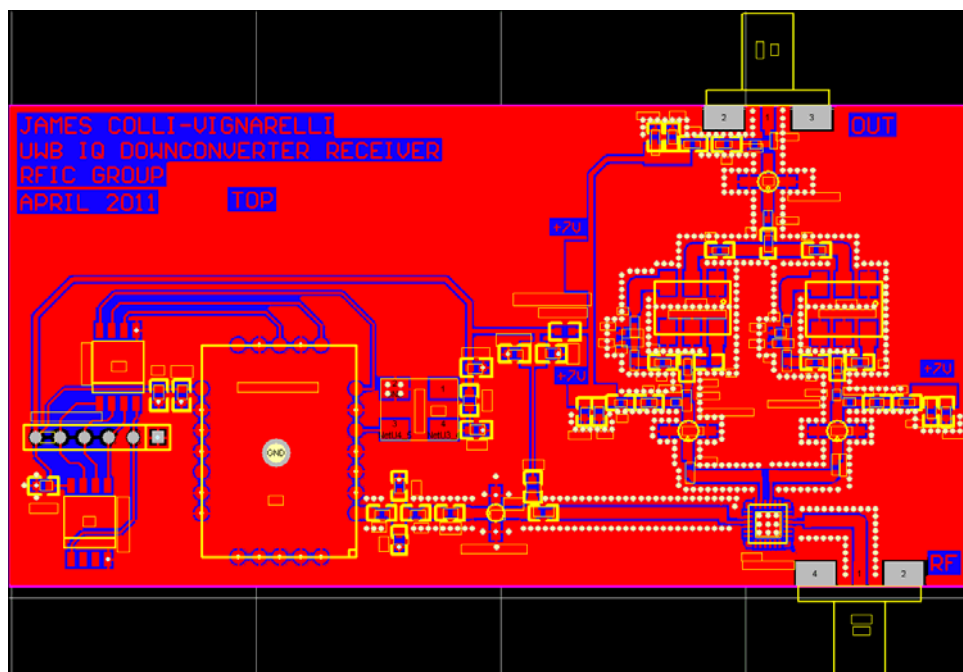<div align="right">

Chapter 10

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Experimental validation and performance evaluation with the UWB testbed

This chapter presents the experimental validations made with the use of the UWB testbed. The first one, presented in [26], shows the experimental validation of a PID algorithm that is robust against multi-user interference (MUI). This algorithm is described in detail in [24] but was never demonstrated experimentally until that time. The other experimental validations made with the testbed concern ranging, as shown in [35] and [10] , and also security as in [36]. It is remarkable that the U-Lite testbed is involved in several PhD works for which it was an essential tool for experimentation and validation.

10.1   Experimental validation of PID synchronisation algorithm

In this section, we present the experimental validation of the PID synchronisation algorithm described in [24]. This validation was one of our most important goal to achieve when we started to design this testbed (see Chapter 1). The PID synchronisation algorithm was developed on a theoretic way but the experimental validation was the last step to consider it as viable for publication and further research. This experimental validation shows that the conventional synchronisation algorithm (see [66]) is not robust against multi user interference while that the PID algorithm (see [24]) strongly outperforms the conventional one in terms of MUI robustness.

10.1.1   System presentation

Our system, as explained in Chapter 9, is completely asynchronous: there is no global synchronization between the transmitters and the receiver. Hence, at the receiver side, the first operation is packet detection and timing acquisition [64]. We implement two possible algorithms: (1) a conventional correlation based algorithm [66] and (2) a multi-user (MUI) robust algorithm [67]. Both algorithms are correlation based: the received signal is continuously correlated with a template. For the conventional algorithm, the correlation Φ of the received signal with the template is the sum of several individual correlations with a pulse template corresponding to a squared impulse i.e.

$$\Phi = \sum_{i=0}^{L_T-1} \Phi_i \tag{10.1}$$

where Φ_i is the i-th individual correlation result and L_T is the length of the template. However, the algorithm in [67] uses a threshold-based interference mitigation mechanism (see [68, 69] and the references therein): instead of summing the individual correlation, the algorithm in [67] applies a hard decision on the output of each individual correlation, i.e. (10.1) becomes

$$\Phi = \sum_{i=0}^{L_T-1} 1_{\{\Phi_i \geq \nu\}} \tag{10.2}$$

where ν is the hard decision threshold and $1_{\{x\}}$ is the indicator function. This threshold operation prevents spurious strong correlation outputs, essentially due to near-far interferers, which may completely blind the presence of a valid transmitter. As shown by simulations in [67] and experimentally in Section 10.1.2, the robust algorithm allows for successful timing acquisitions in the presence of MUI.

A detailed description of both algorithms lies outside the scope of this work. Still, in our implementation, both algorithms bypass coarse timing acquisition and perform directly a fine timing acquisition (they are performed in the digital domain). Once the fine timing acquisition is achieved, a verification phase follows. The initial timing acquisition is declared successful if $\Phi > \sigma_1$. The verification phase is declared successful if for N_v subsequent correlations, we have $\Phi > \sigma_2$. If the verification phase is successful, the receiver begins to search for the preamble delimiter. If successful, the receiver can start the demodulation of the payload. For the demodulation, we currently perform energy detection: The decision rule compares the energy contained at the two possible locations for a zero or a one [66]. The energy at each position is gathered over a duration T_{int}. We use energy detection because of its simplicity

and also because we can avoid any channel estimation. At this moment, we do not have any error correction code. In practice, after band-pass filtering and a low-noise amplification, our receiver performs the I/Q down-conversion. Even though we perform energy detection, we use a mixer for the demodulation for extensibility reasons: We want the ability to implement coherent processing in addition to energy detection. The signal after down-conversion is fed to an analog-to-digital converter (ADC) running at f_S. The ADC is coupled to an FPGA. The samples are then directly moved into a large DRAM on the FPGA and stored. The remaining operations, packet detection and timing acquisition and demodulation, are all performed in the digital domain. For instance, for energy detection, the integration over a duration T_{int} is replaced by a summation of N_{int} samples where $N_{int} = T_{int} \cdot f_S$. These operations are also all performed offline after the signal trace contained in the DRAM is offloaded to a PC. Typically, our ADC is running at $f_S = 2$ GS/s with an 8 bits resolution and we have 512 Mbyte of DRAM. Hence, we can store a signal trace of about 0.256 seconds. In our setting, this is sufficient to capture one or more packets and process them offline. We could use the FPGA to process the signal in real-time. However, an offline processing, although time consuming, allows for a greater flexibility. Real-time processing is scheduled for future work.

An overview of our experimental testbed with its characteristics is shown in Figure 10.1 (see Chapter 4 for more details).

10.1.2 Performance Evaluation

Measurements Settings and Scenarios

We consider three different scenarios for our experimental performance evaluation. First, a single user scenario (scenario A, *single user*, Figure 10.2(a)): one transmitter located at distance L of the receiver. We use Scenario A to validate our implementation and to obtain reference results. For the second scenario, (scenario B, *equal power*, Figure 10.2(b)), we have an additional interfering transmitter also at distance L from the receiver. Hence, the received power from the transmitter of interest and from the interfering transmitter is roughly identical. For the third scenario (scenario C, *near-far*, Figure 10.2(c)), the additional interfering transmitter is positioned in a near-far situation at a distance $L_{nf} < L$ from the receiver. Hence, the received power from the interfering transmitter is much higher than the power received from the transmitter of interest. This is a typical sensor networks or ad hoc network situation. We perform all experiments with line-of-sight (LOS) propagation. We consider $L = 1, 3, 6$ meters and $L_{nf} = 0.2$ meter. Remember that thanks to time-hopping, each transmitter has its own distinct
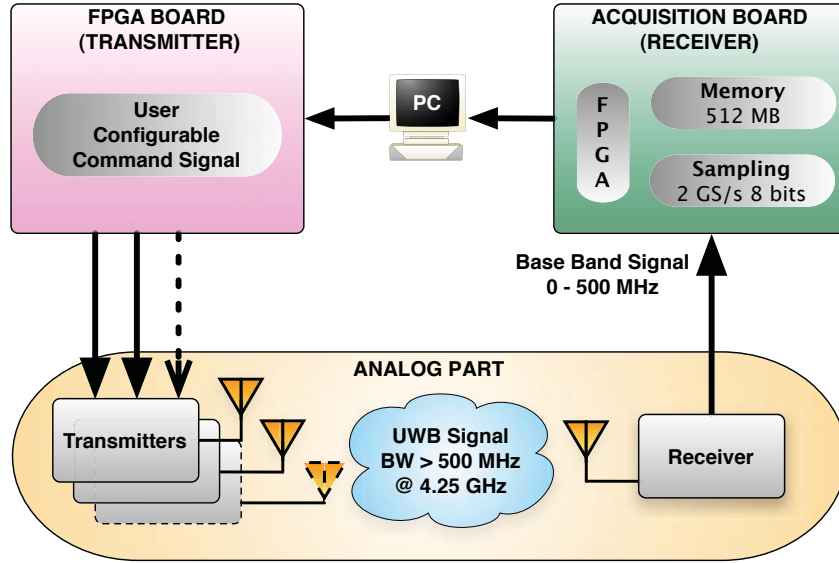
Figure 10.1: Overview of the testbed: an FPGA board controls the transmitters with the desired signal characteristics. The receiver amplifies, filters and down-converts the received signal to the baseband. The acquisition board of the receiver samples the baseband signal and stores this signal trace in DRAM on another FPGA. The signal trace is later offloaded to a PC for offline processing.

(a) Scenario A: *single user* scenario. We use it to validate our implementations and to obtain reference results.

(b) Scenario B: *equal power* scenario. The interfering transmitter is at the same distance from the receiver than the transmitter of interest.

(c) Scenario C: *near-far* scenario. The interfering transmitter is much closer to the receiver than the transmitter of interest.

Figure 10.2: The three topologies used for our experiments: a single user scenario, an equal power scenario and a near-far interference scenario. L and L_{nf}, where $L_{nf} < L$, are distances between the transmitters and the receiver.

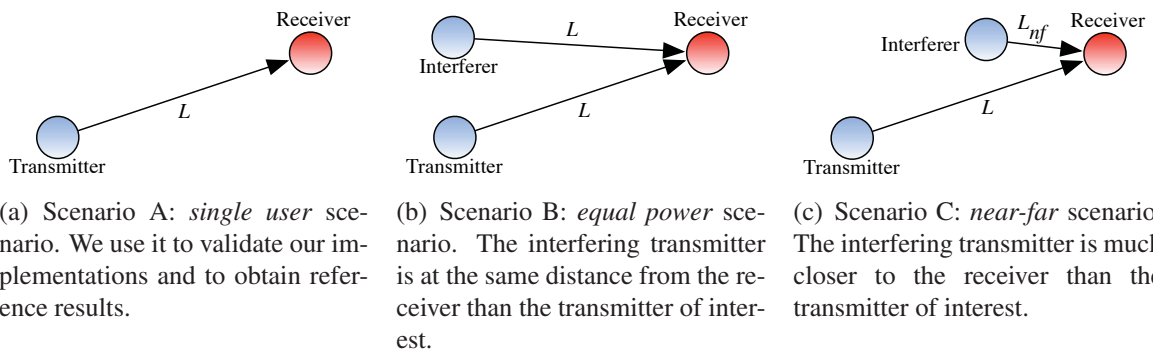preamble and preamble delimiter (see Section 1.1.5). Hence, a receiver can detect and acquire the timing of the packet from a given transmitter while another transmitter is active. Our main performance metric is the percentage of achieved packet detection and timing acquisition (A_{PDTA}). A packet detection and timing acquisition is declared `achieved` if a preamble delimiter is detected. However, this does not ensure that packet detection and timing acquisition is absolutely successful. For this, we would need a time reference for the received packet in order to compare with the timing acquired by our timing acquisition algorithm. However, for each packet where timing acquisition is achieved, we can additionally verify the BER of the payload. We observe during trial runs that if timing acquisition is incorrect, the BER is generally above 0.3 (even with MUI). Hence, for each packet where timing acquisition is achieved, we always compute the BER of this packet. If the BER is above a verification threshold $\gamma = 0.3$, we declare that timing acquisition failed.

In addition, we consider two other performance metrics: the packet error rate (PER) and the bit error rate (BER). For the PER a packet is considered corrupted when at least one bit is erroneous. The BER is computed only with payloads where timing acquisition was achieved. The PER reports both timing acquisition errors and erroneous bits in the payload. In the equal power and near-far scenario, the transmitter of interest sends packets. However, the interfering transmitter sends a continuous signal. This ensures that we evaluate the performance in a worst case scenario. To obtain statistically meaningful results we transmit $10,000$ packets per experiment run. For each experiment run, we always run both the MUI robust algorithm and the conventional algorithm on the same trace. As explained in Section 1.1.5, for each packet transmission, we first store the received signal in the DRAM of the FPGA. We then transfer the signal trace to a PC for offline processing. We perform all the processing with Matlab where we extensively use external functions written in C. Still, a typical $10,000$ packet experiment run lasts around 20 hours. Also, before each experiment run, we always carefully recalibrate the hardware: We verify and adjust the power spectral density of our signal to make sure it is FCC compliant and we adjust the hard decision thresholds. We set the range of the ADC to avoid any clipping on the strongest received signal. These last two operations, threshold setting and range calibration, are normally done automatically by estimating the noise variance and by performing automatic gain control (AGC) at the receiver. This is left for future work.

The parameters of the physical layer (see Section 1.1.5) are assigned the following values: $N_c = 128$ chips, $N_g = 8$ chips and $N_f = 8$ frames. With $T_c = 6$ ns (Appendix 1.1.5), this corresponds to a rate around 1.3 Mbit/s. For the ADC, $f_s = 2$ GS/s. For the packet parameters (see Figure 1.7), we use $L_{pre} = 32 * N_f$, $L_{del} = 8 * N_f$, $L_{pay} = 127$. With these values, the

duration of packet is about 1 ms. The timing acquisition algorithms use a template with a pulse width of 0.5 ns. The initial timing acquisition and verification phase thresholds are $\sigma_1 = 0.625$ and $\sigma_2 = 0.75$. These values are the optimal results found in [67]. For the demodulation, $N_{int} = 40$. A summary of these values is given in Table 10.1.

$N_c = 128$ chips	$N_g = 8$ chips
$N_f = 8$ frames	$T_c = 6$ ns
$f_s = 2$ GS/s	$L_{pre} = 32 * N_f$
$L_{del} = 8 * N_f$	$L_{pay} = 127$ bytes
template pulse width $= 0.5$ ns	$N_v = 16$
$\sigma_1 = 0.625$	$\sigma_2 = 0.75$
$N_{int} = 40$	$\gamma = 0.3$

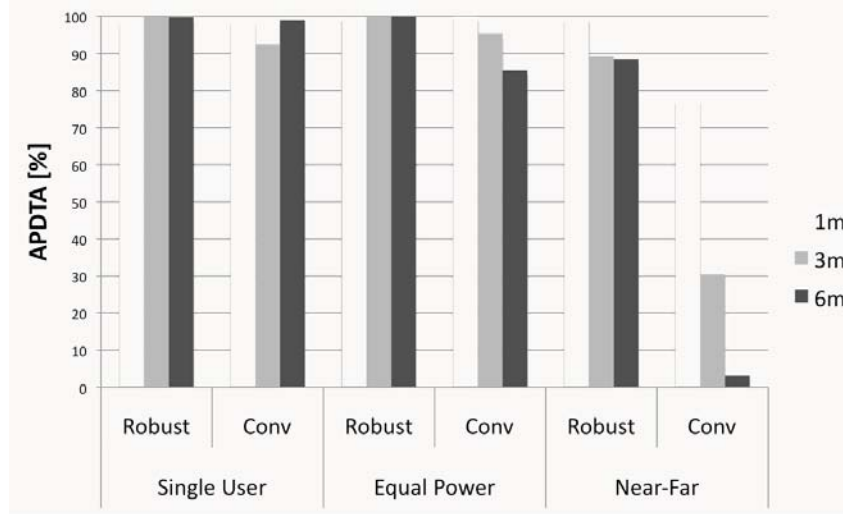Table 10.1: Parameters used for the experiments.

Measurements Results

Figure 10.3: Measurement results of achieved packet detection and timing acquisition (A_{PDTA}) for the Robust (multi-user robust algorithm) and Conv (conventional correlation based algorithm) algorithms, for our three scenarios: single user, equal power and near-far (see Figure 10.2). In each case, we consider $L = 1, 3, 6$ meters. For the near-far scenario, $L_{nf} = 0.2$ meter. The robust algorithm outperforms the conventional algorithms, especially in the near-far scenario. The conventional algorithm does not allow for a reliable packet detection and timing acquisition in the presence of MUI.

Figure 10.3 shows the percentage of achieved packet detection and timing acquisition A_{PDTA}. The MUI robust algorithm performs better than the conventional algorithm, especially

when the distance between the transmitter and the receiver increases. Interestingly, we notice that both algorithms are able to ensure a proper packet detection and timing acquisition in the single user and equal power scenario. However, we display here only the best results obtained with the conventional algorithm. As explained later in Section 10.1.2, the conventional algorithm is extremely sensitive to the surrounding environment and exhibits large variations from one experiment to another. Furthermore, in the near-far scenario, the conventional algorithm yields a much lower A_{PDTA}. It is completely outperformed by the MUI robust algorithm.

PER [%]	Single User		Equal Power		Near-Far	
	ROB	CONV	ROB	CONV	ROB	CONV
1m	1.27	1.27	39.36	39.27	65.98	72.65
3m	0.0	7.62	37.77	40.58	79.47	91.44
6m	0.26	1.01	54.71	61.47	70.43	98.73

Table 10.2: Measurement results of packet error rate (PER).

BER [%]	Single User		Equal Power		Near-Far	
	ROB	CONV	ROB	CONV	ROB	CONV
1m	0.0	0.0	0.49	0.48	2.35	2.40
3m	0.0	0.0	0.28	0.27	3.76	4.16
6m	0.004	0.004	0.85	0.85	4.42	3.95

Table 10.3: Measurement results of bit error rate (BER).

The PER and the BER are reported in Tables 10.2 and 10.3. Remember that no error correction or robust demodulation is used. Also, when timing acquisition fails for a given packet, this packet is not used to compute the BER but is taken into account for the PER. In the single user scenario, we observe a relatively low PER for both methods. In the two other scenarios, the PER is higher due to MUI. As expected, the bit error rate (BER) increases with the distance between the transmitter and the receiver. The PER after the timing acquisition with the MUI robust algorithm can be higher than with the conventional algorithm. This occurs because the MUI robust algorithms allows for timing acquisition in the presence of MUI and consequently allows for more cases where the payload experiences the presence of MUI. Additional observations have been made during trial experiments. For instance, we observed that the BER is lower when N_c is higher and A_{PDTA} is better when N_f is higher for both algorithms.

Validity of Our Results

To assess the validity of our results, two main factors have to be considered: first, our non-perfect hardware and the manual tuning of the thresholds. We have observed that the results obtained with the conventional algorithm show large variations from one experiment to another. In fact, the conventional algorithm is very sensitive to the surrounding environment. The fact that the laboratory where measurements are performed is not fully immune to electromagnetic radiations has to be considered. We believe, however, that the main reason for these variations comes from our hardware. The pulse amplitude is not always as constant as it should be, especially because of the imperfections of the oscillator. It is is very dependent on the power supply stability and on temperature variations. Multi-paths also strongly affect the amplitude of the signal. We did notice for instance that the variation of the signal amplitude has a relatively big impact on the conventional algorithm performance. Nevertheless, despite an imperfect hardware, the MUI robust algorithm exhibits a higher stability and outperforms the conventional algorithm.

Second, the choice of the hard decision threshold ν (see Section 1.1.5) potentially influences the results. The hard decision threshold of both algorithms is separately set, depending on the received power. In practice, we have to decrease the threshold as a function of the distance to obtain the best results. For the scenarios and distances of our measurement sets, the MUI robust algorithm hard decision threshold only requires slight tuning. Whereas, with the conventional algorithm, the hard decision threshold has to be precisely adjusted for each value of the link distance in the first two scenarios (single user and equal power). In the near-far scenario, it is constant because the interference is also constant in power. It is tuned manually and set after a certain number of trials. Therefore, this does not allow for a perfect comparison between the two timing acquisition algorithms. However the overall trend of the results obtained is validated by the multiple measurement runs performed. The MUI robust algorithm is much more resistant than the conventional algorithm, even without MUI.

10.1.3   Conclusion about PID algorithm

We have experimentally demonstrated that concurrent transmissions are feasible in low data-rate IR-UWB networks. We have also shown that interference mitigation techniques are indeed necessary at the physical layer. In particular, because it is the first component for the reception of a packet, we have focused on packet detection and timing acquisition. We have shown that a traditional scheme is not robust against multi-user interference, and prevents concurrent

transmissions. On the contrary, a scheme designed to take MUI into account, even with a very simple interference mitigation scheme, allows for concurrent transmissions, even in strong near-far scenarios. For future work, we will add real-time processing capabilities on the FPGA board. We will also implement a robust demodulation scheme for the payload and add an automatic gain control (AGC) algorithm jointly with an automated way to set the hard decision thresholds.

10.2   Experimental validation of ranging algorithm

As briefly mentioned in Section 1.1.4, the IR-UWB can be used for ranging and positioning applications. Our colleague Hai Zhan works for his PhD thesis on algorithms for UWB ranging and positioning (see [10]); he uses our testbed for validating his algorithmic improvement and also for characterising the behaviour of the UWB channel concerning multi-user robustness, which has a strong influence on the quality of the ranging. We emphasize that, without the testbed, these important results would not be validated as strongly as they were.

10.2.1   Experimental validation of the PQML algorithm

The PQML (Pseudo-Quadratic Maximum Likelihood Estimation Algorithm) is an original algorithm based on statistical techniques with high expected performance for ranging in weak LOS with IR-UWB. This algorithm is described in detail in [10]. In Figure 10.4 and Figure 10.5, we show the performance of the UWB PQML algorithm the absolute ranging error with respect to SNR under different distances and it is compared with the Iterative Quadratic Maximum Likelihood (IQML) algorithm, a similar technique described in [70], it is also compared with the Subspace-base algorithm (see [71]). From these Figures, we find that the absolute ranging errors of the PQML algorithm are significantly smaller than the IQML algorithm and the Subspace algorithm. The absolute ranging error of PQML algorithm becomes closer to the absolute ranging error of IQML even when the SNR is equal to 30dB (see Table 10.4). This validates experimentally that the PQML algorithm has a much higher performance than the others, although these are well known algorithms for ranging and PQML is a new original one.

10.2.2   Statistical Analysis of IR-UWB MUI

According to (see [10]), there are three kind of models for expressing the distribution of the multiuser interference (MUI): the Gaussian, the Middleton Class A Model (or MCA) and the
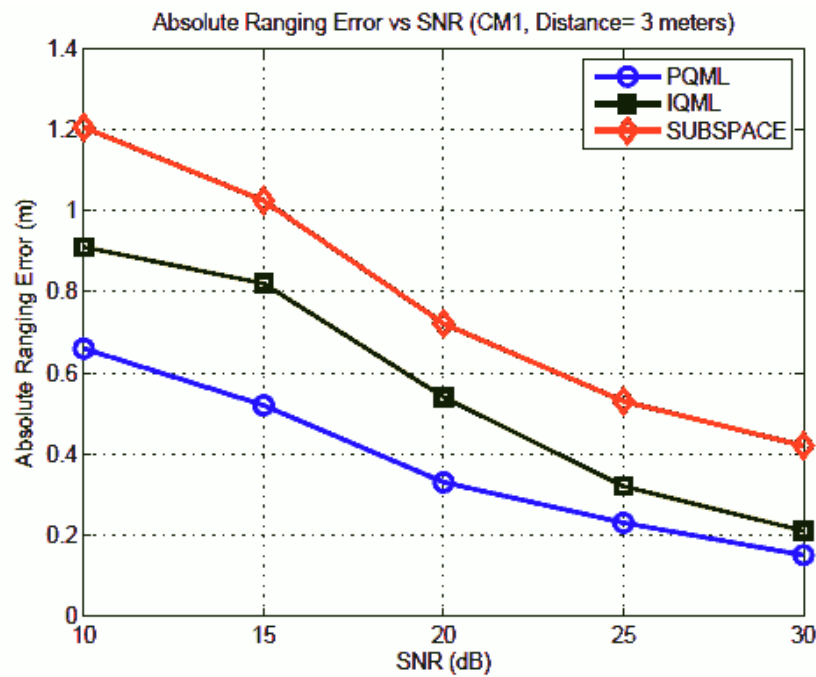
Figure 10.4: Absolute Ranging error vs. SNR. The distance between the transmitter and receiver is 3m (see [10]).
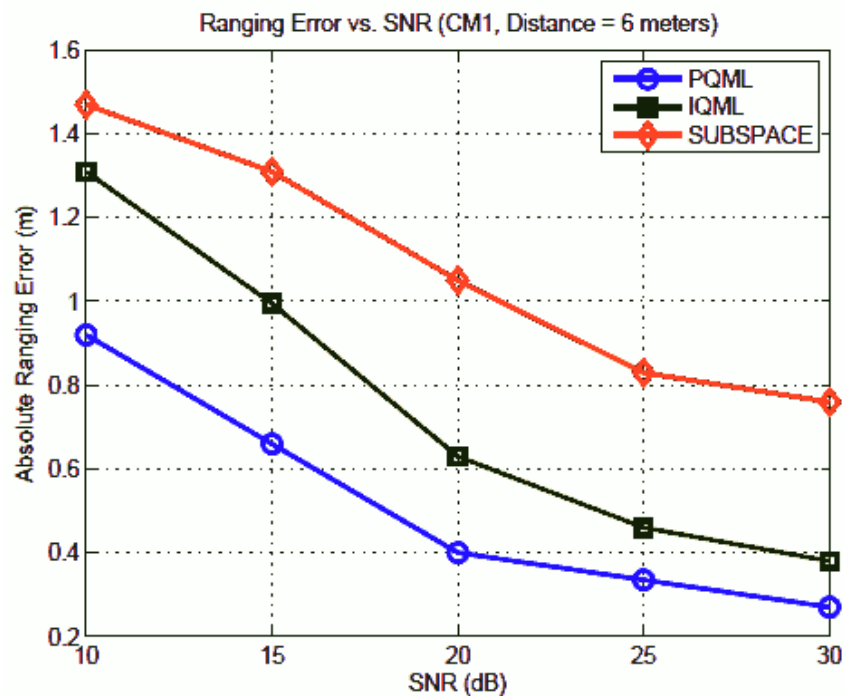

Figure 10.5: Absolute Ranging error vs. SNR. The distance between the transmitter and receiver is 6m (see [10]).

Algorithm	Absolute Ranging Error
PQML	1.63 cm
IQML	3.17 cm
Subspace	8.32 cm

Table 10.4: Absolute Ranging Error under Real Indoor Environments (see [10]).

Gaussian Mixture Model (or GMM). These models are of a high importance for an accurate understanding of MUI and a better design of ranging algorithm. In [10] and [34], our IR-UWB testbed is used to experimentally determine the parameters that belongs to these models according to real life scenarios and to validate the accuracy of these two formal models. Before these works, neither of these statistical models of MUI has been verified by measurements of IR-UWB under real indoor environments. A statistical analysis of IR-UWB MUI data is obtained from an extensive measurement set made in LOS environments. According to this analysis, the following conclusions are made:

- IR-UWB MUI in the time domain does not necessarily fit any Gaussian, GMM or Middleton Class A model alone;

- the samples of IR-UWB MUI are not independent in the time domain;

- the statistical analysis suggests a simple model of MUI in the frequency domain: the square root of MUI amplitude can be approximated with MCA model, the phase of MUI has uniform distribution on the interval $[-\pi, \pi]$ and the amplitude and phase of MUI are mutually independent.

10.3   Experimental validation of security algorithm

The security of IR-UWB communication is one of the most important considerations nowadays for daily life and industrial applications. This field was studied by our colleague Marcin Poturalski in his PhD thesis in which he uses our testbed for experimental validation of his security algorithms and counter measure against malicious attacks. This work is extensively described in reference [36].

10.4   Conclusion

This chapter ends the Part II of this work by showing all the applications our testbed was used in. There are several publications we mentioned that relate the testbed itself and/or its use in research environment. At this point, anyone can build exactly the same testbed for experimenting and validating new concepts and ideas in the field of IR-UWB with the possibility to compare the results by assuming the hardware is the same. This could help research to improve this field by making experimental results to be as much as possible independent to any initial - and sometimes arbitrary - hypothesis about hardware implementation as this is commonly the case. Another improvement is to allow any research group to modify and improve this hardware in order to meet any other specifications. For this, we give in Appendix F all the circuits we considered during the market search in order to make these modifications easier and faster.

The initial goal we planned is achieved; we focus thereafter on improving the power efficiency of a low-power IR-UWB Transmitter architecture made in integrated circuit. This would be described in Part III.

Part III

Design and realisation of integrated low power IR-UWB transmitter

<div align="right">

Chapter 11

</div>

Low-power transmitter architectures

11.1 Introduction

In a previous chapter, we described a discrete-components UWB transmitter that belongs to the UWB testbed. This transmitter was designed with the goal to fulfil as much as possible to UWB specifications in order to validate experimentally synchronization and localization algorithms. These validation procedures require to generate UWB signals that fulfils very accurately the standard regulations in order to make the validation results to be compared with already existing results and to be accepted by other researchers. The cost for generating a highly regulations-compliant UWB impulse is the power consumption that was very high for the discrete-components transmitter, as explained before.

One of the main goals of the work is to design and to develop a very low-power UWB transmitter architecture for mobile applications. This chapter explains the UWB transmitter architectures that were developed in integrated circuit technology and the two next chapters explain in detail how these circuits work and how they were designed. There are many architectures that were designed for UWB signal generation, as presented in several publications [44], [72] and [73]. The architectures presented here intend to go beyond that was already designed concerning the power consumption or, more precisely, concerning the use of the available power. It is important however to keep in mind that the transmitter works at a very high frequency (4.25 GHz) and, before doing the prototypes, it was not very clear what would be the limitations of the chosen technology. For these reasons, we decided from the beginning to focus mainly on the validation of the principle because once validated, it is more straightforward to adapt a proven principle to a more advanced technology. Obviously, all the best would be done to

reach as much as possible the target of 4.25 GHz because we intend to experimentally validate the integrated transmitter with the discrete-components testbed, which is optimally designed to work at this frequency.

11.2   Very low power transmitter architecture

This section presents how to evaluate the smallest level of power consumption that is required in theory to generate an UWB impulse that fulfils the regulations. The solutions already developed in publications are presented for the comparison. A discussion on the known techniques used for producing such a signal with – or without – restrictions on power consumption will be made and the retained solution will be presented. We present the solutions explored in this work and the challenges related to them.

11.2.1   Specifications

As required by the FCC regulations (see Figure 11.1 and [9]), the frequency spectrum allowed for UWB transmission starts from 3.1GHz to 10.6 GHz. The allowed spectrum is divided into different bands, the frequency range for each band and the transmission power level allowed in each band is given in detail in the IEEE 802.15.4a physical layer specifications for low rate personal area networks [74]. As already mentioned, there are two conditions (and only one of both is enough) for a signal to be considered as wide-band : it must have a bandwidth of at least 500 MHz, or its bandwidth must be at least 10% of the central frequency. In the domain of UWB communications, the signal bandwidth is measured at -10 dBr on contrary to the normal definition of bandwidth that is at -3 dBr.

In any case, the maximal average power cannot be greater than -41.3 dBm / MHz considering the EIRP (Equivalent Isotropically Radiated Power). The transmitter is asked to produce an UWB impulse with at least 500 MHz of bandwidth centered at 4.25 GHz with the smallest as possible power consumption. For this purpose, the smallest amount of power required for producing the highest impulse power allowed by the regulations needs first to be determined.

11.2.2   Minimal power estimation for a pulse

In this section, the minimal amount of power required for generating an UWB impulse is determined according to the FCC regulations. This gives a lower bound to the consumption of the
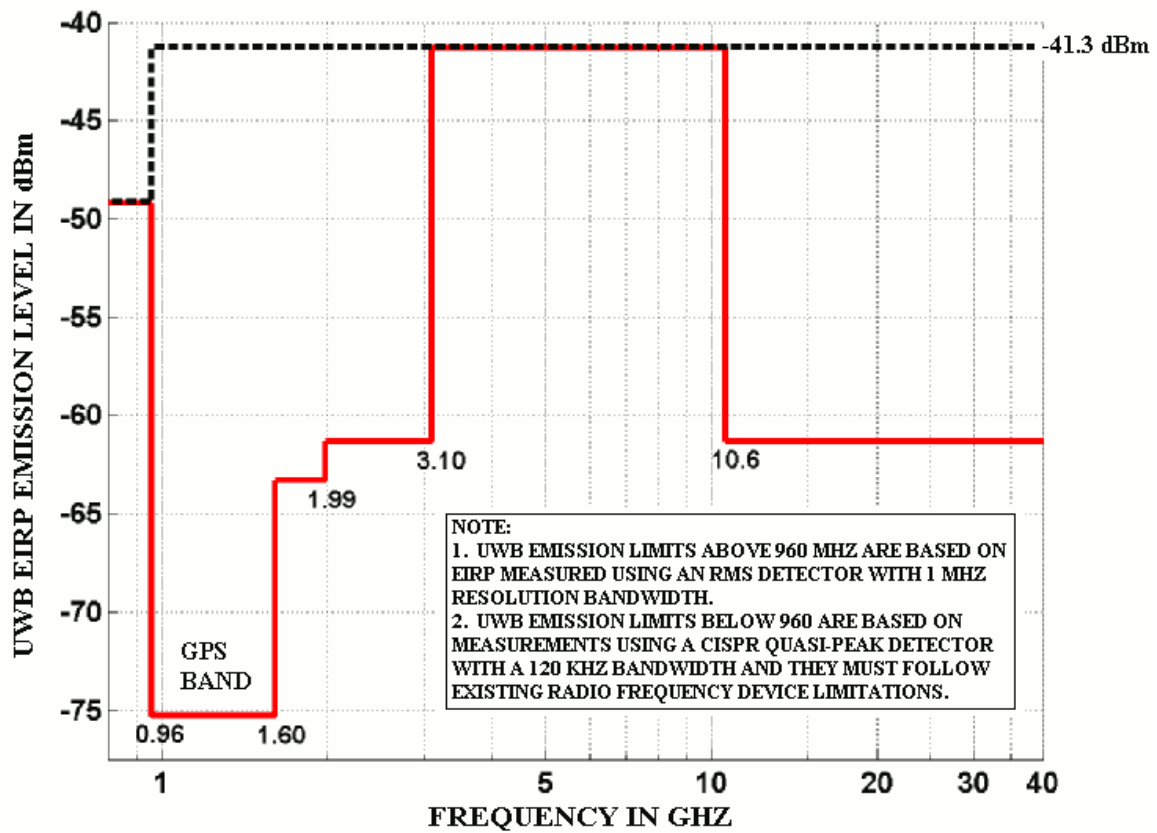
Figure 11.1: The FCC regulation mask for UWB.

circuit in order to make further comparison.

The maximal power allowed for generating an UWB signal in the 4.0 to 4.5 GHz frequency range is -41.3 dBm / MHz EIRP (Equivalent Isotropically Radiated Power). The EIRP corresponds to the equivalent power of the signal if this signal is radiated in all directions by an isotropic antenna. It is given by :

$$P_{EIRP} = P_T - L_C + G_a$$

where P_T is the power coming from the transmitter, L_C is the amount of losses in the cable to the antenna and G_a is the gain of the antenna; all of these are expressed in dB. For remembrance, the gain of an antenna (expressed in dBi, where i stands for *isotropic*) is defined as the ratio between the emitted power in a given direction and the equivalent power emitted by an isotropic antenna. This implies that the gain depends on the direction and the gain of

an isotropic antenna is constant and equal to 0 dBi. It also implies that an isotropic antenna requires the most power from the transmitter circuit in order to reach the maximal radiation power given by the FCC because it does not focus the power in a specific direction. The power of the measured signal is expressed in dBm / MHz since it is in fact a spectral power density; this is equivalent to say that the power is averaged on a duration of $1\mu s$ because it corresponds to the period of 1 MHz, the frequency by which the power is normalized.

By assuming that the antenna is isotropic (the worst case in terms of power requirement is assumed in order to calculate a conservative minimal value) and that the losses are negligible, the EIRP is simply given by :

$$P_{EIRP} = P_T$$

The minimal amount of power required by the transmitter in order to produces the maximal radiating power according to the FCC rules is thus given by :

$$P_{average} \quad = \quad -41.3 \text{ dBm/MHz} \cdot 500 \text{ MHz}$$

$$= \quad 50 \cdot 10^{-9} \text{ W/MHz} \cdot 500 \text{ MHz}$$

$$= \quad 25 \cdot 10^{-6} \text{ W}.$$

In this calculation, we assume a perfectly rectangular spectrum that fits exactly the 500 MHz bandwidth. Hence, a perfect transmitter should not only produce a perfectly rectangular spectrum but it should also have a complete use of its power supply by converting it integrally into an UWB signal. If such a transmitter would exist, it would consume 25μW in the worst case where an isotropic antenna is used. The same perfect transmitter would consume less power in case a non isotropic antenna is used, with the cost of the loss of the omnidirectivity.

11.2.3 Minimal voltage estimation for a pulse

In this section, we determine the voltage required to generate the UWB impulse that reaches the power calculated previously. This voltage is a rough estimation because we assume that the UWB spectrum is rectangular, which is not the case in practice and also because we model the signal in time domain by a truncated sine (see Figure 11.2 below) which has a sinc shape spectrum and not a rectangular one. This estimation will be sufficient, however, to check if the signal can be produced by an integrated circuit.
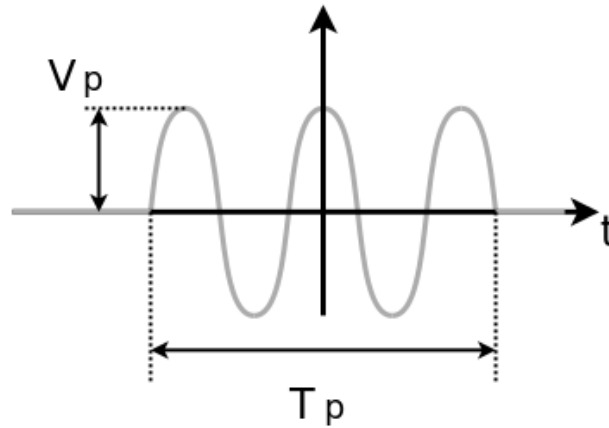
Figure 11.2: The truncated sine wave in the time domain.

We assume that this impulse is repeated $N_{pulses/\mu s}$ times per microsecond as the power is averaged over this time period (we thus have $N_{pulses/\mu s} = \frac{1\mu s}{PRP}$ where PRP that stands for *Pulse Repetition Period*). We thus assume :

- $f_0 = 4.25$ GHz. This frequency has no direct effect on the power calculation.

- The bandwidth is 500 MHz.

- $T_p = 2.94$ ns for a bandwidth of 500 MHz. We remember the relation: $K_{4.25 \text{ GHz}} = B \cdot T_p = 1.47$ (see section 3.4).

- $N_{pulses/\mu s} = 1$ (and thus $PRP = 1\mu s$) to fulfill the original specifications chosen for the testbed.

- The antenna has an impedance of 50Ω.

- The sine wave has an amplitude (or peak voltage) of V_p; this is the value we want to determine.

The average power is given in the time domain by :

$$P_{average} = P_{pulse} \cdot N_{pulses/\mu s} = \frac{P_{pulse}}{PRP}$$

We saw that the average power is at most 25μW. Let determine the peak voltage required to have this average power with the assumptions. As $N_{pulses/\mu s} = 1$, we simply have $P_{average} = P_{pulse}$.

The energy of an UWB impulse is given by :

$$E_{pulse} = \int_{-\frac{T_p}{2}}^{\frac{T_p}{2}} \frac{V^2(t)}{R} \cdot dt$$

where $V(t) = V_p \cdot \sin(2\pi f_0 t)$.

Assuming that the envelope of the impulse is rectangular and that T_p is an integer multiple of the period of the sine wave (such that the oscillating term in the integral vanishes), we have:

$$E_{pulse} = \frac{V_p{}^2}{2R} \cdot T_p$$

Hence, the power averaged over $1\mu s$ is:

$$P_{average} = \frac{E_{pulse}}{PRP} = \frac{V_p{}^2}{2R} \cdot \frac{T_p}{PRP} = \frac{V_p{}^2 \cdot T_p}{2 \cdot R} \cdot N_{pulses/\mu s}$$

As the average power is known, the peak voltage of the sine wave is given as follows :

$$\begin{aligned} V_p &= \sqrt{\frac{2 \cdot P_{average} \cdot R}{T_p \cdot N_{pulses/\mu s}}} \\[2mm] &= \sqrt{\frac{2 \cdot P_{average} \cdot R \cdot PRP}{T_p}} \end{aligned}$$

With the numeric values as assumed previously, we have the peak voltage :

$$V_p = \sqrt{\frac{2 \cdot 25 \cdot 10^{-6}W \cdot 50\Omega}{2.94 \cdot 10^{-3}\mu s \cdot 1/\mu s}} = 922mV$$

Assuming later an increase in the data rate to $PRP = 100ns$ gives $N_{pulses/\mu s} = 10/\mu s$, and we thus would have the peak voltage :

$$V_p = \sqrt{\frac{2 \cdot 25 \cdot 10^{-6}W \cdot 50\Omega}{2.94 \cdot 10^{-3}\mu s \cdot 10/\mu s}} = 292mV$$

Both of these voltages can easily be obtained by conventional CMOS integrated technology.

11.2.4   Overview of actual solutions for very low power UWB transmitter

One of the most current-consuming part of an UWB transmitter is the local oscillator [44] which is mostly an LC type; it is possible to stop it between two pulses but it needs time to set-up [75]. This was one of the first experiment we did (with the kind help of Dr. Norbert Joehl), as shown in Figure 11.3 below. This oscillator is a LC tank with a differential pair that is switched on and off for generating the impulses as shown in Figures 11.4 and 11.5. We see in Figure 11.6 that although the power consumption is very small it is not zero between two consecutive impulse because of the biasing current and leakage. Another problem is power amplification since an oscillator alone has not enough power for driving the antenna. The power consumption shown in Figure 11.6 considers the oscillator with a load impedance of $10k\Omega$. If the load impedance is decreased below this value, the oscillator stops working; as the antenna has an impedance of 50Ω, the oscillator is unable to drive it without a powerful and current-consuming amplifier, so the current consumption shown in Figure 11.6 is not relevant and LC oscillator are not so good candidates for very low-power transmitter designs.
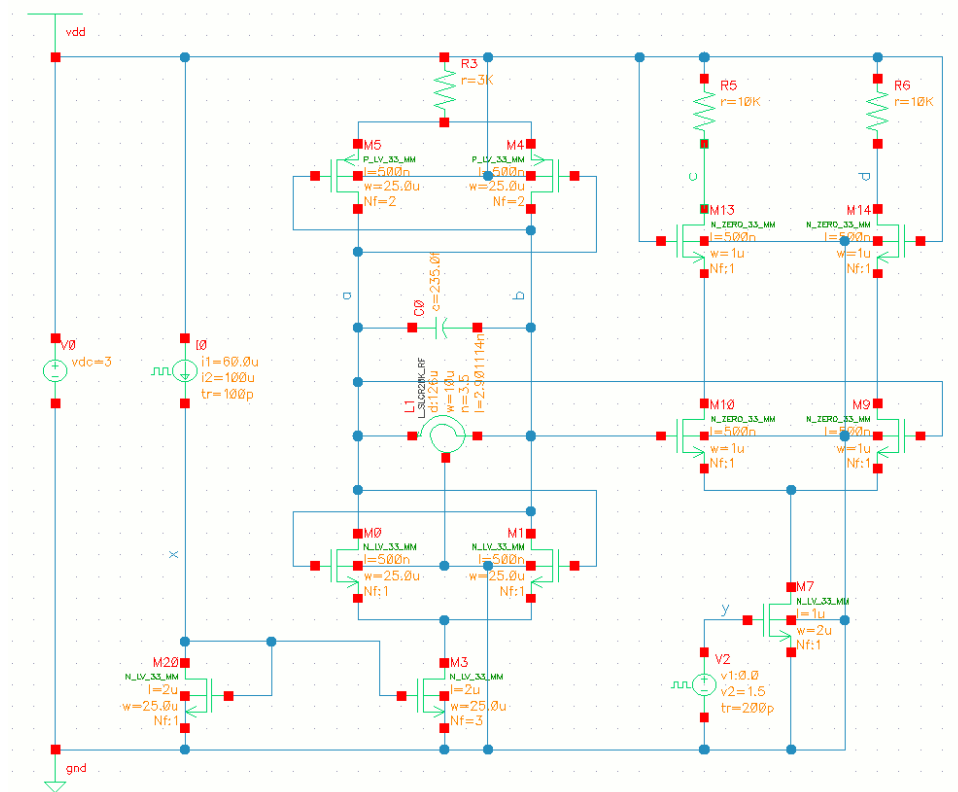
Figure 11.3: The LC oscillator schematic for experimentation (the third connection to the inductor is for a separation ground plane not shown in the schematic).
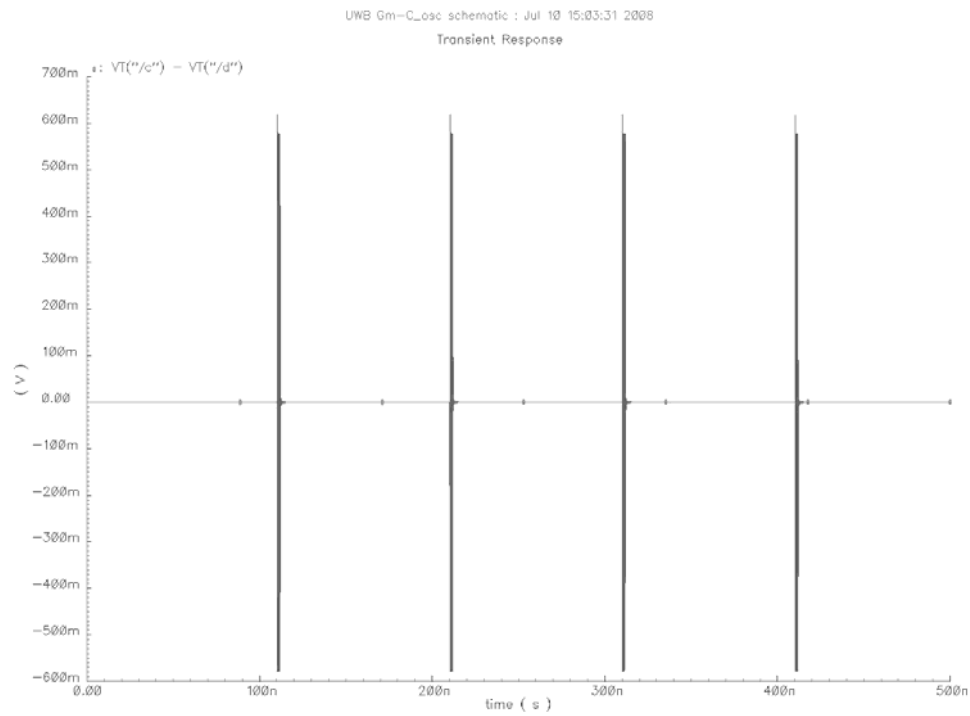
Figure 11.4: The LC oscillator output signal.
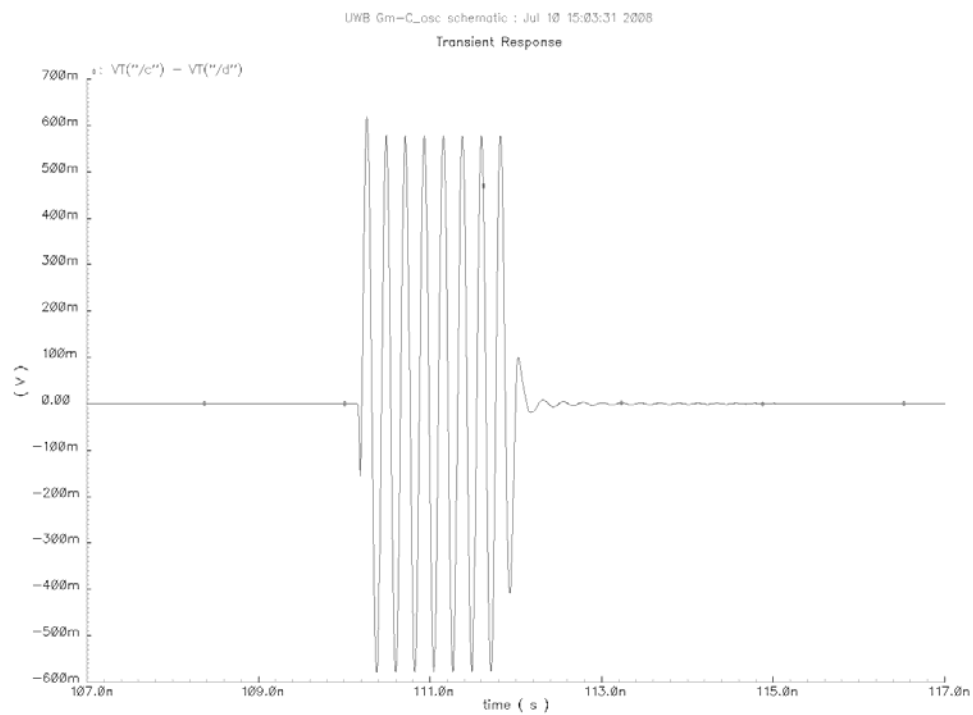
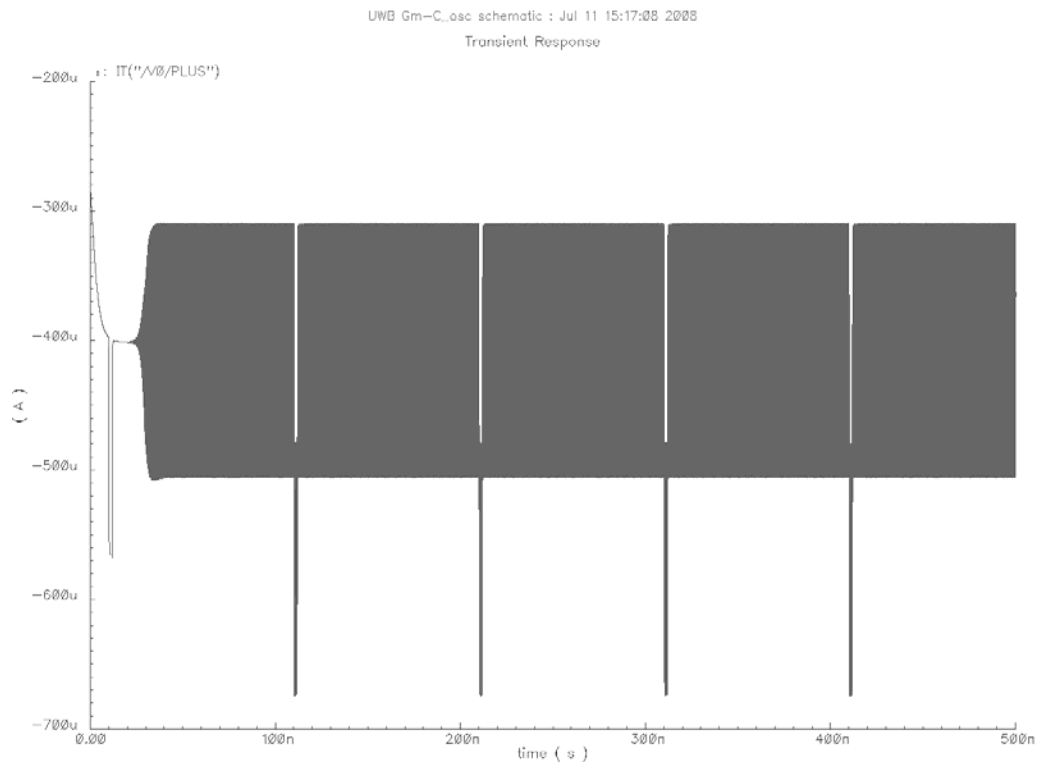Figure 11.5: The LC oscillator output signal - detail of one impulse.

Figure 11.6: The LC oscillator current consumption without amplification.

One way to avoid LC oscillator is to use digital means [33], [76], [77] and ring oscillators: they start instantaneously and have a low power consumption. There is however a problem which is the type of signal coming from these kinds of oscillators. They produce a square wave which has several harmonics at higher frequency than required by UWB specifications. Producing these harmonics is a waste of energy when considering the design of the optimal transmitter with respect to power consumption.

There are two very interesting approaches for solving this problem : one is given in [72] where the signal is created by digital means with delay lines which produce the UWB impulse, the second is given in [73] where an "ideal" impulse is mathematically created and stored in a digital memory where the signal is read and up-converted by an oscillator when a pulse is sent.

11.2.5   Solution retained for this work

According to the previous section, the challenge is to design a transmitter that produces an UWB impulse by using the smallest as possible amount of energy. The best circuit would be one which converts only the required amount of power needed to produce an UWB impulse without dissipation as explained therefore. This means that solutions with oscillators, PLL and any other analog circuits with high continuous bias currents would be rejected. We saw in addition that low-power solutions that produce an UWB signal with spectral power outside the bandwidth of interest like ring oscillators are also wasting energy. Thus, the optimal solution has not only to reduce or, better, to suppress all biasing and leakage currents but also to produce exactly the required signal. One step in the design of our solution is to calculate mathematically the ideal signal that fits the best the specifications – and thus reduces the power consumption – and then to store it in the transmitter in order to replay it during the emission by using the smallest amount of power. We will see in further sections how to store and reproduce on demand such a signal with very low power consumption. This principle is shown in figure 11.7 where the tape recorder symbolizes the mean described thereafter in the work to store and to replay the signal. The OOK modulation is equivalent to press "play" on the tape recorder (more precisely, every time a "one" is sent, the signal is played).
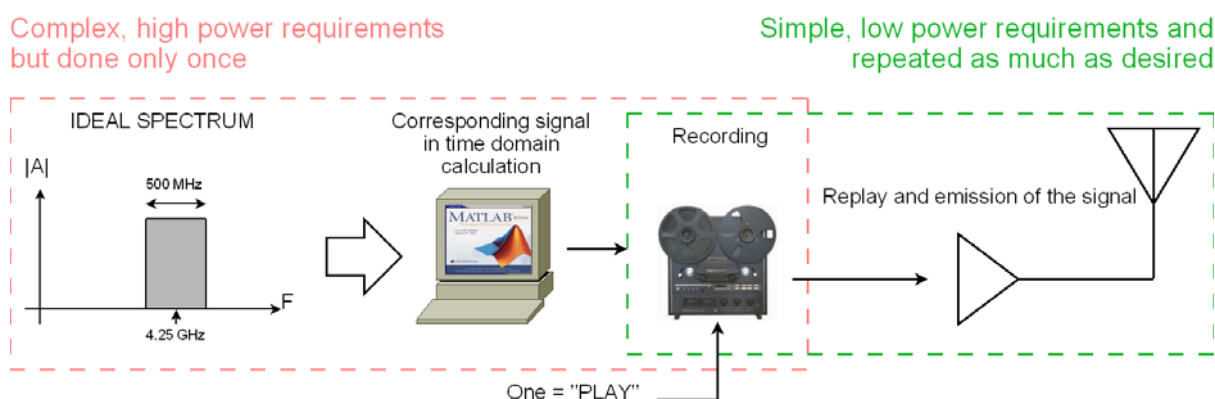
Figure 11.7: The principle of UWB signal recording.

The key idea is to optimize the signal generation by calculating in advance the optimal signal by using the required equipment and mathematic background developed in chapter 3 (red zone in Figure 11.7) in order to replay it as much as necessary by simple and inexpensive means (green zone in Figure 11.7). Obtaining an optimal signal is an endless task as there are many constraints that depend not only on the technological limitations but also on mathematical fundamental properties of the signals involved in the design. For these reasons, we made several

assumptions in further developments such that things remain relatively simple to calculate and to implement in a circuit.

Hardware implementation principle

The principle of the circuit is shown in Figure 11.8. Three different prototypes were designed during this work; they all follow the same signal generation principle as explained further. By using this architecture, we assume that the signal has a relatively small duration time.
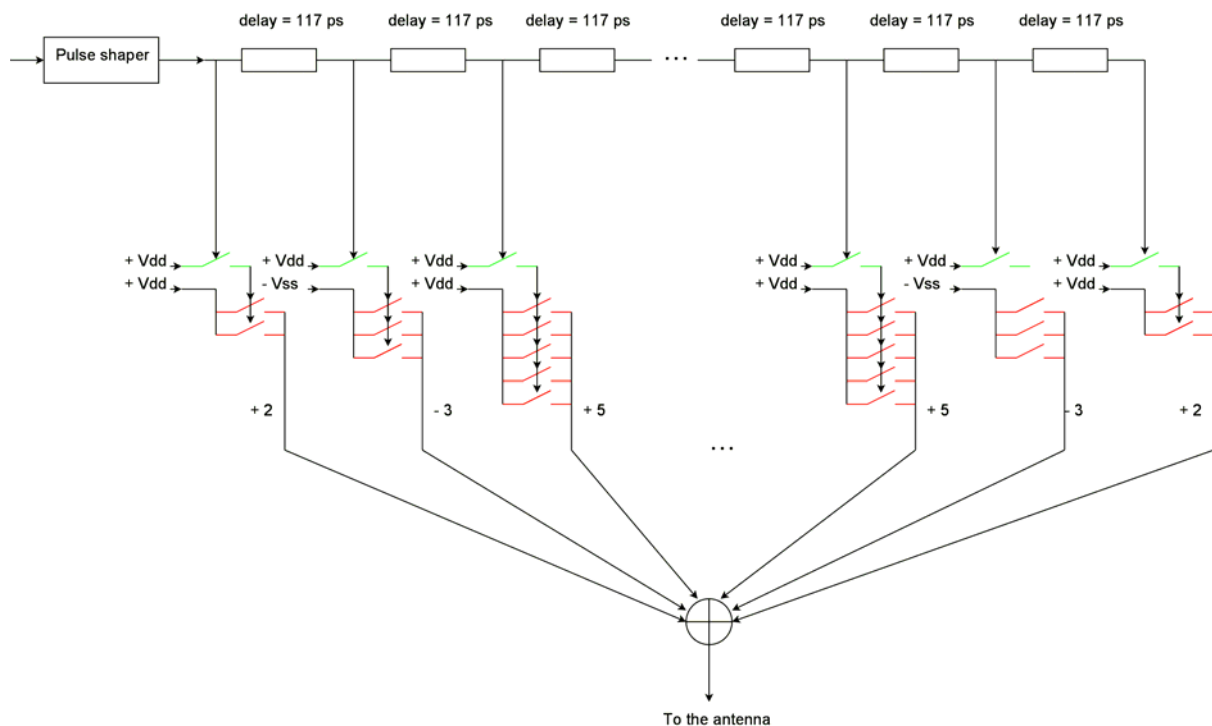

Figure 11.8: The principle of the UWB transmitter with very low power consumption.

The principle is to create point by point, by using digital transistors, an optimal signal whose spectrum fits the best the UWB specifications. This is similar to do a digital recording of the signal; the difference is that the signal is not recorded on a magnetic tape but into the silicon circuit by creating physically the sample's values by placing conveniently several transistors together and activating them at the right time. This activation is made by using a delay line dedicated to this purpose (see Figure 11.8). The delay line acts in this way as a sampling clock. It can be physically a transmission line or a cascade of inverters. It is theoretically possible to record any signal if it has a short enough duration to be stored into the chip (the duration of the signal is discussed later). It becomes thus possible to investigate which is the best signal in terms of UWB shape and energy savings in order to record it as it is without any consideration

on how the signal might be generated by purely analog or digital means.
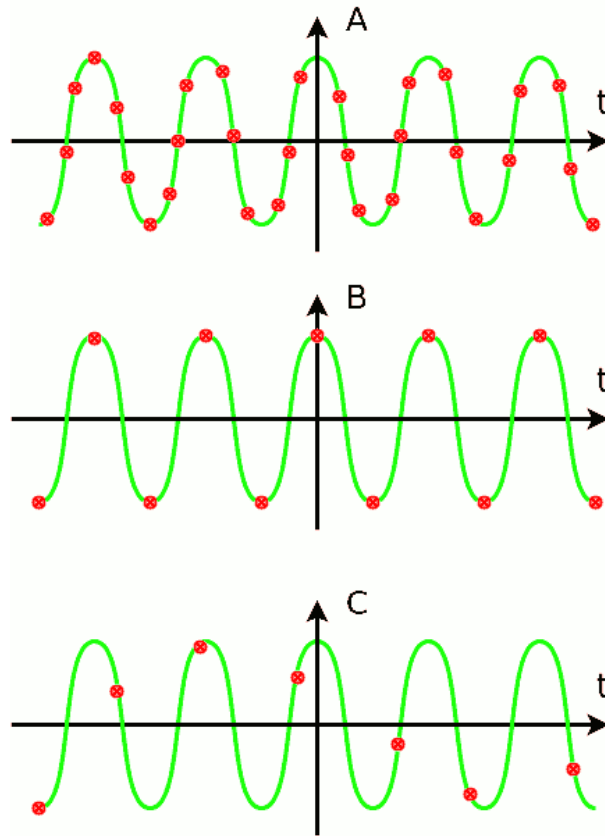
Figure 11.9: The three cases that occur in sampling theorem.

At this point, it is possible to consider the recording constraints. The underlying key idea is to store only the digital samples that represent extrema of the signal and to take advantage on the filtering properties of electronic integrated components. This process is shown in Figure 11.9 where the sampling theorem of Nyquist is illustrated. Let f_s be the sampling frequency and f_m the highest frequency contained in the sampled signal. The case (A) where $2 \cdot f_m < f_s$ is the normal case when a signal is sampled by applying the Nyquist theorem (like most of the cases of signal acquisition). The higher the sampling frequency f_s in comparison with f_m, the better is the signal acquisition. The case (C) shows what happens when Nyquist theorem is not applied by having $2 \cdot f_m > f_s$. The signal is distorted by aliasing and information is lost. The case (B) is the limit case when $2 \cdot f_m = f_s$. This case can only work if the signal is acquired on its extrema because sampling the signal elsewhere will remove the information contained in the signal and degrade the quality of its shape. This means that this kind of sampling can only be made on very well known signals as it is the case of the synthesis presented here.

This implies also that keeping only the local extremum of each inflexion of the signal would be enough to store it without severe degradation if the RLC behaviour of analog devices makes the interpolation. It is a way to benefit from these parasitics which are usually seen as a drawback of analog components.

According to this, the central frequency of the UWB spectrum is only determined by the time delay between two consecutive samples that corresponds to the half-period of the central frequency at 4.25GHz, thus 117.5ps. Changing the central frequency can easily be done by changing the corresponding delay. The wide band shape of the spectrum is not altered by this delay since it depends only on the value of the samples and their resolution. This is because the signal sample's values are discretized by rounding to the closest integer because of the sample's values that are represented by a given number of transistors in parallel. This means that the calculation of the samples is made once for a given central frequency and a given bandwidth in order to determine the sample's value set that gives the best UWB shape by taking into account of these parameters. Then, however, the central frequency can be changed or adjusted later if required by keeping the same samples values and only by changing the delay – i.e. the length of the clocking line between two samples.

The digital transistors are optimized for on/off switching at very high speed and they consume almost nothing (in exception of a very small leakage current) outside the switching process. This implies that the system is like in a stand-by mode between two pulses and when a pulse is emitted the current consumption rises because of the switching of the transistors and then returns to almost zero just after the pulse was sent.

The pulse shaper in Figure 11.8 is a circuit that produces an impulse of about 200 ps from the incoming bit stream (the bit stream could be any digital circuit like a FPGA or a microcontroller). This impulse travels along the delay lines and at every point it arrives to a green switch, this switch turns on. This is the equivalent part of the sampling clock of the digital recorder discussed previously. When a green switch is on, it drives its corresponding red switch cluster and switches it on also. The red switch clusters are the equivalent part of the set of digital samples recorded on the magnetic tape of the recorder. The red switches generate the power of the signal. Since the switches have all the same size and the same electrical properties, each sample value is made by adding as many as required switches in order to reach the integer value of its corresponding sample. This is why the rounding-to-integer process was needed.

The three prototypes described further show slightly different ways to implement this generic principle. The details of the implementation are given in the corresponding chapters.

The current impulses produced by the switches are combined by another transmission line

circuit symbolized by adders in Figure 11.8 in order to build the complete UWB signal and lead it to the antenna that lies outside the chip. This circuit is in fact similar to a FIR filter architecture where the weight given to the samples is determined by the number of transistors used in the red switch clusters and where the input signal is a digital short pulse, as shown in Figure 11.10.
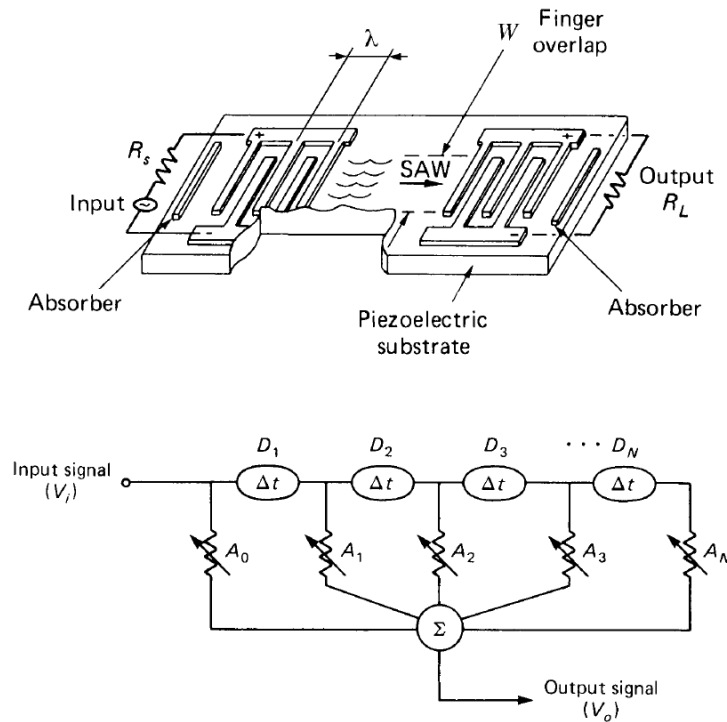
Figure 11.10: The FIR architecture (see [51]).

Mathematical signal determination

By a known property of the Fourier's transform, an infinite signal in the temporal domain gives a finite representation in the frequency domain and conversely. This means that, if we want a signal with a perfectly rectangular shape in order to optimize the spread of power in the desired bandwidth, this signal will be of infinite duration in the time domain. Conversely, if we want to record in the silicium an UWB signal which must have a finite duration, its spectrum will be infinite. According to this, it is impossible to have a finite UWB signal with a perfectly efficient use of the power in the spectrum. The best that can be achieved is to use a signal that have an infinite duration and an infinite spectrum but with most of its power focused both into a small duration time in the time domain and in a small bandwidth in the frequency domain. Such an UWB signal can be truncated for having a short temporal representation, which is required for

a recording, with also a relatively efficient use of the spectral power. According to results of Chapter 3, we consider the Gaussian impulse a good candidate for the UWB impulse shape. Considering a Gaussian spectrum is a good assumption for having a localized temporal function because the Gaussian is infinite but with a high density in the frequency range of interest (see Figure 11.11 thereafter). The Matlab code for obtaining this result is detailed in Appendix A.2.3.
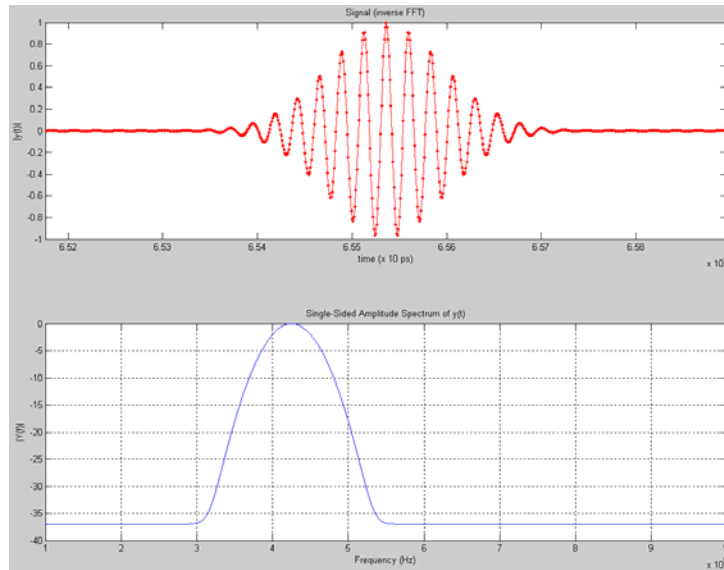
Figure 11.11: The temporal signal which corresponds to an "ideal" Gaussian spectrum.

The temporal signal is a sine wave at 4.25 GHz – which is the central frequency – modulated with a Gaussian envelope (see Chapter 3 for the details). In other words, the signal in the temporal domain is infinite but with locally a high energy density, so the first assumption required to record the signal is to truncate it with a square window in order to remove the negligible samples (see Figure 11.12, Section 3.4 and Appendix A.2.4, lines 15 to 46 for mathematical details). This proves that it is possible to create mathematically and experimentally a signal that fits the desired specifications. More details are given in the article [78].

The processed signal is shown in Figure 11.13 with its corresponding spectrum; the algorithm used here replaces by 0 every sample which is not a local extremum (see Appendix A.2.4, lines 156 to 164). That means that each sample between two points such that the three points make together a monotonically increasing or decreasing curve is replaced by zero.

The last step is to normalize with integer numbers the values of the samples because they will be created by duplication of digital transistors. The value of the sample is made by the summation of the currents flowing across the transistors when they are on (see Figure 11.8, the
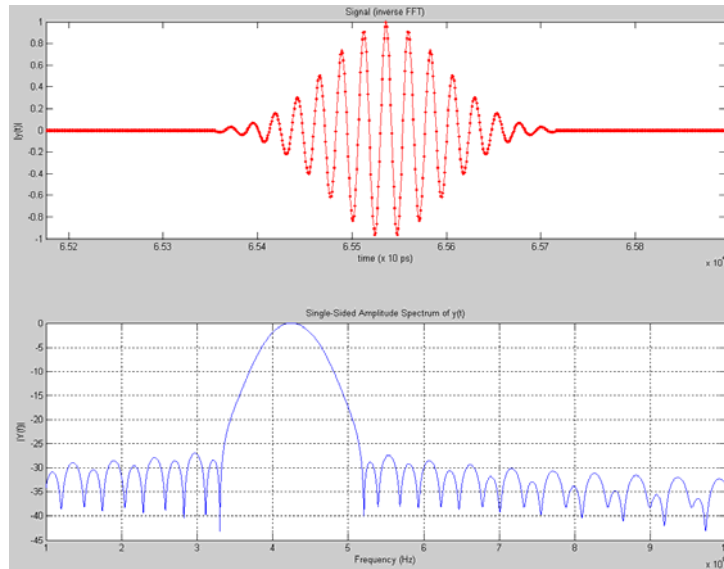
Figure 11.12: The temporal signal which corresponds to a windowed Gaussian spectrum.
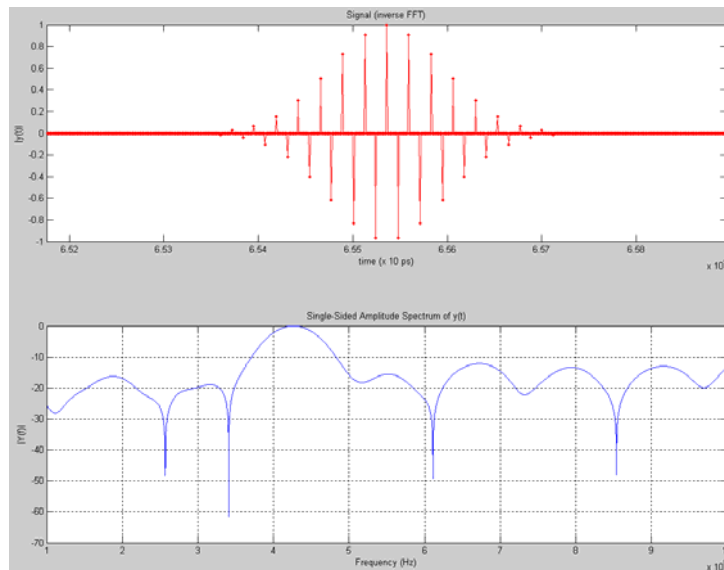
Figure 11.13: The temporal signal which corresponds to a truncated and impulse-like Gaussian spectrum: this is the discrete signal with real sample values.

red switches). The results of this discretization is shown in Figure 11.14 where the maximum value is normalized to 1 in order to compare with previous results (see Appendix A.2.4, lines 81 to 112). In addition, the non-zero samples are repeated three times in order to simulate the duration of the activation pulse that will come from the sampling clock transmission line. The Matlab code for displaying the spectrum of the chosen weights is detailed in A.2.4.
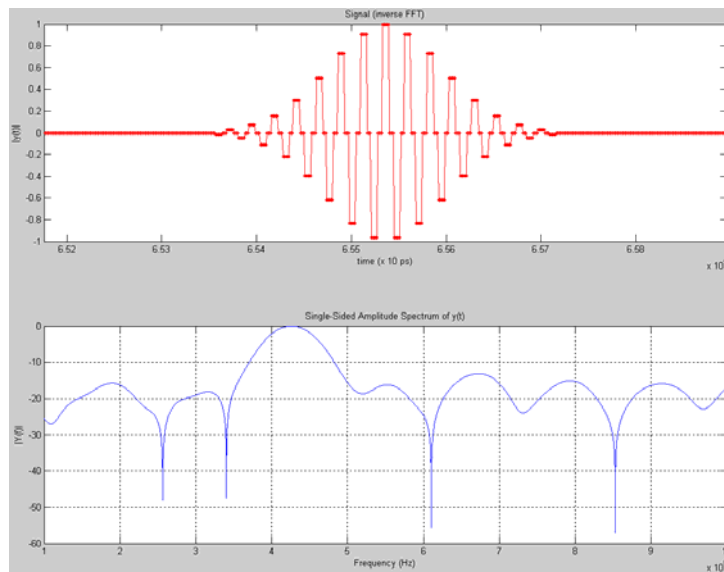
Figure 11.14: The discrete signal with integer sample values.

11.3 Design considerations

We saw that there is a mathematical limitation for generating optimal UWB signals that use efficiently the power. For this reason we chose a Gaussian impulse that optimizes both the time duration and the non-rectangular spectrum shape by concentrating the power in a small interval in the time and the frequency domain. Thus, the mathematically optimal signal (which is to use a true Gaussian with its real values) cannot be obtained as it is with the current physical implementation because the Gaussian we can generate is truncated and its values are rounded. Moreover, in practice, there is also a limitation of accuracy due to the technology constraints and a limitation of power efficiency due to intermediate circuits in the transmitter that consume power that is not found in the UWB signal . According to these points, the main challenge is to imagine a new circuit architecture that is able to transform the incoming power supply current into a very short impulse by reducing as much as possible the use of current flows in the circuit that do not participate directly to the generation of this impulse. This means, for example, that architectures requiring biasing currents and several complex functions must be avoided. Ideally, a low-power transmitter would be a circuit that compels all incoming electrons to go into the output signal path. As it is obviously impossible to do without any loss, the best that can be achieved is to design a circuit that takes place between the power supply and the antenna, as shown in Figure 11.15. In this Figure, most of analog circuits are generally of type A while an ideal circuit would be of type C. In our case, we target circuits of type B where the incoming

power is used in order to be as much as possible a part of the the output signal.
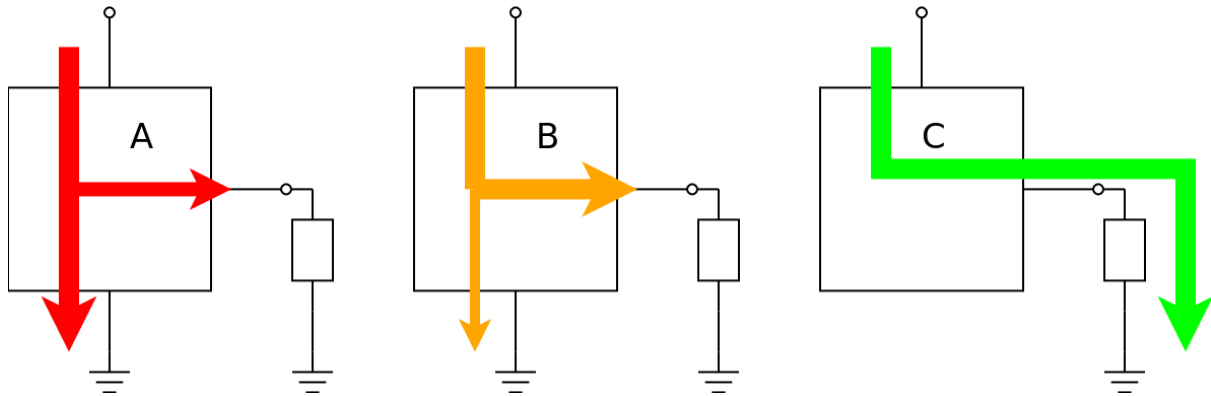
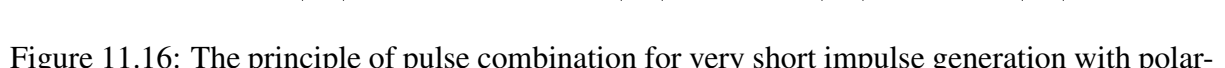Figure 11.15: The energy flow in electronic designs.

11.3.1 The technology

As UWB communications are originally intended to be low-power and to belong to mobile devices, this work focused also on the design of a very low-power UWB transmitter made in CMOS UMC 0.18μm technology. The reasons of the choice of this technology are that it is intended for high-frequency RF integrated designs and relatively cheap (so this helps for prototype experimentation) and it is very well known by our research group (this point is very important for discussing about practical problems that arise during the design process). We use the native UMC 0.18μm technology for the design of prototype n° 1 (see Chapter 12).

Because of limited performance of prototype n° 1, we decided to improve the pulse generation by the use of a balun transformer for prototypes n° 2 and n° 3. However, the conventional tools available in Cadence and in the technology models are not able to manage and design transformers or any other inductive components. For this reason we used *VeloceRF*, a tool from the company *Helic* that works as a plug-in of Cadence.

11.3.2 The design of a prototype: prototype n° 1

We aim to implement the circuit shown in Figure 11.8 with a Gaussian impulse synthesized with 31 samples that are spaced of 117.6 ps. The duration of the signal is thus $0.1176 \cdot 30 = 3.53$ ns, which represents about 3.7 standard-deviation of the Gaussian signal (see Section 3.3). The main challenge here is to find a way to implement the delay lines. Using real transmission lines have the two drawbacks. First, they need to be very long to reach the delay we target and thus the resistive loss is high. Last, Cadence is not a RF tool and another software, like ADS for
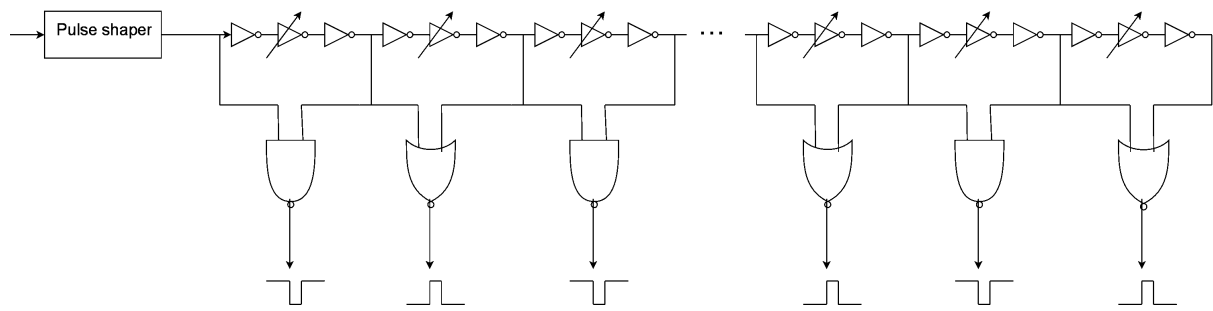
example, is required. The problem is that transmission lines and conventional logic gates work together and, to the best of our knowledge, there is no tool that can simulate simultaneously these two types of designs with both RF transmission lines and logic gates. For all these reasons, we decided to implement the delay lines with chains of inverters where some of them have a variable voltage as power supply in order to tune finely the delay (see Figure 11.16 for the principle).

Figure 11.16: The principle of pulse combination for very short impulse generation with polarity.

Another challenge is generating impulses that are extremely short with conventional logic gates and to delay them with multipoint delay line such that the pulses at the end of the line have similar characteristics as the pulses at the beginning of the line. For this purpose, we send a longer pulse and we used a network of interleaved NOR and NAND gates that use two consecutive delayed impulse to trigger (see Figures 11.17 and 11.18). Thus, it is only the relative delay between two pulses that create the trigger and not the pulse itself so the inverters do not need to have extremely short propagation delay. For generating a positive and negative polarity, we need to connect each NAND or NOR gate at every three inverters; the polarity is naturally produced by the odd number of consecutive inverters (here 3). The NAND gates generate the negative impulse and the NOR gates generate the positive impulse. However, these impulse are amplified by a cascade of inverters for driving the switching transistors and these cascade have an odd number of inverters (they are 3 in Figure 11.16, and 9 in prototype n° 1, see Section 12.3) so driving signals polarity is again changed. In Figure 11.17 the delay can be tuned by changing the inverter in the middle with the semi-interleaved architecture; there is a better approach shown in Figure 11.18 with the interleaved architecture where less inverters are used and smaller delays can be achieved between pulses.

Figure 11.17: The principle of pulse combination with semi-interleaved inverters (Prototype nᵒ 1).

Figure 11.18: The principle of pulse combination with interleaved inverters (Prototype nᵒ 2).

11.3.3   Improvement of prototype nᵒ 1: prototypes nᵒ 2 and 3

The design of prototype nᵒ 1 is a first step to reach our goal to have a very low power UWB transmitter. Unfortunately, exactly the same approach of low-power transmitter is described in a paper (see [79]) and a patent (see [80]) we discovered after sending prototype nᵒ 1 to the foundry. Because of this publication and also because prototype nᵒ 1 does not give the expected results, we design prototypes nᵒ 2 and 3 that are based on the same principle but with the use of a transformer for a simpler architecture and ideally a better performance.

The prototypes nᵒ 1, 2 and 3 are presented sequentially in Chapters 12 and 13 respectively. We present measurements of these three prototypes in Chapter 14 and we conclude Part III on a comparison between our prototypes and similar results in publications.

Chapter 12

The Cadence schematics and layouts of prototype n° 1

This chapter describes our first prototype designed during the summer of year 2009 and sent to the foundry in October 2009. This prototype implements straightforwardly the concepts presented in the previous chapter. As already explained before, the circuit presented here works at the limit of the technology and we mainly intend to demonstrate the concept while performances are a second-step goal. Because we work at a frequency in the limitation range of the technology, the quality of the design of the circuit is more linked to the quality of the computer simulation and the models behind it than only to the knowledge the designer may have on this technology.

There are two kinds of approaches in integrated circuit design. One is based on a deep knowledge of the technology specifications and the behaviour of transistors, and, according to this, to calculate in detail the dimensions of transistors in order to meet the highest performance. The other approach is based on an intuitive knowledge of the technology and transistors' behaviour and to simulate the circuit by improving iteratively the dimensions of transistors until a relatively good and stable performance is achieved. The first approach has the advantage that is gives a complete understanding of the circuit that allows to reach an almost optimal circuit with one or two run of heavy calculations; however it has the drawback to be very complex, sensitive to mistake, and it requires a characterisation of all the parameters of the process that are beyond human ability when we have complex circuit that work at the highest frequency the technology can support. The second approach has the advantage to be empiric - thus its results are close to that obtained in reality - and it does not require absolutely a very deep knowledge

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on the technology but it has the drawback to be a very long process and an optimal result is not guaranteed.

Obviously, these two approaches are opposite extremes and, in practice, every designer has its own methodology that incorporates elements from these two approaches, depending on the kind of circuit (s)he designs and the specification (s)he targets. As we had no previous experience in integrated circuit design before this work, we used our own methodology by applying simple design tenets that hold for any complex engineering project. These tenets are listed below; they all makes a whole that makes the design easy and straightforward.

- The first tenet is the *Divide and Conquer* approach that requires to design a project with a strong hierarchy, like in programming projects. Applying this tenet decreases significantly the amount of work to do and simplifies the design optimization process by doing only local modifications that belong to one cell without the need to modify the remaining part of the project according to it. It is also very efficient in the layout design phase when cells need to be duplicated many times in repetitive structures, as it is the case in this circuit.

- The second tenet is to use calculations and digital circuit theory only as a starting point for the design of the schematic of the cell, and then, to refine it with simulations that take into account the surrounding environment of the circuit (presence of the other cells and parasitics). For this purpose, when we design a cell, we calculate first the ideal dimensions of the transistors according to the theory, then we simulate with ideal components all the parasitics this cell will see in the design, and last, we simulate with other similar cells - and considering post-layout parasitics extraction - in order to ensure the cell behaviour is robust in any situation it may encounter in the design process.

- The third tenet is to design the layout with one different metal layer for every kind of signal and to take advantage of the different layers of metal to introduce in a controlled way the parasitics required for decoupling the power supply and for filtering the output signals. This means also to give the layout of every cell a simple shape that allows building a more complex design by simply juxtaposing the elementary cells like tiles without the need of extra connections in the ideal case.

- The fourth and last tenet is to consider safety margins when simulating for every aspect of the circuit when designing it in order to decrease the risk of technology mismatch and undesired behaviour that cannot be predicted in the simulations, even with post-layout

parasitic extraction. This tenet is one of the most important when we work close to the limitations of the technology.

The design of the cells and of the whole circuit is described in further sections. We present only the final results of the design process of each cell and we avoid to present all intermediate implementations ideas or simulations results required to obtain this cell design because it would be tedious and unnecessary if the tenets listed previously are well understood and applied.

The elementary cells of the design are explained in Section 12.1. Their design determines the speed (and thus the central frequency of the UWB signal) of the final circuit. They are used later to build the complex cells that implement the signal generation in the UWB transmitter, as explained in Section 12.2. The signal is generated with its required power by the weighting circuit which is made of buffers and switches, as described in Sections 12.3 and G.2 respectively. Finally, the complete transmitter is designed in Section 12.4 that is tested by simulation and post-layout extraction in Section 12.5; this section also shows important signals involved in signal generation and their relative timings.

12.1 The elementary cells

The UWB transmitter uses the three elementary logic gates : NOT (inverter), NAND and NOR. The design of the inverter is essential because it determines the dimensions of all the part of the transmitter circuit as it is used here as the reference for the other cells design.

12.1.1 The reference inverter

The reference inverter is an inverter that was not designed until the layout phase but only as a schematic in order to test the technology performance and the relative size of transistor required to drive a similar load. This reference inverter is made with the smallest available size of transistors, as shown in Figure 12.1.

As the mobility of charges in a PMOS transistor are smaller than those of a NMOS, the size of PMOS transistors is increased by a factor of about 2 or 3 for compensating this effect. The test with the reference inverter showed that the best performance is obtained when the size factor is 3. When transistors are small, we decided to implement this size difference by changing the finger number N_f of the concerned transistors. The NMOS has $N_f = 1$ and the PMOS has $N_f = 3$. When the size of transistors becomes too large, the ratio between PMOS
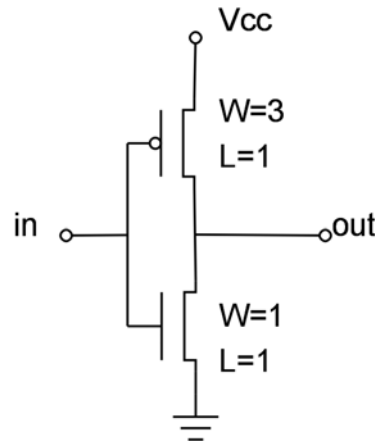
Figure 12.1: The schematic of the reference inverter

and NMOS finger number is not enough because the transistors cannot fit the available place on the layout and Cadence restrict the maximum admissible size of big transistors. In these cases, the ratio is simply made by including it in the width W of the channel of PMOS transistors.

The input capacitance of the reference inverter is proportional to the size of transistors. Let express it as a normalized value :

$$
\begin{aligned}
C_{\text{ref. inv.}} &= L_{NMOS} \cdot W_{NMOS} + L_{PMOS} \cdot W_{PMOS} \\
&= 1 \cdot 1 + 1 \cdot 3 \\
&= 4
\end{aligned}
$$

Simulations showed that this reference inverter is the fastest inverter that can be done with the technology. This is a natural statement as the smallest transistors have the smallest parasitic capacitances, which are the physical limitation to high speed circuit. According to this, we will consider in further sections the reference inverter dimensions to design the other elementary cells we need in the circuit.

12.1.2 The NAND gate

The NAND gate schematic and layout are shown in Figure 12.2. In the layout, Metal layer M_1 is used for power supply and input signals while metal layer M_2 is used for the output signal. The placement of the components is carefully made in order to be the smallest as possible according to the design rules.

We see that there is a distinction between the two inputs because of the speed. The NMOS
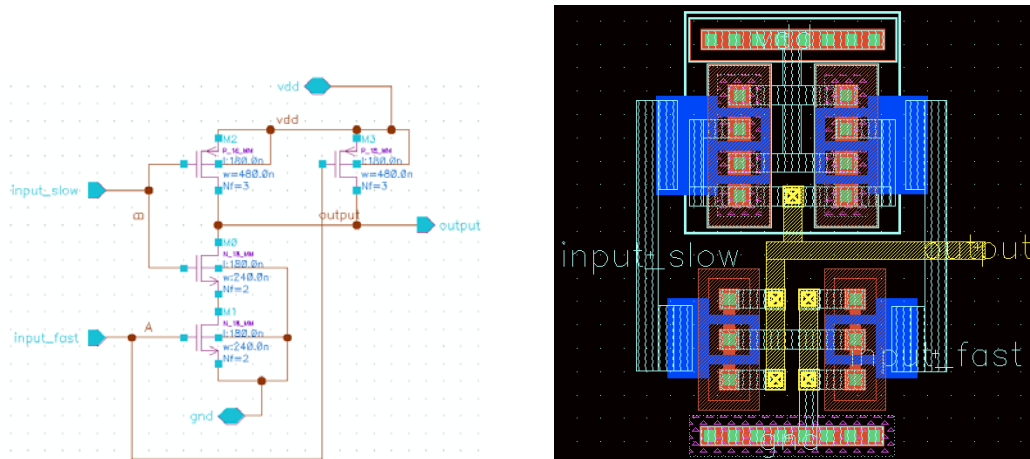
Figure 12.2: The schematic and layout of the NAND gate

transistor that is closer to the ground is faster because the voltage that arrives on its gates is higher than the same voltage arriving on the other NMOS transistor, which has its source connected to the drain of the first NMOS transistor. This distinction will be very important later for ensuring a regular timing in the signals. The rationale in the dimensions of the transistors of NAND gate is the following (see Figure 12.3). We take the reference inverter (A) and duplicate both NMOS and PMOS to have a conventional NAND gate (B); the NMOS width is doubled in order to compensate the fact they are in series. Because of the pulse combination done as explained later, the rising edge of the output need to be very sharp and for this reason the size of the PMOS is also doubled (C) according to simulations. The true dimensions of the transistors are shown in the schematic 12.2.
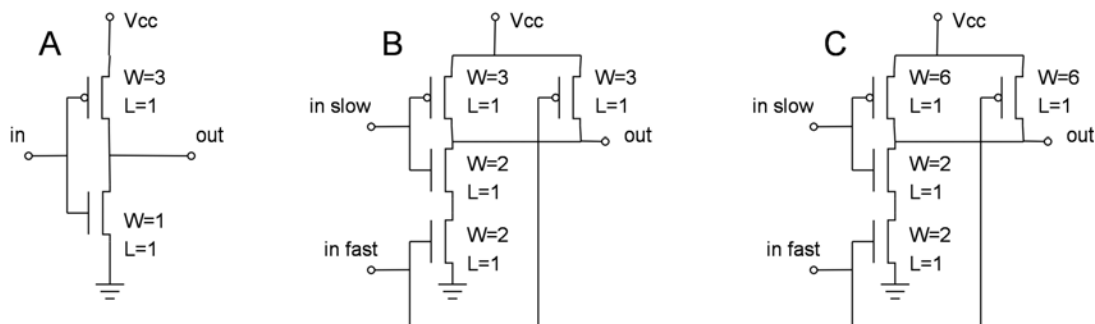
Figure 12.3: Determination of the dimensions of the NAND gate

The input capacitance of the NAND gate is proportional to the size of transistors. Let

express it as a normalized value :

$$C_{\text{NAND}} = L_{NMOS} \cdot W_{NMOS} + L_{PMOS} \cdot W_{PMOS}$$
$$= 1 \cdot 2 + 1 \cdot 6$$
$$= 8$$

12.1.3   The NOR gate

The NOR gate schematic and layout are shown in Figure 12.4. In the layout of the NOR cell, metal layer M_1 is used for power supply and output signals while metal layer M_2 is used for input signals.
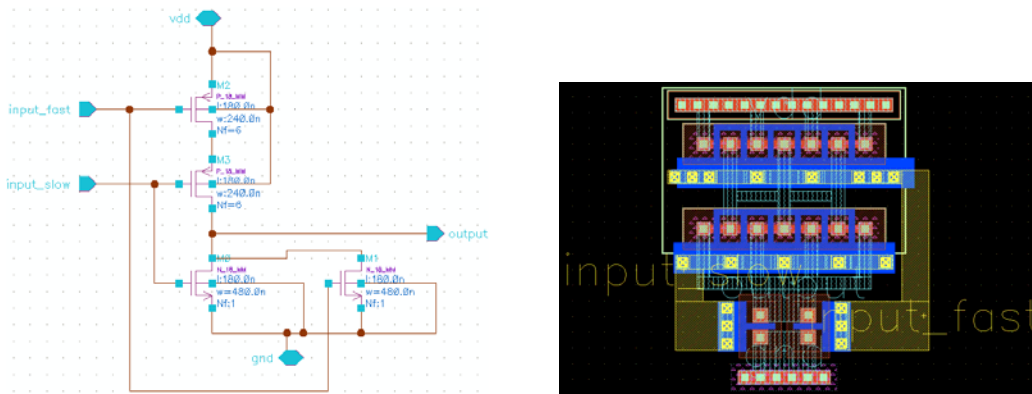
Figure 12.4: The schematic and layout of the NOR gate

The design of the NOR gate is similar to the NAND one and exactly the same remark and rationale applies (see Figure 12.5) excepted that the role of NMOS and PMOS is inverted.
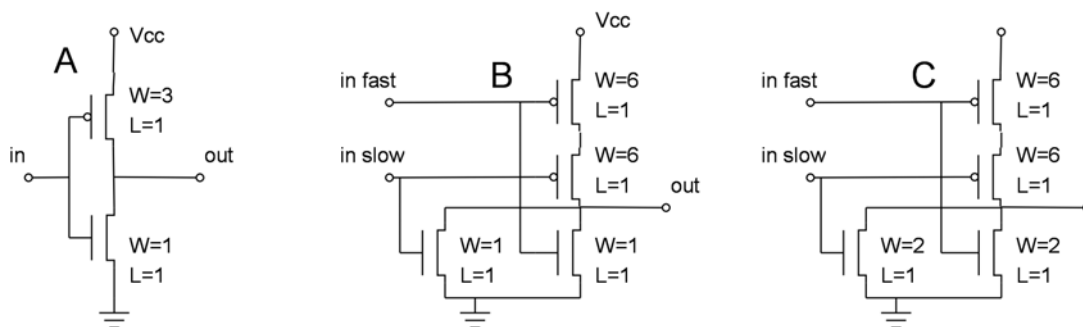
Figure 12.5: Determination of the dimensions of the NOR gate

The input capacitance of the NOR gate is proportional to the size of transistors. Let express

it as a normalized value :

$$
\begin{aligned}
C_{\text{NOR}} &= L_{NMOS} \cdot W_{NMOS} + L_{PMOS} \cdot W_{PMOS} \\
&= 1 \cdot 2 + 1 \cdot 6 \\
&= 8
\end{aligned}
$$

12.1.4   The (real) inverter

This inverter is called *real inverter* - or simply *inverter* because it is used in the circuit but only for a marginal use (see Section 12.2) when the signal arriving at the end of the delay line needs to be amplified for going out of the chip in the *delay line macrocell end circuit*. Figure 12.6 shows the schematic and layout of this inverter. The width of the NMOS transistor is $1.13 \mu m$ because it is the continuation of the geometric serie of transistor dimensions in the *tunable delay line* cell.
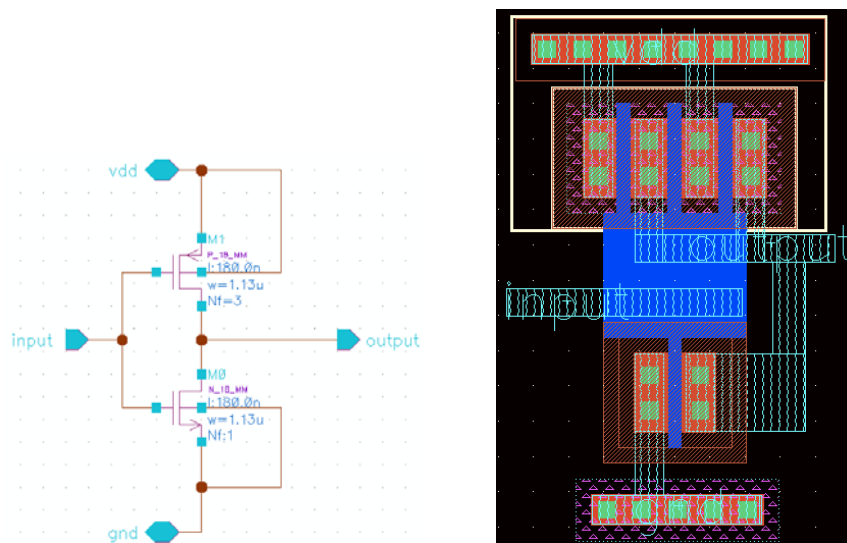
Figure 12.6: The schematic of the inverter

12.2   The complex cells

The complex cells presented in this section are the central parts of the UWB transmitter circuit. They are based on the elementary cells previously explained by incorporating them as they are or, sometimes, by modifying them in order to match new particular specifications. These cells are the *impulse generator* that is used to generate the short impulse that travels along the delay line, the *tunable delay line* that is used to delay the signal with a voltage-controlled delay in order to adjust the sampling frequency, and the *delay line macrocell* that is used to generate the sample impulse by combining the delayed signal with logic gates. The *delay line macrocell* uses a NOR and a NAND gate in order to produce two sample impulses with positive and negative polarity respectively. The delay line is ended with a modified macrocell, the *delay line macrocell - ending cell* in which the NAND gate is replaced by an inverter, the *real inverter* used for amplifying the sampling pulse at the end of the delay line for further measurements if required.

12.2.1   The impulse generator

The impulse generator schematic is shown in Figure 12.7.
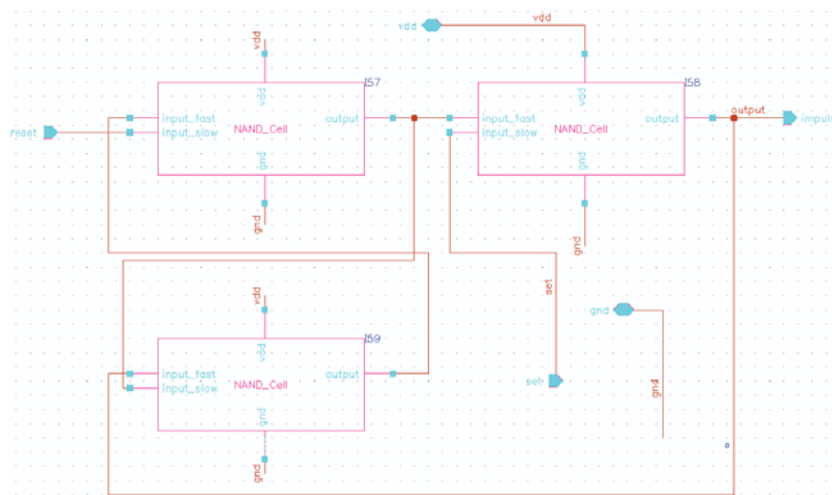
Figure 12.7: The schematic of the impulse generator circuit

The working principle of the impulse generator is the following (see Figure 12.9). The driving signal S that comes from the modulator board (FPGA or microcontroller) arrives to an AND gate for which we assume that the line Q is high. The AND gate's output becomes high and this signal goes to the RS latch which resets its output Q to zero. This switches off the
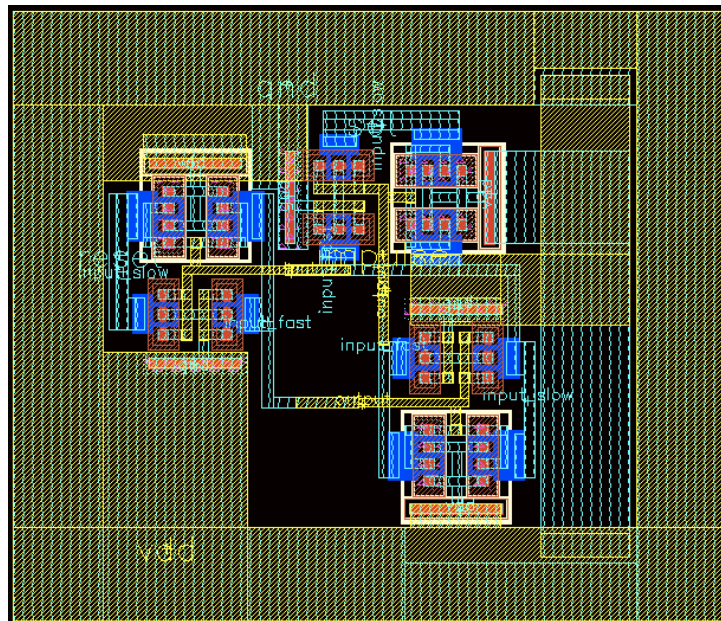
Figure 12.8: The layout of the impulse generator circuit

AND gate's output that falls to zero too. The time needed by the gate to transmit the driving signal and by the RS latch to switch it off is extremely short, about 200 ps, which is enough for the sampling impulse duration we are looking for. When the pulse is sent, the modulator releases the S signal and sends a reset signal R that sets the line Q that is ready for the next impulse generation. Applying De Morgan's rule and elementary logic gate transformations to this principle schematic leads to the schematic of the impulse generator based only on NAND gates, as used in the design. These transformations change not only the polarity of S and R signals (the modulator has to take this into account) but also the polarity of the output impulse. The NAND gates are used here because they have an intrinsic delay that is shorter than the delay of NOR gates. The distinction that was made previously about slow and fast inputs is naturally explained here as fast inputs are used for the feed-back loop in order to increase the travelling speed of the signal. The increase of PMOS transistors size explained in section 12.1.2 for the NAND gate is done for optimizing the short duration of the pulse, and the same modification is done in the NOR gate only for preserving the balance between the signals.

The impulse generator layout is shown in Figure 12.8. The layout is made such that the metal layers dedicated to power supply (M_2 for Vcc and M_1 for ground, as usual) make a natural decoupling capacitor. The three NAND gates are placed such that they are connected with the shortest as possible tracks in order to decrease the parasitics.
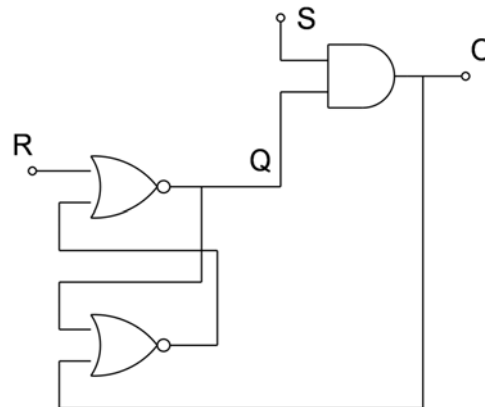
Figure 12.9: The working principle of the impulse generator circuit

12.2.2   The tunable delay line

The tunable delay line schematic and layout are shown in Figure 12.10.
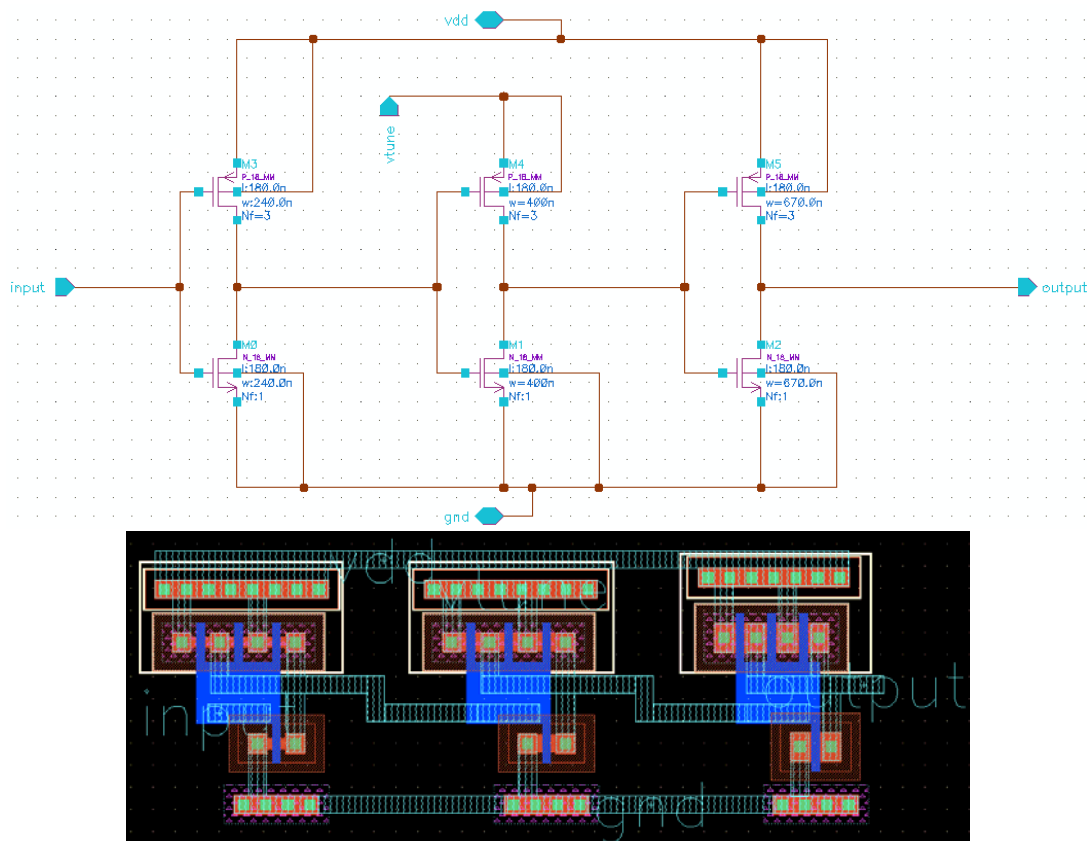
Figure 12.10: The schematic and layout of the tunable delay line circuit

For determining the dimensions of the inverters that belongs to the tunable delay line, let

n be the number of stages (here $n = 3$) and w be its fan out (here $w \approx 5$). Considering the reference inverter as the reference load, the value of w is estimated (see 12.2.3 for the circuit):

$$
\begin{aligned}
w &= \frac{C_{\text{ref. inv.}} + C_{\text{NAND}} + C_{\text{NOR}}}{C_{\text{ref. inv.}}} \\
&= \frac{4 + 8 + 8}{4} \\
&= 5
\end{aligned}
$$

We neglect here the logical effort because we changed the size of NAND and NOR gates from what they should normally be and we determine by simulation that the optimal value for that w is much smaller anyway (see below). However, assuming that the inverter is the reference inverter and that the length of all transistors (either PMOS and NMOS) is $L = 180$ nm, we can express the width W of the transistors of stage i by the following formula :

$$
\begin{aligned}
W &= 0.24 \cdot \sqrt[(n-1)]{w^i} \qquad [\mu\text{m}] \\
\\
&= 0.24 \cdot \sqrt{w^i}
\end{aligned}
$$

In theory, the geometric progression between two consecutive stages is $\sqrt{5} = 2.24$. In practice, i.e. in simulation, we see that we have better results when the geometric progression is reduced to 1.68. This reduction of the ratio value is the *Vtune* voltage that is intended to be variable and which changes the commutation threshold of the intermediate inverter. With this value, we have $W_1 = 0.24$, $W_2 = 0.40$ and $W_3 = 0.67$. In the case of the real inverter, we have $W_4 = 1.13$ (see 12.1.4) according to this geometric progression.

12.2.3   The delay line macrocell

The schematic of the delay line macrocell is shown in Figure 12.11.

The delay line macrocell contains two tunable delay line and two gates (a NOR and a NAND) for the impulse generation by pulse combination. The use of NOR and NAND is simply for generating two impulses with opposite polarity. The layout of the delay line macrocell is shown in Figure 12.12.

12.2.4   The delay line macrocell - the ending cell

The schematic of the delay line macrocell (ending cell) is shown in Figure 12.13.
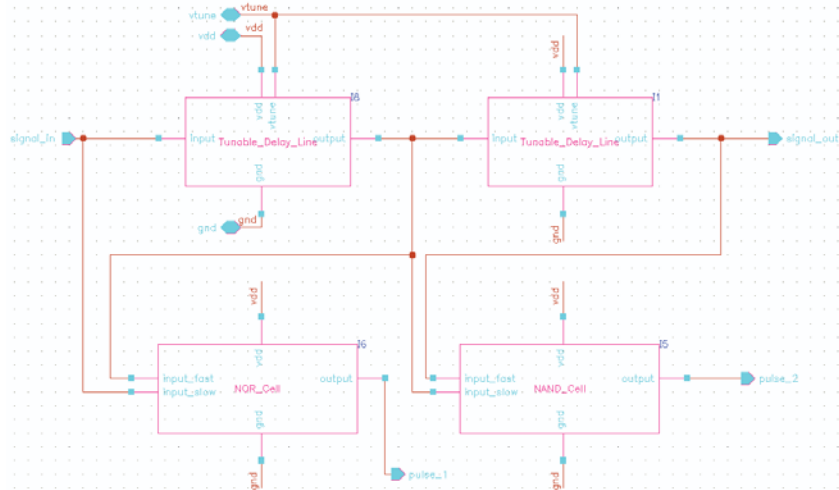
Figure 12.11: The schematic of the delay line macrocell circuit
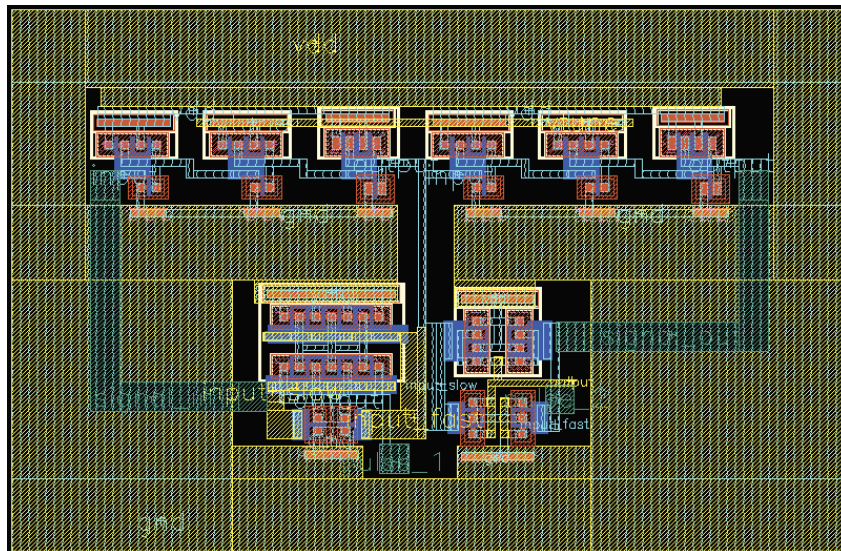
Figure 12.12: The layout of the delay line macrocell circuit
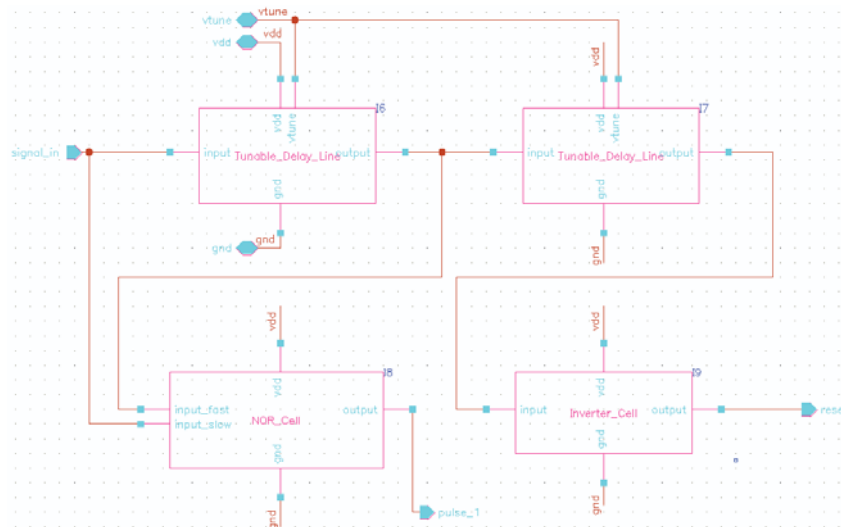
Figure 12.13: The schematic of the delay line macrocell end circuit

The delay line macrocell - ending cell is used to terminate the delay line cascade. It contains two tunable delay lines and one NOR gates for the impulse generation by pulse combination. The NAND that was in the normal cell is replaced in the ending cell by an inverter (the real inverter) because at the end of the delay line there is the need of only one impulse. The layout of the delay line macrocell is shown in Figure 12.14.
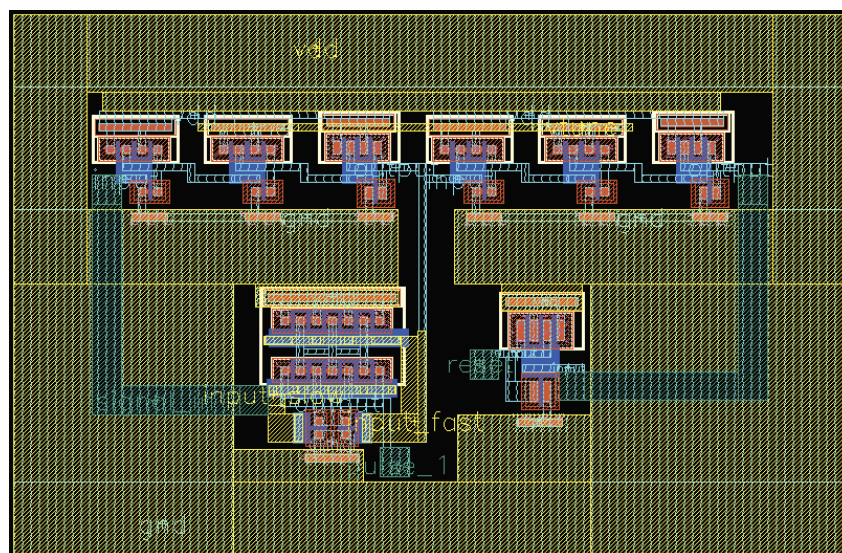
Figure 12.14: The layout of the delay line macrocell end circuit

12.3   The buffers and switches

The buffers, described all in detail thereafter, play an important role in the circuit because they have to assume several roles and to fulfil contradictory constraints:

- to produce the power required for driving the corresponding switch;

- to respect the geometric progression in term of inverter size that ends with the weight of the corresponding switch in order to guarantee a correct timing and impulse shape;

- to use as efficiently as possible the available power;

- to have an odd number of stages in order to respect the polarity of the driving signal for the corresponding NMOS- or PMOS-based switch;

- to have all the same number of stages in order to preserve the timing of impulses.

The challenge when designing the buffers was to determine the total number of stages for all buffers, considering the fact that they may have a weight that lies from 2 to 109; the complete set of values is $S = \{\ -2\ ;\ 3\ ;\ -5\ ;\ 8\ ;\ -12\ ;\ 17\ ;\ -24\ ;\ 33\ ;\ -43\ ;\ 55\ ;\ -67\ ;\ 80\ ;$ $-91\ ;\ 99\ ;\ -105\ ;\ 109\ ;\ -105\ ;\ 99\ ;\ -91\ ;\ 80\ ;\ -67\ ;\ 55\ ;\ -43\ ;\ 33\ ;\ -24\ ;\ 17\ ;\ -12\ ;\ 8\ ;$ $-5\ ;\ 3\ ;\ -2\ \}$. These values are obtained by experimenting the best rounding to the nearest integer of values calculated in Appendix A.2.4, lines 15 to 46. This wide range of weights values makes the buffers to be the weakest parts of the circuit in terms of power consumption because heavy-weighted buffers need normally more stages than light-weighted ones to ensure a correct current driving ability. This makes thus that most of the buffers have more stages than really required. This means that light-weighted buffers will consume more power than really required. The problem is even worse when considering that there are more light-weighted buffers than heavy-weighted ones. This situation is not much in accordance with a low-power design that intends to use the available power with a very high efficiency.

The best that can be done at this phase of the design is to determine the number of stages n such that it is minimal, odd and with a progression ratio that can achieve at the end a weight of 109 by ensuring a transmission of the short impulse without any visible degradation of their shape. By simulation, we found that $n = 9$ is an acceptable value (with $n = 7$, the signal is degraded for the weight 109). At this point, the discussion about another choice of weights that

could decrease the span of weighting values remains open.

For determining the dimensions of the inverters that belongs to the buffer, let n be the number of stages (here $n = 9$) and w be the weight of the buffer. Assuming that the first cell of any buffer is the reference inverter and that the length of all transistors (either PMOS and NMOS) is $L = 180$ nm, we can express the width W of the transistors of stage i by the following formula :

$$W = 0.24 \cdot \sqrt[(n-1)]{w^i} \qquad [\mu\text{m}]$$

For example, the buffer of weight 109 has the following progression (with the rounding imposed by Cadence) : 0.24, 0.43, 0.78, 1.39, 2.51, 4.50, 8.10, 14.55 and 26.16. It is easy to check that the geometric progression between two consecutive stages is $\sqrt[8]{109} = 1.7975$. As for the reference inverter, the PMOS and NMOS charge mobility is compensated by the number of fingers N_f.

The switches are simply made by duplicating as many times as required by their weight a simple transistor layout. The shape of the duplicated transistor is chosen to be as much as possible a square or rectangle that can easily be inserted in the final layout. They are also driven by a buffer that has the same weight that corresponds to the number of duplicated transistors. The details on buffers and switches is presented in Appendix G.

12.4   The complete circuit

The schematic of the whole circuit is shown in Figure 12.15.
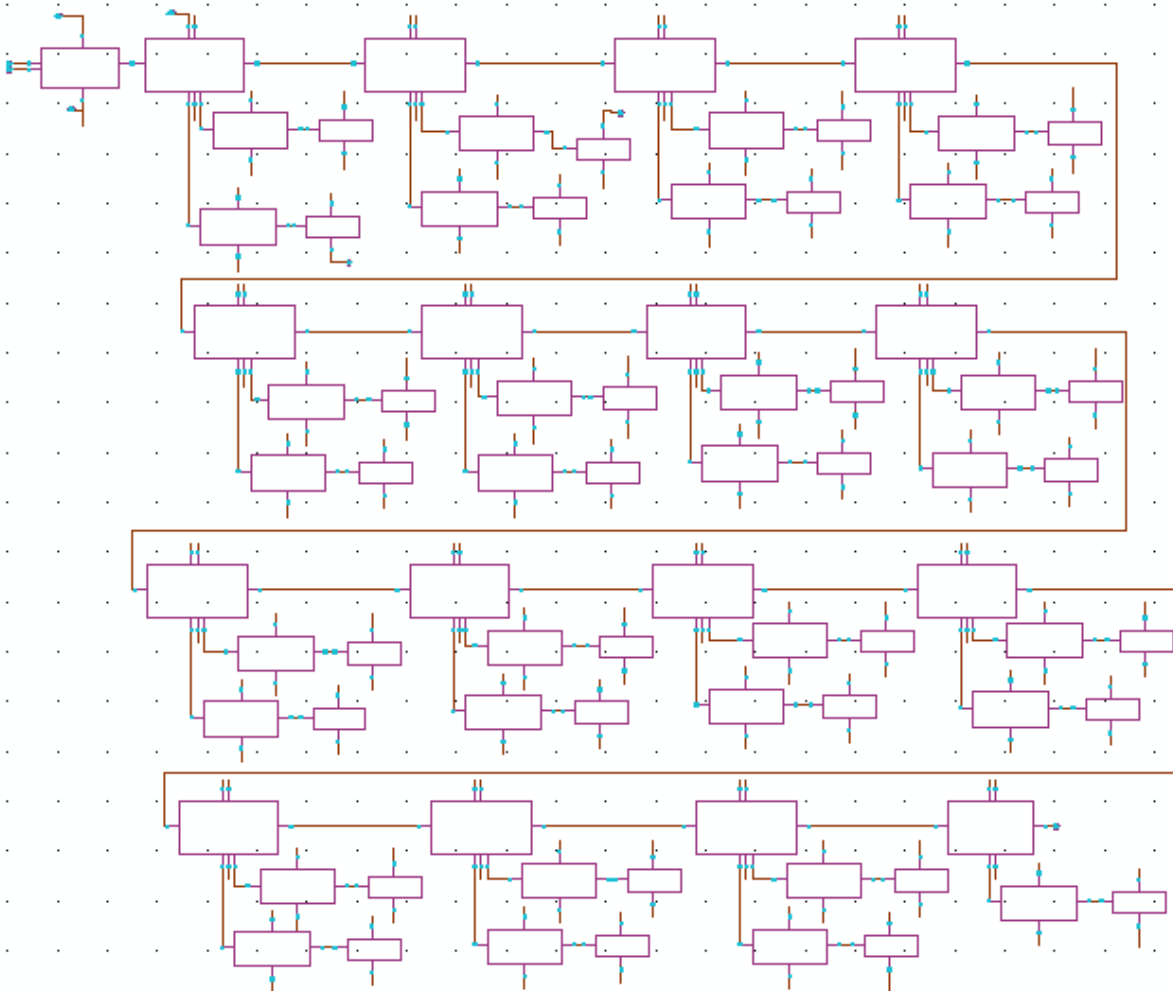
Figure 12.15: The schematic of the complete circuit

Although we cannot see the details of boxes in Figure 12.15, we distinguish clearly the functions of the parts of the circuit that we described previously. The layout of the whole circuit is shown in Figure 12.16 and a detailed view is shown in Figure 12.17. The layout is compact and uses only about one third of the available area and which could be used for another UWB circuit, if available.
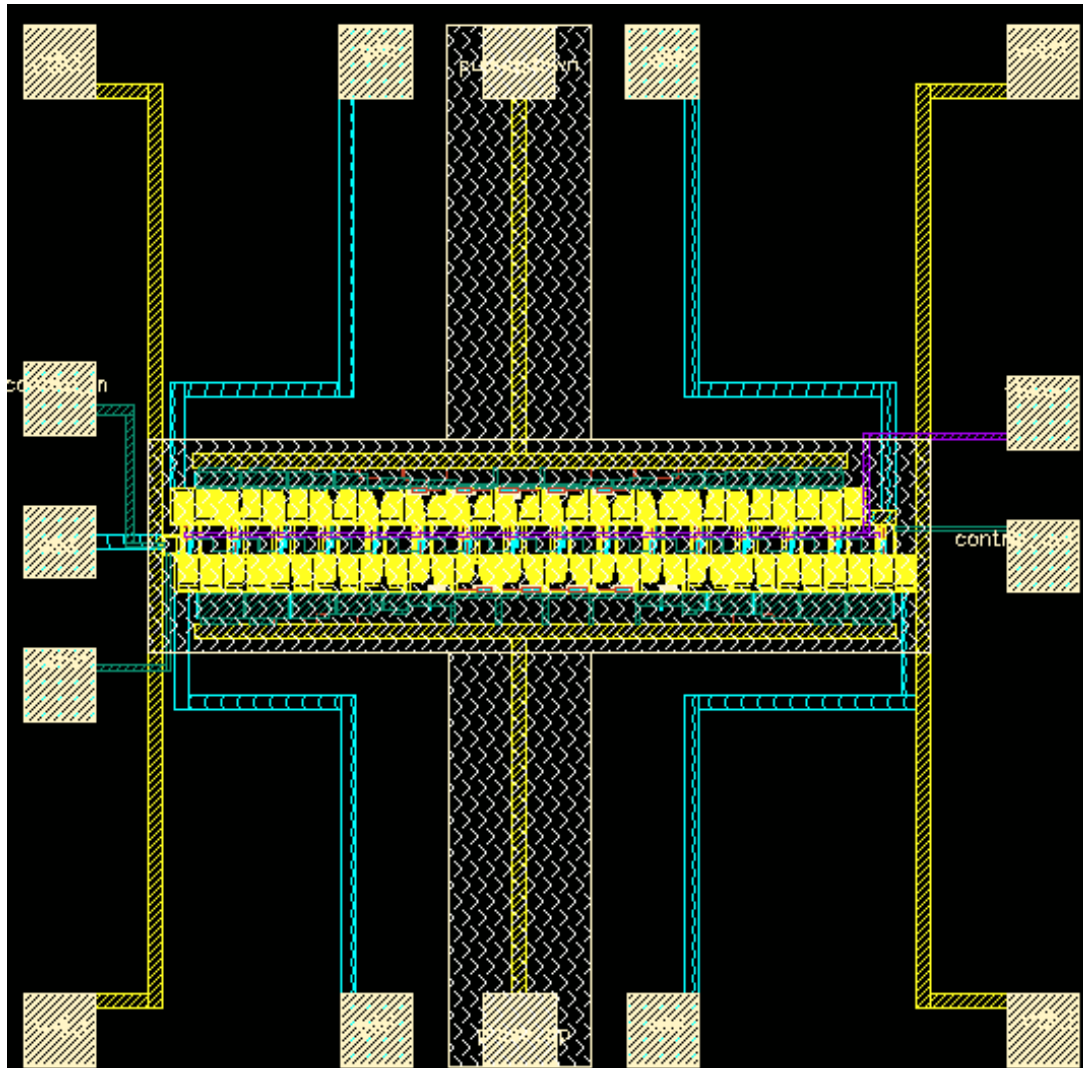
Figure 12.16: The layout of the complete circuit
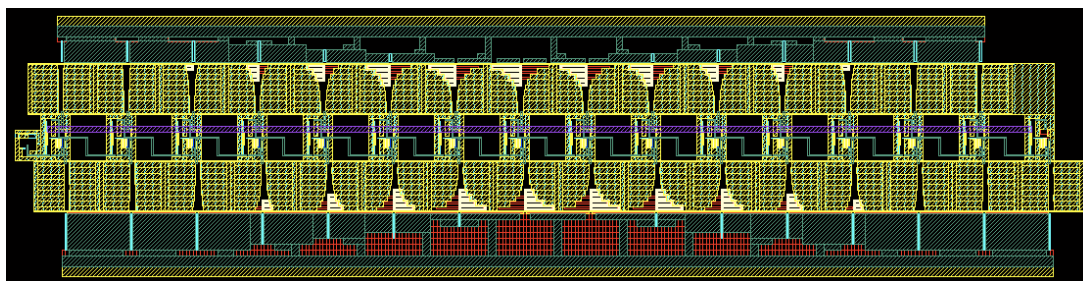
Figure 12.17: Detail of the active part

12.5   Test of Prototype nº 1

The schematic of the test circuit is shown in Figure 12.18.
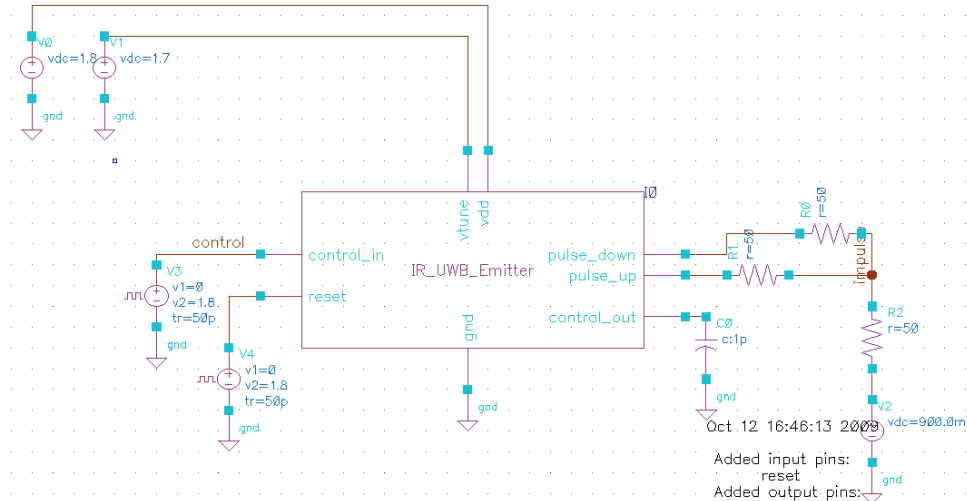
Figure 12.18: The schematic of the test circuit

Some simulation results are shown in Figures 12.19, 12.20 and 12.21. The simulations differ only on the Vtune voltage that is 1.8V, 2.0V and 1.7V respectively. With 1.8V and 2.0V we see the signal Pulse Down is distorted. This is because the delay line has a too short time delay and pulses travel too fast; the pulse combination has the time to happen but the PMOS transistors of the *Pulse Down* line have not the time to react when they are too big. With 1.7V, however, the recombination works perfectly (at least in simulation).
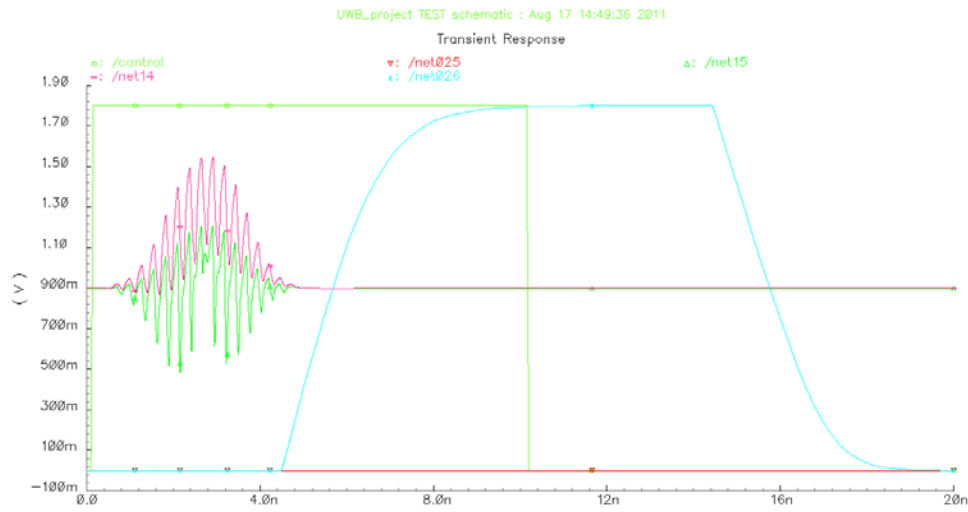
Figure 12.19: The simulation of Prototype nº 1 with $Vtune = 1.8$ V.
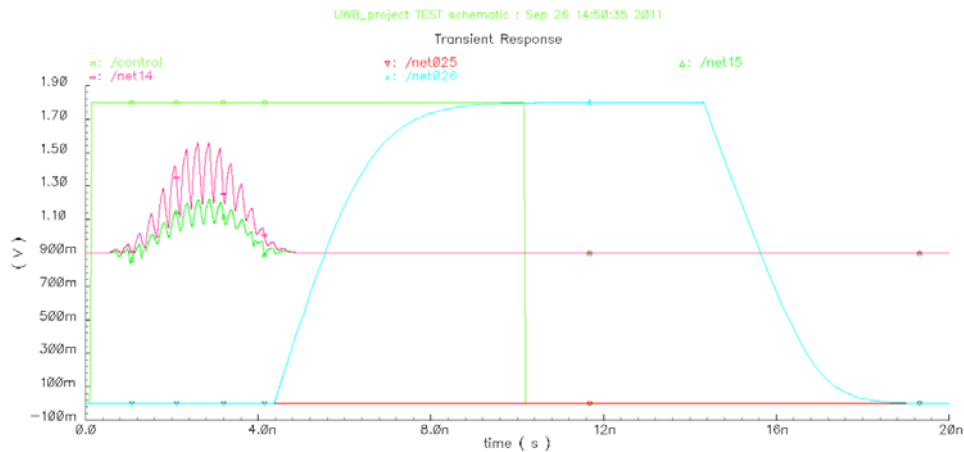
Figure 12.20: The simulation of Prototype nº 1 with $Vtune = 2.0$ V.
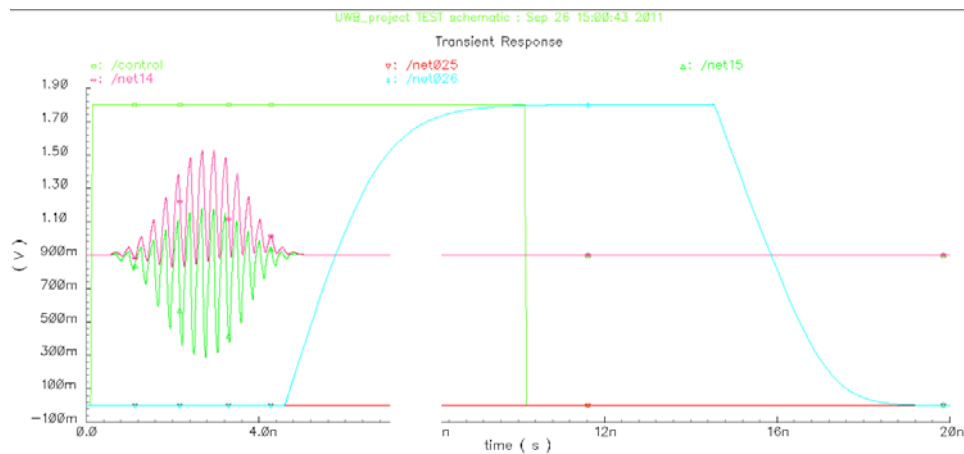
Figure 12.21: The simulation of Prototype nº 1 with $Vtune = 1.7$ V.

The current consumption of Prototype n⁰ 1 is shown in Figure 12.22.
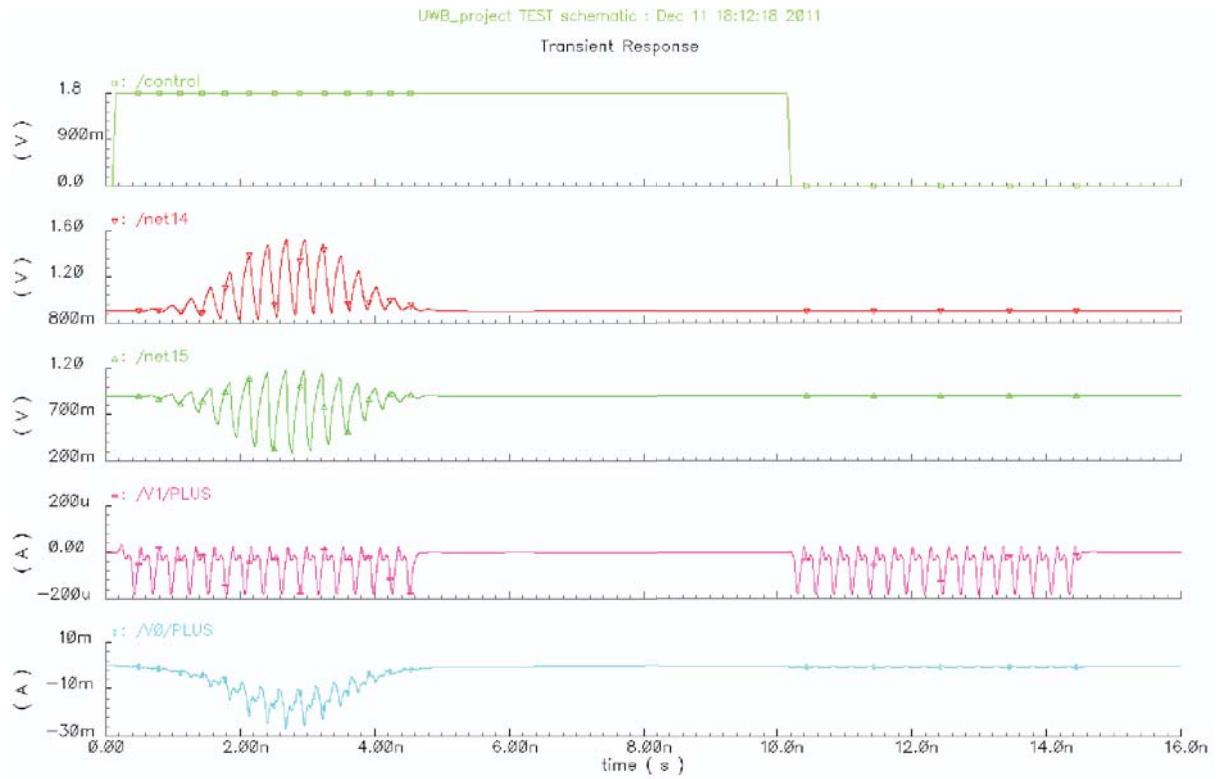
Figure 12.22: The current consumption of Prototype n⁰ 1 with $Vtune = 1.7$ V.

According to the simulations, the current is $I_{Vdd} = 20$mA, $I_{Vtune} = 0.2$mA and $T_P = 3$ns, as shown in Figure 12.22. The energy per pulse is thus :

$$E_{pulse} = Tp \cdot (I_{Vdd} \cdot Vdd + I_{RFpower} \cdot V_{RFpower}) = 110\text{pJ/pulse}.$$

Chapter 13

The Cadence schematics and layout of prototypes nᵒ 2 and nᵒ 3

The prototype nᵒ 1 showed a straightforward implementation of the UWB low-power architecture presented in Chapter 11 and that is measured further in Chapter 14. The measurements and experimental validation of prototype nᵒ 1 confirm the limitations that are exposed in Chapter 12 from simulation results.

The most severe limitation of prototype nᵒ 1 is the balanced outputs *pulse up* and *pulse down* that require an external balun transformer with a common pin at $\frac{Vcc}{2}$. Producing this voltage require at least a voltage divider that consumes unnecessary power. A way to circumvent the use of $\frac{Vcc}{2}$ is to use a balun transformer with three windings, two as primary for *pulse up* and *pulse down* respectively and one as secondary for the output UWB signal. Such a balun is difficult to find and takes place on a PCB that is intended for a low-power and very small device for mobile applications. Another annoying limitation, as already exposed in section 12.3, is the span of weighting values (from 2 to 109) that compels the buffers to have 9 stages of inverters in order to work properly. The measurements of prototype nᵒ 1 show that a so wide span of values is useless because the degradation of precision caused by the mismatch and the variations of process fabrication is greater than the precision of the signal reproduction expected by using so precise values for the samples.

According to these observations, we decided for prototype nᵒ 2 to reduce the span of sample to only 8 values and to integrate a balun transformer into the die for performing internally all the pulse combination process. Because of the balun, the polarity of the UWB samples can be created in a passive way and the topology of the circuit can be strongly simplified (see

Figure 13.1 for the generic principle). The delay line is simplified by the number of inverters that does not need to be odd for generating the polarity and the use of only NAND gates for combining pulses instead of NAND and NOR gates, as done in prototype n° 1. As the buffers drive directly the balun transformer; the switches are no more needed. The prototype n° 2 was designed during the summer of year 2010 and sent to the foundry in October 2010.
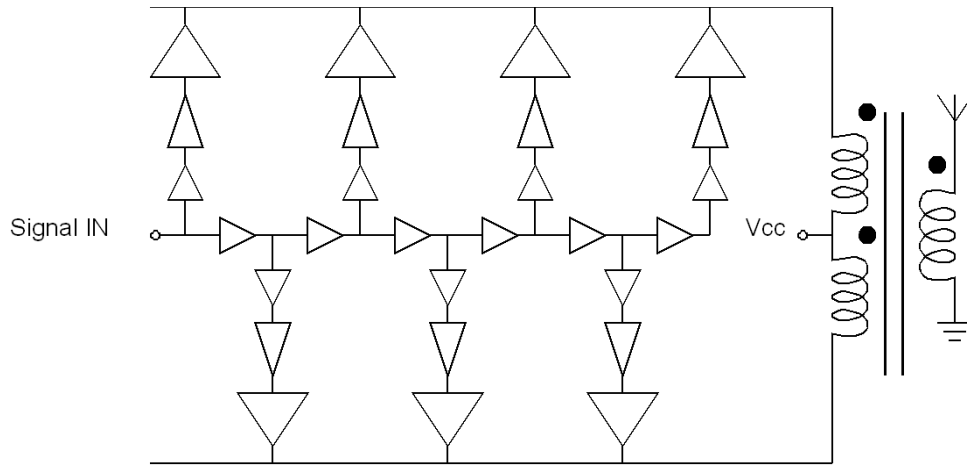
Figure 13.1: The principle schematic of the prototype n° 2

This prototype uses less than half of the available place on the die and we finished the layout several weeks before the scheduled tape-out date. We thus decided to use this time to design on the same die another prototype, the prototype n° 3, which is another way to implement the improvement made with the prototype n° 2. We explained in Chapter 11 that an ideal circuit would use integrally the power it receives on the power supply line for generating the UWB signal. This means that such a circuit should have the load (i.e. the antenna in series with the power supply line). The goal is thus to design a circuit such that it's the glitches produced by the commutations of logic gates that produces the UWB pulses. What kind of process these logic gates are implementing can, in that sense, be ignored provided that the commutations they generate in the power supply line is the desired UWB signal. In practice, we keep the idea of an impulse that travels along a delay line (see Figure 13.2 for the generic principle) and we add a control on the duration of the pulse by switching on or off some cells of the delay line (see red boxes in Figure 13.2) by activating or not Vcc_1, Vcc_2, ..., Vcc_i. Thanks to this, we can control all the parameters of the signal : the power by modifying Vcc, the central frequency by modifying Vcc_i, $\forall i$ and the bandwidth by powering switching of some Vcc_i.
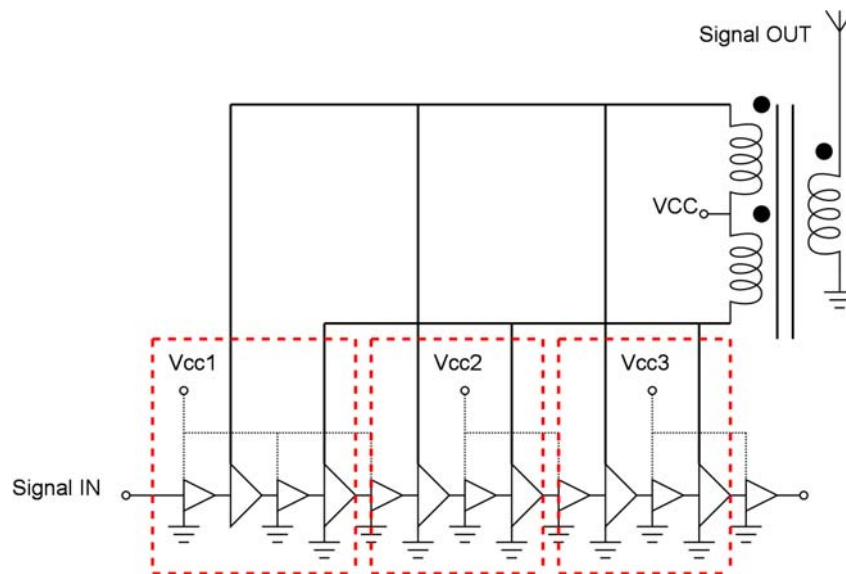
Figure 13.2: The principle schematic of the prototype nº 3

13.1   The prototype nº 2

The prototype nº 2 elements are shown thereafter. As some of them are the same as for prototype nº 1 (the impulse generator and the NAND gate) or only slight modification of some of them (inverter cells 1 and 2), only minimal explanation is given because these are the same that were already for prototype nº 1 elements, unless fundamental changes occur (the buffers).

13.1.1   The impulse generator

The impulse generator is exactly the same as for prototype nº 1 (see section 12.2.1) and the comments already made remain unchanged. The schematic and layout are shown again in Figure 13.3.

13.1.2   The NAND gate

The NAND gate is exactly the same as for prototype nº 1 (see section 12.1.2) and the comments already made remain unchanged. The schematic and layout are shown again in Figure 13.4.

13.1.3   The inverter cell 1

The inverter cell 1 (more precisely it is a buffer) is used only once, at the output of the impulse generator to give more power to the signal. Its schematic and layout are shown in Figure 13.5.
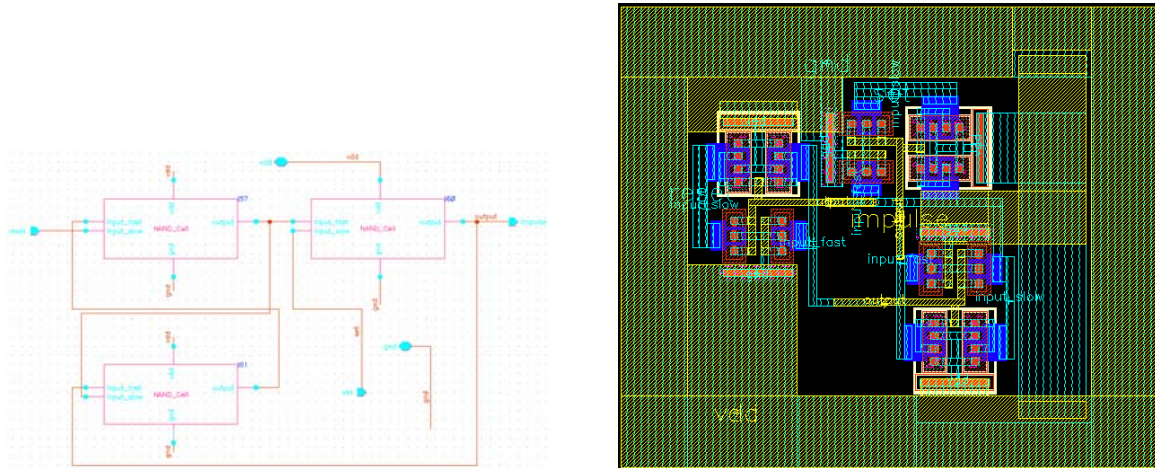
Figure 13.3: The schematic of the impulse generator
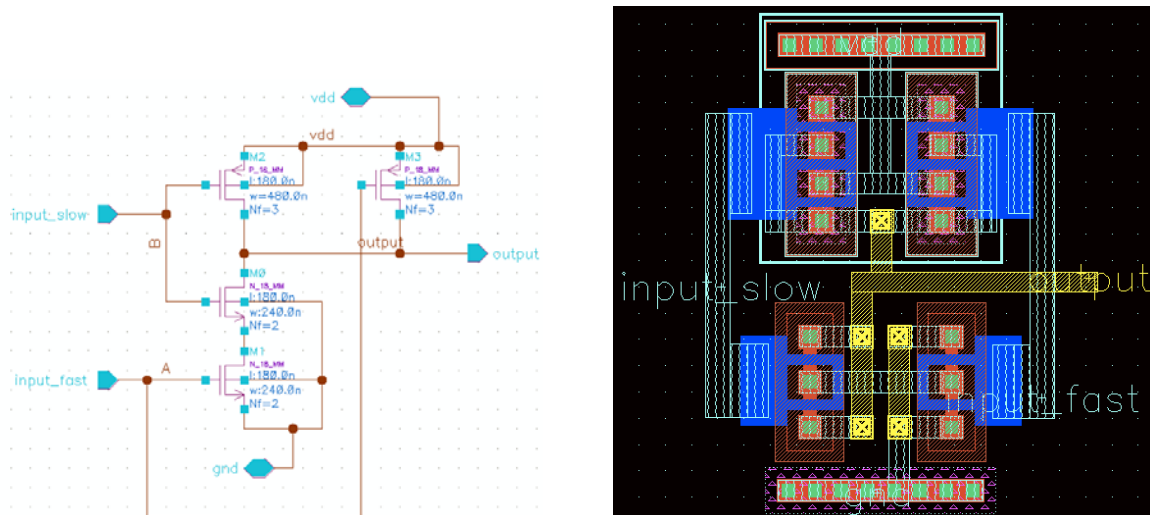
Figure 13.4: The schematic of the NAND gate

It is designed to drive an *inverter cell 2* and one NAND gate input.

13.1.4   The inverter cell 2

The inverter cell 2 is the inverter cell used for the delay line. As the polarity is done with the balun transformer, there is no need to have a specific feature for producing positive and negative impulse. Thus, only one stage is required because of the small fan out it has to drive. Its schematic and layout are shown in Figure 13.6. It is designed to drive an *inverter cell 2* and one NAND gate input, as it was for cell 1.
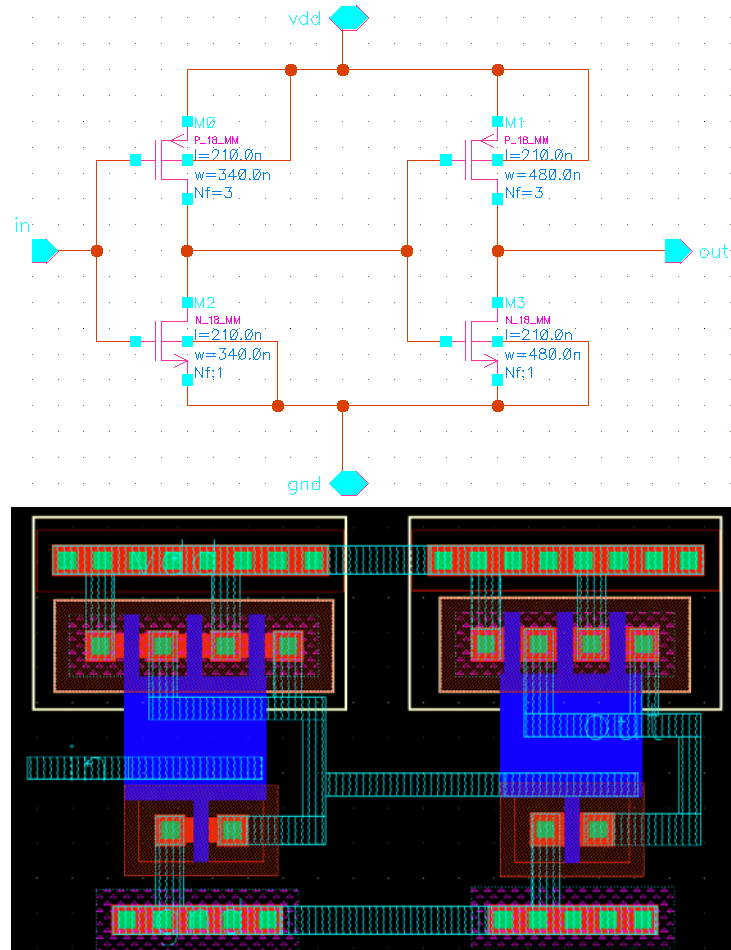
Figure 13.5: The schematic and layout of the inverter cell 1
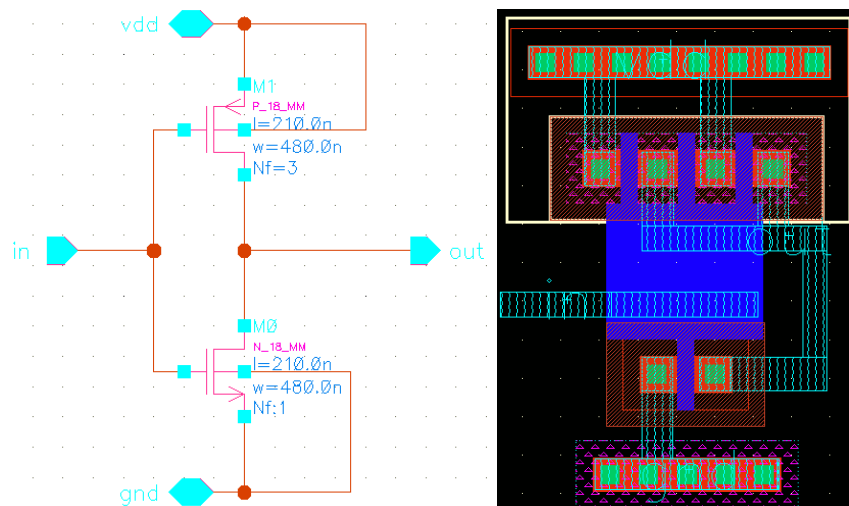
Figure 13.6: The schematic and layout of the inverter cell 2

13.1.5   The buffers

The buffers design and their constraints were already presented in detail in Section 12.3. However, in prototype nᵒ 2, the buffers have several differences with those of prototype nᵒ 1. As the balun transformer creates the polarity of the UWB impulse, only NMOS switches are required (as NMOS are faster than PMOS for the same size) and this simplify also the design of the buffers as follows :

- there is no more the need to have an odd number of stages because we design the delay line such that the sampling impulse has the good polarity for driving the switch transistor;

- the switch transistor is now part of the buffer cell;

- as we have only a span of 8 for the weights, only 5 inverter stages are required instead of 9 as for prototype nᵒ 1;

- we use different finger number for squaring the shape of the transistors in the layouts.

Because the rounding made in Prototype nᵒ 1 can be simplified with lower values without degrading too much the original signal, the complete set of values is now $S = \{\, 1 \,;\, -1 \,;\, 1 \,;\, -2 \,;\, 2 \,;\, -3 \,;\, 4 \,;\, -5 \,;\, 6 \,;\, -7 \,;\, 7 \,;\, -8 \,;\, 8 \,;\, -8 \,;\, 7 \,;\, -7 \,;\, 6 \,;\, -5 \,;\, 4 \,;\, -3 \,;\, 2 \,;\, -2 \,;\, 1 \,;\, -1 \,;\, 1 \,\}$. This rounding requires also less samples and the signal is shorter. These values are obtained by experimenting the best rounding to the nearest integer of values calculated in Appendix A.2.4, lines 15 to 46. In order to guarantee enough power at the output with the balun, we experiment simulations to determine the size of the switch transistors. We found that a width of 100μm, which is the highest value authorized by DRC, for the highest weight buffer 8 gives good results. The other buffers have thus their switch transistor size modified according to their corresponding weight (from 12.5μm to 100μm). The intermediate stage inverter have their transistors designed according to the geometric progression law exposed in section 12.3. The switch transistor is counted as equivalent to a 6th stage of inverter in the calculation of the geometric ratio. The schematics and layouts are shown in Appendix H.

13.1.6   The balun transformer

The balun transformer is produced by the *VeloceRF* software from Helic. For this, the following procedure is followed.

We choose Multi-spiral structure and the operating frequency is set to 4.25 GHz. The primary and secondary are set to 50Ω, then press OK button. The software starts calculating
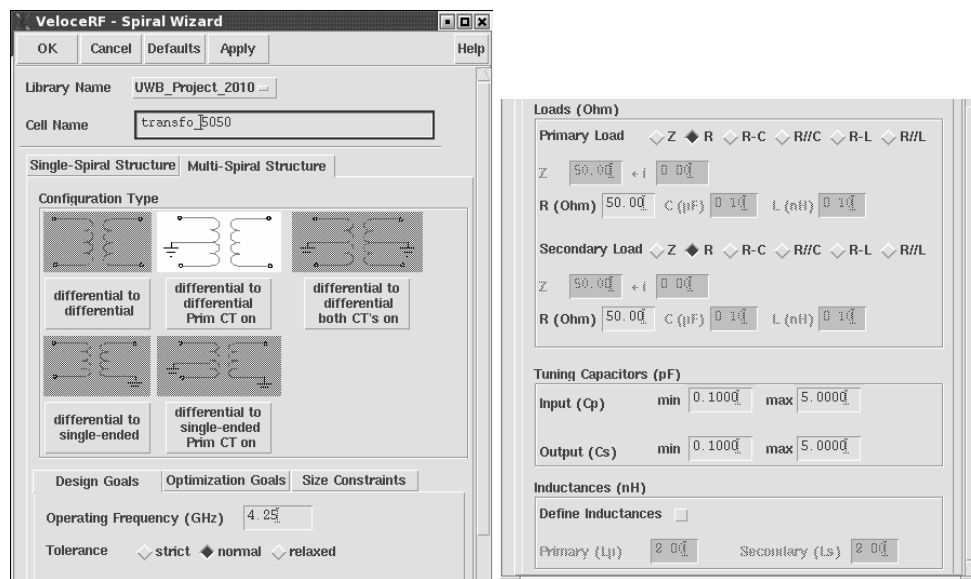
Figure 13.7: The Helic tool dialog box

the transformers and propose a dialog box to choose one when there are several solutions (see Figure 13.8).

Figure 13.8: The different balun transformers proposed by VeloceRF

Then, the software finalizes its calculation and propose the symbol and the layout of the transformer that can both be used as any other component in the design (see Figure 13.9). VeloceRF produces also the model files required for electric simulations.

13.1.7   The complete circuit of prototype n⁰ 2

The schematic of the whole UWB transmitter, prototype n⁰ 2 is shown in Figure 13.10. As the resolution of this schematic is not high enough to have a view in the details, we can refer to Figure 13.11 for a detailed view on the left part and right part. We see the cascade of inverters with interlaced points for driving the gate that generate the short impulses, and the
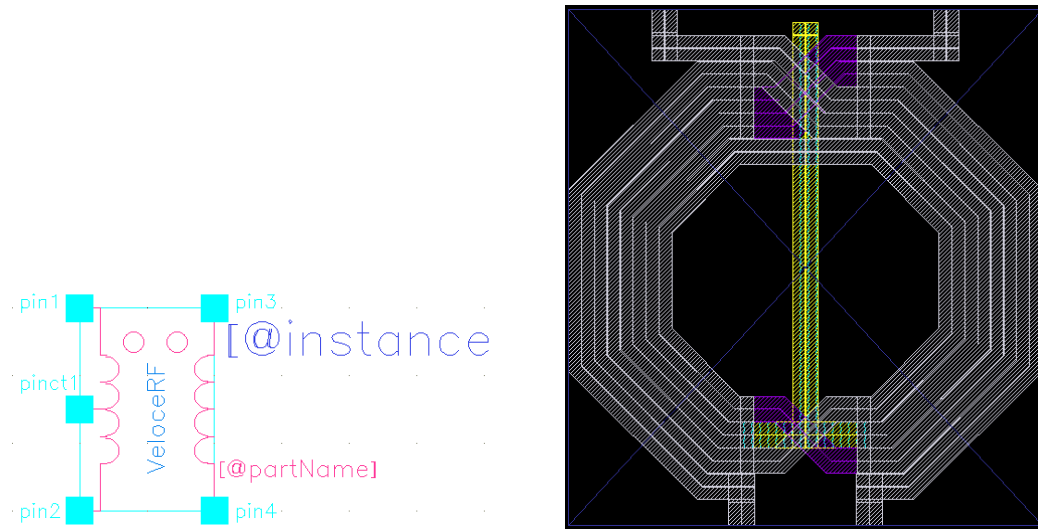
Figure 13.9: The symbol and the layout of the balun transformer

balun transformer that combines the impulse for generating the UWB pulse. The layout of the whole UWB transmitter, prototype nº 2 is shown in Figure 13.12. This layout takes place at the bottom of the die.
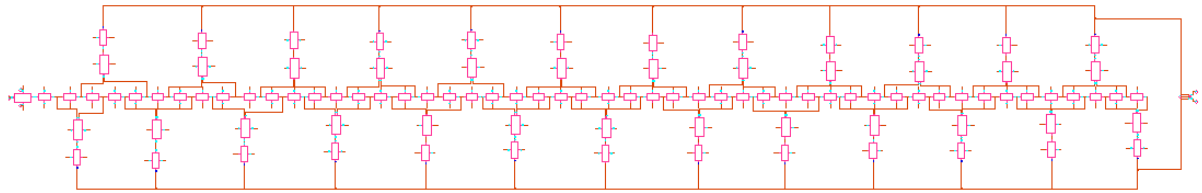
Figure 13.10: The schematic of the complete prototype nº 2 of UWB transmitter

13.1.8   Tests of the Prototype nº 2

The prototype nº 2 circuit is tested by simulation (with the use of VeloceRF tool in Cadence), according to the test circuit shown in Figure 13.13, and the result is presented in Figure 13.15. We see that the UWB impulse lasts about 3 ns as expected with a Vdd voltage (for the logic) of 2.0V and a $V_{RFpower}$ voltage of 1.8V. The UWB impulse shape changes according to the value of these voltages; the central frequency of the impulse (or of the oscillations) is measured to be about 4.25GHz as expected.

According to the simulations, the current is $I_{Vdd} = 18$mA and $I_{RFpower} = 60$mA, as shown
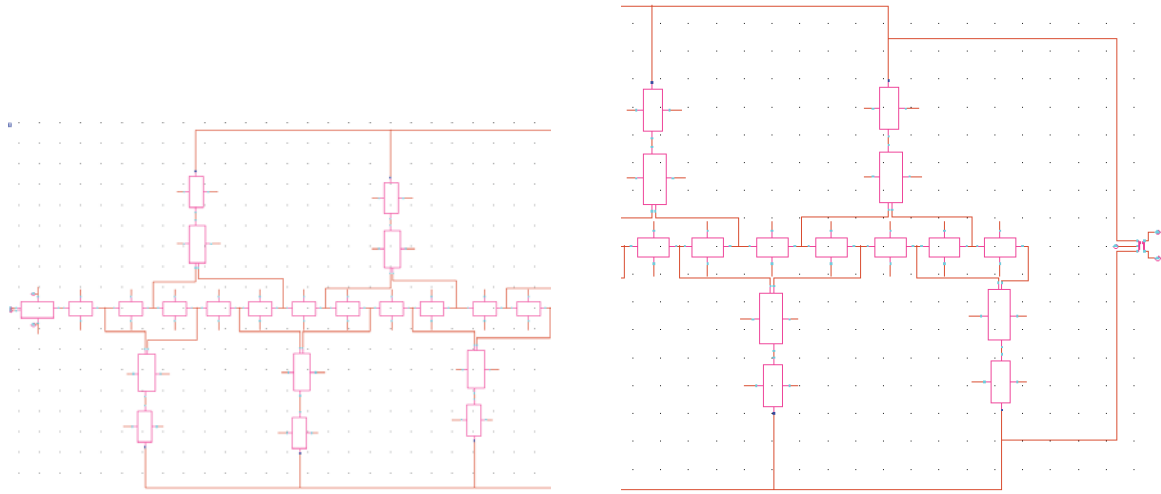
Figure 13.11: The schematic of the complete transmitter - left and right part
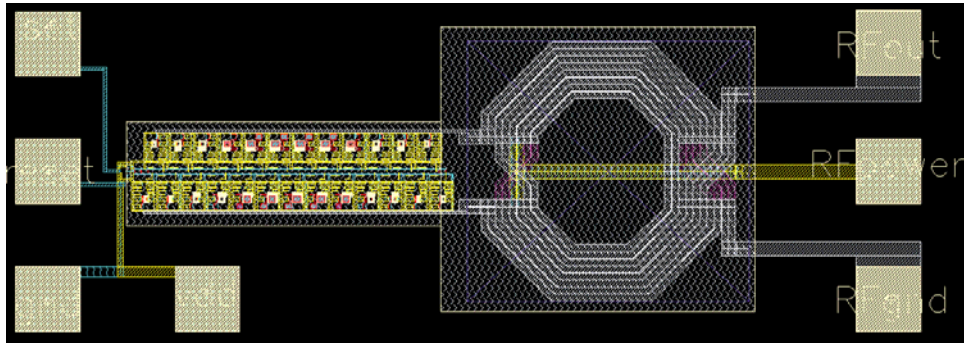
Figure 13.12: The layout of the complete transmitter
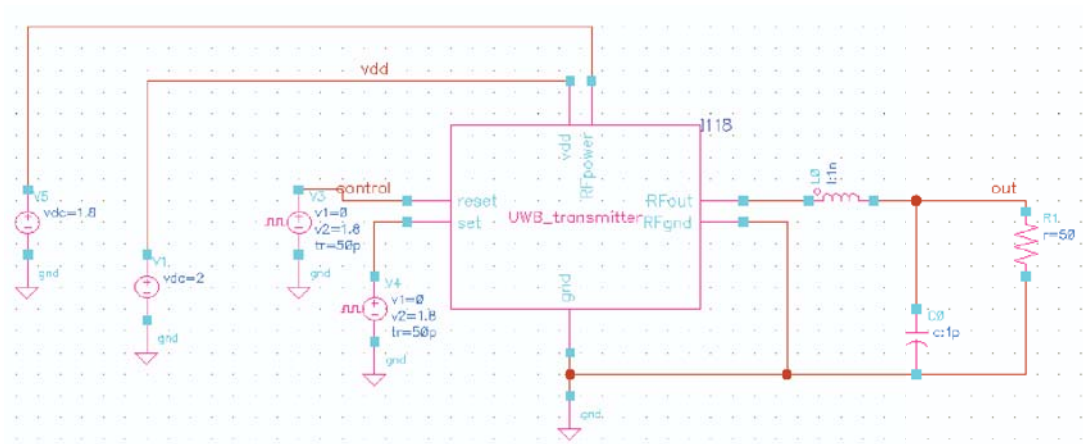
Figure 13.13: The Test schematic for prototype nº 2.

in Figure 13.14. The energy per pulse is thus :

$$E_{pulse} = Tp \cdot (I_{Vdd} \cdot Vdd + I_{RFpower} \cdot V_{RFpower}) = 430\text{pJ/pulse}.$$
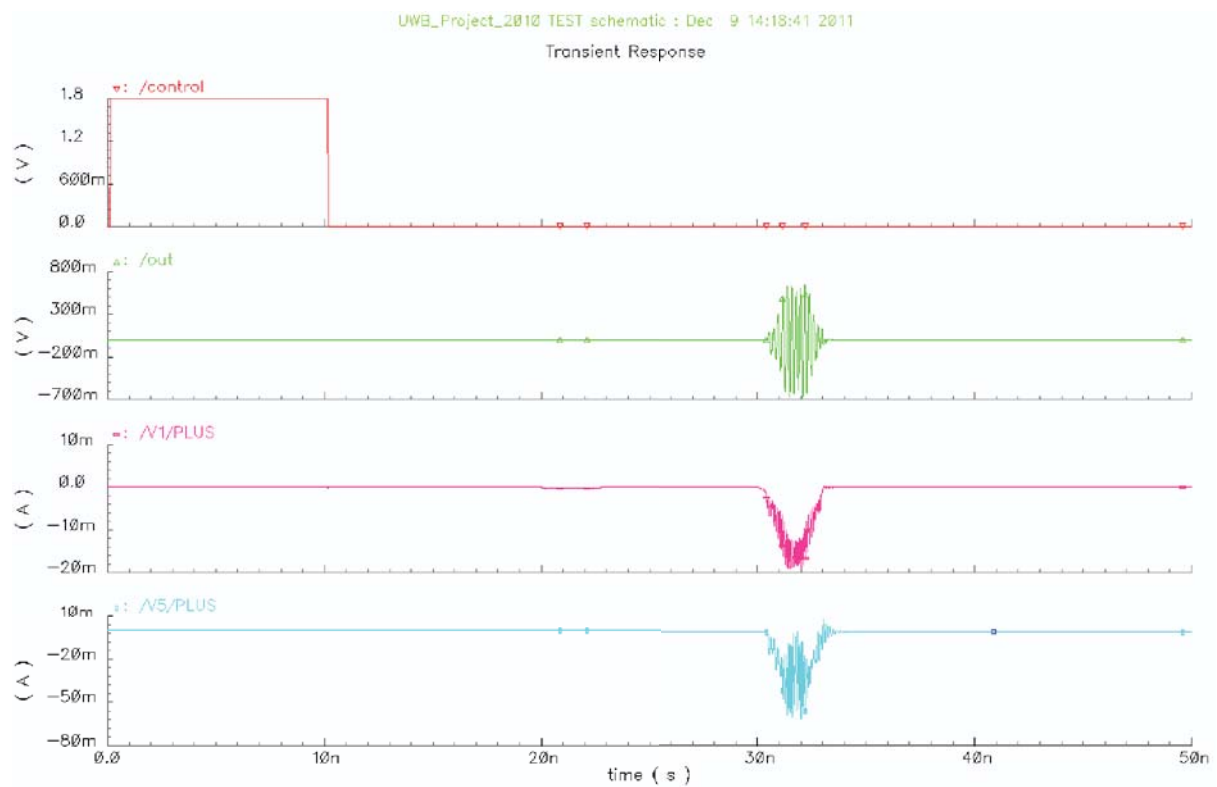
Figure 13.14: The current consumption for prototype nº 2.
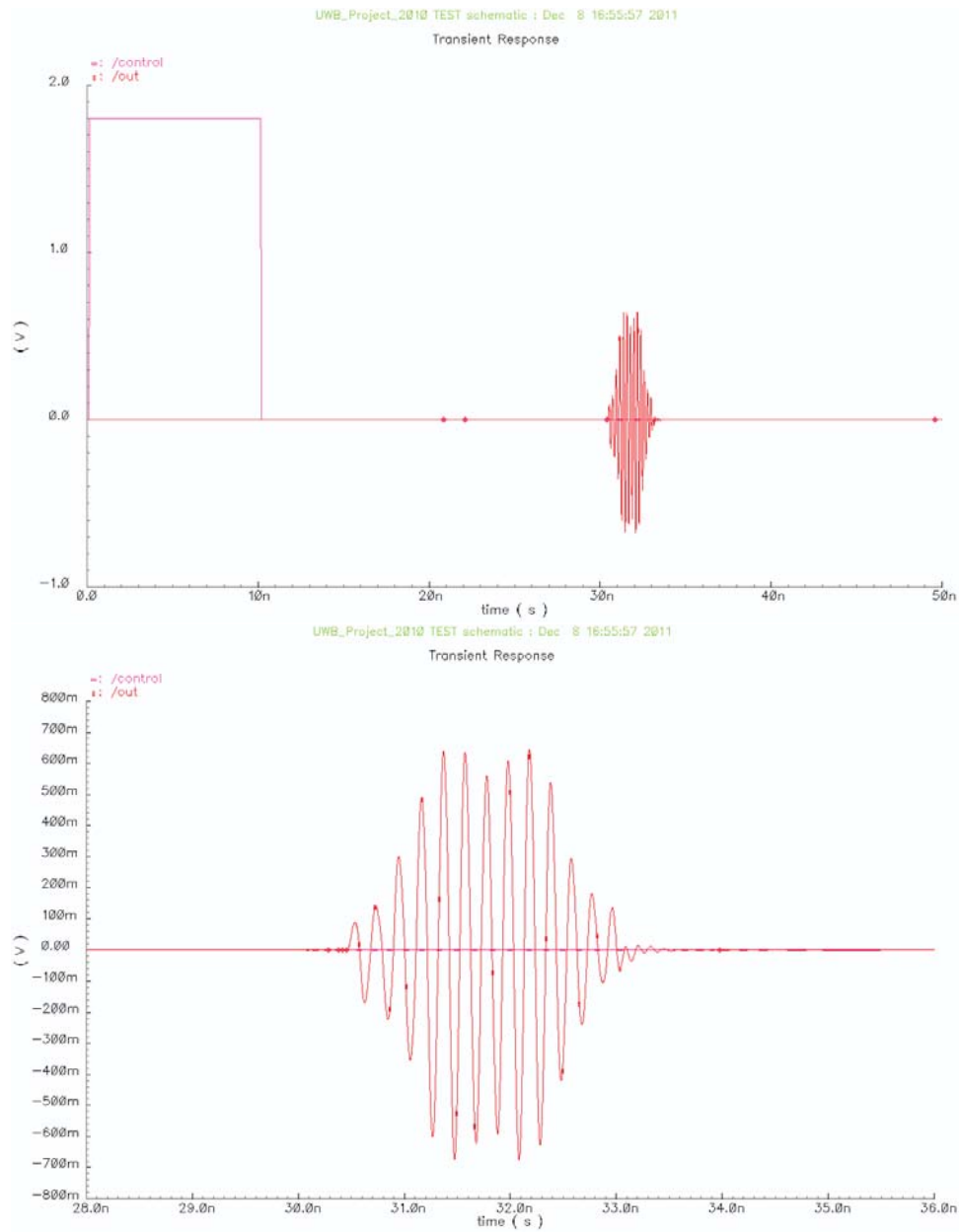
Figure 13.15: The Test simulation results for prototype nº 2.

13.2   The prototype n° 3

13.2.1   The small inverter

The small inverter's schematic and layout, are shown in Figure 13.16, is used to drive the big inverter presented thereafter. Its power supply voltage is controlled independently from the main Vcc such that the delay it introduces can be finely tuned. Its transistors dimensions are obtained by simulation into the completely designed circuit. They need to be small enough to have a negligible power consumption but not too small for avoiding too large delays between two pulses that cannot ensure a 4.25 GHz central frequency.
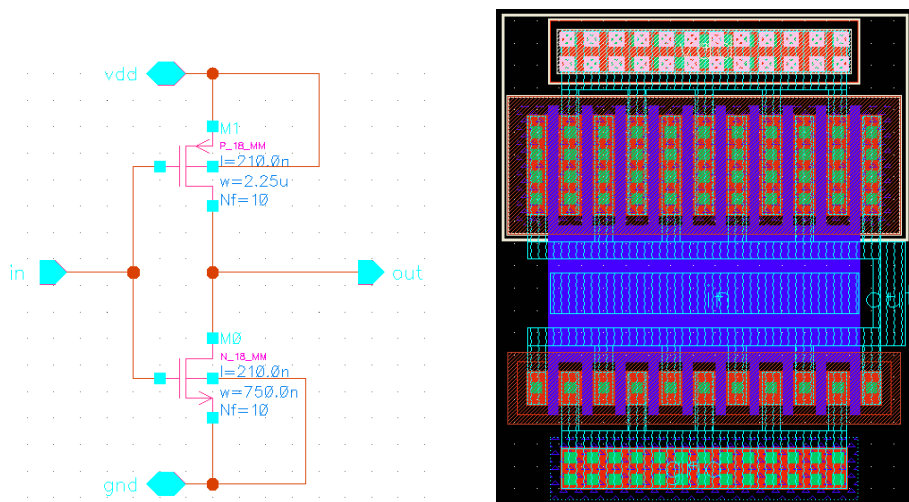
Figure 13.16: The schematic and layout of the small inverter

13.2.2   The big inverter

The big inverter's schematic and layout that are shown in Figure 13.16 is used to drive the next small inverter such that the glitch made in its power supply can produce a UWB impulse collected by the balun transformer and sent to the antenna. Its power supply voltage is controlled through the balun transformer Vcc mid tap such that the power of the impulse can be finely tuned. Its transistors dimensions are obtained by simulation into the completely designed circuit. They need to be big enough to produce a clear UWB impulse but not to big for avoiding too large delays between two pulses that cannot ensure a 4.25 GHz central frequency.
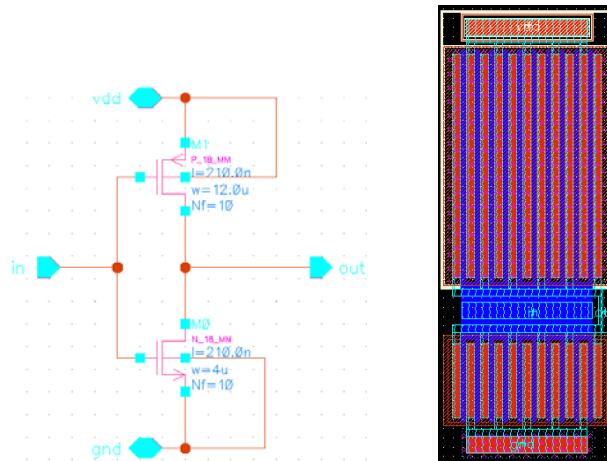
Figure 13.17: The schematic and layout of the big inverter

13.2.3   The delay cell

The delay cell's schematic and layout are shown in Figure 13.18, is a cascade of two pairs of one small and one big inverter. The first pair produces the positive edge of the UWB signal by consuming current in one direction of the primary coil of the balun while the second pair produces the opposite edge of the UWB signal from the other side of the primary coil. This cell is the fundamental unit of the prototype nᵒ 3. It can be duplicated as much as desired, depending of the bandwidth of the UWB signal. It is also intended, in prototype nᵒ 3, to control all these cells independently by powering them or not in order to tune the bandwidth of the signal.
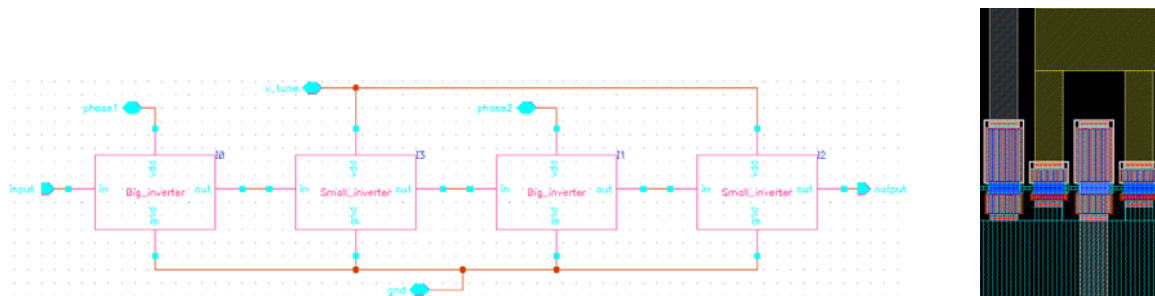
Figure 13.18: The schematic and layout of the delay cell

13.2.4   The balun transformer

The balun transformer for prototype nᵒ 3 is exactly the same as for prototype nᵒ 2 (see section 13.1.6) and the comments already made remain unchanged. The symbol and layout are shown

again in Figure 13.19.
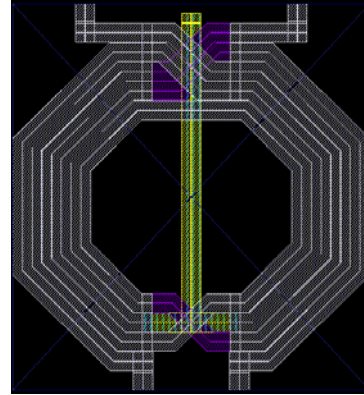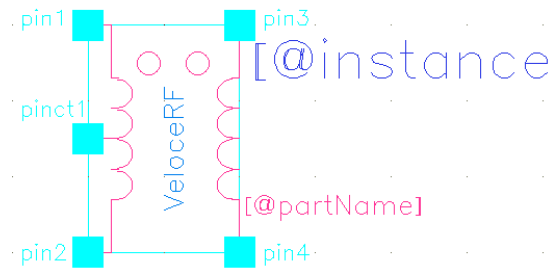
Figure 13.19: The symbol and layout of the balun transformer

13.2.5   The complete transmitter

The schematic of the whole UWB transmitter, prototype n° 3 is shown in Figure 13.20. As the resolution of this schematic is not high enough to have a view in the details, we can refer to Figure 13.21 for the left part and Figure 13.22 for the right part. We see the two delay cells used for each $Vtune$ pad for adjusting the duration of the pulse.
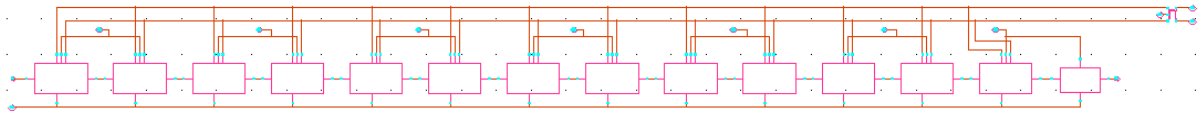

Figure 13.20: The schematic of the complete transmitter
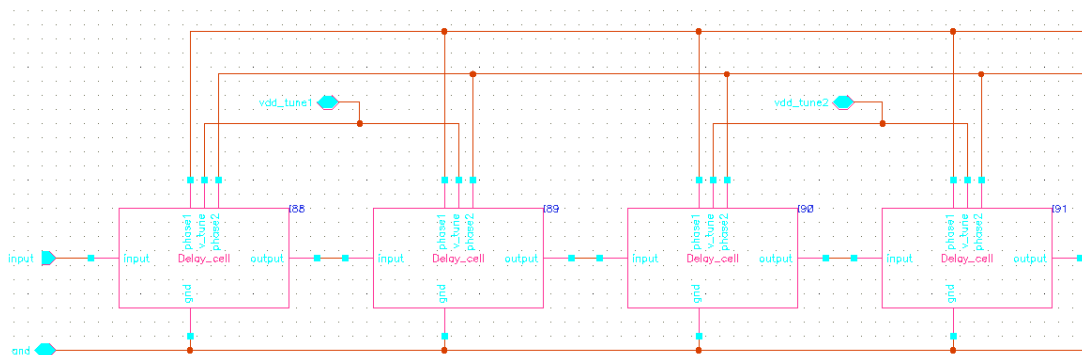
Figure 13.21: The schematic of the complete transmitter - left part
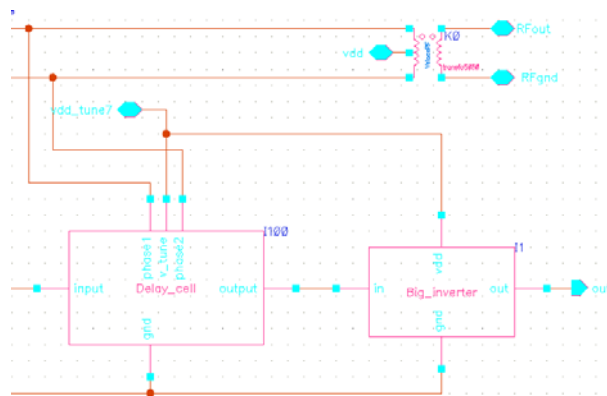
Figure 13.22: The schematic of the complete transmitter - right part

The layout of the whole UWB transmitter, prototype nᵒ 3 is shown in Figure 13.23. A closer view on the active part is shown in Figure 13.24.
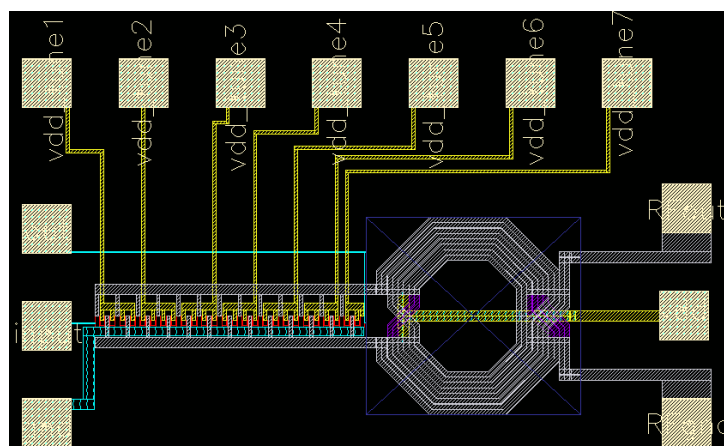
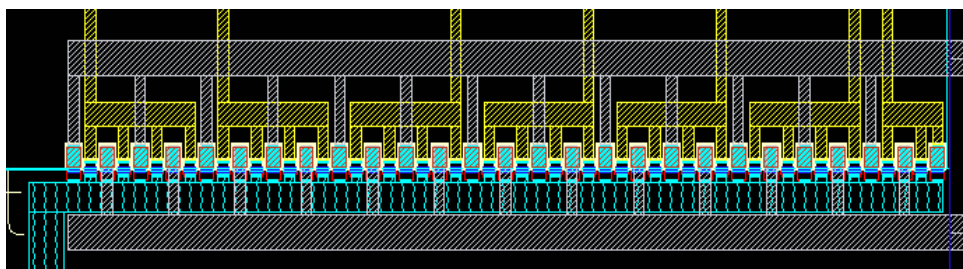Figure 13.23: The layout of the complete transmitter

Figure 13.24: The layout of the complete transmitter - detail of active part

13.2.6 Tests of the Prototype nº 3

The prototype nº 3 circuit is tested by simulation (with the use of VeloceRF tool in Cadence), according to the test circuit shown in Figure 13.25, and the result is presented in Figure 13.26 (with $V_{tune} = (1000000)$). The Vdd voltage (for the logic) of 2.3V and a V_{tune} voltage of 2.3V. The UWB impulse shape changes according to the value of these voltages; the central frequency of the impulse (or of the oscillations) is measured to be about 4.25GHz as expected.
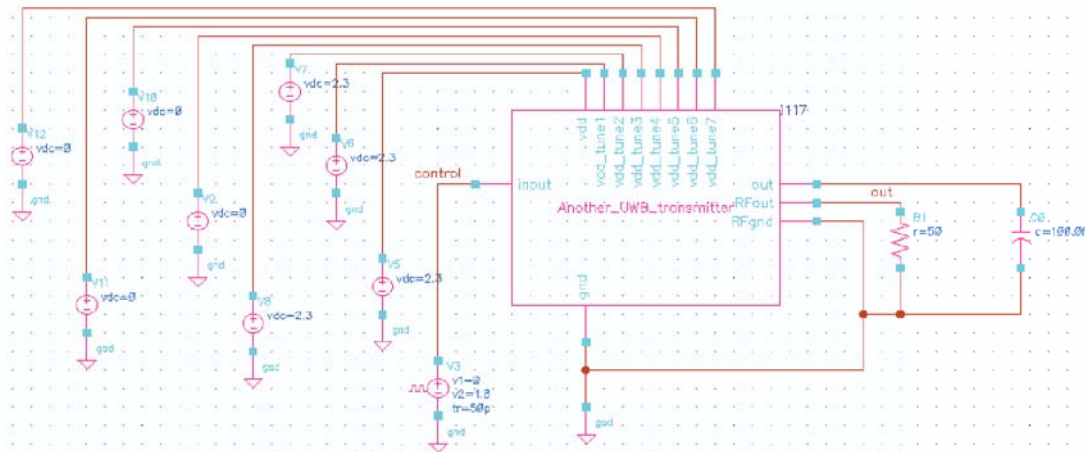

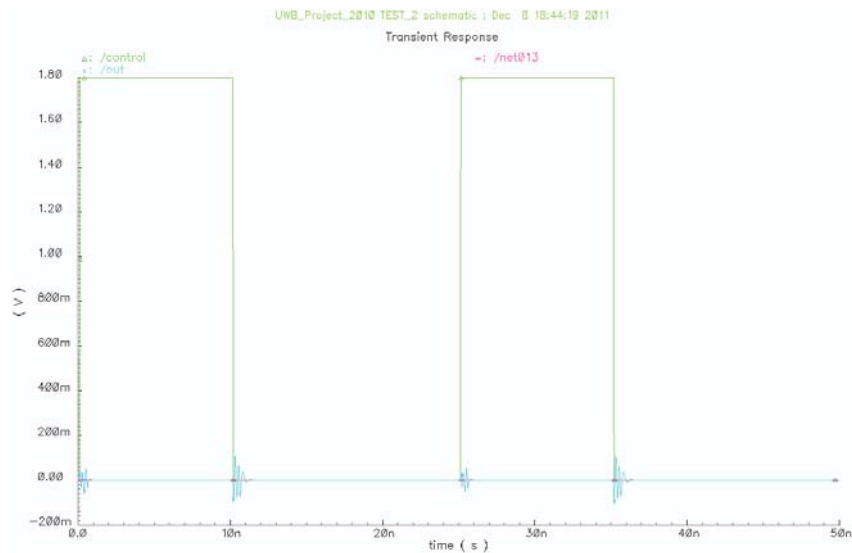Figure 13.25: The Test schematic for prototype nº 3.

Figure 13.26: The simulation of prototype nº 3 with $V_{tune} = (1000000)$ - Global view.

The simulations for all V_{tune} vector configuration are shown in Figure 13.27. We see that the duration of UWB impulses increases with the number of cells activated. With $V_{tune} =$
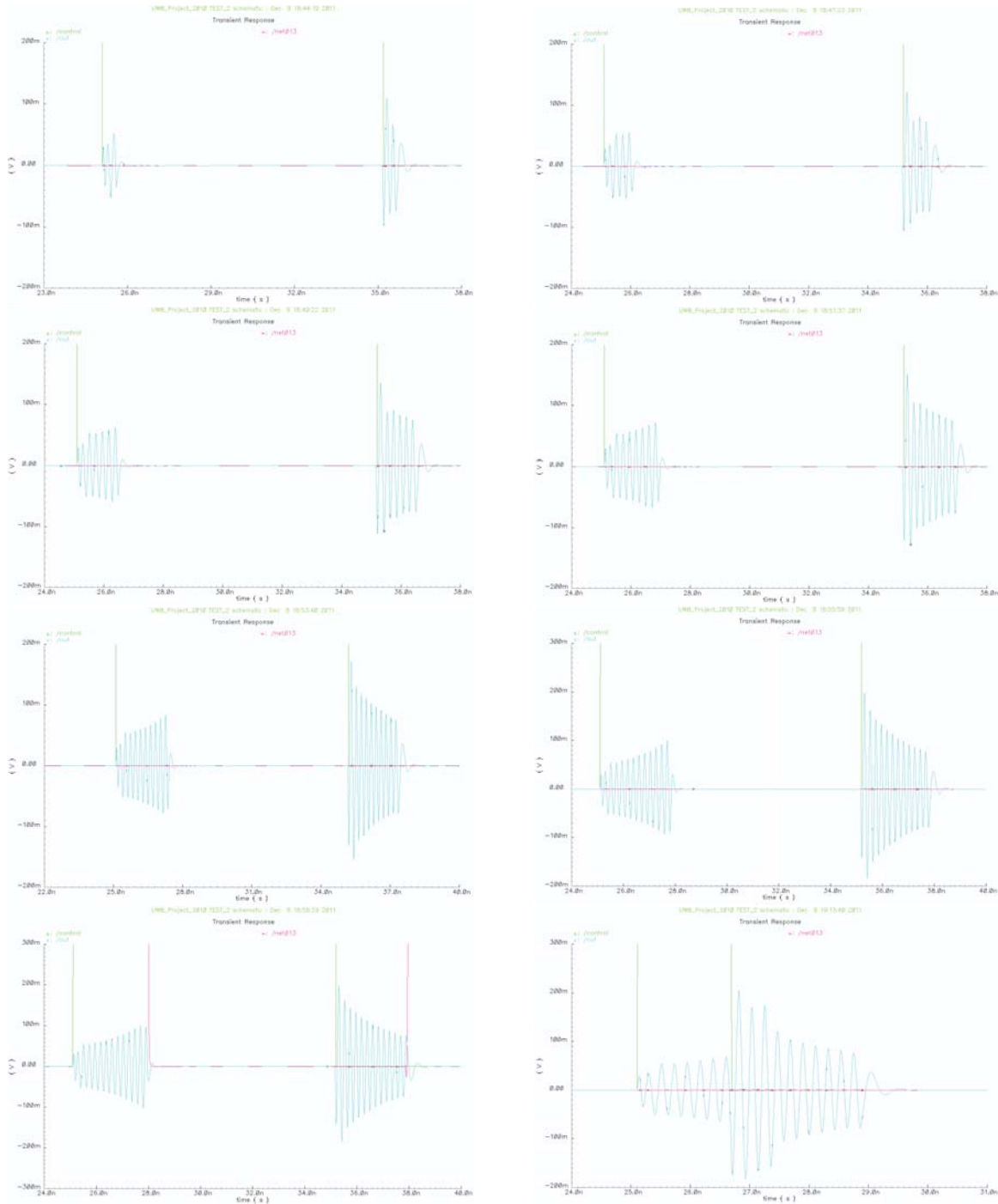
Figure 13.27: The simulation of prototype nº 3 - Detailed views. From left to right, and top to bottom : with $V_{tune} = (1000000)$, (1100000), (1110000), (1111000), (1111100), (1111110), and (1111111) respectively. The bottom right is with $V_{tune} = (1111100)$ and a driving impulse of 1.5ns for concatenating the two parts of the UWB impulse.

(1111100), we concatenate the two parts of the signal in order to have only one signal by reducing the duration of the control signal to 1.5ns. We do that in order to compare with the same configuration in Chapter 14 where it gives the most accurate spectrum according to our expectations.
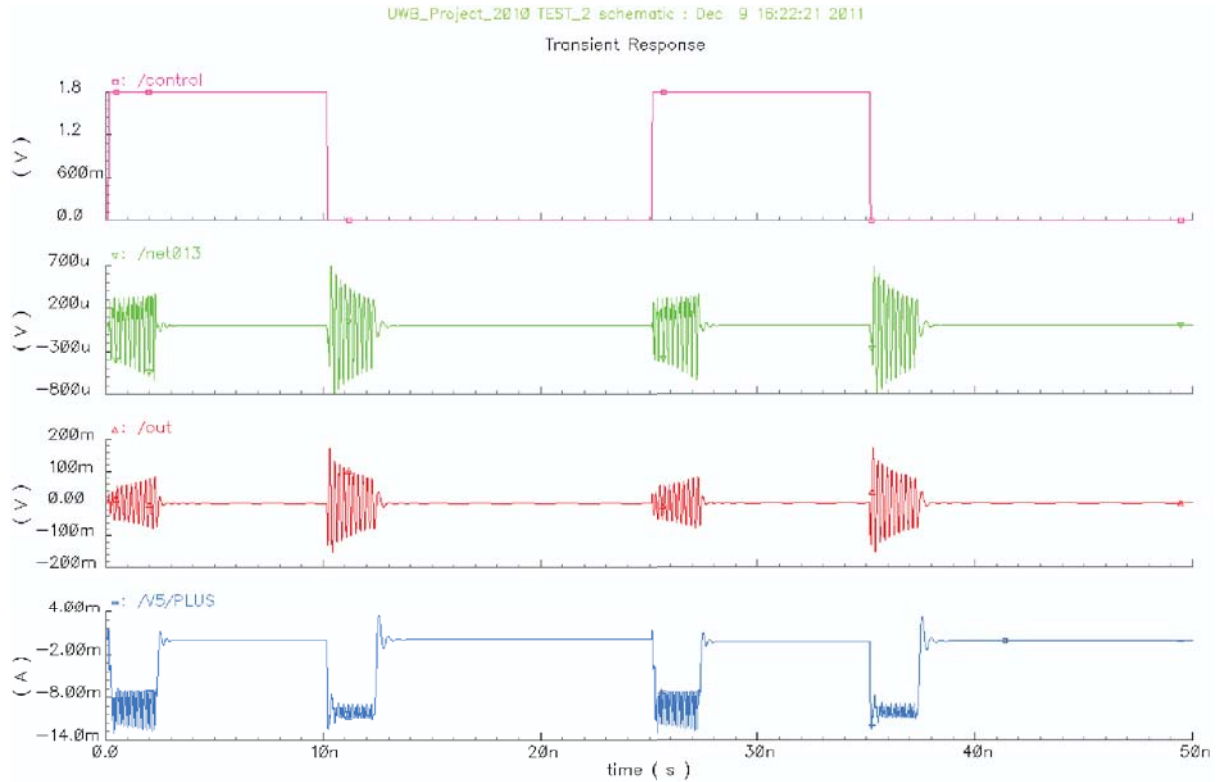

Figure 13.28: The current consumption of prototype nº 3 with $V_{tune} = (1111100)$

According to the simulations, the current is $I_{Vdd} + I_{Vtune} = 11\text{mA}$ (we group both Vdd and Vtune) and $T_P = 4\text{ns}$ (we consider both parts of the signal), as shown in Figure 13.28. The energy per pulse is thus :

$$E_{pulse} = Tp \cdot (I_{Vdd} \cdot Vdd + I_{RFpower} \cdot V_{RFpower}) = 100\text{pJ/pulse}.$$

<div align="right">

Chapter 14

Experimental validation and measurements

</div>

This chapter presents the test boards of prototypes nº 1, nº 2 and nº 3, and the measures of the UWB signals produced by the corresponding chips, with their power consumption in each case. Many results presented in this chapter for prototype nº 1 have a strong influence on the design of the prototypes nº 2 and nº 3 because the latter were designed to correct and improve the results obtained with the former. Before doing all the measurements, we explain a method for measuring the very small impulse currents consumed by the circuits.

14.1   Current measurements

The current consumed by the UWB transmitters described in this work are small and very short. It is not possible to measure the transient current of the impulse directly with a multimeter, which can only measure the average current consumption. One way to measure the transient current consumption is to place resistors in the power supply lines and to measure the voltage drop across these resistors with an oscilloscope. As the circuits are high-frequency, we avoid to place these resistors in the ground connection and we prefer to place them in the positive power supply line. This implies that we need a differential measure as the oscilloscope and the DUT share the same ground. All current measurement made with the three prototypes have the same generic shape as shown in Figure 14.1. The signal is measured across a resistor of 1Ω because this value is enough for the desired precision but not too high to introduce a voltage drop that could disturb the tested circuit. The oscilloscope is set to AC coupling in
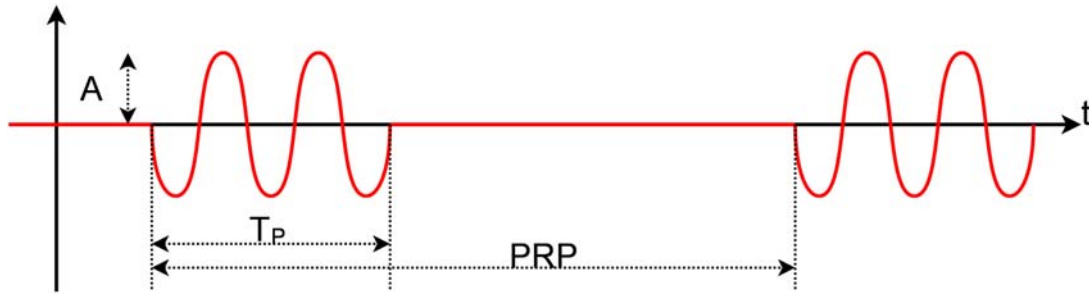
Figure 14.1: The current impulse waveform.

order to remove the DC voltage and to see only the variation of the signal. Two probes are used, one for each terminal of the resistor, and the oscilloscope is set to measure the voltage drop in differential mode. This should be the simplest and most accurate way to measure this voltage with the smallest effect on the circuit under test. Unfortunately, this method displays very approximate results and it is not reliable enough to measure the transient current, even with a good oscilloscope because of the noise.

Another way to measure the power consumption is to measure the average current with a multimeter and to calculate the transient current consumption and the energy per pulse. This method gives very accurate and reliable results; it is used in our measurement campaign for evaluating the power consumption and energy per pulse,

When the transient current consumption is known and assuming it has a duration of T_p ns then, the energy per pulse is given by the following expression :

$$E_{pulse} = Vcc \cdot Icc_{transient} \cdot T_p$$

When we cannot measure the transient current consumption but only the average one, the transient current is expressed as (see Figure 14.1) :

$$I_{transient} = I_{average} \cdot \frac{PRP}{T_p}$$

Then, the energy per pulse is expressed as :

$$E_{pulse} \quad = \quad Vcc \cdot Icc_{transient} \cdot T_p$$

$$= \quad Vcc \cdot I_{average} \cdot \frac{PRP}{T_p} \cdot T_p$$

$$= \quad Vcc \cdot I_{average} \cdot PRP$$

14.2   Prototype n° 1 measurement board

The design of the test board of any integrated circuit has to follow some dimensional rules in order to improve the bonding process, as already explained previously (see Chapters 12 and 13). The schematic and layout of test board for prototype n° 1 are shown in Figures 14.2 and 14.3 respectively. As the circuit has a very high transient current consumption, the decoupling is carefully designed in order to sustain the current impulse by using a high value capacitor C_1 and a series inductor L_1 on the main power supply line. In front of every power supply pin a smaller capacitor is added (C_2, C_3, C_4 and C_5). The RF connections are made with conventionnal SMA connectors. The RF tracks are designed as microstrip line as done previously (see Appendix A.1.1). Ground and power supply connections are made with conventional pins. The PCB is gold-plated by electro-chemical means in order to preserve the copper and to help the bonding that will be made with aluminium bonds.

The detail of the layout of the PCB around to the integrated circuit is shown in Figure 14.4. Special care was taken to bring the power supply in a regular way in order to avoid unexpected parasitic behaviours that could introduce delays in the different part of the chip. The top and bottom ground planes are connected with several vias that were placed close to the corresponding pins of the chip. The width of RF tracks is decreased close to the chip in order to make the bonding possible; the portion of the narrow part of these tracks was kept as short as possible.

The PCB with bonded chip is shown in Figure 14.5. We see dark regions, particularly near texts. This is a normal phenomenon that is produced by the glue used by the PCB manufacturer when doing the etching and has no effect on the electrical performance of the circuit.

The Prototype n° 1 bonded on the test PCB is shown in Figure 14.6 thereafter.
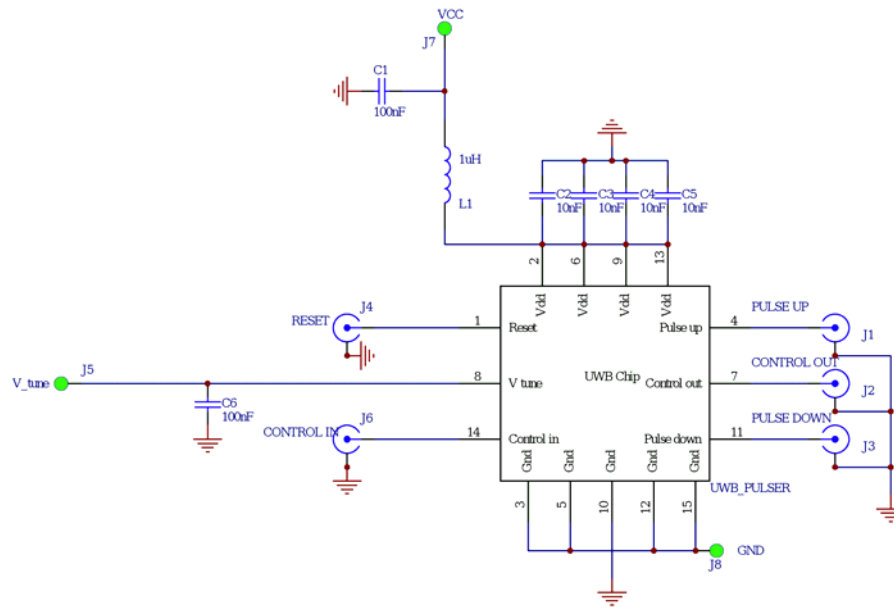
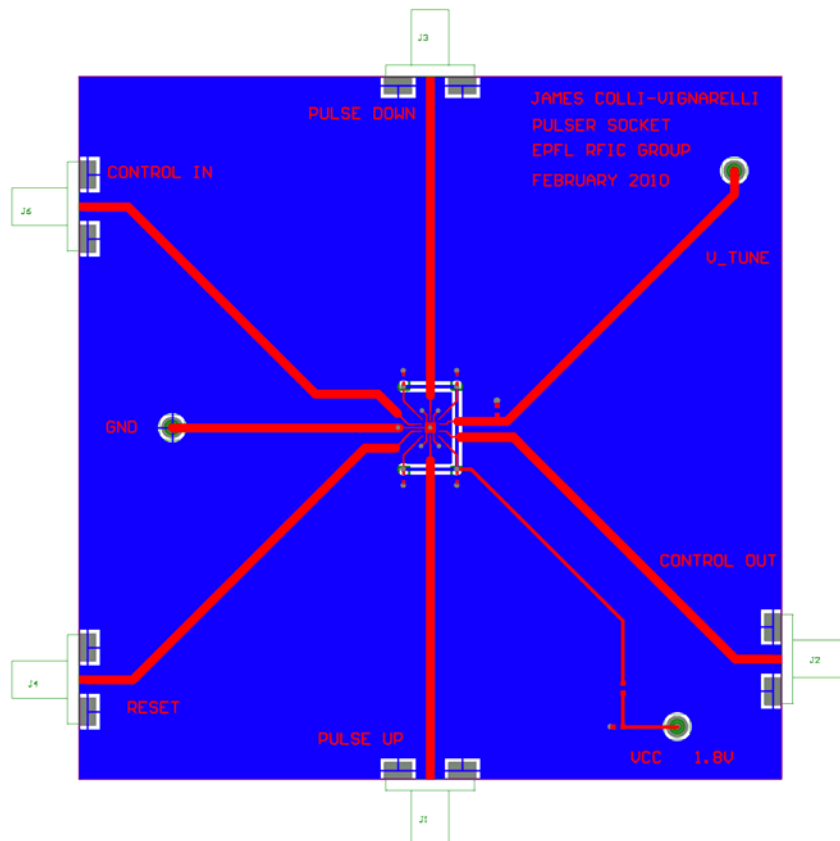Figure 14.2: The schematic of the testing board for Prototype n⁰ 1.

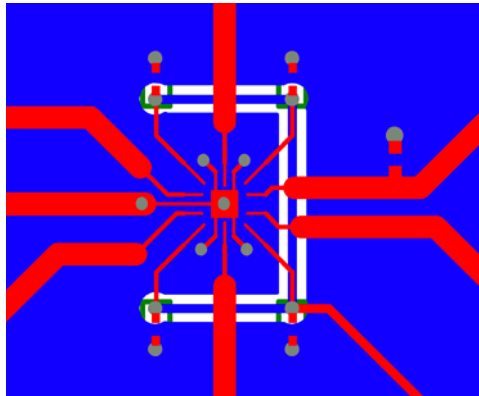Figure 14.3: The PCB of the testing board for Prototype n⁰ 1.

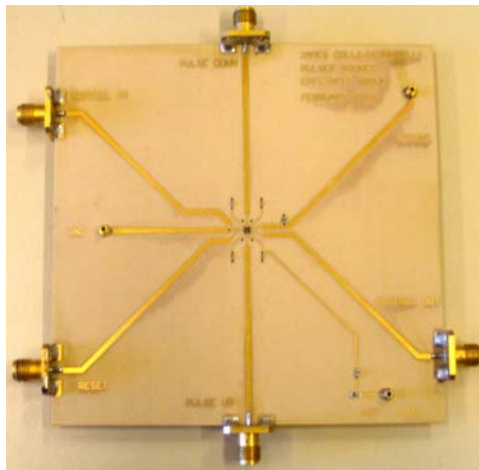Figure 14.4: Detail on the chip pattern on PCB of the testing board for Prototype n° 1.

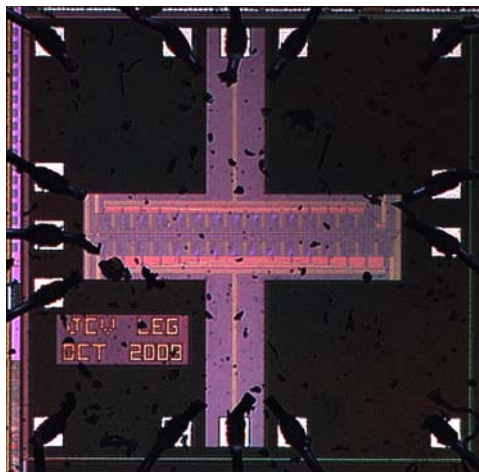Figure 14.5: The PCB of the testing board for Prototype n° 1.

Figure 14.6: The Prototype n° 1 chip.

14.3   Prototype nº 1 validation

The Prototype nº 1 is measured by using a RFC module (see Figure 14.7) that gives the power to the output stage (either *pulse up* or *pulse down*) and by blocking it for the measurement device. The measurements are made with $V_{tune} = 2.1$V and $Vdd = V_{pulseup} = V_{pulsedown} = 2.7$V.

Figure 14.7: The RFC module used powering output stages of Prototype nº 1. The drawing on it is self-explanatory.
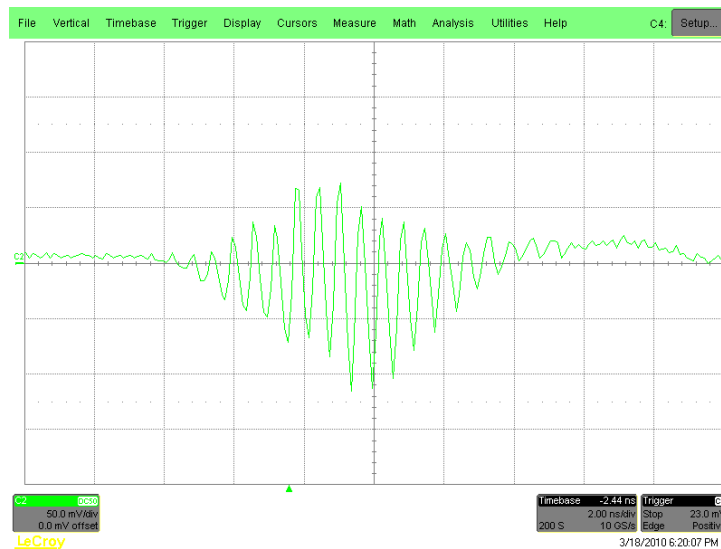

Figure 14.8: The output signal (pulse down) from Prototype nº 1.

The measured signal is shown in Figures 14.8 (time domain) and 14.9 (frequency domain) where we have the *pulse down* only. Unfortunately, the *pulse up* signal does not work and we have no signal to show. We assume this is due to the PMOS transistors on *pulse up* that are too slow. Although we cannot check what happens exactly, we expect to have better results on Prototypes nº 2 and 3 by using only NMOS transistors that are much faster. The average

current is measured to $I_{pulsedown} = 0.3$mA and, as the $PRP = 1000$ns, the energy per pulse is thus 810 pJ/pulse.
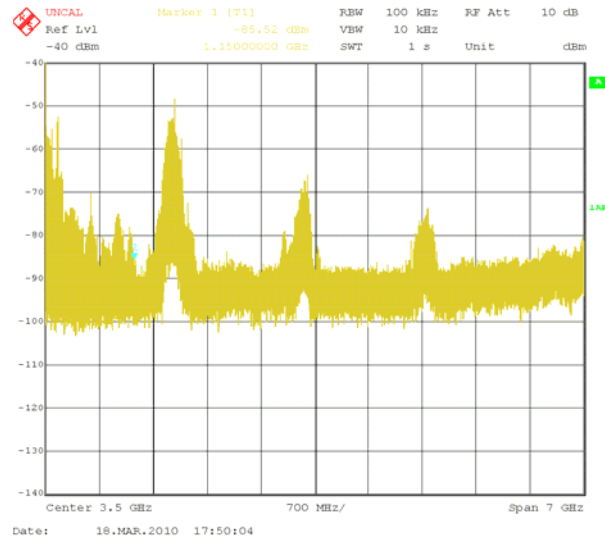

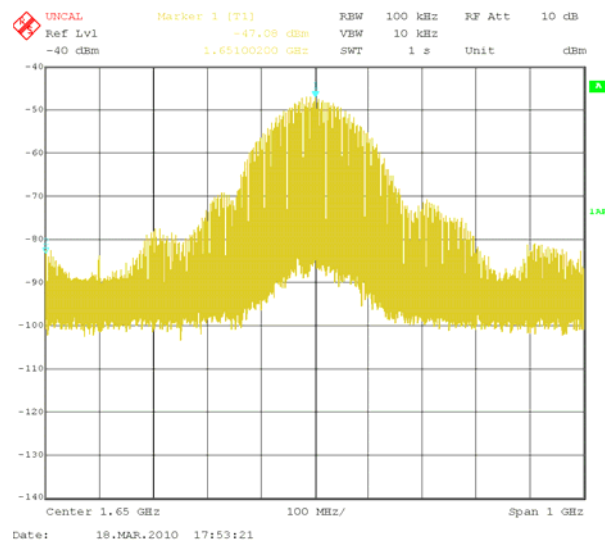Figure 14.9: Spectrum of the output signal from Prototype n° 1.

Figure 14.10: detail of the spectrum of the output signal from Prototype n° 1.

The signal is maximum at about 1.65GHz. This low frequency is caused by the missing points of the other half that double the period between two consecutive samples.

14.4   Prototypes nº 2 and nº 3 measurement board

The schematic and PCB layout of the measurement board for Prototypes nº 2 and nº 3 are shown in Figures 14.11 and 14.12 respectively. The board has a linear voltage regulator for delivering stable voltages to the chip; the maximum available voltage is 2.8V. Although the CMOS technology we used supports 1.8V, we can safely rise the voltage to 2.8V without any problem for experimental purpose; however such a voltage could cause a stress on the long run to the circuit that may reduce its lifetime. A key diode protects the board against polarity mistake. Several trimmer potentiometers allow adjusting the required voltages for both prototypes circuits. There are decoupling capacitors of high value that also stores the energy required by the chip during a pulse. These capacitors are necessary because the trimmers have a $1k\Omega$ resistance that could create a voltage drop during the pulse generation if the capacitors are not present. The voltage can be switched on or off or bypassed in case it is provided by an external voltage source when required.
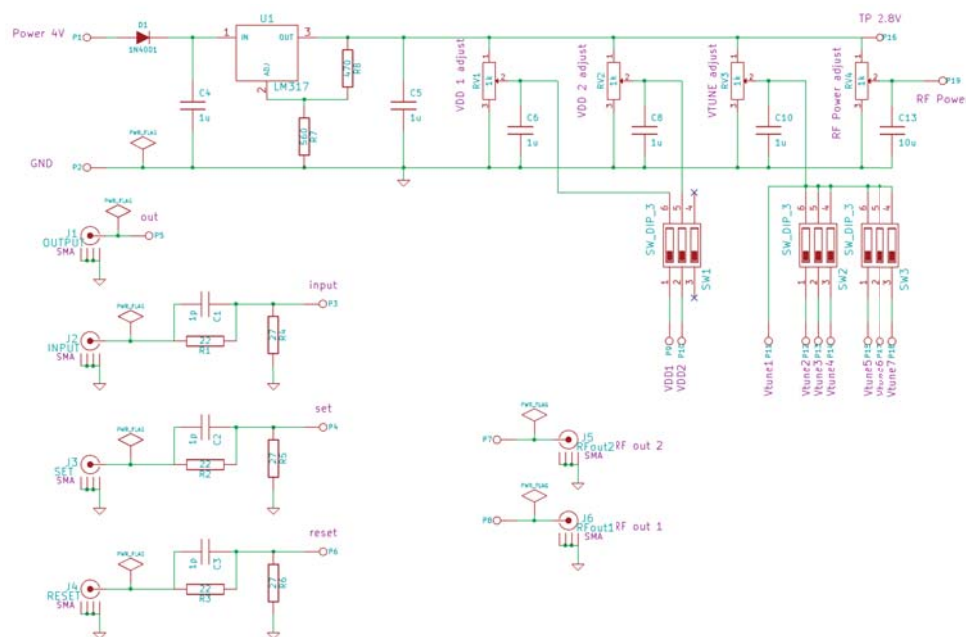

Figure 14.11: The schematic of the testing board for Prototype nº 2 and nº 3.

As the external driving circuit (Khepera or FPGA board) deliver 3.3V and the chip supports normally 1.8, we need a voltage divider to adjust the level. As a resistive divider has a slower response to short impulse, it can be improved by adding capacitors in parallel with the resistors of the divider (see [81]). The ratio between the capacitors and the resistors has to be the same

for optimal performance. As we estimate the input capacitance to be lower than $1pF$ and the resistors' values are almost the same, we use a $1pF$.
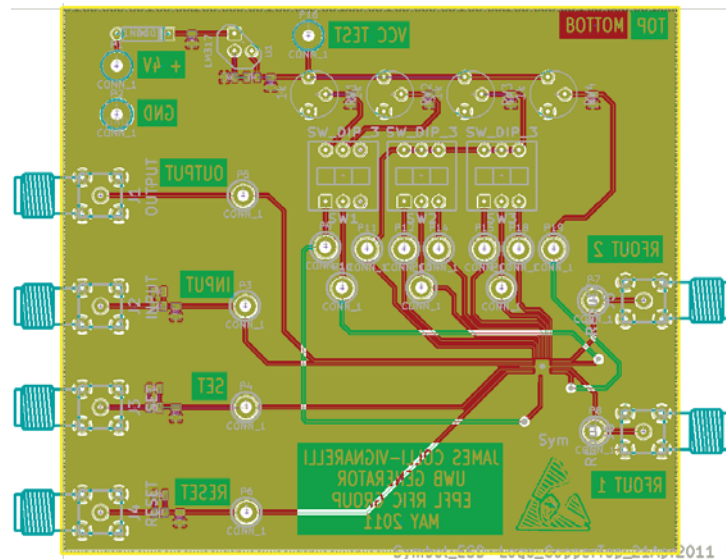

Figure 14.12: The PCB of the testing board for Prototype nº 2 and nº 3.

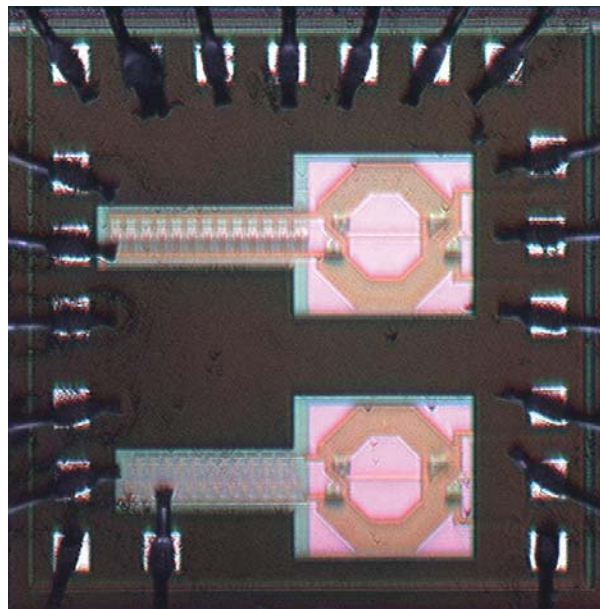The die photo of Prototypes nº 2 and nº 3 is shown in Figure 14.13.

Figure 14.13: The Prototypes nº 2 (bottom) and nº 3 (top) chip.

14.5   Prototype nᵒ 2 validation

The prototype nᵒ 2 is first measured by using a Agilent 33250A function generator for generating a clean and easily reproducible driving signal. The settings of the signal generator are the following :

- period = 100 ns

- pulse width = 50 ns but this has no effect on the shape of the signal

- low level = 0 V

- high level = 3.9 V

- edge time = 14 ns

We assume that the driving signal is a periodic signal (not a random one) with a period of 100 ns. This has an effect on the spectrum because it introduces spurs in the spectrum that do not occur when the driving signal is real data. In practice, we can neglect this phenomenon as the frequency of the driving signal frequency is much smaller compared with the RF UWB signal.

14.5.1   Tests with the function generator

As the working frequency is close to the technical limitations of the technology (that are around 4.0 GHz according to collaborators of our laboratory), we decided to overdrive the circuit by raising the power supply to $VDD_1 = 2.80$ V instead of 1.80V. The tuning voltage is rose to the same level : $V_{\mathrm{RF\,power}} = 2.80$ V. These settings are made manually by checking on the oscilloscope and the spectrum analyser the shape of the signal.

The UWB signal obtained in the time and frequency domains is shown in Figures 14.14 and 14.15 respectively. The setting for $V_{\mathrm{RF\,power}}$ is chosen here to show the maximum power that the prototype nᵒ 2 of the UWB transmitter is able to produce. The spectrum is maximum at $f_0 = 3.1$ GHz (see the blue arrow in Figure 14.15) with approximately -30 dBm/MHz. This power is above the regulations and the central frequency is much below the initial specifications. The current consumed by the circuit is $I_{\mathrm{RF\,power}} = 1735\mu$A on average for the power part and $I_{VDD_1} = 477\mu$ A on average for the logic part. The energy per pulse is 620pJ/pulse.
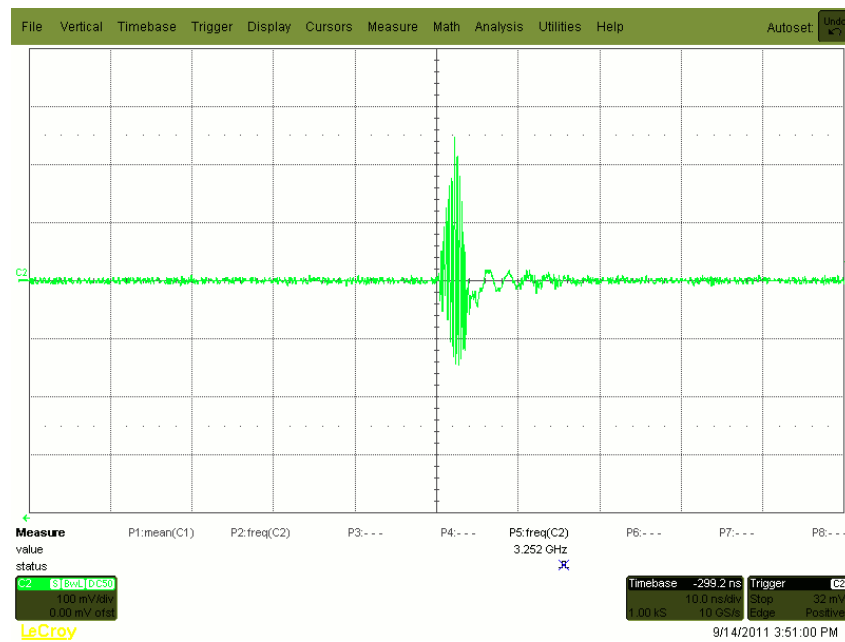
Figure 14.14: The output signal in the time domain for Prototype nᵒ 2 with maximal power.
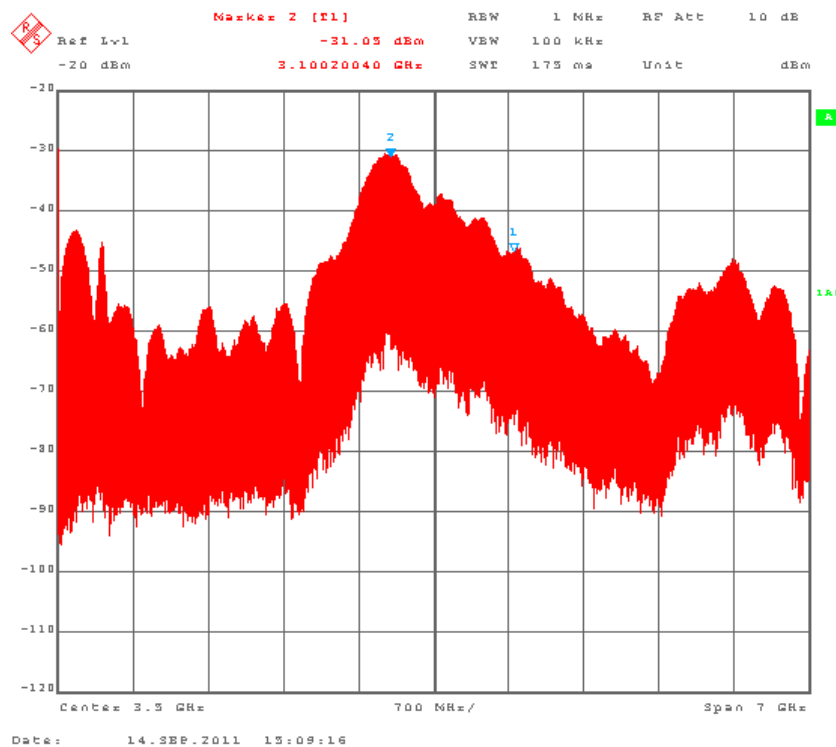

Figure 14.15: The output signal in the frequency domain for Prototype nᵒ 2 with maximal power.
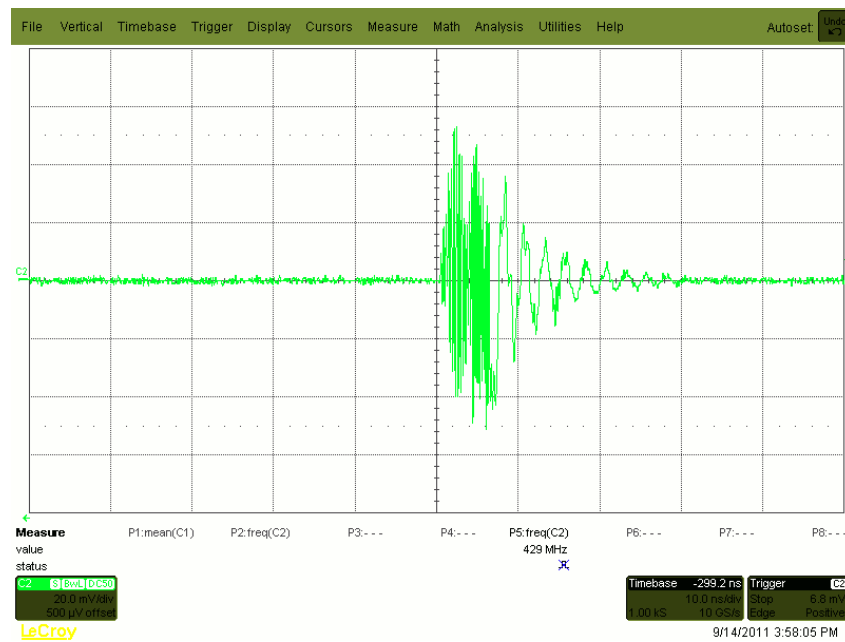
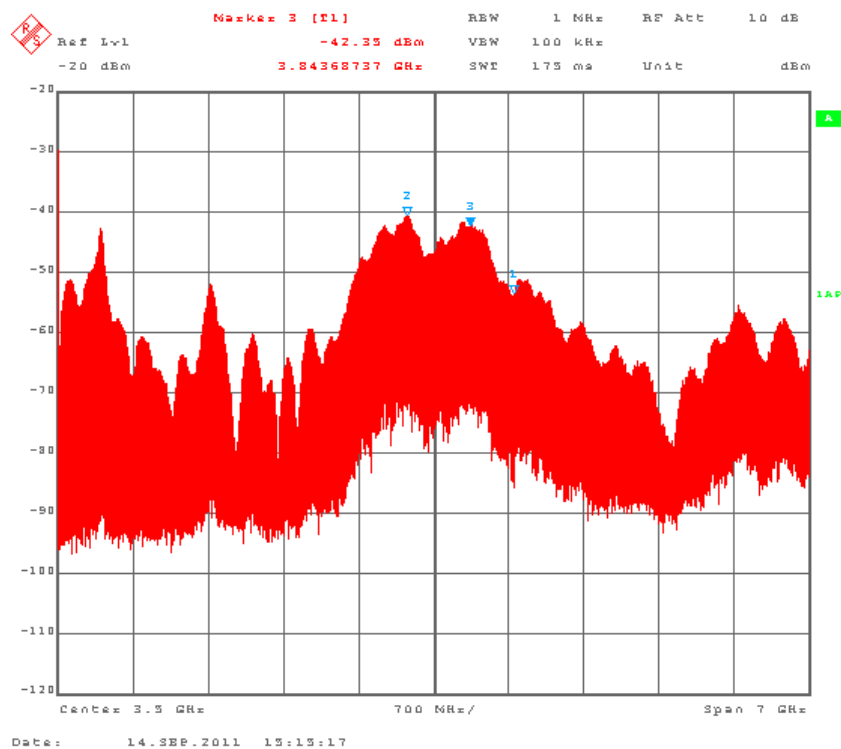Figure 14.16: The output signal in the time domain for Prototype nº 2 with FCC compliant power.

Figure 14.17: The output signal in the frequency domain for Prototype nº 2 with FCC compliant power.

The $V_{\text{RF power}}$ voltage is decreased to 0.76V in order to be FCC compliant. The new UWB signal obtained in the time and frequency domains is shown in Figures 14.16 and 14.17 respectively. The spectrum is maximum now at $f_0 = 3.25$ GHz (see the blue arrow nᵒ 2 in Figure 14.17) with approximately -41 dBm / MHz and another extremum is reached at $f_0 = 3.85$ GHz with approximately -42.3 dBm/MHz. This second maximum is very close to the target specifications. Unfortunately, there is no way to act on the delay line excepted to change the power supply voltage which changes also the switching threshold voltage that change the shape of the spectrum. This is why the prototype nᵒ 3 will implement later such a setting. The current consumed by the circuit is $I_{\text{RF power}} = 949\mu$A on average for the power part and $I_{VDD_1} = 897\mu$ A on average for the logic part. The energy per pulse is 325pJ/pulse.

14.5.2   Tests with the Khepera modulator

The driving signal is a periodic signal (not a random one) with a period of 1000 ns (Datarate is 1 Mbit/s with Khepera modulator). The same remark holds for the spurs on the spectrum. The power supply voltage is raised to $VDD_1 = 2.80$ V instead of 1.80V, as it was before. The RF power voltage is rose to the same level : $V_{\text{RF power}} = 2.80$ V because the decrease of datarate decreases the output power. The signal is maximum at $f_0 = 3.10$ GHz with a power of about -51.3 dBm/MHz (see Figures 14.18 and 14.19). We can increase $V_{\text{RF power}}$ in order to increase the output power but there is a risk to destroy the circuit (remember it is a 1.8V technology). The current consumed by the circuit is $I_{\text{RF power}} = 188\mu$A on average for the power part and $I_{VDD_1} = 171\mu$ A on average for the logic part. The energy per pulse is 1005pJ/pulse. The decrease of 10 times in the power consumption is directly linked to the decrease of the same factor of the period, according to Section 14.1.
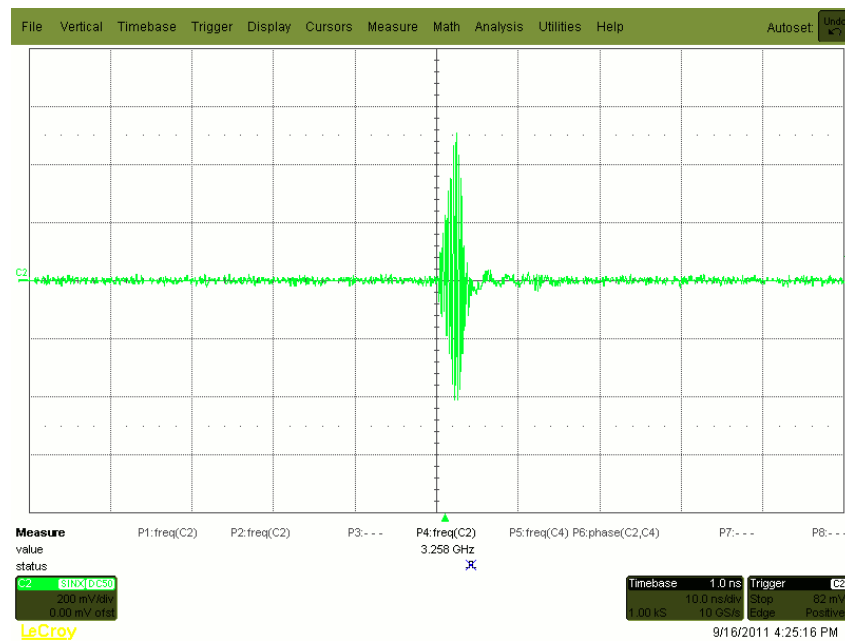
Figure 14.18: The output signal in the time domain FCC compliant for Prototype nº 2 with Khepera modulator.
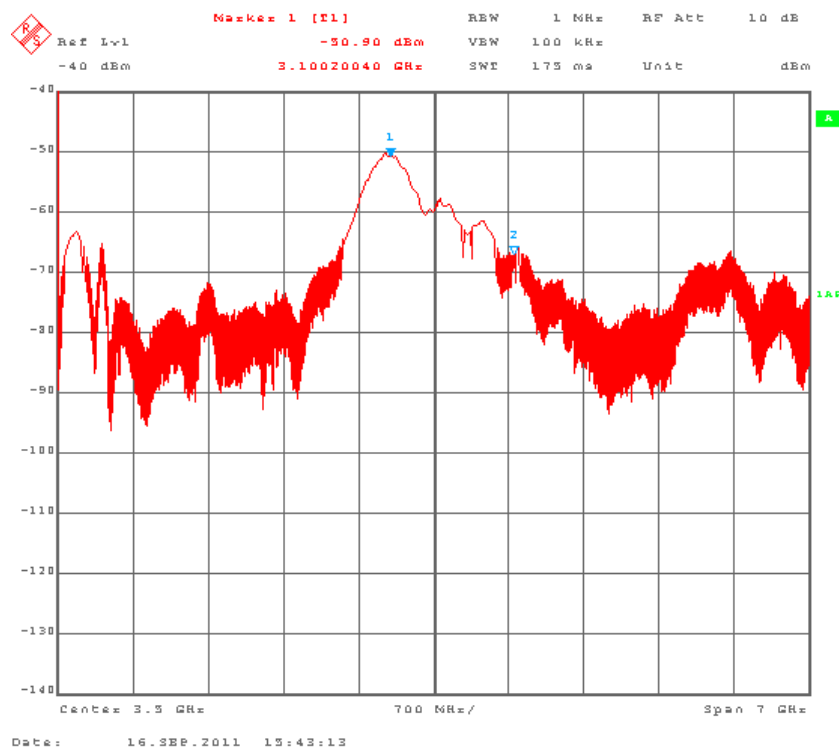

Figure 14.19: The output signal in the frequency domain FCC compliant for Prototype nº 2 with Khepera modulator.

14.6   Prototype n° 3 validation

The prototype n° 3 is measured by using a Agilent 33250A function generator for generating a clean and easily reproducible driving signal. The settings of the signal generator are the following :

- period = 100 ns

- pulse width = 62 ns to compensate the rising/falling edge asymmetry

- low level = 0 V

- high level = 3.9 V

- edge time = 14 ns

We assume that the driving signal is a periodic signal (not a random one) with a period of 100 ns. This has an effect on the spectrum because it introduces spurs in the spectrum that do not occur when the driving signal is real data. In practice, we can neglect this phenomenon as the frequency of the driving signal frequency is much smaller compared with the RF UWB signal. In order to simplify the notation of the switches position, we note their position as a vector (Vtune1;...; Vtune7) where 1 means the switch is on (Vtune is applied to the pin) and 0 means the switch is off (the pin is not connected and thus floating). As we need at least one stage active, the voltage V_{tune1} is always set to 1 according to the test PCB topology.

14.6.1   Tests with the function generator

As the working frequency is close to the technical limitations of the technology (that are around 4.0 GHz according to collaborators of our laboratory), we decided to overdrive the circuit by raising the power supply to $VDD_2 = 2.36$ V instead of 1.80V. The tuning voltage is rose to the maximum voltage available on the PCB : $V_{tune} = 2.80$ V. These settings are made manually by checking on the oscilloscope and the spectrum analyser the shape of the signal. This voltage configuration is maintained for all further measures with the function generator. The blue arrow shows the power at $f_0 = 4.25$ GHz in order to give an idea of how the spectrum's shape varies with the configuration of the switches.

Configuration $V_{tune} = (1000000)$

The current consumed by the circuit is $I_{VDD2} = 6160\mu A$ on average for the power part (current directly used for UWB generation) and $I_{Vtune} = 1200\mu$ A on average for the delay gates part (current not directly used for UWB generation). The energy per pulse is 1790pJ/pulse.

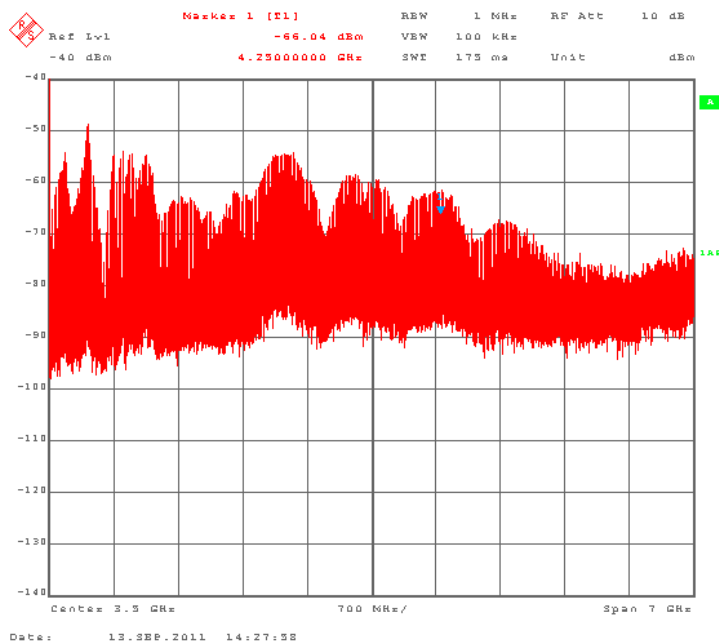Figure 14.20: The output signal in the time domain for Prototype nº 3 with $V_{tune} = (1000000)$.

Figure 14.21: The output signal in the frequency domain for Prototype nº 3 with $V_{tune} = (1000000)$.

Configuration $V_{tune} = (1100000)$

The current consumed by the circuit is $I_{VDD2} = 5190\mu$A on average for the power part (current directly used for UWB generation) and $I_{\text{Vtune}} = 782\mu$ A on average for the delay gates part (current not directly used for UWB generation). The energy per pulse is 1445pJ/pulse.

Figure 14.22: The output signal in the time domain for Prototype n° 3 with $V_{tune} = (1100000)$.

Figure 14.23: The output signal in the frequency domain for Prototype n° 3 with $V_{tune} = (1100000)$.

Configuration $V_{tune} = (1110000)$

The current consumed by the circuit is $I_{VDD2} = 5420\mu$A on average for the power part (current directly used for UWB generation) and $I_{\text{Vtune}} = 780\mu$ A on average for the delay gates part (current not directly used for UWB generation). The energy per pulse is 1500pJ/pulse.
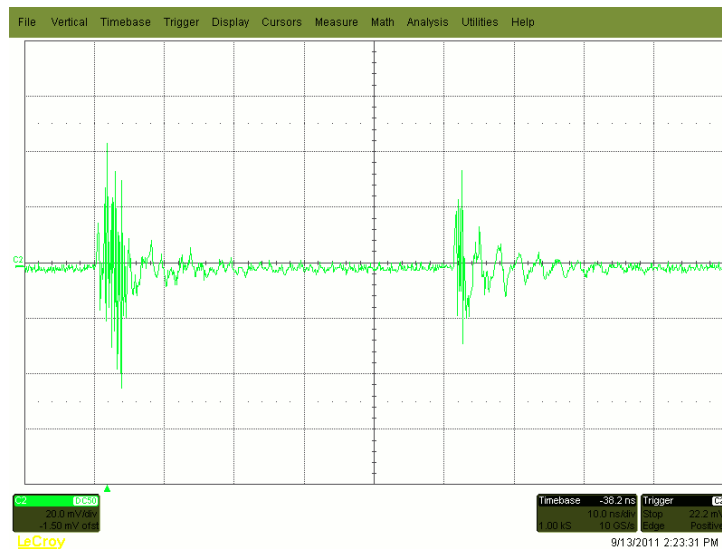

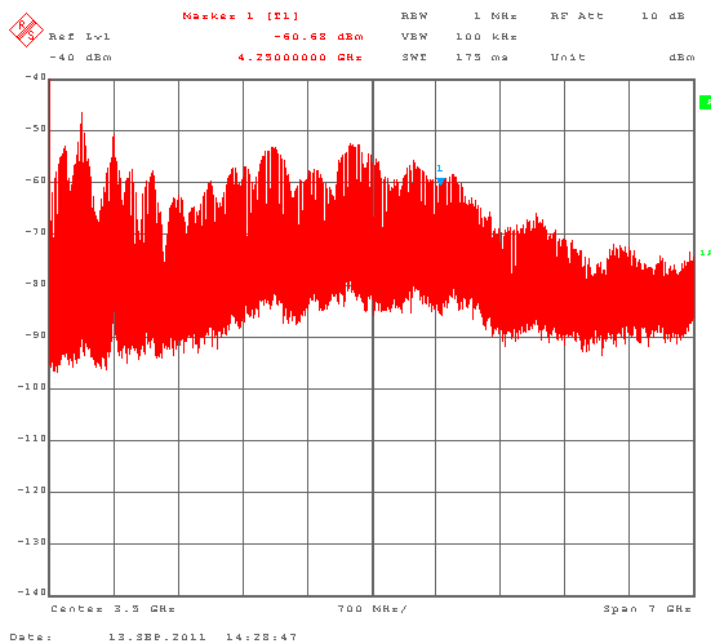Figure 14.24: The output signal in the time domain for Prototype n° 3 with $V_{tune} = (1110000)$.

Figure 14.25: The output signal in the frequency domain for Prototype n° 3 with $V_{tune} = (1110000)$.

Configuration $V_{tune} = (1111000)$

The current consumed by the circuit is $I_{VDD2} = 8510\mu$A on average for the power part (current directly used for UWB generation) and $I_{\text{Vtune}} = 2720\mu$ A on average for the delay gates part (current not directly used for UWB generation). The energy per pulse is 2770pJ/pulse.

Figure 14.26: The output signal in the time domain for Prototype n° 3 with $V_{tune} = (1111000)$.

Figure 14.27: The output signal in the frequency domain for Prototype n° 3 with $V_{tune} = (1111000)$.

Configuration $V_{tune} = (1111100)$

The current consumed by the circuit is $I_{VDD2} = 7330\mu A$ on average for the power part (current directly used for UWB generation) and $I_{Vtune} = 2070\mu$ A on average for the delay gates part (current not directly used for UWB generation). The energy per pulse is 2310pJ/pulse.
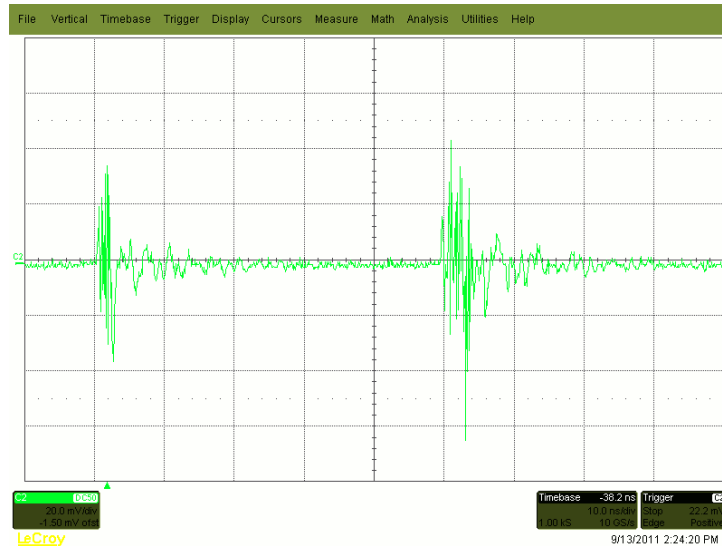

Figure 14.28: The output signal in the time domain for Prototype n° 3 with $V_{tune} = (1111100)$.
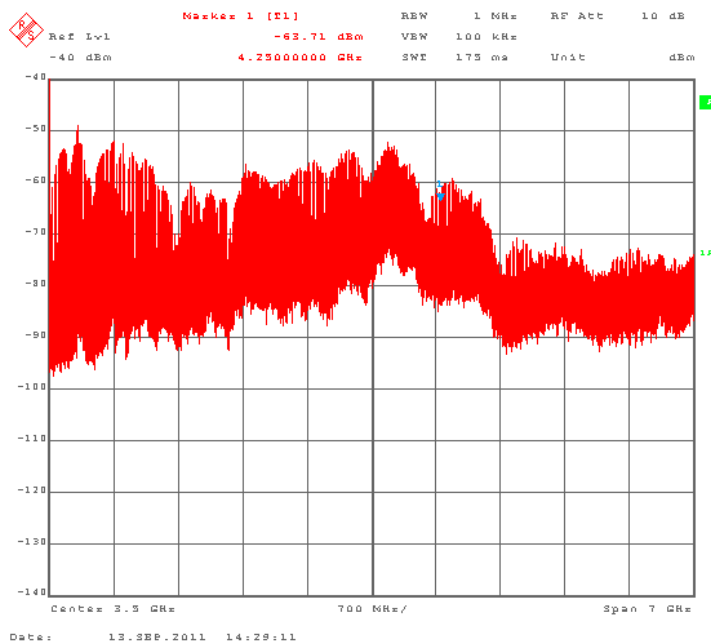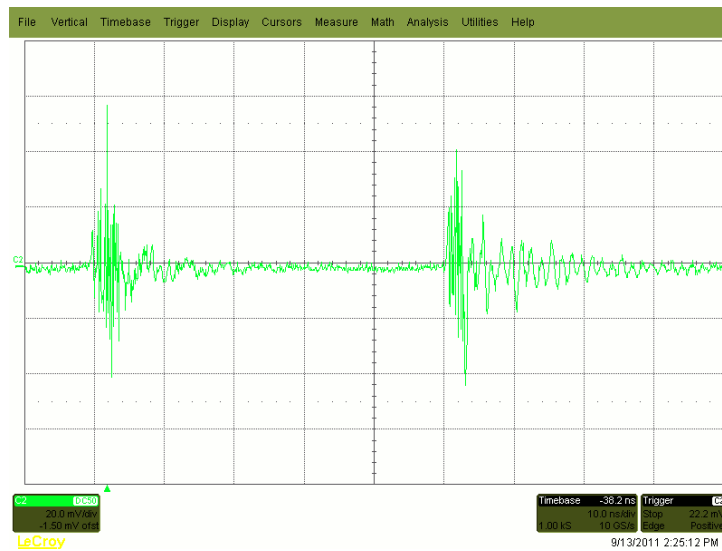

Figure 14.29: The output signal in the frequency domain for Prototype n° 3 with $V_{tune} = (1111100)$.

Configuration $V_{tune} = (1111110)$

The current consumed by the circuit is $I_{VDD2} = 9660\mu$A on average for the power part (current directly used for UWB generation) and $I_{\text{Vtune}} = 3420\mu$ A on average for the delay gates part (current not directly used for UWB generation). The energy per pulse is 3240pJ/pulse.

Figure 14.30: The output signal in the time domain for Prototype nᵒ 3 with $V_{tune} = (1111110)$.

Figure 14.31: The output signal in the frequency domain for Prototype nᵒ 3 with $V_{tune} = (1111110)$.

Configuration $V_{tune} = (1111111)$

The current consumed by the circuit is $I_{VDD2} = 13450\mu$A on average for the power part (current directly used for UWB generation) and $I_{\text{Vtune}} = 12580\mu$ A on average for the delay gates part (current not directly used for UWB generation). The energy per pulse is 6700pJ/pulse.

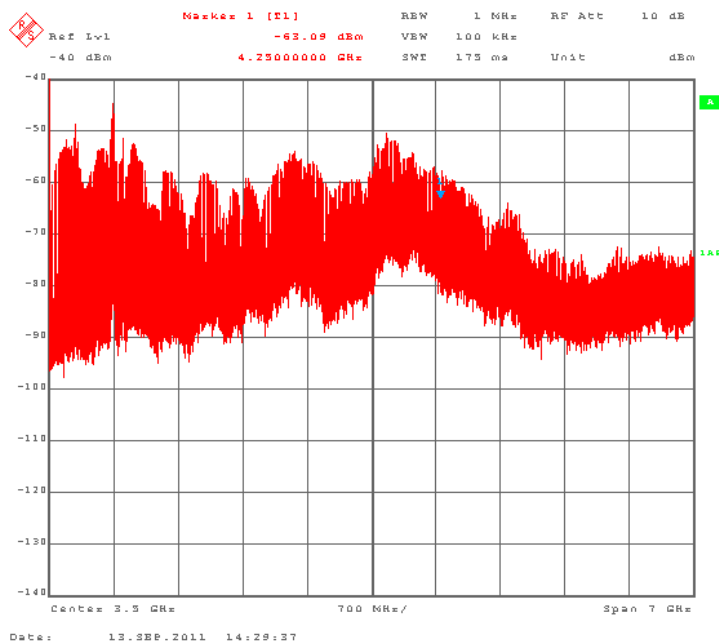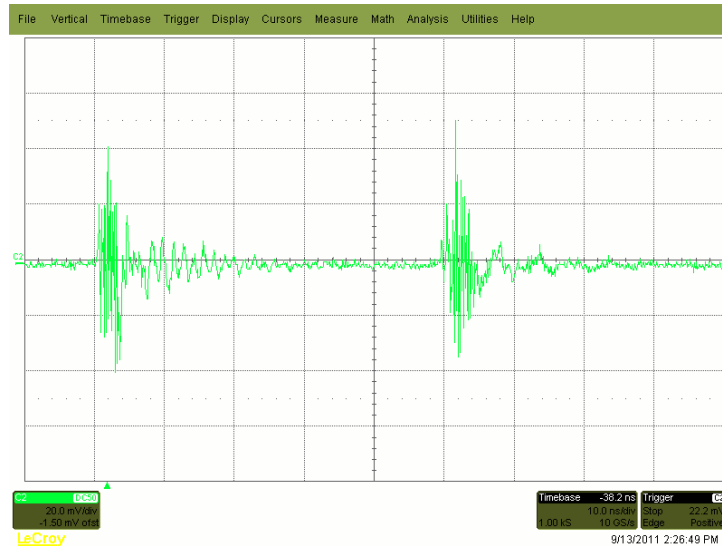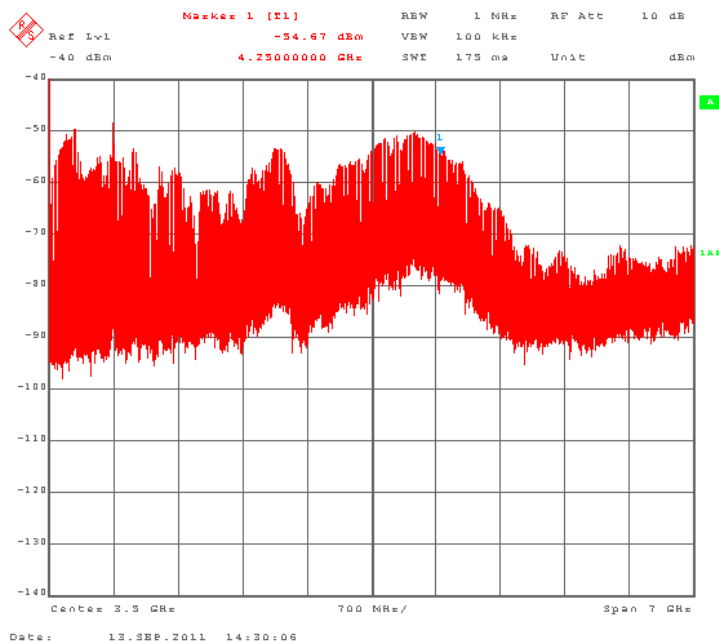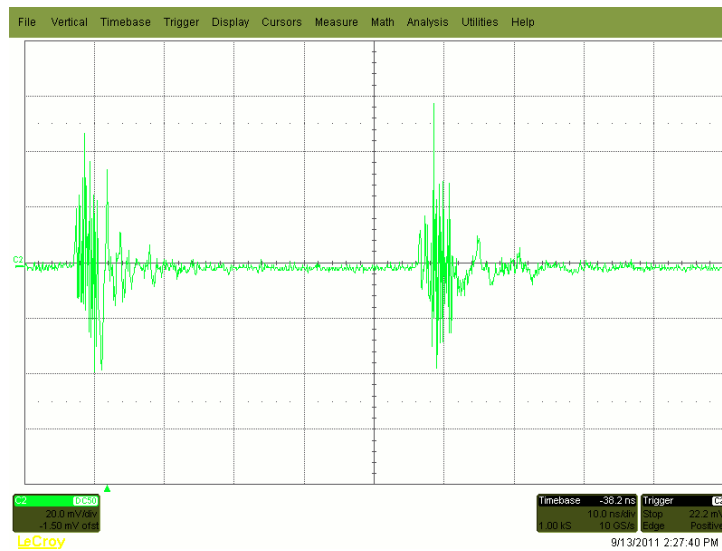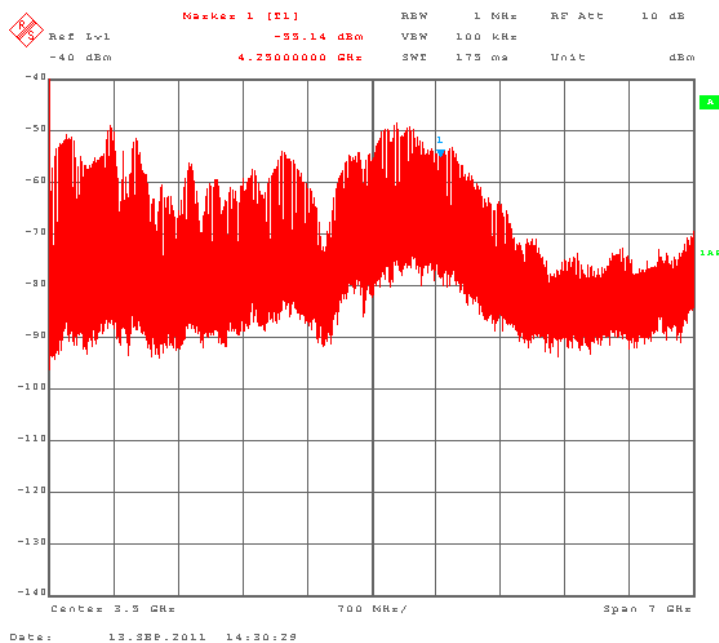Figure 14.32: The output signal in the time domain for Prototype nº 3 with $V_{tune} = (1111111)$.

Figure 14.33: The output signal in the frequency domain for Prototype nº 3 with $V_{tune} = (1111111)$.

14.6.2   Tests with current consumption optimization

The prototype n° 3 is measured by using a Hewlett-Packard 8131A function generator for generating a clean and easily reproducible driving signal. This generator is able to produce extremely short driving pulse duration that decrease the current consumption by reducing the time the power transistors are on in the circuit. The settings of the signal generator are the following :

- period = 1000 ns

- pulse width = 450 ps (!) to simulate the Impulse Generator used in Prototype n° 2

- low level = 0 V

- high level = 3.9 V

- $V_{tune} = 1111000$

The current consumed by the circuit is $I_{VDD2} = 847\mu$A on average for the power part (current directly used for UWB generation) and $I_{Vtune} = 257\mu$ A on average for the delay gates part (current not directly used for UWB generation). The energy per pulse is 2720pJ/pulse.
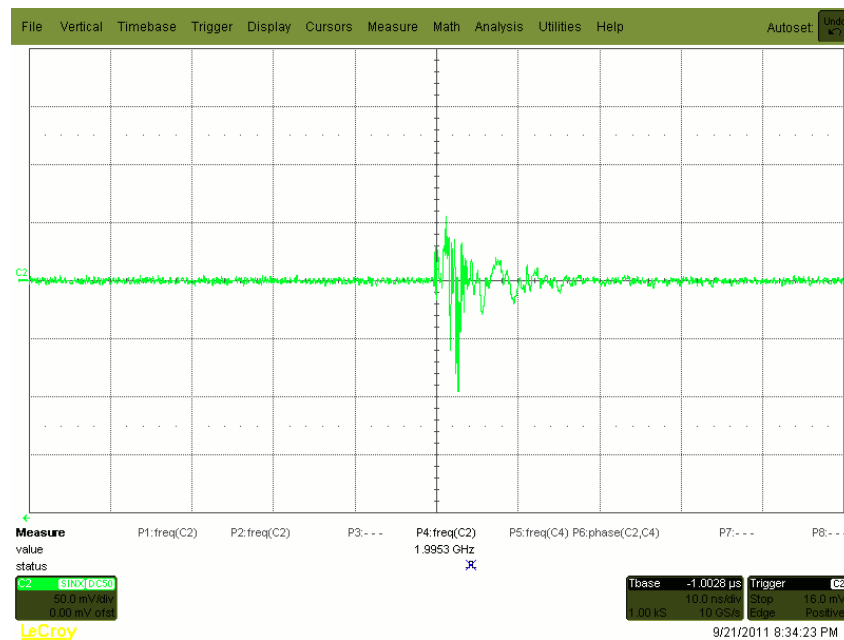
Figure 14.34: The output signal in the time domain for Prototype n° 3 with current consumption optimization.
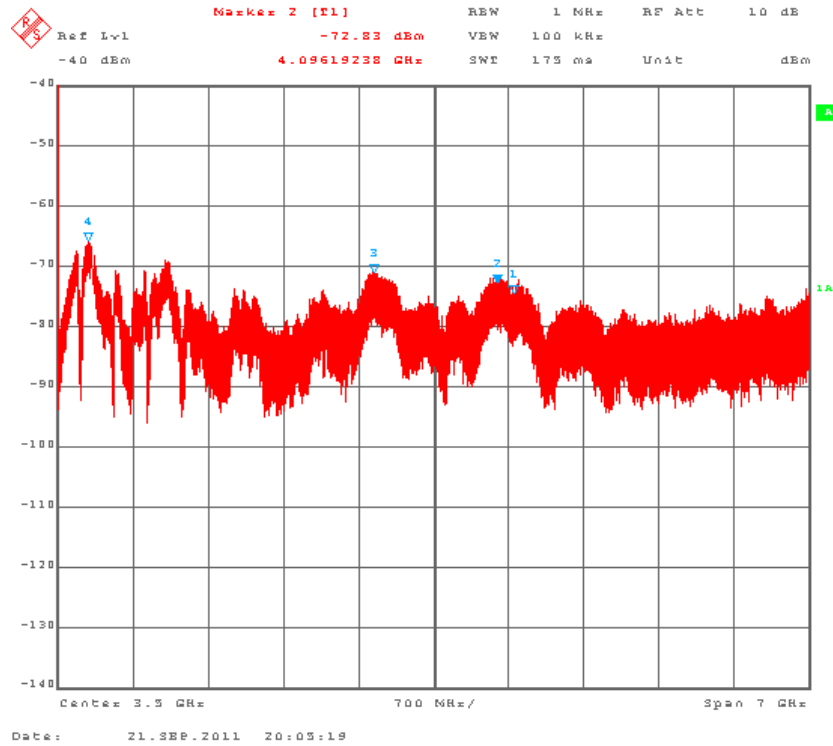
Figure 14.35: The output signal in the frequency domain for Prototype n° 3 with current consumption optimization.

14.6.3 Tests with Khepera modulator

As the working frequency is close to the technical limitations of the technology (that are around 4.0 GHz according to collaborators of our laboratory), the power supply to $VDD_2 = 1.94$ V instead of 1.80V. The tuning voltage is rose to the maximum voltage available on the PCB : $V_{tune} = 2.80$ V. These settings are made manually by checking on the oscilloscope and the spectrum analyser the shape of the signal. The Vtune configuration is chosen to (1110000) as it gives the best UWB output according to the desired specifications. The blue arrow shows the power at $f_0 = 2.53$ GHz with a power of about -51.3 dBm/MHz: the specifications are clearly not met in this situation. The current consumed by the circuit is $I_{VDD2} = 3350\mu$A on average for the power part (current directly used for UWB generation) and $I_{Vtune} = 2360\mu$ A on average for the delay gates part (current not directly used for UWB generation). The energy per pulse is 13100pJ/pulse.
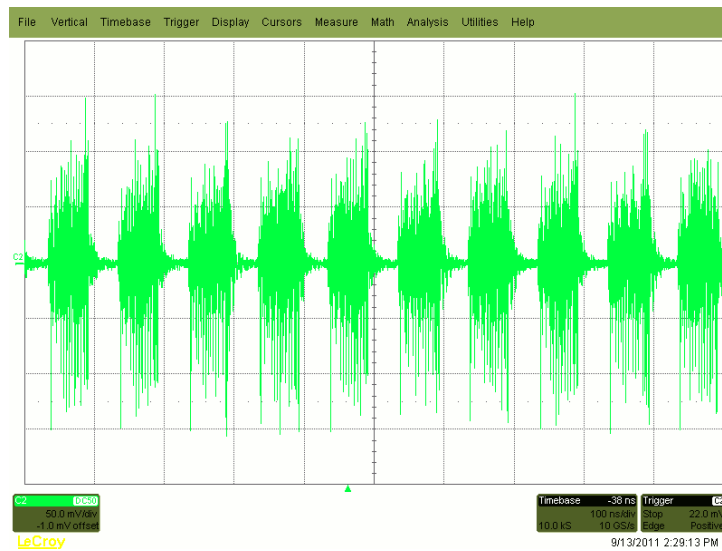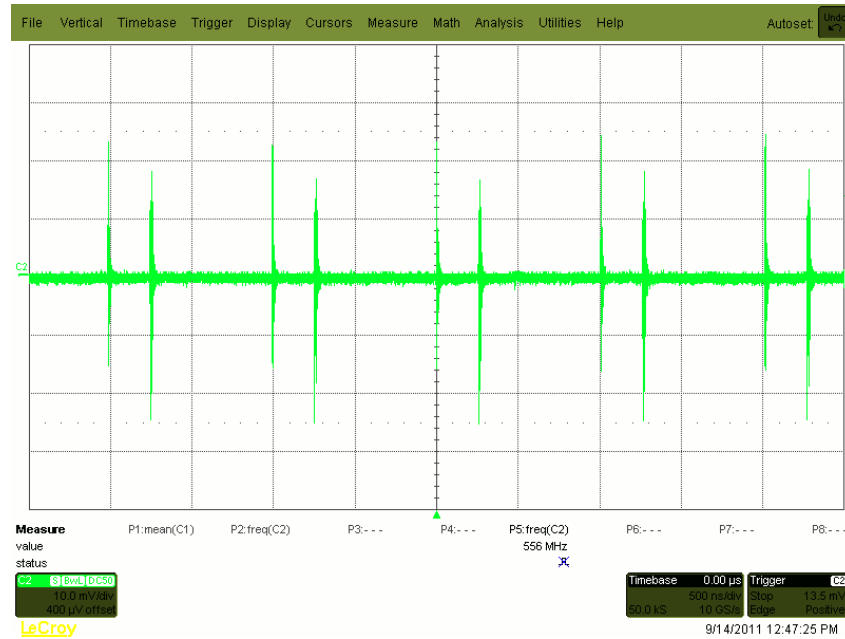
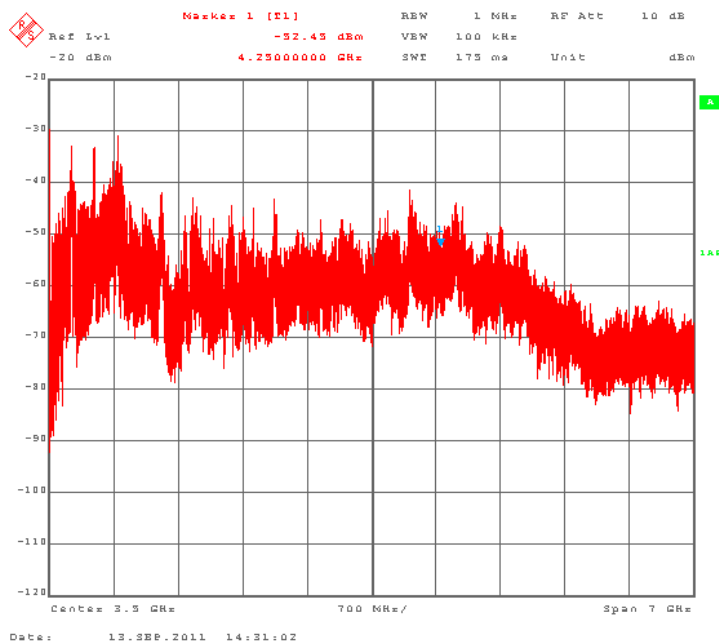Figure 14.36: The output signal in the time domain for Prototype nº 3 with $V_{tune} = (1110000)$ when driven by Khepera modulator.

Figure 14.37: Detail of the 1st pulse in the time domain for Prototype nº 3 with $V_{tune} = (1110000)$ when driven by Khepera modulator.
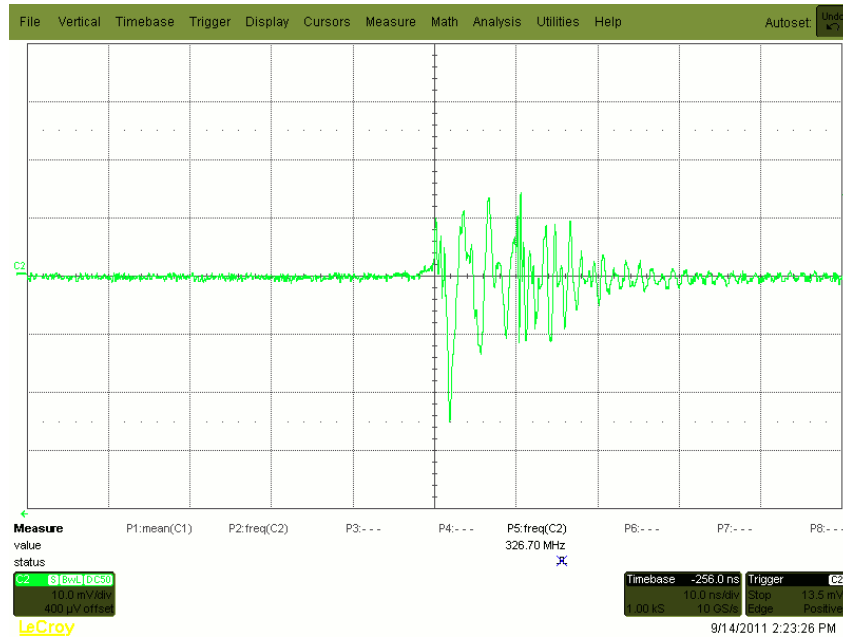
Figure 14.38: Detail of the 2nd pulse in the time domain for Prototype nº 3 with $V_{tune} =$ (1110000) when driven by Khepera modulator.
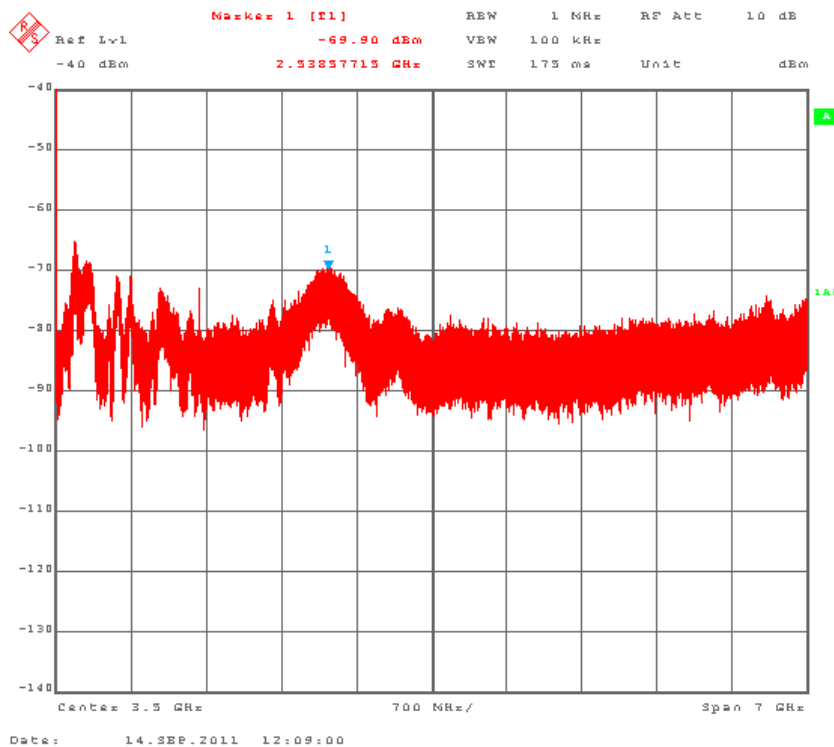
Figure 14.39: The output signal in the frequency domain for Prototype nº 3 with $V_{tune} =$ (1110000) when driven by Khepera modulator.

14.7   Conclusion and perspective

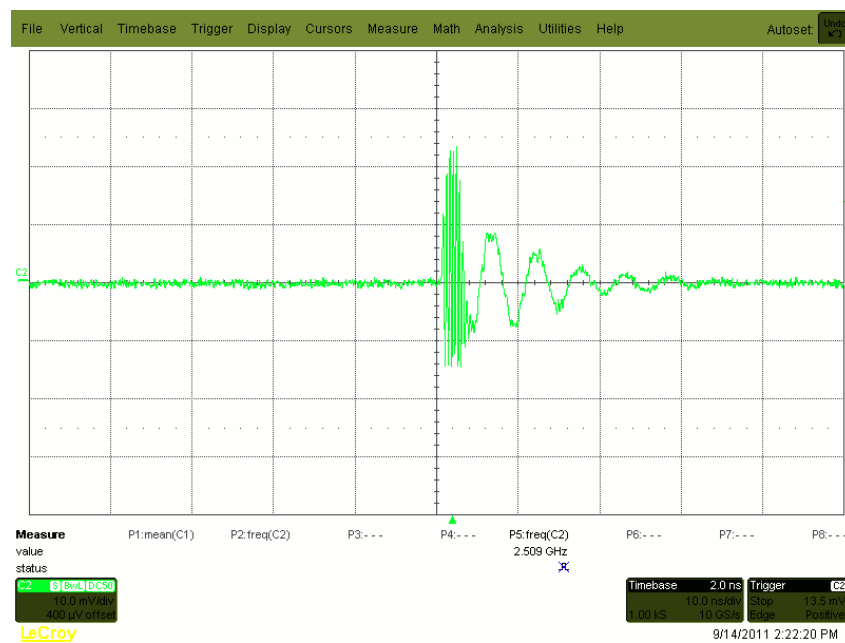We developed three prototypes of integrated low-power UWB transmitters. The simulation results we obtained previously with the three prototypes showed very low-power consumption's values that are beyond many similar circuits. Unfortunately, the UMC 0.18μm is not able to deal with signals that are short enough to reach the 4.25GHz frequency range. This is a known problem that other researchers in our laboratory have already faced by using this technology: although the technology reaches its working limits at 4.0 GHz, the model used for simulations does not take into account this effect and gives apparently good results even above this frequency. However, if we neglect the fact we have a lower frequency, we demonstrate that the principles we describe in this work give the expected results; the prototypes could reach the target frequency of 4.25GHz if they are used with a smaller and faster technology as it is done in similar publications (see Table 14.1).

	Bandwidth	Technology	E_{pulse} [pJ]	Comments
Prototype nº 1	1.5 to 2.0 GHz	UMC 0.18μ	810	As one output does not work, we cannot compare. The simulated energy per pulse is 110pJ/pulse.
Prototype nº 2	3.5 to 4.0 GHz	UMC 0.18μ	325	This is our best result. The simulated energy per pulse is 430pJ/pulse.
Prototype nº 3	3.5 to 4.2 GHz	UMC 0.18μ	2310	$V_{tune} = 1111100$. The simulated energy per pulse is 100pJ/pulse.
[79]	0.5 to 5.0 GHz	Digital CMOS 0.18μ	50	High datarate (2.5GB/s)
[82]	3.1 to 5.0 GHz	CMOS 0.18μ	210	High datarate (0.5GB/s)
[83]	3.5 to 4.5 GHz	CMOS 0.13μ	470	Maximum power is -58dBm
[84]	3.1 to 10.6 GHz	CMOS 0.18μ	9.9	Datarate is 100MHz

[85]	2.8 to 3.8 GHz	CMOS 90nm	250	Datarate is 1MHz

Table 14.1: Comparison with the state of the art

The prototype n° 1 is the closest to our original principle as exposed in Chapter 11 but it is too complex and, according to experimentation, this complexity is not required for a good UWB synthesis. One drawback of Prototype n° 1 is that it uses PMOS transistors and need a balun (not used because of the defective *pulse up* signal) for working and generating a convenient UWB signal. The measurements of this prototype cannot be well compared to the others because we have one half of the signal that is missing. We can reasonable expect that is we had the other half, the frequency would reach about 3.3GHz. Assuming the model used for simulations is accurate, we can expect a power consumption of about 110pJ/pulse. After sending the circuit to the foundry, we discovered that an article (see [79]) and a patent (see [80]) already describe this architecture. This motivates us to find another architecture with better expected performance.

The Prototype n° 2 shows the best results and is simpler than the n° 1. The use of an internal balun transformer for combining positive and negative impulse increases the efficiency of the consumed power. Using only 8 levels instead of the hundreds as in Prototype n° 1 decrease the complexity, the number of stage required for amplification and thus the power consumption. However, it does not reach the target bandwidth of 4.0 to 4.5 GHz. It offers a good balance between complexity, signal synthesis accuracy and low power requirements. Assuming the model used for simulations is accurate, we can expect a power consumption of about 430pJ/pulse. In practice, we obtain 325pJ/pulse that is much better than the simulations and even goes beyond some results from the state of the art (see Table 14.1). If we use another technology that is more suited for very high frequency design, we could expect to reach all the targets.

The prototype n° 3 is a variation of Prototype n° 2 that uses transient commutation of inverters to produce a signal. It has a huge power consumption that does not appear at all during simulations. We measure that the current drawn by the circuit when is is steady is about 2.2mA which should not be so high according to its working principle. We conjecture that there is a problem like a short circuit or an undesired parasitic behaviour we do not see in simulation. An important point to take care of it is that we designed this transmitter for testing a new idea because we had time before the tape-out and we did not want to give it an impulse generator

circuit as done with the other prototypes because we wanted to have the choice for the excitation signal.

This Part III show and demonstrate new architecture for UWB low-power transmitter. However, these low-power architecture can be used for the synthesis of any other signal, even not UWB. We can extend the concept to other type of signals or by having banks of pre-recorded signals as in a function generator. The signal can be recorded in the silicium and played when desired upon request; it can also be repeated in a circular way for generating periodic signals.

Chapter 15

Conclusion

15.1 Contributions made in this work

In this work, we achieve the following contributions :

- We demonstrate that a complete UWB testbed can be built with conventional discrete-components at a reasonable cost;

- We summarized all the knowledge required by anyone who wants to build exactly the same testbed;

- We demonstrate, with this testbed, that the PID algorithm described in [15] is more robust against interference that conventional ones and allows synchronization in concurrent communication environment (see [26]);

- With the testbed, a new ranging algorithm described in [10] is validated and demonstrated as more efficient than the other ones;

- With the testbed, a new security algorithm described in [36] is validated and demonstrated as more efficient than the other ones;

- We develop a complete mathematical study about generic UWB signals (sine with square window, with Gaussian envelope and truncated Gaussian envelope) and their corresponding spectra; we use these results to build efficient and well design UWB transmitter;

- We developed, for the testbed, a Low-Noise Amplifier with wide bandwidth (500 MHz), very low noise-figure (2.2 dB), high gain (30 dB) and voltage-controlled gain for AGC

purpose, which out-performs most of integrated equivalent design described in publications;

- We developed, for the testbed, a generic UWB transmitter with square window envelope that can be tuned in order to fulfil with a high accuracy the FCC standard regulation; such a compliance is required in order to publish new results in a realistic environment;

- We developed, for the testbed, a novel receiver architecture that combines both down-conversion techniques and energy detection in one stage with the use of I/Q mixer; such a receiver was, to the best of our knowledge, never used in conventional UWB designs;

- We explore a novel architecture of integrated very low power UWB transmitter;

- Although another research group worked on exactly the same idea, we developed another new architecture in order to stay ahead of the competition; we intend to patent this new approach

- We describe and explain the knowledge required for practical construction of the devices of the testbed; although this is not a fundamental contribution to research, it could be difficult to find in only one work a description about how to do things properly because workers who have this knowledge have rarely the occasion to share it; we believe that this knowledge is as important to the quality of the obtained results than the design itself.

15.2   Future work and perspective

The U-Lite UWB testbed gives very good results concerning UWB specifications and it is widely used for several UWB research and experimental validation. However, there are improvement that can be done on the design for simplifying the construction and reducing significantly the power consumption. The LNA can be much simplified and improved by merging the three circuits (LNA + filter + power VGA) into one. This would simplify the mounting and reduce the loss due to the coaxial cable. The other elements like the transmitter and the I/Q demodulator can have a better power consumption by using switching power supply circuits instead of resistive voltage divider for which we estimated a decrease of power consumption of about 15 %. The power consumption of the UWB transmitter could also be improved by modifying its firmware such that the local oscillator is switched off between two consecutive impulses. This would imply that the FPGA that implements the IR-UWB physical layer wakes

up the oscillator before sending the pulse.

Another improvement that concerns a UWB transmitter for a UWB application more oriented to the market would be to use a SRD diode as done in our first testbed provided we do not need to control and calibrate the parameters of the signal with the same level of accuracy as done in our experimental prototype. In the case of such a design, the improvements listed at the end of Chapter 2 could be considered as well.

The CMOS low-power UWB transmitters require several improvements in order to be used in a real UWB system. The main drawback of the three prototypes is they are not able to achieve a working central frequency of 4.25 GHz because the technology is unable to reach this speed. This is a known feature of this technology and the model used in the simulator does not take this effect into account, even with corner simulations. This implies that targeting such a working frequency requires to use a smaller and faster technology and by doing so, we can reasonably expect that the three prototypes can work and achieve the specifications.

Part IV

Appendices

Chapter A

Matlab source codes

A.1 RF line design

A.1.1 Stripline calculation

See Sections 2.2.6 and D.1.1 for details.

```
1   % Matlab code for designing an RF Mictrostrip line impedance
    % James Colli-Vignarelli
    % 23 august 2006
    % LEG - EPFL
5
    % Definition of input parameters

    % Characteristic impedance
    Z0 = 50;
10  % Relative epsillon (RO4003 here)
    Eps_r = 3.38;
    % Thickness of the board (in mm)
    h = 0.508;
    % Thickness of the track (in um)
15  t = 35;

    % Calculation of intermediate variables :
    A = Z0*sqrt((Eps_r+1)/2)/60 + (Eps_r-1)*(0.23 + (0.11/Eps_r))/(Eps_r+1)
    B = 60*pi*pi/(Z0*sqrt(Eps_r))
20
    % Calculation of microstrip - approximation of first order (w in mm):
```

```
     if A > 1.52
         w = h*(8*exp(A)/(exp(2*A)-2))
     else
25       w = (h*2/pi)*(B-1-log(2*B-1)+ (Eps_r-1)*(log(B-1) + 0.39 - ...
             (0.61/Eps_r))/(2*Eps_r) )
     end


     % Correction of second order (thickness of the microstrip):
30
     %conversion um into mm:
     t = t/1000;


     % calculation correction
35   if (w/h) < 1/(2*pi)
         delta_w = 1.25*t*(1 + log(4*pi*w/t))/pi;
     else
         delta_w = 1.25*t*(1 + log(2*h/t))/pi
     end
40
     % actualisation of the width w:
     w_eff = w + delta_w


     % conversion into mils
45   w_eff_mils = w_eff*1000/25.4


     % End of file
```

A.1.2   Coplanar Waveguide calculation

See Sections 6.2.2 for details.

```
1    % James Collli-Vignarelli
     % Matlab script for calculating the impedance of
     % Coplanar Waveguide with Ground
     % Reference: Transmission Line Design Handbook, Bian C. Wadell, page 79
5    % 13 February 2008


     % Parameters of the board:


     % Height (or thickness) of the board (in mm)
10   h = 0.8;
     h = h*1000/25.4; % conversion in mils
```

```
     % Thickness of the metal layer (in microns)
     t = 35.0;
15   t = t/25.4; % conversion in mils

     % Relative permittivity
     Eps_r = 3.6;

20   % Parameters of the lines:

     % Width of the signal track (in any units while it is the same as b)
     a = 2.1;

25   % Width between the two ground lines (in any units while it is the same as a)
     b = 2.54;

     % LINE CALCULATION

30   k = a/b;
     k_tick = sqrt(1 - k*k);

     k1 = tanh(pi*a / (4*h)) / tanh(pi*b / (4*h));
     k1_tick = sqrt(1 - k1*k1);
35
     K = ellipke(k);
     K_tick = ellipke(k_tick);

     K1 = ellipke(k1);
40   K1_tick = ellipke(k1_tick);

     % Effective permittivity calculation:

     Eps_eff = (1 + Eps_r*(K_tick*K1) / (K*K1_tick)) / (1 + (K_tick*K1) / (K*K1_tick));
45
     % Characteristic impedance calculation:

     Z0 = (120*pi / sqrt(4*Eps_eff)) * (1 / ( (K/K_tick) + (K1/K1_tick) ))

50   % END OF FILE
```

A.1.3   RFC stripline calculation

See Section 2.3.2 for details.

```matlab
% Matlab code for designing an RFC microstrip
% James Colli-Vignarelli
% 23 august 2006
% LEG - EPFL

% Definition of input parameters

% Characteristic impedance
Z0 = 50;
% Relative epsillon (RO4003 here)
Eps_r = 3.38;
% Thickness of the board (in mm)
h = 0.508;
% Thickness of the track (in um)
t = 35;
% Width of the track (in mils)
w = 10;
% Frequency to reject (in Hz)
f = 4.31e9;
% Resistivity dof the material of the track (i.e. copper) (ohm*meter)
rho = 17e-9; %Cu
% DC current in the line (A):
I = 0.05;


% Conversion w in mm :
w_mm = w*25.4/1000;
% Conversion t in metres:
t = t/1000000;
% Conversion w in metres:
w_m = w_mm/1000;
% Conversion h in metres:
h = h/1000;


% Correction of relative epsillon due to the air on one side :
Eps_RE = ((Eps_r+1)/2) + ((Eps_r-1)/(2*sqrt(1+(10*h/w_m)))) - ...
(((Eps_r-1)*t/h)/(4.6*sqrt(w_m/h)))


% Calculation of the lenght L of the RFC microstrip in mm (1/4 wavelenght):
```

```
     L = 1000 *3e8/(4*f*sqrt(Eps_RE))
40   L_mils = L *1000/25.4


     % L in meters:
     L = L/1000;


45   % Calculation of the resistance of the line (in mOhm):
     R = rho*L/(t*w_m);
     R_mOhm = R*1000


     % Power dissipated in the line (in uW):
50   P_uW = 1000000*I*I*R


     % End of file
```

A.1.4   Microstrip inductance calculation

See Section D.1.1 for details.

```
1    % Design of a microstrip inductance on PCB
     % James Colli-Vignarelli
     % 9th of january 2007
     % LEG - EPFL
5
     % Reference : IPC-2251


     % Definition of input parameters :


10   % thickness of the track (in um)
     T = 35;
     % width of the track (in mils)
     W = 20;
     % lenght of the track (in mils)
15   L = 30;
     % thickness of the board (in mils)
     H = 20;
     % Relative epsillon
     Eps_r =3.4;
20   % Conversion in mils
     T_m = T/25.4;


     % Impedance calculation (in ohm):
```

```
    Z0 = 87* (log(5.98*H/(0.8*W +T))) /sqrt(Eps_r+1.41)
25

    % intrinsic propagation delay (in ps) :
    Tpd = (L/1000) * 84.75 * sqrt(0.475 * Eps_r + 0.67)


    % intrinsic line capacitance (in pF):
30  C0 = (L/1000) * Tpd / Z0


    % intrinsic line inductance (in nH):
    L0 = Z0 * Z0 * C0 / 12


35  % End of file
```

A.2   Numeric applications

A.2.1   Matlab code for α calculation

See Section 3.2.2 for details.

```
1  % Time-Frequency relation resolution


   B = 0.5; % BW @ -10 DB
   fo = 4.25;
5

   alpha =12.46;
   beta = 1 +(B/(2*fo));


   A = (sinc((1+beta)*alpha)-sinc((1-beta)*alpha))/(sinc(2*alpha)-1)
```

A.2.2   Matlab code for Gauss integral error estimation with Chu estimation

See Section K.2 for details.

```
1  % Chu estimation accuracy


   X = linspace(-6, 6, 1000);
   Y = 0.5*(1+erf(X/sqrt(2)));
5
   % cf : http://fr.wikipedia.org/wiki/Fonction_d'erreur
   ERF = sign(X).*sqrt(1-exp(-2*X.*X/pi));
   Z = 0.5*(1 + ERF);
```

```
10   subplot(3,1,1)
     plot(X,Y,'r.-')
     title('Exact gaussian bell integration')
     xlabel('X')
     ylabel('Y')
15   grid on;

     subplot(3,1,2)
     plot(X,Z)
     title('Approximated gaussian bell integration')
20   xlabel('X')
     ylabel('Z')
     grid on;

     subplot(3,1,3)
25   plot(X,Y-Z)
     title('Approximated gaussian bell integration')
     xlabel('X')
     ylabel('error')
     grid on;
```

A.2.3   Matlab code for weight calculation

See Section 11.2.5 for details.

```
1    % Etude generation signal UWB

     close all;
     clear all;
5    goldnumber = 1024*128;
     shift_goldnumber = 180;
     Fs = 100e9;                    % Sampling frequency
     T = 1/Fs;                      % Sample time
     L = goldnumber;                % Length of signal
10   t = (0:L-1)*T;                 % Time vector

     NFFT = goldnumber;
     f = (0:1/(L-1):1)*Fs;
     Y = 10e-5 + gaussmf(f,[240e6 4250e6]);
15
     %Plot single-sided amplitude spectrum.
```

```matlab
    figure;
    subplot(3,1,1)
    plot(f,10*log10(abs(Y)))
20  xlim([1.0e9 8e9])
    title('Single-Sided Amplitude Spectrum of y(t)')
    xlabel('Frequency (Hz)')
    ylabel('|Y(f)| [dB]')
    grid on;
25


    % Inverse :
    Z = ifft(Y, NFFT, 'nonsymmetric');
    Z = ifftshift(Z);
30
    %Z = real(Z);
    Z = real(Z)*sqrt(1 + (imag(Z)/real(Z))^2);


    %Z(shift_goldnumber+1:2*shift_goldnumber)=wrev(Z(1:shift_goldnumber));
35  O = zeros(1, goldnumber);
    O(goldnumber/2-shift_goldnumber:goldnumber/2+shift_goldnumber)
    = Z(goldnumber/2-shift_goldnumber:goldnumber/2+shift_goldnumber);
    Z = O;


40  % % For removing non extremal points
    for n=1: goldnumber

        if (n ~=1 && n ~=goldnumber)
            if ( (Z(n-1)<Z(n)&&Z(n)<Z(n+1)) || (Z(n+1)<Z(n)&&Z(n)<Z(n-1)))
45              O(n) = 0.0;
            end
        end
    end;
    Z = O;
50  %
    % Z(goldnumber/2-shift_goldnumber:goldnumber/2+shift_goldnumber)
    %
    display = Z(goldnumber/2-shift_goldnumber:goldnumber/2+shift_goldnumber);
    display/max(display)
55
    % For repeting extremal points
    % for n=1: goldnumber
```

```
%      if (Z(n) ~=0.0)
%          O(n-3) = Z(n);
60  %          O(n-2) = Z(n);
%          O(n-1) = Z(n);
%          O(n+1) = Z(n);
%          O(n+2) = Z(n);
%          O(n+3) = Z(n);
65  %      end
% end;
% Z = O;


Z = Z/max(Z);
70

subplot(3,1,2)
plot(Fs*t(1:goldnumber-1),Z(1:goldnumber-1),'r.-')
xlim([goldnumber/2-2*shift_goldnumber goldnumber/2+2*shift_goldnumber])
title('Signal (inverse FFT)')
75  xlabel('time (x 10 ps)')
ylabel('|y(t)|')
grid on;


X = fft(Z,NFFT);
80

X = X/max(X);


% redo of the spectrum
subplot(3,1,3)
85  plot(f,10*log10(abs(X)))
xlim([1.0e9 10e9])
title('Single-Sided Amplitude Spectrum of y(t)')
xlabel('Frequency (Hz)')
ylabel('|Y(f)|')
90  grid on;
```

A.2.4   Matlab code for weight verification

See Section 11.2.5 for details.

```
1  % Etude generation signal UWB
```

```
    close all;
    clear all;
 5  goldnumber = 1024*128;
    shift_goldnumber = 180;
    Fs = 100e9;                    % Sampling frequency
    T = 1/Fs;                      % Sample time
    L = goldnumber;                % Length of signal
10  t = (0:L-1)*T;                 % Time vector

    NFFT = goldnumber;
    f = (0:1/(L-1):1)*Fs;

15  % Z = [0,0,0,0,0,-0.0157,...
    %      0,0,0,0,0,0,0,0,0,0,0,0.0267,...
    %      0,0,0,0,0,0,0,0,0,0,0,-0.0437,...
    %      0,0,0,0,0,0,0,0,0,0,0.0693,...
    %      0,0,0,0,0,0,0,0,0,0,0,-0.1063,...
20  %      0,0,0,0,0,0,0,0,0,0,0,0.1562,...
    %      0,0,0,0,0,0,0,0,0,0,0,-0.2199,...
    %      0,0,0,0,0,0,0,0,0,0,0.3028,...
    %      0,0,0,0,0,0,0,0,0,0,0,-0.3998,...
    %      0,0,0,0,0,0,0,0,0,0,0,0.5059,...
25  %      0,0,0,0,0,0,0,0,0,0,-0.6183,...
    %      0,0,0,0,0,0,0,0,0,0,0,0.7334,...
    %      0,0,0,0,0,0,0,0,0,0,0,-0.8338,...
    %      0,0,0,0,0,0,0,0,0,0,0,0.9086,...
    %      0,0,0,0,0,0,0,0,0,0,-0.9642,...
30  %      0,0,0,0,0,0,0,0,0,0,0,0,1,...
    %      0,0,0,0,0,0,0,0,0,0,0,-0.9642,...
    %      0,0,0,0,0,0,0,0,0,0,0.9086,...
    %      0,0,0,0,0,0,0,0,0,0,0,-0.8338,...
    %      0,0,0,0,0,0,0,0,0,0,0,0.7334,...
35  %      0,0,0,0,0,0,0,0,0,0,-0.6183,...
    %      0,0,0,0,0,0,0,0,0,0,0.5059,...
    %      0,0,0,0,0,0,0,0,0,0,0,-0.3998,...
    %      0,0,0,0,0,0,0,0,0,0,0.3028,...
    %      0,0,0,0,0,0,0,0,0,0,-0.2199,...
40  %      0,0,0,0,0,0,0,0,0,0,0,0.1562,...
    %      0,0,0,0,0,0,0,0,0,0,-0.1063,...
    %      0,0,0,0,0,0,0,0,0,0,0,0.0693,...
    %      0,0,0,0,0,0,0,0,0,0,-0.0437,...
```

```
   %        0,0,0,0,0,0,0,0,0,0,0,0.0267,...
45 %        0,0,0,0,0,0,0,0,0,0,0,-0.0157,...
   %        0,0,0];


   % Z = [0,0,0,0,0,-2,...
   %        0,0,0,0,0,0,0,0,0,0,0,3,...
50 %        0,0,0,0,0,0,0,0,0,0,0,-5,...
   %        0,0,0,0,0,0,0,0,0,0,8,...
   %        0,0,0,0,0,0,0,0,0,0,0,-13,...
   %        0,0,0,0,0,0,0,0,0,0,19,...
   %        0,0,0,0,0,0,0,0,0,0,0,-27,...
55 %        0,0,0,0,0,0,0,0,0,0,37,...
   %        0,0,0,0,0,0,0,0,0,0,0,-47,...
   %        0,0,0,0,0,0,0,0,0,0,62,...
   %        0,0,0,0,0,0,0,0,0,0,-75,...
   %        0,0,0,0,0,0,0,0,0,0,0,89,...
60 %        0,0,0,0,0,0,0,0,0,0,0,-102,...
   %        0,0,0,0,0,0,0,0,0,0,0,111,...
   %        0,0,0,0,0,0,0,0,0,0,0,-118,...
   %        0,0,0,0,0,0,0,0,0,0,0,122,...
   %        0,0,0,0,0,0,0,0,0,0,0,-118,...
65 %        0,0,0,0,0,0,0,0,0,0,111,...
   %        0,0,0,0,0,0,0,0,0,0,0,-102,...
   %        0,0,0,0,0,0,0,0,0,0,0,89,...
   %        0,0,0,0,0,0,0,0,0,0,0,-75,...
   %        0,0,0,0,0,0,0,0,0,0,62,...
70 %        0,0,0,0,0,0,0,0,0,0,0,-47,...
   %        0,0,0,0,0,0,0,0,0,0,0,37,...
   %        0,0,0,0,0,0,0,0,0,0,-27,...
   %        0,0,0,0,0,0,0,0,0,0,0,19,...
   %        0,0,0,0,0,0,0,0,0,0,0,-13,...
75 %        0,0,0,0,0,0,0,0,0,0,0,8,...
   %        0,0,0,0,0,0,0,0,0,0,-5,...
   %        0,0,0,0,0,0,0,0,0,0,0,3,...
   %        0,0,0,0,0,0,0,0,0,0,0,-2,...
   %        0,0,0];
80
   % Z = [0,0,0,0,0,-2,...
   %        0,0,0,0,0,0,0,0,0,0,0,3,...
   %        0,0,0,0,0,0,0,0,0,0,0,-5,...
   %        0,0,0,0,0,0,0,0,0,0,8,...
```

```
85    %        0,0,0,0,0,0,0,0,0,0,0,-12,...
      %        0,0,0,0,0,0,0,0,0,0,0,17,...
      %        0,0,0,0,0,0,0,0,0,0,0,-24,...
      %        0,0,0,0,0,0,0,0,0,0,33,...
      %        0,0,0,0,0,0,0,0,0,0,0,-43,...
90    %        0,0,0,0,0,0,0,0,0,0,0,55,...
      %        0,0,0,0,0,0,0,0,0,0,-67,...
      %        0,0,0,0,0,0,0,0,0,0,0,80,...
      %        0,0,0,0,0,0,0,0,0,0,0,-91,...
      %        0,0,0,0,0,0,0,0,0,0,99,...
95    %        0,0,0,0,0,0,0,0,0,0,-105,...
      %        0,0,0,0,0,0,0,0,0,0,0,109,...
      %        0,0,0,0,0,0,0,0,0,0,0,-105,...
      %        0,0,0,0,0,0,0,0,0,0,99,...
      %        0,0,0,0,0,0,0,0,0,0,0,-91,...
100   %        0,0,0,0,0,0,0,0,0,0,0,80,...
      %        0,0,0,0,0,0,0,0,0,0,0,-67,...
      %        0,0,0,0,0,0,0,0,0,0,55,...
      %        0,0,0,0,0,0,0,0,0,0,0,-43,...
      %        0,0,0,0,0,0,0,0,0,0,0,33,...
105   %        0,0,0,0,0,0,0,0,0,0,-24,...
      %        0,0,0,0,0,0,0,0,0,0,0,17,...
      %        0,0,0,0,0,0,0,0,0,0,0,-12,...
      %        0,0,0,0,0,0,0,0,0,0,0,8,...
      %        0,0,0,0,0,0,0,0,0,0,-5,...
110   %        0,0,0,0,0,0,0,0,0,0,0,3,...
      %        0,0,0,0,0,0,0,0,0,0,0,-2,...
      %        0,0,0];
      %

115   Z = [0,0,0,0,0,0,...
           0,0,0,0,0,0,0,0,0,0,0,0,...
           0,0,0,0,0,0,0,0,0,0,0,0,...
           0,0,0,0,0,0,0,0,0,0,1,...
           0,0,0,0,0,0,0,0,0,0,0,-1,...
120        0,0,0,0,0,0,0,0,0,0,0,1,...
           0,0,0,0,0,0,0,0,0,0,0,-2,...
           0,0,0,0,0,0,0,0,0,0,2,...
           0,0,0,0,0,0,0,0,0,0,0,-3,...
           0,0,0,0,0,0,0,0,0,0,0,4,...
125        0,0,0,0,0,0,0,0,0,0,-5,...
```

```
          0,0,0,0,0,0,0,0,0,0,0,6,...
          0,0,0,0,0,0,0,0,0,0,0,-7,...
          0,0,0,0,0,0,0,0,0,0,0,7,...
          0,0,0,0,0,0,0,0,0,0,-8,...
130       0,0,0,0,0,0,0,0,0,0,0,8,...
          0,0,0,0,0,0,0,0,0,0,0,-8,...
          0,0,0,0,0,0,0,0,0,0,7,...
          0,0,0,0,0,0,0,0,0,0,0,-7,...
          0,0,0,0,0,0,0,0,0,0,0,6,...
135       0,0,0,0,0,0,0,0,0,0,0,-5,...
          0,0,0,0,0,0,0,0,0,0,4,...
          0,0,0,0,0,0,0,0,0,0,0,-3,...
          0,0,0,0,0,0,0,0,0,0,0,2,...
          0,0,0,0,0,0,0,0,0,0,-2,...
140       0,0,0,0,0,0,0,0,0,0,0,1,...
          0,0,0,0,0,0,0,0,0,0,0,-1,...
          0,0,0,0,0,0,0,0,0,0,0,1,...
          0,0,0,0,0,0,0,0,0,0,0,0,...
          0,0,0,0,0,0,0,0,0,0,0,0,0,...
145       0,0,0,0,0,0,0,0,0,0,0,0,0,...
          0,0,0];



    Z = Z/max(Z);
150
    %Z(shift_goldnumber+1:2*shift_goldnumber) = wrev(Z(1:shift_goldnumber));
    O = zeros(1, goldnumber);
    O(goldnumber/2-shift_goldnumber:goldnumber/2+shift_goldnumber) = Z;
    Z = O;
155
    % % For removing non extremal points
    for n=1: goldnumber

        if (n ~=1 && n ~=goldnumber)
160         if ( (Z(n-1)<Z(n)&&Z(n)<Z(n+1)) || (Z(n+1)<Z(n)&&Z(n)<Z(n-1)))
                O(n) = 0.0;
            end
        end
    end;
165 Z = O;
```

```
    display = Z(goldnumber/2-shift_goldnumber:goldnumber/2+shift_goldnumber);
    display/max(display);


170 %For repeting extremal points
    % for n=1: goldnumber
    %     if (Z(n) ~=0.0)
    %         O(n-3) = Z(n);
    %         O(n-2) = Z(n);
175 %         O(n-1) = Z(n);
    %         O(n+1) = Z(n);
    %         O(n+2) = Z(n);
    %         O(n+3) = Z(n);
    %     end
180 % end;
    % Z = O;


    Z = Z/max(Z);


185 subplot(2,1,1)
    plot(Fs*t(1:goldnumber-1),Z(1:goldnumber-1),'r.-')
    xlim([goldnumber/2-2*shift_goldnumber goldnumber/2+2*shift_goldnumber])
    title('Signal (inverse FFT)')
    xlabel('time (x 10 ps)')
190 ylabel('|y(t)|')


    X = fft(Z,NFFT);


    X = X/max(X);
195

    % redo of the spectrum
    subplot(2,1,2)
    plot(f,10*log10(abs(X)))
    xlim([1.0e9 10e9])
200 title('Single-Sided Amplitude Spectrum of y(t)')
    xlabel('Frequency (Hz)')
    ylabel('|Y(f)|')
    grid on;


205 % end of file
```

Chapter B

The oscillator's firmware

This section presents the oscillator's firmware code that is implemented in the ATtiny13 microcontroller. This firmware has a very simple task to do: setting the correct parameters in the synthesizer's registers in order to generate a 4.25GHz sine wave. This means that the firmware works only once, at the power on, and then the microcontroller can stop working. If required, the firmware can be restarted manually by resetting the microcontroller with the reset switch, as mentioned earlier. To simplify the programming and the debug, we use a highly hierarchical structure to write the firmware by applying *divide and conquer* approach. Doing like this helps to focus on one thing at a time and to reduce mistakes. It helps also to test separately every function of the code and to improve later the firmware if required. We first present the internal registers of the synthesizers and how to use them. Then, we present the elementary functions in the code we use to communicate physically with the synthesizer and how the code is structured. Finally, we present the obtained code as a whole such that the reader can copy and paste it in the ATMEL's software for programming the microcontroller.

During the development of the firmware, we decided to first place the synthesizer's parameter values in the SRAM memory instead of microcontroller's registers and, then, to transfer them to the synthesizer's registers. Doing like this helps to locate and to modify any parameter's value quickly and safely without the risk to alter and corrupt the firmware code. The only small drawback of this approach is an increase of the execution time but this has no importance at all while the firmware is executed once at the start-up.

The structure of the firmware code is presented in Figure B.1, which gives an overview of how the code works and the relation between the different subroutines, and Table B.1 summarises the function of the microcontroller's registers used in the code. When the firmware

starts, the *reset* is the first part of the code to be executed during which registers are initialized, the starting position of Stack Pointer is defined and the synthesizer's parameters are loaded in the SRAM. Then, in the *main* part, the subroutine *Load_PLL* is called for sending parameters to the synthesizer. These parameters are transmitted by blocks of 24 bits each by calling the subroutine *sendvalue*, in which the physical communication with the synthesizer is implemented. This physical communication manages the loading of the synthesizers' registers with 24-bits block of data and the protocol for addressing to the correct register. Finally, when all synthesizer's registers are loaded, the output pins are de-activated and set to zero. They remain in this state unless there is a forced new execution of the code. A block of 24 bits is transferred serially to the synthesizer's register by using the subroutine *send_bits*. Depending on whether the bit sent is a one or a zero, the subroutine *send_bits* calls the subroutines *send_one* or *send_zero* respectively.
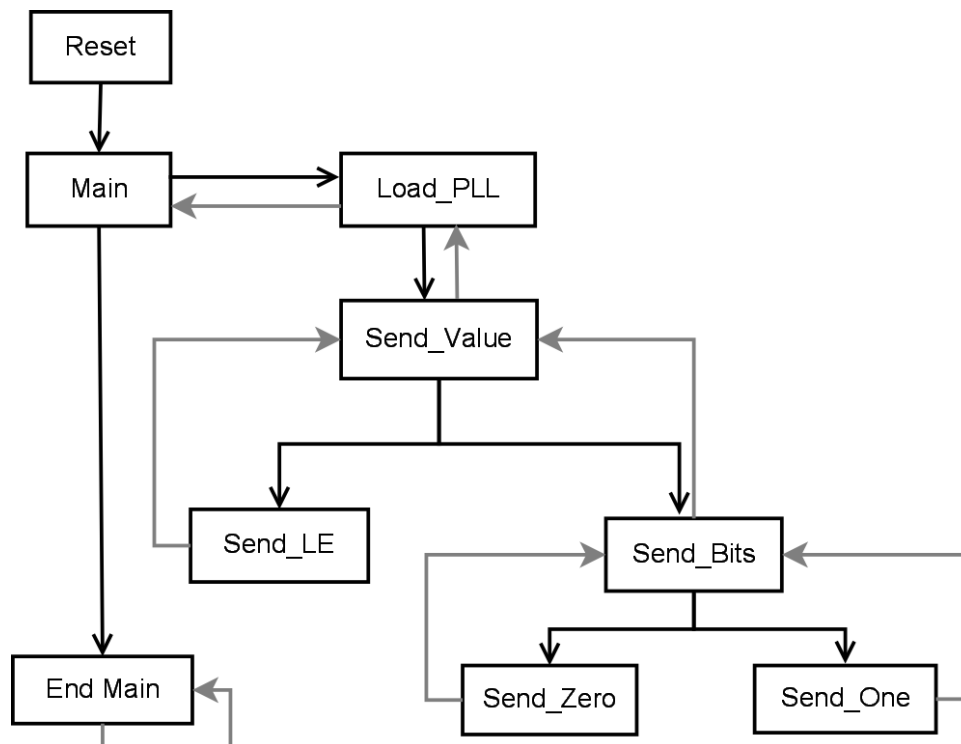
Figure B.1: Structure of the firmware's code

Register	Functionality
r16	Initializing the Stack-Pointer and configuring the direction of I/O port pin
r17	Bits counter
r18	Register counter

Z register	Pointer to the Y register
Y register	Data
r20	Variable for processing the data pointed by Z register
r21	Variable for transferring the PLL's data to the Y register

Table B.1: Description of the microcontroller's registers

B.1 The synthesizer's registers

This section presents the synthesizer's registers, how they work and how to program them in order to generate a 4.25 GHz sine wave.

B.1.1 The Shift register

As described in [X8], the synthesizer device, which is based on an Analog Devices PLL synthesizer, has four internal registers for programming the desired frequency. In our case, however, there are only three of them that need to be programmed: the *R counter*, the *N counter* and the *Initialisation Latch*. The fourth register, the *Functional Latch*, is not used. However, these registers are not loaded directly, but by the use of an intermediate 24-bit register named the *shift register*. It is in this register where the serial data that comes from the microcontroller is shifted on the rising edge of the clock, with the most significant bit first. Then, the data are transferred from the intermediate input shift register to one of the internal register of the synthesizer on the rising edge of load enable LE, mentioned previously. The input shift register is presented in Table B.2, where every bit, excepted the two MSB bits $C1$-$C2$, have a different meaning depending on the data latch where the bits are going to be transferred to (see Table B.3). That means that $C1$ and $C2$ indicate in which synthesizer's register to transfer the data from the shift register. The bits from $F1$ to $F22$ are general purpose depending on the destination register.

C2	C1	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20	F21	F22

Table B.2: The 24-bit Shift register

C2	C1	Data Latch
0	0	R counter

0	1	N counter
1	0	Function Latch
1	1	Initialisation Latch

Table B.3: Truth table for $C1$ and $C2$

B.1.2 The Initialisation Latch register

The Initialisation Latch value is given in Figure B.4 and the meaning of each bit value is described in table B.5.

P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2	C1
1	0	X	1	1	1	1	1	1	0	0	0	0	X	0	0	1	0	0	1	0	0	1	1

Table B.4: Content of the Initialisation Latch register

Bits	Value	description
C2-C1	11	Initialisation Latch
F1	0	Normal Operation
PD2-PD1	X0	Normal Operation
M3-M1	001	Digital lock detect
F2	1	Phase Detector Polarity
F3	0	Charge Pump 3-State
F5-F4	X0	No FastLock mode
TC4-TC1	0000	Timer Counter Control
CPI6-CPI1	111111	Icp = 5mA with Rcp = 4.7KΩ
P2-P1	10	Prescaler Value = 32/33

Table B.5: Function description of Initialisation Latch register

B.1.3 The R counter register

The R counter register value is given in table B.6 and Table B.7 describes the functionality of its bits.

X	DLY	SYNC	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2	C1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Table B.6: Content of the R counter register

Bit	Value	Description
C2-C1	00	R counter
R14-R1	000...000101	Divide ratio of the reference divider
ABP2-ABP1	00	Pulse Width = 3ns
T2-T1	00	Normal operation
LDP	0	3 clock cycles before lock detect
SYNC	0	Normal operation
DLY	0	Normal operation
X	0	Do not care

Table B.7: Function description of R counter register

With the exception of $R14$-$R1$, all others bits are low by default, meaning that their functionalities are not necessary for generating the desired frequency. However, the value of R-bits have been already calculated in section 5.1.2, when we wanted to define the most appropriate reference frequency to drive the PLL synthesizer. The value of these bits are set to 5, and correspond to a reference frequency of 50 MHz.

B.1.4 The N counter register

The N counter register value is given in table B.8 and Table B.9 below describes the function of its bits.

X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2	C1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	1

Table B.8: Content of N counter register

Bit	Value	Description

C2-C1	0	N counter
A6-A1	1001	A counter
B13-B1	1101	B counter
G1	0	Charge Pump Gain [9]
XX	00	Bits not used

Table B.9: Function description of N counter register

The value of A and B counters are defined by following the instructions given in [86]. These values, in combination with the modulus prescaler P defined in the Initialisation Latch register, allow to generate the output frequency such that they are spaced only by the reference frequency value divided by R, as explained in the equation below (see [86] for details).

$$f_{\text{VCO}} = \frac{[(P \cdot B) + A] \cdot f_{\text{REF IN}}}{R} = \frac{N \cdot f_{\text{REF IN}}}{R}$$

where $A < B$, and

$$\frac{f_{\text{VCO}}}{P} = \frac{4250 \text{ MHz}}{32} = 133 \text{ MHz} < 200 \text{ MHz}$$

Then, for an output frequency of 4.25 GHz, the parameters are:

- $R = 5$

- $P = 32/33$

- $f_{\text{REF IN}} = 50 \text{ MHz}$

- $N = \frac{f_{VCO}}{\text{SizeStep}} = \frac{4250 \text{ MHz}}{10 \text{ MHz}} = 425$

- $B = \text{integer} \left(\frac{N}{P} \right) = [13.28] = 13$

- $A = N - (B \cdot P) = 425 - (13 \cdot 32) = 9$

B.2 Code description

This section describes in detail the firmware organisation and how each subroutine work. The structure of the firmware code was already presented in Figure B.1 and it may be referred to as a guideline. The next section B.3 gives the whole code.

B.2.1   The reset

The reset part of the code focuses on defining the Stack Pointer register, I/O direction pins and on charging the synthesizer's data in the SRAM memory, as summarized in Figure B.2. It is divided into two sub-parts: *reset* and *loadData*.

B.2.2   The reset part

```
reset: ; Set up address (r16) in the Stack Pointer address register
ldi r16,0x8F
out spl,r16
; Clear r16
clr r16
; Global interrupt disable
CLI
; Clear carry
CLC
; Define direction for port pins
ldi r16,0x07
out DDRB,r16
; Initialize Z_register
clr r30
; Initialize Y_register
clr r28
; Initialize r21 register
clr r21
; Initialize byte counter register
ldi r18,0x03
```

B.2.3   The loadData part

```
loadData:
; Load Latch registerdata
ldi r28,$9F
ldi  r21,0x9F
```

```
st  Y,r21
ldi r21,0x80
st  -Y,r21
ldi  r21,0x93
st  -Y,r21
; LoadR-counter data
ldi  r21,0x00
st  -Y,r21
ldi  r21,0x00
st  -Y,r21
ldi  r21,0x14
st  -Y,r21
; Load N-counter data
ldi r21,0x00
st -Y,r21
ldi r21,0x0D
st -Y,r21
ldi r21,0x25
st -Y,r21
rjmp main
```

The important point to note in this code is that the Stack Pointer is located at the address $8F$ instead of $9F$ (the last address in the SRAM memory). By this way, a potential stack overflow will not erase the synthesizer's data that are stored in the address 9F. The external interruptions are disabled since they are not necessary for programming the PLL. By setting the pin register DDRB = 7, thee pins PB1 and PB2 are specified as output pins, and the remaining as input pins. These pins correspond to the MISO and the SCK pins of the microcontroller ATtiny13. Once the reset branch is finished, the synthesizer's data are stored on the SRAM memory. The Latch register's data are the first to be loaded because they are the first bytes to be transferred to the synthesizer's shift register. They are followed by R counter's data and then by N counter's data. It is important to specify that for all these registers, it is always the most significant bit to be load first. Finally, the main part is executed to begin loading the data in their corresponding register in the PLL chip. As said previously, the SRAM memory is used instead of the general purpose working register to store the synthesizer's parameters, which are going to be sent to
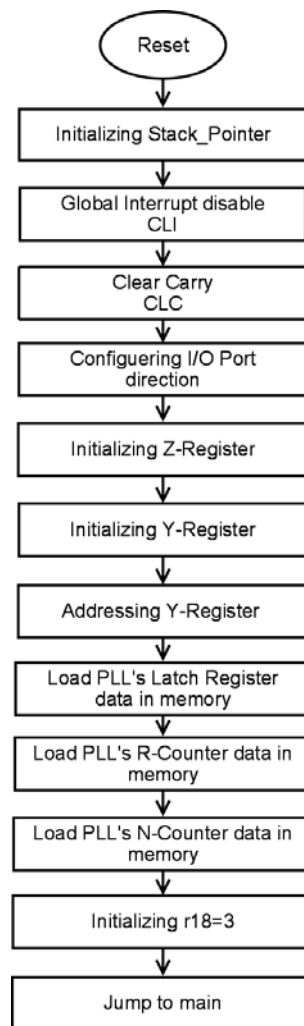
Figure B.2: Reset flow chart

the device. We decided to use the SRAM for storing the synthesizer's parameters because it helps to locate and to modify any parameter's value quickly and safely without the risk to alter and corrupt the firmware code.

B.2.4   The main

The *main* calls the subroutine *load_PLL* to transfer the synthesizer's data to the synthesizer's chip. Once this is done, it stops by deactivating the outputs of the microcontroller and entering in an infinite loop, as shown in Figure B.3.

main: rcall load_PLL
end: ; Transmission end

ldi r16,0x00
out PORTB,r16
rjmp end
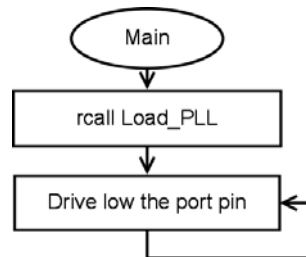
Figure B.3: Main flow chart

B.2.5 Load_PLL

This is the central part of the code as it sends data to the synthesizer's shift register. It first starts to set the Z_register in the corresponding SRAM address where it stores the first byte to send to the PLL. This byte is then loaded in the register r20 to be processed in the subroutine *sendvalue* (see Figure B.4).

load_PLL: ldi r30,$9F
ld   r20,Z
; Send Latch_register data
rcall sendvalue
ld r20,-Z
; Send R_counter data
rcall sendvalue
ld r20,-Z
; Send N_counter data
rcall sendvalue
ret

During the execution of this subroutine, it sends, for each synthesizer's register, the corresponding three bytes for programming the PLL at the required frequency. For this purpose,

before calling the subroutine *sendvalue*, we update the register r20 with the new first byte of the next PLL register to load.
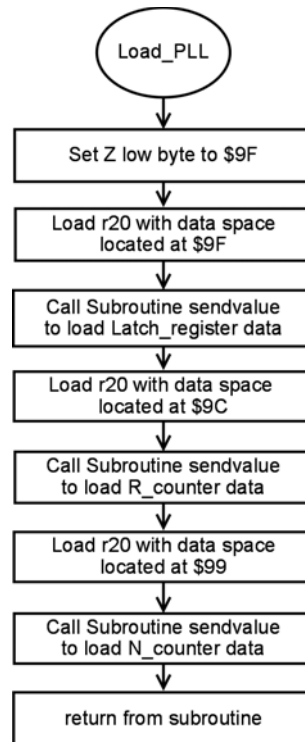
Figure B.4: Load_PLL flow chart

B.2.6   Sendvalue

This subroutine sends the three bytes that constitute one synthesizer's register (see Figure B.5). First, the value of register r18, which represents the number of bytes sent to the shift register, is saved on the stack. Then, the subroutine *send_bits* is called to send one byte. When it is finished, the value of r18 is decremented, and compared with zero. If it is equal to zero, an enable load signal LE is sent to the PLL chip to allow transferring the data saved in the PLL shift register to the PLL register defined by C2 and C1. Otherwise, the next byte to send is saved into the register r20, and the function *sendnextbyte* is executed once again to restart sending bytes. When the three bytes are transmitted, the original value of r18 that was previously stored on the Stack Pointer, is restored, and the subroutine *Load_PLL* is executed once again.

sendvalue: ; Save r18 on the stack
push r18

sendnextbyte: ; Send bytes

rcall send_bits

dec r18

cpi r18,0x00

; if r18 = 0, send enable load LE register signal

breq loadRegisterEnable

; if r18 !=0, load next byte to send

ld r20,-Z

rjmp sendnextbyte

loadRegisterEnable: rcall send_LE

end_sendvalue: ; restore r18

pop r18

; return from subroutine

ret
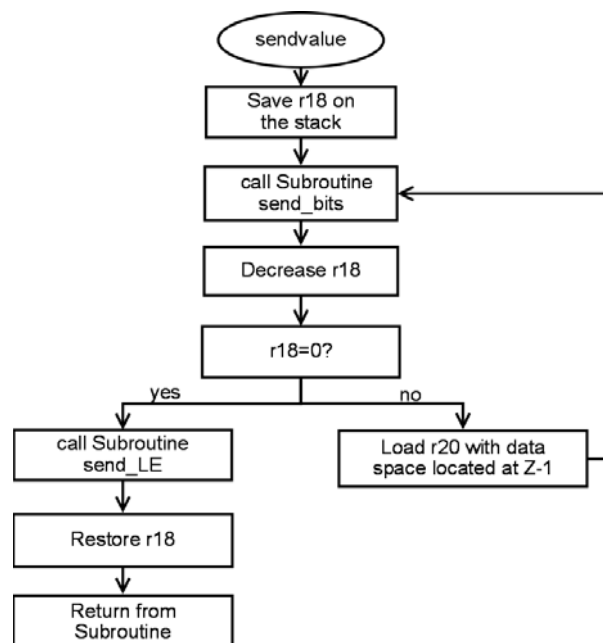
Figure B.5: Sendvalue flow chart

B.2.7   Send_bits

In this subroutine, a string of 8 bits is sent. For that purpose, the register r17 is used as a bit counter, which is decremented each time a bit is sent to the PLL chip. The bit to send depends on the value of the carry flag, which is set with the instruction rol r20. If carry flag is set to one, the subroutine *send_one* is called, otherwise, it is the subroutine *send_zero*. This loop is executed until r17 = 0. At this moment, the previous value of r17 is restored before returning to the subroutine *sendvalue* (see Figure B.6).

```
send_bits: CLC
push r17
; Initialize bits counter register
ldi r17,0x08
shift: rol r20
; If C = 1, send one
BRCS One
; If C = 0, send zero
rcall send_zero
rjmp next

One: rcall send_one
next: ; Update the value of r17
dec r17
cpi r17,0x00
; If r17 != 0 go to shift
brne shift
; If r17 = 0 restore r17 from stack
pop r17
ret
```

B.2.8   Send_one

This subroutine is called each time we want to send a 1 to the PLL chip. for doing this, the pin 8 of the PLL is set high and then, the loading is allowed by setting a high level in the SCK pin.
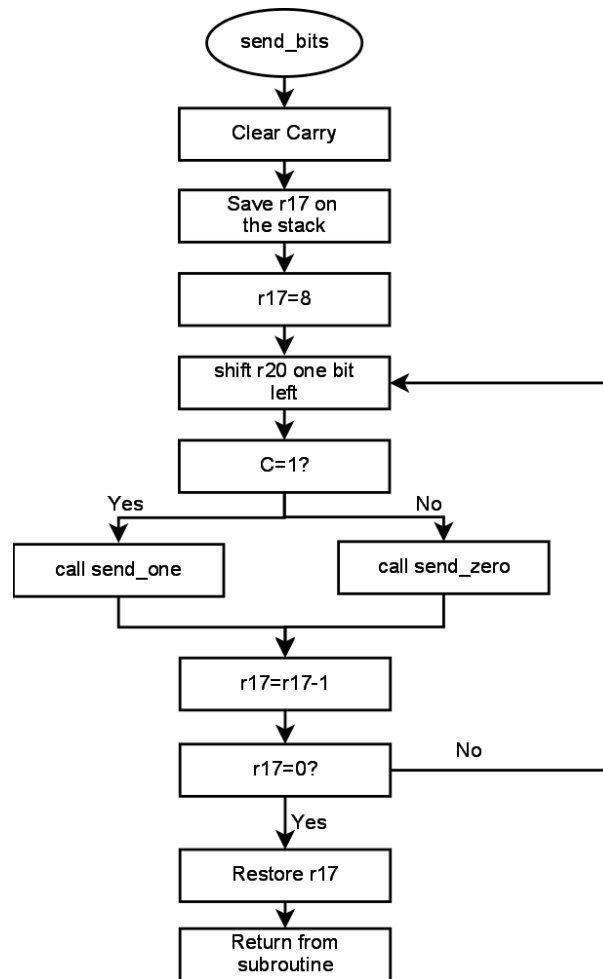
Figure B.6: Send_bits flow chart

The data is transferred into the PLL shift register on the rising edge of the CLK signal. By this way, we are sure that the bit is effectively loaded into the PLL chip. Finally, the output pin is restored to low level, as well as the previous value of the register r16 is stored on the stack (see Figure B.7).

send_one: push r16
; Put high the pin number 8 of the PLL
ldi r16,0x02
out PORTB,r16
; Enable the load of the bit into the PLL chip on the rising edge
ldi r16,0x06
out PORTB,r16

```
clr r16
out PORTB,r16
pop r16
ret
```
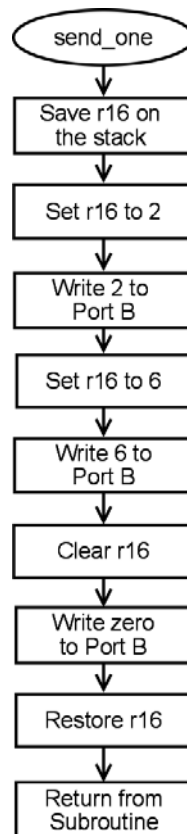

Figure B.7: Send_one flow chart

B.2.9   Send_zero

This subroutine works similarly to the subroutine *send_one*. The only difference is that instead of setting the pin 8 of the PLL chip to high level, it sets to low level. But the principle of using an CLK signal to allow the load on the PLL chip remains the same (see Figure B.8).

```
send_zero: push r16
; Put low output pin
ldi r16,0x00
```

```
out PORTB,r16
; Enable the load of the bit into the PLL chip on the rising edge
ldi r16,0x04
out PORTB,r16
clr r16
out PORTB,r16
pop r16
ret
```
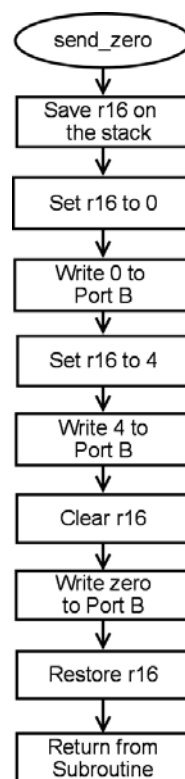

Figure B.8: Send_zero flow chart

B.2.10   Send_LE

The last subroutine used in the code enables to load the data stored in the PLL shift register to its destination PLL internal register. The subroutine pulls high the SCK pin of the microcontroller. It corresponds to the LE pin in the PLL device (see Figure 5.3). So, the PLL sends the data from the shift register to one of the three internal register on the rising edge of LE. A NOP instruction is used during the execution of the subroutine in order to be sure that the PLL chip

has enough time to load the bytes to the register. At the end of the subroutine, all the output pins are pulled to low level and the previous value of the register r16 is restored. Finally, the subroutine return from the caller subroutine *sendvalue* to go on with the rest of the data transfer.

```
send_LE: push r16
; Set SCK pin to high
ldi  r16,0x01
out  PORTB,r16
nop
; Set microcontroller's output pins to low level
ldi  r16,0x00
out  PORTB,r16
pop  r16
ret
```
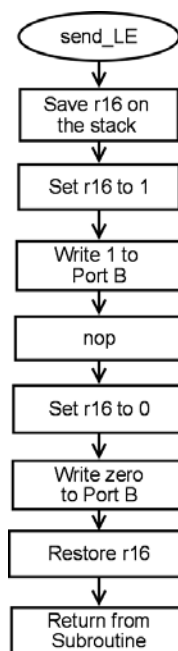

Figure B.9: Send_LE flow chart

B.3   Code script

```
;Yasmine Akhertouz Moreno and James Colli-Vignarelli
;LEG laboratoire d'electronique générale
;March 28th, 2008
;References:
; 8-bit microcontroller with 1KBytes In-System Programmable Flash

    ; 8-bit AVR Instruction Set
;%%%% INCLUDE %%%%
.include "tn13def.inc"
.include "definitions.asm"
;%%%% END INCLUDE %%%%
;%%%% RESET %%%%

reset: ; Set up address (r16) in the Stack Pointer address register
ldi r16,0x8F
out spl,r16
; Clear r16
clr r16
; Global interrupt disable
CLI
; Clear carry
CLC
; Define direction for port pins
ldi r16,0x07
out DDRB,r16
; Initialize Z_register
clr r30
; Initialize Y_register
clr r28
; Initialize r21 register
clr r21
; Initialize byte counter register
```

```
ldi r18,0x03

loadData: ; Load Latch register data
ldi  r28,$9F
ldi  r21,0x9F
st   Y,r21
ldi  r21,0x80
st   -Y,r21
ldi  r21,0x93
st   -Y,r21
; Load R-counter data
ldi  r21,0x00
st   -Y,r21
ldi  r21,0x00
st   -Y,r21
ldi  r21,0x14
st   -Y,r21
; Load N-counter data
ldi  r21,0x00
st   -Y,r21
ldi  r21,0x0D
st   -Y,r21
ldi  r21,0x25
st   -Y,r21
rjmp main
;%%% END RESET%%%


;%%% MAIN%%%

main: rcall load_PLL
end: ; Transmission end
ldi r16,0x00
out PORTB,r16
rjmp end
```

```
;%%% END MAIN%%%

;%%% LOAD PLL%%%

load_PLL: ldi  r30,$9F
ld   r20,Z
; Send Latch_register data
rcall sendvalue
ld r20,-Z
; Send R_counter data
rcall sendvalue
ld r20,-Z
; Send N_counter data
rcall sendvalue
ret

;%%% END LOAD PLL%%%

;%%% SEND VALUE %%%

sendvalue: ; Save r18 on the stack
push r18
sendnextbyte: ; Send bytes
rcall send_bits
dec  r18
cpi  r18,0x00
; if r18 = 0, send enable load LE register signal
breq loadRegisterEnable
; if  r18 !=0, load next byte to send
ld   r20,-Z
rjmp sendnextbyte
loadRegisterEnable: rcall send_LE
end_sendvalue:  ; restore r18
```

```asm
pop r18
; return from subroutine
ret
;%%%% END SEND VALUE%%%
```

```asm
;%%%% SEND_BITS %%%%
send_bits: CLC
push r17
; Initialize bits counter register
ldi r17,0x08
shift: rol r20
; If C = 1, send one
BRCS One
; If C = 0, send zero
rcall send_zero
rjmp next
One: rcall send_one
next: ; Update the value of r17
dec r17
cpi r17,0x00
; If r17 != 0 go to shift
brne shift
; If r17 = 0 restore r17 from stack
pop r17
ret
;%%%% END SEND 8 BITS %%%%
```

```asm
;%%%% SEND_ONE %%%%
send_one: push r16
; Put high the pin number 8 of the PLL
ldi r16,0x02
out PORTB,r16
; Enable the load of the bit into the PLL chip on the rising edge
ldi r16,0x06
```

```
out PORTB,r16
clr r16
out PORTB,r16
pop r16
ret
;%%% END SEND_ONE %%%

;%%% SEND_ZERO %%%%
send_zero: push r16
; Put low output pin
ldi r16,0x00
out PORTB,r16
; Enable the load of the bit into the PLL chip on the rising edge
ldi r16,0x04
out PORTB,r16
clr r16
out PORTB,r16
pop r16
;%%% END SEND_ZERO %%%

;%%% SEND_LE %%%%
send_LE: push r16
;Set SCK pin to high
ldi  r16,0x01
out  PORTB,r16
nop
; Set microcontroller's output pins to low level
ldi  r16,0x00
out  PORTB,r16
pop  r16

;%%% END SEND_LE %%%%

;%%% END %%%%
```

Chapter C

Device construction

C.1   About This Project

This appendix was written by MM. Karim Jaber, Anurag Mangla and Haisong Wang during their MICS summer internship in 2009; corrections and additions were made by the author. The goal of their project was to build and test several of the UWB transmitter and receiver presented in this work.

This Appendix describes the building blocks of the U-Lite UWB testbed, with LNA, VGA and Oscillator which constitute the receiver chain and, the Transmitter. A detailed circuit building process (soldering, assembly etc.) and the test procedure and results are explained in the following sections.

The next section gives a brief introduction of UWB. In Section C.2 we discuss about the general constraints in RF PCB design and soldering.

- **Section C.3** describes in detail about the general considerations for soldering passive and active SMD components.

- **Section C.4** gives an overview of the building blocks of the complete system detailing their use and specifications.

- **Sections C.5** to **C.9** explain about each of the building blocks in more detail by giving their schematic diagrams and the instructions for building and testing each of them.

The goal of this Appendix is to serve as a *Designer's Manual* for the UWB system which presents a step-by-step procedure for any such further work to be carried out with ease. This is

why we include it as an essential complement to this work for helping the construction of the devices.

C.2 General Constraints in RF PCB Design

RF PCBs and circuits require a more careful design and manufacturing approach than conventional designs. This is because the signals involved range from DC to GHz. Because of the low component values, high gains and impedances and of course, very high frequencies, the signal integrity and interference issues become very important. The signal integrity and interference issues could be caused due to one or more of the following factors:

- EMI (radiations beyond the board or susceptibility to radiations from outside the board)

- Reflections on a single net

- Crosstalk between two or more nets

- Power system instability during component switching

The most important design considerations for RF PCBs are the following:

1. The board should be divided into functional areas, eg. oscillator components in one part, amplifier in the other etc.

2. The decoupling capacitors are very important to isolate the power supply from the RF components.

3. Decoupling should always be done with at least two capacitors- a low value one for high frequencies and a high capacitance one for low frequency decoupling.

4. Ground is the most important feature of a RF board. The board must have as much ground as possible with vias connecting the component side to the ground plane.

5. In the RF circuits the traces act as transmission lines. Careful design considerations need to be applied to design the microstrip lines correctly. Proper thicknesses of copper and dielectric layers must be chosen. Then, the trace length should be designed correctly according to the signal wavelengths in consideration.

C.3   General Considerations About Soldering Components on Printed Circuit Boards (PCB)

In this section we discuss the basic guidelines on soldering and desoldering SMD components on PCBs. In general, the soldering procedure for the passive and active components remains the same. However, as will be discussed, some additional guidelines must be followed for the active components. Some key points to bear in mind that we learnt from our experience while soldering/desoldering have also been listed.

C.3.1   Soldering Surface Mounted Devices (SMD)

Material List

- **Soldering flux** : liquid used to protect the PCB from oxidation when soldering.

- **Roll of tin** : thin wire of 60% tin and 40% lead used to make the joint between the component and the PCB by heating it.

- **Iron tip and its support** : the purpose of the iron tip is to melt the soldering tin and guide it by heating the places where the solder must go. It's accompanied by a support for resting it when not in use and for cleaning it with a sponge from any impurity.

- **Tip activator** : substance used to tin the iron tip.

- **Clamper**: tool for clamping components and place them on the PCB.

- **Brush and alcohol**: for cleaning the residual flux from the clamper, PCB etc.

- **Microscope** : Indispensable for working with small elements.

- **Cutter**: Sharp tool for cutting dongle connectors.

- **Vice**: Mechanical tool for holding a PCB in a convenient way for soldering or desoldering. It is also used for holding dongle connector when preparing it.

- **Wick** : Twisted copper braid that removes soldering when heated

- **Ultrasonic bath** : removes residual flux and other impurities from completed PCBs.

- **Abrasive tool** : Grinder to shorten the pins of a dongle connexion.

Passive Components

- **Step 1:** Turn on microscope and soldering iron. Put some water in the sponge, as shown in Figure C.1.
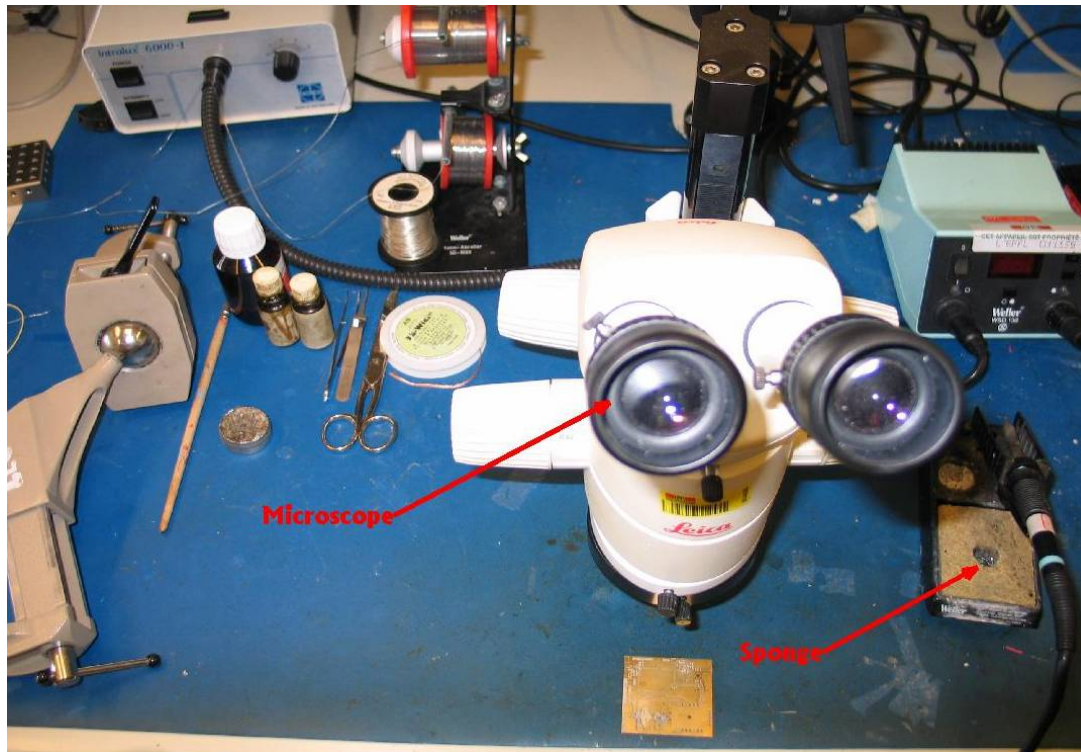
Figure C.1: Operating Station

- **Step 2:** Shine the iron tip, as shown in Figures C.2 and C.3.

(a) put the tip in activator   (b) clean it using sponge

Figure C.2: Shining the Iron Tip

(a) before shining   (b) after shining

Figure C.3: Before and after Shining

- **Step 3:** Put a little soldering flux on pad, as shown in Figure C.4.
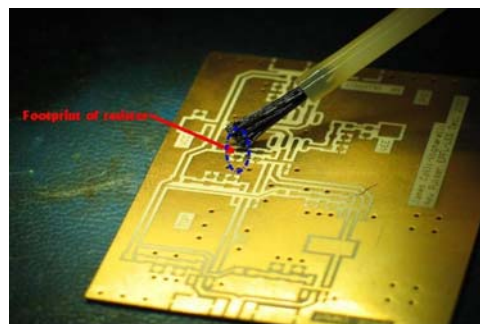
Figure C.4: Put Sodering Flux On Pad

- **Step 4:** Put a little solder on the pad, on which soldering flux is just added, as shown in Figure C.5. The outcome of this step is also given in Figure C.5.

(a) adding little solder on pad   (b) outcome
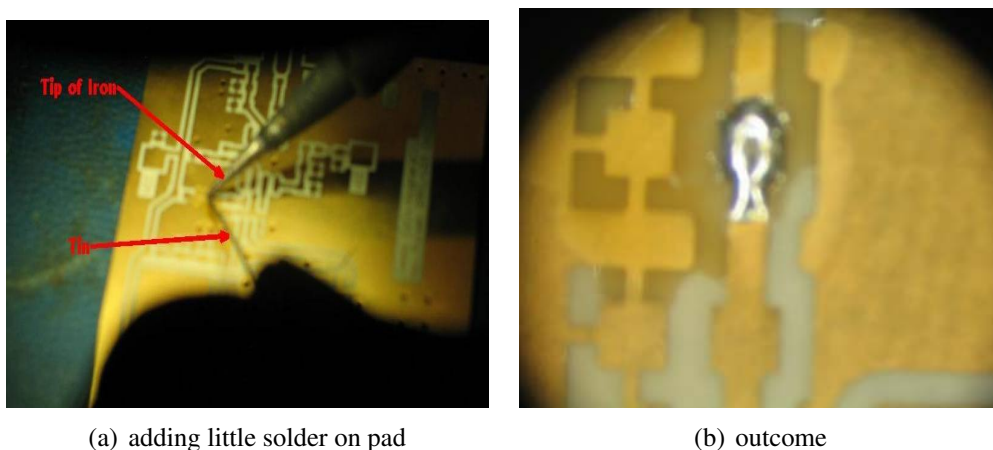
Figure C.5: Comparison Before and After Shining

- **Step 5:** Put the component on the PCB and align it with the pad. Fix one pad by heating the solder while controlling the component using clamper, as shown in Figure C.6. Check whether the component is flat on PCB or not.
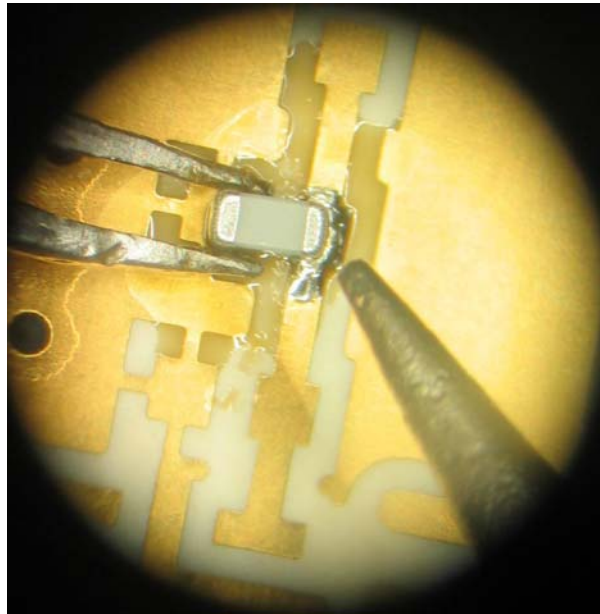
Figure C.6: Fix the Component

- **Step 6:** Put some soldering flux and solder the other pad, as shown in Figure C.7.
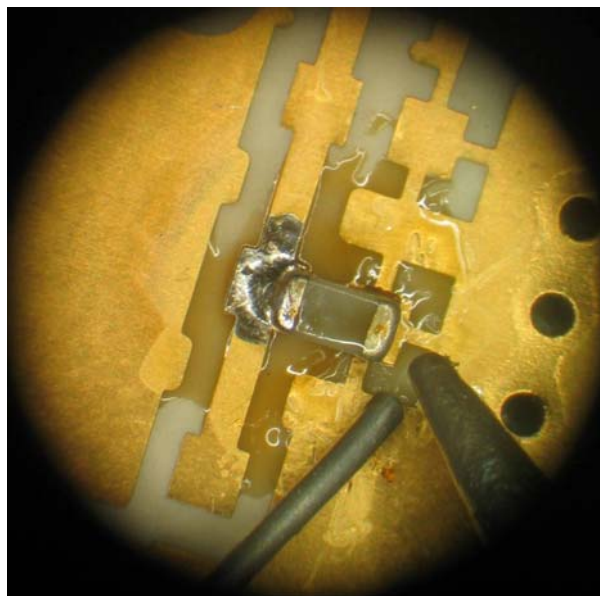
Figure C.7: Soldering the Other Pad of Component

- **Step 7:** Put more solder on the previous pad and finish the soldering, as shown in Figure C.8.
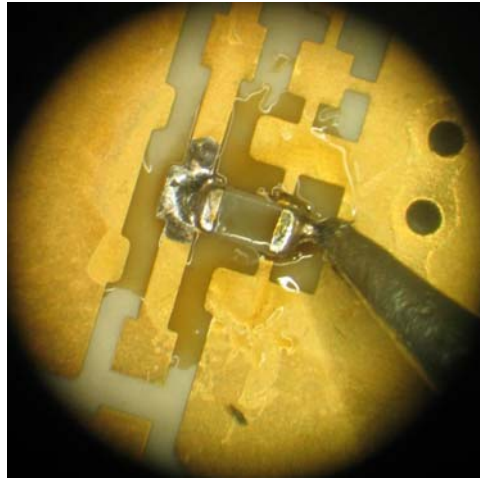
Figure C.8: Finishing Soldering

- **Step 8:** Check the component to make sure it's flat on PCB, as shown in Figure C.9.
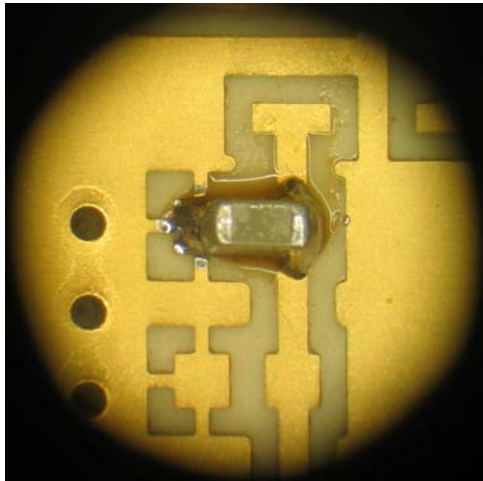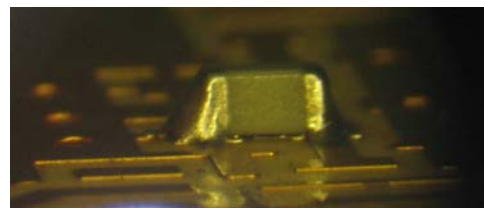
(a) top view   (b) side view

Figure C.9: Check the Soldering

Active Components

The basic procedure of soldering active components is similar to that of passive ones. Here, one example of soldering eight-pins SMDs is given to illustrate the difference.

- Compared to two-pin passive component mentioned before, special attention should be paid to the sequence of soldering each pin. In order to fix the components, the diagonal pins should be soldered first. As it was done when soldering passive components, put some soldering flux on pads first. The illustration is shown in Figure C.10.
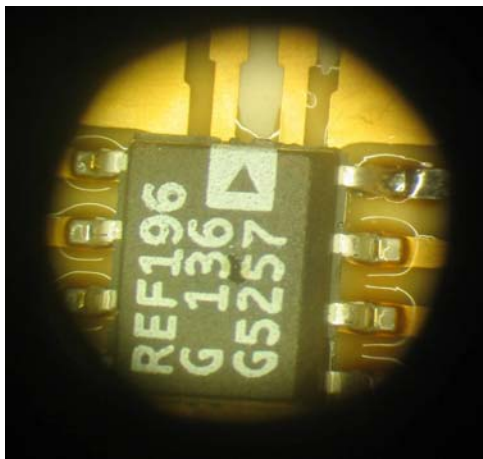
(a) fixing one pin
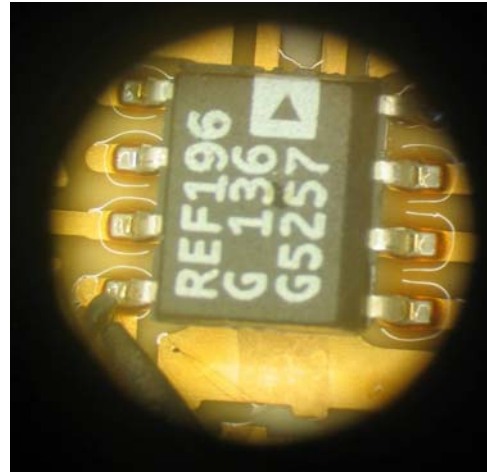
(b) fixing the diagonally opposite pin

Figure C.10: Fixing Diagonally Opposite Pins

- Solder the left pins in arbitrary sequence. The finished work is shown in Figure C.11.
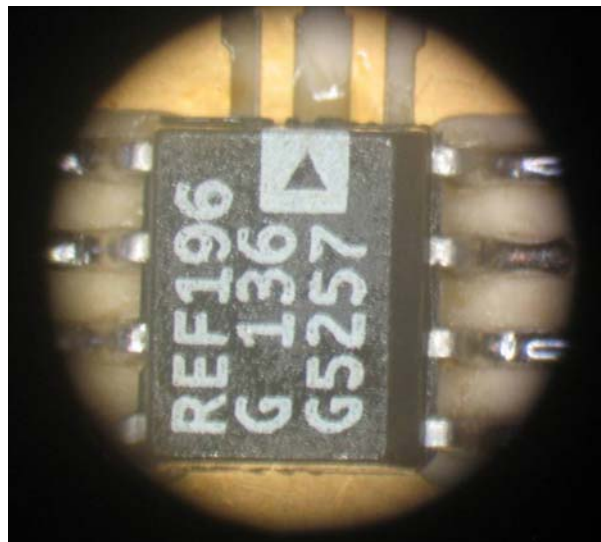
Figure C.11: Finished Soldering

Preparing and soldering a dongle connection   Dongle connections are used to connect for example a PCB to a computer to program a microcontroller. However, such connexions need to be prepared before getting soldered because often one of the pins will be connected through a via to the ground and thus need to be longer. An example of dongle connexion's pad is shown in Figure C.12. Here are the steps to follow to succeed in this task:
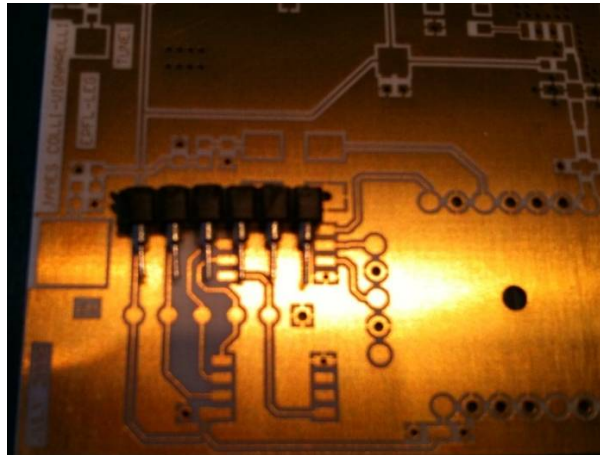
Figure C.12: Dongle Connection Pads

- **Step 1:** Cut the exact number of pins (here six) that your connexion require to fit in the PCB with the cutter.

- **Step 2:** Hold the dongle connexion with the vice and make sure not to damage it doing so. The pin should be easily accessible as in Figure C.13

Figure C.13: Placing the Dongle Connector In the Vice

- **Step 3:** Using the abrasive tool, shorten all the pins for around 1mm (depending on the thickness of the PCB) except the ground pin. It should look as suggested in Figure C.14

(a) Shortening the pins

(b) Final result (note the longest pin on the top)
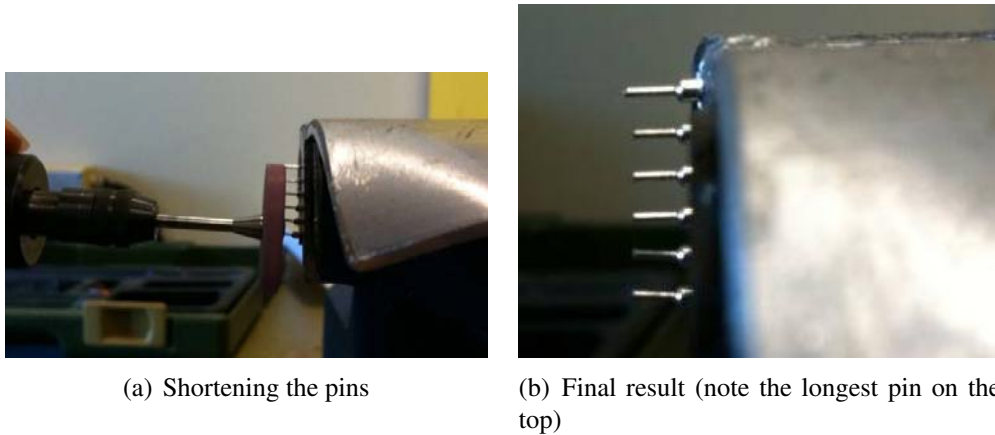
Figure C.14: Finishing the Dongle Connector

- **Step 4:** After having checked that the dongle connector fits on the belonging pads, put a little amount of soldering on the pad that is on the opposite of the ground pad

- **Step 5:** Put some flux on all the pads where the connector should go. Then, solder the first pad of the dongle connector being really cautious that each pin is in the middle of its corresponding pad and that the connector is flat and vertical. Check that the ground pin doesn't emerge on the other side of the PCB as well (refer to Section C.3.3 for more information on this point)

- **Step 6:** Solder the pin that is next to the ground pin so that the connector is stable.

- **Step 7:** Finally, using enough flux, solder all the remaining pins and finish with the ground connection. Figure C.15 shows the final result.

C.3.2   Desoldering

- **Step 1:** Put some soldering flux on copper wick, as shown in Figure C.16.

  Step 2: Put the copper wick on the solder, and heat the copper to make solder melt. The solder will be attached to the copper wick and be removed, as shown in Figure C.17.

  Step 3: For active component, first remove the solder on each pad shown in Figure C.18. And then heat each pin using iron while detaching the pin from the pad at the same time using clamper as shown in Figure C.19.
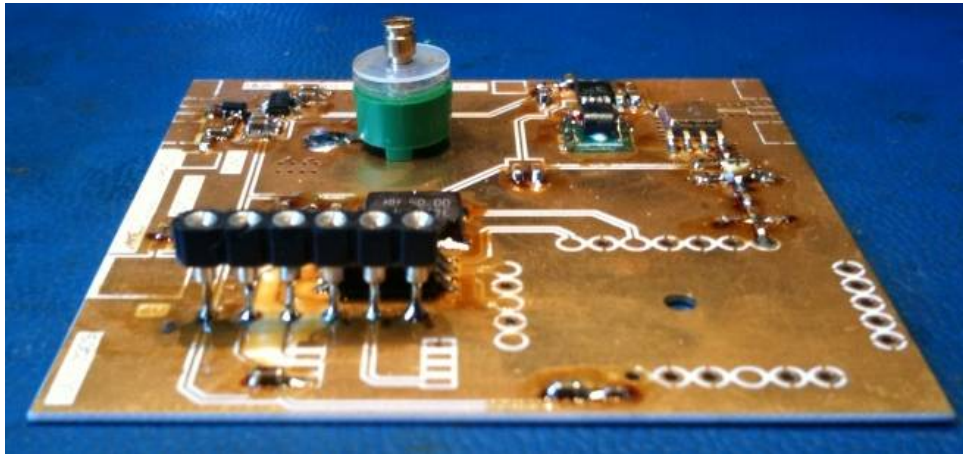
Figure C.15: Final Outcome

Figure C.16: Put Soldering Flux On Copper Wick

Step 4: Clean the residual solder on pad using copper wick, as shown in Figure C.20.
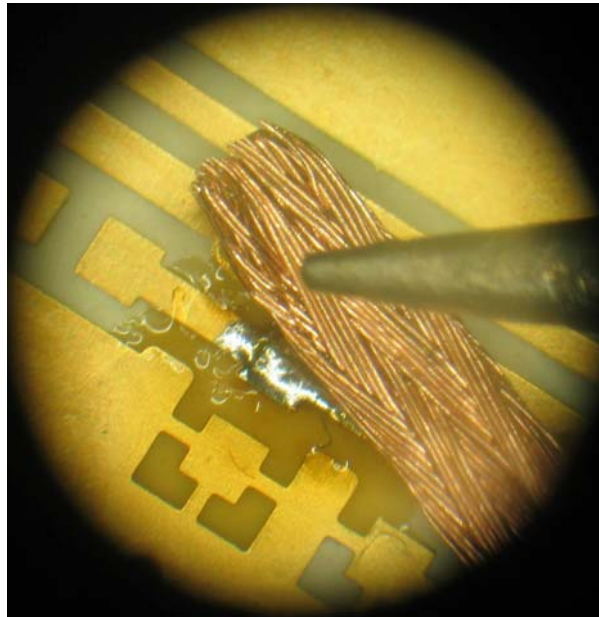
Figure C.17: Remove the Solder On Pad
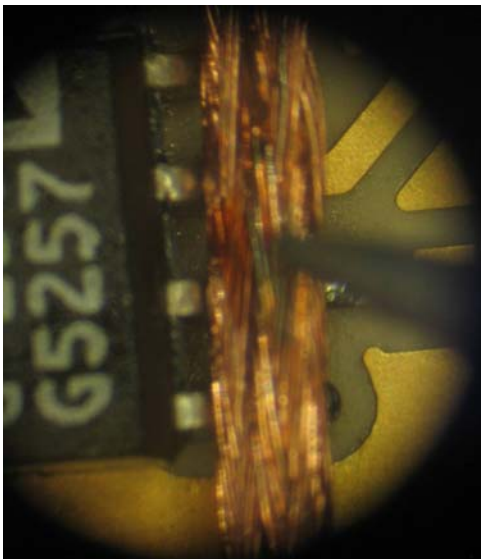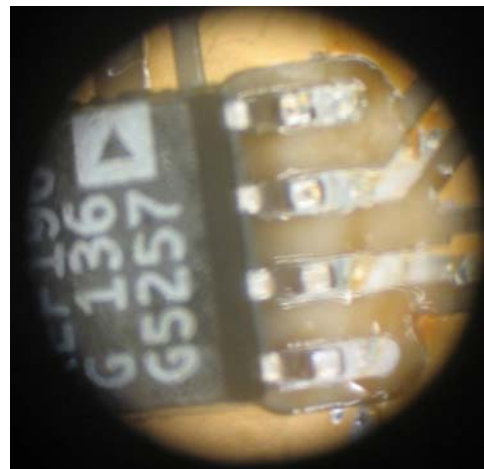
(a) put wick on solder   (b) heat the wick and remove the solder

Figure C.18: Removing Solder On Pins

C.3.3   Key points to bear in mind

1. Always think forward when soldering: think of the whole PCB, and make an effective plan of soldering each component. Generally, we could start from small components and then to the relatively big ones. Also bearing in mind that soldering of one component
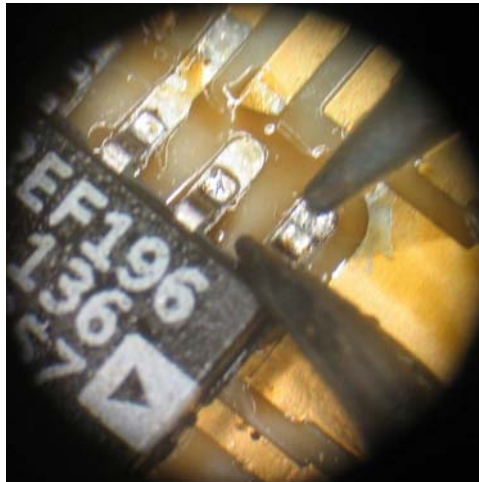
Figure C.19: Detach Using Clamper
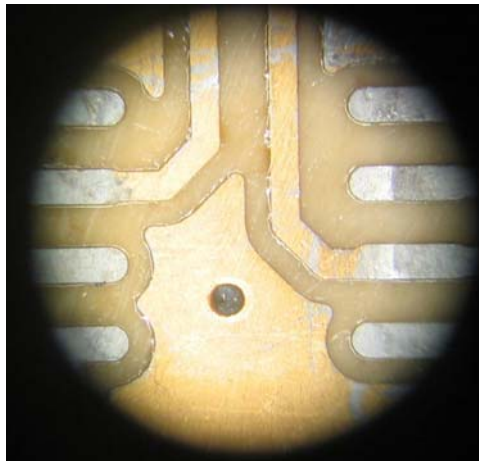
Figure C.20: Pads After Cleaning

should not prevent soldering of nearby ones.

2. Since some active components are susceptible to ESD, the soldering should be done on ESD protection station.

3. When soldering the passive component, it is advisable to use highest temperature for tip of iron, e.g. $450\,^\circ\text{C}$, and solder as fast as possible to avoid the damage of component due to excess heating. Usually the total soldering time should be shorter than 10 seconds.

4. While for active component, make sure the temperature of tip of iron is not higher than recommended in the datasheet. Also, try to finish the soldering as fast as possible to avoid damage due to excess heating. Specific to active component, since usually there are

more than two pins for active component, it is advisable to leave enough time between soldering of each pin to make the heating on die release to avoid the accumulation of heating.

5. Solder the non-ground pad first, since soldering ground pad needs more heating and a little more difficult than non-ground pad.

6. Put soldering flux on pad before soldering to avoid oxidation of metal, and also make the solder easier to spread.

7. When removing the component, especially using hot iron, the component usually is damaged. It is suggested to use a new component in order to minimize the uncertainty in the circuit.

8. When one pin of dongle has been fixed by solder, don't try to adjust it without heating, since it may damage the pad.

9. Use the soft grinding disk for grander since the dongle is hard, and vice versa.

10. Be sure to wear protecting glasses when grinding the dongle.

11. For the components with more than two pins, if there is already one pad with some tin on it due to soldering of nearby components, use that pad as the first pad to solder.

C.4   System Building Blocks

In this section, the different blocks that will be built are presented. The main ones are the low noise amplifier (LNA), the voltage-controlled gain amplifier (VGA), the oscillator and the Ultra Wideband (UWB) transmitter. Figure C.21 shows the schematic block diagram of the system. The principle is the following: a bit stream is generated by an algorithm in the FPGA board which feeds the transmitter. Inside, the stream is passed through an impulse generator which shortens the pulses width from 6μs to 2 ns. It is then mixed with an oscillator working at 4.25 GHz to create the ultra wideband pulses that will be transmitted. From the receiver side, two LNAs regenerates the received signal with a variable gain. The next block is the digital to analog conversion, it samples at 2 Gsample/s, thus down conversion of frequency is needed to respect Shannon's theorem. This is done by using an oscillator. To make sure that a good signal without beat is obtained in time domain a complex demodulation, made with an

I/Q mixer, is performed. Indeed, oscillators can have imprecisions that will impact on the time domain signal if this technique isn't used.
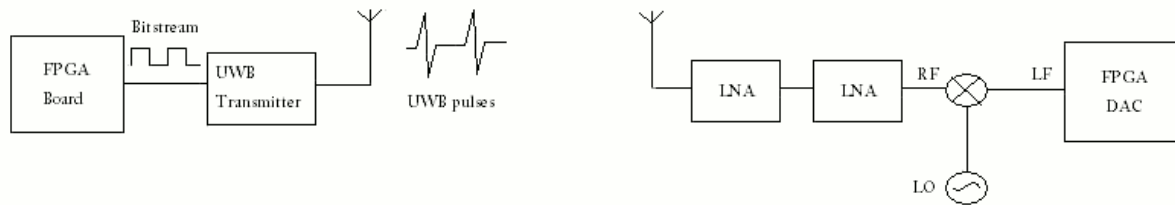

Figure C.21: Block Scheme of the UWB Transceiver System

After this introduction on the general functioning of this ultra wide-band transmitter, more details on the specific parts are presented thereafter.

1. **Low Noise Amplifier (LNA)**: The LNAs used in this work are actually composed of three cascaded blocks each as presented in Figure C.22 : the MOS LNA with a gain of 10 dB is connected to a bandpass filter, that rejects undesired harmonics created by the first stage and feeds a voltage controlled gain amplifier thanks to which the gain is controllable. At maximum we can have 30 dB of gain for each amplifier. Using such topology allows not only to control the gain but also to guarantee the impedance matching between the blocks (this point will be clarified in the next section). Finally, the gain at the output of the two LNAs is 60 dB at max. Moreover, they will be enclosed in a shielding box such that no interferences couples with the signal and thus avoiding oscillations due to the high gain of this amplifier array.
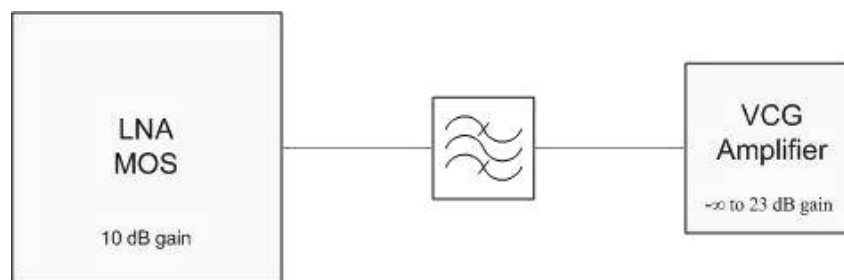
Figure C.22: Block Diagram of the LNA and its Voltage Gain Control

2. **Oscillator (Osc)**: The aim of this oscillator is to down convert the frequency of the received signal before sending it to the ADC of the FPGA board. It is composed mainly by a programmable PLL (Phase Locked Loop) synthesizer and a quartz oscillator. Indeed,

the PLL provides a high quality signal using the quartz oscillator as reference frequency. There are many subtleties in the design of this circuit, the details on the use of each component will be presented in Section C.7.

3. **Ultra Wide Band Transmitter (UWBT)**: The transmitter is composed of three parts : one is the same oscillator as before but this time for up-conversion in frequency, an impulse generator that process the bit stream received from the FPGA and a mixing part to multiply the generated pulses with the oscillator signal and in the end obtain the wanted UWB pulses. The antenna receives the pulses to transmit at quiet a high power (10 - 15 dBm).

C.5   Low Noise Amplifier (LNA)

This section discusses about the specifics of constructing the LNA. After a brief overview of the schematic, the PCB and the components, we will discuss the best practices in soldering the components on the PCB, assembling the mechanical parts like the shielding box and finally testing the completed assembly. These best practices have been drawn out of our experience with the construction of the LNA and are expected to serve as guidelines for anyone hoping take up the same or a similar project in the future.

C.5.1   Schematic and PCB Layout

Figure C.23 and C.24 show the schematic and the PCB layout respectively, of the LNA.

The LNA is built around an HEMT ATF35143. Figure C.25 shows the pinout of the IC package. The bottom-left "Source" pin distinguishes itself from the others by being wider than the others. This is connected to the ground pad (labeled "1") for Q1 on the PCB. The other components are passives with R_1, R_2, R_3, R_4, R_5, C_1, C_2, C_3, C_4, C_5, L_3 and L_4 having 0402 footprints.

C.5.2   Soldering Guidelines

In this section we present the guidelines, best practices and rules-of-the-thumb for soldering the components on the LNA PCB.
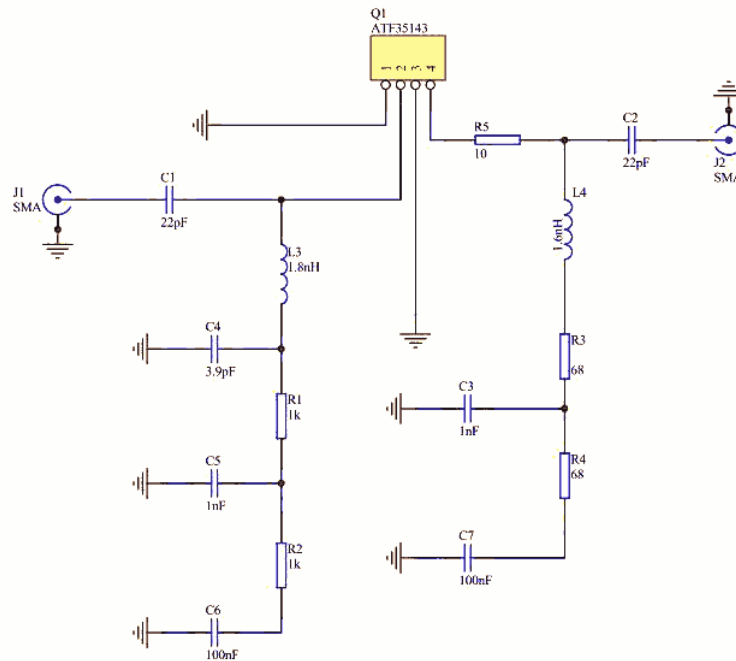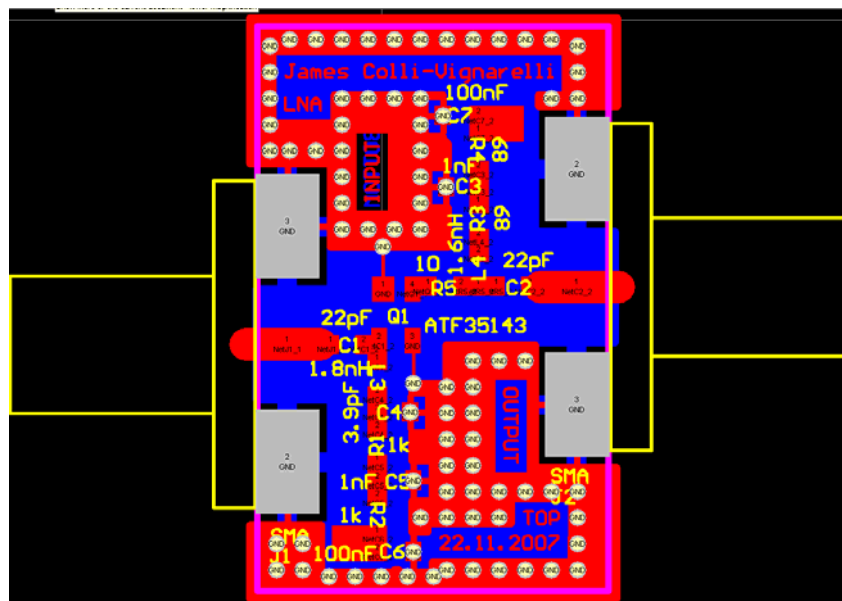
Figure C.23: Schematic of the LNA

Figure C.24: LNA PCB Layout

The LNA PCB is a very small one with only 15 components and is quite easy to solder. A look at the PCB layout reveals that there are two branches with a ladder topology of the passive
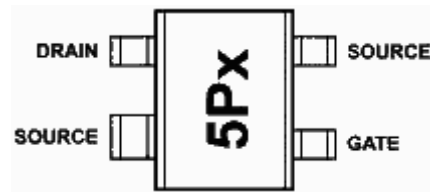
Figure C.25: Pinout of ATF35143 HEMT

components with the active pHEMT at the center. As a general rule-of-the-thumb the active components should be soldered last. Following is the recommended sequence for soldering the components:

1. C_6: Here, there is compromise between soldering the broad pad on the left or the ground pad first since both require longer time to be heated. Still it is better to start with the left pad and not the ground pad because the ground pad has a via and will in dissipate away much more heat.

2. R_2: The top pad is the obvious first choice for the first solder but the bottom pad could be used if there is already enough solder on this left from the soldering of C_6.

3. R_1

4. C_5: It could be easily fixed on the left pad because of the tin that would already be there from the soldering of R_1 and R_2.

5. L_3 and C_4

6. C_1: A little care must be taken in soldering the right pad of C_1 which it shares with Q_1 since solder tin might overflow onto pad 2 of Q_1. This may make resting Q_1 on the pad difficult while soldering.

7. Solder C_7, C_3, R_4, L_4, R_3, C_2 and R_5 in order following the same guidelines as listed above. Take care while soldering left pad of R5 to avoid too much solder on pad 4 of Q_1.

8. Finally, solder Q_1 taking care to align the pin correctly and following the guidelines for soldering active components already discussed in a previous section. The finished circuit is shown in Figure C.26
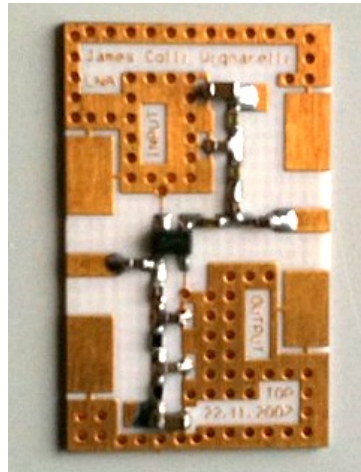
Figure C.26: Finished LNA PCB

C.6   Variable Gain Amplifier (VGA)

This section discusses about the construction of the VGA including the best practices in soldering the components on the PCB, assembling the mechanical parts like the shielding box and testing the completed assembly.

C.6.1   Schematic and PCB Layout

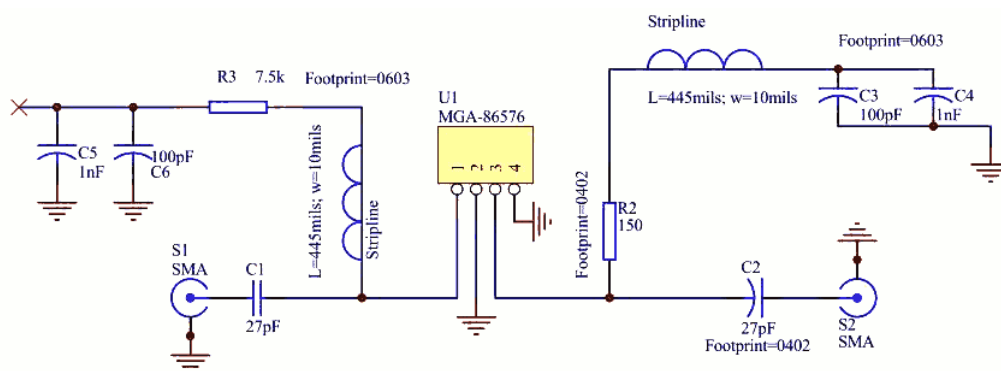Figure C.27 and C.28 show the schematic and the PCB layout respectively, of the VGA.
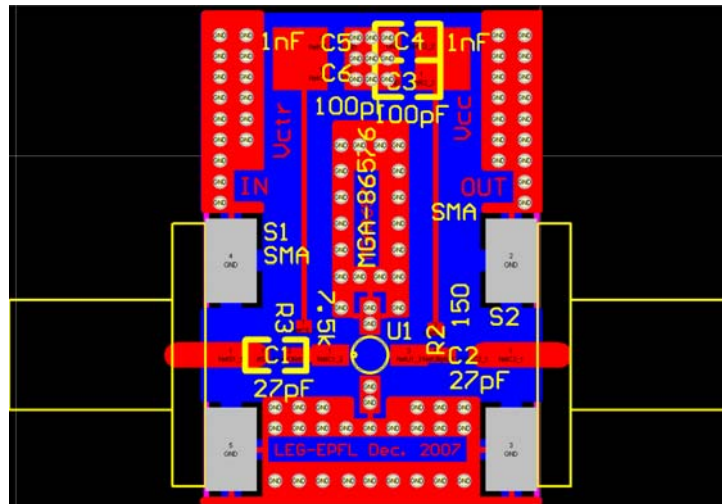

Figure C.27: Schematic of the VGA

Figure C.28: VGA PCB Layout

The VGA is built around the amplifier MGA-86576. Figure C.25 shows the pinout of the IC package. The left pin *RF-IN* is the distinguishing pin as it has a wedged end. The ground pins are broader than the others. Apart from the amplifier, there are 6 capacitors and 2 resistors. In addition, there are two striplines which are easily distinguishable on the PCB layout.
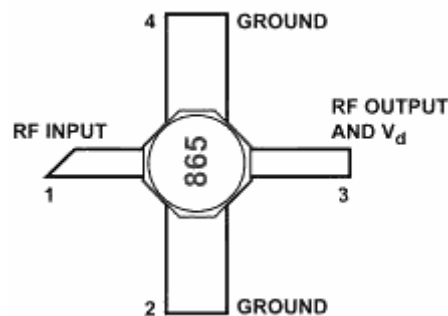
Figure C.29: Pinout of MGA-86576

C.6.2   Soldering Guidelines

In this section we present the guidelines, best practices and rules-of-the-thumb for soldering the components on the VGA PCB.

The VGA PCB is easiest one to solder with less than 10 components to be soldered which are arranged in a symmetric layout. As a general rule-of-the-thumb the active components should be soldered last. Following is the recommended sequence for soldering the components:

1. C_4, C_5, C_3, C_6: These being pairs of capacitors with same values. Moreover, these are located at the top end of the PCB and isolated from the rest of the components.

2. C_1 and C_2, R_2 and R_3: These components have 0402 footprint and have no constraints on soldering them in place.

3. U_1 (MGA-86576): The IC should be correctly oriented noting that the input pin is to the left on the PCB. The best way to solder the IC is to tin the left and the right pads (non-ground). Then place the IC and apply flux. While holding the IC in place with a pair of tweezers, apply heat on the right leg with the soldering iron enough to melt the tin below and fix the IC in place. Do the same for the right leg after ensuring that the IC legs are well placed on the pads. Then add more solder to both the pads to cover the legs and ensure a good contact. Finally, finish off by soldering the ground pins. The finished circuit is shown in Figure C.30
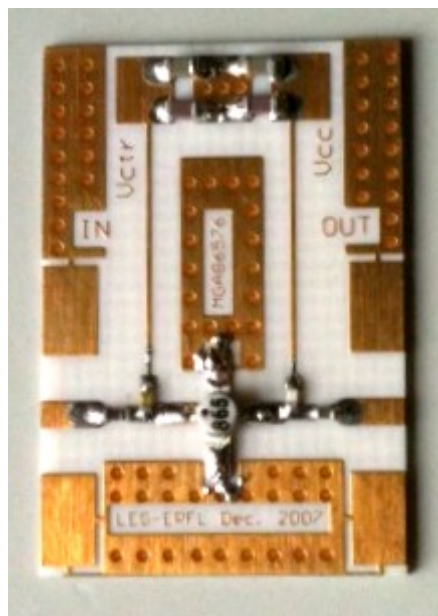
Figure C.30: Finished VGA PCB

C.7 Oscillator

In this section, we present the procedure for soldering the oscillator circuit. Previous sections considerations must be kept in mind while going through this part. The schematics are presented in Figures C.31 and C.32. It is composed of a quartz oscillator (U_3), a 4-switch IC (U_2), a microcontroller (U_1), a PLL (U_4), a dongle connector (J_1) and an amplifier (U_5). Concerning the passives, the resistor array R_2 to R_5 and the capacitors C_6 and C_9 have 0402 footprints; the remaining passives have all 0603 footprints.

- **Step 1:** Begin by soldering the six passive elements that are near the power supply in the following order : C_{14}, R_8, C_{15}, C_2, R_1, C_3. Then solder the decoupling capacitors C_7 and C_8. Finish this step with C_1, C_4 and C_5.

- **Step 2:** Now the resistor array R_2 to R_5 are to be soldered in a clockwise order starting by R5 so that the common pad of the four resistors is the most accessible. Moreover, as this pad is shared between the four resistors, one should take care not to put to much soldering on it as each time a resistor is added, soldering is added as well. If necessary, do some adjustments to this center pad so that the resistor array is well soldered. Solder capacitor C_6 before proceeding.

- **Step 3:** For this step, make sure that you are working in a static free place and that you are always in contact with the ground while handling components. Solder the MGA-86576 by starting with pin 1, there is a dot on top of the IC indicating the first pin (moreover its shape is different than the other pins). The orientation of this IC is such that its input (pin 1) is just after C_6, therefore, one could use C_6 solder to fix the MGA. Solder then the opposite pin and finish by the two grounded side pins. R_6 and C_9 are to be soldered after the MGA, otherwise this IC soldering will be over-constrained.

- **Step 4:** Now solder the quartz oscillator (U_3) following this procedure : as the IC has no "legs" but only bottom connexions, thus one should put some solder directly on the PCB corresponding pads taking care to have flat soldering. The orientation should follow the schematic noting that pin 1 is indicated by a little circle on the IC. After placing the component correctly, melt the solder pad by pad and then add as much soldering as needed to completely contact the oscillator with its pads. Using extra flux is very helpful here.
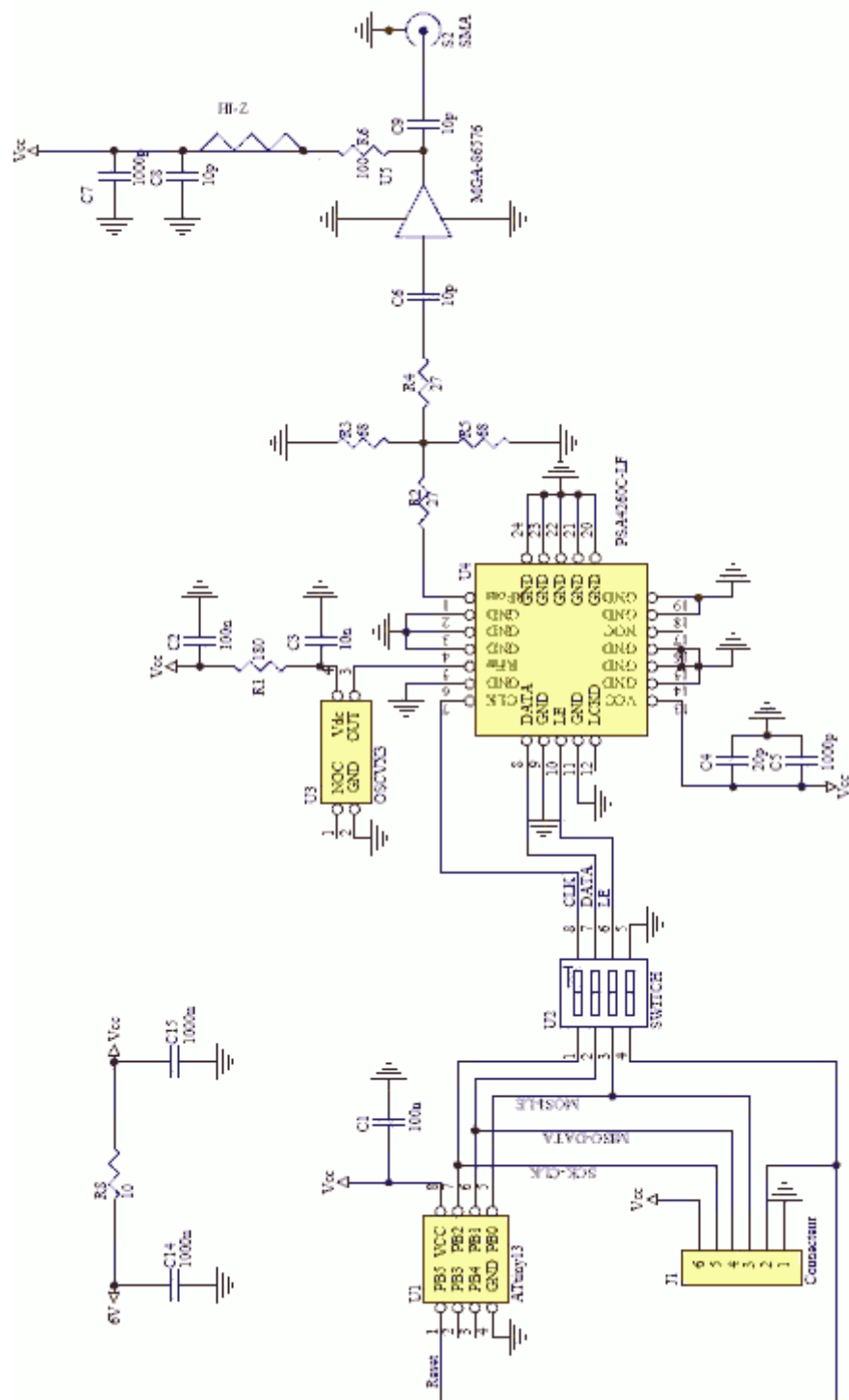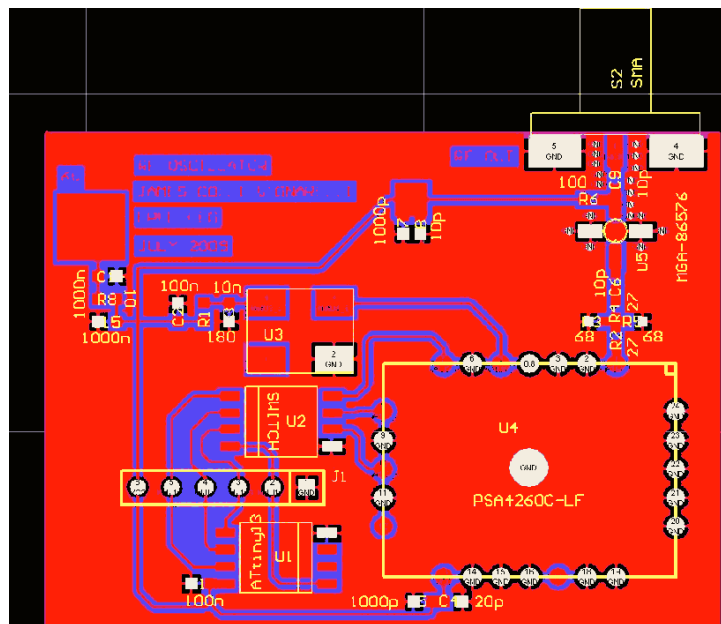
Figure C.31: Oscillator's Schematic

Figure C.32: Oscillator's PCB

- **Step 5:** In order not to be constrained, solder the remaining ICs in this order : the switches (U_2) first, then the dongle connector, the microcontroller and finally the PLL. PLL soldering will be detailed in the next step but for the rest, one should follow the instructions of Section C.3.1. Note that for the microcontroller (U_1) one should start by soldering pin 8 as there is already solder there because of C_1. The orientation when looking to Figure C.32 indicates that pin 1 of the switch (U_2) should be top left; pin 1 of the microcontroller (U_1) should be bottom right. Soldering in this order avoid to be too constrained and let one operate with ease.

- **Step 6:** The first step to solder the PLL is to place an align it. To do so, take advantage of the remaining solder on R2 of the capacitor array for soldering pad 1 of the PLL and put also some solder on pad 12, a non-signal pad that is almost opposite to pad 1. Consequently, soldering these two pads will make the PLL stable for the next operations. Make sure the PLL is correctly aligned: looking at the back of the PCB, one can see directly through the ground pads if the PLL is well aligned or not. Then, solder the non-ground pads and pay attention to leave enough cooling time between each pad. Finish by soldering the ground pads knowing that it requires a lot of heat, thus wait long enough between each pads and solder pads that are far from each other as much as possible so that the heat waves are well dissipated. To be sure not to damage the chip, one can put a

drop of water on top of the shielding of the PLL: the drop should not boil. Figure C.33 shows the final result.
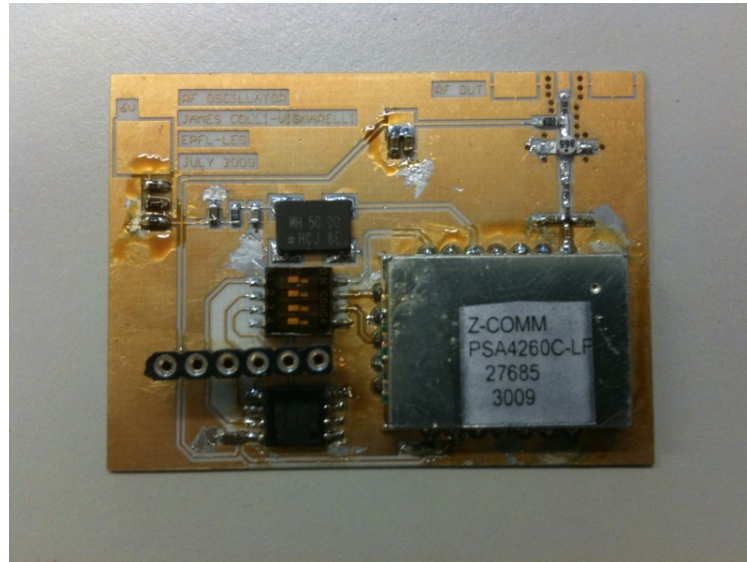

Figure C.33: Completed Oscillator Circuit and Assembly

C.8   Oscillator construction

In this section, the practical realization of the PLL is explained, especially the exact steps to follow for a good soldering of the circuit components. Because of the frequency restriction, the PCB is gold plated with electro-chemical deposition to reduce as much as possible the parasitic capacitances. This PCB was made by the EPFL circuit workshop due to its difficulty. Moreover, the workshop also drilled the PCB to make vias. The PCB is shown in Figure C.34

Soldering the SMA connector is the first device to solder, followed by the passive components (resistances, capacitances, the switch and the microcontroller's connector). Then, the microcontroller, the oscillator, the PLL chip and finally the MMIC are soldered. Following this order, the most sensitive components are not exposed too much long to the heat, so its electrical characteristics are preserved.

To solder the SMA connector, it is first fix to the PCB by soldering the central pin of the connector on the output track of the PCB. Afterwards, the whole is maintained in a vice to melt down easier the tin on both the connector and the PCB. Figure C.35 gives a visual description of these steps.
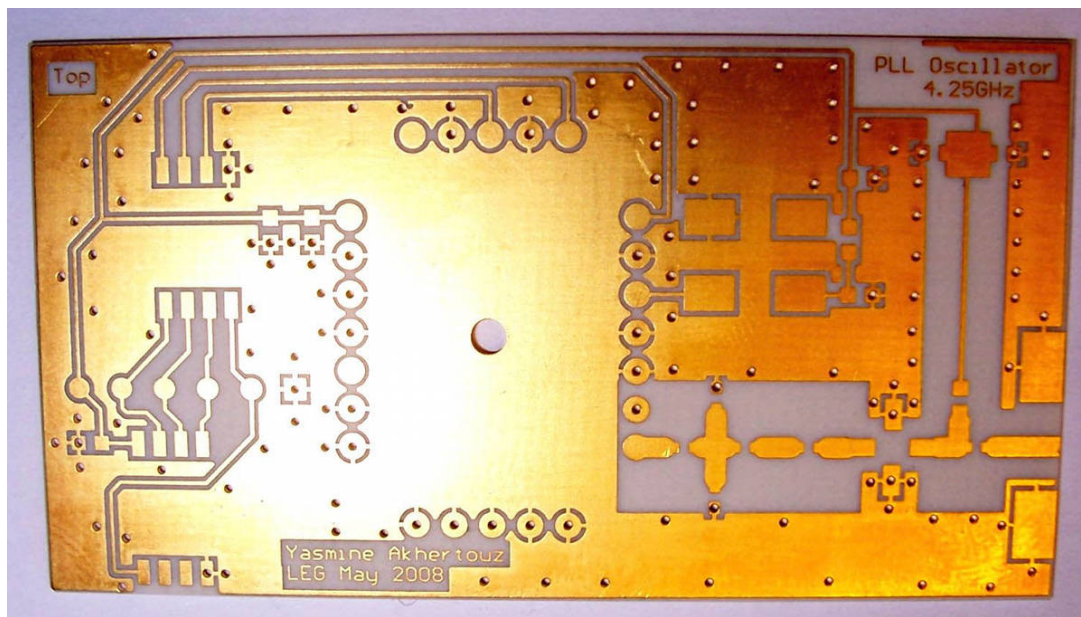
Figure C.34: Oscillator's PCB
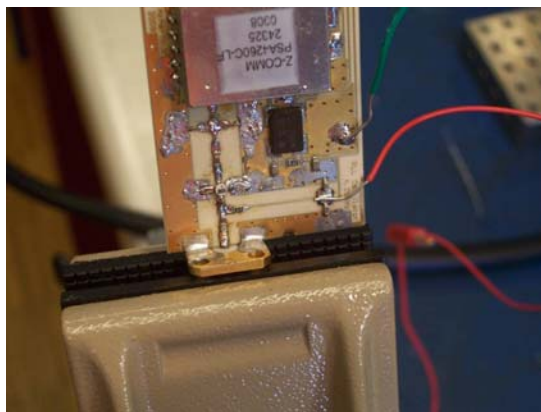
(a) Large view of how to solder the SMA connector

(b) Close view of the SMA once soldered on the PCB

Figure C.35: The soldering process of a SMA connector.

Then, the microcontroller's connector shown in Figure C.15 is soldered. This component is quite hard to solder on the PCB, because it is not an SMD component, and it cannot be soldered through holes to avoid the short circuit with the metallic shield. This practical limitation involves filing the connector's pins to transform them into a flat surface. It is important to say that the filling is done to all connector's pin but the pin 6, which corresponds to the ground, as it is shown in the schematic circuit in Figure C.12. Actually, this pin will be pushed into the ground via, but not much to go through the PCB. Thus, this via works as a support to stabilize the connector, and giving enough time to solder this pin 6 first, before going on with the rest of

them. The result of these steps is shown on Figure C.36
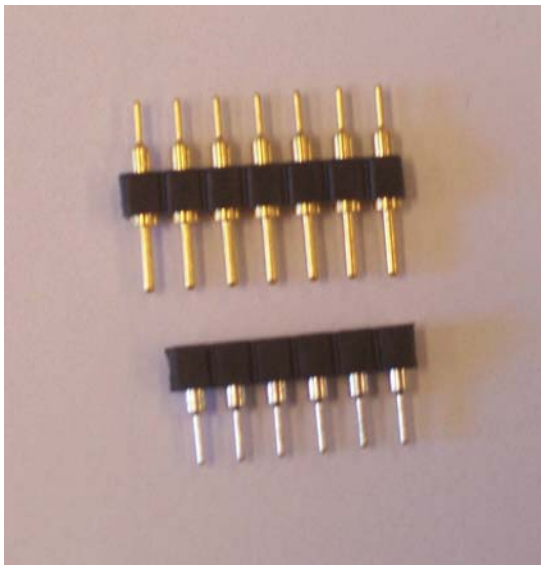
(a) Final configuration of the microcontroller's connector

(b) Microcontroller's connector before the filling

Figure C.36: The milling process of the in line connector.

The switch and the passive components are soldered by putting first a drop of tin on the track. Next, the component is maintained on it with a thin tool, and the tin is touched with the tip of the iron to melt it, so the pin and the pad are connected. It is important to pay attention to the fact that the component lies horizontally on the board, to avoid any possible short circuit.

The microcontroller ATtiny13 is also soldered in the same way as the SMD components, but instead of soldering each neighbour pad one after the other, it is alternated. Some seconds must be waited before each soldering. Therefore, heating the component is avoided, and so changing its electrical characteristics. Then, the code is loaded into ATtiny13 using PonyProg program and a dongle (see Figure C.38 and [43]). Afterwards, the power supply is switched off and the serial port is removed off from the microcontroller's connector. Then, the feed is turned on, and the output of the microcontroller is checked whether it generates the right bits.

The microcontroller's connector is not a serial port, but a series of pins through which the code is going to be loaded into the microcontroller. However, all the cables used for programming a microcontroller have serial port in both edge sides. Thus, a pin-serial port cable is built (see Figure C.39) to be able to load the code into the microcontroller. When making the cable, be extremely careful to align each pin with its exactly serial port wire, otherwise, the microcontroller will not be programmed. The layout of the serial port of the dongle is displayed in
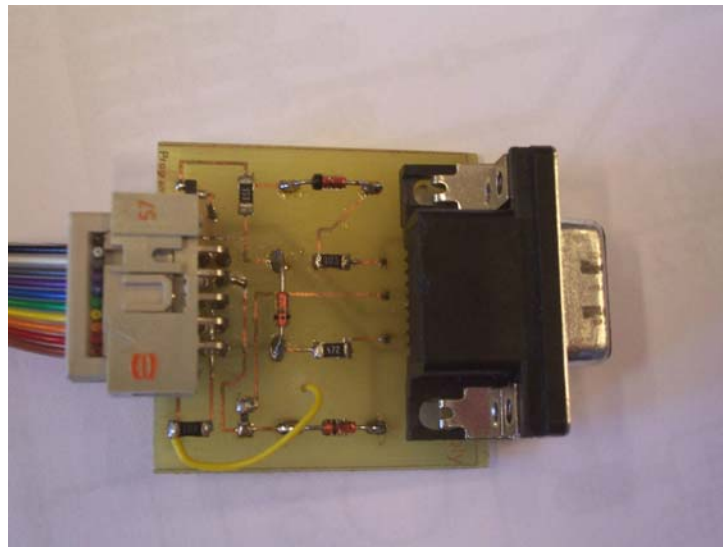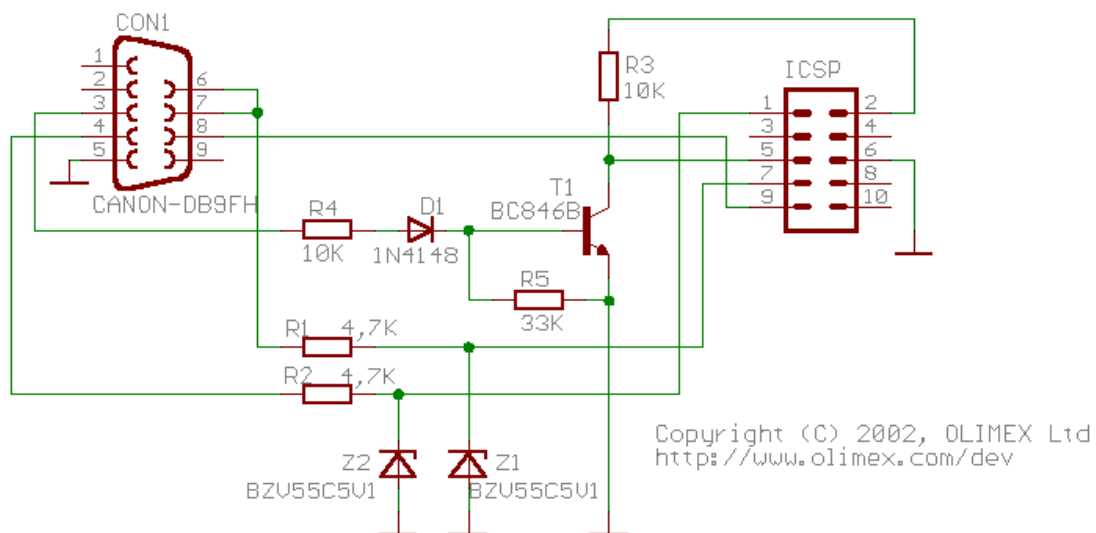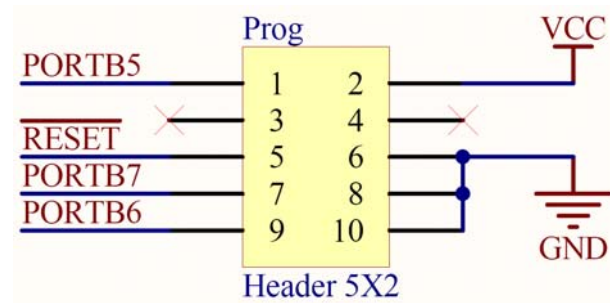
Figure C.37: The dongle

Figure C.38: The schematic of the dongle

Figure C.39.

To be sure that the code is well loaded in the microcontroller, and so the right bits are generated, logic analyser is used to check whether each microcontroller's output pin gives the right data stream. Figures C.40 and C.41 show that we obtain exactly the same data stream defined for each PLL internal register (Appendix B), and that in the rise clock, the data is already set to the right value.

(a) Pin-serial port cable

(b) Serial port configuration

Figure C.39: The serial cable used to progrmm the microcontroller with the dongle.
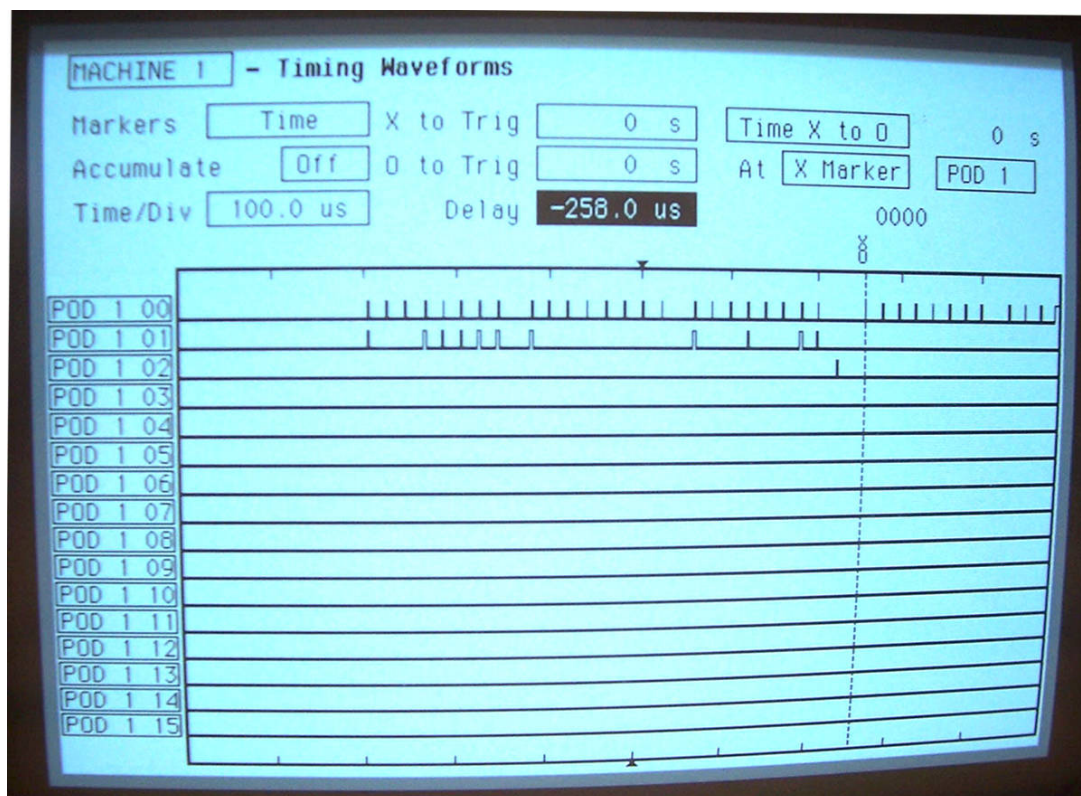
Figure C.40: The signals measured at the output of the microcontroller

The measured signals are arranged in the following way:

- POD 1 00: Signal that load the data in the shift register.

- POD 1 01: The data stream.
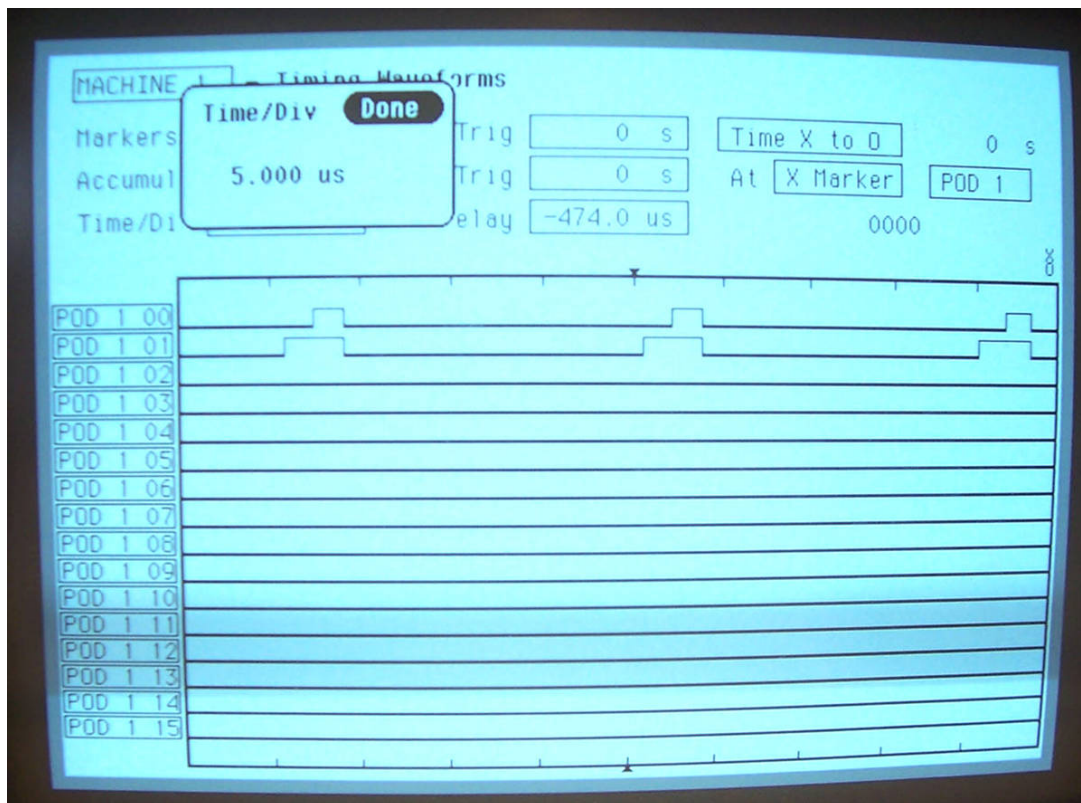
Figure C.41: The value of the data is already set when the clock is raised

- POD 1 02: LE signal.

To do this measurement, the main part of the code must be written as:

main: rcall load_PLL

end: ; Transmission end

ldi r16,0x00

out PORTB,r16

WAIT_MS 10

rjmp main

By this way, the loop gives to the logic analyser time to measure the signals. Next, the crystal oscillator device is soldered in the same way as it is explained for passive component, and then the oscilloscope is used to verify whether the reference frequency is correct (see Figure C.42).

The next step is soldering the PLL. This is an extremely sensitive component, it is advised to be very careful when soldering it to not burn it. Following the same procedure as the micro-
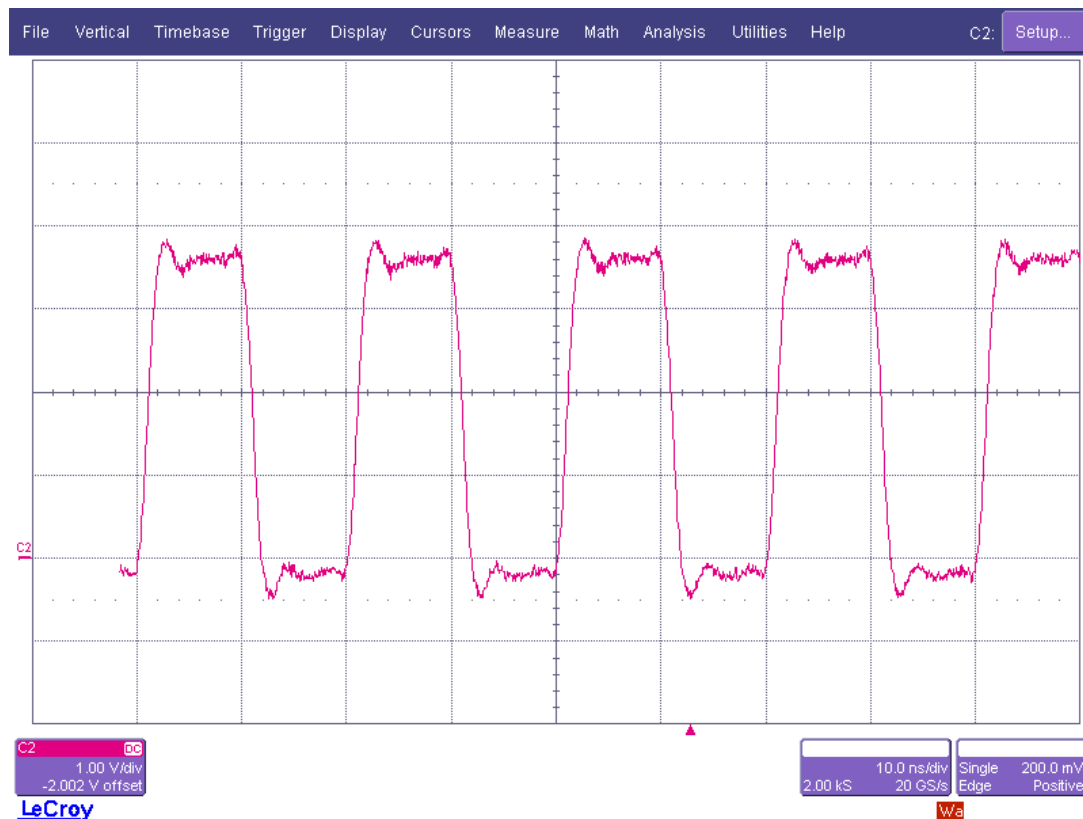
Figure C.42: Reference clock of 50MHz

controller device and waiting at least 30 seconds before performing another soldering seeing the big size of the PLL package, everything should go without incidence. Lastly, the amplifier device is soldered carefully adopting the same advices made for the PLL device, and be careful to not mount it in a wrong position. The whole soldered circuit is represented in Figure C.43.

C.9   Transmitter

In this section, one way of soldering a transmitter is presented. General key points to make a good soldering should still be kept in mind while going through this part. The transmitter comprises mainly two parts: one is the oscillator, which is exactly the same as mentioned in the above section and not repeated in this section. The other part is the baseband pulse generation circuits and RF mixer, soldering of which is explained with detail in the following. The schematics are presented in Figures C.44 and C.45. By studying these schematics, the circuit covered in this section is composed of a slow comparator (U_6), an inverter (U_7), a fast comparator (U_8), a transformer (T_1), a mixer (U_9) and some capacitors and resistors, of which
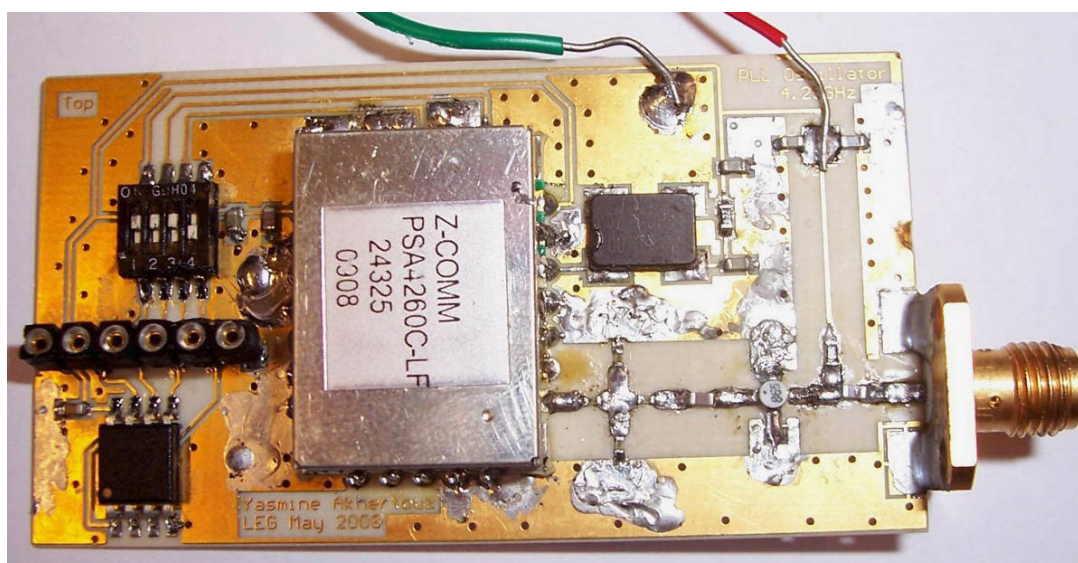
Figure C.43: Oscillator view

the resistor R_8 to R_{11}, and R_1 have 0402 footprints and the remaining have all 0603 footprints.

- **Step 1:** Solder all the capacitors and resistors. There are two clusters surrounding slow comparator and fast comparator, separately. Finish the soldering of one cluster before starting the soldering of the other in order to avoid missing components.

- **Step 2:** The slow comparator, inverter and fast comparator are relatively small compared with trimmer, transformer, and mixer, so they are soldered first. Make sure place the components in right orientation. Especially for the fast comparator, place the component carefully to fit the pins with the footprints.

- **Step 3:** Considering the left components: trimmer, transformer and mixer are relatively big and the transformer is placed in the middle of the other two, so transformer is soldered first. Noticing that even there are six pins for the transformer, the two middle pins are left free, since they are not used. Special attention should be given to the placing of this component to avoid short circuit. For the trimmer, the right pin should be cut away, and the ground pin should be heated with higher temperature to make good connection. The profile of mixer is larger than its footprint on PCB, so we have to cut the pins of mixer to make it fit in the footprint. Cutting should be done on the hard metal brick with scalpel. And the soldering of ground via should be done later when finishing the elementary test.
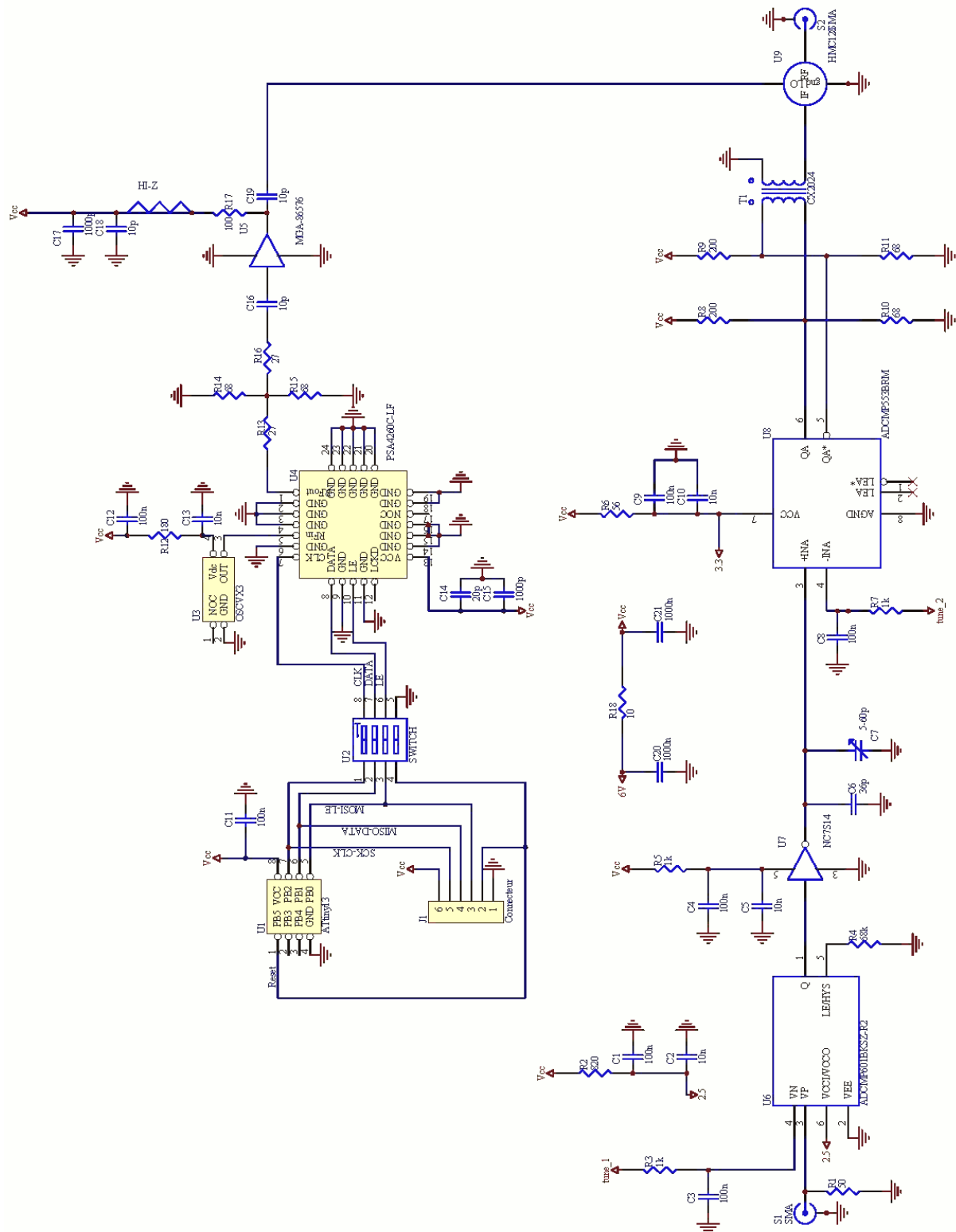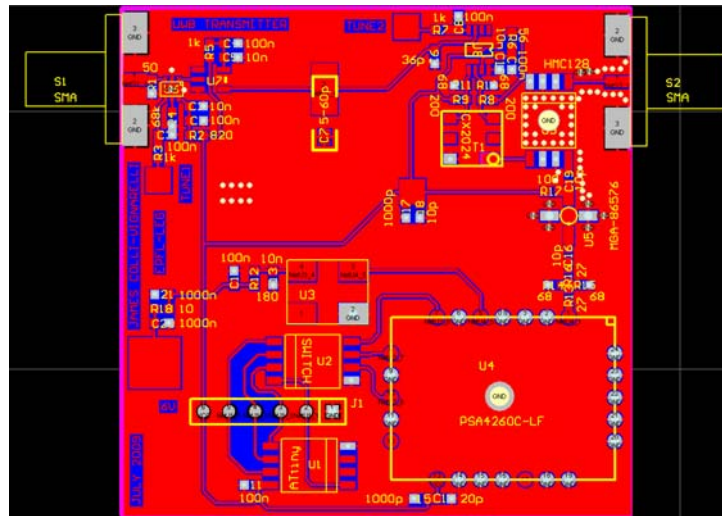
Figure C.44: Transmitter's schematic

Figure C.45: Transmitter's PCB

Figure C.46: Completed transmitter PCB

C.10   Customizing the shielding boxes

The commercially available shielding boxes are available in various sizes. An appropriate size can be selected according to the size of the PCB(s) to be enclosed. However, the boxes are

available without any through holes for SMA connectors, ground pins etc. Hence they need to be customized according to the PCB design by drilling in through and threaded holes for screwing in the connectors. This chapter gives a general overview of drilling and threading the holes in the shielding boxes.

C.10.1   Equipment Required

Figure C.47 shows the tools required for preparing the shielding boxes for customization. The tools shown are:

Flat Granite Plane The granite plane is a perfectly flat plane surface. All measurements and marking working should be done by placing the boxes on the plane to ensure accuracy.

Marking Gauge As its name suggests, the marking gauge (also called scratching gauge) is used to scribe a line parallel to a reference edge or surface of the granite plane. It has a sharp metal pin attached to a Vernier calibrated scale. The scale is used to adjust the height of the pin accurately and the then the pin is used to scratch the metal surface of the box.

Plan Drawing The plan shows the elevation and orthographic views of the shielding box giving the measurements for the location and diameter of the holes.

**Shielding Box** The shielding box to be customized.

Electric Drill The electric drill is installed on a stand and is used to drill in the holes in the boxes.

Cross Table Vice The vices have two degrees of freedom and can be used to position the box accurately under the drilling bit.

Vacuum Cleaner The vacuum cleaner is used to clean away the metal shreds and shaving produced during drilling.

C.10.2   Marking the boxes

The first step before marking the boxes is to prepare the plan of the boxes and ensure the correctness of the same. Software like Solidworks^{TM} can be used for the same. It is very important to check the accuracy of the drawings at this stage ourselves because if the plan
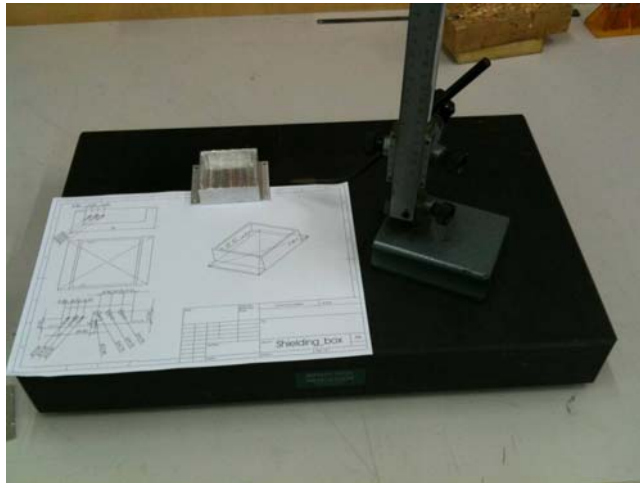
(a) Tools for marking the shielding boxes

(b) Tools for drilling the holes

Figure C.47: Equipment required

drawing is incorrect the holes will be misplaced. This could be detrimental since the connectors could then be misplaced relative to the pads on the PCB.

To begin marking the boxes place the granite plane on a flat surface and place the marking gauge on it. Choose one of the holes to be marked first and determine its height on the elevation plan. Set the marking gauge correctly to the same height. The uninitiated can refer to [87] and [88] to learn how to use the vernier scale. Figure C.48 shows the ruler set up for measurement. Now, put the box horizontally on the plane with the face where the hole has to be marked facing the marking pin. Run the pin of the gauge across the face of the box applying a firm pressure ensuring that there is a visible horizontal line as shown in Figure C.49.

To prevent errors of measurement and to be consistent in measurement and marking (and to save time as well), it is recommended to mark all the lines of the same height on one or multiple boxes and only then readjust the gauge for marking lines at other heights. Now, rest the box vertically against the edge of the plane and marks the lines measuring orthogonal distances. The intersection of the horizontal and vertical lines mark the center of the hole. Figure C.50 shows a finished marked box.

Figure C.48: The scale of the marking gauge

Figure C.49: Marking a line on the shielding box with the marking gauge

C.10.3 Drilling the holes

Drilling starts by first selecting the hole to be drilled. Determine the diameter of the hole from the plan and then fix the appropriate drilling bit into the drill. Place the box to be drilled in the vice with the face to be drilled facing up. Position the box using the cross table such that the drill bit is accurately positioned above the hole to be drilled. Give a few turns to the drill with the hand (without switching it on) to mark the position to be drilled. Check again if the mark made by the bit coincides with the mark drawn earlier. Readjust the position if required, else

Figure C.50: Shielding box with markings for center of the holes

switch on the drill and drill the hole. It is better to use a steady force and drill-in slowly rather as it creates a finer hole with a better tolerance to the required diameter. Keep the vacuum cleaner on while drilling as it will continuously suck away the metal shreds. Figure C.51 shows the drilling of one of the holes on a marked box. Note that once the hole is through the wall of the box, the drill bit should be lowered just a little further down but not farther as it may scratch the floor of the box.

C.10.4 Threading the screw holes

Figure C.52 shows the threading of an already drilled screw hole. To thread a hole determine the appropriate threading bit for the required diameter. Fix the bit into the handle and mount the box into the vice with the hole to be threaded facing up. Start by gently inserting the thread bit vertically into the hole and giving it a few turns. Keep on turning the tool while applying equal pressure on both the handles while ensuring all the while that the bit is completely perpendicular to the hole. Continue till the bit cannot be rotated further. Draw out the bit by gently unscrewing it back.

C.10.5 LNA shielding box

Considering the high operating frequency and coupling interference between various potential electromagnetic sources, it is necessary to put LNA and VGA in the shielding metal box to ensure clean electromagnetic environment. There are mainly three parts inside the LNA shielding

Figure C.51: Drilling a hole

Figure C.52: Threading a screw hole

box as shown in Figure C.53: LNA, bandpass filter and VGA. The input SMA is connected to the input of LNA while the output SMA is connected to the output of VGA. A bandpass filter connects the LNA and VGA while filters out unwanted signals. The GND hole in the shielding

box is used as common ground for box LNA and VGA. Bias and supply voltage for the LNA
and VGA are separated for decoupling and flexibility to optimize LNA and VGA individually
for optimal performance.

The mechanical work plan is designed in SolidWorks. The sizes and positions of holes and
screws are shown in Figure C.54. The holes and screws are made by following the instructions
in preparation of this mechanical section. It is advisable to follow these instructions to make
precise and nice work. For example, the tip of SMA connector should just touch the pad on
PCB to avoid any discontinuity or mechanical constraints. Mechanical constraints make the
connection difficult while discontinuity even degrades the impedance matching and further
deteriorates the performance.
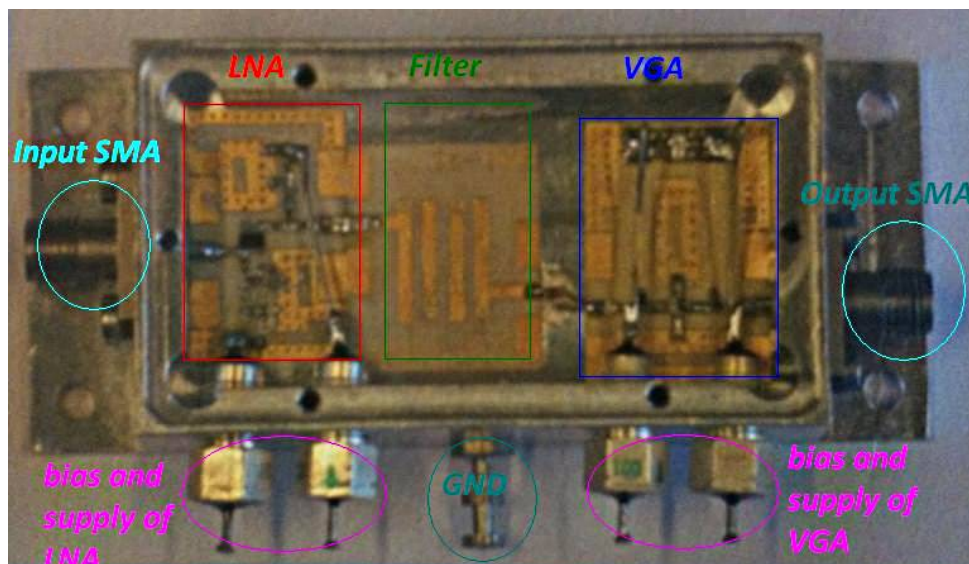
Figure C.53: LNA shielding box

C.10.6   Transmitter shielding

Figure C.55 shows the drilling plan of the transmitter shielding box. There are two SMA
connector holes, three supply voltage and tuning holes and one common ground pin hole. The
drilling and threading should follow the procedure given in Section C.10. Accuracy when
drilling this box is the most important: indeed having even one or two tenth of millimeter of
imprecision could lead to a dysfunction of the circuit. The problem comes from the SMA
connectors; if the connector does not fit precisely on the track, the input or output signal can
be shorted to the ground (not centered drilling), have discontinuities (too deep drilling holes)
or don't let space for the PCB to fit in the box (too low drilling). Thus, drilling imprecisions

Figure C.54: Work plan of LNA shielding box
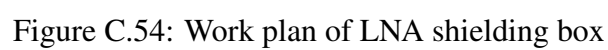
should be avoided as much as possible. However, some solutions exist ; one of them is to use Sandpaper to reduce the PCB size. The idea is to remove one or two millimeter of PCB where there are no components and signal tracks. The final result should look as presented in Figure C.56.

C.11   Finalizing the circuits

To be able to use these circuits, these last steps should be followed.

- **Step 1:** Glue the PCBs in their corresponding shielding boxes using argentic glue. Special care has to be taken when using the glue. When gluing, check that the PCBs are well aligned with the SMA connector holes; if yes, put some weights on the PCB so that it doesn't move.

- **Step 2:** Bake the boxes with the glued PCBs inside at a temperature of $80\,^{\circ}\text{C}$ for around 8 hours so that the glue solidifies. Make sure when you remove them that the transition in temperature is smooth to avoid damaging the components.

- **Step 3:** Now the SMA connectors should be machined with an abrasive tool to fit on the signal path on the PCB. The idea is to make tip of the connector thinner and give it a ramp shape as it is shown in Figures C.57 and C.58. Care must be taken while machining the tip since it is vulnerable to slide through and fro in the plastic enclosing.

- **Step 4:** The SMA connectors should then be screwed and the tip soldered on the PCB such that the solder completely inundates the connector tip but does not form a big sphere around it.

- **Step 5:** Screw one by one the supply voltage connector and solder a connexion line between the connector and the supply voltage pad it should feed. The output should resemble Figure C.59. When done, the PCB should be washed to be ready to use.
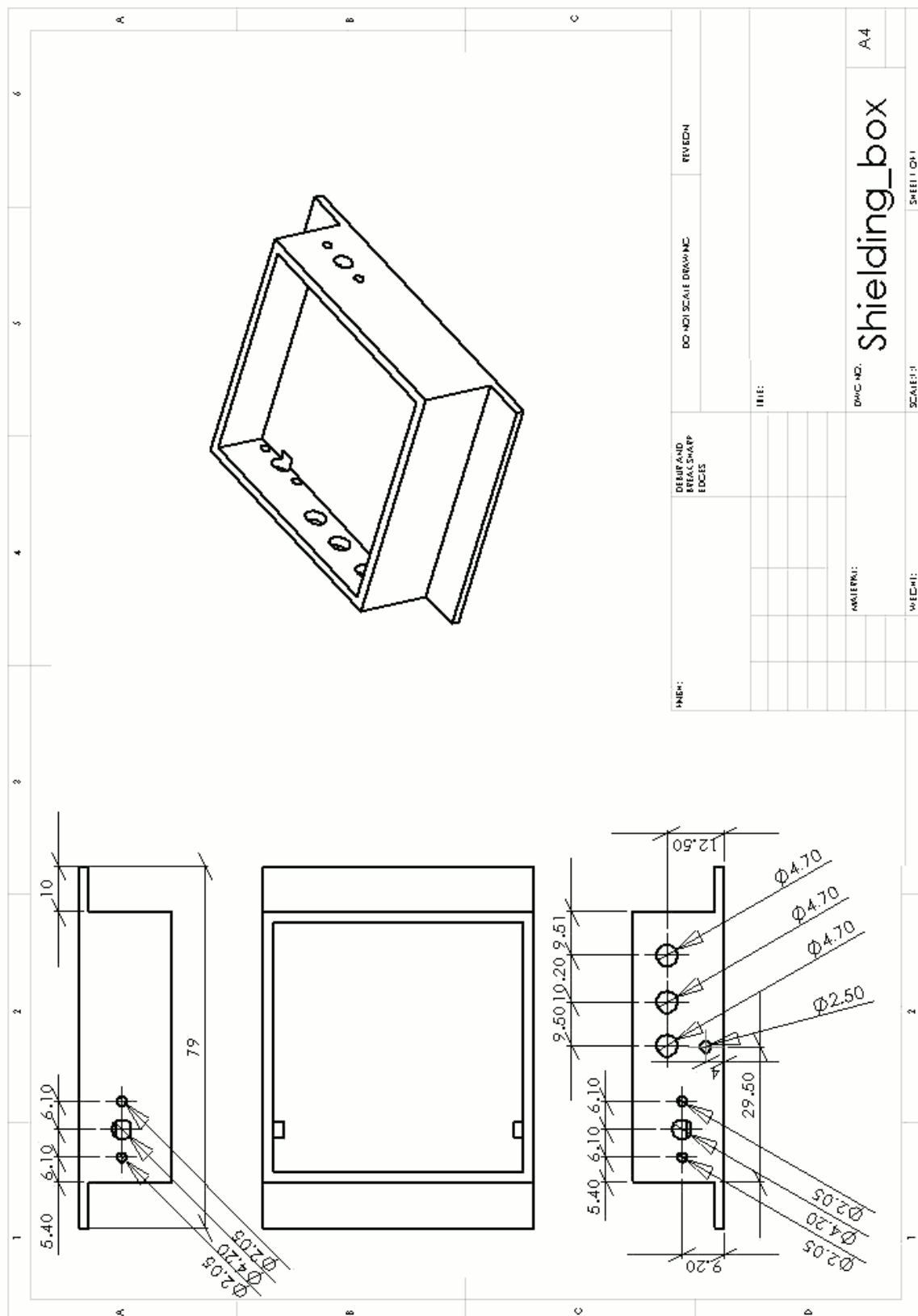
Figure C.55: Drilling plan of the transmitter shielding box
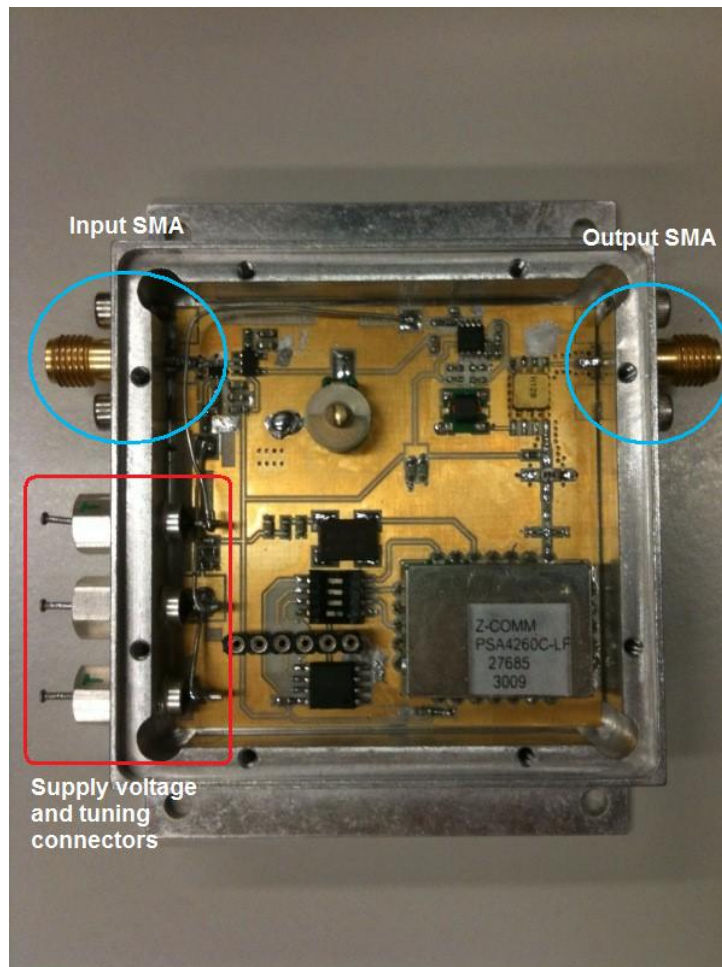
Figure C.56: Transmitter shielded

Figure C.57: SMA connector before machining

(a) Top View

(b) Side View

Figure C.58: SMA after machining

Figure C.59: Finished box

Chapter D

LNA n° 1 : addendum

D.1   Construction of LNA prototype n° 1

The aim of this section is to describe in detail how the circuit that was simulated in the previous section will be realised, and to explain what the points to take care of are. It is intended for people who have no particular knowledge on how to build very high frequency RF circuits. The first part explains how tracks are designed on the printed circuit board and how the components have been chosen and placed on the PCB. It shows also why every tiny detail has its importance at such frequency. The second part explains and guides the reader on how to build physically the circuit, what tools are used and some tricks that make the circuit realisation easy and reliable.

Traditionally, printed circuit boards are made with FR4 that is a very common material used for most of the circuits. In case of very high frequency design, FR4 is not appropriate because there are too many losses that attenuate the signal. For this reason, other materials were developed especially for RF designs. The material chosen for mounting the LNA is Duroid RO4003 from Rogers Corporation. This material supports RF designs until 10 GHz, that is widely enough for this application.

D.1.1   The printed circuit board design

The first step before doing any practical realisation is to give the schematic in the routing software as shown in the next sub-section. It also describes the component technology chosen for this circuit.

The schematics

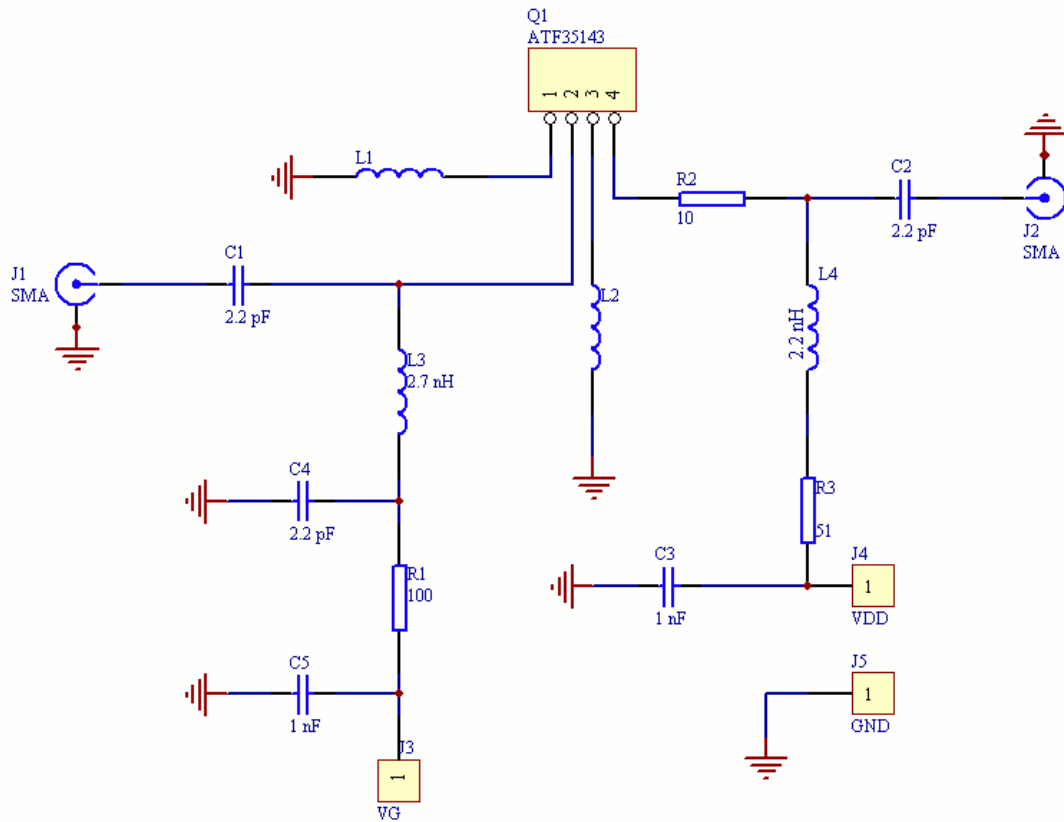The schematics of the single LNA is given in Figure D.1 as shown below.

Figure D.1: The schematic of the single LNA with pHEMT

This schematic is in fact a straightforward repetition of the ADS corresponding schematic. The LNA will be made with RF surface mounted components that are able to work at many GHz. Their case size is 0402 which is a very small package that needs careful manipulation when soldering as explained further. Because it is hard to estimate how much parasitic capacitance and inductance there will be in the design, L1 and L2 are expected to be made in two different ways. The first is to use SMD Coilcraft RF inductances of 1 nH with tracks as short as possible. The other possibility is to use a microstrip inductor whose dimensions are designed to reach also 1 nH. Further measures and tests will show what is the microstrip inductance is the best solution.

The case of the complete LNA schematic is more complex because there are some modifications in comparison with the ADS schematic as shown in Figure D.2 below.
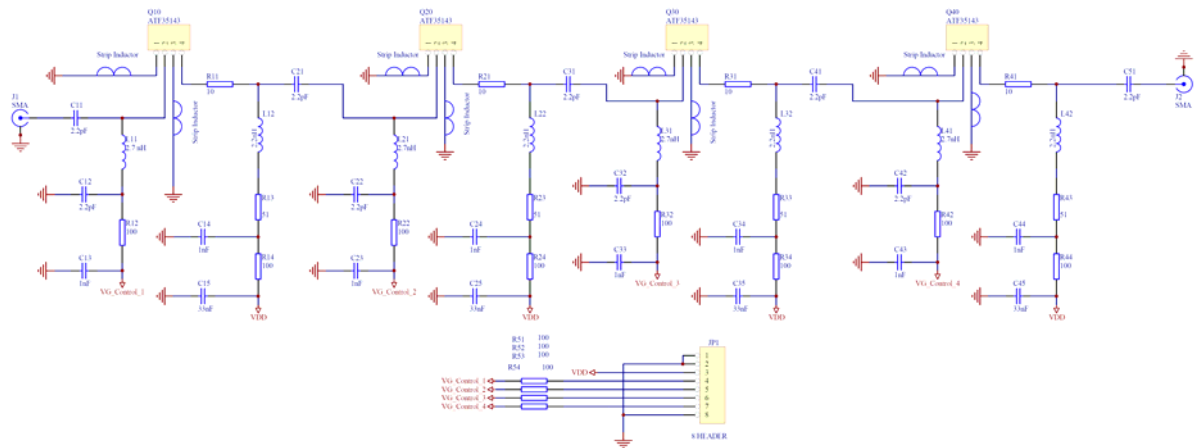
Figure D.2: The Protel schematic of the complete LNA with pHEMT

The modifications shown in the schematic come from experimentations on connecting two single LNAs with microstrip inductance degeneration in cascade in order that these single LNAs have a very good matching and gain performance when connected together without any modification. For these reasons, the single LNA schematic was simply repeated four times in the complete LNA schematic. The only modification made here is the decoupling circuitry in order to have a greater separation between stages. This is necessary because experimentations show that the circuits oscillates when there are in cascade due to the feedback through the power supply lines.

The next step needed before designing the layout is to determine the dimensions of the transmission lines that will connect the LNA stages and the SMA connectors together and also to determine the dimensions of the source microstrip inductances. This is the purpose of the Matlab scripts presented in Appendix A.1.1 and A.1.4 for calculating a track matched to 50Ω and to create a microstrip inductance of 0.3 nH respectively. In order to clarify the variable definitions, a cross section view of the board with the microstrip dimensions is given in Figure D.3 below.
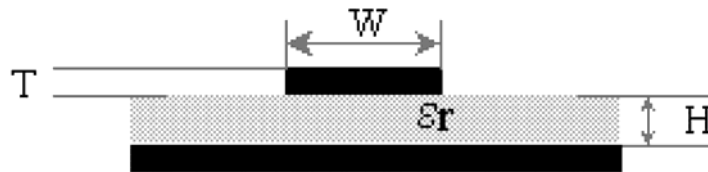
Figure D.3: Microstrip cross section view

The value obtained for the stripline track width is 48 mils and calculating the microstrip inductance gives :

- Z_0 equals 34.6 Ω;

- T_{pd} equals 3.84 ps;

- C_0 equals 0.003 pF;

- L_0 equals 0.332 nH

These values were obtained in order to reach a small value of L_0 because experimental results were good when testing the single LNA. In fact, as explained later, this value has to be increased because when LNA are cascaded, they become unstable. However, this value is sufficient for preliminary results.

The PCB layout

At such a frequency range, the design of a PCB becomes more as much an art than a science. The purpose of this sub-section is to explain some points that are important to focus on when designing a RF circuit board. It explains why some tracks are made in a given manner rather than another.

There is a list of points that are all of great importance when designing a RF layout :

- Straight angles should be avoided as much as possible because it introduces locally a mismatch which induces reflexions, and thus a loss of signal power;

- The design has to be as small as possible in order to reduce the resistive losses in copper tracks;

- Tracks should be gold plated in order to avoid oxidation and thus a degradation of the electrical properties of the PCB;

- No varnish or any other protecting layout should be deposited at the PCB surface because it modifies the relative permittivity of the material which can modify the matching of the transmission lines;

- Pads of SMD components should be larger than the pad itself because the soldering is made by hand, so it needs some place for the soldering iron tip;

- All individual power supplies should be strongly decoupled to each other in order to avoid oscillations;

- The ground plane is of high importance because it ensure the return path for every signal and power supplies; it also shields the circuit against parasitic interferences;

- Vias are of high importance when connecting a pad to the power ground; they need to be small and numerous in order to reduce the parasitic inductance they introduces (it has been shown previously the importance of a correctly controlled inductance value);

The obtained layout are shown in Figures D.4 and D.5 for the single LNA with respectively a discrete and a microstrip inductance degeneration.
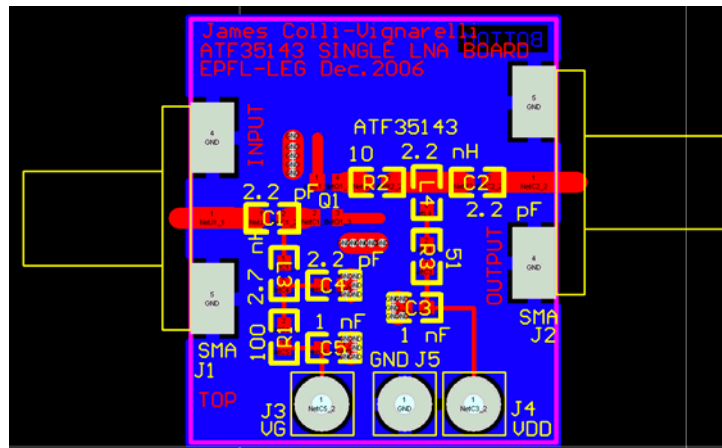
Figure D.4: The PCB layout of the single LNA with discrete source inductances

The size of the microstrip inductance is given by the Matlab script explained previously with the same values.

The wide tracks are transmission lines carrying the RF signal; their width is of 48 mils. In theory, their length is not important for the matching when this one is correct. However, too much long lines introduce power loss.

The complete LNA is shown in Figure D.6. As explained previously, it is mainly a copy of four single LNAs with microstrip inductances. However, additional capacitors and resistors were placed in order to improve the power supply decoupling as shown in the corresponding schematic. Finally, large copper traces were added in order to solder on them the shielding box
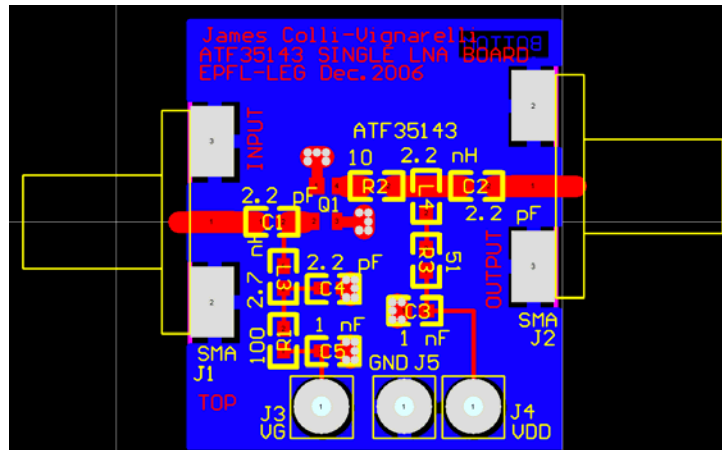
Figure D.5: The PCB layout of the single LNA with microstrip source inductances
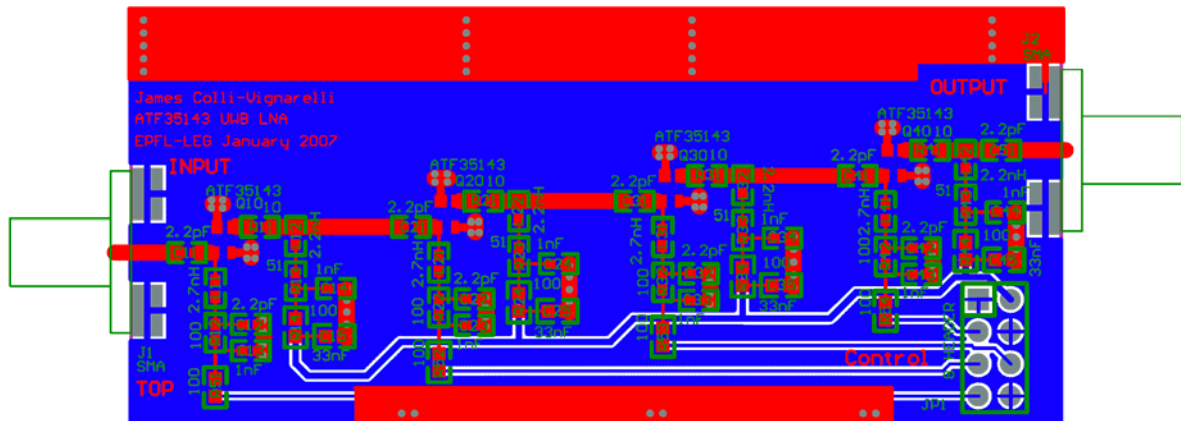

Figure D.6: The PCBlayout of the complete LNA

which will be made by assembling some pieces of copper together in order to make a box with walls inside it that separate every single amplifiers, as shown further.

D.1.2   The printed circuit board construction

This sub-section will explain the practical construction of both single and complete LNAs. The circuits were made by a specialised department in EPFL because of the metal plating of vias. Before doing any soldering, the circuits were gold plated with gold cyanide and then the texts printed in the copper were tinned because they are too small for the gold plating brush.

Since components are very sensitive to heat and the Duroid is a very good thermal conductor, it is important to solder first connectors, then the passive components and last, the transistor.

The soldering iron tip should be as hot as possible in order to perform very quick soldering. The temperature used was around $450\,^{\circ}\text{C}$. It is better to solder quickly with a hot tip rather than longer with a colder one.

The best way to solder the connector is to solder first the central pin of the connector on the PCB and then, to maintain the whole in a vice as shown in Figure D.7. It is then easy to solder the body of the connector on the PCB; this position helps the soldering tin to melt on both the connector and the PCB.

Figure D.7: Large and close view on the single LNA showing how to solder the SMA connectors

The passive components are soldered as follows. First a drop of tin is deposited on the track; the component is then maintained on it with a thin tool and a liquid that helps the tin to melt on the material is added. When the tip of the iron touches it, the tin melts and the pad is soldered. It is important to check here that the component lies horizontally on the board. The same procedure for the other pad ends the soldering of the components. It can be useful to test the soldering with a multimeter.

The transistor is soldered in the same way with the exception that it is better to wait for 30 seconds before performing another soldering in order to give enough time to the heat to leave the transistor package. It is very important to never test the transistor solder joints with a multimeter because it can destroy it. The final results is shown in Figure D.8.

The procedure for building the complete LNA is the same, with the exception that there is a shielding that has to be made, as shown in Figure D.9.
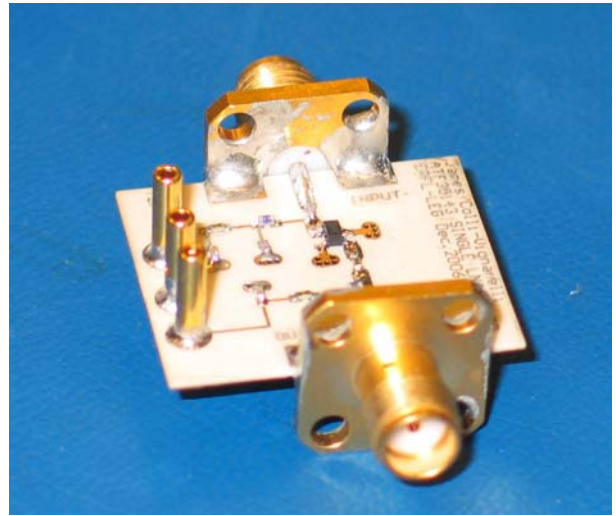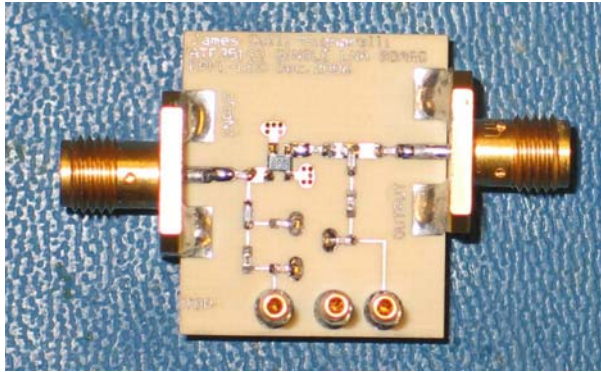
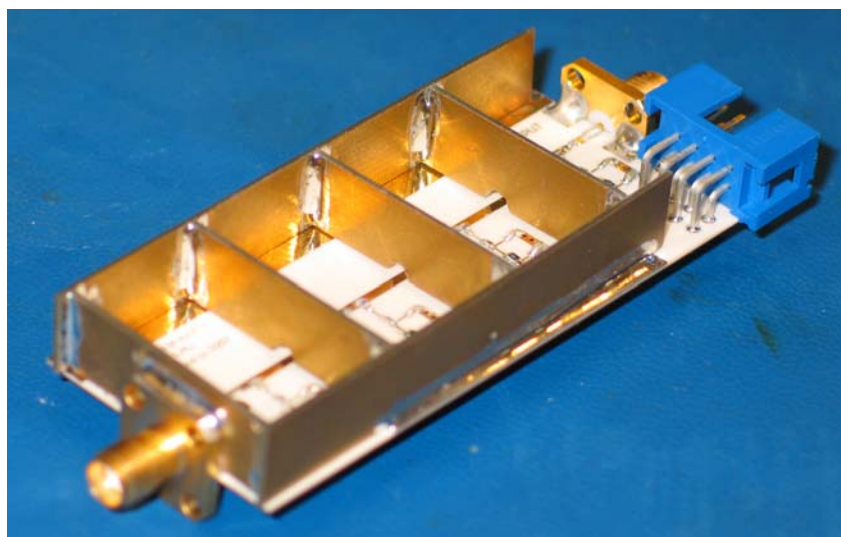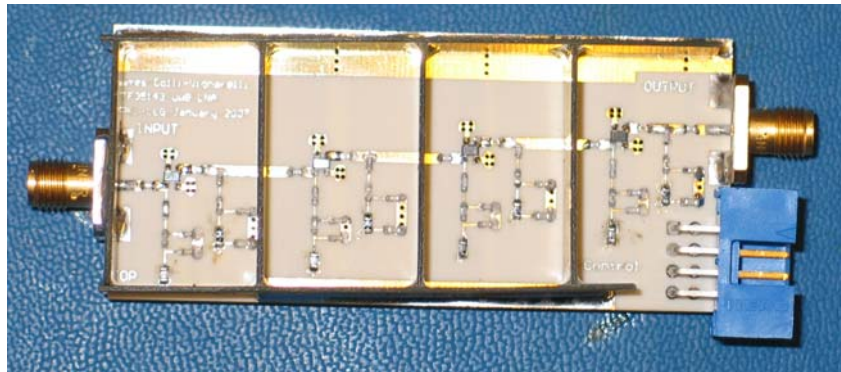Figure D.8: Close views on the single LNA

Figure D.9: Close views on the complete LNA with its shielding

The shielding box is made with small rectangular pieces of copper that are soldered together. There is no specific dimensions they need to have. It is important however to make a small hole in the internal walls in orde to avoid a short circuit with the signal path. It can be helpful to use weight for maintaining the pieces of copper when soldering in order to keep them in the correct position; it is particularly important because the shielding box will be soldered on the PCB, so any mismatch here will introduce slots that the solder could not fill up.

If the previous steps were made correctly, the builder is expected to obtain the same measure results as shown in the next section.

D.2   Improvements of the LNA prototype nº 1 construction

The printed circuit board improvement

The first point that should be considered when improving the PCB is the design of the source inductance. By running the Matlab script described in section D.1.1 with a length of 50 mils and a width of 25 mils (as previously) gives the following values:

- Z_0 equals 30.35Ω;

- T_{pd} equals 6.50 ps;

- C_0 equals 0.011 pF;

- L_0 equals 0.822 nH

These values are acceptable especially given the fact that the value of the inductance is very sensitive to any variation of its dimensions in this range. The corresponding PCB is shown in Figure D.10.

There are also many other modifications of the previous design. The power supply and control connector is placed in the middle of the bottom edge because it allows having a better separation between the control and power supply lines; in the previous design, these were too much close to each other. The ground plane on the top side surrounds now completely the circuit in order to solder the shielding without leaving any slot.

As shown in Figure D.11, the power supply connection is also corrected in order to have the vias arriving below the decoupling capacitor and not below the resistor, improving thus the decoupling.

Figure D.10: The layout of the complete LNA PCB

Figure D.11: Detail of the power supply connection

The shielding improvement
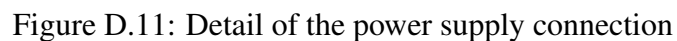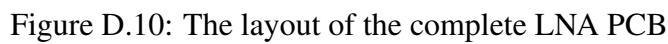
The shielding of the circuit is one of the most important points to consider when improving the stability. The frequency range involved in this design is so high that any part of the circuit will radiate and influence the other parts, introducing thus a lot of feedback which will make the amplifier to oscillate. For this reason, the circuit must be completely closed inside a metal box with conductive walls inside it in order to separate and shield every stage of the LNA. The previous design shielding was made with some double-sided PCB material that was assembled to make a box with walls; however there were some parts of the circuit that stay open, introducing

thus a lot of RF radiation. The new shielding is made with a 0.2 mm beryllium copper plate and it closes the entire design as shown in Figure D.12.
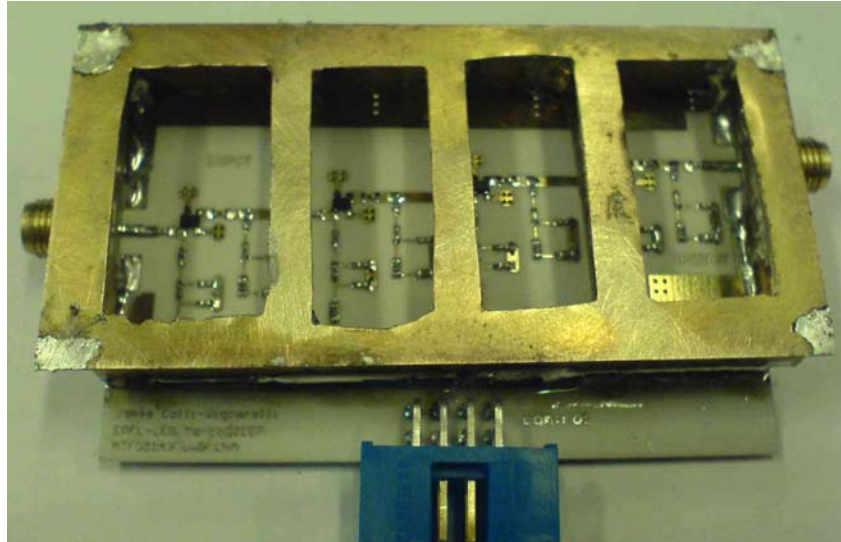
Figure D.12: The new complete LNA with its metal shielding.

Although it is important to shield completely the circuit, it is also important to allow the user to open it in order to replace any defective part of the circuit if necessary. For this purpose, the shielding consists of a metal box that is soldered on the PCB tracks that surrounds the circuit, and whose top plate has four square holes for servicing purpose, as shown in Figure D.12. These holes are closed in normal operation with an adhesive tape of copper as shown in Figure D.13. The shielding's construction is similar to that of the previous design. The surrounding and internal walls are cut in the beryllium copper plate with shears and they are gold plated in order to avoid oxidation. They are then assembled and soldered in order to make a rectangular box that fits the surrounding tracks of the circuit and also that touches both SMA connectors. The edges are equalized with a sheet of abrasive paper in order to avoid any slot when soldering both the top plate and the circuit. The top plate is soldered on this assembly and the four holes are cut. This is simply done by making small holes with a drill that follow the outline of the square hole. The central part of metal is removed with a small cutting pincers and the edges are smoothed with a file. A small hole is made in every internal wall with a file in order to avoid short circuit with the signal track and a rectangular hole is made in both side walls that touch the SMA connector in order leave some place for their corresponding soldering. When the shielding is finished, it is soldered on the circuit board by taking care of the SMA connectors and the signal tracks that go under the internal walls. It is important to use a very hot soldering

iron and to perform a quick solder in order to avoid the transistor destruction. The solder joint has to run along the outline of the box on the circuit.
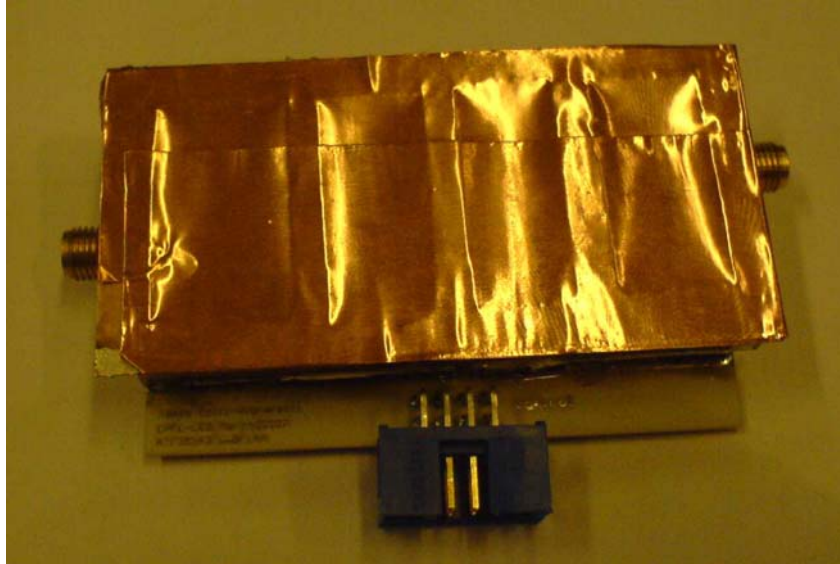

Figure D.13: The new complete LNA with its shielding closed.

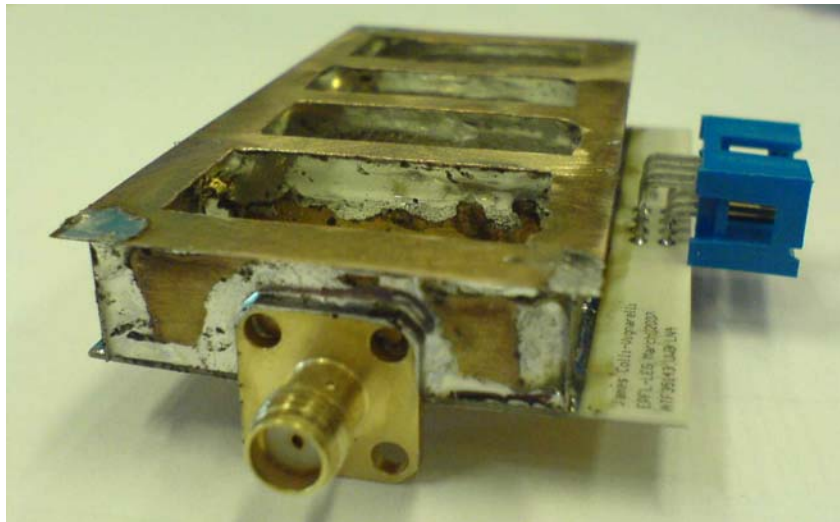The outline comprises the the SMA connector shape as shown in Figure D.14.

Figure D.14: Detail of the box soldering including the SMA connector.

The solder joint ensures thus a completely closed shielding of the LNA. For this reason, the shape of the hole in the wall that let the place for the SMA soldering should be as much as possible close to the connector's edge in order to allow a good soldering joint between the connector and the wall, as shown in Figure D.15.
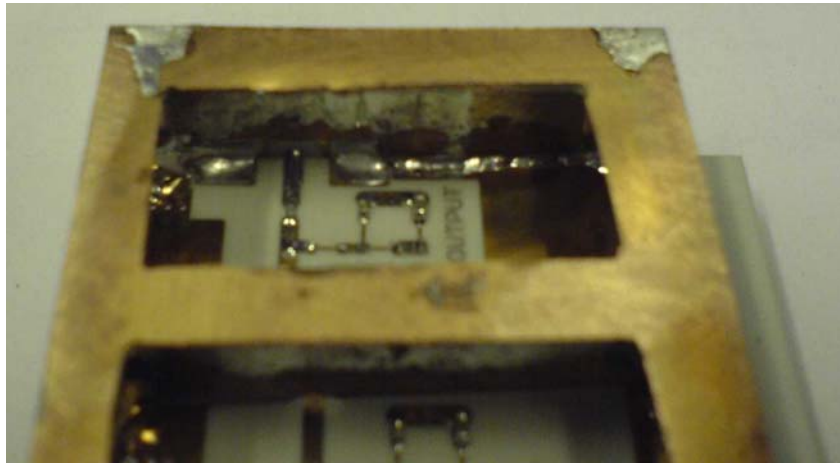
Figure D.15: Close view on the internal side of the shielding box.

It is also possible to see in Figure D.15 how the small hole made for the signal track is adjusted to the circuit dimensions and how the internal wall fits perfectly the printed circuit board.

Measurements

The obtained LNA is installed as shown in Figure D.16 for the measurements. A sine wave generator and a spectrum analyser are used to determine the behaviour of the circuit; there is also a network analyser that is not shown in this picture.

The full bandwidth spectrum of the LNA is shown in Figure D.17 with an input signal at 4.25 GHz and a power of -60 dBm. Although all the corrections made previously, the oscillations are always present, so they are not linked to a problem with the shielding as said previously. In order to understand what induces these oscillations, a network analysis was performed: the S parameters are the same as these obtained with the previous complete LNA. The S_{11} and S_{22} parameters become positive regardless of the simulation results; the impedance matching should be reconsidered in further LNA designs (at this point, the positive S_{11} and S_{22} parameters means there are oscillations somewhere in the circuit but we cannot exclude that these oscillations are due to a mismatch between two consecutive stages). Since simulations are useless here, the only way to obtain an improvement is to replace SMD components at input, output and between single LNA with other components having a neighbouring value (manual tuning). These components are mainly the coupling capacitors; however it is only a supposition at this point. The spectrum was also measured with a resolution bandwidth of 100 KHz in order to distinguish between thermal noise and effective oscillations as shown in Figure
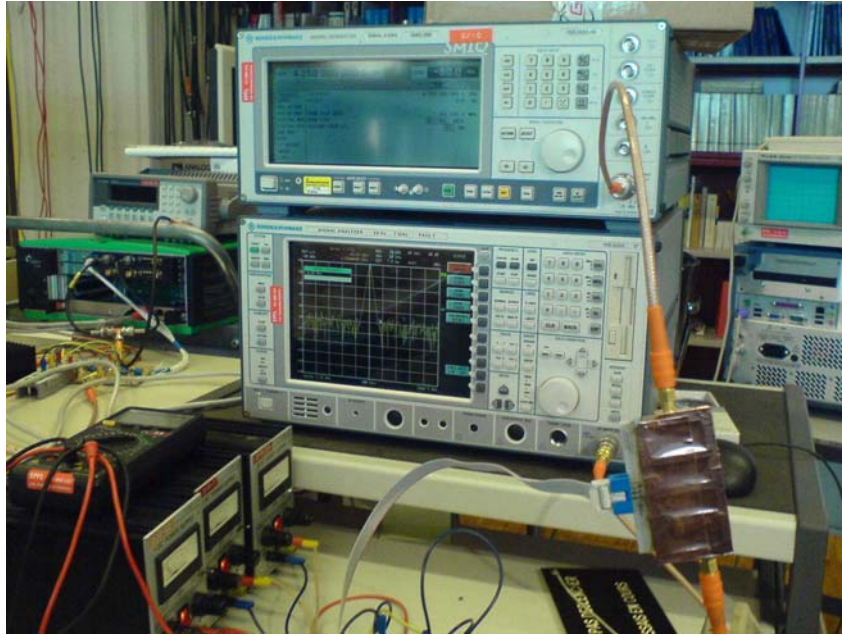
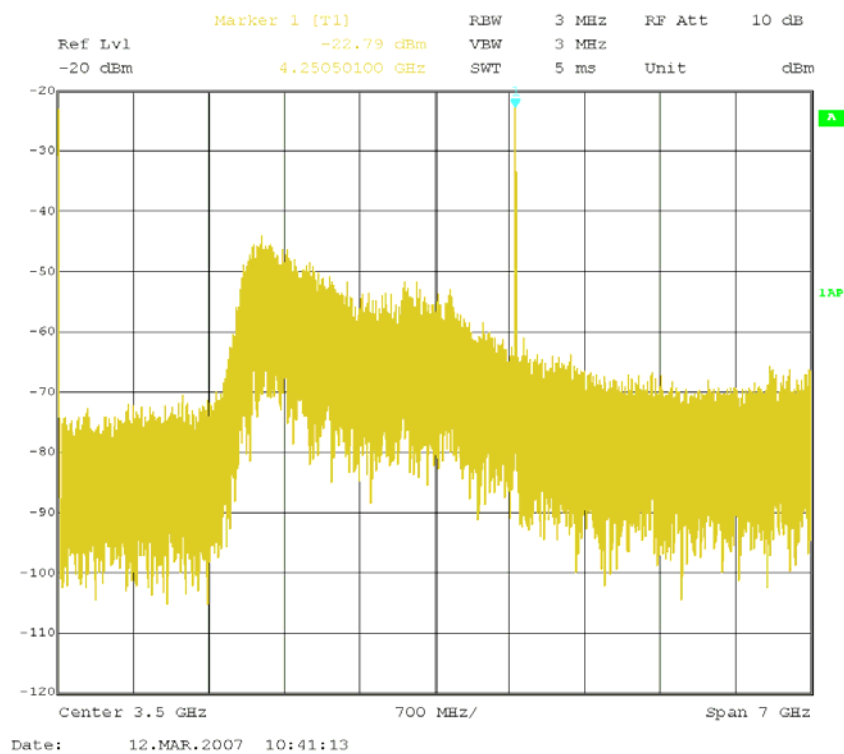Figure D.16: A view on the measurement tools used with the LNA.

Figure D.17: Spectrum of the output of the LNA from 0 to 7 GHz.

D.18.

Figure D.18 shows a parasitic peak at 1.84 GHz with its corresponding harmonics. Since
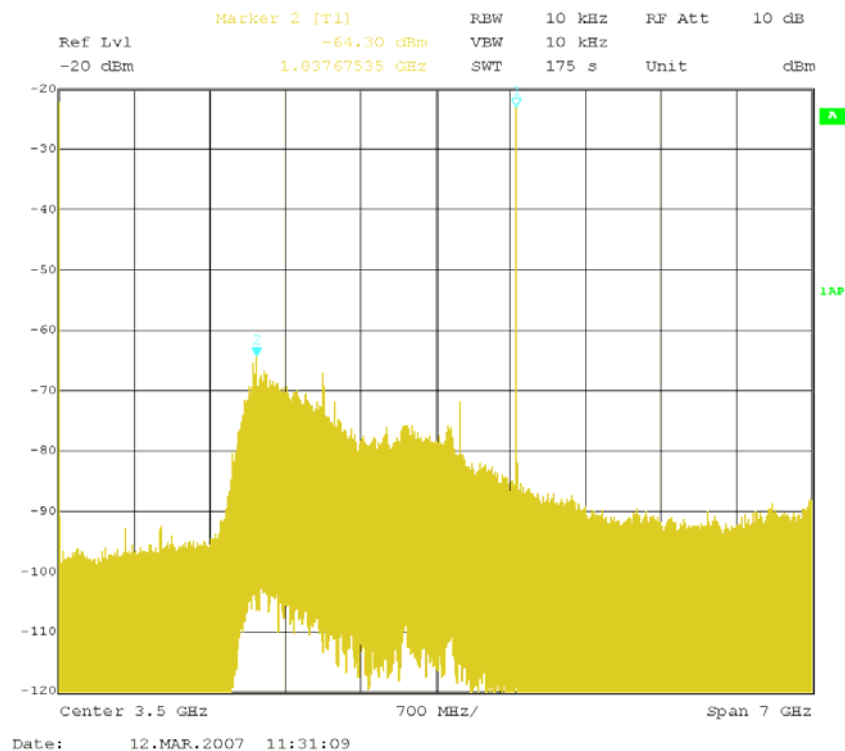
Figure D.18: Spectrum of the output of the LNA from 0 to 7 GHz, with 100KHz of bandwidth resolution.

its value is around -64.3 dBm, it does not interfere too much with the signal of interest. At this point, it is however interesting to see how the LNA behaves in the desired bandwidth. This is shown in Figure D.19.

This shows that the LNA works as expected in the frequency range of interest because it has almost the same behaviour when the input sine wave is 4.0 GHz and 4.5 GHz. It is a good point that the oscillations do not disturb the signal in this band. Another good reason why these oscillations will not affect the transmitted signal is the presence after the LNA of the band-pass filter made at LEMA which is designed to let only signals between 4.0 until 4.5 GHz to go on.
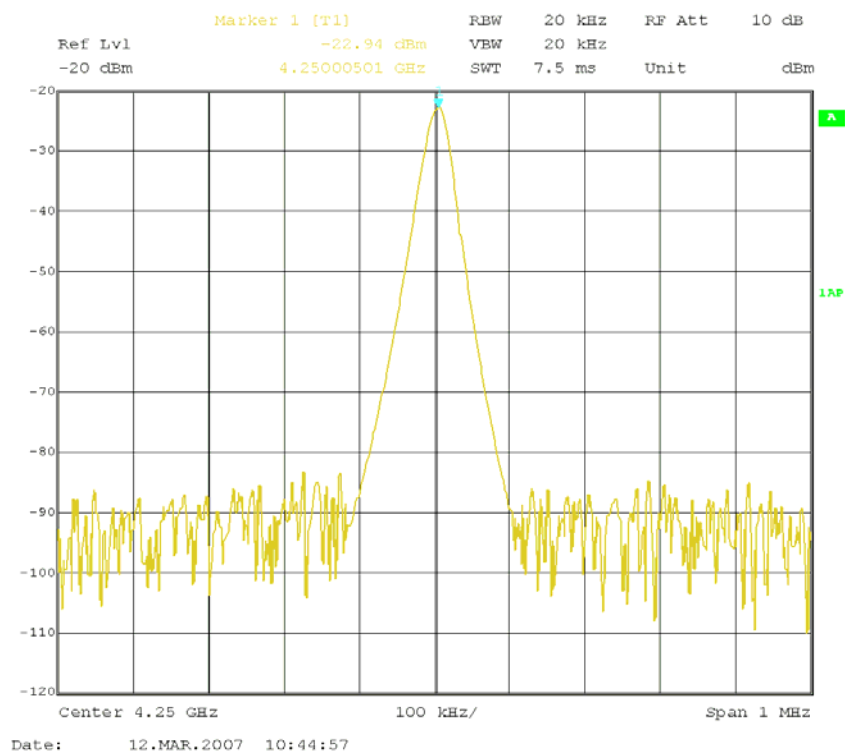
Figure D.19: Close view on the LNA at 4.25 GHz, with a span of 1 MHz.

Chapter E

Resistive Networks

In the design of RF circuits, it is necessary to connect several devices together by ensuring that their characteristic impedance is matched. Fortunately, the characteristic impedance is fixed, usually to 50Ω. This appendix presents two fundamental resistive circuits, the power splitter/combiner and the attenuator, that is very useful in this work for the design of UWB devices.

The circuits presented in this Appendix have a very useful property: they can be designed independently and connected together without the need to calculate the whole network. This independence comes from the fact that the impedance matching condition makes the impedance seen on all terminals of the circuits to be perfectly known and constant. It is thus possible to build an arbitrarily large and complex resistive network by duplicating and connecting the circuits described here without the need to consider all the parts of the networks in the calculations.

E.1   Power splitter/combiner

This section describes the power splitter/combiner resistive networks. The power splitter/ combiner are fundamentally the same circuit; the distinction between splitter or combiner depends mainly on the direction of the power flow on the terminals. More generally, when there are more than three terminals, it may not be possible to tell if the circuit is splitting or combining power because it can do both. The power splitter/combiner circuit is shown in Figure E.1. Its architecture is very simple: all ports are connected through a resistor to the same point in a star configuration. The resistor value R is the same for all ports because of the symmetry and

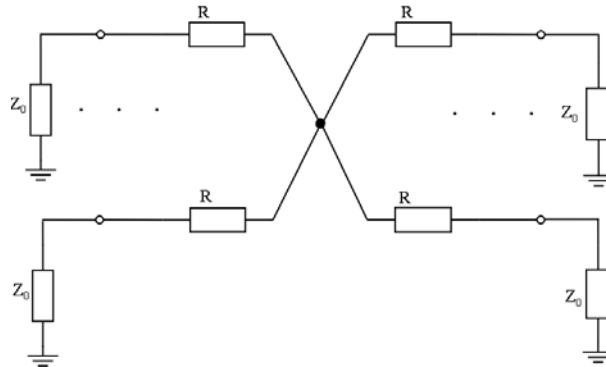depends only on the number of ports for a given characteristic impedance.

Figure E.1: Power splitter/combiner circuit

This network needs to be matched on an impedance Z_0 that we assume to be real (no complex part). Let N be the number of ports of the power splitter/combiner. For calculating the value of R that ensures impedance matching, one port is considered and the equivalent impedance of the $N-1$ other ports is calculated, as shown in Figure E.2.
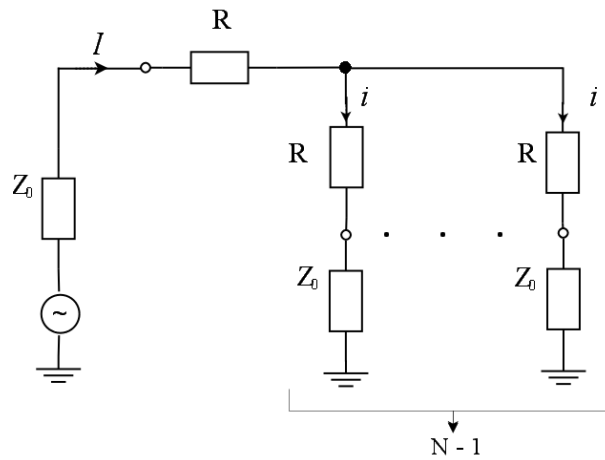

Figure E.2: Impedance seen by one port with definition of currents and voltages

E.1.1   Calculation of R

Considering figure E.2, the input impedance at one port is given by:

$$Z_0 = R + \frac{R + Z_0}{N - 1}$$

If all ports are matched, the input impedance Z_0 corresponds to the characteristic line

impedance. The resistance R is thus obtained from the previous equation:

$$R = \frac{N-2}{N} \cdot Z_0$$

E.1.2   Calculation of the attenuation

If I the total amount of current injected in the circuit, the current i in each branch is:

$$i = \frac{I}{(N-1)}$$

and the power dissipated in each port is given by:

$$P_0 = Z_0 \cdot i^2$$

while the power injected at the input corresponds to:

$$P_i = Z_0 \cdot I^2$$

The gain due to the resistances of the power combiner is given by:

$$G = 10 \log \frac{P_0}{P_i} = 10 \log \frac{1}{(N-1)^2}$$

so the attenuation A of the resistive networks corresponds to:

$$A = -G = 10 \log(N-1)^2$$

Because the signal is equally split, the attenuation of power seen in the other ports depends only on the number N of ports. The resulting resistances' values, gains and attenuations with respect to the number of ports are shown in Table E.1.

The equations of this circuit show that the attenuation/gain of the power splitter/combiner depends only on the number of ports N; in practice, an amplifier may be required after the power splitter/combiner. In the trivial case when there are only two ports (see Table E.1), all the power is transmitted from one port to the other and the gain is one; there is no need of resistance R to adjust the power so R is zero. When the number of ports increases, the gain decreases as well, and with an infinite number of ports, the gain is zero, which means that there

is no transmitted power to the other port because of the dilution; the output power is also zero.

Ports	R [Ω]	Gain	Gain[dB]	Attenuation	Attenuation [dB]
2	0.000	1.000	0.000	1.000	0.000
3	16.667	0.250	-6.021	4.000	6.021
4	25.000	0.111	-9.542	9.000	9.542
5	30.000	0.063	-12.041	16.000	12.041
6	33.333	0.040	-13.979	25.000	13.979
7	35.714	0.028	-15.563	36.000	15.563
8	37.500	0.020	-16.902	49.000	16.902
9	38.889	0.016	-18.062	64.000	18.062
10	40.000	0.012	-19.085	81.000	19.085

Table E.1: Gain and attenuation of an N-ports

The attenuation is caused by two factors: the splitting of a given amount of power between several ports and the thermal dissipation in the resistor R. When the number of ports increases, the value of R increases and approaches 50Ω so the thermal dissipation becomes maximum; the power splitter/combiner has thus a better yield when N is small.

E.2   Power splitter as an attenuator

An attenuator is a two port used to decrease the power of a signal by dissipating thermally the excess of non-desired power; the design of an attenuator in RF circuit requires to ensure the impedance matching on both ports. An attenuator is generally designed by using non inductive resistances. There are several types of attenuators: Pi attenuator, Tee attenuator, bridged-Tee (T), balanced attenuator, reflection attenuator (see Figure E.3 and [89, 90]). The Tee, Pi and bridged Tee require two different resistance values, while the reflection and balanced attenuators need only a matched pair of resistors. In this section, we study only the Pi, T and bridged T attenuator, as the goal is to find an attenuator which has a fixed constant attenuation.

The idea is to design a circuit that has different attenuations for each port. The first case is based on a power splitter which could be used as an attenuator (see Figure E.3), the second case is based on a power splitter for which the input port has a T-type attenuator (see Figure E.5). The third case is based on a power splitter/combiner for which one of the port has an attenuator (see Figures E.6 and E.7) and the last case is based on a Tee-attenuator-pad (see Figure E.8).
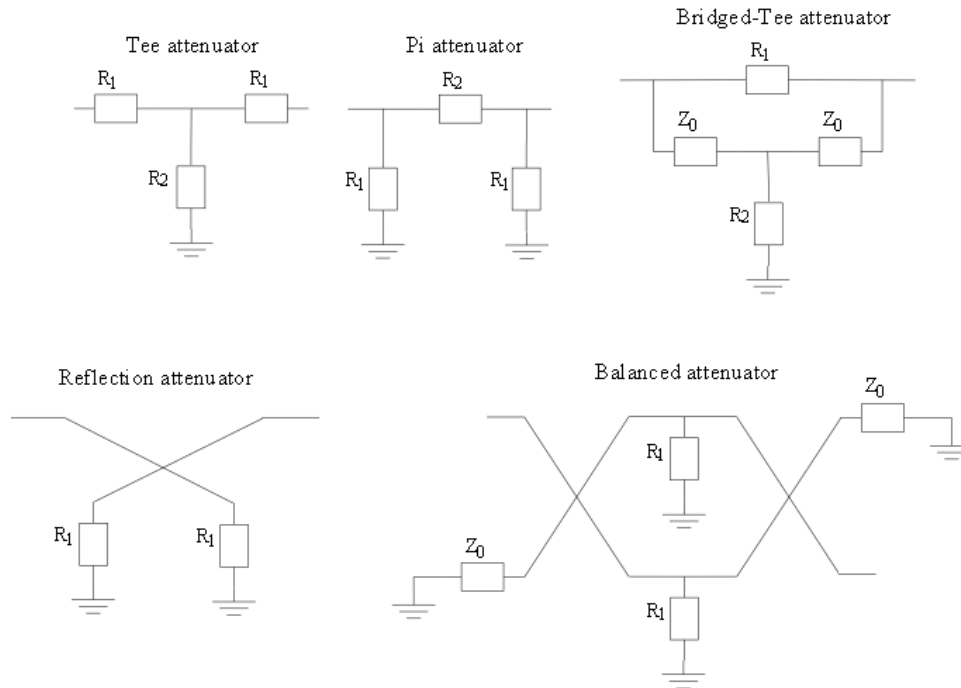
Figure E.3: Different types of attenuators (see [90])

Initially, the power splitter was used to split the power in different ports. With the help of this circuit, would it be possible to build power attenuators that use the same principle, so that the power on a port is weakened ? We study different cases for this purpose.

E.2.1   Case n⁰ 1 : Power splitter with at input port a Tee-type attenuator

The question that we want to answer here is : *Is it possible to make an attenuator using a power splitter/combiner, with $N = 3$ ports ?*
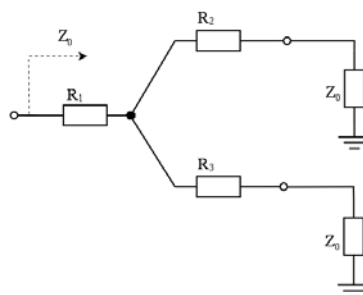
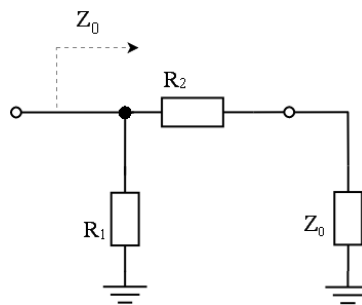Figure E.4: Power splitter attenuator

As the attenuator impedance is matched, the impedance seen by the amplifier is equal to

the line impedance Z_0:

$$Z_0 = R_1 + (R_2 + Z_0) \parallel (R_3 + Z_0)$$

After calculation, we have:

$$Z_0^2 - 2Z_0 R_1 = R_1 \cdot R_2 + R_2 \cdot R_3 + R_1 \cdot R_3$$

We note that if we calculate the input impedance seen from the other port, the right member of the above expression will remain the same because of the symmetry of the circuit. We thus have :

$$R_1 \cdot R_2 + R_2 \cdot R_3 + R_1 \cdot R_3 = R = \text{constant}$$

Because the above expression remains the same for each port when a circular permutation is made, we have :

$$Z_0^2 - 2Z_0 R_1 = Z_0^2 - 2Z_0 R_2 = Z_0^2 - 2Z_0 R_3 = R$$

this means that all resistance have to be of the same value:

$$R_1 = R_2 = R_3$$

This proves that this is exactly the power splitter/combiner we presented in Section E.1 where $N = 3$.

E.2.2 Case nº 2 : Power splitter with at input port a Tee-type attenuator

The question that we want to answer here is : *Is it possible to make an attenuator using a power splitter/combiner, with T-attenuator at the input port* ?

Figure E.5: Power splitter with T-attenuator

As the impedance attenuator is matched, the impedance seen by the amplifier is equal to the line impedance Z_0

Condition 1: $Z_0 = R_1 \parallel (R_2 + Z_0)$

which leads to:

$$R_2 = \frac{Z_0^2}{R_1 - Z_0}$$

and

Condition 2: $Z_0 = R_2 + (R_1 \parallel Z_0)$

which gives:

$$R_2 = \frac{Z_0^2}{(R_1 + Z_0)}$$

These conditions are contradictory: this circuit cannot work.

E.2.3   Case nº 3 : Power splitter/combiner with T-type attenuator at one output port

The question that we want to answer here is : *Is it possible to make an attenuator using a power splitter/combiner, with T-attenuator at one of the output ports*?

In this case, the power splitter is useful. As the attenuator impedance is matched, one uses the results obtained previously (Case 1). The impedance seen at the output and the input with an attenuator is equal to the line impedance Z_0.
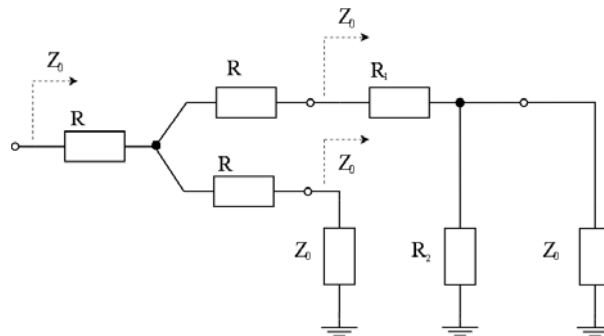
Figure E.6: Power splitter with attenuator at one of the output

Using impedance matching properties, one studied the matching of impedance at this output. Therefore it will be easy to obtain a simple expression which leads to a contradiction.

Condition 1: $Z_0 = R_1 + (R_2 \parallel Z_0)$

which corresponds to:

$$R_1 = \frac{Z_0^2}{R_2 + Z_0}$$
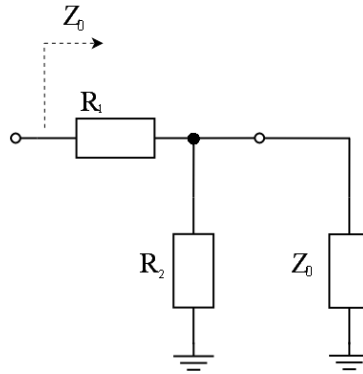
Figure E.7: Impedance seen from the input of the attenuator

Condition 2: $Z_0 = R_2 \parallel (Z_0 + R_1)$

which gives:

$$R_1 = \frac{Z_0^2}{R_2 - Z_0}$$

These conditions are contradictory: this circuit cannot work.

E.2.4   Case nº 4 : Power splitter/combiner with attenuator-pad at one output port

The question that we want to answer here is : *Is it possible to make an attenuator using a power splitter/combiner, with an attenuator pad at one of the output ports* ?
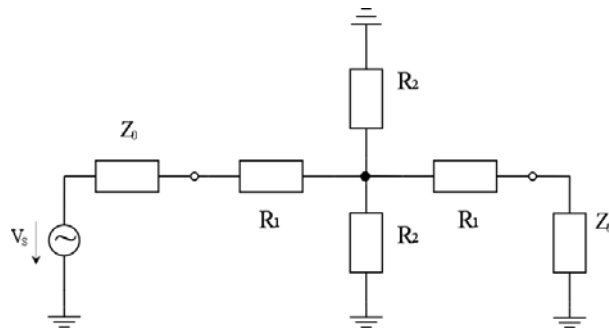
Figure E.8: T- Attenuator pad

The answer is yes and is detailed in Section E.3.

Conclusion

Case 1: As the resistors are interchangeable, there is no possibility to build an attenuator using power splitter with different attenuation for each port. The simple power splitter is always symmetric.

Case 2: It shows that the only possibility is the case where the impedance line is equal to zero ($Z_0 = 0\Omega$). It is not possible to build an asymmetric power splitter.

Case 3: Same conclusion as in the Case 2, as the same conditions on Z_0 ($Z_0 = 0\Omega$) are found.

Case 4: One can obtain a signal attenuated using an attenuator pad. Knowing the gain of the attenuator pad, one can approach this value using different values of resistances calculated with formulas that are found in Section. Using values of the known resistances, the attenuation wanted could be approached, as seen in Section E.3.

E.3   Cross Attenuator

This section describes the cross attenuating pad. The cross attenuating pad equations are described in detail and a design methodology is given for obtaining the desired attenuation with the available components values. The cross attenuator is shown in Figure E.9 and has two independent component values, R_1 and R_2.
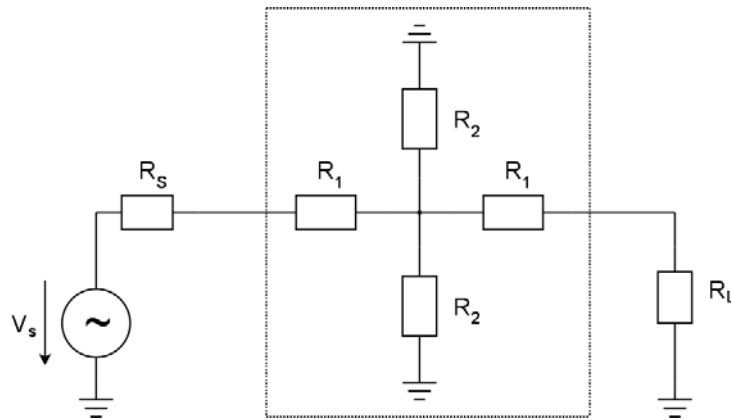
Figure E.9: The topology of the cross attenuator

Since the pad topology is symmetric, the impedances seen on both sides are the same; this means that the cross attenuator cannot be matched if both source and load impedances values are not equal. This means that this topology cannot be used for coupling circuits that have different characteristic impedance; in this work, however, it is not a limitation because all circuits are matched to 50 Ω. For further calculations, let :

$$Z_0 \overset{def.}{=} R_S = R_L$$

In order to simplify calculations and to avoid heavy notations, we define the equivalent resistance Z' as shown in Figure E.10.
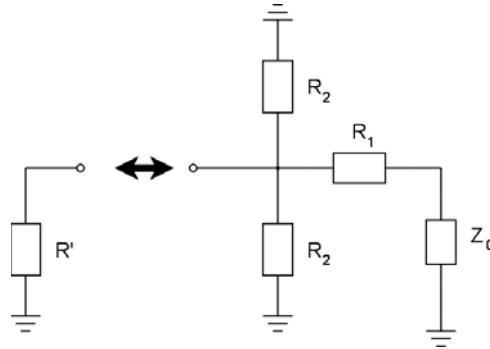

Figure E.10: The equivalent resistance R'

This gives the expression:

$$Z' = (Z_0 + R_1) \parallel \frac{R_2}{2} = \frac{Z_0 R_2 + R_1 R_2}{2Z_0 + 2R_1 + R_2}$$

E.3.1   Calculation of R_2 with R_1 known in order to match Z_0

Considering what was said previously, the impedance is matched when the total impedance seen from the pad is equal to Z_0, as shown in Figure E.11
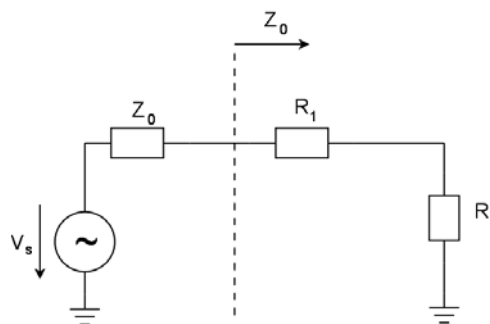
Figure E.11: The impedance matching condition

In other words, we need to have :

$$Z_0 = Z_{\text{in}} = R_1 + Z'$$

By replacing with the equivalent expression of Z_0 given previously, we get :

$$Z_0 = R_1 + \frac{Z_0 R_2 + R_1 R_2}{2Z_0 + 2R_1 + R_2}$$

By multiplying the expression with the denominator, we have :

$$2Z_0^2 + 2Z_0 R_1 + Z_0 R_2 = 2Z_0 R_1 + 2R_1^2 + R_1 R_2 + Z_0 R_2 + R_1 R_2$$

We simplify :

$$2Z_0^2 + 2Z_0 R_1 + Z_0 R_2 = 2Z_0 R_1 + 2R_1^2 + R_1 R_2 + Z_0 R_2 + R_1 R_2$$

We thus get :

$$2Z_0^2 = 2R_1^2 + 2R_1 R_2$$

By dividing by 2 and rearranging the terms, we get :

$$R_1 R_2 = Z_0^2 - R_1^2$$

Finally, we get :

$$R_2 = \frac{Z_0^2 - R_1^2}{R_1}$$

E.3.2   Calculation of the attenuation

For calculating the attenuation, we consider the current and voltage definitions in the pad circuit shown in Figure E.12.
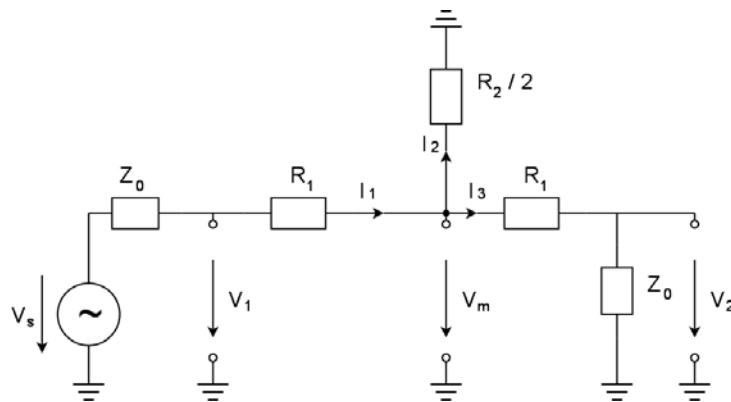
Figure E.12: The attenuating pad currents and voltages

Calculation of V_2

The equation for currents gives : $I_1 = I_2 + I_3$ By calculating currents with Kirchhoff's law on each resistor, we get :

$$\frac{V_1 - V_m}{R_1} = \frac{V_m - V_2}{R_1} + \frac{V_m}{R_2/2}$$

We split the fractions :

$$\frac{V_1}{R_1} - \frac{V_m}{R_1} = \frac{V_m}{R_1} - \frac{V_2}{R_1} + \frac{2V_m}{R_2}$$

We rearrange the terms :

$$\frac{V_2}{R_1} = \frac{2V_m}{R_1} + \frac{2V_m}{R_2} - \frac{V_1}{R_1}$$

We can thus express V_2 with the other variables:

$$V_2 = 2V_m + 2V_m \cdot \frac{R_1}{R_2} - V_1$$

After simplifying, we get :

$$V_2 = 2V_m \left(1 + \frac{R_1}{R_2}\right) - V_1 = 2V_m \left(\frac{R_1 + R_2}{R_2}\right) - V_1$$

Calculation of V_m

We express V_m with respect to V_1 (it is a resistive divider) and we use the expression for R_1 obtained previously :

$$V_m = V_1 \frac{Z'}{R_1 + Z'} = V_1 \cdot \frac{\frac{Z_0 R_2 + R_1 R_2}{2Z_0 + 2R_1 + R_2}}{R_1 + \frac{Z_0 R_2 + R_1 R_2}{2Z_0 + 2R_1 + R_2}} = V_1 \cdot \frac{Z_0 R_2 + R_1 R_2}{Z_0 R_2 + 2R_1 R_2 + 2Z_0 R_1 + 2R_1^2}$$

By replacing the value of V_m by the one obtained above, we get :

$$V_2 = 2 \cdot V_1 \cdot \frac{Z_0 R_2 + R_1 R_2}{Z_0 R_2 + 2R_1 R_2 + 2Z_0 R_1 + 2R_1^2} \cdot \left(\frac{R_1 + R_2}{R_2}\right) - V_1$$

Calculation of the gain

The gain A of the attenuating pad is given below (V_2 is divided by V_1) :

$$A = \frac{V_2}{V_1} = 2 \cdot \frac{Z_0 R_2 + R_1 R_2}{Z_0 R_2 + 2R_1 R_2 + 2Z_0 R_1 + 2R_1^2} \cdot \left(\frac{R_1 + R_2}{R_2}\right) - 1$$

We multiply both fractions :

$$A = \frac{2Z_0 R_1 R_2 + 2R_1^2 R_2 + 2Z_0 R_2^2 + 2R_1 R_2^2}{Z_0 R_2^2 + 2R_1 R_2^2 + 2Z_0 R_1 R_2 + 2R_1^2 R_2} - 1$$

We calculate the resulting fraction and simplify its terms :

$$A = \frac{2Z_0 R_1 R_2 + 2R_1^2 R_2 + 2Z_0 R_2^2 + 2R_1 R_2^2 - Z_0 R_2^2 - 2R_1 R_2^2 - 2Z_0 R_1 R_2 - 2R_1^2 R_2}{Z_0 R_2^2 + 2R_1 R_2^2 + 2Z_0 R_1 R_2 + 2R_1^2 R_2}$$

$$A = \frac{Z_0 R_2^2}{Z_0 R_2^2 + 2R_1 R_2^2 + 2Z_0 R_1 R_2 + 2R_1^2 R_2} = \frac{Z_0 R_2}{Z_0 R_2 + 2R_1 R_2 + 2Z_0 R_1 + 2R_1^2}$$

$$A = \frac{1}{1 + \frac{2R_1 R_2 + 2Z_0 R_1 + 2R_1^2}{Z_0 R_2}}$$

We finally obtain the expression of the gain :

$$A = \frac{1}{1 + \frac{2R_1}{Z_0 R_2} \cdot (Z_0 + R_1 + R_2)}$$

E.3.3 Design methodology

The methodology to calculate the values of R_1 and R_2 is straightforward.

- choose a normalized value for R_1, where $0 < R_1 < Z_0$;

- calculate the corresponding R_2 by applying the formala : $R_2 = \frac{(Z_0^2 - R_1^2)}{R_1}$

- round (if required) the value of R_2 to the nearest normalized value (this rounded value of R_2 is noted R_2');

- calculate the corresponding gain by applying the formala : $G = \frac{1}{1 + 2\frac{R_1}{(Z_0 R_2)} \cdot (Z_0 + R_1 + R_2)}$

- the gain can be coarsely tuned by choosing another value for R_1;

- the gain can be finely tuned by rounding R_2 to the other possible normalized value when the calculated R_2 falls equally between two normalized values.

The values obtained by applying this methodology are summarized in the following tables for a characteristic impedance Z_0 equal to 50Ω. Table E.2 shows the values obtained by choosing R_1 first while Table E.3 shows the values obtained when R_2 is chosen first.

R_1 [Ω]	R_2 [Ω]	R_2' [Ω]	G'	G' [dB]
10	240	240	0.667	-3.522
11	216.2727	220	0.640	-3.874
12	196.3333	200	0.614	-4.237
13	179.3077	180	0.588	-4.619
15	151.6667	150	0.538	-5.390
16	140.25	150	0.520	-5.673
18	120.8889	120	0.470	-6.559
20	105.000	100	0.4237	-7.458
		110	0.4331	-7.269
22	91.636	91	0.388	-8.220
24	80.167	82	0.354	-9.025
27	65.593	68	0.303	-10.378
30	53.333	51	0.245	-12.248
33	42.758	43	0.205	-13.747
36	33.444	33	0.162	-15.838
39	25.103	24	0.120	-18.429
43	15.140	15	0.075	-22.532
47	6.192	10	0.047	-26.492

Table E.2: Resistance values of the attenuator pad when R_1 is a normalized-valued resistor and R_2 is calculated accordingly. We assume $Z_0 = 50\Omega$

The choice of the resistances' value has an impact on the gain. As the resistances has normalized values, it is essential to take into account the small error caused by the rounding. In case the value of the resistances R_2 is known, the value of resistance R1 is given by :

$$R_1 = \frac{(R_2 \pm \sqrt{R_2^2 + 4Z_0^2})}{2}$$

As the expression inside the square root is always larger than R_2, only the positive solution has a physical meaning. Table E.3 shows the value of the resistances R_1, knowing the value of R_2. The comparison between Tables E.2 and E.3 shows that choosing one resistance first or

the other has a small impact on the impedance mismatch. In practice, it is obviously easier to choose R_1 first from normalized values and calculate R_2 accordingly and rounding the obtained value to the nearest normalized value.

R2' [Ω]	R1' [Ω]	R1 [Ω]	G'	G' [dB]
240	10.000	10.000	0.667	-3.522
220	10.831	11.000	0.640	-3.874
200	11.803	12.000	0.614	-4.237
180	12.956	13.000	0.588	-4.619
150	15.139	15.000	0.538	-5.390
150	15.139	15.000	0.520	-5.673
120	18.103	18.000	0.477	-6.430
100	19.3303	20.000	0.4237	-7.4582
110	20.7107	20.000	0.4331	-7.2688
91	22.104	22.000	0.388	-8.220
82	23.661	24.000	0.354	-9.025
68	26.465	27.000	0.303	-10.378
51	30.627	30.000	0.245	-12.248
43	32.927	33.000	0.205	-13.747
33	36.152	36.000	0.162	-15.838
24	39.420	39.000	0.120	-18.429
15	43.059	43.000	0.075	-22.532
10	45.249	47.000	0.047	-26.492

Table E.3: Resistance values of the attenuator pad when R_2 is a normalized-valued resistor and R_1 is calculated accordingly. We assume $Z_0 = 50\Omega$

E.3.4 Conclusion

The study of resistive networks illustrated several ways to implement simple circuits made only with resistances: the power splitter/combiner and the cross attenuator pad. It shows that it is not possible to make power splitters or power combiners with resistances that have different values and it also shows that the resistances R_1 and R_2 of the cross attenuator pad could be determined in order to reach accurately the needed attenuation. All topologies studied here with resistive

network are made by assuming an impedance matching on 50Ω but they can be design with any another value for Z_0.

Chapter F

Components market exploration

This appendix gives the details about the market exploration that was made for finding and choosing the components for the oscillator and the I/Q demodulator devices. It is given as a help for anyone who needs to design and build a similar UWB testbed but with other specifications.

F.1   The oscillator components

This section presents the component selection process of the oscillator circuit described in chapter 5. The most effective way to do a market search about the possible best elements to use in this circuit, is first to look for the PLL synthesizer, and/or VCO available in market which satisfy the design specifications. Then, we compare them together and choose the suitable ones for our local oscillator.

F.1.1   PLL synthesizer

The PLL synthesizers we found in market (in 2009) that best suits our specifications are listed in table F.1

PLL chip	characteristics	conclusion
AD4156 Analog Device	• RFin_max = 6000MHz • Vcc = 2.7/3.3 V • Icc_max = 32mA • Pin = -20dBm at 4.2GHz	• Low power supply • High current supply • High input power sensitivity
LMX2434 National Semiconductor	• RFin_max = 5000MHz • Vcc = 2.5V • Icc_RF_max = 6.2mA • Icc_IF_max = 3.5 mA • Pin_RF = -12dBm	• Low power supply • Low current supply • High input power sensitivity
LMX2486 National Semiconductor	• RFin_max = 4500MHz • Vcc = 3V • Icc_total = 8.4mA • Pin_RF = -15dBm	• Low power supply • Low current supply • High input power sensitivity
PSA4202C Z-Communication	• RF = 4144-4260MHz • Vcc = 5V • Icc = 26mA • Pout = 0 ±3dBm	• Suitable power supply • High current supply • Low output power
PSA4260C-LF Z-Communication	• RF = 4260MHz • Vcc = 5V • Icc = 34mA • Pout = 3 ±2dBm	• Suitable frequency range • Suitable power supply • High current consumption • Low output power

Table F.1: Potential PLL synthesizers

The PLL synthesizers we consider are highlighted in red. The first two, indeed, work in the desired frequency range with a low current consumption while the last one consumes a lot of current because it includes a whole PLL synthesizer and a VCO on the same chip. This explains why its current consumption is high, as shown in Table F.1; the other devices, however, contain only a PLL synthesizer.

F.1.2 VCO

As shown in table F.2, the best candidates as VCO are highlighted in red. They all have a high current consumption but these ones have the lowest power consumption in comparison with the others for similar performance.

VCO chip	characteristics	conclusion
CRO4250A-LF Z-Communication	• RF = 4225-4275MHz • Vcc = 5V • Icc = 28mA • Pout = 5 ±3dBm	• Suitable frequency range • Suitable power supply • High current supply • Low output power
HMC391LP4 Hittite	• RF = 3.9-4.45GHz • Vcc = 3V • Icc = 30mA • Pout = 5dBm	• Suitable frequency range • Low power supply • High current supply • Low output power
HMC586LC4B Hittite	• RF = 4-8GHz • Vcc = 5V • Icc_max = 75mA • Pout_max = 5dBm	• High frequency range • Suitable power supply • Very high current supply • Low output power
HMC-C028 Hittite	• RF = 4-8GHz • Vcc = 12V • Icc = 185mA • Pout = 20dBm	• High frequency range • Very high power supply • Very high current supply • High output power
V910ME02 Z-Communication	• RF = 4245-4335MHz • Vcc = 5V • Icc = 16mA • V_tune = 4V @ 4.25GHz • Pout = 0.5 ±2.5dBm	• Suitable frequency range • Suitable power supply • Low current supply • Low output power • Suitable tuning voltage
V910ME05 Z-Communication	• RF = 4020-4330 MHz • Vcc = 5V • Icc = 26mA • V_tune = 7V @ 4.25GHz • Pout = 1 ±3dBm	• Suitable frequency range • Suitable power supply • High current supply • High tuning voltage • Low output power

V910ME13-LF Z-Communication	• RF = 4200-4400 MHz • Vcc = 5V • Icc = 26mA • V_tune = 5.5V @ 4.25GHz • Pout = 0.5 ±3.5dBm	• Suitable frequency range • Suitable power supply • High current supply • High tuning voltage • Low output power
V910ME15 Z-Communication	• RF = 4020-4330MHz • Vcc = 5V • Icc = 21mA • V_tune = 6.5V @ 4.25GHz • Pout = 2 ±3dBm	• Suitable frequency range • Suitable power supply • High current supply • High tuning voltage • Low output power
V910ME16 Z-Communication	• RF = 3990-4490MHz • Vcc = 5V • Icc = 20mA • V_tune = 5V @ 4.25GHz • Pout = 2.5 ±2.5dBm	• Suitable frequency range • Suitable power supply • High current supply • Suitable tuning voltage • Low output power
V910ME20 Z-Communication	• RF = 3920-4520MHz • Vcc = 5V • Icc = 27mA • V_tune = 4V @ 4.25GHz • Pout = 4 ±3dBm	• Suitable frequency range • Suitable power supply • High current supply • Suitable tuning voltage • Low output power
V950ME09-LF Z-Communication	• RF = 4200-5000MHz • Vcc = 12V • Icc = 54mA • V_tune = 1.75V @ 4.25GHz • Pout = 12.5 ±2.5dBm	• Suitable frequency range • Very high power supply • High current supply • Low tuning voltage • High output power

Table F.2: Potential VCO elements

F.1.3 PLL synthesizer-VCO

The Tables F.3, F.4 and F.5 compare the PLL and the VCO chips retained previously. Afterwards, we decide which chips are used for the final PLL synthesizer.

PLL CHIP	VCO CHIP	REMARKS

AD4156
• Vcc = 2.7-3.3V
• Icc_max = 32mA
• VcpoutRF = 4.5V
	CRO4250A-LF
	• Vcc = 5V
	• Icc = 28mA
	• V_tuning = 3V
	• P_{out} = 6.8 dBm
	   @ 3V
		• I_tot = 60mA →
		  High current consumption
		• No voltage amplifier
		• Suitable output power

	HMC391LP4
	• Vcc = 3V
	• Icc = 30mA
	• V_tuning = 4.25V
	• P_{out} = 5.25 dBm
	   @ 4.25V
		• I_tot = 62mA →
		  High current consumption
		• No voltage amplifier
		• Suitable output power

	HMC586LC4B
	• Vcc = 5V
	• Icc_max= 75mA
	• V_tuning = 2V
	• P_{out} = 4 dBm
	   @ 2V
		• I_tot = 107mA →
		  Very high current consumption
		• No voltage amplifier
		• Small output power

Table F.3: Comparing AD156 PLL synthesizer with potentials VCO

PLL CHIP	VCO CHIP	REMARKS

LMX2434
• Vcc = 2.5V
• Icc_max = 6.2mA
• VcpoutRF = 2.5V
• Pin_RF = -12dBm
	CRO4250A-LF
	• Vcc = 5V
	• Icc = 28mA
	• V_tuning = 3V
	• Pout = 6.8dBm
	   @ 4.25Ghz
		• I_tot = 34.2mA
		• V_tuning > VcpoutRF →
		   Not enough charge pump voltage, we need a voltage amplifier

	HMC391LP4
	• Vcc = 5V
	• Icc = 30mA
	• V_tuning = 4.25V
	• Pout = 5.25dBm
	   @ 4.25V
		• I_tot = 34.6mA
		• V_tuning > VcpoutRF →
		   voltage amplifier

	HMC586LC4B • Vcc = 5V • Icc_max = 75mA • V_tuning = 2V • Pout = 4dBm @ 2V	• I_tot = 81.2mA • V_tuning < VcpoutRF → No voltage amplifier • Small output power
	V910ME13-LF • Vcc = 5V • Icc = 26mA • V_tuning = 5.5V • Pout = 3dBm @ 5.5V	• I_tot = 32.2mA • V_tuning > VcpoutRF → voltage amplifier • Small output power
	V910ME16 • Vcc = 5V • Icc = 20mA • V_tuning = 5V • Pout = 2dBm @ 5V	• I_tot = 26.2mA • V_tuning > VcpoutRF → voltage amplifier • Small output power
	V910ME20 • Vcc = 5V • Icc = 27mA • V_tuning = 4V • Pout = 5.5dBm@ 4V	• I_tot = 33.2mA • V_tuning > VcpoutRF → voltage amplifier • Suitable output power

Table F.4: Comparing LMX2434 PLL synthesizer with potential VCOs

PLL CHIP	VCO CHIP	REMARKS

LMX2486
 	
• Vcc = 3V
• Icc = 5.7mA
• VcpoutRF = 3V
	CRO4250A-LF
	  • Vcc = 5V
	  • Icc = 28mA
	  • V_tuning = 3V
	  • Pout = 6.8dBm @ 3V
		• I_tot = 33.5mA
		• voltage amplifier not needed
		• Suitable output power

	HMC391LP4
	  • Vcc = 3V
	  • Icc = 30mA
	  • V_tuning = 4.25V
	  • Pout = 5.25dBm @ 4.25V
		• I_tot = 35.7mA
		• High tuning voltage
		  → voltage amplifier
		• Suitable output power

	HMC586LC4B
	  • Vcc = 5V
	  • Icc_max = 75mA
	  • V_tuning = 2V
	  • Pout = 4dBm @ 2V
		• I_tot = 80.5mA (high)
		• Low tuning voltage
		  → No voltage amplifier
		• Small output power

	V910ME13-LF
	  • Vcc = 5V
	  • Icc = 26mA
	  • V_tuning = 5.5V
	  • Pout = 3dBm @ 5.5V
		• I_tot = 31.7mA
		• High tuning voltage
		  → voltage amplifier
		• Small output power

	V910ME16
	  • Vcc = 5V
	  • Icc = 20mA
	  • V_tuning = 5V
	  • Pout = 2dBm @ 5 V
		• I_tot = 25.7mA (low)
		• High tuning voltage
		  → voltage amplifier
		• Small output power

	V910ME20
	  • Vcc = 5V
	  • Icc = 27mA
	  • V_tuning = 4V
	  • Pout = 5.5dBm @ 4V
		• I_tot = 32.7mA
		• High tuning voltage
		  → voltage amplifier
		• Suitable output power

Table F.5: Comparing LMX2486 PLL synthesizer with potential VCOs

Choosing the best components requires further considerations because, when an element matches some conditions, it does not necessarily fulfil the others. For this reason, we list below the most important criteria by decreasing order of importance for choosing the best devices in a rational way:

- Range frequency

- Less current consumption

- Small V_tuning of the VCO chip

- High output power

Following these criteria, the elements presented in Table F.3 are discarded because of the high current consumption, which is the highest one in the table. Applying the criteria to Table F.4, the best choice is the pair LMX2434-CRO4250A-LF. Actually, this choice offers a good output power with a low current consumption, even if it uses a voltage amplifier to reach the appropriate V_tuning to drive the VCO chip. For instance, if V910ME16 is chosen as a VCO chip, the whole circuit will consume less current, but a powerful voltage amplifier is needed to obtain the desired V_tuning for generating the output frequency, as well as another powerful output amplifier is needed to increase the output power which is very low for our needs. However, CRO4230A-LF also uses voltage and power amplifiers, but is less powerful than the ones used for V910ME16, having thus less power consumption. In Table F.5, the best choice is the pair LMX2486-CRO4250A-LF. Indeed, this pair offers the best performance in current consumption, V_tuning and output power. The others pairs, however, have high current consumption (HMC586LC4B), or smaller output power (V910ME16) or higher V_tuning (HMC391LP4).

The last possible candidate is already chosen during the market search of the potential PLL synthesizers (table F.1). As said, even if the circuit PSA4260C-LF offers a low output power, it has low current consumption seeing that it includes a PLL synthesizer and a VCO in the same chip. Furthermore, it works at the exact frequency range ideal for the local oscillator. In consequence, after this exhaustive comparison, the possible circuits are listed below in order of preference:

- Choice n⁰ 1: LMX2434, CRO4250A-LF.

- Choice n⁰ 2: LMX2486, CRO4250A-LF.

- Choice nº 3: PSA4260C-LF.

All these three choices fulfil the requirements concerning the frequency range and have similar current consumption, in consequence, the choice of the best device will depend at this step on output power and V_tuning criterion. As said at the beginning of this section, choices nº 1 and 2 do not satisfy the output power requirement. As a solution, a power amplifier must be used at the output of the system to reach this specification. On the other hand, choice nº 1 does not either offer enough voltage to drive the VCO in order to generate the corresponding output frequency, thus, beside the power amplifier, this choice must also use a voltage amplifier at the input of the VCO device. An overview of the suggested system for choice nº 1 and 2 is shown in figure F.1.
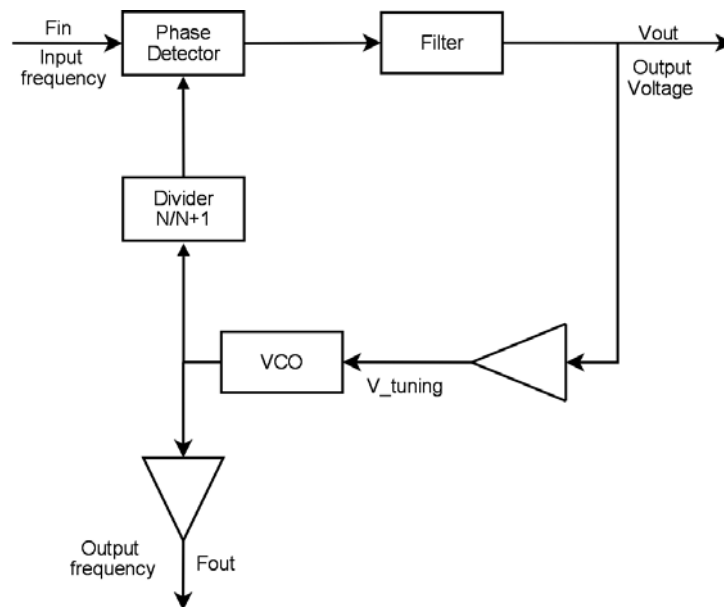
Figure F.1: Overview of the system for choices nº 1 and 2. The input VCO amplifier is used only for choices nº 1 and 2 but not for choice nº 3

Comparing choice nº 1 with choice nº 2, we decide that the best device for this case is choice 2. In fact, it offers a similar output power but without needing a voltage amplifier to generate the desired frequency, thus, we save 1 device, and so, we decrease the current consumption. Concerning the choice nº 3, comparing it with choice nº 2, it looks worst. Actually, even if its current consumption consumes is similar to choice nº 2, it offers 3 dBm less power, compelling to use a more powerful output amplifier, and so much consumption. Nevertheless, the last criterion that leads us to choose the PLL synthesizer PSA4260C-LF is delivering time.

In fact, this device takes six weeks to be delivered from the company Z-Communication. It is also the same time that need the components of choice nº 2 to be delivered, but from different companies, which will take longer than six weeks. In addition, PSA4260C-LF includes the PLL synthesizer and the VCO inside the same chip, as said previously, and offers similar characteristics in consumption, desired frequency and output power, as each pair does, but these characteristics will be more accurate and precise than the ones bring by the first two choices. PSA4260C-LF uses the Analog Devices circuit ADF4106 as frequency synthesizer, and we will follow the instructions given in this datasheet to program conveniently the PLL device.

F.2   The I/Q demodulator components

This section presents the component selection process for the components of the I/Q demodulator described in chapter 9. We show the research made for different mixers, I/Q mixers, and amplifiers available on the market (in 2010) that meet the targeted specifications.

F.2.1   I/Q Mixer

The I/Q demodulator has to down-convert the UWB signal by preserving the I and Q components in order to remove any beat as explained in Section 9.1.2. The I/Q mixer needs to accept a frequency range of 4.25 GHz for the LO and from 4 to 4.50 GHz for the RF signal. On the market, the available circuits we found are **HMC525LC4** and **HMC620LC4** from Hittite Coproration. Their specifications are shown in Table F.6.

I/Q Mixer Devices	Features	Conclusion
HMC525LC4 I/Q Mixer www.hittite.com	• Frequency Range, RF/LO: 4.0 - 8.5GHz • Frequency Range, IF: DC - 3.5GHz • Conversion loss (As IRM): Typically 7.5dB • Image Rejection: 35dB • 1dB Compression : +14dBm • LO to RF Isolation: 45dB • LO to IF Isolation: 20dB • IP3(Input): +23dBm • Amplitude Balance: 0.3dB • Phase balance: 8 deg. • Size: 1.49 x 1.14 x 0.1 mm	• Good frequency range, but it begins just outside the frequency used • High Image Rejection: **35dB** • High LO to RF Isolation: **45dB** • High Input IP3: **+23dBm**

| HMC620LC4 I/Q Mixer www.hittite.com | • Frequency Range, RF/LO: **3.0 - 7.0GHz**

• **Wide IF Bandwidth: DC - 3.5GHz**

• **Conversion loss (As IRM):** Typically **7.5dB**

• **Image Rejection: 27dB**

• **1dB Compression (Input): +12dBm**

• **LO to RF Isolation: 43dB**

• **LO to IF Isolation: 30dB**

• **IP3(Input): +22dBm**

• **Amplitude Balance: 0.1dB**

• **Phase balance: 3Â°**

• **24 Lead Ceramic 4x4 SMT Package: 16mm2** | • It covers the frequency band used

• High Image Rejection

• High LO to RF Isolation

• High Input IP3: **+22dBm** |

Table F.6: I/Q mixers

All the I/Q mixers fulfil the specifications mentioned previously as they cover the desired frequency range and, in particular, they have the same package. Both circuits are difficult to solder as the pins are under the circuits (see Figure F.2). The HMC525LC4 circuit covers the desired frequency range but its input frequency range starts exactly at 4 GHz, which means that both inputs have the same frequency range and this may be too close to the limit. The advantage on the **HMC620LC4** I/Q mixer is that it has a wider RF bandwidth that starts at 3

GHz and which contains safely our working bandwidth. As they cost the same price and are from the same company, we choose the **HMC620LC4** - I/Q Mixer SMT, 3 - 7 GHz which is highlighted in green.

Figure F.2: The LC4 package

F.2.2   Conventional mixer

The conventional mixers have to work in the frequency range of DC to 1 GHz. All selected mixers on the market - highlighted in green - are listed in Table F.7. The first choice was based on mixers which work below 1 GHz; by eliminating the mixers that have small frequency ranges, meaning a range from around DC to 1GHz, the choices have been narrowed down to the following list:

- ADE-2+ / ADE-2

- ADE-2ASK+ / ADE-2ASK [5]

- ADE-2M+

- ADE-R2ASK+ [6]

The circuits **ADE-2+ / ADE-2** and **ADE-2M+** have a high conversion loss, so the **ADE-2ASK+ / ADE-2ASK** and **ADE-R2ASK+** circuits were considered as both of them fulfil the expectations. Therefore the last choice was made on the LO/RF and LO/IF isolation value. The **ADE-R2ASK+** circuit has a little bit higher LO/RF isolation, hence it is chosen for the demodulator.

Product	Features	Observations
ADE-1L+ ADE-1L	- Frequency range: **2 to 500MHz** **LO Power: +3dBm** **RF Power : 50mW** **IF Current : 40mA** **Conversion loss: 5.2dB** **LO/RF isolation: 55dB** **LO/IF isolation: 45dB** **Low profile package**	- Low range frequency - Low RF power consumption - Low consumption current - Low conversion loss - Good isolation - Application: cellular and instrumentation - Price: **$3.95 ea.**
ADE-2+ ADE-2	- Frequency range: **5 to 1000MHz** - LO Power: **7dBm** - RF Power : **50mW** - IF Current : **40mA** - Conversion loss: **6.67dB** - LO/RF isolation: **47dB** - LO/IF isolation: **45dB** - Low profile package	- Enough range frequency - Low RF power consumption - low consumption current - High conversion loss - Good isolation - Application: cellular and PCS - Price: **$ 1.99 ea.**

ADE-2ASK+ ADE-2ASK	- Frequency range: **1 to 1000MHz** **LO Power: 7dBm** **RF Power : 50mW** **IF Current : 40mA** **Conversion loss: 5.4dB** **LO/RF isolation: 45dB** **LO/IF isolation: 32dB** **Low profile package**	- Enough range frequency - low consumption current - Low RF power consumption - Low conversion loss - Good isolation - Application: VSAT systems, instrumentation, cellular - Price: **$ 4.25 ea.**
ADE-2M+	- Frequency range: **5 to 1000MHz** **LO Power: 7dBm** **RF Power : 200mW** **IF Current : 40mA** **Conversion loss: 6.67dB** **LO/RF isolation: 40dB** **LO/IF isolation: 30dB** **Low profile package**	- Enough range frequency - High RF power consumption - Low consumption current - High conversion loss - Good isolation - Application: cellular, GSM, ISM - Price: **$ 2.19 ea.**

ADE-4+ ADE-4	• Frequency range: **200 to 1000GHz** • **LO Power: 7dBm** • **RF Power : 50mW** • **IF Current : 40mA** • **Conversion loss: 6.8dB** • **LO/RF isolation: 53dBm** • **LO/IF isolation: 40dBm** • **Low profile package**	• Low range frequency • Low RF power consumption • low consumption current • High conversion loss • Good isolation • Application: cellular, VHF/UHF, receivers • Price: **$ 4.25 ea.**
ADE-10H ADE-10H+	• Frequency range: **400 to 1000MHz** • **LO Power: 17dBm** • **RF Power : 200mW** • **IF Current : 40mA** • **Conversion loss: 7.0dB** • **LO/RF isolation: 39dB** • **LO/IF isolation: 25dB**	• Low range frequency • High RF power consumption • low consumption current • High conversion loss • Good isolation • Application: cellular, UHF • Price: **$ 7.95 ea.**

ADE-R1+	- Frequency range: **1 to 500MHz** **LO Power: 7dBm** **RF Power : 50mW** **IF Current : 40mA** **Conversion loss: 5.0dB** **LO/RF isolation: 60dB** **LO/IF isolation: 45dB** **www.minicircuits.com Low profile package**	- Low range frequency - Low RF power consumption - low consumption current - Low conversion loss - Good isolation - Application: VHF/UHF - Price: **$ 3.35 ea.**
ADE-R1L+	- Frequency range: **2 to 500MHz** **LO Power: +3dBm** **RF Power : 50mW** **IF Current : 40mA** **Conversion loss: 5.6dB** **LO/RF isolation: 55dB** **LO/IF isolation: 45dB** **Low profile package**	- Low range frequency - Low RF power consumption - low consumption current - Low conversion loss - Good isolation - Application: cellular, instrumentation - Price: **$ 4.35 ea.**

ADE-R1LH+	• Frequency range: **1 to 500MHz** • **LO Power: 10dBm** • **RF Power : 50mW** • **IF Current : 40mA** • **Conversion loss: 5.2dB** • **LO/RF isolation: 60dB** • **LO/IF isolation: 45dB** • **Low profile package**	• Low range frequency • Low RF power consumption • Low consumption current • Low conversion loss • Good isolation • Application: VHF/UHF receivers • Price: **$ 3.39 ea.**
ADE-R2ASK+	• Frequency range: **2 to 1000MHz** • **LO Power level: 7dBm** • **RF Power : 50mW** • **IF Current : 40mA** • **Conversion loss: 5.4dB** • **LO/RF isolation: 48dB** • **LO/IF isolation: 32dB** • **Low profile package**	• Enough range frequency • Low RF power consumption • Low consumption current • Low conversion loss • Good isolation • Application: VSAT systems, instrumentation, cellular • Price: **$ 4.65 ea.**

Table F.7: Mixer devices (all from www.minicircuits.com)

F.2.3   Amplifier

There are many amplifiers available on the market. The choice is based on their frequency range, gain, maximum output power, current consumption and the package. All amplifiers chosen work in a frequency range from DC to 1 GHz. Knowing the signal level that will be sent to the FPGA board, and the signal level needed at the RF input of the I/Q mixer, the amplifiers were chosen according to the budget link of the signal at different points of the circuit. The amplifiers that might be used for the circuits, as well as their characteristics are shown in Table F.8.

Product	*Features*	*Observations*
HMC580ST89 **HMC580ST89E** **www.hittite.com**	• Frequency range: **DC - 1GHz** • Gain: **22dBm** • Output Power for 1dB Compression: **22dBm** • Current consumption: **88mA** • Package: **Industry Standard SOT89** • Single Supply: **+5V**	• Average Gain • High Output Power for 1dB Compression • High Current consumption • Average Single Supply voltage

MAR-8ASM+ **www.minicircuits.com**	• Frequency range: **DC - 1GHz** • Gain: **31.5dBm** • Maximum input power:**+13dB** • Output Power for 1dB Compression: **+12.5dBm** • Current consumption: **65mA** • Device operating voltage: **+3.7V**	• High gain • Average Output Power for 1dB Compression • low current consumption • Low Single Supply • Exact footprint substitute MAR-8SM and MSA-0886
MAR-8SM+ **www.minicircuits.com**	• Frequency range: **DC - 1GHz** • Gain: **32.5dB at f=0.1GHz** , 22.5dB at 1GHz • Maximum input power: **13dBm** • Output Power for 1dB Compression: **12.5dBm** • Maximum current consumption: **65mA** • The package: **Micro-X** • Device operating voltage:**7.8V**	• Exact footprint substitute for Avago's MSA-0886 • High gain • Average Output Power for 1dB Compression • Low current consumption • High operating voltage

MAR-8A+ www.minicircuits.com	• Frequency range: **DC - 1GHz** • Gain: **31.5dB at f=0.1GHz** , 25dB at 1GHz • Output Power for 1dB Compression: **12.5dBm** • Maximum current consumption: **65mA** • The package: **Micro-X** • Device operating voltage:**3.7V**	• High Gain • Average Output Power for 1dB Compression • Low Current consumption • Low operating voltage
MAR-1+ **www.minicircuits.com**	• Frequency range: **DC to 1GHz** • gain: **17.8dB** typically. at 0.1GHz • Output Power for 1dB Compression: **+2.5dBm** • Current consumption: **40mA** • Micro-X package. • Exact foot print substitute for MSA-0185 • Device operating voltage: **+5.0V**	• Low Gain • Low Output Power for 1dB Compression • Low current consumption • Average operating voltage • Unconditionally stable

MAR-1SM+ www.minicircuits.com	• Frequency range: **DC to 1GHz** • Gain: **17.8dB** typically at 0.1GHz • Output Power for 1dB Compression: **2.5dBm** • current consumption : **40mA** • Micro-X package. • Single supply voltage: **+5V** • Unconditionally stable	• Low gain • Low Output Power for 1dB Compression • Low current consumption • Average Single Supply
GALI-74 www.minicircuits.com	• frequency range: **DC-1GHz** • Gain: **25.1dB** • maximum input power: **10dBm** • Output Power for 1dB Compression: **19.2dBm** • Current consumption : **130mA** • The package: **SOT-89** • Single Supply voltage: **4.8V**	• Enough Gain • High Output Power for 1dB Compression • High Current consumption • Average Single Supply

MAR-4+ www.minicircuits.com	• Frequency range: **DC -1GHz** • Gain: **8.3dB at 0.1GHz, 8dB at 1GHz** • Maximum input power: **13dBm** • Output Power for 1dB Compression: **12.5dBm** • Current consumption: **5mA** • The package: **Micro-X** • Unconditionally stable • Operating voltage: **5.25V**	• Low gain • Average Output Power for 1dB Compression • High current consumption: • Average Single Supply
MAR-4SM+ www.minicircuits.com	• Frequency range: **DC -1GHz** • Gain: **8.3dB at 0.1GHz , 8dB at 1GHz** • Maximum input power: **13dBm** • Output Power for 1dB Compression: **12.5dBm** • Current consumption: **5mA** • Device operating voltage: **5.25V** • The package: **Micro-X**	• Exact footprint substitute for MSA-0486 • Low Gain • Average Output Power for 1dB Compression • High current consumption • Average operating voltage

RAM-8+ **www.minicircuits.com**	• Frequency range: **DC -1GHz** • Gain: **32.5dB at f=0.1GHz , 23dB at 1GHz** • Output Power for 1dB Compression: **12.5dBm** • Maximum current consumption: **65mA** • The package: **ceramic surface-mount** • Device operating voltage**: 7.8V**	• High Gain • Average Output Power for 1dB Compression • Low Current consumption • High operating voltage
MAR-6+ **www.minicircuits.com**	• Frequency range: **DC -2GHz** • Gain: **22dB at f=0.1GHz ,** 20dB at 1GHz, 17dB at 2GHz • Maximum input power: **+ 13dBm** • Output Power for 1dBCompression: **+3dBm** • Maximum current consumption: **50mA** • The package: **Micro-X** • Device operating voltage: **3.5V**	• Average gain • Low Output Power for 1dB Compression • Low Current consumption • Low operating voltage

| **RAM-1+** **www.minicircuits.com** | Frequency range: **DC -1GHz** Gain: **19dB** at 0.1GHz , 15.5dB at 1GHz. Maximum input power: **13dBm** Output Power for 1dB Compression: **1.5dBm** Maximum current consumption: **40mA** Package: **ceramic surface-mount** Device operating voltage: **5.0 V** | Average gain Low Output Power for 1dB Compression Low current consumption: Average operating voltage |

Table F.8: Amplifier devices (in green: our choice)

The problem with these circuits is that no one meets all the expectation without a drawback. Hence the choice of the amplifiers is finally made by applying the exclusion principle. The characteristics of the amplifiers that primarily need to be considered are the frequency range and the current consumption. The circuit **MAR-6+** that works from DC to 2 GHz, is eliminated because it adds noise outside our frequency band (DC - 1 GHz). The circuit **GALI-74** needs a lot current compared with other circuits, therefore it is preferable to eliminate it from the list. **MAR-4+** and **MAR-4SM+** have the same characteristics; they are not chosen because of their low gain. **RAM-8+** has not a 50Ω impedances, it is conditionally stable and needs a high operating voltage. Therefore it is eliminated. **RAM-1+** and **HMC580ST89/HMC580ST89E** could be used, but the later is eliminated because of its too high gain and **RAM-1+** is eliminated because of its output power at 1dB compression. In Table F.9, the amplifiers are grouped with respect to their main characteristics. Therefore all amplifiers in the same group have almost the same characteristics but different gains. **MAR-8ASM+**, **MAR-8A+** and **MAR-8SM+** have similar characteristics. The drawback of **MAR-8SM+** is that it has a too large gain and is

more expensive than **MAR-8ASM+** and **MAR-8A+**. Hence the choice is done between **MAR-8ASM+** and **MAR-8A+**. **MAR-8ASM+** amplifier is less expensive than **MAR-8+**, therefore **MAR-8ASM+** (in green in Table F.8) is chosen.

Amplifier groups	Particular characteristics	Characteristics
MAR-8ASM+	- Gain: **31.5dB** - Device operating voltage: **+3.7V** - Thermal resistance: **140 C/W** **Price : $1.17 ea. QTY. (30)**	- Frequency range : DC - 1GHz - Output Power for 1dB Compression: 12.5dBm - Maximum current consumption: 65mA - Maximum input power : 13dBm - Thermal resistance : 140 C/W
MAR-8A+	- Gain: **32.5dB** - Device operating voltage:**7.8V** - Price: $1.32 ea. QTY. (30)	same as above

MAR-8SM+	- Gain: **31.5dB** - Device operating voltage:**+3.7V** - Price: **$1.37 ea.** QTY. (30)	same as above
MAR-1+	–	- Frequency range: **DC to 1GHz** **Gain: 17.8dB** **Output Power for 1dB Compression: +2.5dBm** **Current consumption: 40mA** **Device operating voltage: +5.0V**
MAR-1SM+	–	same as above

Table F.9: Amplifiers group

As **MAR-1+** and **MAR-1SM+** have same characteristics, **MAR-1+** (in green in Table F.8) amplifier has been chosen arbitrarily. The choice of these amplifiers allows having an acceptable signal level. Since the exact level of the input signal is not known yet, the **MAR-8ASM+** amplifier with high gain is chosen to amplify the signal coming from the I/Q mixer. Therefore the **MAR-1+** amplifier with a low gain increases strongly the level of the signal before the FPGA board.

Chapter G

Buffers and Switches schematics and layouts for Prototype nº 1

The Appendix gives the detail on the buffers and the switches circuits of the Prototype nº 1 of the integrated UWB transmitter (see Section 12.3).

The layouts are made such that the metal layers dedicated to power supply (M_2 for Vcc and M_1 for ground, as usual) make a natural decoupling capacitor. All the buffers have exactly the same size in order to simplify their placement in the final layout; This size is determined by the biggest buffer that was designed first and all the others follow the same shape template which is progressively modified inside with the decreasing size of the transistors of smaller buffers.

G.1   The buffers

G.1.1   Buffer 2

Figure G.1: The buffer of weight 2 schematic

Figure G.2: The buffer of weight 2 layout
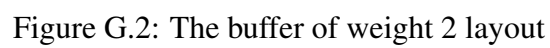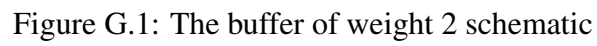
G.1.2   Buffer 3
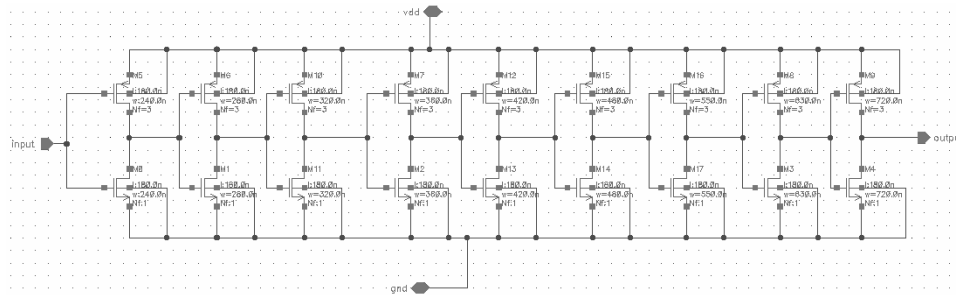
Figure G.3: The buffer of weight 3 schematic
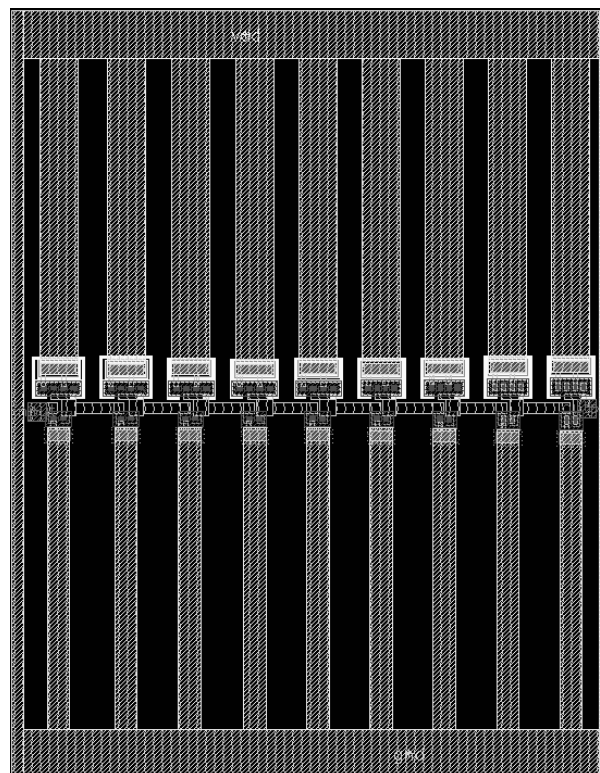
Figure G.4: The buffer of weight 3 layout

G.1.3   Buffer 5
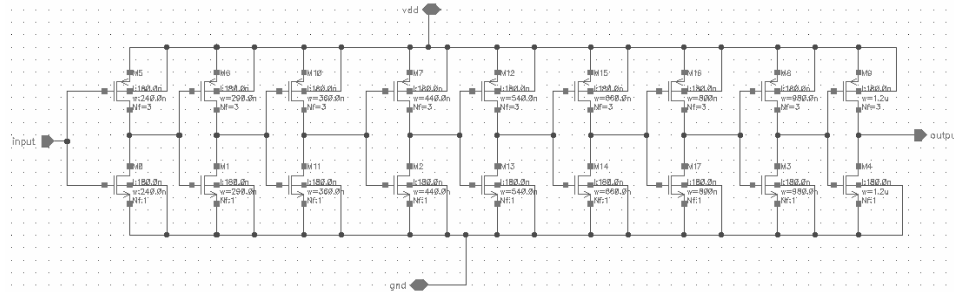
Figure G.5: The buffer of weight 5 schematic
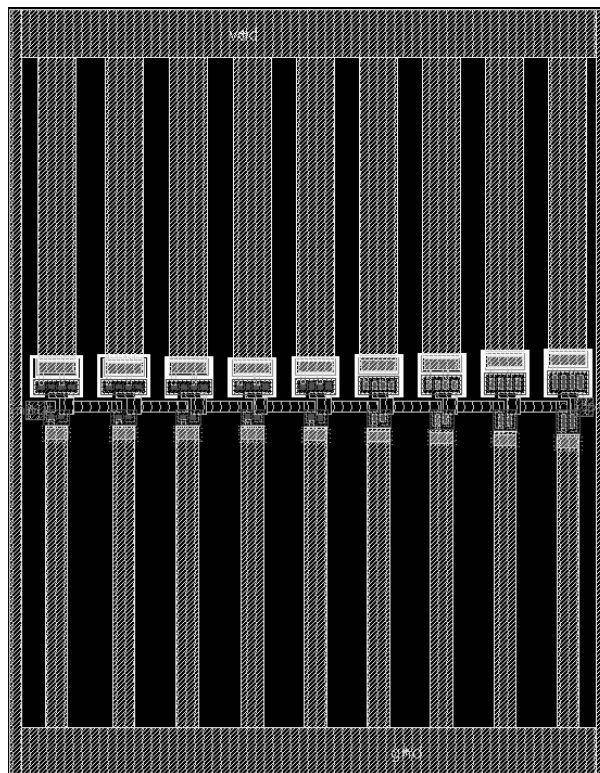
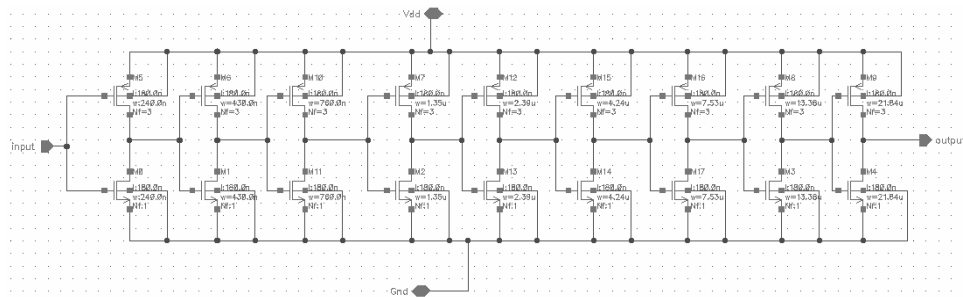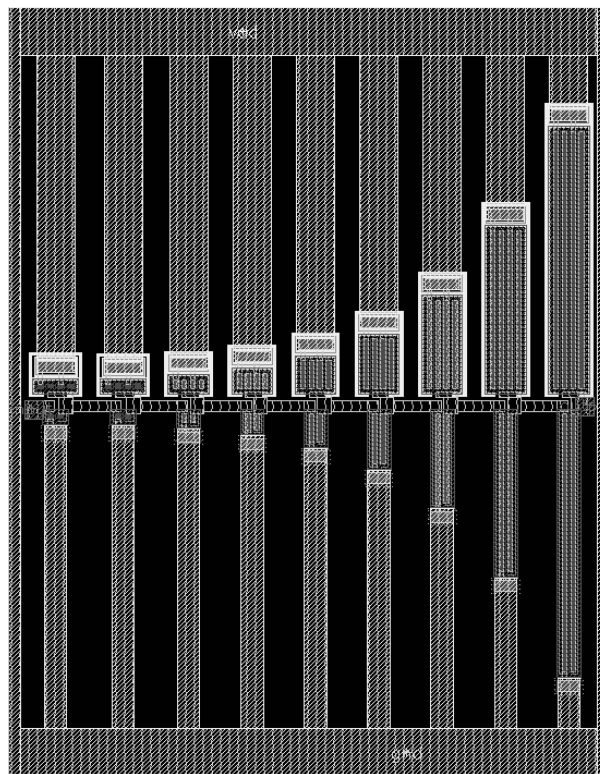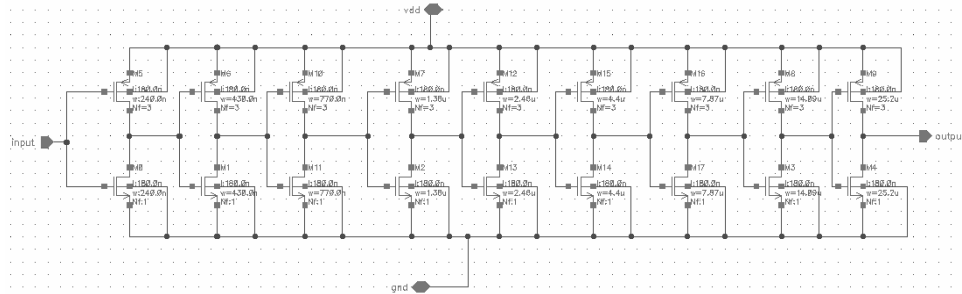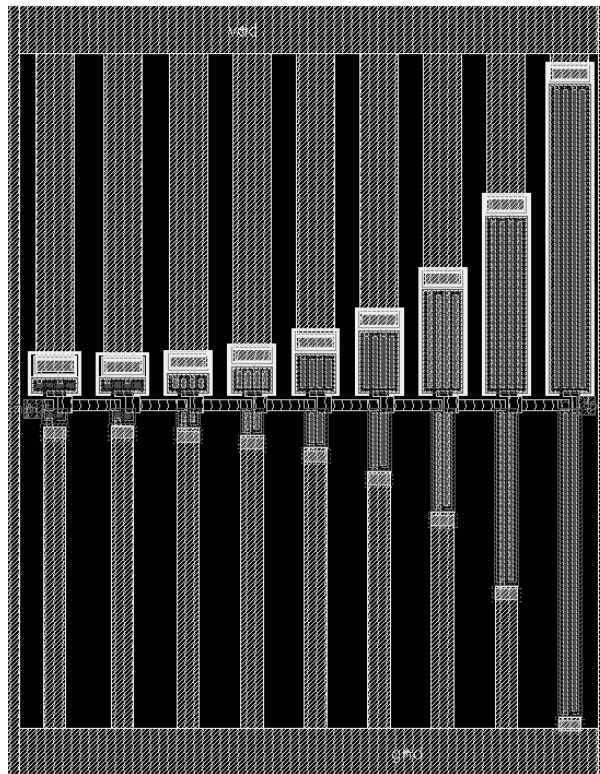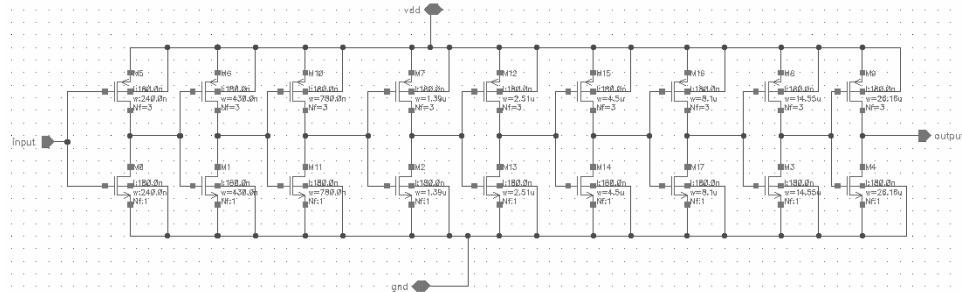Figure G.6: The buffer of weight 5 layout

G.1.4 Buffer 8
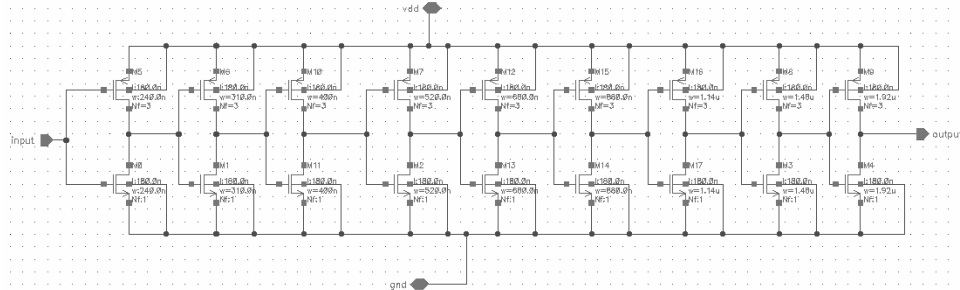
Figure G.7: The buffer of weight 8 schematic
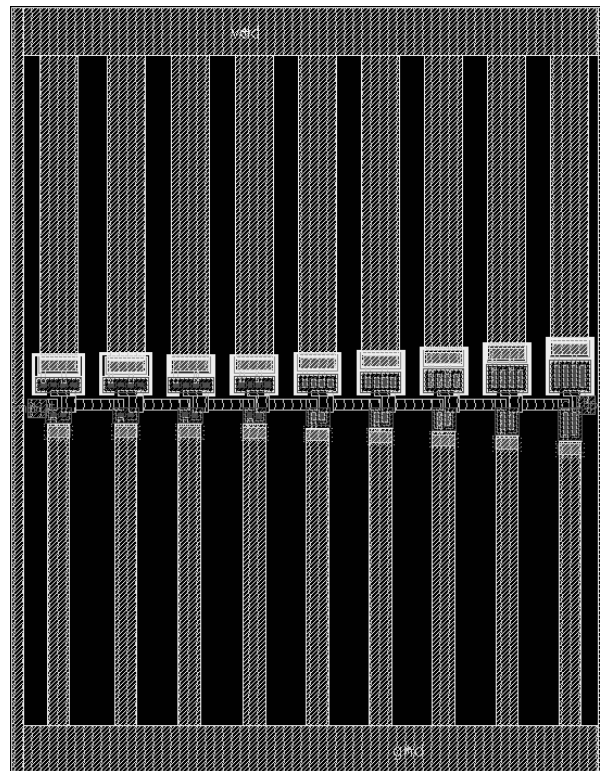
Figure G.8: The buffer of weight 8 layout

G.1.5 Buffer 12
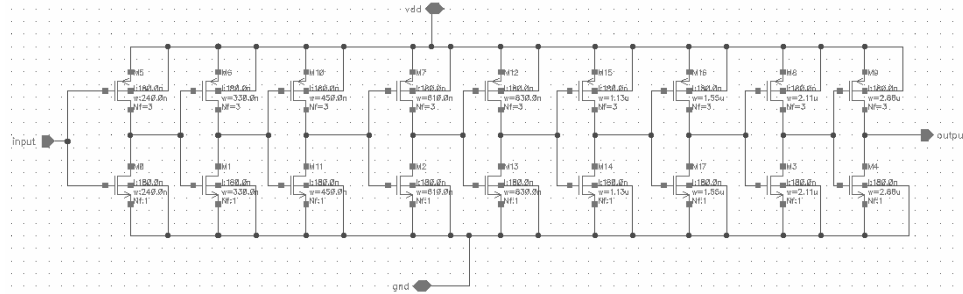
Figure G.9: The buffer of weight 12 schematic
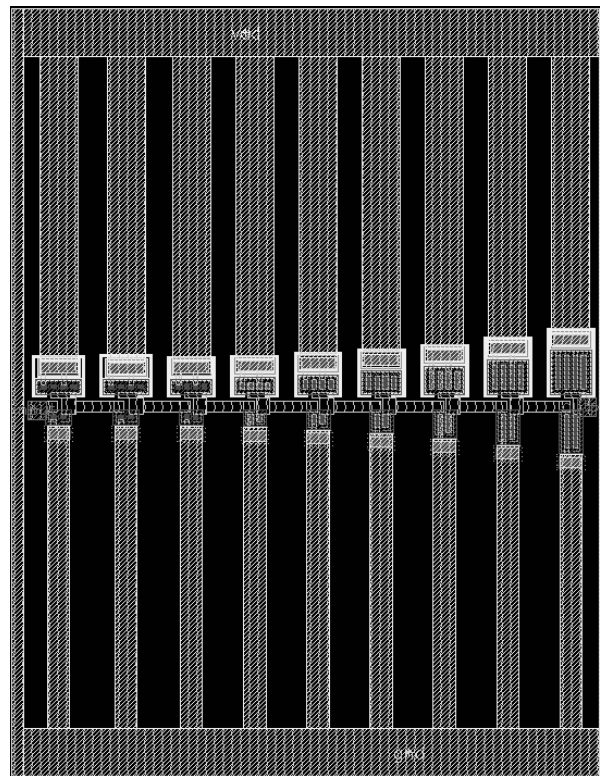
Figure G.10: The buffer of weight 12 layout

G.1.6   Buffer 17
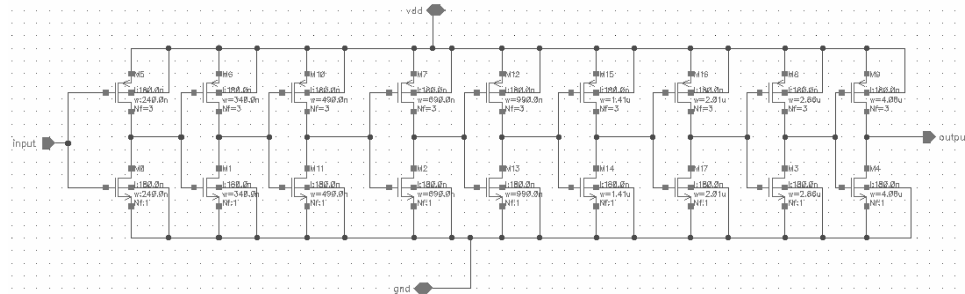

Figure G.11: The buffer of weight 17 schematic
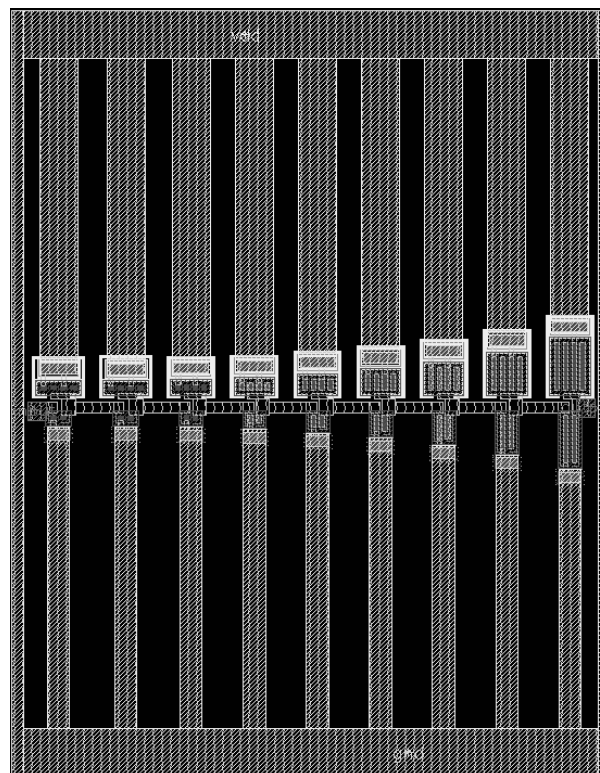
Figure G.12: The buffer of weight 17 layout

G.1.7   Buffer 24
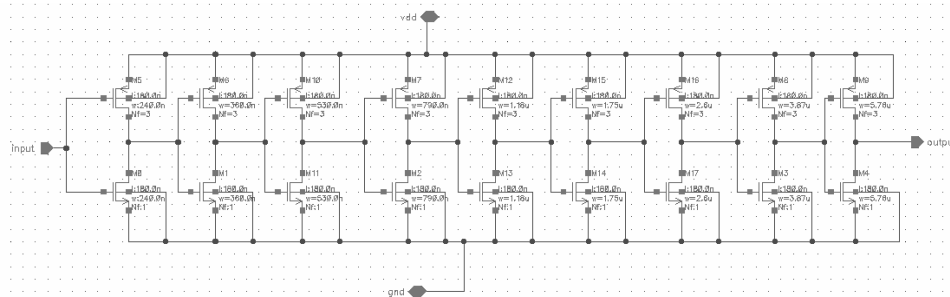
Figure G.13: The buffer of weight 24 schematic
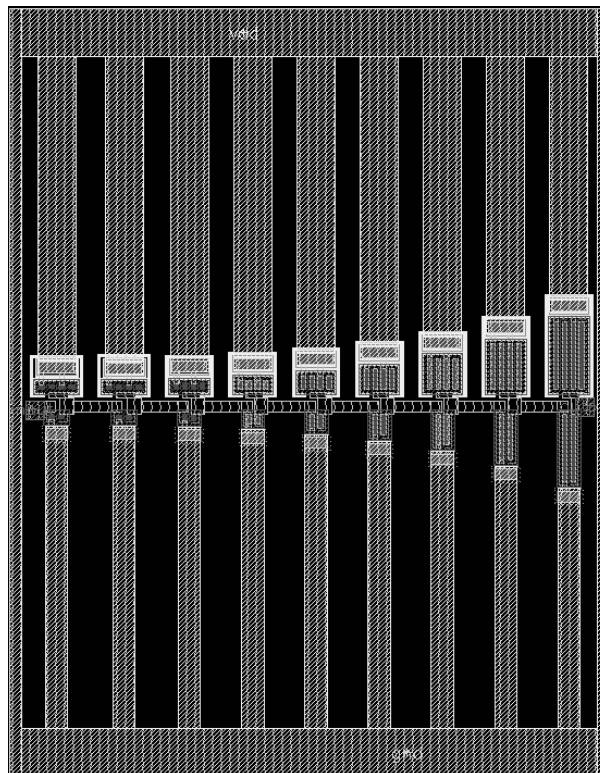
Figure G.14: The buffer of weight 24 layout

G.1.8 Buffer 33
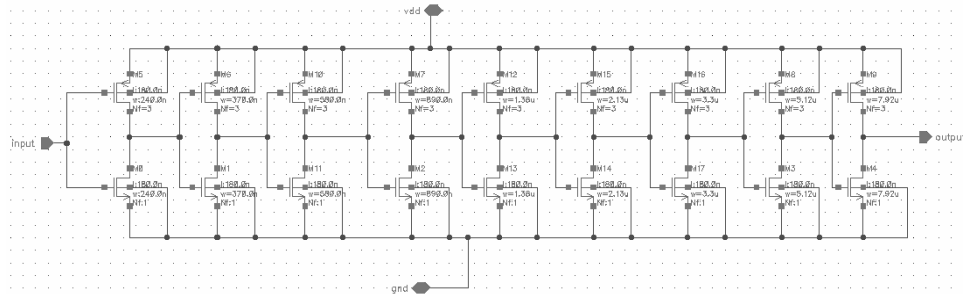
Figure G.15: The buffer of weight 33 schematic
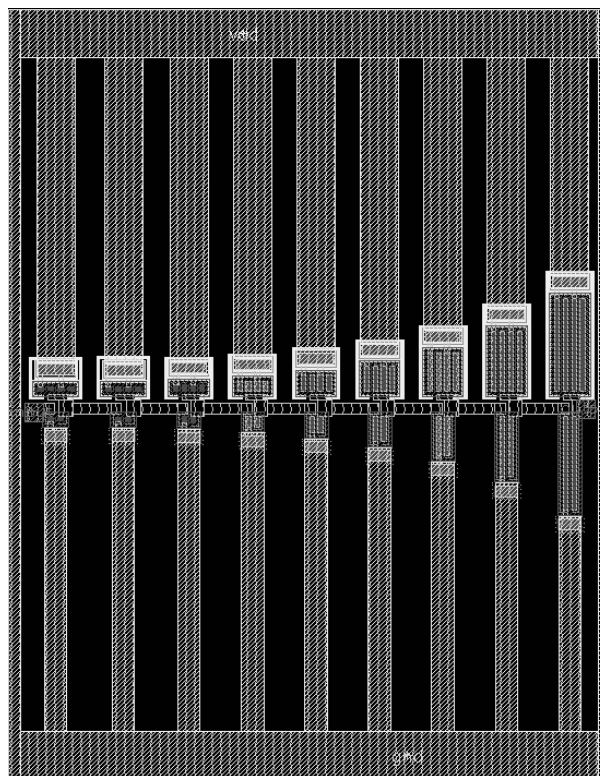
Figure G.16: The buffer of weight 33 layout

G.1.9 Buffer 43
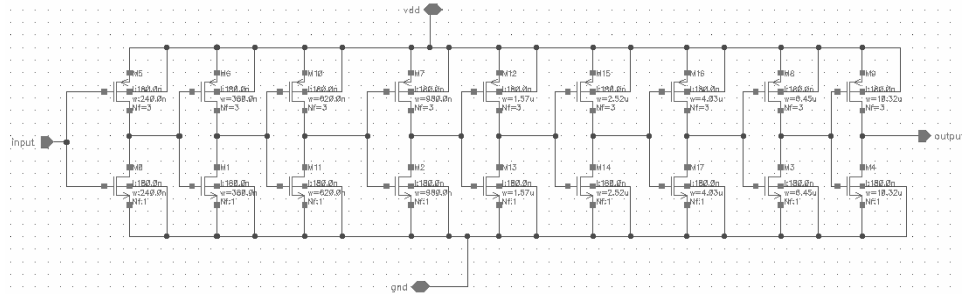
Figure G.17: The buffer of weight 43 schematic
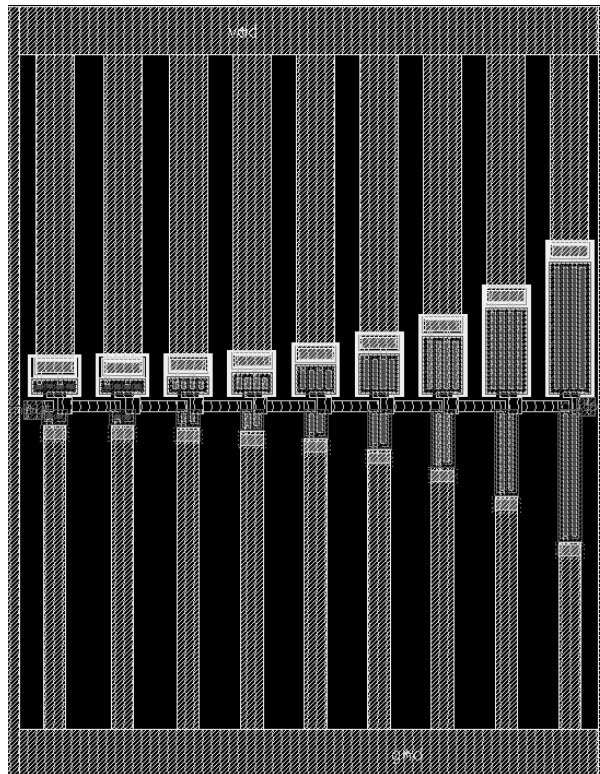
Figure G.18: The buffer of weight 43 layout

G.1.10 Buffer 55
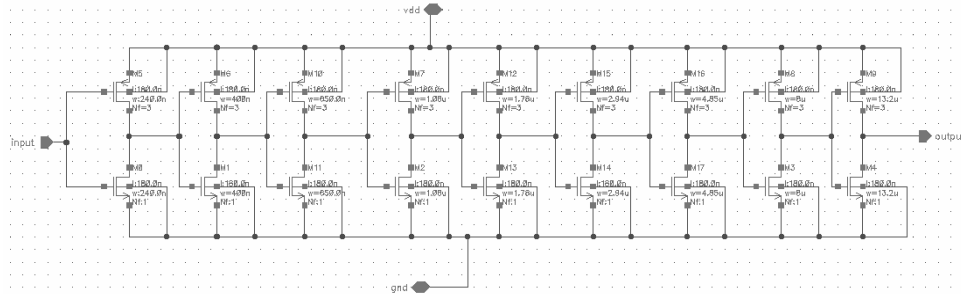
Figure G.19: The buffer of weight 55 schematic
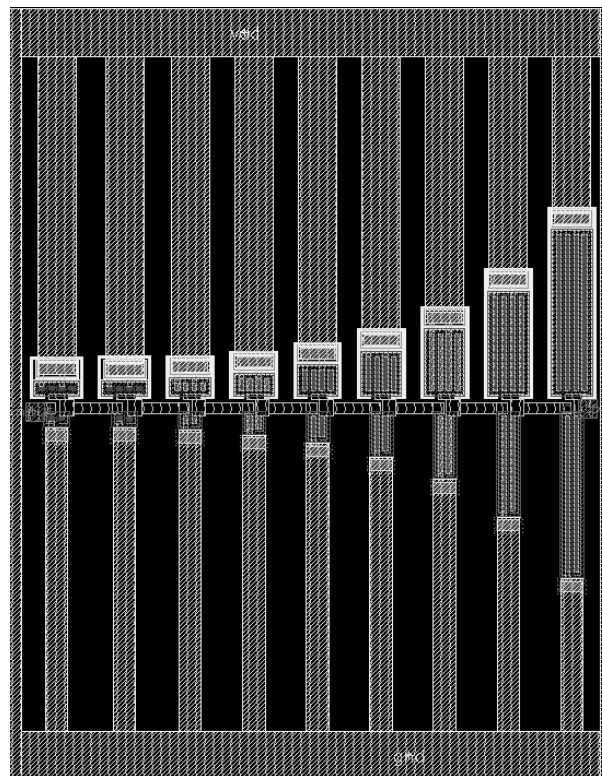
Figure G.20: The buffer of weight 55 layout

G.1.11   Buffer 67
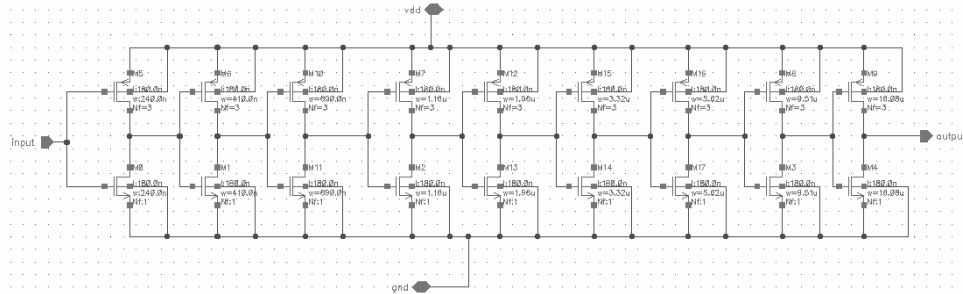
Figure G.21: The buffer of weight 67 schematic
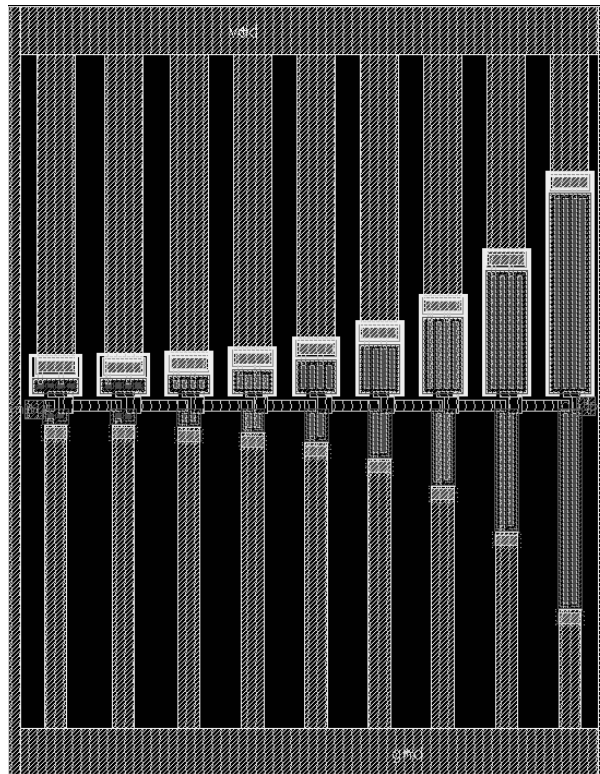
Figure G.22: The buffer of weight 67 layout

G.1.12 Buffer 80
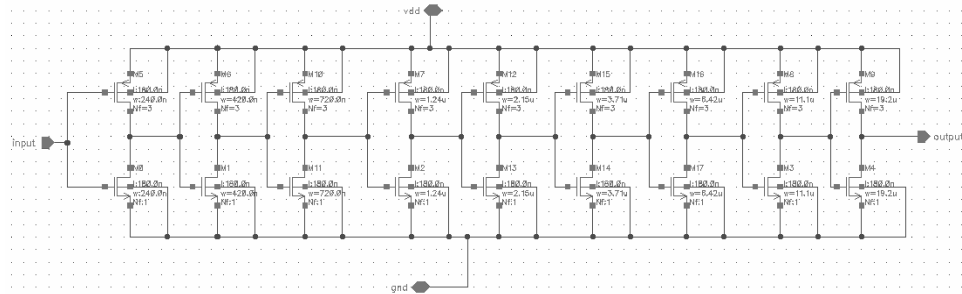
Figure G.23: The buffer of weight 80 schematic
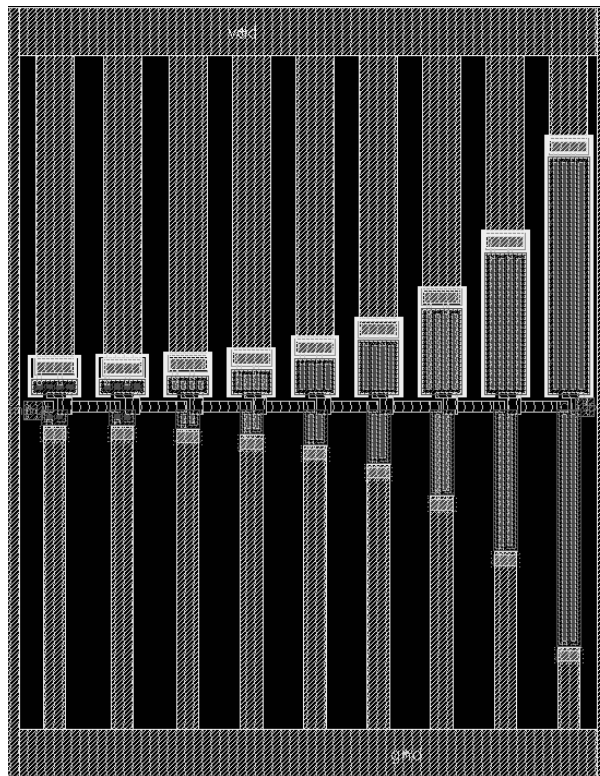
Figure G.24: The buffer of weight 80 layout

G.1.13   Buffer 91
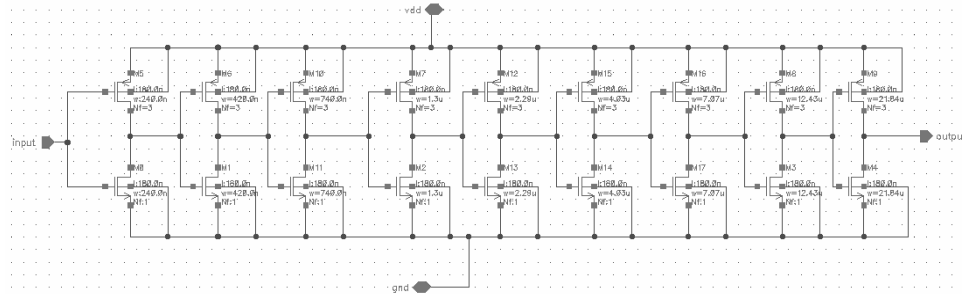
Figure G.25: The buffer of weight 91 schematic
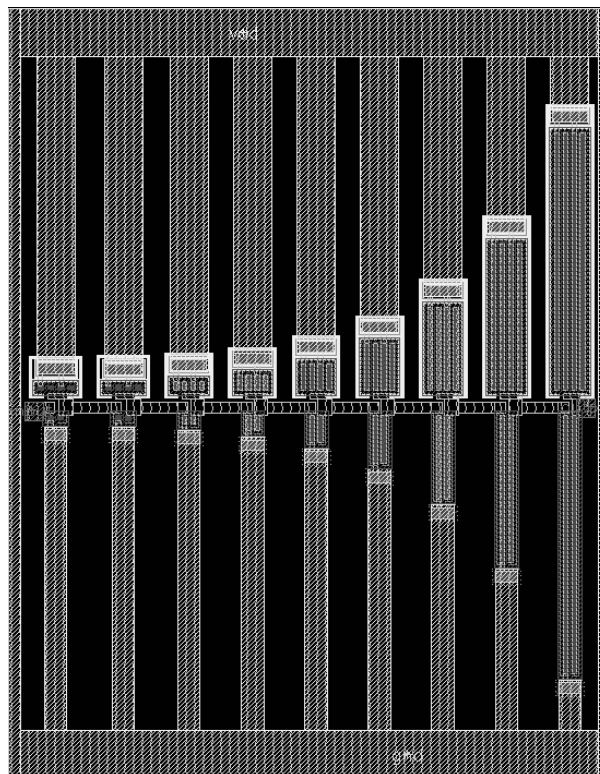
Figure G.26: The buffer of weight 91 layout

G.1.14   Buffer 99

Figure G.27: The buffer of weight 99 schematic

Figure G.28: The buffer of weight 99 layout

G.1.15   Buffer 105

Figure G.29: The buffer of weight 105 schematic

Figure G.30: The buffer of weight 105 layout

G.1.16 Buffer 109

Figure G.31: The buffer of weight 109 schematic
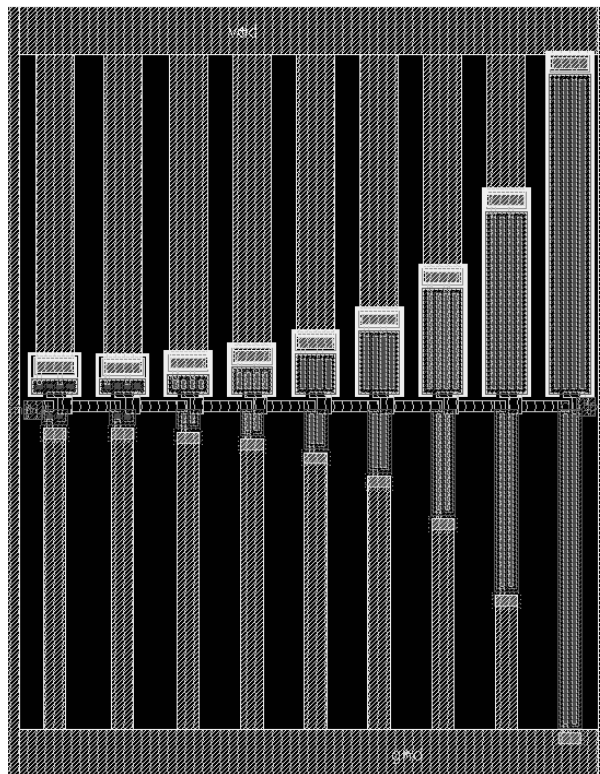
Figure G.32: The buffer of weight 109 layout

G.2   The switches

The switches are the simplest cells of this circuit because they are simply made by juxtaposing identical transistors like tiles the number of times it is required to reach the weight calculated in end of chapter 11. For remembrance, these weights are 2, 3, 5, 8, 12, 17, 24, 33, 43, 55, 67, 80, 91, 99, 105 and 109 with an alternating polarity. The NMOS and PMOS tile schematics and layouts are shown in Figures G.33 and G.34 respectively. The dimension of their transistor is the same as for the reference inverter.
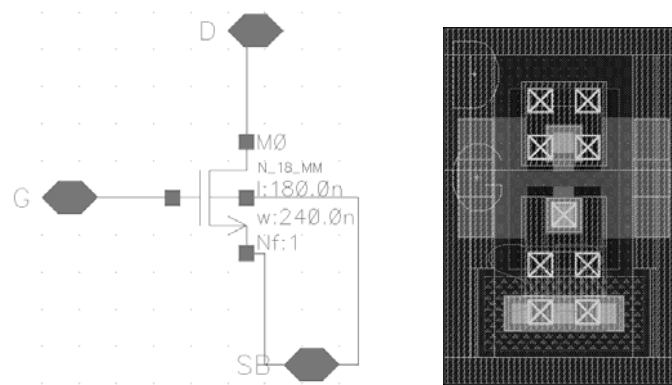
Figure G.33: NMOS tile used for switch building
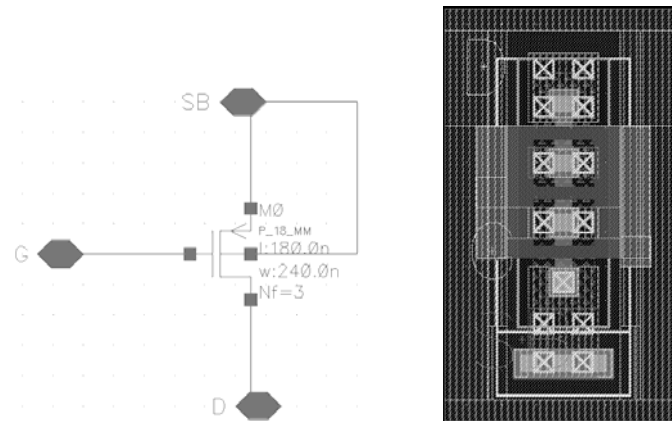
Figure G.34: PMOS tile used for switch building

Metal layer M_1 is used for gate, metal layer M_2 is used for the drain and metal layer M_3 is used for source for both NMOS and PMOS transistors.

G.2.1 Switch 2

The switch 2 is made with 2 PMOS transistors, as shown in Figures G.35 and G.36.
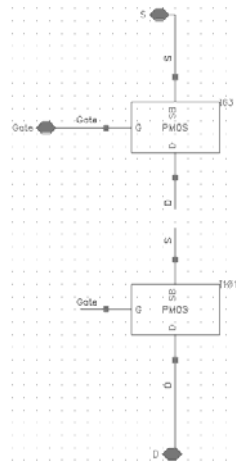
Figure G.35: The switch of weight 2 schematic
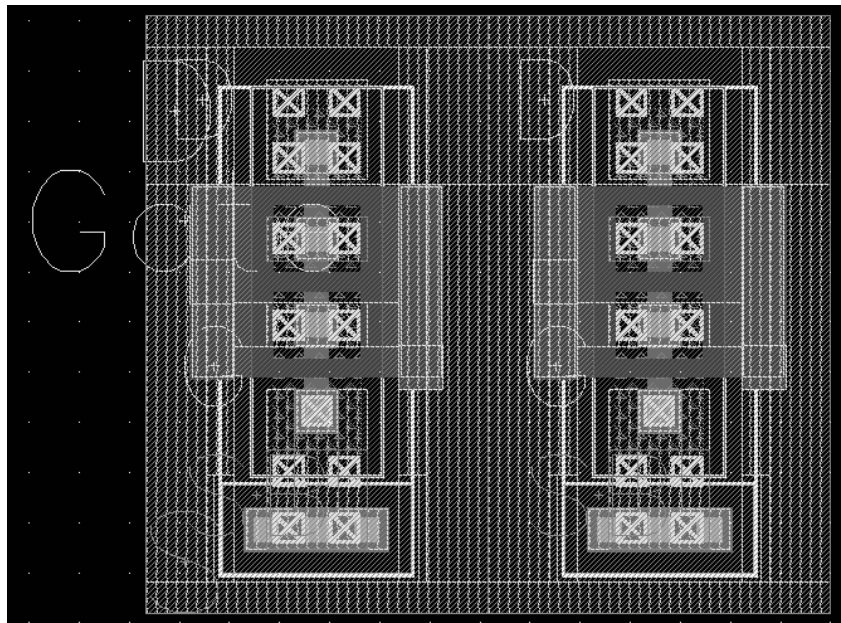
Figure G.36: The switch of weight 2 layout

G.2.2   Switch 3

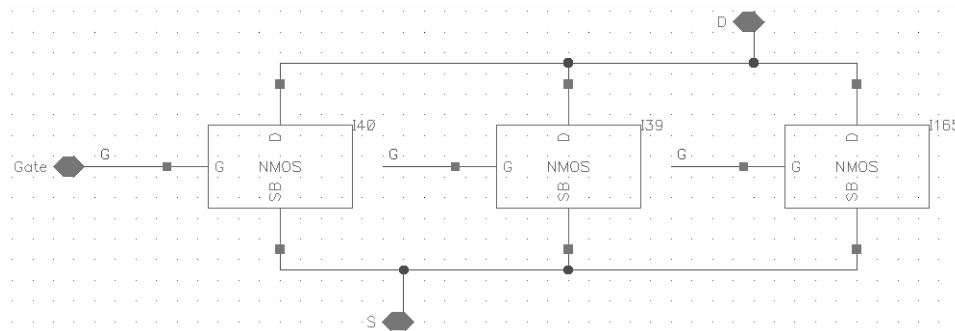The switch 3 is made with 3 NMOS transistors, as shown in Figures G.37 and G.38.

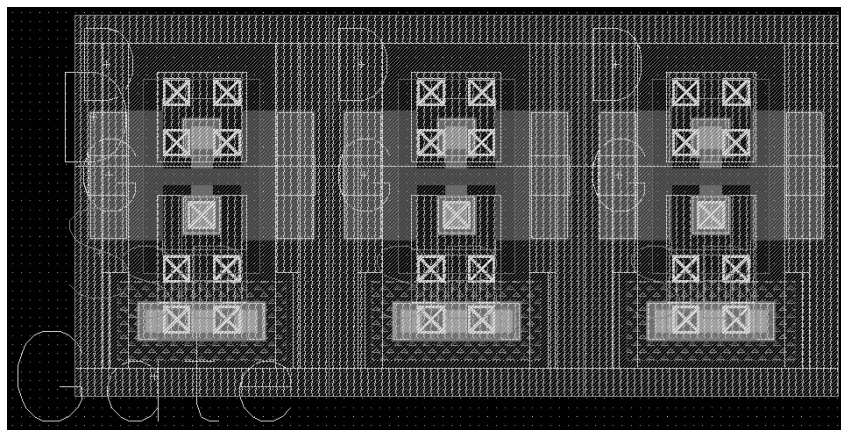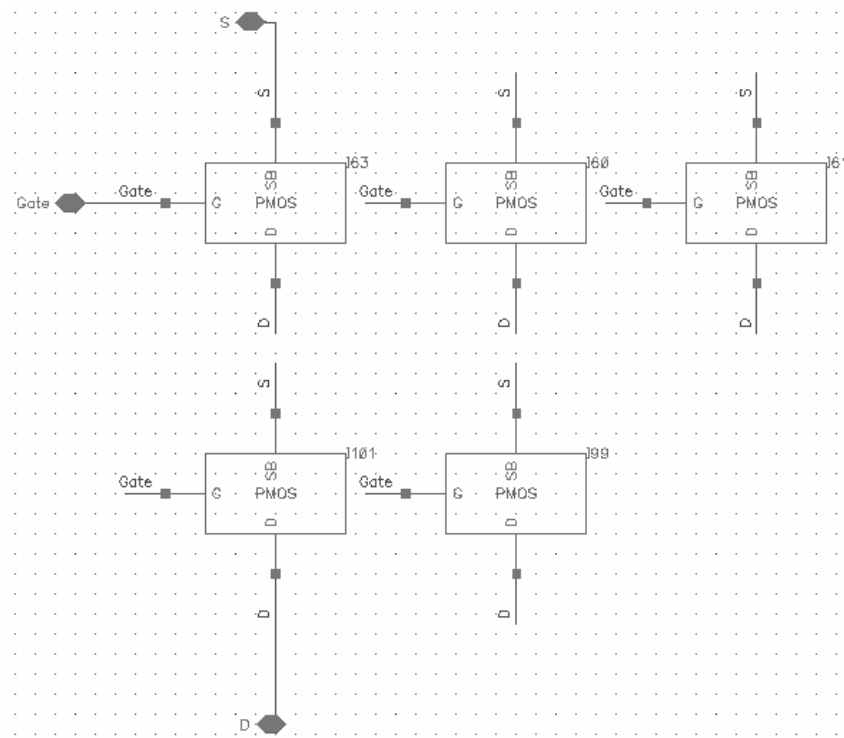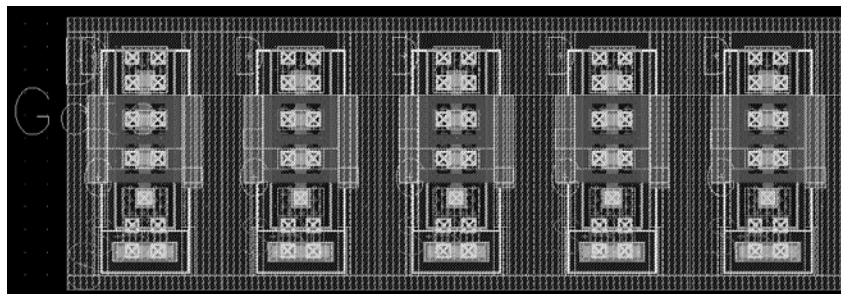
Figure G.37: The switch of weight 3 schematic

Figure G.38: The switch of weight 3 layout

G.2.3 Switch 5

The switch 5 is made with 5 PMOS transistors, as shown in Figures G.39 and G.40.

Figure G.39: The switch of weight 5 schematic

Figure G.40: The switch of weight 5 layout

G.2.4   Switch 8

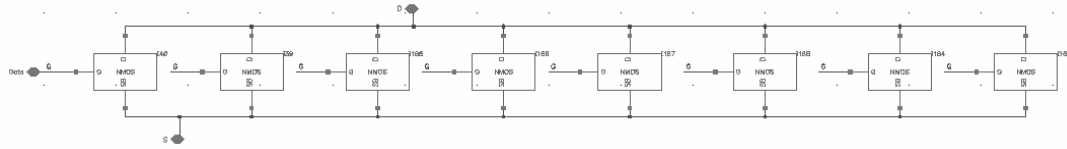The switch 8 is made with 8 NMOS transistors, as shown in Figures G.41 and G.42.

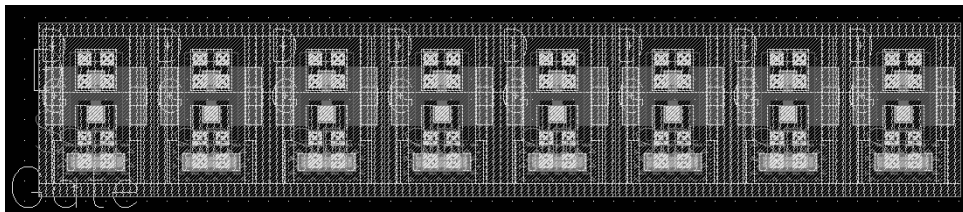Figure G.41: The switch of weight 8 schematic

Figure G.42: The switch of weight 8 layout

G.2.5   Switch 12

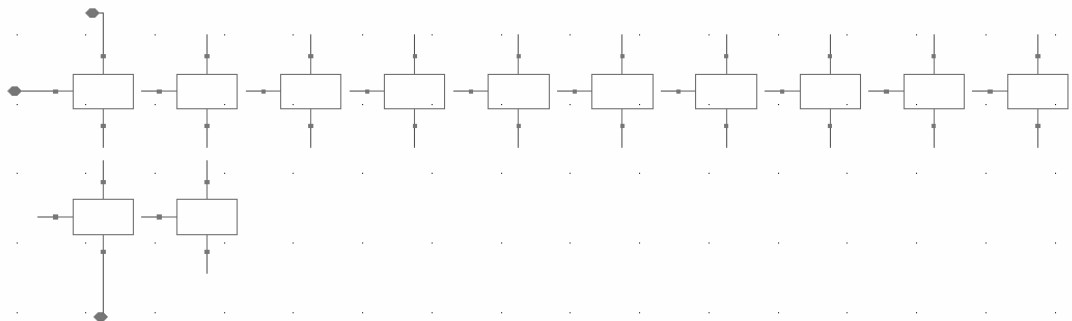The switch 12 is made with 12 PMOS transistors, as shown in Figures G.43 and G.44.
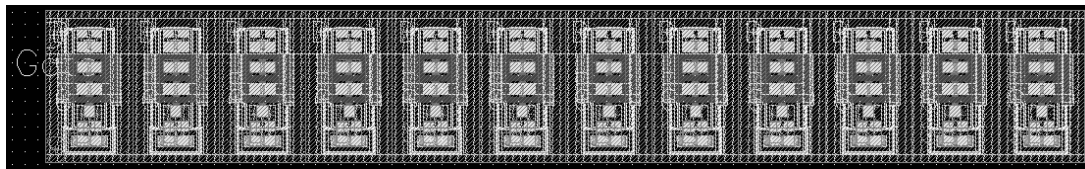

Figure G.43: The switch of weight 12 schematic

Figure G.44: The switch of weight 12 layout

G.2.6   Switch 17

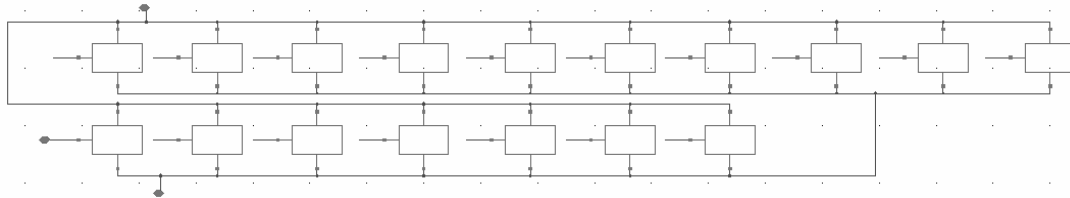The switch 17 is made with 17 NMOS transistors, as shown in Figures G.45 and G.46.
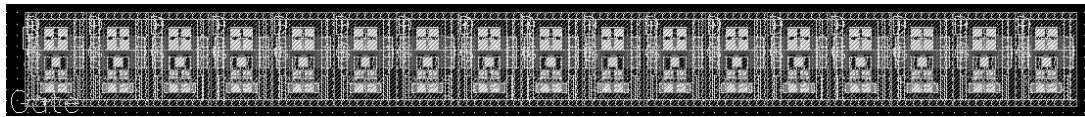

Figure G.45: The switch of weight 17 schematic

Figure G.46: The switch of weight 17 layout

G.2.7   Switch 24

The switch 24 is made with 24 PMOS transistors, as shown in Figures G.47 and G.48.
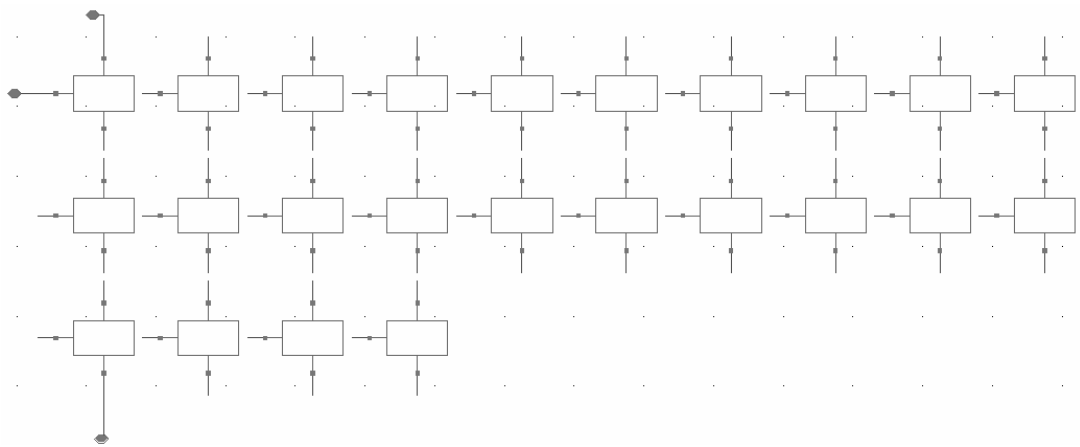

Figure G.47: The switch of weight 24 schematic

Figure G.48: The switch of weight 24 layout

G.2.8   Switch 33

The switch 33 is made with 33 NMOS transistors, as shown in Figures G.49 and G.50.

Figure G.49: The switch of weight 33 schematic

Figure G.50: The switch of weight 33 layout

G.2.9 Switch 43

The switch 43 is made with 43 PMOS transistors, as shown in Figures G.51 and G.52.

Figure G.51: The switch of weight 43 schematic
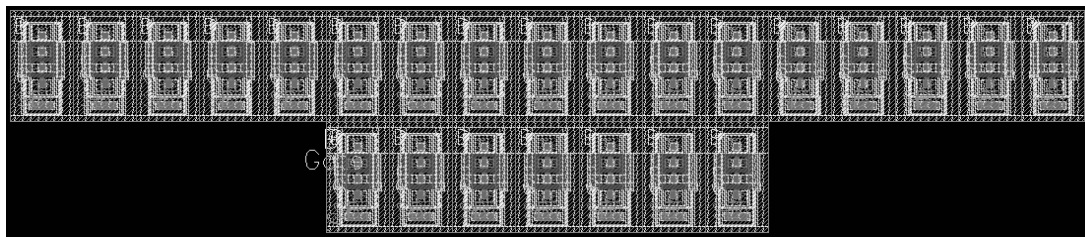

Figure G.52: The switch of weight 43 layout

G.2.10   Switch 55

The switch 55 is made with 55 NMOS transistors, as shown in Figures G.53 and G.54.

Figure G.53: The switch of weight 55 schematic

Figure G.54: The switch of weight 55 layout

G.2.11 Switch 67

The switch 67 is made with 67 PMOS transistors, as shown in Figures G.55 and G.56.
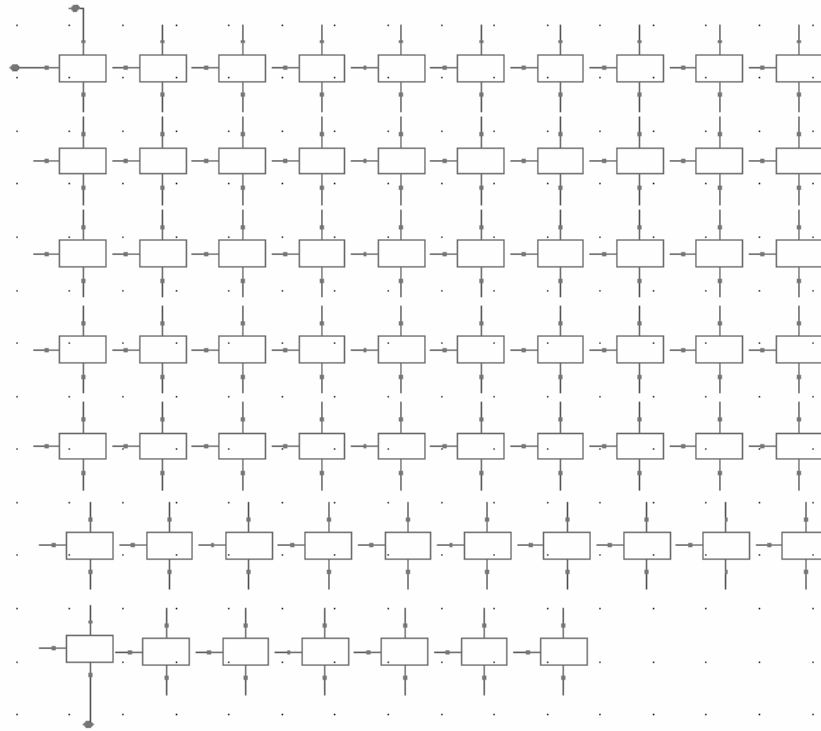
Figure G.55: The switch of weight 67 schematic
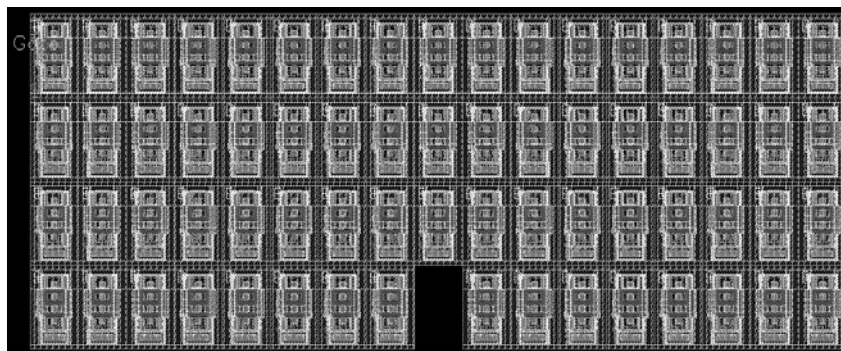
Figure G.56: The switch of weight 67 layout

G.2.12   Switch 80

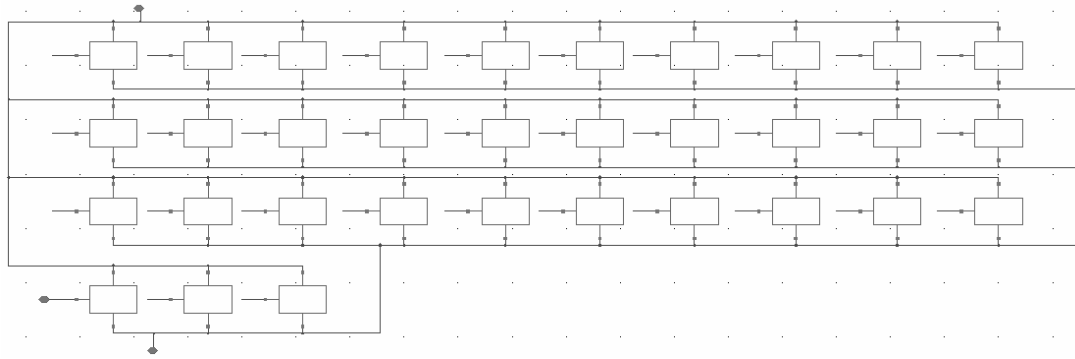The switch 80 is made with 80 NMOS transistors, as shown in Figures G.57 and G.58.
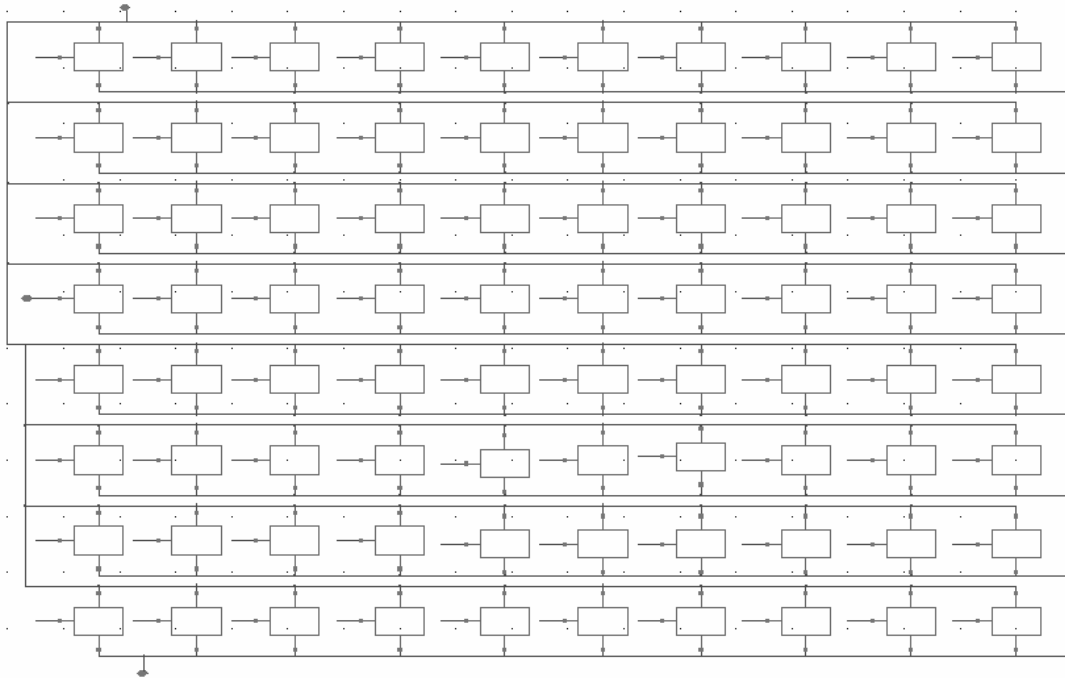
Figure G.57: The switch of weight 80 schematic
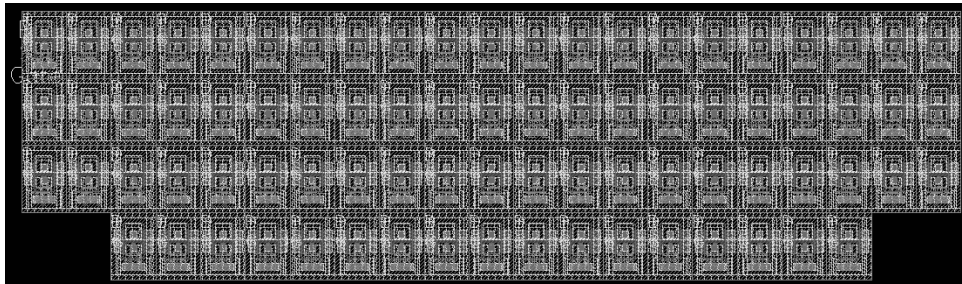
Figure G.58: The switch of weight 80 layout

G.2.13   Switch 91

The switch 91 is made with 91 PMOS transistors, as shown in Figures G.59 and G.60.
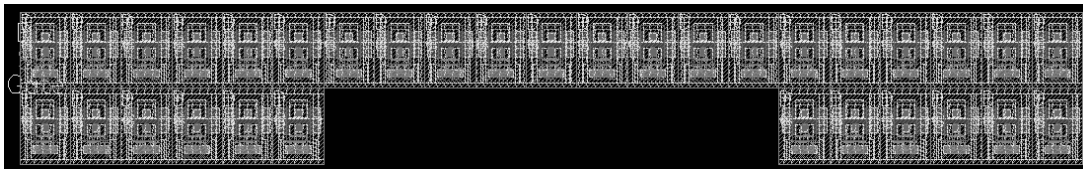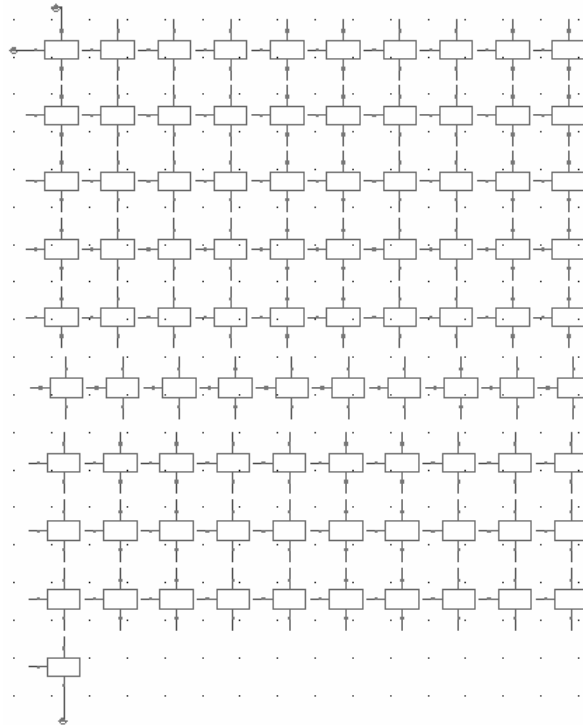

Figure G.59: The switch of weight 91 schematic
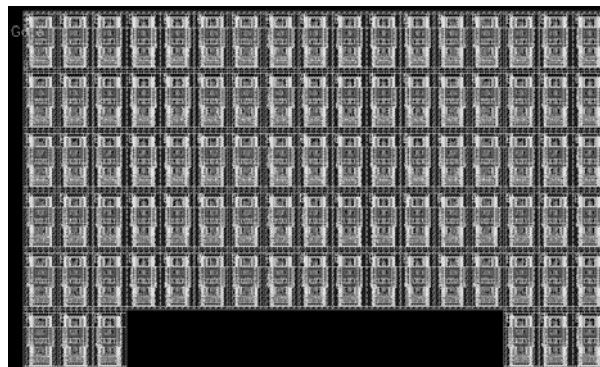
Figure G.60: The switch of weight 91 layout

G.2.14   Switch 99

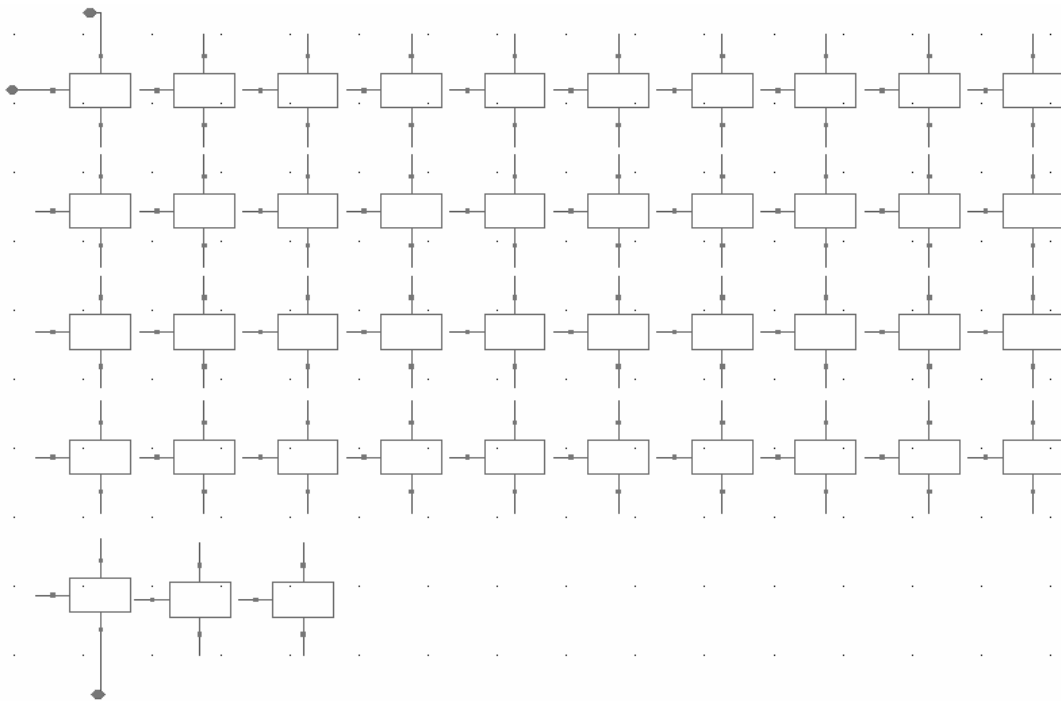The switch 99 is made with 99 NMOS transistors, as shown in Figures G.61 and G.62.
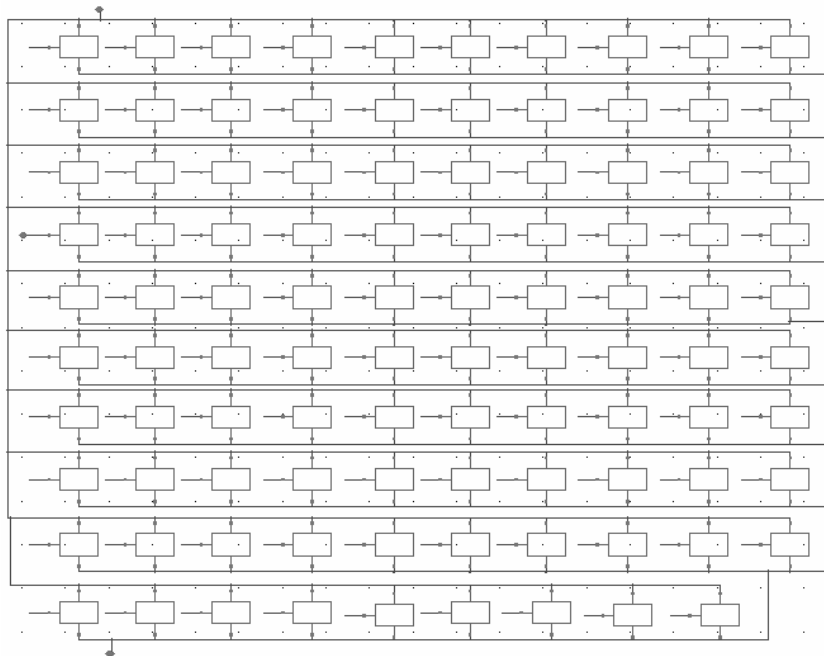
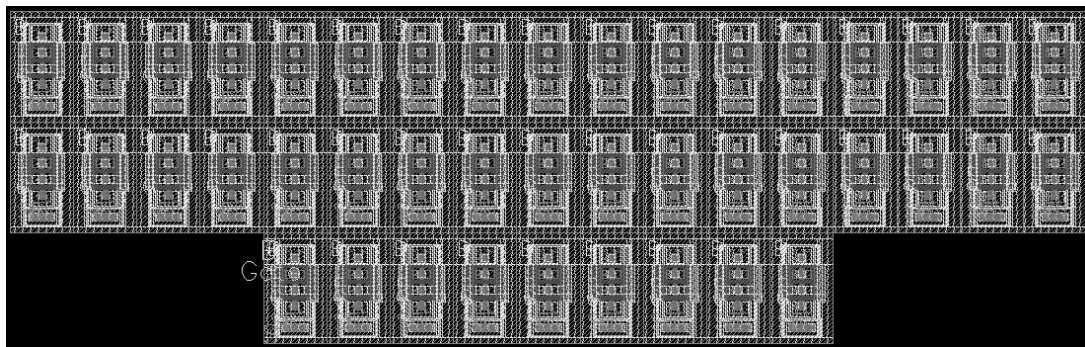Figure G.61: The switch of weight 99 schematic
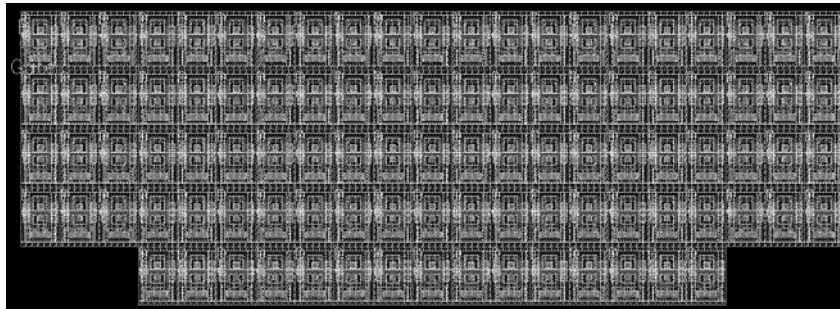
Figure G.62: The switch of weight 99 layout

G.2.15   Switch 105

The switch 105 is made with 105 PMOS transistors, as shown in Figures G.63 and G.64.
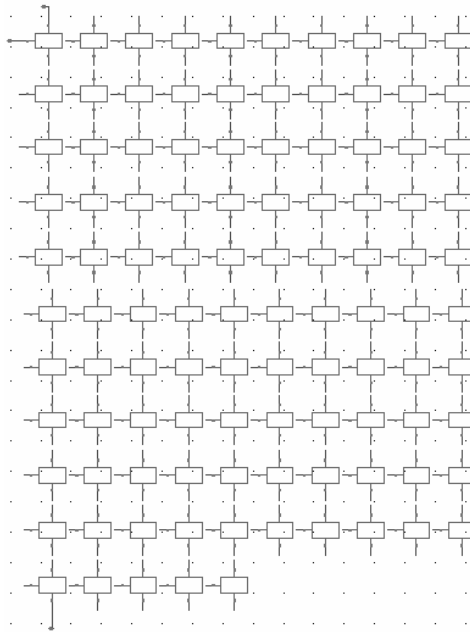
Figure G.63: The switch of weight 105 schematic
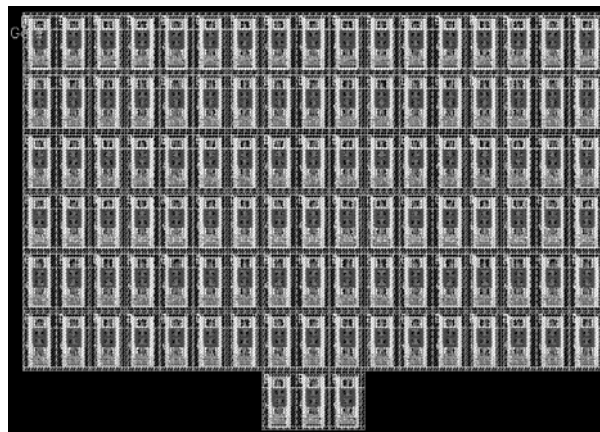
Figure G.64: The switch of weight 105 layout

G.2.16   Switch 109

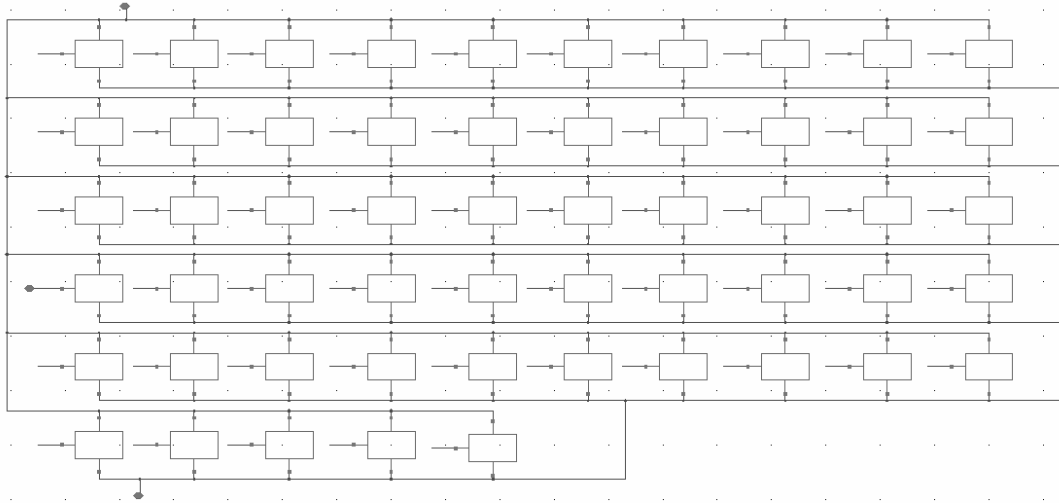The switch 109 is made with 109 NMOS transistors, as shown in Figures G.65 and G.66.
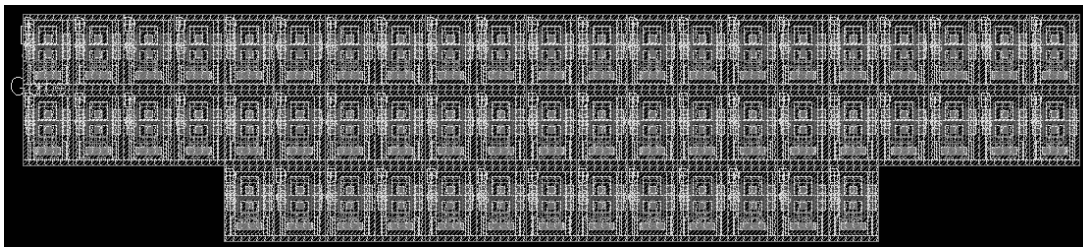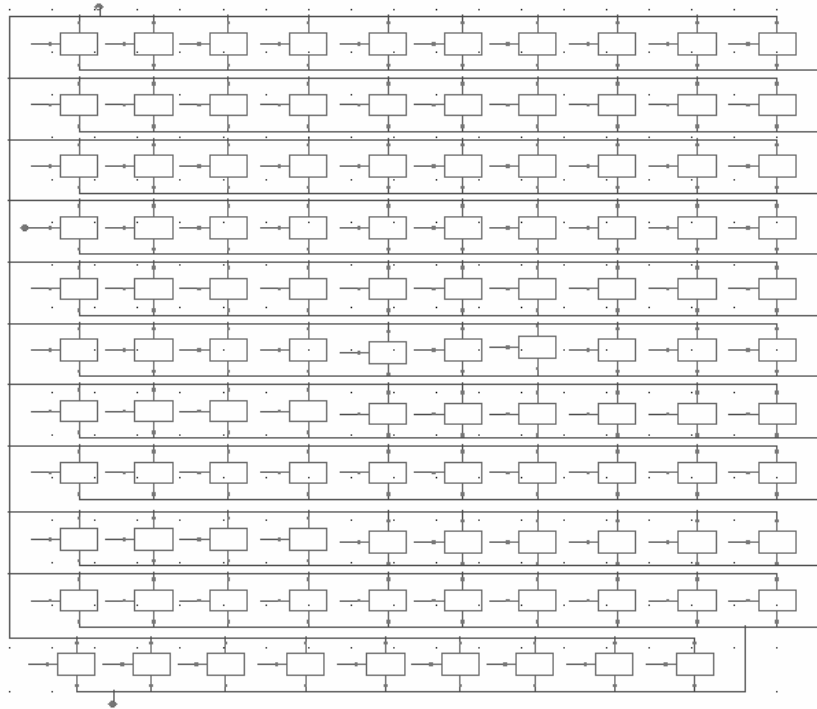

Figure G.65: The switch of weight 109 schematic
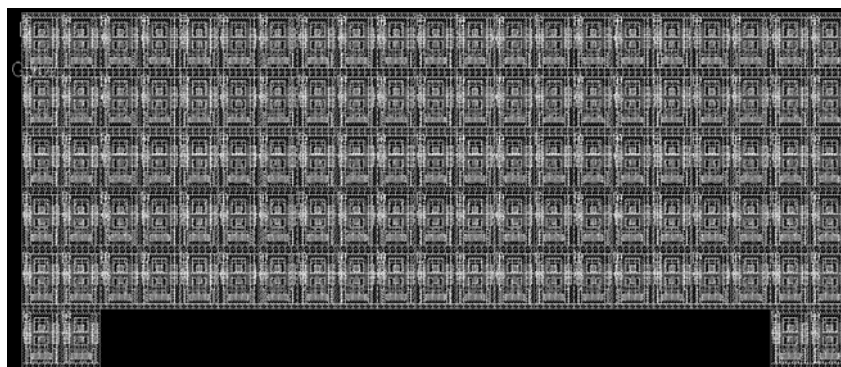
Figure G.66: The switch of weight 109 layout

Chapter H

Buffers layouts for Prototype n° 2

The Appendix gives the detail on the buffers and the switches circuits of the Prototype n° 2 of the integrated UWB transmitter (see Section 13.1.5).

H.1   The buffer 1

The buffer 1 schematic and layout are shown in Figures H.1 and H.2.
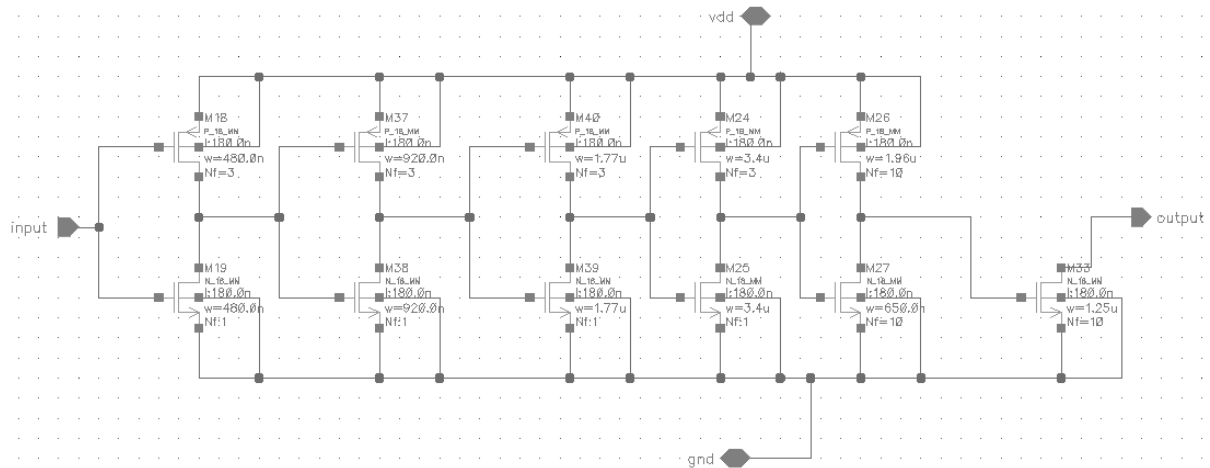
Figure H.1: The schematic of the buffer 1
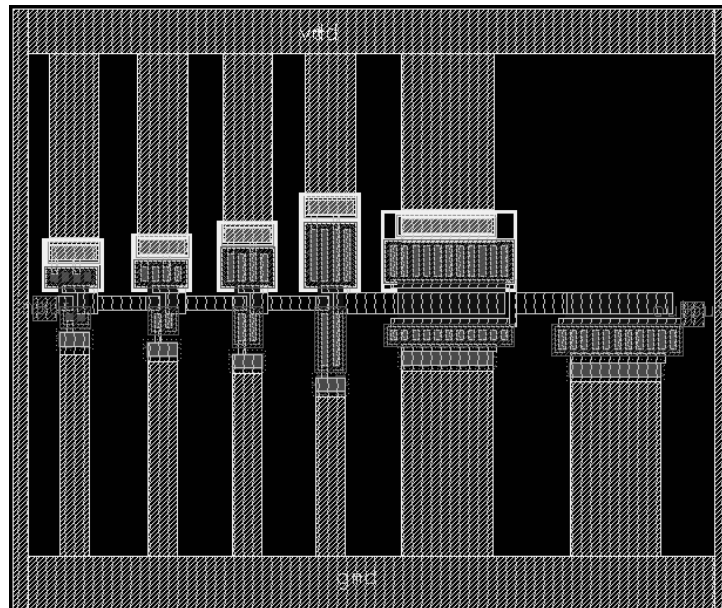
Figure H.2: The layout of the buffer 1

H.2   The buffer 2

The buffer 2 schematic and layout are shown in Figures H.3 and H.4.
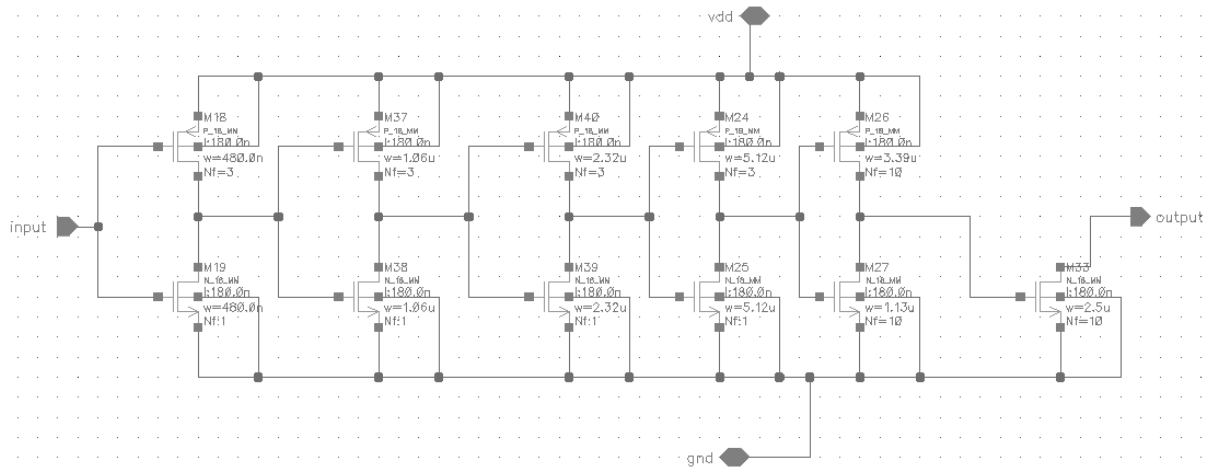
Figure H.3: The schematic of the buffer 2
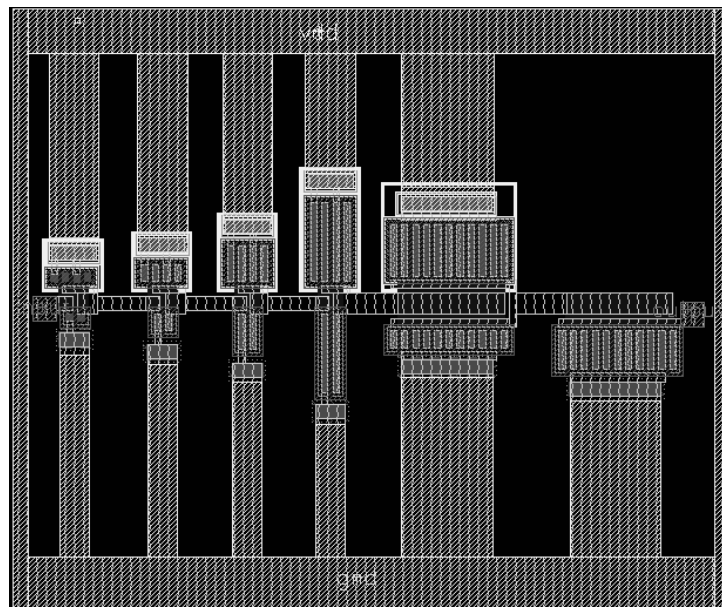
Figure H.4: The layout of the buffer 2

H.3   The buffer 3

The buffer 3 schematic and layout are shown in Figures H.5 and H.6.
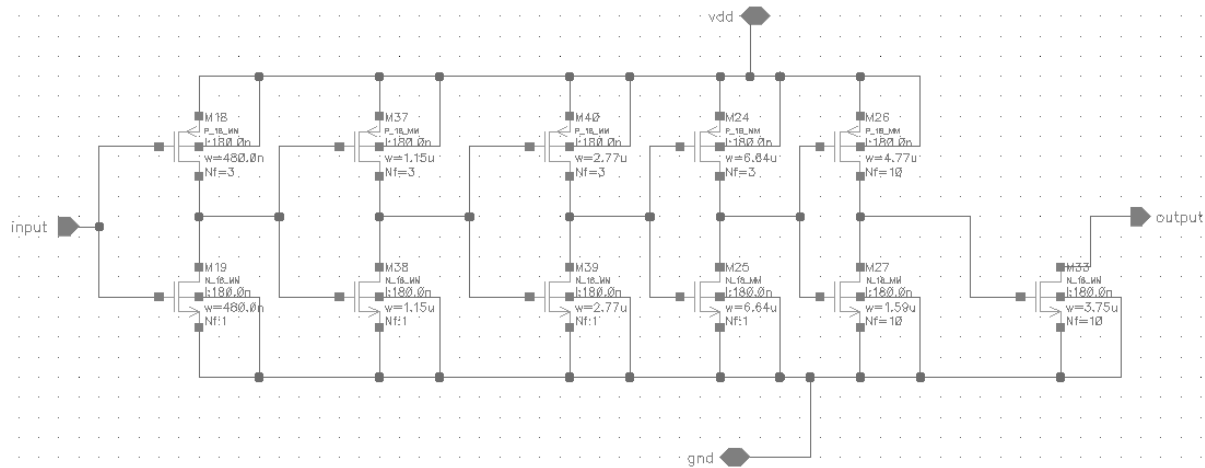
Figure H.5: The schematic of the buffer 3
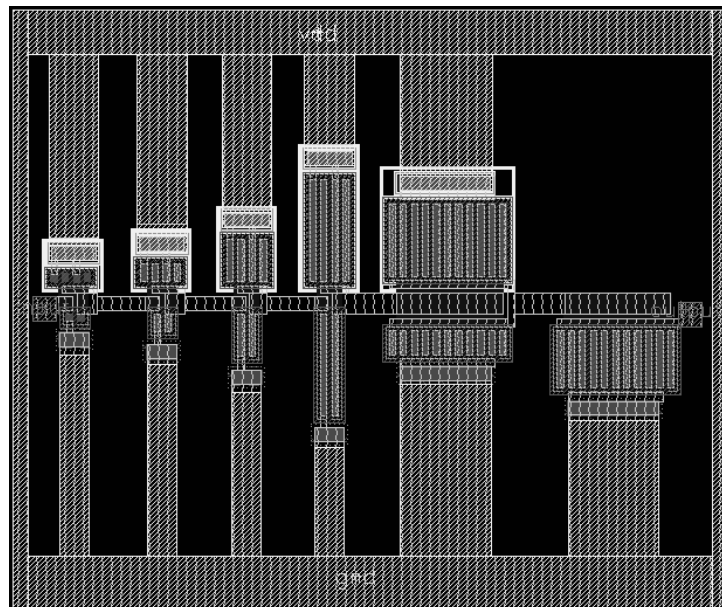
Figure H.6: The layout of the buffer 3

H.4   The buffer 4

The buffer 4 schematic and layout are shown in Figures H.7 and H.8.
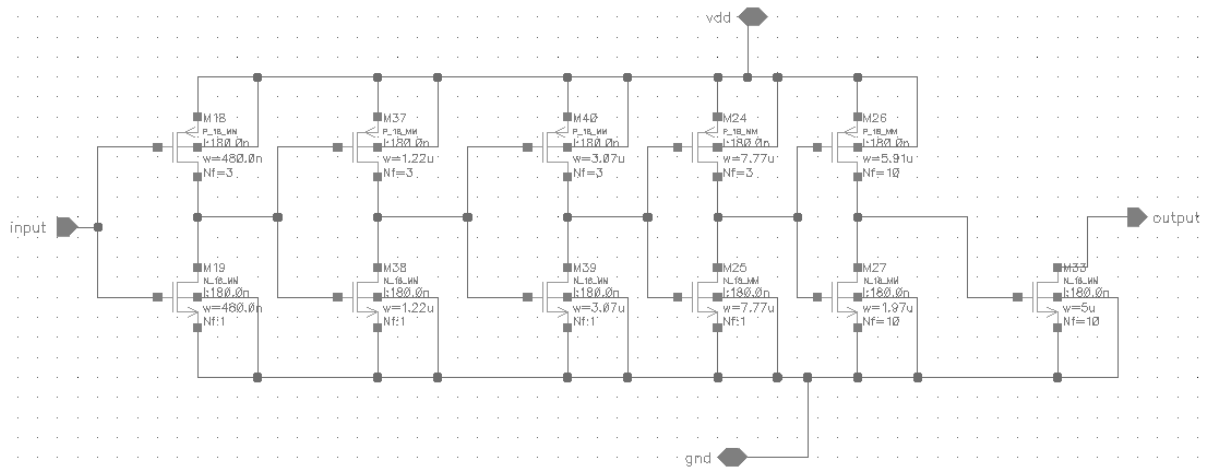
Figure H.7: The schematic of the buffer 4
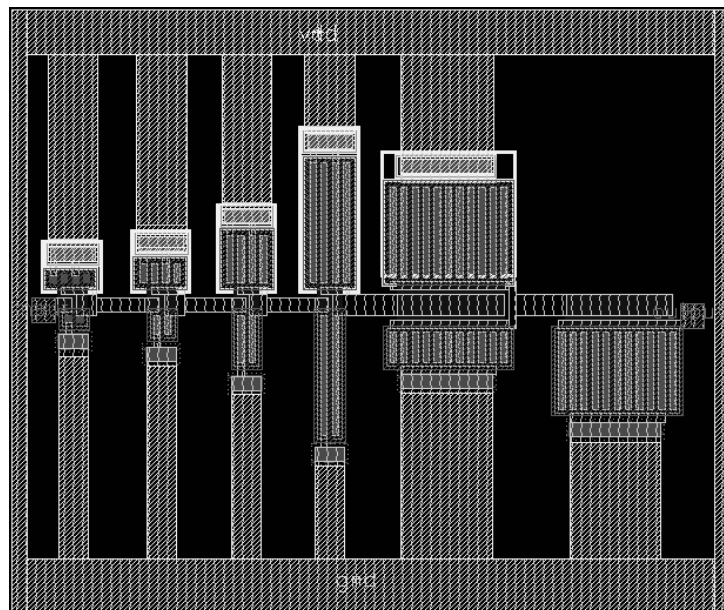
Figure H.8: The layout of the buffer 4

H.5   The buffer 5

The buffer 5 schematic and layout are shown in Figures H.9 and H.10.
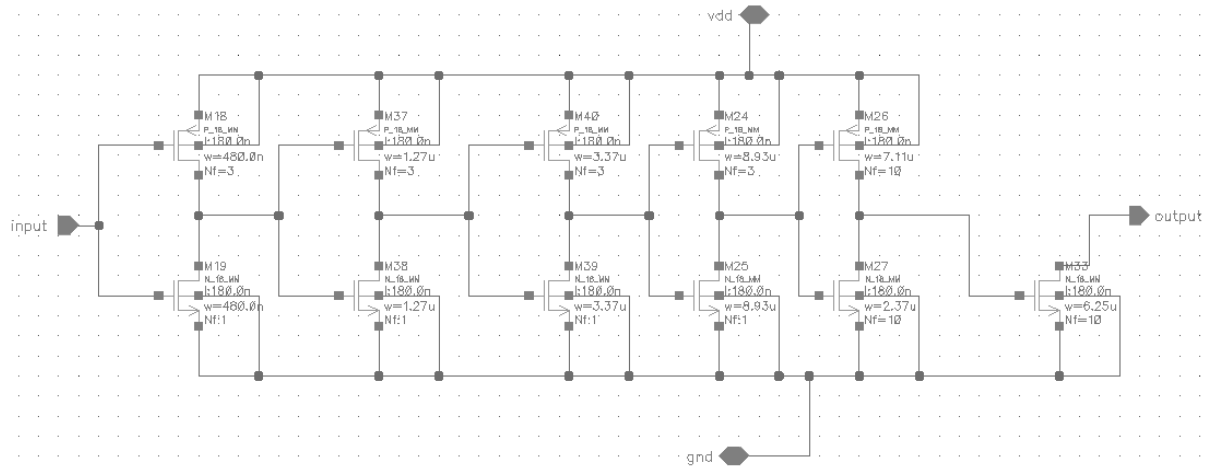
Figure H.9: The schematic of the buffer 5
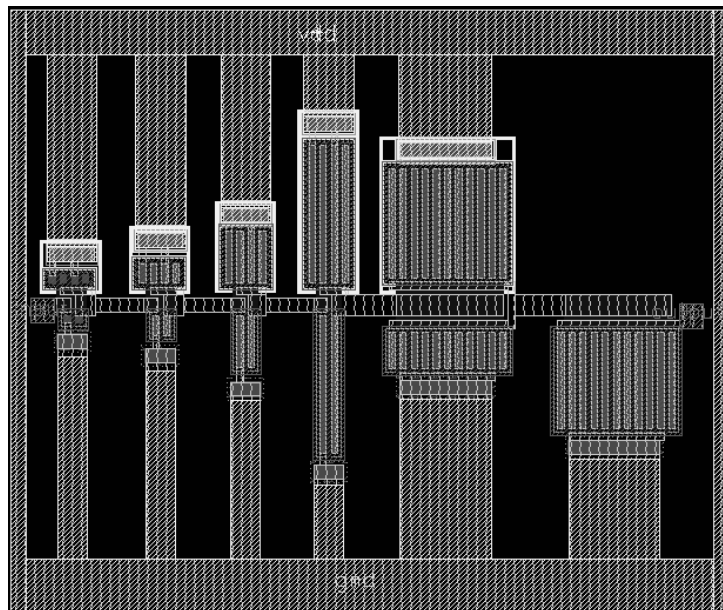
Figure H.10: The layout of the buffer 5

H.6 The buffer 6

The buffer 6 schematic and layout are shown in Figures H.11 and H.12.
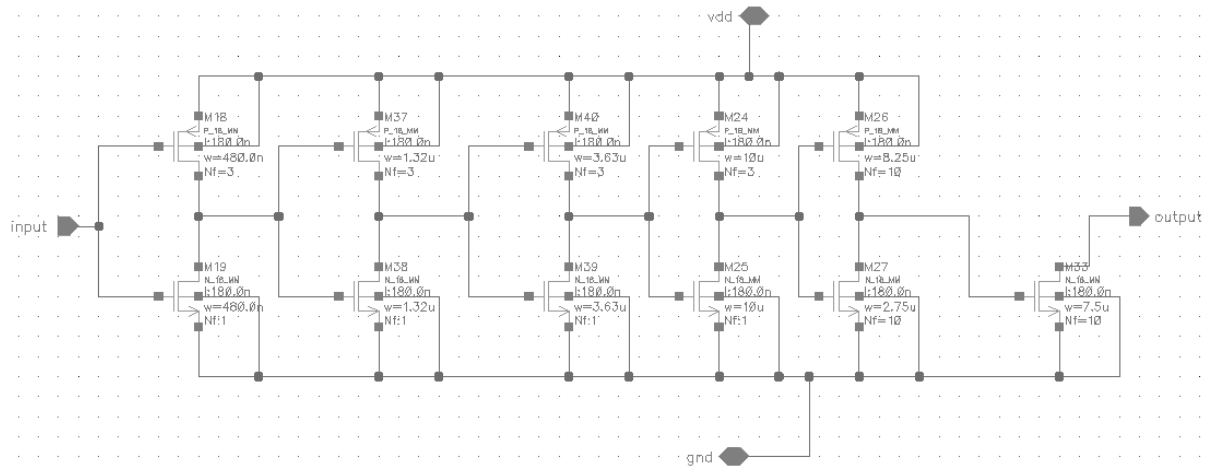
Figure H.11: The schematic of the buffer 6
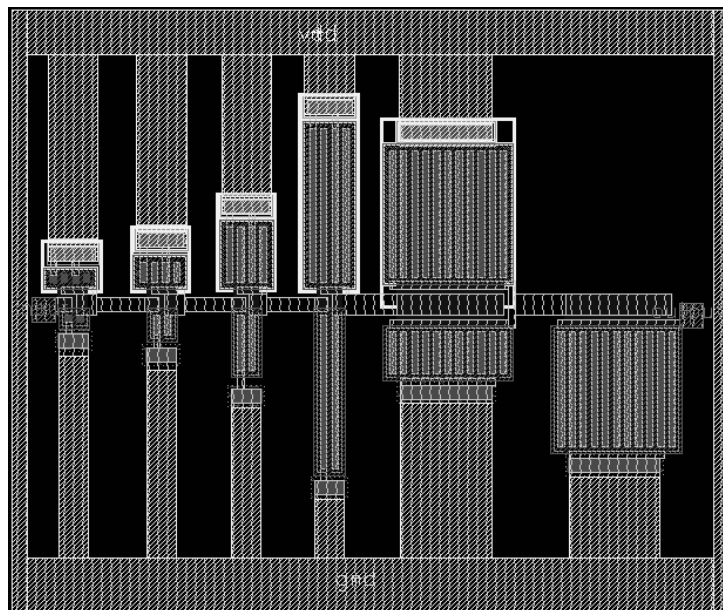
Figure H.12: The layout of the buffer 6

H.7   The buffer 7

The buffer 7 schematic and layout are shown in Figures H.13 and H.14.
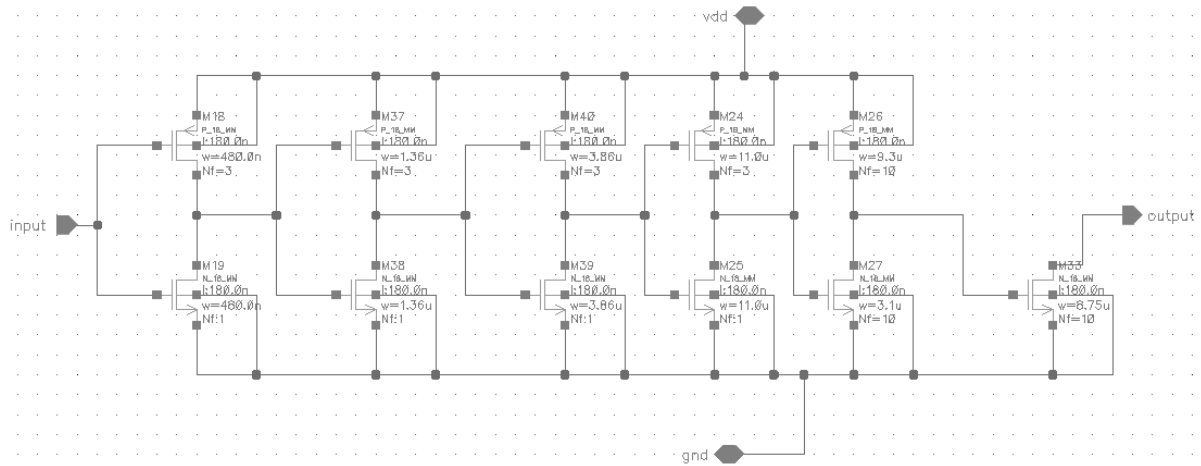
Figure H.13: The schematic of the buffer 7
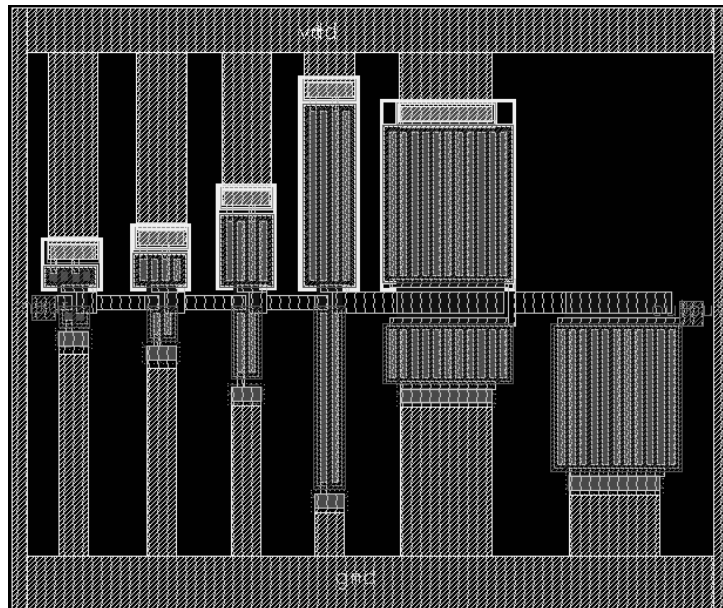
Figure H.14: The layout of the buffer 7

H.8 The buffer 8

The buffer 8 schematic and layout are shown in Figures H.15 and H.16.
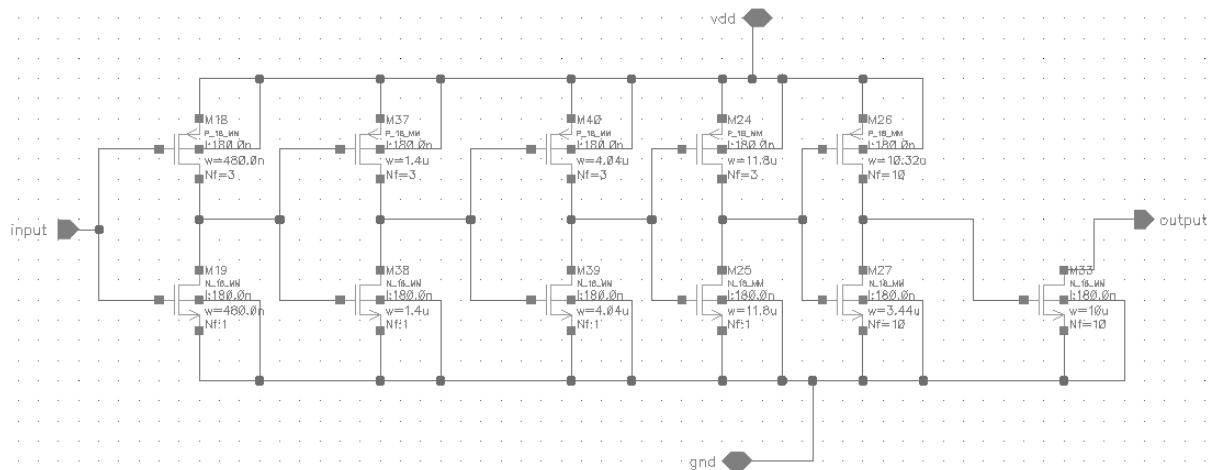
Figure H.15: The schematic of the buffer 8
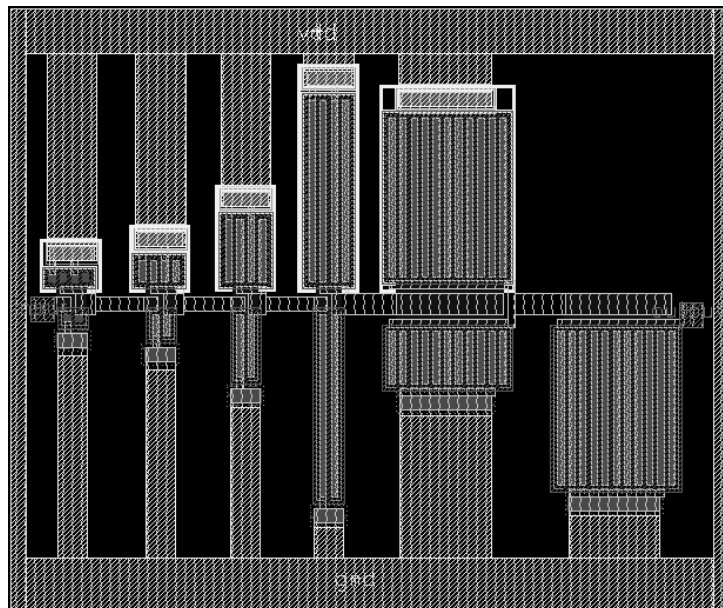
Figure H.16: The layout of the buffer 8

Chapter I

Initial UWB hardware specifications (2006)

This appendix gives the original UWB hardware specifications (UWB Receiver RF Architecture Proposal) as they were given to the author for designing the first UWB testbed. This document shows all the initial research made by Prof. Jean-Yves Le Boudec's team at LCA 2 and on which much of this work was initially based.

UWB Receiver RF Architecture Proposal

UWB MICS network

`ruben.merz@epfl.ch`

May 16, 2006

The datasheets can be found at

`http://icsil1www.epfl.ch/projects/mics-uwb`

Unless it is specified, all frequencies are in GHz.

1 Issues that need to be solved

A+B Link budget for the two proposals

A+B Find proper filters

A+B Tunable amplifier: according to Catherine Dehollain it might be really difficult to find a commercial one. Hence, we might have to build it. So we could perfectly start with a non-tunable one.

A IQ mixer: it appears difficult to find an IQ mixer for the required frequency range (from [1.4, 1.9] to [0.1, 0.6]). According to what we could find, we have already changed the proposed frequency band.

2 Proposal A

2.1 Description and list of the components

Antenna	Skycross SMT-3TO10M
Amplifier 1	MGA86576 (LNA but non-tunable)
Amplifier 2	n/a (does not need to be LNA but should be tunable?)
Filter 1	n/a
Filter 2	n/a
Frequency Synthesizer 1	ADF4360-?
Frequency Synthesizer 2	ADF4360-0 (operated at half the frequency)
Mixer 1	Mini-Circuits ZMX-7GMH (the LO/RF is 3.7-7.0)
	or Mini-Circuits ZX05-C60 (the LO/RF is 1.6-6.0)
Mixer 2	from Amplifonix, MIQ2xMS-1 (LO/RF is 1.4-2.8 and IF DC-0.5)
	or from Marki Microwave IQ-1545 (LO/RF is 1.5-4.5 and IF DC-0.5)
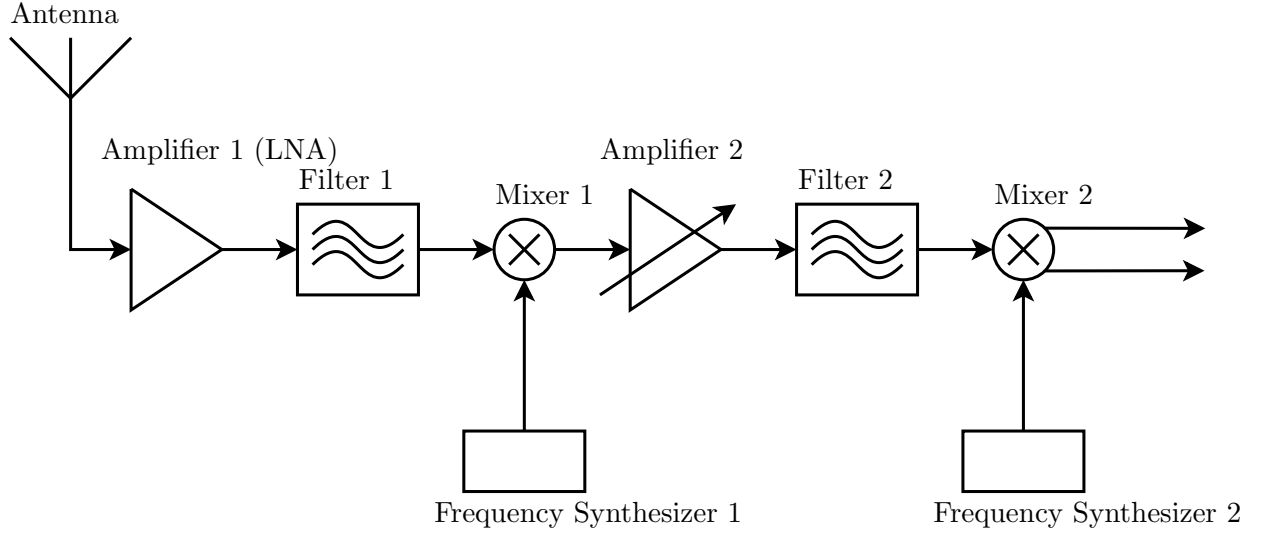
Figure 1: UWB receiver RF architecture: first proposal (A)

2.2 Operating Frequencies

If the ZMX-7GMH is used, the LO/RF of the mixer is [3.7, 7.0] and the IF is [DC, 2.0]. We can select the frequency synthesizer to operates around 4.0 GHz. Hence, the proposal for the various frequencies of the RF chain is

$$[5.4, \ 6.0] \longrightarrow [1.4, \ 1.9] \longrightarrow [0.1, \ 0.6]$$

If the ZX05-C60 is used the LO/RF of the mixer is [1.6, 6.0].

3 Proposal B

3.1 Description and list of the components

Antenna

Amplifier 1 (LNA)
Filter 1

Amplifier 2

Mixer 1

×2 Frequency Doubler

Frequency Synthesizer 1
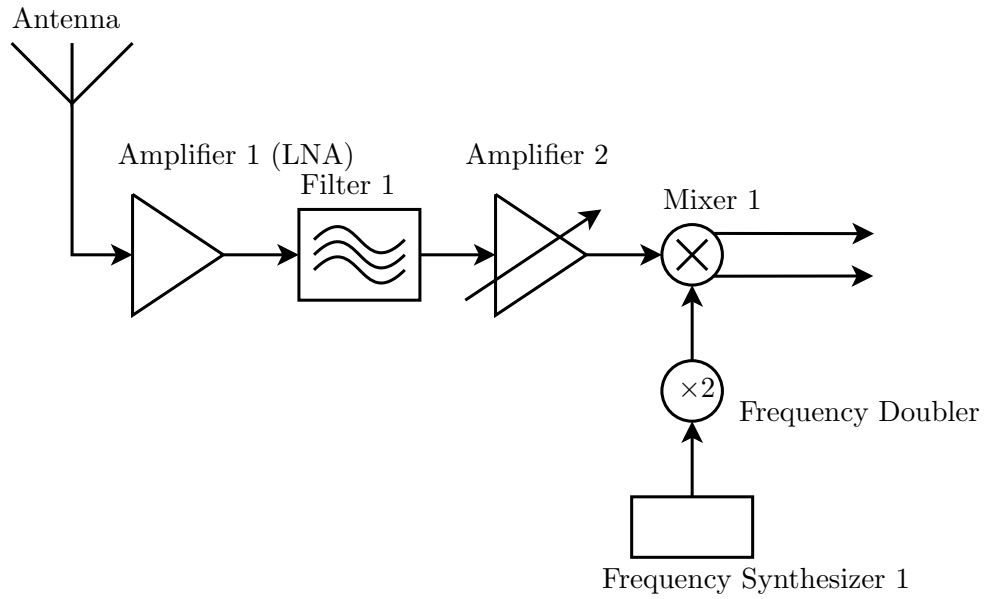
Figure 2: UWB receiver RF architecture: second proposal (B)

Antenna	Skycross SMT-3TO10M
Amplifier 1	MGA86576 (LNA but non-tunable)
Amplifier 2	n/a (does not need to be LNA but should be tunable)
Filter	n/a
Frequency Synthesizer 1	ADF4360-0 or ADF4360-1
Frequency doubler	HMC189MS8
Mixer	HMC525LC4 or HMC-C009

Another possibility for the frequency doubler and synthesizer is the synergy microwave device (Raymond?)

3.2 Operating Frequencies

With the ADF4360-1 (2.050×2)

$$[4.0, \ 4.5] \longrightarrow [0, \ 1]$$

or with the ADF4360-0 (2.600×2)

$$[4.0, \ 4.5] \longrightarrow [-1, \ 0]$$

4 Detailed Information about the Components

4.1 Amplifier, frequency synthesizer and frequency doubler

SMT-3TO10M   From Skycross. Already ordered 12 pieces at a cost of \$60/pc.

MGA86576 From Avago. Is available, samples can be ordered from a retailer.

ADF4360 From Analog Devices. Is available, it seems that samples can be obtained. There is also an evaluation board, but I'm not sure how to obtain it yet. There is -0 version that ranges from 2400 to 2725 MHz. The -1 version ranges from 2050 to 2450 MHz. They both support a 1/2 frequency divider.

HMC189MS8 From Hittite.

4.2 Mixers

ZX05-C60 From Mini-Circuit, it has coaxial connections. No info on the availability. The LO/RF is 1600-4400 MHz or 4400-6000 and the IF is DC-2000 MHz. See the document dg03-84a.

MCA1-60LH From Mini-Circuit, needs a PCB. No info on the availability, one piece can be ordered. The LO/RF is 1700-4400 MHz or 4400-6000 and the IF is DC-2000 MHz. See the document dg03-96.

ZMX-7GMH From Mini-Circuit, it has coaxial connections. No info on the availability, one piece can be ordered. The LO/RF is 3700-7000 MHz and the IF is DC-2000 MHz. See the document dg03-102.

ZMX-8GLH From Mini-Circuit, it has coaxial connections. No info on the availability, one piece can be ordered. The LO/RF is 3700-8000 MHz and the IF is DC-2000 MHz. See the document dg03-98.

ZMX-10G From Mini-Circuit, it has coaxial connections. No info on the availability, one piece can be ordered. The LO/RF is 3700-10000 MHz and the IF is DC-2000 MHz. See the document dg03-94.

HMC525LC4 From Hittite. Not sure about the availability. At least ten pieces must be ordered.

HMC-C009 From Hittite. Not sure about the availability. Quite expensive, but one piece can be ordered.

MIQ2xMS-1 From Amplifonix, needs a PCB. Not sure about the availability. The RF is 1.4-2.8, the LO 1.4-2.8 and the IF DC-0.5.

5 Some Information About the Frequencies

According to Ofcom (checked on their website [2] on May 2006), the band from 3.1 to 4.95 GHz is under study for UWB within ECC.

The WiMax frequencies in Switzerland are at 3.4-3.6 GHz, 3.7 GHz and around 5.8 GHz [1].

References

[1] Faq bwa/wimax from ofcom. `http://www.bakom.admin.ch/dienstleistungen/faq/00732/01291/index.html?l%ang=fr`, 2006.

[2] Ofcom. `http://www.ofcom.admin.ch`, 2006.

Chapter J

Application Note MGA 86576

This appendix gives the original Application Note from Hewlett-Packard for the MGA 86576 which describes the control of the gain because it is impossible to find this very old and rare document anywhere. This document was faxed by a Hewlett-Packard ingineer to Mr Jean-François Zürcher (EPFL-LEMA) who kindly accepted to send us a paper copy. The author scanned it for reference to include in this work. The quality of the original document was very poor (fax) and it is normal that some parts of it are badly reproduced. It is given here as it is with the best fidelity we can.

The variation of the gain is explained on page 5 of this document. To the best of our knowledge, this is the only official mention form Hewlett-Packard of a voltage-controlled gain with this MMIC and, more generally, the only mention of any variable gain amplifier by them.

Practical Applications of a Low Cost Low Noise GaAs PHEMT MMIC for Commercial Mark s

by
A. Ward
Hewlett-Packard CMCD Applications Department
Richardson, TX.
and
H. Morkner
Hewlett-Packard CMCD R&D Division
Newark, Ca.

ABSTRACT

A high performance low cost surface mount ceramic packaged GaAs MMIC for the 1.5 to 8 GHz frequency range is described. The MMIC uses .15 u gate PHEMT devices, self biasing current sources, source follower interstage, resistive feedback and internal impedance matching to produce a state-of-the-art amplifier. Using a minimum of external components, the MMIC provides a nominal 20 dB gain from 1.5 to 8 GHz, a 2 dB noise figure and a nominal power output of +5 dBm from a single dc power supply. With a simple series inductor, the noise figure can be lowered to 1.6 dB over a smaller bandwidth. Working circuits for various commercial applications are presented along with actual test results.

INTRODUCTION

A GaAs monolithic microwave integrated circuit low noise amplifier has been designed for use in the numerous commercial applications in the 1.5 to 8 GHz frequency range[1]. Typical markets include GPS at 1.5 GHz, PCN at 1.9 GHz, MMDS at 2.1 GHz, ITFS at 2.5 GHz, ISM at 2.4 GHz and 5.8 GHz, TVRO at 4 GHz and instrumentation in the 1.5 to 8 GHz frequency range.

The MMIC includes internal impedance matching and integrated biasing allowing simplified low noise amplifier design eliminating the numerous components normally required for a discrete low noise amplifier design. The MMIC delivers an Fmin within a dB of a typical discrete design in a fraction of the space. The MMIC is available in a low cost ceramic package and is now available as the Hewlett-Packard MGA-86576.

The performance of the MMIC as a low noise amplifier will be described. Other special applications such as a variable gain amplifier and active mixer will also be addressed.

DESIGN

The schematic diagram shown in Figure 1 is a lumped element representation of the MMIC. The MMIC consists of two gain stages, an interstage source follower stage, three current sources, two resistive feedback networks, several bias resistors and bypass capacitors. The current sources insure that each PHEMT stage is biased at 25% of Idss. Process variations effect both

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the FET and current source simultaneously resulting in a constant device Idss producing devices with very repeatable RF performance. .
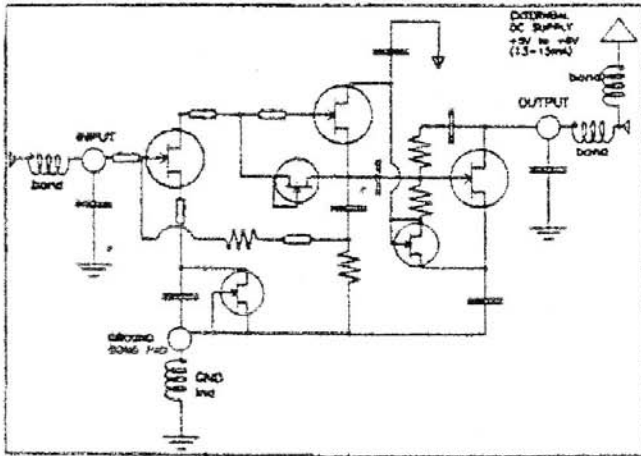
Figure 1. MMIC Schematic Diagram

An advantage of the PHEMT process is the inherent low knee voltages which allow the FET stages to be connected in series to share the device current. This results in a low current MMIC that operates from a supply voltage of only 5 volts.

PERFORMANCE: MMIC VS FET

The MMIC offers several advantages over a discrete FET design. The primary advantage of the MMIC is in the bias configuration. Whereas a typical discrete FET amplifier design may use active biasing to set the bias point, the MMIC requires only a simple RF choke to feed in bias from a 5 volt power supply. This minimizes the board space required to bias the device by eliminating 10 to 15 components. The internal current sources in the MMIC keep the device current bias in a fairly narrow window which results in very repeatable RF performance.

A second advantage of the MMIC is that the input is partially matched to 50Ω making the MMIC easier to match than the generally high impedances associated with the unmatched FET. As an example at 4 GHz, the S11 of the MMIC is less than 0.5 while Gamma Opt is less than 0.4. Typically, the S11 and Gamma Opt of the unmatched FET are much higher at 4 GHz. The lower

input impedance generally means it is easier to achieve a wide bandwidth with a low tolerance matching structure. Even with no input matching, the 50 Ω noise figure is about 2 dB. With a small amount of inductance in the input network, it is possible to achieve device noise figure as low as 1.6 dB.

A third advantage of the MMIC is that its gain is equivalent to a two stage FET amplifier. This has additional advantages in the form of decreased component count and decreased board space required.

The disadvantage is its inherently higher noise figure. The MMIC noise figure is generally about 1 dB higher than the typical low noise PHEMT device. This is due to the resistive loading and feedback inherent to the design. For most applications, this may not be a problem. The nominal 2 dB noise figure does make the MMIC an ideal first stage for most applications and an ideal second stage device in a very low noise amplifier.

APPLICATION

BIAS DECOUPLING NETWORKS

Biasing the device simply requires the use of an RF choke to supply 5 volts to the output terminal. The RF choke at microwave frequencies can be in the form of a high impedance microstripline properly bypassed at the power supply end. The optimum length would be a quarterwave at the desired frequency of operation but as the results show one nominal length does provide good operation from 2 to at least 6 GHz. The use of lumped inductors is not desired since they do tend to radiate and cause undesired feedback.

Low loss capacitors are used to couple the RF in and out of the device. The dc blocking capacitors should provide a low impedance over the desired operating bandwidth without adding excessive series inductance. Although there is no voltage present at the input of the device, it is suggested that a dc blocking capacitor be used especially if the device is preceded with another amplifier device. A suggested value of blocking capacitor for use in the 1.5 to 6 GHz frequency range is 27 pF.

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NOISE MATCH

The device's 50Ω noise figure is approximately 2 dB. Decreasing the noise figure at 4 GHz, as an example, requires that a matching network transform 50Ω to Gamma Opt of the device. (Gamma Opt is the device reflection coefficient required for the device to produce its minimum noise figure) At 4 GHz, the Gamma Opt is .38 @ 51 degrees. A Smith Chart exercise suggests a series inductance of about 2 nH and a shunt capacitance less than 0.2 pF to transform 50Ω to Gamma Opt. The best way to implement this matching circuit would be to raise the input lead of the device and make it into a loop. The shunt capacitance required is so low that it can be overlooked and still achieve good results. The matching network will lower the noise figure about 0.5 dB at 4 GHz.

PRINTED CIRCUIT BOARD MATERIALS

Most commercial applications dictate the need to use inexpensive epoxy glass materials such as FR-4 or G-10. Unfortunately the losses of the this type of material can become excessive above 2 GHz. A 0.5 inch long 50 Ω microstripline along with a 27 pF blocking capacitor and two SMA end launch connectors has a measured 0.35 dB loss at 4 GHz and 1.25 dB loss at 6 GHz! We can generally tolerate the loss as a gain loss but not as an increase in device noise figure.

A second concern would be the thickness of the material. In a typical microstripline topology, the common leads of the MMIC must be attached to the bottom ground plane with the use of plated through holes. The inductance associated with these plated through holes adds series inductance which can cause gain peaking and potential instability. The MMIC has been designed to accommodate dielectric board thicknesses of 0.040 inch or less without adversely effecting MMIC operation.

ACTUAL CIRCUITS AND MEASURED PERFORMANCE

GAIN AND NOISE FIGURE PERFORMANCE

The schematic diagram of the demonstration amplifier is shown in Figure 2. The amplifier consists of 50 Ω microstripline and dc block capacitors and a bias decoupling line. The resistor in series with the bias decoupling line can be adjusted depending on the available supply voltage. It is suggested that a minimum of 10Ω be used to de-Q the bias decoupling line.

1. 50 OHM LINE = .060 " WIDE
2. HI-Z LINE = .020 " WIDE, 0.2 " LONG
3. FR-4/G-10 DIELECTRIC MATERIAL .031 " THICKNESS
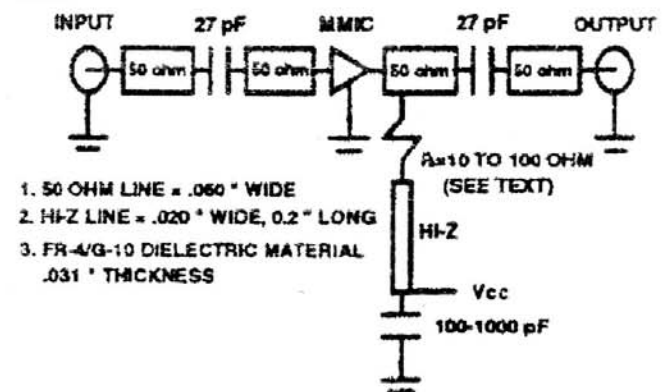
Figure 2 Schematic Diagram of MMIC demonstration amplifier

The gain performance of the MMIC as measured in a demonstration amplifier using G-10 dielectric material is shown in Figure 3. The gain is shown for device voltages of 5, 6, 7, and 10 volts.
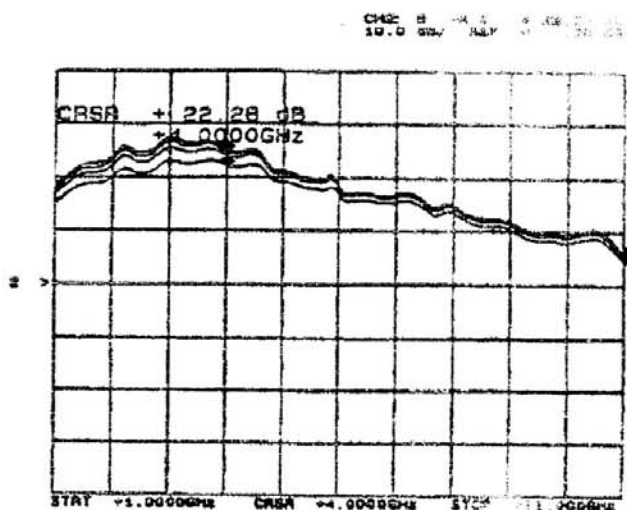
Figure 3. Gain vs. frequency for G-10 demonstration amplifier

The extraordinary band width of this amplifier makes it usable anywhere in the 1 to 10 GHz frequency range. The gain peaks

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between 3 and 4 GHz with about 22 dB gain at a device voltage, Vdd, of 5 volts. Increasing, Vdd, to 7 volts increases the gain at 3 GHz to 26 dB. The noise figure of the device was optimized for lowest noise in the 2 to 6 GHz frequency range. Actual untuned noise figure at 2.3 and 4 GHz including board losses is 2.5 dB. Subtracting the 0.35 dB loss for the input microstripline plus dc blocking capacitor suggests an untuned device noise figure of 2.15 dB at 4 GHz.

For applications that require a lower noise figure, the use of a low loss material such as Duroid^{TM} or Taconics TLY-5 is highly recommended. Measured noise figure of a demonstration board using Duroid 5880 is shown in Table I. The amplifier exhibits less than a 2.54 dB noise figure from 1.3 to 5.8 GHz. The low noise performance of this device makes it suitable for low noise amplification in the 2.4 and 5.8 GHz spread spectrum bands. Noise figure at 900 MHz increases to 2.97 dB while noise figure at 10.5 GHz is still a respectable 3.34 dB.

FREQ(GHz)	Noise Figure(dB)
0.9	2.97
1.3	2.46
1.6	2.27
2.3	2.10
4.0	2.04
5.8	2.54
10.4	3.34

Table I Noise Figure vs. frequency (Duroid 5880 dielectric material)

The noise figure of the MMIC amplifier can be decreased by implementing a noise match instead of being driven directly from a 50 Ω source. The schematic diagram shown in Figure 4 shows an amplifier which has been optimized for low noise in the 3.7 to 4.2 GHz frequency range. The input match is implemented by the use of the input lead acting as an inductor.

1. 50 OHM LINE = .060 " WIDE
2. HI-Z LINE = .020 " WIDE, 0.2 " LONG
3. FR-4/G-10 DIELECTRIC MATERIAL .031 " THICKNESS
4. L1 = .150" INPUT LEAD BENT INTO A LOOP
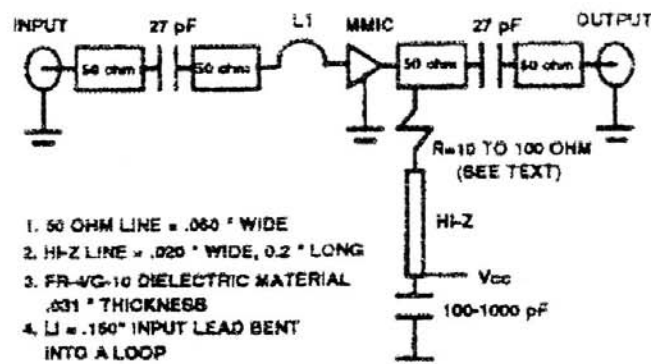
Figure 4 Noise Matched MMIC amplifier (G-10 dielectric material)

The performance of the circuit shown in Figure 4 is shown in Table II.

FREQ(GHz)	GAIN (dB)	N.F.dB)
3.7	24.0	1.92
3.8	24.0	1.92
3.9	23.7	1.89
4.0	24.0	1.89
4.1	23.9	1.90
4.2	23.3	1.86

Table II Gain and Noise Figure for MMIC amplifier with noise match (G-10 dielectric material)

Subtracting the 0.35 dB loss of the G-10 dielectric material suggests an actual noise figure of 1.55 dB for the device. To achieve within a 0.1 dB of this noise figure in an actual board will require the use of one of the lower loss materials discussed earlier.

POWER OUTPUT PERFORMANCE

Although primarily designed for low noise and broad band stable gain, the MGA-86576 provides moderate power output considering its low bias point. At a Vdd, of 6 volts, the device provides a measured output 1 dB gain compression point, P1dB, of +5 dBm at 4 GHz. At a higher Vdd of 7 volts, P1dB increases slightly to +5.5 dBm. The measured two-tone third order intercept point, IP3, as referenced to the output is +16 dBm. Increasing the Vdd to 7 volts increases IP3 to +17 dBm.

OTHER PROPERTIES

Although specifically designed for use as a low noise amplifier, the MMIC also works well as a variable gain amplifier and an active mixer. The following section discusses the MMIC in these two applications and presents actual but not guaranteed performance data.

VARIABLE GAIN AMPLIFIER

An added benefit of the MGA-86576 is its ability to operate as a variable gain amplifier. By simply adding a 7.5 K ohm chip resistor and an additional bias decoupling line appropriately bypassed, an additional positive or negative voltage can be injected into the input terminal of the device for manual gain control. The device can only withstand a small voltage at this port.

Figure 5 shows the decrease in gain in 5 dB steps as the input voltage is increased to a maximum of +.430 volts. Figure 6 shows the decrease in gain in 5 dB steps as the input voltage is increased to -.762 volts. With a slight negative voltage applied to the input terminal of -.093 volts, the gain actually increases about 2.7 dB before decreasing with increased negative voltage. The graphs also indicate that the gain reduction versus frequency is fairly constant over a very wide bandwidth.
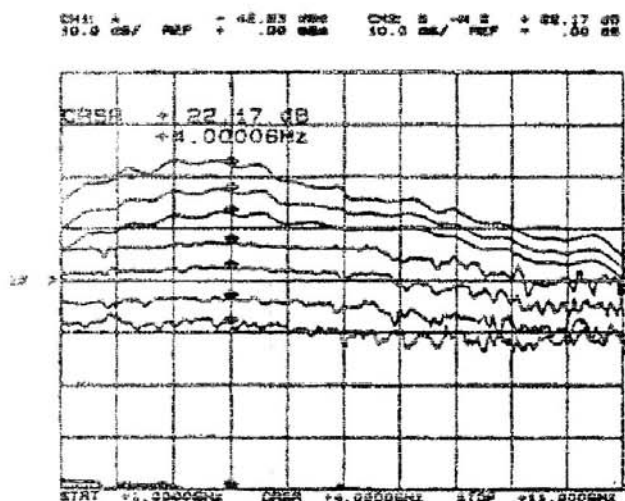
Figure 5 Variable gain operation with positive control voltage
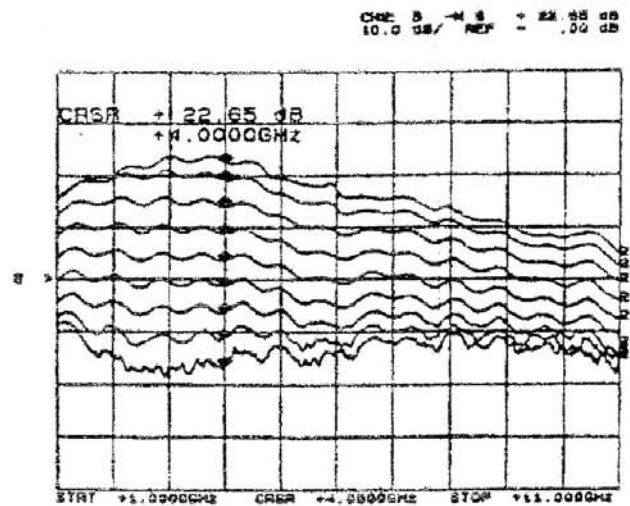
Figure 6. Variable gain operation with negative control voltage

Using a negative control voltage as opposed to a positive voltage for gain control actually is better if lower noise figure at reduced gain is desired. As an example at 4 GHz, when using a negative voltage to decrease the gain by 15 dB, the noise figure increases to 3.9 dB. Using a positive voltage to decrease the gain by 15 dB increases the noise figure to 9.9 dB.

12 GHz ACTIVE MIXER

The MMIC was also tested as an active downconverter for use in DBS applications at 12 GHz. A schematic diagram is shown in Figure 7. The circuit is etched on low cost G-10 dielectric material. The MMIC was configured as a drain or output pumped mixer by injecting a +11 dBm 10.8 GHz local oscillator signal into the output port. The input port is used as the RF port while the IF is coupled out the output port. Quarterwave microstriplines are used at the output port to achieve LO to IF isolation. The mixer achieved a SSB noise figure between 11 and 12 dB and a conversion gain between 1.5 and 2.5 dB over the entire 11750 to 12250 MHz frequency range. The noise figure performance can be improved by several dB by using lower loss material. Considerably better performance is possible at the lower frequencies where dielectric losses are lower and the basic noise figure of the device is a couple of dB lower.
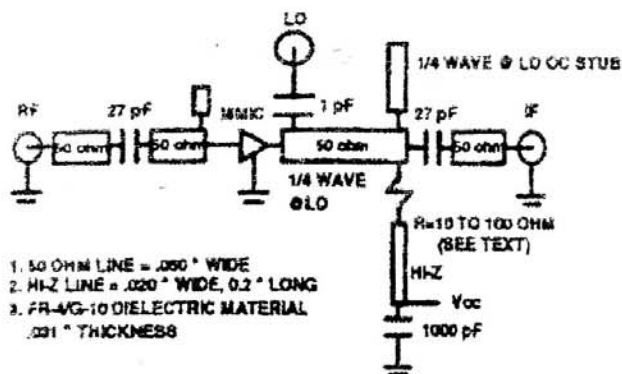
Figure 7.MMIC DBS downconverter (G-10
dielectric material)

... ...asured LO to IF isolation is 17 dB
while ... ...measured LO to RF isolation is 23
dB ... ...F isolation is obtained by
the ... ...ple quarterwave
microstriplines in the output network while
... S12 of the ... ...ntributes to the LO
... isolation ... ...xer.

... ...logy is
... ...entation of low
cost high ... ...ow noise amplifier
designs ... ...applications.
... ...MMICs are
... ...that rival

... ...
... ...ber M. ...ess, D ... ...
Pa... ... 1.5 dB Low N...se ... PHEMT MMIC
Amplifier for low cost 1.5 - 8 GHz commercial
applications", 1993 ... MONOLITHIC CIRCUITS
SYMPOSIUM, PG 15

Chapter K

Demonstration of important propositions

This appendix presents demonstration of important propositions we used in Chapter 3.

K.1   The integral of a Gaussian function over R, Normalization of the Gaussian

Let

$$f_\sigma(t) = e^{-\frac{t^2}{2\sigma^2}}$$

be a generic Gaussian function centered at $t = 0$ and with a standard deviation σ. We want to calculate the normalisation factor A defined as :

$$A = \int_{-\infty}^{\infty} f_\sigma(t)dt$$

such that :

$$G_\sigma(t) = \frac{1}{A} \cdot f_\sigma(t) \qquad \Leftrightarrow \qquad \int_{-\infty}^{\infty} G_\sigma(t)dt = 1$$

where $G_\sigma(t)$ is expected to be exactly the Gaussian function as defined and used previously in this chapter. The factor A is interpreted as the area between the function $f_\sigma(t)$ and the x-axis.

Let consider the square of this area :

$$A^2 = \left[\int_{-\infty}^{\infty} f_\sigma(t)dt \right]^2$$

$$= \left[\int_{-\infty}^{\infty} f_\sigma(x)dx \right] \cdot \left[\int_{-\infty}^{\infty} f_\sigma(y)dy \right]$$

$$= \left[\int_{-\infty}^{\infty} e^{-\frac{x^2}{2\sigma^2}} dx \right] \cdot \left[\int_{-\infty}^{\infty} e^{-\frac{y^2}{2\sigma^2}} dy \right]$$

$$= \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} e^{-\frac{(x^2+y^2)}{2\sigma^2}} dx \cdot dy$$

where x, y and t are three independent variables and by applying lastly the Fubini theorem. Transforming the Cartesian coordinates into polar coordinates leads to the following substitutions :

$$\left. \begin{array}{l} x = r\cos(\theta) \\ y = r\sin(\theta) \end{array} \right\} \qquad \Leftrightarrow \qquad \left\{ \begin{array}{ll} \sqrt{x^2+y^2} & = r \\ dx \cdot dy & = r \cdot dr \cdot d\theta \end{array} \right.$$

We obtain :

$$A^2 = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} e^{-\frac{(x^2+y^2)}{2\sigma^2}} dx \cdot dy$$

$$= \int_0^{\infty} \int_0^{2\pi} e^{-\frac{r^2}{2\sigma^2}} \cdot r \cdot dr \cdot d\theta$$

$$= \left[\int_0^{\infty} e^{-\frac{r^2}{2\sigma^2}} \cdot r \cdot dr \right] \cdot \left[\int_0^{2\pi} d\theta \right]$$

$$= 2\pi \cdot \int_0^{\infty} e^{-\frac{r^2}{2\sigma^2}} \cdot r \cdot dr$$

By applying the substitution $u = \frac{r^2}{2}$ and $du = r \cdot dr$, we have :

$$
\begin{aligned}
A^2 &= 2\pi \cdot \int_0^\infty e^{-\frac{r^2}{2\sigma^2}} \cdot r \cdot dr \\[2ex]
&= 2\pi \cdot \int_0^\infty e^{-\frac{u^2}{\sigma^2}} \cdot du \\[2ex]
&= -2\pi\sigma^2 \cdot \underbrace{\left[e^{-\frac{u^2}{\sigma^2}} \right]_0^\infty}_{-1} \\[2ex]
&= 2\pi\sigma^2
\end{aligned}
$$

This gives finally $A = \sqrt{2\pi}\sigma$ and

$$
G_\sigma(t) = \frac{1}{A} \cdot f_\sigma(t) = \frac{1}{\sqrt{2\pi}\sigma} \cdot e^{-\frac{t^2}{2\sigma^2}}
$$

This proves the theorem.

K.2   The integral of a Gaussian function, General case

It can be proved that the Gaussian function integral cannot be expressed in an analytical way; the case of the normalization seen above is the only particular case where the coordinate change allows the calculation of this integration. However, there are analytical expressions that approximate with a very good accuracy this integral.

Let

$$
f_\lambda(t) = e^{-\frac{t^2}{\lambda}}
$$

be a generic Gaussian function. By doing the adequate substitution, we have :

$$
\begin{aligned}
\int_0^x f_\lambda(t)dt &= \int_0^x e^{-\frac{t^2}{\lambda}} dt \\[2ex]
&= \int_0^{\frac{x}{\sqrt{\lambda}}} e^{-u^2} \cdot \sqrt{\lambda} \cdot du \\[2ex]
&= \sqrt{\lambda} \cdot \int_0^{\frac{x}{\sqrt{\lambda}}} e^{-u^2} \cdot du
\end{aligned}
$$

where

$$u^2 = \frac{t^2}{\lambda}$$

$$u = \frac{t}{\sqrt{\lambda}}$$

$$du = \frac{dt}{\sqrt{\lambda}} \qquad \Leftrightarrow \qquad dt = \sqrt{\lambda} \cdot du$$

In the article [91], Chu demonstrated the following approximation :

$$\mathrm{erf}(x) = \frac{2}{\sqrt{\pi}} \cdot \int_0^x e^{-u^2} \cdot du \approx \sqrt{1 - e^{-\frac{4x^2}{\pi}}}$$

Assuming the approximation is an equality, we can write :

$$\int_0^x e^{-u^2} \cdot du = \frac{\sqrt{\pi}}{2} \cdot \sqrt{1 - e^{-\frac{4x^2}{\pi}}} = I(x)$$

From previous development :

$$\int_0^x f_\lambda(t)dt = \int_0^x e^{-\frac{t^2}{\lambda}} dt$$

$$= \sqrt{\lambda} \cdot \int_0^{\frac{x}{\sqrt{\lambda}}} e^{-u^2} \cdot du$$

$$= \sqrt{\lambda} \cdot I\left(\frac{x}{\sqrt{\lambda}}\right)$$

$$= \sqrt{\frac{\lambda\pi}{4}} \cdot \sqrt{1 - e^{-\frac{4x^2}{\lambda\pi}}}$$

This results can be used as an equality in this chapter since the precision is about $3 \permil$ according to the Matlab simulation in Figure K.1 below (see Appendix A.2.2 for the Matlab code).
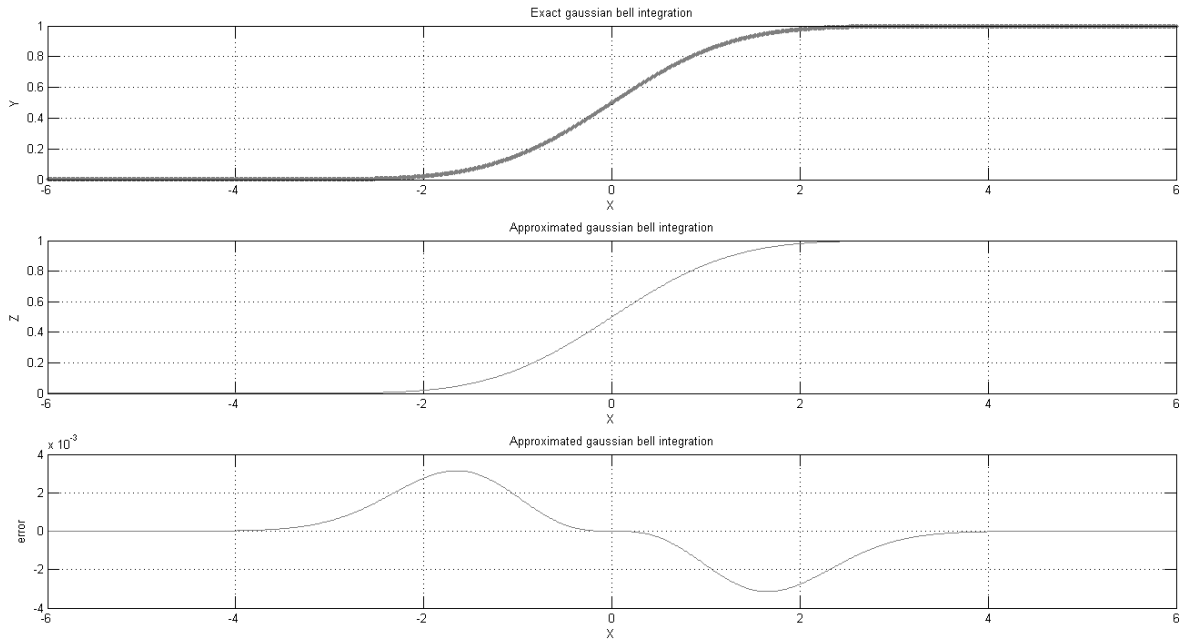
Figure K.1: Numeric estimation of the error on Chu estimation.

K.3   The Convolution theorem

Let

$$z(t) = y(t) \cdot x(t) \qquad \forall t \in \mathbf{R}$$

be a product of two real functions in the time domain. We thus have :

$$Z(f) = \int_{-\infty}^{\infty} y(t) \cdot x(t) \cdot e^{-j2\pi ft} dt$$

By replacing $y(t)$ with the inverse Fourier transform of $Y(\hat{f})$, where $\hat{f}$ is another frequency variable that is independent of f, we have :

$$
\begin{aligned}
Z(f) &= \int_{-\infty}^{\infty} \underbrace{\left[\int_{-\infty}^{\infty} Y(\hat{f}) \cdot e^{j2\pi \hat{f} t} d\hat{f} \right]}_{y(t)} \cdot x(t) \cdot e^{-j2\pi ft} dt \\
&= \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} Y(\hat{f}) \cdot e^{j2\pi \hat{f} t} \cdot x(t) \cdot e^{-j2\pi ft} d\hat{f} \cdot dt \\
&= \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} Y(\hat{f}) \cdot x(t) \cdot e^{-j2\pi (f-\hat{f})t} d\hat{f} \cdot dt
\end{aligned}
$$

By exchanging the order of the integration, we have :

$$Z(f) = \int_{-\infty}^{\infty} Y(\hat{f}) \cdot \underbrace{\left[\int_{-\infty}^{\infty} x(t) \cdot e^{-j2\pi(f-\hat{f})t} dt \right]}_{X(f-\hat{f})} d\hat{f}$$

$$= \int_{-\infty}^{\infty} Y(\hat{f}) \cdot X(f - \hat{f}) d\hat{f}$$

$$= Y(f) \star X(f)$$

This proves the theorem.

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Glossary

This glosary gives the meaning of the abbreviations used in this work:

AC : Alternating Current

ADC : Analog to Digital Converter

ADS : Advanced Design System (a software from Agilent)

AGC : Automatic Gain Control

BALUN : BALanced/UNbalanced transformer

BER : Bit Error Rate

BPPM : Binary Pulse Position Modulation

BW : Band Width

cascode : *cas*cade of cath*ode*, a way to cascade transistors or vacuum tubes

CDMA : Code-Division Multiple Access

CMOS : Complementary Metal Oxide Semiconductor

DAC : Digital to Analog Converter

dB : decibel

dBi : antenna gain expressed in dB where *i* stands for *isotropic*

dBm : A power expressed in dB where 0 dBm correspond to 1 mW

DC : Direct Current

DRAM : Dynamic Random Access Memory

DSP : Digital Signal Processing

DUT : Devive Under Test

EIRP : Equivalent Isotropically Radiated Power

EPFL : Ecole Polytechnique Fédérale de Lausanne

ESD : Electro Static Discharge

FCC : Federal Communications Commission

FET : Field Effect Transistor

FFT : Fast Fourier Transform

FM : Frequency Modulation

FPGA : Field Programmable Gate Array

GMM : Gaussian Mixture Model

HEMT : High Electron Mobility Transistor

IC : Integrated Circuit

IF : Intermediate Frequency

IFFT : Inverse Fast Fourier Transform

IQML : Iterative Quadratic Maximum Likelihood estimation algorithm

IR : Impulse Radio

ISI : Inter-Symbol Interference

I/Q : In-phase/Quadrature

LC : a resonant circuit with inductor and capacitor (L stands for Lenz)

LCA : Laboratoire pour les Communications informatiques et leurs Applications (EPFL)

LEMA : Laboratoire d'Electro-Magnétisme et d'Acoustique (EPFL)

LNA : Low Noise Amplifier

LO : Local Oscillator

LOS : Line Of Sight

LSB : Least Significant Bit

LVDCI : Low Voltage Digitally Controlled Impedance

MCA : Middleton Class A Model

mHEMT : metamorphic High Electron Mobility Transistor

MICS : Mobile Information and Communication Systems

MMIC : Monolithic Microwave Integrated Circuit

MOS : Metal Oxide Semiconductor

MOST : Metal Oxide Semiconductor Transistor

MSB : Most Significant Bit

MUI : Multi User Interference

NF : Noise Figure

NLOS : Non Line Of Sight

NMOS : N-channel MOS

OFDM : Orthogonal Frequency Division Multiplexing

OOK : On-Off Keying

PCB : Printed Circuit Board

PECL : Positive Emitter Coupled Logic

PER : Packet Error Rate

pHEMT : pseudo High Electron Mobility Transistor

PID : Power Independent Detection

PLL : Phase Locked Loop

PMOS : P-channel MOS

PQML : Pseudo-Quadratic Maximum Likelihood estimation algorithm

PRP : Pulse Repetition Period

PSK : Phase-Shift Keying

Q : Quality factor

QPSK : Quadrature Phase-Shift Keying

RF : Radio Frequency

RFC : Radio Frequency Choke

SMA : Sub Miniature Version A (a type of RF connector)

SMD : Surface Mounted Device

SNR : Signal to Noise Ratio

SRAM : Static Random Access Memory

SRD : Step Recovery Diode

TH : Time Hopping

THS : Time Hopping Sequence

UWB : Ultra Wide Band

VCO : Voltage Controlled Oscillator

VGA : Variable Gain Amplifier

Curriculum Vitæ

James Colli-Vignarelli was born in Geneva, Switzerland, in 1978. He received the B.Sc. degree in Mathematics from University of Geneva (Switzerland) in 2002. He received the M.Sc. degree in Electrical Engineering from Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland, in 2007. In the Summer of 2006, he started an internship at EPFL in the RFIC group with Dr. Catherine Dehollain. In February 2008, he joined the RFIC group (STI) and the Laboratory for Computer Communication and Applications (LCA) at EPFL, Doctoral School in Microsystems and Microelectronics (EDMI), and started his PhD thesis under the supervision of Dr. Catherine Dehollain and Pr. Jean-Yves Le Boudec. There, he participated to the National Center of Competence in Research on Mobile Information and Communication Systems (NCCR-MICS). He was a teaching assistant for the HF and VHF circuits and Techniques I and II course.

He was awarded a Silver Leaf Award (paper in the 20th centile) at the 2010 IEEE Ph.D. Research in Microelectronics and Electronics Conference (PRIME 2010) for the paper "A Discrete-Components Impulse-Radio UWB Low-Noise Amplifier with Voltage Controlled-Gain" and a Gold Leaf Award (paper in the 10th centile) at the 2011 IEEE Ph.D. Research in Microelectronics and Electronics Conference (PRIME 2011) for the paper "A Discrete-Components Impulse-Radio UWB Receiver with I/Q Demodulation". He also receives a best demo award at the 2006 MICS Scientific Conference for the demo "An Impulse-Radio Ultra-Wide Band Testbed with Interference".

His current research interests include RF CMOS circuit design and architecture for UWB applications.

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