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Top-down fabrication of very-high density vertically stacked silicon nanowire arrays with low temperature budget

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ABSTRACT

We report on a top-down complementary metal oxide semiconductor (CMOS) compatible fabrication method of ultra-high density Si nanowire (SiNW) arrays using a time multiplexed alternating process (TMAP) with low temperature budget. The flexibility of the fabrication methodology is demonstrated for curved and straight SiNW arrays with different shapes and levels. Ultra-high density SiNW arrays with round or rhombic cross-sections diameters as low as 10 nm are demonstrated for vertical and horizontal spacing of 60 nm. The uniqueness of the technique, which achieves several advantages such as bulk-Si processing, low-thermal budget, and wide process window makes this fabrication method suitable for a very broad range of applications such as nano-electro-mechanical systems (NEMS), nano-electronics and bio-sensing.

1. Introduction

Recently, there has been a huge interest in the physical properties of Si nanowires (SiNW) due to their excellent mechanical [1] and electrical properties [2]. The one dimensionality of SiNWs makes these structures excellent candidates for sensing [3] as well as channels for solid-state field effect transistor (FET) devices [4]. Thus, reliable and inexpensive top-down fabrication methods of SiNWs are of huge interest for several applications. In this respect, stacking multiple layers of nanowires is emerging as potentially powerful approach for building high density systems [5].

One method, proposed by Javey et al. [6], relies on the iteration of contact printing and metallization techniques to stack several layers of nanowire-based circuits. The key advantage of the technique is that it can be applied to any type of nanowires grown by bottom-up approaches and it can be applied to any kind of substrates, including flexible plastics. However, the throughput of the method is limited by the number of steps and the use of different substrates for nanowire growth and pattern transfer. Another method to produce vertically-stacked SiNWs is based on Si/SiGe epitaxy and has been reported by several groups [7–9]. The epitaxial method allows for very tight control of the film thickness and therefore, of nanowire dimensions; however, it lacks fabrication compatibility with conventional CMOS processes. Indeed, the number of stacked SiNW levels on a wafer is fixed by the epitaxial layers and careful control on the stress-build up is required in order to obtain reproducible electrical characteristics [9]. A third method recently published [10,11] leverage on the formation of $SiO_2 - Si_3N_4$ dielectric cavities in which ultradense polysilicon nanowires can be conformally grown and etched. In particular, in [11] low horizontal pitch of about 150 nm and a vertical pitch of 50 nm are demonstrated. Another method uses time multiplexed alternating process (TMAP) etching, also known as deep reactive ion etching (DRIE) or Bosch process in combination with high temperature oxidation to form vertical stacks of SiNWs. Several groups, including the authors, have reported on variations of the TMAP-DRIE process for the fabrication of vertically stacked SiNWs arrays for micro-electro-mechanical-systems MEMS [12] and FET devices [13,14]. Nevertheless, the SiNW fabrication typically relies on thermal oxidation and/or hydrogen annealing techniques [7,8,13,14] which increase the temperature budget.

This work focuses on the top-down fabrication of ultra-high density vertically-stacked SiNWs arrays with sub-50 nm diameter from a single etching step with low thermal budget, without the need for thermal oxidation or hydrogen annealing techniques. For instance, since all processing steps are performed at room temperature,this feature can be used in CMOS post-processing or for flexible polymeric substrates [15], for which temperatures lower than 200 °C are needed. Very-high horizontal and vertical SiNWs density is demonstrated for curved and straight geometries with edge-to-edge SiNW spacings down to 60 nm for a cross-sectional density of $2 \times 10^{10}/cm^2$. The etching recipes are optimized to obtain either round- or rhombic-shaped SiNWs. Si fins are also fabricated.

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Additionally, the number of vertically placed SiNWs in-a-stack can be easily tuned from 1 to 6.

In Section 2 the typical fabrication steps are summarized. Section 3 details the TMAP physics of etching at the nano-scale and the process developments required for optimization of the different vertically-stacked SiNW arrays designs. In Section 4 we discuss on the obtained fabricated structures. Finally, in Section 5 we draw the conclusions.

2. Device fabrication

The process starts with a bulk-Si wafer. The wafer is dipped for 60 s in tetramethylammonium hydroxide (TMAH) for priming the Si surface for hydrogen silsesquioxane (HSQ) coating, after it is dehydrated on a hot plate at 180 °C for 10 min. A 150 nm thick HSQ layer is spin coated at 4000 rpm. Then single lines (Fig. 1a) and dense arrays (Fig. 1b) are patterned using Vistec EBPG5000 e-beam lithography system. Typical HSQ lines are written with 50 nm width with line distance from 50 nm to 500 nm. After exposure the wafer is developed in TMAH and rinsed in water, acetone and IPA, in order to lower surface tension and avoid stiction. After the exposure the wafers are processed in Alcatel AMS 200 DSE Fluorine etcher using different TMAP recipes. Four process parameters are tuned; flow rate, step time of SF_6 and C_4F_8 gases and one design parameter, the distance of the nanowire to the sidewall and pitch for the arrays. In particular, round (see Fig. 1c and d) and rhombic (see Fig. 1e and f) cross-sections can be obtained using optimized recipes, as will be explained in Section 4.

3. Nano-scale etching

The presented work is based on time multiplexed alternating process (TMAP) [16], also known as DRIE or Bosch process. The more advanced etching recipes presented in this work target scallops dimension between 20 and 30 nm, to allow the formation of stacks of nanowires from mask line widths of 50 nm and below. The etching rate and profile are mainly determined by three key phenomena:

- Loading effect [17].
- Microloading effect [17,18].
- Ion induced defluorination of the passivation film (IIDPF) [19,20].

A quick summary of design and process parameters dependencies with these physical phenomena is given in Table 1. More details are explained in the following paragraphs. The loading effect [17] is the decrease of the etching rate of the reactive ion etching due to the increased area exposed to the SF_6 plasma. In our test structures more than 90% of total wafer area is exposed. In case the pattern is required to cover more than 50% of the total wafer area then the loading effect cannot be used as part of the strategy to lower the etch rate. A special case of the loading is the microloading effect. The microloading effect is the etching rate degradation due to the high density of a pattern, the main mechanism for microloading is, etchant depletion [17,18]. Etchant depletion happens inside an etching trench and it is due to the difficulty for the etchant species to be replenished, as the etching opening reducing. The smaller the nanowire pitch, the lower the etch rate. Microloading can be controlled by flow rate. Thus, reducing the flow rate it reduces the rate at which the etchants are replenished leading to etchant depletion, magnifying the microloading effect. The TMAP consists of the alternation of etching and passivation steps. At the beginning of each etching cycle the plasma needs to remove the passivation at the bottom, deposited at the passivation cycle. The time needed for the passivation removal is a function of its thickness, which in turns is controlled by C_4F_8 flow rate and time step. The time needed to clear the passivation is very short in standard TMAP processes. However, this effect is not negligible for nano-scale etching, as the passivation etching time becomes comparable with the total SF_6 time step. Similarly, thicker passivation films reduce the Si etching rate [16] since a larger fraction of the SF_6 step is needed to remove the passivation. To keep the etching rate low, the time step and flow rate of SF_6 needs to be kept as low as possible. Thin passivation layers should be used in order to avoid micrograss formation [16]. The downside of very thin passivation layers is that ion induced defluorination, the ion bombardment assisted desorption of fluoride from the carbofluride film, creates chemical species in the passivation film that etches away the underlying Si [19,20]. The favorable aspect of low SF_6 flow rate is reduced roughness due to higher local plasma uniformity [18]. This effect can be exploited to affect the cross-section of the nanowires with the following mechanism: (1) The diameter of the nanowire is reduced isotropically (2) Sharp points and low dimension features are removed first, creating an elliptical shape.

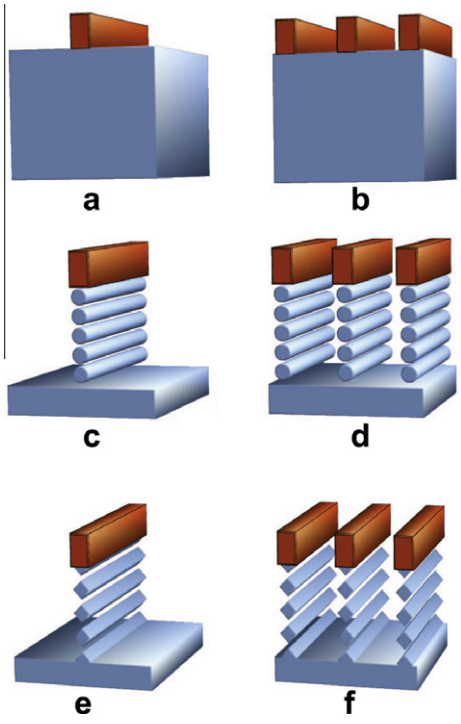


Fig. 1. Fabrication flow. (a) Single HSQ line patterned on Si substrate. Typical HSQ width is 50 nm. (b) Dense HSQ line arrays. (c and d) After etching with recipe (2) as reported in Table 3. (e and f) After etching with recipe (3) as reported in Table 3.

4. Results and discussion

The etching of vertically stacked SiNW arrays is investigated for the following designs:

- Straight-line nanowire stacks.
- Curved-line nanowire stacks.
- Ultra-high density arrays.

Process development has been carried out by parameterizing individual device design in order achieve a high repeatability and fabrication yield. In Table 2 the design parameters are listed. In the following sections each device type is addressed separately.

Table 1
Experimental design and process parameter dependencies with the main physical phenomena affecting the nano-scale TMAP process.

Phenomena	Design variation	Process variation	Common problems	Effect
Loading [17]	Reduce exposed area	N/A	N/A	Reduced etching rate
Microloading [17,18]	Denser patterns	Reduce SF_6 (1) Flow rate, (2) Time step	(1) Micrograss [16], (2) Formation of fins instead of SiNWs	(1) Reduced etching rate, (2) Reduced roughness [18]
IIDPF [19,20]	N/A	Reduce C_4F_8 (1) Flow rate, (2) Time step	Complete etched away structures	Alter cross section from rhombic to elliptical

Table 2
Mask design parameters for straight lines, curved lines and dense array nanowire structures.

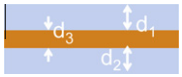
Mask design	Top view	d_1	d_2	d_3
Straight-line nanowire stacks		Trench opening: 100, 200, 500 nm	Trench opening: 100, 200, 500 nm	Nanowire width: 50, 100, 150 nm
Curved-line nanowire stacks		Trench opening: 200 nm	Nanowire width: 50 nm	Outer diameter: 250, 450, 850 nm
Ultra-high density arrays		Pitch: 50, 60, 75, 100, 200 nm	Nanowire width: 50 nm	N/A

Table 3
Recipes overview optimized for different mask designs. The substrate temperature is kept at 20° C.

Process recipes	SF_6 (cm^3/min)	SF_6 (s)	C_4F_8 (cm^3/min)	C_4F_8 (s)	Mask design (see Table 2)
(1)	300	3	150	1	Straight-line nanowire stacks
(2)	200	2.5	150	1	Curved-line nanowire stacks, ultra-dense arrays (d_1 = 75, 100, 200 nm)
(3)	200	2.5	100	1	Ultra-dense arrays (d_1 = 50, 60, 75 nm)

4.1. Straight-line nanowire stacks

Lines widths of 50 nm, 100 nm, 150 nm are written with lengths 100 nm, 200 nm, 0.5 μm, 1 μm, 2 μm. The patterns are placed inside a trench to reduce and control the etching rate through microloading. Trench opening of 100 nm, 200 nm and 500 nm are designed. Flow rate used are 300 cm^3/min for SF_6 and 150 cm^3/min for C_4F_8 with step times have 3 s and 1 s, respectively. The process can achieve very good repeatability, with a wire diameter variation of less than 10 nm. The smallest fabricated structures for the straight-line design are nanowires obtained from 50 nm mask line width, 200 nm trench opening and of independent length. In Fig. 2a and b a stack of six nanowires is shown in bird's eye view and cross-section, respectively. The importance of the trench opening dimension is established by the observation that, for 500 nm trench opening nanowires are not formed (see Fig. 2c) while for 200 nm trench opening, while using the same process, 50 nm nanowires are fabricated (as shown in Fig. 2b). The trench opening etching rate dependence can be explained by the microloading effect causing local etchant depletion.

4.2. Curved-line nanowire stacks

Curved line nanowires are patterned with a line width of 50 nm. The patterns are carved into Si as for the case of straight-line nanowires, as depicted in Fig. 3a. The trench opening is kept constant at 200 nm. The pattern consists of semi-circles connected in a serpentine fashion. Three circle diameters are explored: 200 nm, 400 nm, and 800 nm, as shown in Fig. 3c. In Fig. 3b a bird's eye view of a stack of three nanowires with 200 nm circle diameter encased in Pt is shown.

A drawback of the design is that the trench opening cannot be kept constant in case the circle diameter is double the trench opening, as can been seen from Fig. 3c by comparing the designs with 200 nm and 800 nm diameter. Etching rate is faster where trench opening is wider, again due to microloading effect. To reduce the

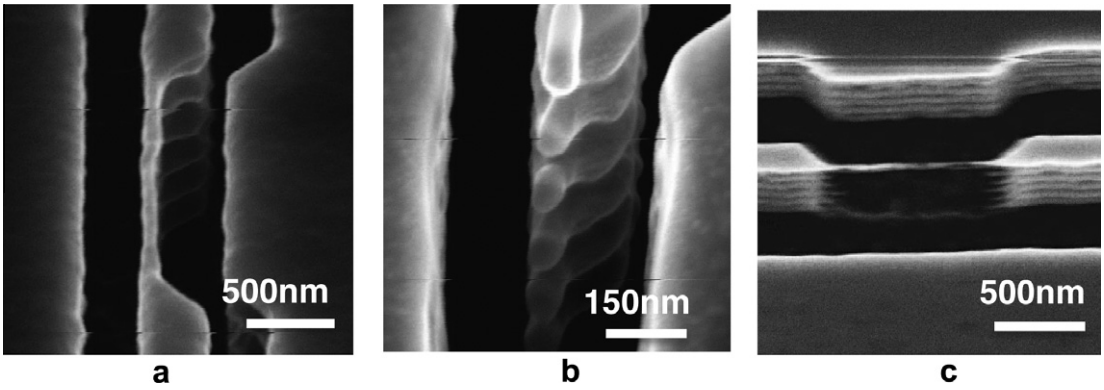


Fig. 2. Vertically stacked 50 nm diameter for straight-line nanowires carved inside a 200 nm narrow trench. (a) Bird's eye view. (b) Cross-section. The etching parameters are 300 cm^3/min and 3 s for SF_6, 150 cm^3/min and 1 s for C_4F_8. (c) Tilted view of a straight-line nanowire stack carved in a 500 nm wide trench. Due to a reduced etchant depletion effect, all the nanowires but the top one are overetched.

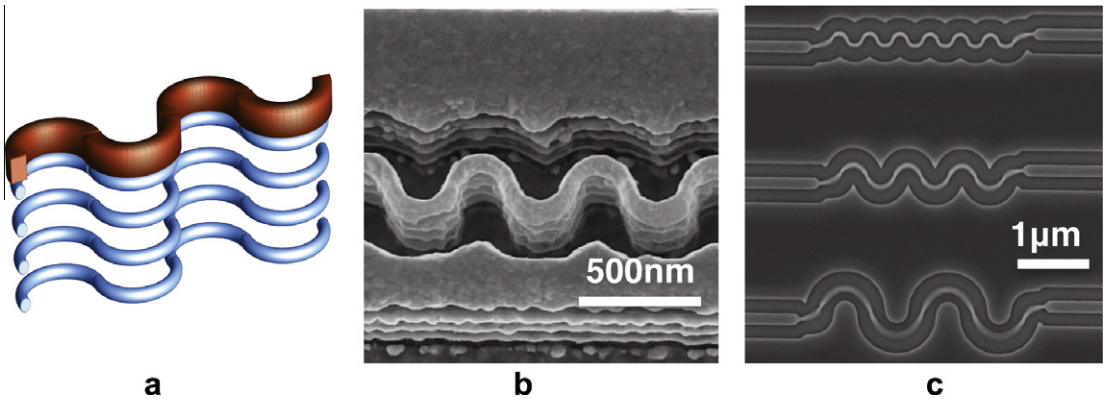


Fig. 3. (a) Concept view of vertically-stacked curved nanowires. Etching parameters are 200 cm^3/min and 2.5 s for SF_6, 150 cm^3/min and 1 s for C_4F_8. (b) Bird's eye view of the nanowire stack covered by a 50 nm thick Pt layer for conformal PtSi silicide formation. (c) Top view of the three curved nanowire design.

etching rate created by the irregular trench openings a reduced flow rate recipe is used. Flow rate of 200 cm^3/min for SF_6 and 150 cm^3/min for C_4F_8 were used where step times are 2.5 s and 1 s, respectively.

4.3. Ultra-high density arrays

Dense array designs for 50 nm line widths and pitches ranging from 100 nm to 300 nm were explored for lengths from 100 nm to 50 μm. The array pattern was etched faster than the reference case of the straight line nanowires explained in Section 4.1. This could be due to the vertical nanowire separation that alters the etchants flow once the nanowire is released as illustrated in Fig. 4, countering this effect is microloading that slows down etching rate the denser the array gets. Two recipes are selected: the first is optimized for 200 nm trench opening and it uses 200 cm^3/min for SF_6 in 2.5 s time steps and 150 cm^3/min for C_4F_8 in 1 s time steps. In Fig. 5 a stack of 3 nanowires, which is fabricated with the first recipe, is shown in bird's eye view and cross-section. Average diameter of the SiNWs is 30 nm and pitch is 200 nm. The length of the nanowires is 1 μm. The same recipe is used to fabricate a stack of six round SiNWs with pitch of 75 nm and 300 nm long (Fig. 6a) and SiNW diameters of 20 nm (Fig. 6b), producing repeatable SiNW structures with minimal diameter variation. The second recipe is designed for denser arrays and uses 200 cm^3/min for SF_6 for 2.5 s and 100 cm^3/min for C_4F_8 for 1 s. A stack of six rhombic SiNWs with pitch of 75 nm (Fig. 7a) is fabri-

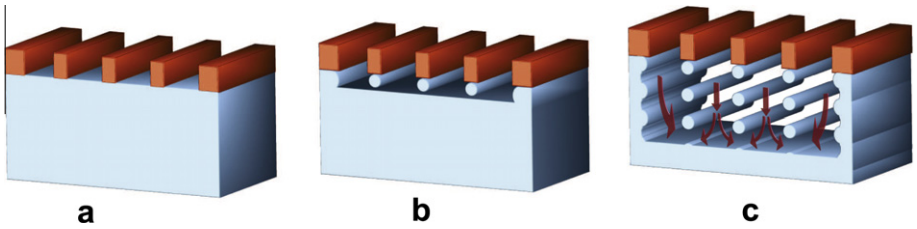


Fig. 4. (a) Dense array before etching. (b) Nanowire formation at etching time step t_1. (c) After $4 \cdot t_1$ 3 levels of SiNWs are obtained and a fourth one begins to form. The arrows indicate the plasma flow directions.

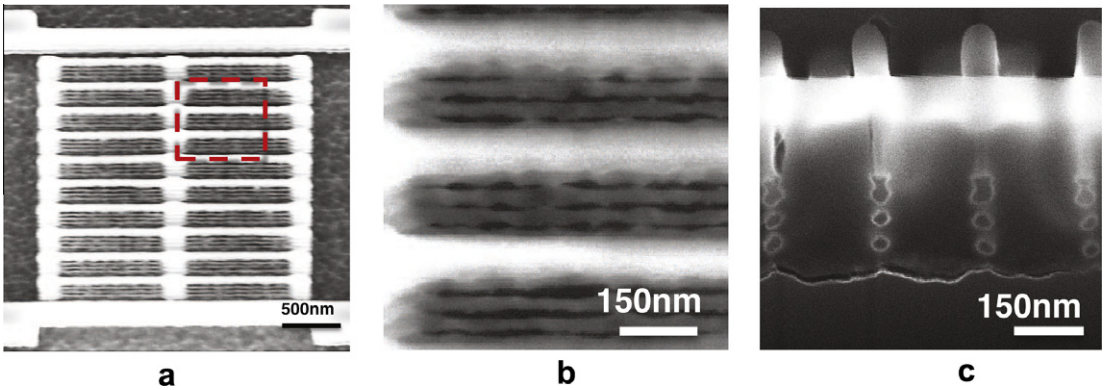


Fig. 5. Examples of nanowire arrays with 200 nm pitch, μm length and 30 nm average diameter. Etching parameters are 200 cm^3/min and 2.5 s for SF_6, 150 cm^3/min and 1 s for C_4F_8. (a) Bird's eye view. (b) High magnification showing the vertical stacks. (c) Cross-section of the vertically stacked array.

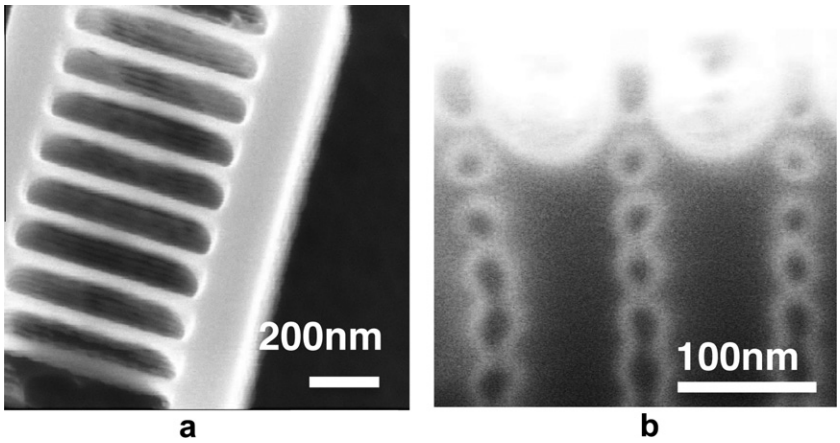


Fig. 6. Examples of dense nanowire arrays. Etching parameters are 200 cm^3/min and 2.5 s for SF_6, 150 cm^3/min and 1 s for C_4F_8. (a) Bird's eye view of a 550 nm long wires with 200 nm pitch cut with FIB. (b) Cross-section for an array with 300 nm long wires and 100 nm pitch. The average nanowire diameter is 25 nm.

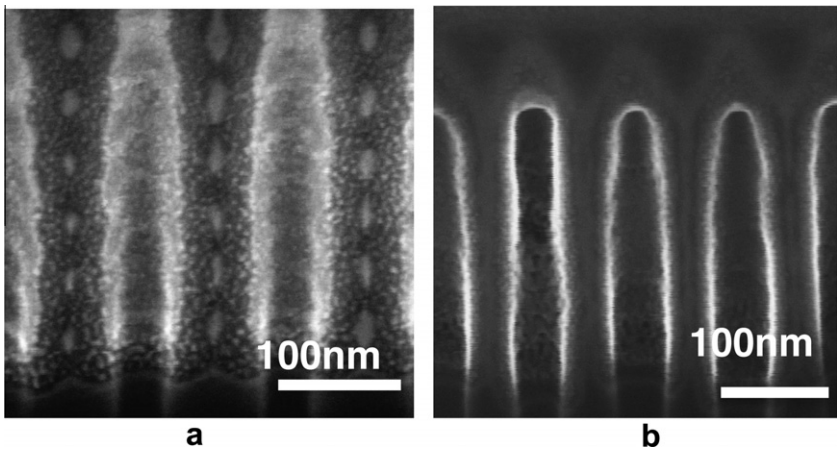


Fig. 7. Examples of dense nanowire arrays. Etching parameters are 200 cm^3/min and 2.5 s for SF_6, 100 cm^3/min and 1 s for C_4F_8. (a) Cross-section showing 18 SiNWs (3 parallel stacks with 6 levels each) having 75 nm horizontal spacing and 60 nm vertical spacing, with rhombic cross-sections. Average diameter is 25 nm. (b) Cross-section showing scalloped fins for 50 nm horizontal spacing (dimension d_1 for dense array design as in Table 2).

cated for 75 nm horizontal and 60 nm vertical spacings. Typical SiNW diameter is 10 nm with lengths of up to 550 nm, yet diameter variability is larger compared to earlier examples. Higher density arrays lead to the formation of scalloped fins, as shown in Fig. 7b.

5. Conclusions

Vertical stacks of SiNWs with round or rhombic shapes of diameters down to 10 nm are fabricated using a simple TMAP process in

bulk Si with very-low thermal budget. To our knowledge, the cross-sectional nanowire density of $2 \times 10^{10}/cm^2$ result is among the highest for top-down fabricated SiNWs arrays reported in the literature. Moreover, SiNWs arrays with lengths from 50 nm up to 1 μm and horizontal inter-wire spacing ranging between 50 nm and 200 nm are demonstrated. The technique is presented in terms of its potential use for the fabrication of a broad range of nano-scale devices, from NEMS, to nano-electronics and sensing.

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