A 0.24-nJ/bit Super-Regenerative Pulsed UWB Receiver in 0.18-μm CMOS

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***Abstract*—This paper describes a receiver system design for impulse-radio ultra-wideband (IR-UWB) that operates at two carrier frequencies—3.494 and 3.993 GHz—with a 10-Mbps data rate. To reduce the power consumption of the front-end amplifiers, a super-regenerative architecture is used. An integrated circuit, implemented in a CMOS 0.18-μm technology and operating with a 1.5-V power supply, exhibits energy consumption of 0.24 nJ/bit with a measured sensitivity of -66 and -61 dBm at 3.494 and 3.993 GHz, respectively, with a BER of 10^{-3}. Also included on the integrated circuit is an automatic tuning circuit based on a digital phase-locked loop that is used to set the resonant frequency of the super-regenerative block.**

***Index Terms*—Digital phase-locked loop, oscillator, receiver architecture, super-regenerative system, ultra-wideband communication, wireless sensor network.**

I. Introduction

ULTRA-WIDEBAND (UWB) is a wireless technology that sends modulated signals over a relatively wide bandwidth, typically at least 500 MHz. The resulting spread spectrum allows more robust transmission in the presence of multipath, jamming, and other phenomena that are challenging to conventional narrowband technologies [1], [2]. Moreover, for low bit rates that are compatible with sensor networks, impulse-radio ultra-wideband (IR-UWB) technology can be implemented in CMOS technology with low power dissipation.

A well-known circuit technique that dates from the early 20th century, known as the super-regenerative principle [3], [4], allows reception of short carrier pulses with very low power dissipation, and is well-suited for demodulation of IR-UWB signals. This technique is based on the use of an LC-VCO that is turned on briefly during each unit interval. If an input carrier pulse—typically of duration of only a few cycles—is present, the VCO will start up quickly. If a carrier pulse is not present, then the VCO will take longer to start up. By detecting the envelope of the VCO output and comparing the envelope peak with an appropriate reference, the bit sequence can be detected with a reasonable bit error rate. The graph illustrating the above principle is shown in Fig. 1. The first waveform in Fig. 1 indicates the time-varying bias current $I(t)$ of the core oscillator where the peak current $I_{\rm bias}$ is greater than the critical current to start oscillation. The second waveform is the time-varying effective conductance ($G_0 + G_m(t)$) seen by the resonant circuit (LC) where G_0 is the resonant element loss and $G_m(t)$ is the time-varying negative conductance. The third waveform indicates the incoming RF pulse $V_{\rm rf}(t)$ centered around the *LC* resonant frequency and the fourth waveform indicates the envelope variation $V_{\rm en}(t)$. As seen in the fourth waveform due to the RF pulse, the core oscillator is forced to start immediately and reaches a higher amplitude in comparison to the state when the oscillator is allowed to start due to noise. The sampled value $V_{\rm peak}(t)$ is compared with a reference voltage to indicate the presence/absence of a pulse.

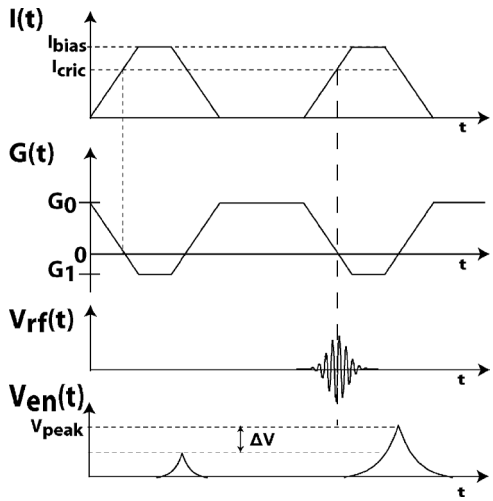

Fig. 1. Graph showing super-regenerative principle.

IR-UWB signals are transmitted in the 3.1–10.6-GHz frequency spectrum, which are further divided into numerous subbands [5]. In order to demodulate IR-UWB signals using a super-regenerative architecture, the VCO must be tuned to the desired subband. In this paper, we describe a super-regenerative IR-UWB receiver realized in a 0.18-μm CMOS technology that accommodates two carrier frequencies—3.494 and 3.993 GHz—using a digital phase-locked loop (DPLL) for tuning. A description of the overall receiver and the design of each block are given in Section II, measurement results are given in Section III, and conclusions are given in Section IV.

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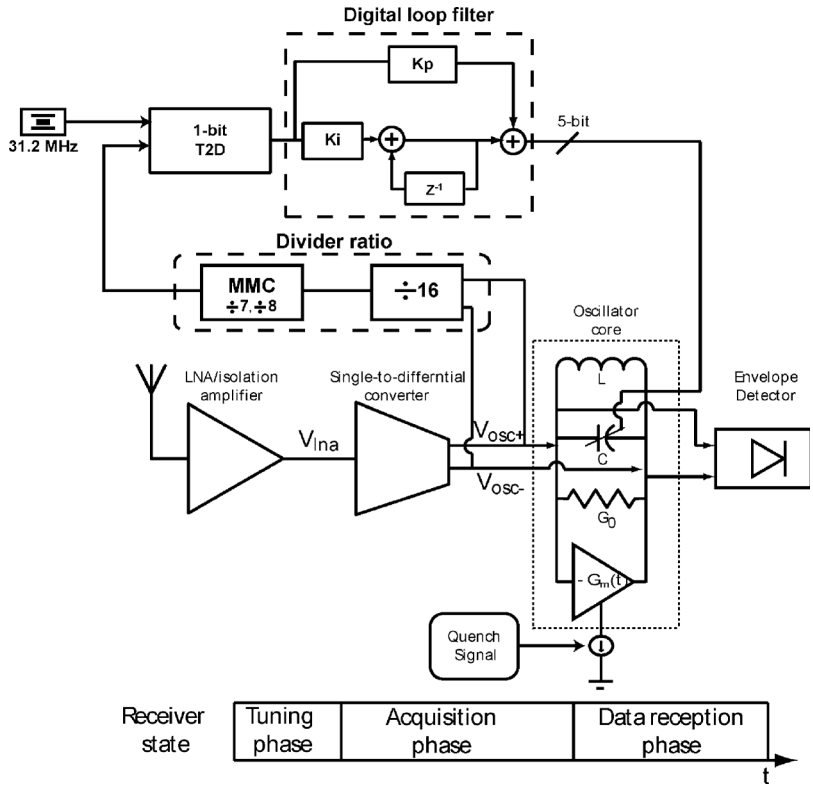

Fig. 2. IR-UWB SR front-end implemented in CMOS 0.18-μm technology.

II. Circuit Description

A. Receiver Architecture

The IR-UWB receiver block diagram is shown in Fig. 2. The architecture consists of an initial gain/isolation stage, a single-to-differential converter, a core oscillator whose bias current is controlled by a "quench" signal, an envelope detector, and a comparator. Applying a single-ended signal to the chip and performing the conversion to differential signaling gives a favorable noise figure compared to using an external balun. These blocks are designed to have a relatively wide bandwidth that includes both carrier frequencies. In addition to improving the overall noise figure, using two stages before the oscillator structure provides isolation, thus preventing reradiation of the signal back to the antenna. As shown in Fig. 2, the differential output of the converter is injected into the resonant core. The *LC* tank circuit is tuned via a fixed capacitor for coarse tuning and a digitally switched capacitor structure for fine tuning. The fine tuning is performed with a DPLL, which will be described later in this section. The envelope variation at the oscillator structure output is detected using the envelope detector and appropriately latched to either a logic "1" or "0" using the comparator/regenerative latch.

1) Quench Signal Shape: As the received input pulse is detected based on the start-up time of the core oscillator output, it is to be periodically taken in and out of oscillatory state. This implies the effective conductance across the *LC* resonant element ($G(t)$) periodically varies between positive and negative values. For a given quench period, the core oscillator selectivity is directly proportional to the rate at which the effective conductance $G(t)$ goes from positive to negative [3], [6]. Thus, in a super-regenerative system to achieve wide bandwidth, the effective conductance $G(t)$ should change sign within an order of the pulse duration [7]. Second, the front-end gain in a super-regenerative system is dominated by the core oscillator, which is controlled by the duration for which the effective conductance is less than zero. To have maximum influence on the core oscillator startup time which results in high gain, the incoming pulse should be aligned with the effective conductance around the time when it changes sign. This alignment problem is similar to synchronization issues present in any non-coherent IR-UWB receiver. Hence, the quench signal slope and duty cycle determines the super-regenerative system bandwidth and gain, respectively. In this implementation, a trapezoidal quench signal shape is selected as it offers the required selectivity and gain [8]. Furthermore, such a shape can be easily generated using digital gates, allowing less power consumption in comparison to other quench signal shapes. In this implementation, an external quench signal is used to have more flexibility on the quench signal slope and duty cycle.

2) Data Reception Phases: The different phases in a super-regenerative receiver system are shown in Fig. 2. In the tuning phase, the DPLL circuitry is enabled with the core oscillator sufficiently biased to generate oscillation and the resonant element is tuned to the desired frequency with the corresponding digital bits stored in a register. Once the resonant element is tuned, the DPLL circuitry is disabled and the receiver enters the acquisition mode, which is similar to a clock recovery phase. In the acquisition and data reception mode, the receiver core oscillator operates in open-loop mode with the oscillating frequency controlled by the tuned bits stored in the register. At the end of the

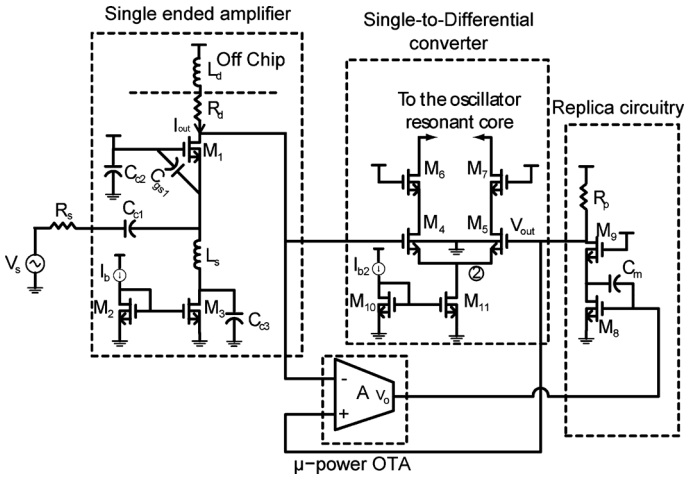

Fig. 3. Transistor schematic of the single-to-differential converter.

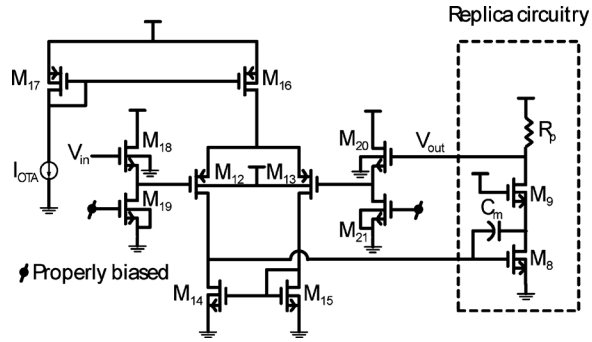

Fig. 4. Transistor schematic of the μ-power OTA.

acquisition mode, the quench signal is synchronized with the incoming pulse and the data reception starts.

B. Single-Ended LNA/Isolation Amplifier

A common-gate amplifier topology is used as the single-ended LNA configuration as shown in Fig. 3. The LNA input impedance is $1/g_{m1}$, which is set to match the 50-Ω input impedance by properly biasing transistor M_1. Capacitor C_{C3}, used to bypass the noise generated by transistors M_2 and M_3, is made sufficiently large to provide a low impedance at signal frequencies. The source inductance L_s is used to resonate with capacitance C_{gs1}, thereby improving interference rejection from other frequencies outside the required band of interest. To increase the pole frequency set by the load capacitance C_d shunt-peaking inductor L_d is added; its value is set to increase the bandwidth by 72% without introducing peaking in the frequency response [9]. The wideband noise from the LNA output is filtered by the regenerative VCO resonant element. It is also possible to have a LNA output tuned to the required band of interest but then automatic tuning becomes difficult. It is for this reason that the first stage is wideband and the tuning is done at the regenerative VCO.

C. Single-Ended-to-Differential Converter

A single-ended signal could be directly injected into the core oscillator from the LNA output, and the core oscillator would naturally convert the input to a differential signal. However, injecting a single-ended signal in this way would introduce asymmetry into the core oscillator. Such asymmetry will reduce the oscillator startup time, which is undesirable since this would result in reduced sensitivity to an external injected signal. For this reason a separate single-to-differential (S2D) converter between the LNA output and VCO input is required.

The converter is realized using a differential amplifier, as shown in Fig. 3, where one input is ac grounded and the other input is connected to the signal from the LNA output. If this circuit exhibits high common-mode rejection at the carrier frequency, then the output currents, taken at the drains of transistors M_6 and M_7, will be nearly balanced. This can be verified by first observing that node 2 in the Fig. 3 circuit moves at the signal frequency with an amplitude equal to half the signal at the transistor M_4 gate. The cascode transistors M_6 and M_7 provide isolation between the resonant core and the input. The condition for high common-mode rejection is that the *RC* time constant associated with node 2 is much lower than the inverse of the input frequency:

$$\frac{1}{f_s} \gg \frac{2\pi(2C_{gs4-5} + C_{db11})}{2g_{m4-5}}. \tag{1}$$

In the design, the transistor pair (M_4–M_5) is biased at a high overdrive voltage to satisfy the above criterion, which is limited by the required transistor pair transconductance for a given bias current. In order to maintain symmetry at the S2D input, a replica biasing as shown in Fig. 3 is used. The replica circuitry is scaled down by a factor of 12 with respect to the LNA in order to reduce the power dissipation, and an OTA is used to servo the outputs of the LNA and replica circuit to be nearly identical. The transistor schematic of the OTA used for proper biasing of the S2D converter is shown in Fig. 4, whose gain-bandwidth product can be kept low ($\sim$ 1.5 MHz-simulated) since it is used only to align dc signals; thus the power dissipation can be made very small. The input source follower configurations M_{18}–M_{19} and M_{20}–M_{21} are used to level-shift the inputs to be compatible with pMOS transistors M_{12}–M_{13} as well to reduce the capacitive loading on the LNA output. The input offset in the OTA can be scaled down to an acceptable level by properly sizing the OTA input transistors which can be achieved without consuming more power. The combined gain of the OTA and replica circuitry is 40 dB (simulated); with such a gain the mismatch between the replica circuitry and LNA is greatly reduced and the offset due to the differential pair (M_4–M_5) starts to dominate. The differential pair (M_4–M_5) is sized to achieve an input offset of 7 mV (3σ).

D. Core Oscillator

The *LC* VCO used as the core oscillator is shown in Fig. 5. The capacitance change between the weak and strong inversion regions in an n-channel transistor is used to change the frequency. The coarse control signals V_{1-3} are used to select the appropriate band and the bits b_{0-4}, set by a digital PLL (described in Section II-E) are used for fine-tuning the frequency. The transistors M_{3-7} are properly dimensioned to achieve an LSB frequency resolution of around 5 MHz ($K_{\mathrm{DCO}} = 5$ MHz/LSB). This resolution is fine enough to maintain sufficient gain of the super-regenerative receiver. The

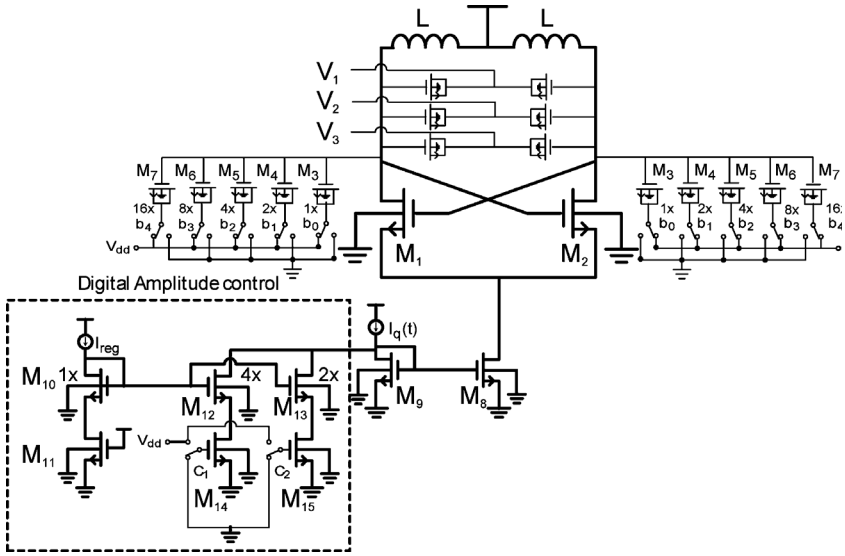

Fig. 5. Transistor schematic of the core oscillator.

simulated resonant element quality factor at 3.993 GHz is close to 8.

The VCO bias current $I_{\rm bias}$ is given by

$$I_{\rm bias} = I_q(t) - I_{\rm reg} \cdot [4c_1 + 2c_0]. \tag{2}$$

where $I_q(t)$ is the time-varying quench current. In practical scenarios, the core oscillator startup time is affected by noise, transistor mismatch, and Q variation, all of which have an adverse effect on the super-regenerative gain as the oscillation build-up follows an exponential curve. Thus, to regulate the core oscillator output voltage, $I_{\rm reg}$ is used. In the present implementation, the bits c_0 and c_1 are set manually to achieve a given oscillation amplitude.

In the described system, the oscillator circuitry tuned to 3.993 GHz achieves a phase noise of -105 dBc/Hz (simulated) at 1 MHz offset when biased at 3 mA.

E. Digital PLL

The incoming pulse will have maximum influence on the startup time when the core oscillator is tuned very close to the carrier frequency [10], [11], which can be achieved using PLL-based circuitry. In an analog PLL implementation, the VCO is set by an control analog voltage. However, once the core oscillator is tuned to the appropriate frequency, the tuning circuitry is turned off, the desired voltage is stored on the capacitor in the loop filter, after which the data reception starts. Charge injection and leakage in the loop filter will change the oscillation frequency of the analog VCO over time [11]–[13]. On the other hand, in a digital implementation, a digital controlled oscillator (DCO), comprised of an *LC* oscillator and a bank of capacitors, is used. The oscillator frequency is controlled by switching appropriately sized capacitors in or out, and the digital bits are stored once it is tuned, thereby maintaining a stable frequency once the data reception begins.

In a DPLL, the frequency resolution is limited by the number of bits, and in the locked state the oscillator frequency is offset from the carrier frequency by as much as an LSB. The same will be true when the loop is opened. Thus, the number of bits must be set based on the acceptable frequency resolution for the design. Though such a tuning circuit does not achieve maximum gain as it is not tuned to the exact frequency, in the case of UWB systems the signal bandwidth is wide enough so that the inaccuracies in the core oscillator frequency due to this limited resolution do not significantly degrade the gain. In this implementation, a 5-bit capacitor bank is chosen achieving an LSB frequency resolution of 5 MHz, and the gain degradation due to the finite resolution is less than 0.1 dB (simulated) making DPLL-based tuning circuitry viable for this application.

The DPLL consists of a time-to-digital converter (T2D), a digital loop filter, a DCO, and a divider as shown in Fig. 2. Each block is designed as follows.

1) T2D Converter: The T2D converter generates either an up or a down pulse signal depending upon whether the feedback signal is behind or ahead of the reference clock, respectively [14], [15], which after filtering through a digital loop filter drives the DCO towards lock. A one-bit T2D converter is chosen as it is enough to achieve a frequency synchronization between the reference and feedback clock. The generation of up/dwn signals in the T2D is carried out in two stages as shown in Fig. 6. The first stage consists of flip-flops DFF1 and DFF2 that generate pulses such that the difference between their widths is proportional to the phase difference between the reference and divider output clock as in a conventional PFD. The second stage, consisting of DFF3 and DFF4, samples the output and correspondingly retimes the up/dwn signals so that they are synchronized by the divider output and reference clock, respectively.

2) Digital Loop Filter: In order to realize a Type-II DPLL, the digital loop filter consists of a proportional and an integral element, implemented externally in an FPGA. To achieve loop stability, the proportional (K_p) and integral (K_i) coefficients can be derived from

$$\omega_z = \frac{K_i}{K_p T_s} \tag{3}$$

$$\omega_0 = \frac{K_{pd} * K_{\rm DCO} * K_p}{N}. \tag{4}$$

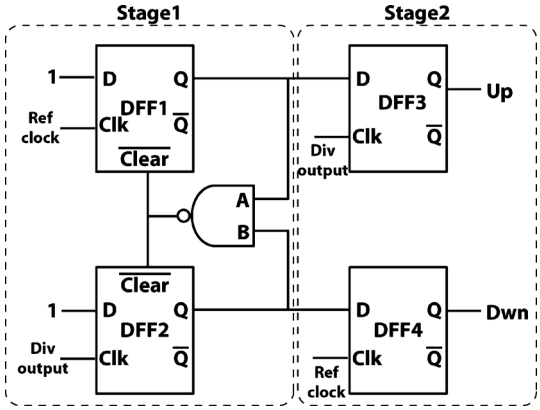

Fig. 6. Schematic diagram of the T2D converter.

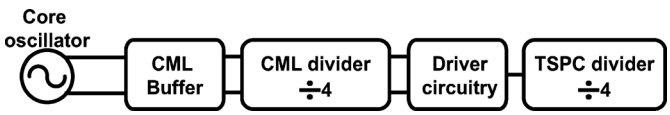

Fig. 7. Schematic diagram of the fixed divider.

The loop parameters for this design are chosen as follows. The frequency resolution ($K_{\rm DCO}$) is chosen to be 5 MHz per bit. For ease of implementation we set $K_{pd} = 1$ and $K_p = 1$. The parameters are summarized as follows:

- reference frequency $f_s = 31.2$ MHz;
- $K_{\rm DCO} =$ 5 MHz/LSB;
- $N = 112$;
- $K_{pd} = 1$;
- $K_p = 1$.

Using (4), the result is a unity-gain frequency $f_0 =$ 7.1 kHz. In order to realize sufficient phase margin, we choose $\omega_z = 2\omega_0$; thus, from (3), we have $K_i = 2.86 \times 10^{-3}$. We choose $K_i = 2^{-10}$ for ease of realization. During the acquisition phase, the time required to change the DCO frequency control register by LSB is equal to $1/(K_i * f_{\rm ref})$. Therefore, the time required to reach midrange of full scale of the control register is $2^{(n-1)}/(K_i * f_{\rm ref})$, where n is the size of the control register. In the present implementation, where the control register size is 5 bit, the time required is calculated to be 525 μs.

The appropriate capacitors in the DCO are switched in or out depending on the up and down signals from the digital loop filter, thus setting the oscillator frequency within 1 LSB to the carrier frequency. In this implementation, the targeted frequencies are 3.494 and 3.993 GHz, which correspond to the frequencies in the lower band of the IEEE 802.15.4a standard [5]. The 31.2-MHz reference frequency is used as it can generate all center frequencies for the various bands in the UWB system using an integer division.

3) Frequency Divider: To achieve a divide ratio of 112 or 128, a fixed divide ratio of 16 and a variable divide ratio of 7 or 8, respectively, is implemented using a multi-modulus counter as shown in Fig. 2. The fixed divider is implemented using a combination of CML and TSPC logic as shown in Fig. 7, where a CML buffer provides isolation between the divider and the core oscillator. Following the CML divide-by-4, a driver is used to generate rail-to-rail signals that are input to the TSPC divide-by-4 [11].

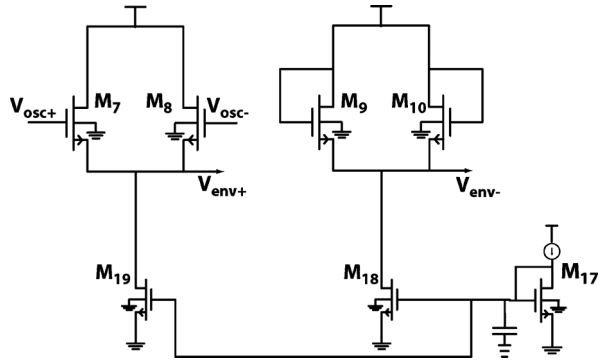

Fig. 8. Transistor schematic of the envelope detector.

An alternative approach to achieve frequency synchronization is to use a frequency-locked loop (FLL) as shown in [16]. There are merits to both approaches: The FLL described in [16] has very fast acquisition time, but additional circuitry is needed in order to compensate for timing variations in the counter outputs which further becomes critical for higher oscillator frequency. On the other hand, the DPLL used in this circuit has a longer acquisition time but with the advantage of a more simple circuit structure. Higher acquisition time is acceptable for this circuit since after the startup of the system it is only necessary to track the frequency changes. Therefore, a DPLL-based frequency tuning is used for this implementation.

F. Detection Circuitry

1) Envelope Detector: The schematic of the envelope detector is shown in Fig. 8. The source-coupled node $V_{\rm env+}$ of the differential pair M_7–M_8 performs a squaring operation on the differential signal $V_{\rm osc}$–$V_{\rm osc-}$ while the capacitance at that node filters out the second- and higher-order frequency components, thereby leaving only the envelope of the input signal. The output $V_{\rm env+}$ is compared with a reference signal $V_{\rm env-}$ that is derived from the replica biasing of differential pair M_9–M_{10}.

2) Comparator and Regenerative Latch: In the present system, a 1-bit comparator is used. The advantage of having a higher number of bits is to tolerate higher interference power level and to reduce the synchronization time at the cost of power consumption and implementation complexity. The choice of 1-bit comparator is to reduce the power consumption and to use such a system where the BER is not interference limited. For OOK modulation, the envelope detector output is to be compared with a reference voltage to determine whether a pulse is transmitted. However, the reference voltage is only on the order of tens of millivolts, making the use of an external voltage reference impractical since power supply noise could severely degrade the comparison operation. To overcome this difficulty, an appropriate reference voltage is generated internally by adding mismatch to a differential amplifier as shown in Fig. 9. The reference voltage generated for a 1-bit change using mismatch in transistor dimensions is given by

$$\Delta V = \frac{\Delta W \cdot I}{W \cdot g_m} \tag{5}$$

where g_m, I, W, and ΔW correspond to the input transistor pair transconductance, bias current, input transistor pair width,

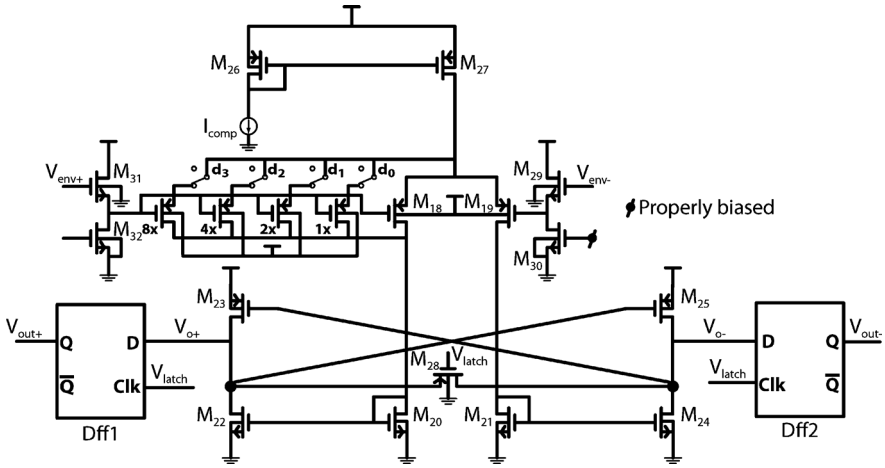

Fig. 9. Transistor schematic of the comparator and regenerative latch.

and change in transistor width, respectively. It should be noted that for proper comparator operation the input differential pair should be properly sized in such a way that $\Delta V > V_{\rm offset}$, where $V_{\rm offset}$ is the random offset due to the differential pair. In a general case for $\rm n$ bits, the reference voltage is given by

$$V_{\rm thres} = \Delta V \left(2^{n-1} d_{n-1} + 2^{n-2} d_{n-2} + \cdots + 1\right) \quad (6)$$

where $d_0, d_1, \ldots$ correspond to the input bits.

The comparator output is applied to the regenerative latch as shown in Fig. 9, which amplifies the input difference to a hard "1" or "0." The input source follower pairs M_{29}–M_{31} are used to level-shift the dc level at the envelope detector outputs so that they are compatible with the input pMOS differential pair M_{18}–M_{19}. The regenerative latch operates in two phases—comparison and regeneration —that are controlled by the transistor switch M_{28} driven by the clock signal $V_{\rm latch}$. Since the envelope build-up in the oscillator follows an exponential curve, to achieve maximum sensitivity the peak value of the envelope detector output is sampled and compared with the reference voltage. Thus, the clock signal $V_{\rm latch}$ is identical to the quench signal that is applied to the VCO bias current, so that the start/end of the regeneration/comparison phase is equivalent to sampling the envelope peak value. The flip-flops DFF1 and DFF2 are used to sample the value in the regeneration phase; adequate care is to be taken during the flip-flop design to prevent any setup/hold violation. During the regenerative phase the pMOS cross-coupled pair (M_{23}–M_{25}) acts as a regenerative amplifier resulting in a rail-to-rail output signal.

3) Transient Simulation: The transient simulation with noise at various stages of the IR-UWB super-regenerative receiver is shown in Fig. 10. The transmitted signal bandwidth is 500 MHz centered at 3.993 GHz with a data sequence alternating between "1" and "0" at a rate of 10 Mbps. The communication is based on an OOK modulation, where "1" indicates the presence of a pulse and "0" indicates no pulse. In practical scenarios, the received signal consists of multipath components, with the amplitude of the multi-path components determined using a power-delay profile with an exponential characteristic. In this simulation, to mimic a scenario close to the practical case multipath components are taken into account and the multipath components are assumed to spread over a duration of 10 ns.

Fig. 10(a) shows the received pulse sequence at the input of the single-ended amplifier, where the received signal amplitude is adjusted for multipath components. When the quench signal is synchronized with the arrival of the pulse, the voltage build-up at the oscillator output is shown in Fig. 10(b), which indicates a difference in the peak value between the presence and absence of a pulse. The oscillator output reaches a peak value of 250 mV for an average input power of -61 dBm. Since the super-regenerative receiver is periodically quenched, the front-end gain (G) is measured in the time-domain. As the peak voltage at the resonator output is sampled to determine the presence of a pulse, the front-end voltage gain of the IR-UWB receiver is defined as the ratio between the peak oscillator output voltage and the input received voltage across 50 Ω to yield

$$G = \frac{\hat{V}_{\rm osc}}{V_{\rm in}}. \quad (7)$$

Thus, the simulated front-end gain for an average input power of -61 dBm (peak power $= -44$ dBm) is 41.9 dB. As the envelope detector conversion loss is different in the presence and absence of a pulse, the difference in peak voltage at the envelope detector output is higher in comparison to the core oscillator output as shown in Fig. 10(c). The reference voltage at the comparator input is properly tuned and Fig. 10(d) shows the regenerative output. In the comparison phase, the output voltage ($V_{o+/-}$) are held together by turning on transistor M_{28}. Once M_{28} is turned off, the transistor pair (M_{23}–M_{25}) enters into regenerative phase. The regenerative output is sampled appropriately with a delay of one period using a D-flip-flop as shown in Fig. 10(e) and (f).

III. Measurement Results

The IR-UWB super-regenerative receiver is implemented in a CMOS 0.18-μm technology, with a die size of 1.5 mm × 1 mm; the area is dominated by the bond pads and on-chip inductors. Since the PLL circuitry consists of larger digital blocks, dedicated power supplies are used for the divider circuitry and the super-regenerative receiver chain in order to reduce noise coupling. The receiver circuit consists of 58 bond pads that are

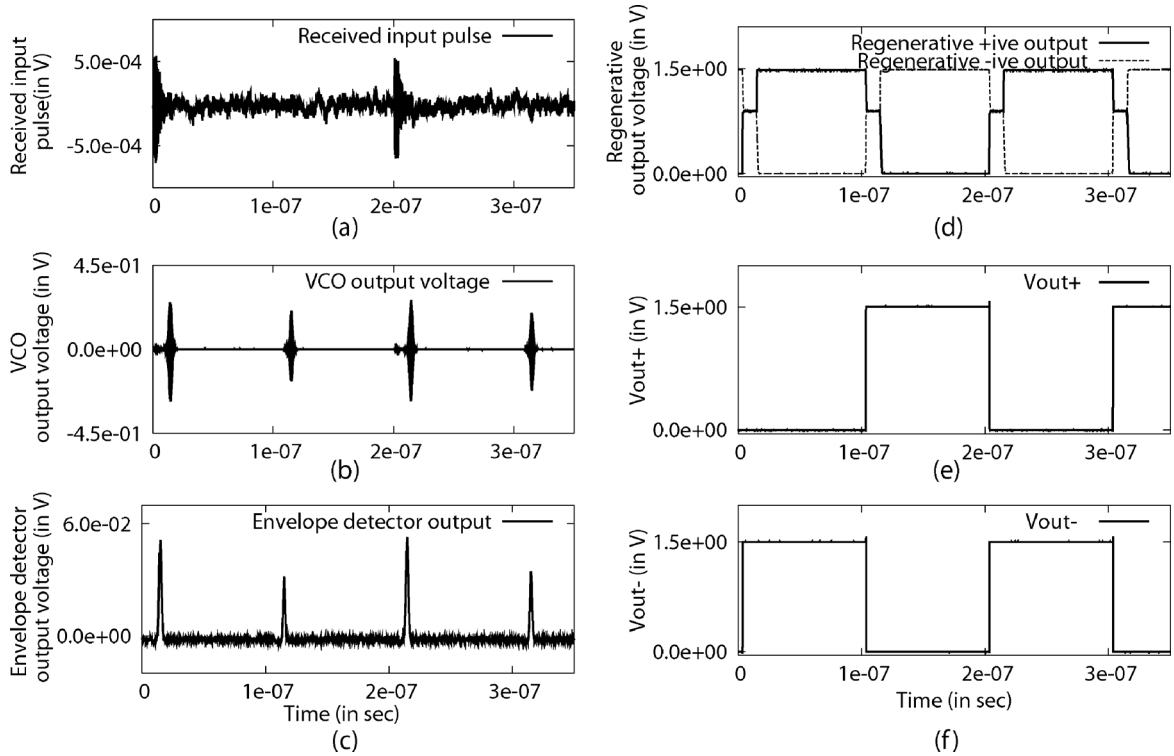

Fig. 10. Transient simulation with noise at various stages of the IR-UWB SR receiver for an average input power level of −61 dBm.

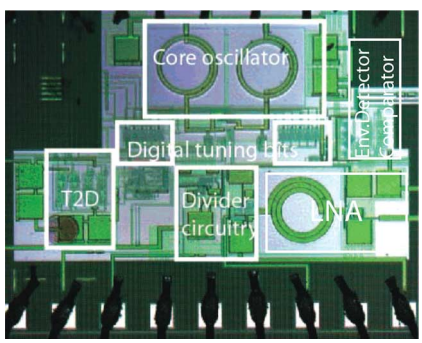

Fig. 11. Chip microphotograph of the UWB receiver.

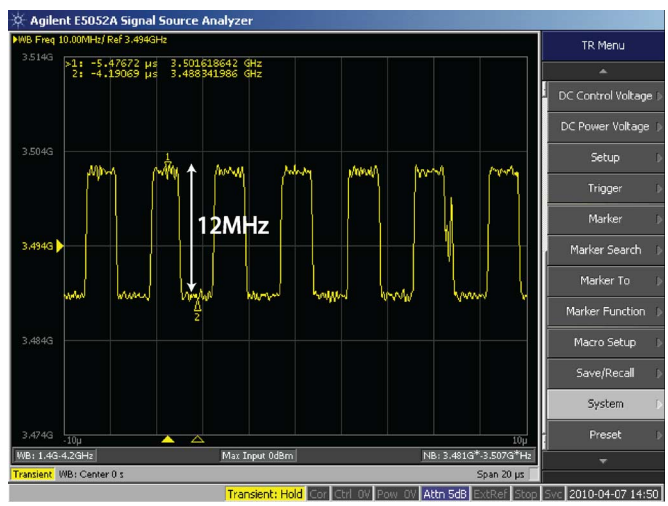

Fig. 12. DPLL steady-state output tuned at 3.494 GHz.

gold-wired onto a low-dielectric Rogers 4003C PCB. The chip microphotograph is shown in Fig. 11. If packaged, adequate care is to be taken to choose the appropriate package so as to avoid any potential problems in LNA input matching degradation. The LNA output uses an external inductor for bandwidth extension, parasitic inductance due to packaging is to be accounted for while choosing the value.

A. Closed-Loop DPLL Measurement Results

The DPLL core oscillator output was measured in closed-loop with the output frequency tuned to 3.494 GHz, corresponding to a divide ratio of 112. The oscillator output frequency as a function of time is shown in Fig. 12, where the core oscillator output toggles between the two frequencies corresponding to a frequency resolution of ± 1 LSB (12 MHz). The difference of 1 MHz between the simulated and measured frequency resolution is due to the variation in MOS capacitance. Once the DPLL circuitry is turned off, the digital low-pass filter output corresponding to one of these frequencies is stored and the data reception starts.

The core oscillator output frequency spectrum at centered 3.494 GHz is shown in Fig. 13 corresponding to the DPLL being active; the two side lobes correspond to the toggling frequencies that generate 3.494 GHz on an average. The side lobe amplitude is not important in this implementation as the data reception is carried out in open-loop mode.

B. IR-UWB Receiver Measurements

1) Measurement Setup: The setup used for the measurements is shown in Fig. 14. The wide bandwidth baseband signal of 500 MHz is generated using the HP8131A pulse generator,

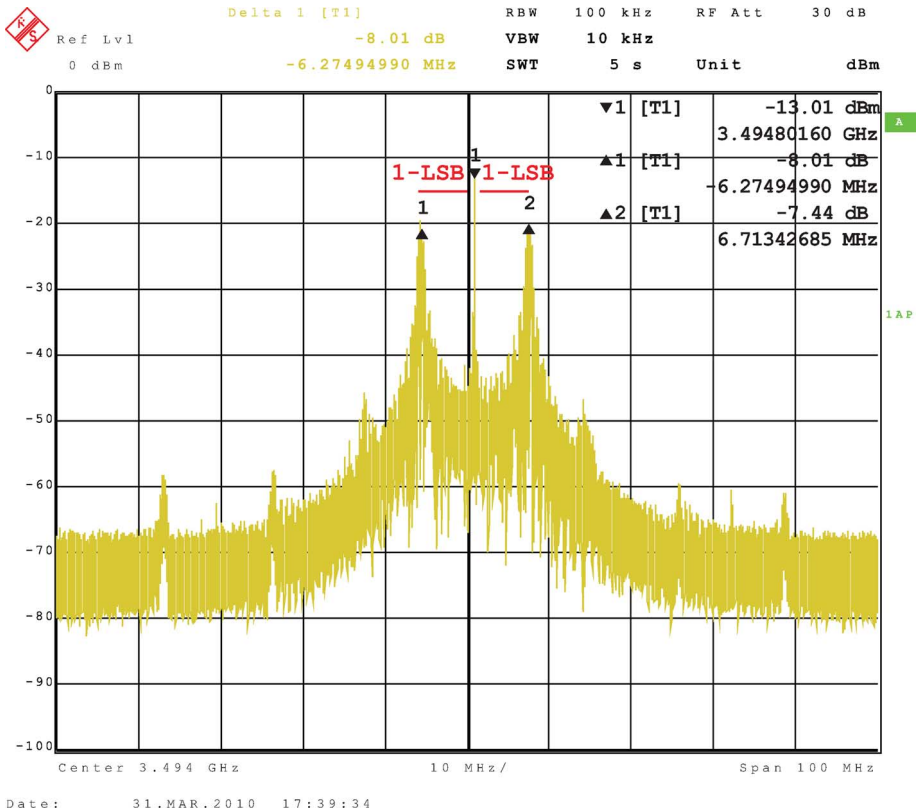

Fig. 13. Core oscillator output spectrum at 3.494 GHz.

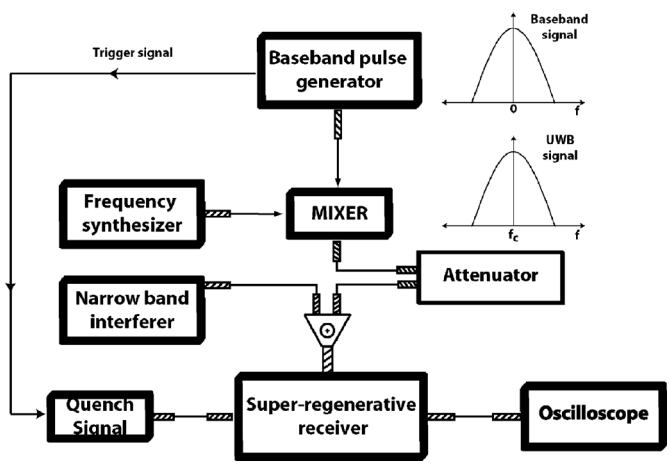

Fig. 14. BER and interference measurement setup.

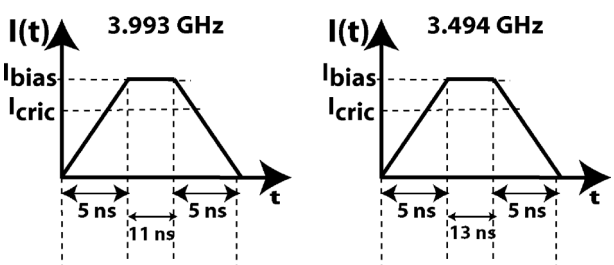

Fig. 15. Quench signal duty cycle for 3.494 and 3.993 GHz.

and the local oscillator signal is generated using a Rohde and Schwarz signal generator. The two signals are mixed using a passive mixer from a Hittite-H128 mixer board. The IR-UWB signal is passed through an attenuator to mimic the path loss in

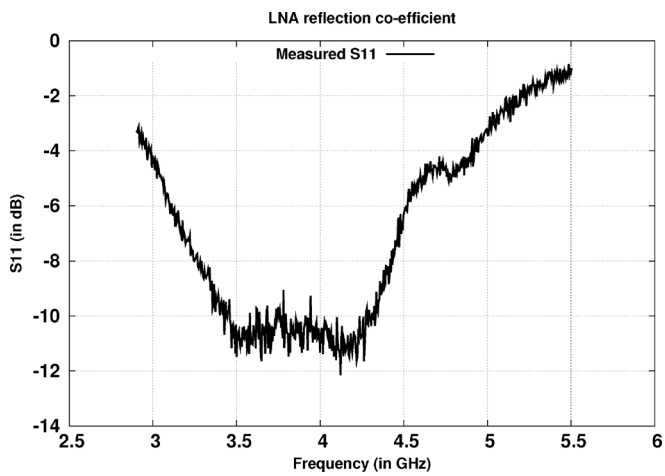

Fig. 16. Measured input reflection coefficient for the single-ended LNA.

the wireless transmission. The clock synchronization between the transmitter and the receiver is achieved manually using the trigger signal from the HP8131A baseband pulse generator. In this implementation an external quench is used, which is generated using Agilent 33520A 80-MHz arbitrary waveform generator. The transmitted data rate is 10 Mbps using an OOK modulation. In order to achieve sufficient gain and optimum receiver sensitivity, the quench duty cycle was set to 23% and 21% for 3.494 and 3.993 GHz, respectively, and the quench slope duration, which controls the selectivity of the receiver, was set to 5 ns, as shown in Fig. 15.

2) Reflection Measurement: The reflection coefficient ($S11$) of the input single-ended LNA/isolation amplifier as shown in

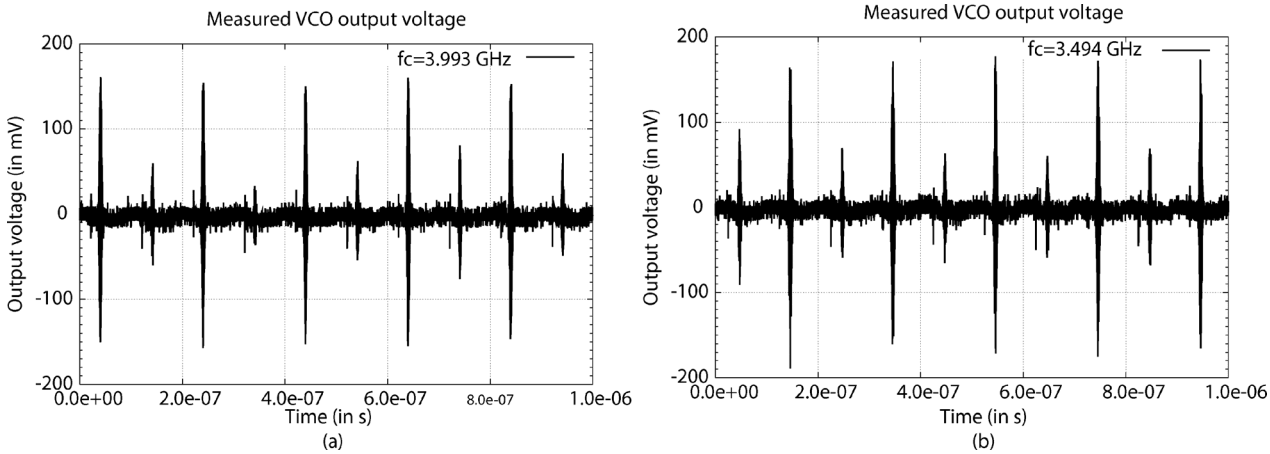

Fig. 17. Measured oscillator output voltage at 3.993 and 3.494 GHz.

Fig. 16 is measured using properly calibrated network analyzer HP8731D. From the figure, the average $S11$ shows -10 dB and -10.7 dB at 3.494- and 3.993-GHz bands, respectively, which meets the specification of -10 dB.

3) Time-Domain Measurement: To measure the voltage gain and to show the envelope variation between the presence and absence of a pulse, a periodic data pattern of ones and zeros is transmitted. For an average input received power of -61 dBm (peak power $= -44$ dBm) at 3.993 GHz, the measured variation in the oscillation build-up between the presence and absence of a pulse is shown in Fig. 17(a). The peak output voltage across the resonator in the presence of a pulse is around 160 mV. Thus, the front-end gain of the IR-UWB receiver based on super-regenerative principle at 3.993 GHz is 38 dB using (7). The difference between the simulated and achieved gain is due to the parasitic resistive loss in the oscillator resonant circuitry. In a similar set-up, the difference in the presence and absence of a pulse transmitted at 3.494 GHz is shown in Fig. 17(b). In the presence of a pulse, the oscillator reaches a peak voltage of 175 mV for an average input received power of -66 dBm (peak power $= -49$ dBm). The front-end voltage gain of the IR-UWB super-regenerative receiver at 3.494 GHz is 43 dB.

4) BER Measurement: Bit error rate (BER) measurement is carried out to measure the sensitivity of the IR-UWB super-regenerative receiver, which is often an accepted benchmark to compare different receiver performances. For the BER measurement, the reference voltage at the input of the comparator is manually set to 15 mV and the measured BER graph for 3.494 and 3.993 GHz is shown in Fig. 18. The measured sensitivity of the IR-UWB super-regenerative receiver is -66 and -61 dBm in the 3.494- and 3.993-GHz bands, respectively, at a BER of 10^{-3}. This translates into a peak received signal amplitude of 1.1 and 2 mV in the 3.494- and 3.993-GHz bands, respectively. This measurement assumes that the quench signal is perfectly synchronized with the incoming pulse; a deviation of ± 2.5 ns from the synchronized position results in the output signal being indistinguishable from the oscillation build-up due to noise.

One method to achieve synchronization would be to divide the pulse repetition period into smaller time windows and to search for a pulse in each successive window [17], [18]. For example: let us assume the pulse repetition rate is T_p and a single

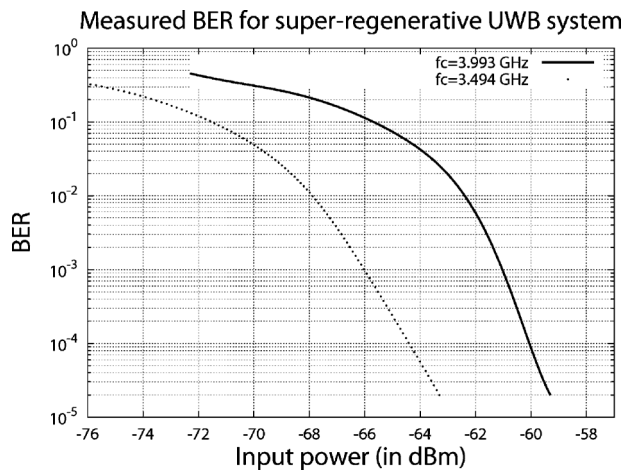

Fig. 18. BER plot for 3.494 and 3.993 GHz.

repetition period is divided into N time slots each with a width of T_l s, i.e., $N = T_p/T_l$. In a pulsed super-regenerative receiver T_l corresponds to the quench cycle duration (from the proposed implementation when the oscillator is tuned to 3.494 GHz, T_l corresponds to 23 ns). At the end of each quench cycle duration, the comparator output data indicates the presence/absence of a pulse which is used for synchronization.

Assuming a path loss coefficient of 2 and using the Friis relation, the theoretical range is calculated to be close to 1.7 m to achieve a BER of 10^{-3} when the receiver is tuned to 3.993 GHz. The present implementation was tested in a lab environment with a Skycross UWB antenna, manual synchronization and the core oscillator tuned to 3.993 GHz at a data rate of 10 Mbps. The communicating distance was close to 1.2 m in order to have an oscillation build-up amplitude of 160 mV. In a pulsed super-regenerative receiver using back-to-back pulses in order to increase the effective system range, a certain time interval between the pulses is needed to discharge the energy stored in the resonant element before demodulating the next pulse. For example, back-to-back pulses should have an interval of at least 5 ns (for Q $= 8$ and tuned to 3.494 GHz) to be sure that the energy is completely discharged.

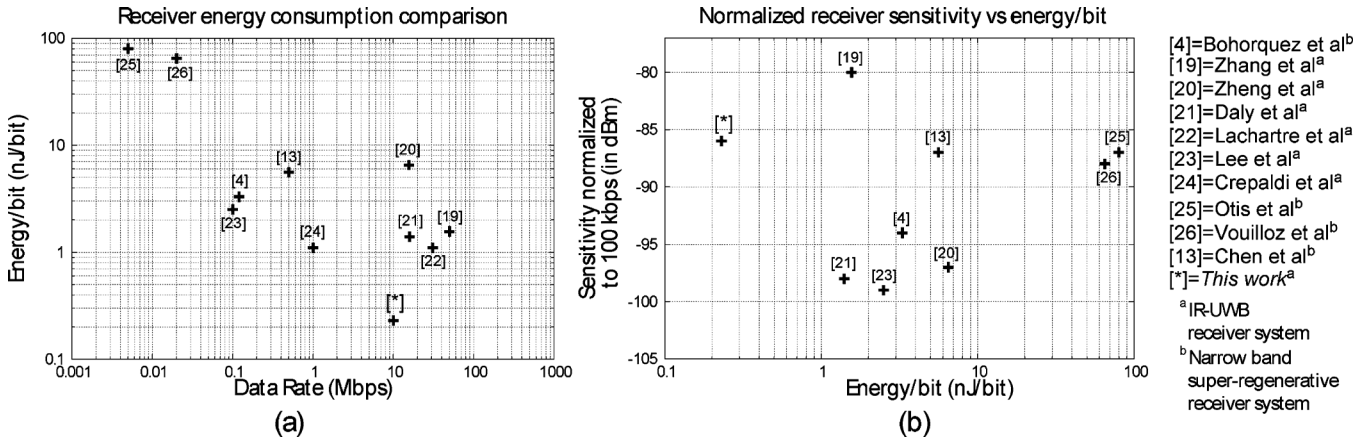

Fig. 19. (a) IR-UWB receiver energy/bit versus data rate scatter plot. (b) IR-UWB receiver sensitivity versus energy/bit scatter plot.

5) Interference Measurement: Often the receiver sensitivity is strongly degraded due to interfering signals, which is an important issue in the noncoherent receiver system. In the case of a UWB system, the potential interferences come from other UWB transmitters that are within the band of interest and out-of-band interferer primarily at 2.4 GHz (Bluetooth). For the interference tolerance measurements, the input UWB signal power is set to 3 dB above the required power to achieve a BER of 10^{-3} and the interferer at 2.4-GHz power level is increased until the measured BER is 10^{-3}. In the measurement setup as shown in Fig. 14, the narrowband interference signal is combined with the UWB signal using a resistive power combiner. The measured rejection from an interferer at 2.4 GHz when the receiver is tuned to 3.494 and 3.993 GHz is -10 dBm. Thus, the receiver when tuned to either 3.494 or 3.993 GHz can tolerate an interferer signal amplitude of 100 mV at 2.4 GHz achieving a BER of 10^{-3}. The rejection is due to LNA input matching network and the core oscillator resonant element.

C. Power Consumption-Energy/Bit Analysis

Assuming the super-regenerative receiver is tuned to the required band of interest, the power consumption of the individual blocks in the receiver chain at a supply voltage of 1.5 V is given in Table I. The main power consuming block in the IR-UWB super-regenerative receiver is the front-end circuitry (input amplifiers + oscillator structure), which consumes almost 92.5% of the total power consumption.

In the case of an IR-UWB super-regenerative receiver, based on the quench signal, the front-end circuitry should be active at least for a duration of at least 23 ns for proper pulse reception, which corresponds to an energy/bit of 0.24 nJ/bit (10.8 mW $\times$ 23 ns $=$ 0.24 nJ/bit). Energy comparison with the other published IR-UWB receivers is shown in Fig. 19(a), using data from [4], [13], [19]–[26].

The energy/bit is not necessarily the only meaningful metric to be used as a benchmark for a receiver [19], [21]. In particular, it does not take into account the receiver sensitivity. In Fig. 19(b), a comparison between the normalized sensitivity for various published receiver architectures with this work is shown, with the data plotted from Table II. Table II shows a significant reduction in energy consumption for the IR-UWB receiver using super-regenerative architecture, and the normalized sensitivity is acceptable for UWB systems.

TABLE I
POWER CONSUMPTION OF THE IR-UWB SUPER-REGENERATIVE RECEIVER

Input SE-LNA/Isolation amplifier (including bias)	2.25 mW
S2D converter	
Bias circuitry	225 μW
S2D converter	3 mW
μ-power OTA	12 μW
Replica circuitry	150 μW
Oscillator structure	
Amplitude control loop (including bias)	300 μW
Core oscillator structure	4.8 mW
Total front-end consumption	**10 mW**
Envelope detector	112 μW
Comparator and regenerative circuit	
Input source followers	300 μW
Comparator	375 μW
Digital Low pass filter	External
Number of bits	5
Divider circuitry	4.5 mW
Total chip consumption (excluding divider)	**10.8 mW**

In the present implementation, a decreased sensitivity in comparison to an energy collection receiver is attributed to the fact that in the absence of a pulse the oscillation build-up due to noise reaches a significant amplitude, thus degrading the SNR. One of the reasons for this oscillation build-up in the absence of a pulse is that the quench signal slope duration, which influences the startup, is relatively close to the core oscillator time period. Since the quench signal slope duration and time period are relatively close, the quench signal energy that is leaked through the bias transistor to the resonant element is less attenuated and hence influences the startup time in the absence of a pulse. The energy leakage through the bias transistor is a common-mode signal but due to the mismatch between the cross-coupled transistors finds its way to the *LC* resonant element. For example,

TABLE II
RECEIVER PERFORMANCE COMPARISON

	Data rate	Power consumption	Energy/bit	Receiver sensitivity P_{ss}	Sensitivity normalized to 100 kbps (in dBm)
Zheng et al [20][a]	15.6 Mbps	102 mW	6.51 nJ/bit	-75	-97
Zhang et al [19][a]	50 Mbps	156 mW	N/A	-53	-80
Lee et al [23][b]	100 kbps	35.8 mW	2.5 nJ/bit	-99	-99
Daly et al [21][b]	16 Mbps	22.5 mW	1.4 nJ/bit	-76	-98
Vouilloz et al [26][c]	20 kbps	1.3 mW	65 nJ/bit	-95	-88
Chen et al [13][c]	500 kbps	2.8 mW	5.6 nJ/bit	-80	-87
Otis et al[25][c]	5 kbps	0.4 mW	80 nJ/bit	-100	-87
Bohorquez et al[4][c]	120 kbps	0.4 mW	3.3 nJ/bit	-93	-94
Ayers et al[16]	2 Mbps	215 μW	0.175 nJ/bit	-75	-88
Pelissier et al[8][d]	1 Mbps	11.16 mW	N/A	-99	-109
This work[b]	10 Mbps	10.8 mW	0.24 nJ/bit	-66	-86

[a] Coherent IR-UWB receiver system.

[b] Non-coherent IR-UWB receiver system.

[c] Narrow band super-regenerative receiver system.

[d] Circuit consists of RF-Front end only.

in the implementation, the quench signal slope is 5 ns and the oscillator period is 286 ps for 3.494 GHz, which gives a ratio close to 17.5.

Table II also shows a comparison between narrowband and wideband super-regenerative receivers. Their sensitivities are similar, but the energy gain in a wideband system is much greater than a factor of 10. Although the instantaneous power consumption in a wideband super-regenerative system is much higher than a narrowband super-regenerative system as shown in Table II, due to aggressive duty cycling wideband super-regenerative systems achieve a lower energy per bit.

IV. CONCLUSION

In a noncoherent IR-UWB receiver, the main power consuming blocks are the front-end amplifiers, which need to provide sufficient gain for proper operations of further stages. In this paper, a front-end architecture based on the super-regenerative principle that uses an oscillator to amplify the received signals was described. Since an oscillator is used to amplify the received signals, such an architecture achieves high gain while consuming less power. The proposed receiver was implemented in a CMOS 0.18-μm technology and consumes 0.24 nJ/bit. The receiver system in the best case achieves a BER of -66 dBm at a data rate of 10 Mbps. Furthermore, a tuning circuitry based on a DPLL architecture was described. Due to the wide bandwidth of received signal, a DPLL-based tuning circuitry is an ideal candidate for such a system consuming 9.3 mW and can tune to either 3.494 or 3.993 GHz.

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