CONTRIBUTION TO THE ACTIVE GENERATOR PRINCIPLE: The Gate-Commutated Polyphased Matrix Converter

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Abstract

This work is part of the innovative « Active Generator » (AG) project. AG is a concept that suggests a new arrangement of the turbine-generator line of a high power utility (a few hundred of MW) in order to de-synchronize the rotation speed of the turbine-generator group from the fixed grid frequency (50Hz or 60Hz). This de-synchronization has essentially two advantages. First, the variable speed of the group enables the operation of the turbine at its best available efficiency in function of the delivered power. Second, the de-synchronization allows to eliminate the gearbox between the turbine and the generator without losing the important degree of freedom in the choice of optimal nominal rotation speed of the turbine. The latter advantage is particularly interesting for high power utilities, whose prime mover is a gas turbine, because for this power range the gearbox constitutes a heavy burden. The de-synchronization is realized with a static frequency converter which is a power electronics circuit composed of silicon power devices. The converter must ensure the same nominal frequency ratio than the gearbox it replaces, which can go above 50%. For such ratio the converter must be inserted between the stator windings of the generator and the grid. There are numerous different frequency converters. Some of them are available as industrial products and others are still in a development state. Not all of these different frequency converters are well adapted to high power applications. In the AG literature, a few recommendations suggest to use a low frequency commutation sequence, combined with a high number of input phases. The high number of input phases ensures a sufficient resolution of the converter's output voltage. Compared to others, this sequence is supposed to decrease the commutation losses of the converter, avoid the usual overdesign of the nominal power of the generator, and, finally, does not require the converter to include bulky intermediary DC storage components (capacitor or inductor). This sequence is a variant of the "Cosine Waveform Crossing" (CWC) method used for Naturally Commutated Cyclo-converters (NCC) and is named *slowCWC*. However, up till now, there is no converter that is able to run properly with this sequence. Thus a new converter is needed.

This PhD work introduces a new converter that is able to fulfill the *slowCWC* sequence. It is derived from a slight modification of an existing topology (NCC) and is called "gate-commutated Polyphased Matrix Converter" (PPMC). It is a direct frequency converter with a high number of input phases, generally greater than twenty, and a matrix structure of the valves that allows to connect each of the three output phases to each of the generator (input) phases. The valves are bi-directional in voltage and current and are transistor-based to achieve the turn-off capability required by the commutation sequence. The PPMC requires to add protection circuits across each generator stator winding. These circuits protect the stator windings from overvoltages which appear during some forced commutations.

In its first part this PhD work uses an analytical approach and the results are expressed in a per unit system that is also adequate to describe the electrical machines. In this first part, it is about the development of design rules for the components of the protection circuits. In addition the energy losses linked to these circuits are evaluated. Those losses strongly depend on the commutation type, which is itself influenced by the presence of the protection circuits. The expression of the duration of natural commutations in the per unit system is also developed in this first part and it constitutes a key parameter in the determination of the commutation type. These theoretical developments are illustrated with numerical simulations.

In its second part this PhD work presents the realization of a small-scale experimental set-up with reduced power (1kW) but a high input phase number (27). The aim of the experimental set-up is to implement and experiment in real-time the command and control algorithm of the PPMC as well as to verify the theoretical predictions developed in the first part. The results of those developments lead to the quantitative assessment of the efficiency of the PPMC. Besides the key parameters that can help to improve this efficiency are pointed out. In certain cases the efficiency of the PPMC is acceptable under the condition that a generator parameter (its leakage reactance) remains under a

given limit. This work ends with a list of suggestions for future works related to the improvement of the PPMC and related to the AG project.

Keywords: frequency conversion, power electronics, power generation utility, gas turbine, variable speed, gearbox, efficiency, overvoltage, protection circuit, natural commutations, forced commutations, commutation duration, cosine waveform crossing.

Résumé

Ce travail s'inscrit dans le contexte d'un projet d'innovation nommé «the Active Generator » (AG). AG est un concept proposant un nouvel arrangement de la ligne turbine-générateur d'une centrale de production d'électricité de grande puissance (quelques centaines de MW) afin de désynchroniser la fréquence fixe du réseau électrique (50Hz ou 60Hz) de la fréquence de rotation du groupe turbine-générateur. La désynchronisation amène principalement deux avantages. Premièrement, la vitesse variable du groupe permet d'utiliser la turbine de manière efficace en fonction de la puissance délivrée. Deuxièmement la désynchronisation permet d'éliminer le réducteur mécanique, généralement inséré entre la turbine et le générateur, sans perdre la liberté du choix de la vitesse de rotation nominale optimale pour le dimensionnement de la turbine. Ce dernier avantage est particulièrement intéressant pour les centrales de grande puissance, dont la source mécanique est une turbine à gaz, car le réducteur pour ces puissances est un fardeau incontournable. Le rapport de transformation des vitesses de ces engrenages est d'environ 2:1 ou supérieur. La désynchronisation et le remplacement du réducteur peuvent être réalisés par le biais d'un convertisseur statique de fréquence, c'est-à-dire un circuit électronique composé d'éléments à semi-conducteurs de puissance. La valeur du rapport des fréquences impose un convertisseur statique de fréquence de puissance nominale égale au groupe turbine-générateur. En plus, ce convertisseur doit être placé entre le stator du générateur et le réseau. Il existe aujourd'hui une multitude de convertisseurs de fréquence différents, certains fonctionnant déjà sous forme de produits industriels d'autres sont encore au niveau expérimental. Ces différents convertisseurs peuvent plus au moins bien être adaptés à des grandes puissances. Dans la littérature au sujet de AG, une série de recommandations proposent une séquence de commutation à basse fréquence avec un nombre de niveaux d'entrée élevé afin de garantir une résolution suffisante de la tension de sortie du convertisseur en se passant de filtre. Cette séquence est une variante de celle qui est utilisée pour les Cyclo-convertisseurs à commutations naturelles (CCN). Cette séquence aurait comme avantage, par rapport aux autres solutions, de diminuer les pertes du convertisseur, d'éviter un surdimensionnement de la puissance nominale du générateur, et enfin, de se passer de gros éléments passifs de stockage intermédiaires (condensateur ou inductance). Cependant il n'existe à ce jour aucun convertisseur capable d'exécuter cette séquence correctement. Un nouveau convertisseur est donc nécessaire.

C'est ainsi que ce travail propose une modification d'un convertisseur déjà existant (CCN) afin de réaliser un système compatible avec la séquence proposée dans la littérature. Cette solution est nommée « Polyphased Matrix Converter » (PPMC). Il s'agit d'un convertisseur de fréquence direct avec un nombre de phases d'entrée élevé, généralement supérieur à vingt, et une structure matricielle permettant de relier chacune des trois phases de sorties à chacune des phases du générateur d'entrée. Les interrupteurs sont de type bidirectionnels en tension et en courant, au pouvoir d'interruption contrôlable, une qualité imposée par la séquence de commutation utilisée. Le PPMC nécessite l'ajout de circuits d'aide à la commutation aux bornes de chaque phase statorique du générateur afin de protéger celles-ci contre des surtensions apparaissant lors de certaines commutations forcées. La première partie de ce travail est théorique et est constituée de développements algébriques qui expriment les résultats par des grandeurs adimensionnelles compatibles avec le système usuellement utilisé pour la description des machines électriques. Il s'agit de dimensionner les éléments du circuit de protection en fonction des contraintes données et d'évaluer les pertes supplémentaires occasionnées par ceux-ci. Ces pertes dépendent fortement du type de commutation qui est lui-même influencé par la présence des éléments de protection. Le développement du calcul de la durée relative des commutations naturelles est aussi donné dans cette première partie et constitue la clef de voûte dans la détermination du type de commutation. Ces résultats théoriques sont appuyés par des exemples de simulations numériques. Une deuxième partie de ce travail consiste en la réalisation et la mise en œuvre d'un modèle physique de PPMC à échelle réduite (puissance nominale 1kW) mais avec un nombre de phases d'entrée élevé (27) afin de tester la commande et le contrôle du PPMC en temps réel et aussi de vérifier les calculs théoriques donnés en première partie de ce travail. Les développements amenés tout au long de ce travail

permettent de donner une appréciation quantitative du rendement énergétique du PPMC et de mettre en évidence les paramètres clés par lesquels il est possible d'améliorer ce rendement. Dans certains cas, le rendement du PPMC est admissible pour l'application sous la condition qu'un paramètre du générateur (la réactance de fuite) reste au-dessous d'une valeur critique. Le travail est ponctué par une liste de propositions de développements futurs relatifs au PPMC et au projet d'innovation AG.

Mots clefs: conversion de fréquence, électronique de puissance, centrale électrique, turbine à gaz, vitesse variable, train d'engrenages, rendement énergétique, surtension, circuit de protection, commutations naturelles, commutations forcées, temps de commutation.

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Chapter 1 - Introduction

1.1 Context and structure of the work

The "Active Generator" (AG) provides the framework of this PhD thesis. The AG principle, as shown in Fig. 1.1, describes a non-classical arrangement of a power generation utility, which consists in the insertion of a static frequency converter between the electrical generator and the electrical 50Hz (or 60Hz) grid. In general, the AG principle is associated installation of a power range of several hundreds of MW per generation group. The AG principle was first mentioned in [1], [2] and [3] where the prime mover is a gas turbine. At EPFL's LEI, two PhD thesis have been dedicated to the AG principle [13] and [14], both of them focus on the analysis of a specific converter topology in order to assess the feasibility of the given topology for the AG application. Similarly, in this PhD work, a new static frequency converter is proposed and its feasibility is analyzed. This new converter is derived from existing converters and is called gate-commutated "Poly-Phased Matrix Converter" (PPMC).

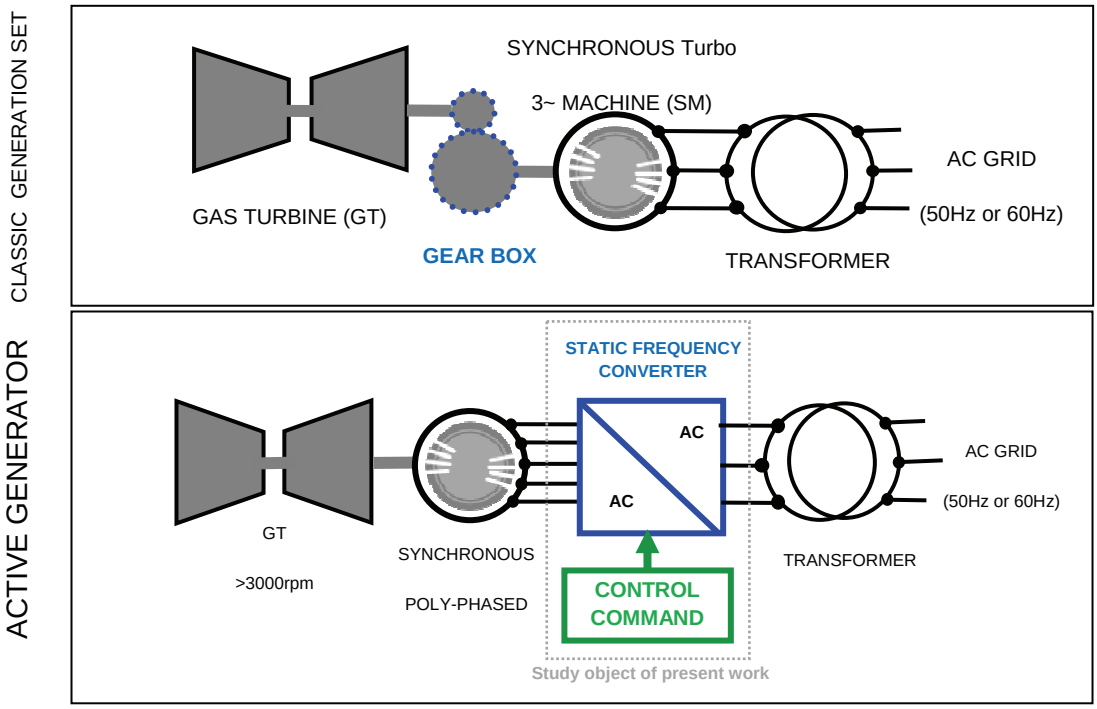


Fig. 1.1– Classical vs. Active Generator layout of a power utility

The next section of this introductory chapter presents an overview of the AG principle and a review of the literature related to this topic. This review leads to the presentation and justification of the proposed new converter. Fig. 1.2 (right) shows a simple schematic of the PPMC, which is a direct frequency converter, gate-commutated as opposed to the line-commutated converters proposed in the literature (Fig. 1.2, left). The PPMC is linked to an interesting and advantageous commutation sequence previously mentioned in the literature [1] but never used efficiently because of the limitations of natural commutations. This commutation sequence is renamed slow "Cosine Waveform Crossing" (*slowCWC*) in this thesis, as a result of a detailed analysis and comparison with the better known CWC (Cosine Waveform Crossing) sequence, as defined in [5]. As this sequence plays a key role in the proposed new topology, chapter 2 presents the theory about commutation sequences for poly-phased direct frequency conversion application.

Chapter 2 details the steps that, from the existing commutation sequence, lead to the commutation sequence *slowCWC*. The interesting input and output properties of the *slowCWC* sequence are highlighted with frequency spectrum of ideal waveforms. Those properties are important because they have a strong influence on the elements connected on each side of the converter. This chapter also introduces the basic commutation cell which will be used extensively throughout this work. In particular, to achieve the *slowCWC* sequence, the basic commutation cell shows that the PPMC must be able to perform natural and forced commutations. By appropriated command algorithm, one can choose to operate the PPMC only with forced commutations or with a mix of forced and natural commutations, i.e., the full forced or the mix mode.

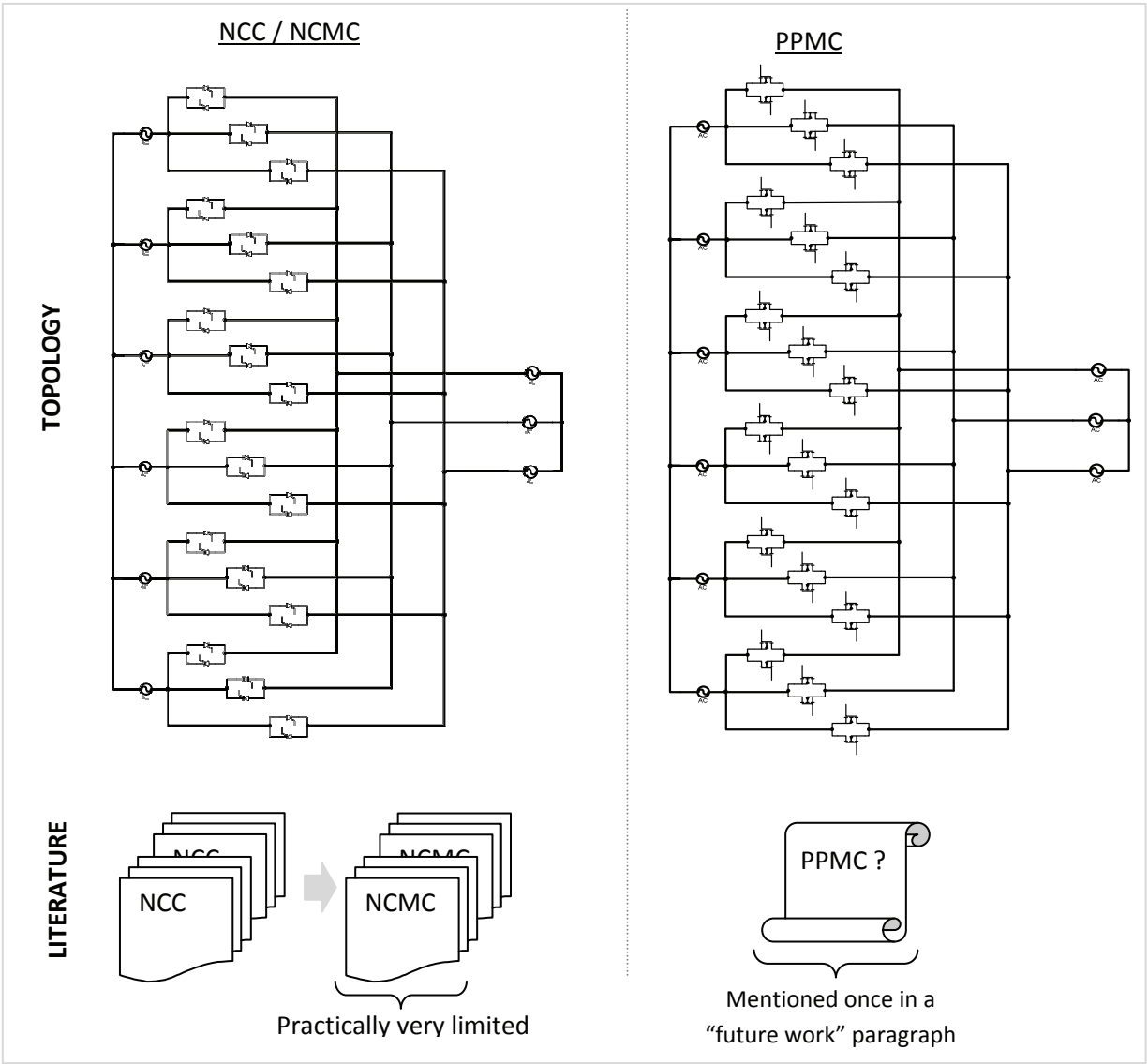


Fig. 1.2 – State of the art of Topology and literature for AG principle

Chapter 3 and chapter 4 are the core of this work. Chapter 3 presents in details the new proposed static frequency converter, the PPMC. Because the PPMC operates with the *slowCWC* sequence, some of its commutations must be forced, which requires to add a passive protection circuit (or free-wheeling path) across each input phases to avoid destructive overvoltages. The presence of this free-

wheeling path modifies the basic commutation cell. Chapter 3 gives a detailed analysis of the modified commutation cell. This detailed analysis is essential in order to understand the PPMC operation, in order to evaluate its energetic properties and in order to select a suitable mode of operation, i.e. full forced mode or mix mode. The particularity of the analysis of the modified commutation cell is that it expresses the results in a per unit system where the relative parameters of the generator and of the protection circuit also appear. The relative system allows to highlight how each parameter influences the studied properties. Chapter 3 gives an original analysis of the duration of natural commutation expressed in the per unit system. The relative duration of the natural commutation is a key parameter that influences the type of commutations and their distribution along one period of the output of the converter. The false natural commutation and the early cut-off are phenomena that are directly influenced by the duration of the natural commutation. Chapter 3 gives an extensive study of both of those phenomena because they can have a significant influence on the energetic properties of PPMC. Also, chapter 3 gives an assessment of the conduction and switching losses of the PPMC.

Chapter 4 first develops a design method of the protection circuit that is based on algebraic equations, expressed in the per unit system defined in chapter 3. The design method gives the optimal values of the components of the protection circuit from a single design abacus, where the optimum corresponds to the minimum value of installed passive component for a given overvoltage constraint. Second, on the basis of result of chapter 3, chapter 4 develops algebraic formula that describe the energetic properties of the protection circuit and its role in the global efficiency of the PPMC. This energetic analysis takes into account two phenomena of the modified commutation cell, which are the false natural commutation and the early cut-off. This energetic analysis of the protection circuit helps to conclude on the advantage of running the PPMC with a mix of forced and natural commutations. In chapter 3 and 4, simulation results are presented in order to illustrate and verify the theoretical calculations.

Chapter 5 gives the details of the command algorithm of the PPMC. In particular, the method for the synchronization of the PPMC with the AC grid is explained. The understanding of the command algorithm of the PPMC is very important to design its power control. In this regard, chapter 5 also sets the basis for the design of a current control for the PPMC and presents some preliminary results. In particular chapter 5 highlights the dynamics limitations that are intrinsic to the *slowCWC* commutation sequence.

Chapter 6 presents the experimental set-up that has been realized during this PhD work and first experimental results. Finally, chapter 7 summarizes the obtained results to obtain a global picture of the new proposed converter. Besides, the conclusion gives a generous list of perspectives and future developments related to the PPMC and to the AG principle.

1.2 Active Generator principle overview

The Fig. 1.1 describes the AG principle. It consists in the insertion of a static frequency converter in-between the generator and the AC grid in order to de-synchronize the rotational speed of the generator and the stiff AC grid 50Hz (or 60Hz). The AG concept also recommends to use a direct static frequency converter with a naturally commutated sequence. Likewise it recommends the use of a poly-phased generator, i.e. a synchronous machine (SM) that has a number of stator windings

higher than three. To be noted that the generator is still referred to as a “Synchronous Machine” (SM) because its basic operation principle is identical to a standard three-phase SM. The converter topology and the commutation sequence will be described in detail in chapter 2 and 3. The next paragraph presents the main advantages of the de-synchronization, or variable speed feature of the AG.

1.2.1 Motivation for de-synchronization (or variable speed)

For power generation utilities connected to an AC grid, like wind turbine, hydro power plants or even gas/steam turbine driven generators, the variable speed feature can offer several advantages that are listed below.

- part load efficiency optimization
- elimination of gear box
- unique prime mover design for several grid frequencies
- control of power flow through the static converter (FACTS functionality)
- elimination of the auxiliary converter for start-up

Without the variable speed feature, the prime mover’s rotational speed is linked to the grid frequency by a factor that depends on the number of poles of the electrical machine and on the ratio of the mechanical gearbox, if any. For a SM with two poles, the rotational speed of the shaft is 3000rpm,. For a SM with four poles , the rotational speed decreases to 1500rpm. The prime mover is designed for a given nominal rotational speed and delivers a nominal power at this speed with the nominal efficiency, assumed to be the best one. If the optimal rotating speed does not match 3000rpm or 1500rpm, a gear box is inserted between the prime mover and the generator. In general, the efficiency curve of the prime mover in function of the delivered/absorbed power with a fixed rotational speed has the shape of a bell. This means that the part load operation of the prime mover degrades the efficiency. Briefly, the reasons for this bell shape efficiency curve are to be found in the mechanical and thermal laws governing those machines (e.g. a fixed orientation angle of runner blades). Examples of bell-shape efficiency curves can be found in [40] for gas turbines and in [48] and [59] for hydro turbines. The variable speed feature, achieved with a frequency converter, allows adapting the speed to operate the prime mover on its maximum efficiency point for whatever the load is. Usually, this requires a relatively small speed variation, in the range ±30% of nominal speed.

The gear box inserted between the prime mover and the generator allows an optimal design of the mechanical prime mover but becomes a drawback for high power installation (maintenance, noise, efficiency, space and cost). For high power, if no gear box is used, the fixed rotational speed of 3000rpm or 1500rpm forces design trade-off of the rotating machines, and often compromises the efficiency of those machines. In this case, the replacement of the gear box by a static frequency converter allows to design the prime mover with the desired rotational speed without the burden of the gear box. However, the frequency ratio could then easily reach the value of 50% or more, which represents a speed variation greater than the one required for the function of maximizing the efficiency point, described above. The required frequency ratio for the frequency converter will strongly influence the converter-machine arrangement, as discussed below.

FACTS functionality: The power control will be achieved through control of the converter output in terms of phase shift and magnitude. This strategy will surely change the rules for the design of the

SM in term of internal impedance. The presence of the converter between the machine and the network considerably redefine the dynamic of the power plant and all the issue around the tripping of the group in case of short circuit on the network side.

1.2.2 Converter-machine arrangement

Before power electronics and converters were available on the level of industrial products, frequency conversion was realized by the use of back to back and cascaded rotating electrical machines and playing with the windings connections and voltage levels. Discussing this arrangement here is beyond the scope of this thesis. Today, the advances in the power electronics field allow to build satisfying frequency static converters. There are two possibilities to de-synchronize the electrical machine. Either the converter is placed between the grid and stator of the machine or it is placed between the grid and the rotor of the machine. In the latter case, this requires an asynchronous machine with an accessible three phase wound rotor (through brushes usually). This arrangement is often referred to as Doubly Fed Induction Machines (DFIM). The DFIM arrangement is very efficient and the nominal power of the converter is only in the order of $s*P_N$ where s is the slip speed and P_N is the nominal power of the fed machine. In practice, s ranges between 0 and 0.3 in order to keep the eddy current losses in the rotor low. Unfortunately, in the AG principles because the frequency converter replaces the gear box, the sliding speed s would be too large and the elegant DFIM solution must be discarded. That is why, in Fig. 1.1, the static frequency converter is inserted between the grid and the stator of the SM. The nominal power of the converter is equal to the nominal power of the SM.

1.2.3 Variable speed power generators applications in the world

Variable speed applications are wide spread in the field of hydraulic pump/turbine storage machinery (mostly in a DFIM configuration) in order to run the hydraulic machines with the best efficiency whatever power is demanded. In case of a pumped storage plant, the optimal rotational speed of both pump and turbine mode are usually different. With variable speed, pump and turbine mode can both work at their best efficiency for a range of operating points. For large gas turbines power utilities, no realization has been reported in the literature with the exception of the starting devices. Table 1.1 gives some examples of real applications of variable speed.

Table 1.1 – A few samples of variable speed power generation applications in the world

Place	Year	Mechanical mover	Configuration	Nominal Power	Speed range
Ukraine	1985/1991	Turbine (steam)	DFIM	200MW	-
USSR	1960-1962	Hydro (turbine)	DFIM	50MVA	-
Japan	1980	Hydro (Pump/turbine)	DFIM	360MVA	+8/-10%
Japan (Ohkawachi)	1993	Hydro (Pump/turbine)	DFIM (NCC)	400MVA	330 to 390 rpm
Germany (Goldisthal)	2004	Hydro (Pump/turbine)	DFIM (NCC)	2x265MW (1060MW total installed)	+4%/-10%
Japan (Yagisawa)	1991	Hydro (Pump/turbine)	DFIM (NCC)	82MW	130 to 156 rpm
Germany (GROWIAN project)	1983	Wind	FSC	3MW	+30%/-90%

Sources: [12], [18], [42], [44], [45], [48] to [54]

1.2.4 Converter and Generator requirements

As written above, the variable speed features should also be applied for large Gas Turbines (GT) power gen sets. This would remove the gear box, eliminate the start up converter but add the main frequency converter.

In the AG literature, a converter topology and its associated sequence are recommended. The precise choice of the best converter topology needs criteria in order to compare topologies among them. Most of these criteria are technical and are listed in Table 1.2 and commented hereafter. The economical criterion is also important but won't be taken into account in this thesis, because it relies on cost functions that can widely vary with time and the politico-economical situation.

Table 1.2 – Criteria for AG frequency converter

Criterion	Importance for AG
Weight	Not critical
Space	Not Critical
Efficiency	Critical
Output quality	Critical
Dynamic Behaviour	Critical

Weight: the weight of the converter is not critical because it is not a mobile application.

Space: the required room to build the converter is not critical because in the context of a high power generator set, the GT already requires a large room and there are no high constraints on available room.

Current and voltage quality: as the converter is connected to the grid and is part of a generation utility, the requirements in terms of THD of the output voltage and currents are severe. For example the THD requirements for a 110kV connection point are 2.5% for voltage and current [15]. There are also harmonics not to be over passed. On the side of the generator, the THD of the stator current should be limited to avoid heating losses.

Dynamic behavior: Power generation installations must fulfill a set of given conditions during transient behavior when connected to the grid. It also helps maintaining the grid. The kind of transient behavior that he power generation set must be able to manage correctly will not be discussed in this thesis.

Efficiency: in the context of power generation, the efficiency of the converter is critical for obvious ecological and economical reasons. However, one should above all consider the global efficiency of the power plant. In this respect, there could be special power plant configurations where the relevance of the converter's efficiency is relatively low. This could be the case if a combined cycle power plant configuration is used, where the losses of the converter could be used as heat source in a CHP system.

If the role of the converter is only to replace the gear box, then in order not to alter the overall efficiency, the converter must have a similar efficiency as the gearbox. To be more accurate, the converter effect on the generator must also be taken into account. The waveform of the currents in the generator windings will have to be defined in detail in order to assess this effect.

Table 1.3 provides examples of efficiencies of the components of the power generation set. The efficiency of the generator is given for two configurations: connected to a converter or directly to the grid. The efficiency of the gas turbine is given for two cases: in variable speed or fixed speed mode. Each efficiency value is given for a nominal point and for a 50% part load. These are only approximation and only the order of magnitude is to be considered here. Those values are taken from [15] in which the static converter is a NCMC from which the PPMC is derived. For the full load, it is important that the effect of the converter on the generator efficiency is reduced, and the converter itself must have comparable efficiency with the gear box, or even slightly higher to compensate for the reduction of the generator efficiency. Overall, it is clear that for full load, the gain in efficiency of the AG is not a key motivation. To be noted in the values presented in Table 1.3 the classical configuration contains a gear box, so in the design of the Gas turbine its nominal rotational speed is a freedom degree. It could be that for high power, the use of a gear box is discarded which cancels this freedom degree which in turn would affect the GT efficiency. In this case the AG configuration would be advantageous.

Table 1.3 – Numerical examples of efficiencies of the components involved in an AG generation set

Device	Efficiency		
	Symbol	Typical nominal value	50% load efficiency
Gas turbine without var. speed	η_{GT}	40	20 to 30
Gas turbine with var speed	η'_{GT}	40	40
Gear box	η_{GB}	98.5	97
Generator without converter	η_{Gen}	98.2	97.6
Generator with converter	η'_{Gen}	97.8	96.4
Converter	η_C	99.6	99.5
Overall Classical solution	$\eta_o = \eta_{GT}*\eta_{GB}*\eta_{Gen}$	38.7	18.9 to 28.4
Overall AG solution	$\eta = \eta'_{GT}*\eta'_{Gen}*\eta_C$	38.9	38.4

Sources [15]

For the part load, the increased efficiency of the GT with variable speed largely compensates for the negative effect of the converter on the generator and for the converter the own part load efficiency decreases.

In the literature of thermo-dynamical engineering, GT efficiency in different configurations has been discussed. Fig. 1.3 from [40] shows examples of GT efficiency in function of relative delivered power, from no load to full load, for different configurations. There are several means to enhance the efficiency of a GT, which constitute a purely thermo-dynamical solution. Besides, there is the variable speed solution, which is the curve #1 in Fig. 1.3. Although Fig. 1.3 is given for medium power GT, we assume similar tendencies for higher power GT. This clearly shows the high potential of variable speed for increasing the part load efficiency of a GT.

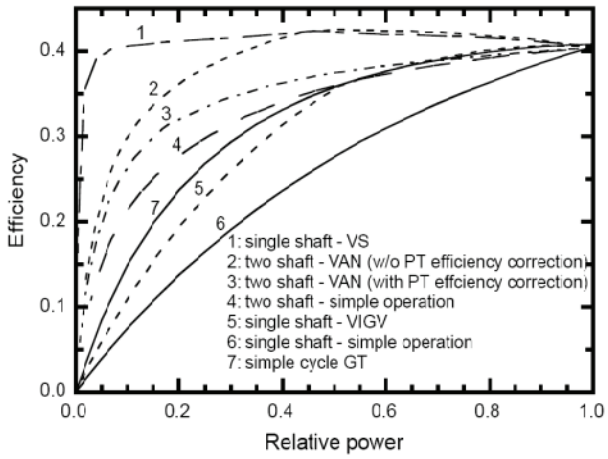


Fig. 1.3 – Example of different configurations and various part load operation strategies of GT (source [40])

Even if the overall efficiency is mainly affected by the GT efficiency, it is important for electrical engineering to keep the high efficiency converter and make all possible effort to gain a few efficiency points in order not to cancel out the effort from the mechanical engineering part to gain a few efficiency points. But it is clear that most improvements are in the hands of mechanical engineers.

1.2.5 Frequency converter topology

The literature about AG principle, as said earlier in this section, has already recommended a converter topology and a respective commutation sequence. Here, a brief review of frequency converter topologies is provided to understand the recommendations made in the literature about the AG principle.

Indirect Converters vs. Direct

A frequency converter is a power electronic circuit that permits to interconnect two AC power sources which have different frequencies and optionally different voltage levels. There are two main categories of frequency converters: indirect and direct converters that are depicted in Fig. 1.4. Both categories can perform frequency conversion along with voltage adaptation. They also can both deal with bidirectional power flow.

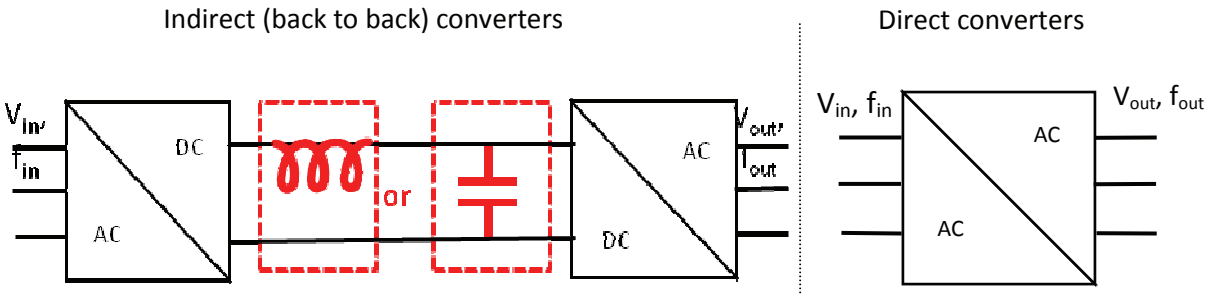


Fig. 1.4 – Two main AC/AC converter categories

The indirect converters process the conversion in two steps: a rectifying step followed by an inverting step. Those converters absolutely need a DC energy storage unit for their DC link, either a large capacitor or a large inductor. The load current has to go through two silicon stages. This technology is very well known and practically used. Back to back Voltage Source Converter (VSC) or Current Source Inverter (CSI) are practical implementations of the indirect conversion.

The direct frequency converters process the conversion in a single step. They skip the rectifying process and do not store energy inside. They take portions of the input sine waves to build the output wave with the desired frequency (lower) and possibly desired harmonic contents. This solution does not require any device for energy storage but has a strong influence on both sides in terms of frequency content. The load current flows through two stages of silicon devices. For direct converters, there is abundant literature and practical realizations on Naturally Commutated Cyclo-converters (NCC) [5], [16] and [18] or Matrix Converter [19], [55] to [57]. Another argument in favor of the direct converters is the advantage of avoiding a double conversion that results in a cascade of partial efficiencies.

Switching frequency

Both categories of frequency converters can be operated with a high switching frequency ($F_{switching} >> F_{out}$) or a low switching frequency ($F_{switching} >= F_{out}$), where the switching frequency is the frequency of use of one switch. Both categories can be run with high or a low number of levels. The number of levels directly influences the resolution of the quantification of the ideal output waveform the converter should produce. To obtain the desired ideal output waveform (a pure sinus), it is required to place an output filter that selects the fundamental or wanted component. Usually, in order to keep the size of the output filter reasonable, a low number of levels implies to operate the converter with a high switching frequency, whereas a low switching frequency implies a high number of levels. The THD of the output voltage of low commutation frequency switching converters can be improved by increasing the number of input phases, as suggested in [1] and [6]. The needed number of input phases depends mainly on the THD requirements on the output waveforms. To comply with the grid codes' constraints, the number of input phases is usually set to 20 and higher.

For direct converters, a high number of levels is obtained by increasing the number of input phases. In general, on the side of the source of the converter, it is not acceptable to have high frequencies in the spectrum of the current. A high switching frequency requires an additional input filter which might not be necessary with a low switching frequency combined with high number of levels.

1.3 Towards the proposed new converter

Most of the literature of the AG principle recommends using a direct frequency converter in order to get rid of the supposedly costly and dangerous DC storage component. In some applications this DC storage component plays a second role of energy reserve for a short duration. In the AG case, this short reserve is available from the inertia of the generator rotor. However reference [14] presents a back to back configuration in the frame of AG principle. The reference [14] suggests a special back to back three or five levels NPC in a low switching frequency (square mode), which shows excellent efficiency. However it requires a DC intermediary capacitor and an output filter. The AG literature about AG assumes here that a high switching frequency is not suitable for high power applications

because of too high commutation losses and because of the necessary input filter to decrease high frequency current harmonics that the generator cannot accept. The modeling of a poly-phased generator has been newly covered in detail by [43]. This reference will certainly help in assessing the constraints to observe in terms of current harmonics allowed into the generator stator to keep damper cage losses low and torque ripple in a reasonable frame.

With the given recommendation of direct conversion, no input filter and slow switching frequency, the NCC topology would be an eligible solution, provided that the input phase number is high enough. Usual NCC count up to 12 input phases (12 pulses NCC). The NCC is attractive and suitable for high power since it uses thyristors as valves. However, the NCC and its associated switching scheme, the Cosine Waveform Crossing (CWC), present one big disadvantage, i.e. reactive power consumption. More precisely, the CWC makes the input displacement factor of the input sources more reactive than the power factor of the grid. This usually implies an over sizing of the generator in term of apparent power. To get rid of this issue, it is suggested in [1], [2] and [3] to use a switching scheme, derived from CWC, which makes the input displacement factor equal to the load angle and, by the way, reduces the commutation number per output period compared to the CWC. In particular, [4], [7], [8], [9], [10] and [15] studies the implementation of this scheme using thyristors and only natural commutations. In the literature, this converter is called the NCMC (Naturally Commutated Matrix Converter) where the reference to the matrix converters is due to the matrix configuration of the valves of the NCMC (Fig. 1.2 top left). The natural commutations imply delaying some of the commutation instants, which limits the real application of the suggested slow switching scheme. The practical implementation of the NCMC is restricted to some lagging operating points only, which is of course not compatible with the requirement set by the AG principle. Indeed, a power plant must be able to deliver power with leading and lagging operating points, even within a restricted range, but at least unity power factor must be achievable. For those reasons, the NCMC should be discarded.

It comes out that recommendations about converter topologies are made and a certain direction is privileged but there are no satisfying practical converters for this direction that is studied, nor available. In response to the recommendations to use a direct converter with a given slow switching scheme and a high number of levels, a straightforward converter topology would be to replace the thyristors of the NCMC with transistors in order to get rid of the natural commutation limitations. This idea is indeed briefly mentioned in [15] as a future work. This leads to the proposed new converter, named gate-commutated "Poly-Phased Matrix Converter" (PPMC), which is shown in Fig. 1.2 (right) in a simplified schematic. The aim of the thesis is to investigate the PPMC topology and highlight its pros and cons. The detailed structure of this work is given earlier, in section 1.1. This work aims at clarifying the recommendations found in the literature about the converter topology choice, but does not pretend to be a tool to select the best converter topology for the AG application.

Chapter 2 - Poly-phased direct frequency conversion

2.1 Introduction

It has been said in the previous chapter that a new switching method was suggested in the literature, denoted here *slowCWC*. In order to give more insight and to show how to derive the slowCWC sequence this chapter addresses the synthesis of a sine waveform of a given amplitude and frequency from a set of *m* sine waveforms input with different, generally higher, frequency and amplitude. This is the poly-phased direct frequency conversion. Fig. 2.1 (left) illustrates the general problem of curve synthesis. Which input curve is to be selected at what time to follow a given target curve, and how to select it, are the basic questions to answer to perform the synthesis of the target curve (black curve). The possible sequences to synthesize the target are:

- Venturini's PWM modulation and its multiple derivate forms
- Minimum error sequence
- Cosine Waveform Crossing (CWC)
- ***slowCWC***

The PWM and the *CWC* sequence belongs to the state of the art and are largely used in industrial applications. As stated in chapter 1, the PWM commutation sequences are discarded for the AG application and will not be exposed here. *CWC* and *slowCWC* are exposed and detailed in two sections of this chapter.

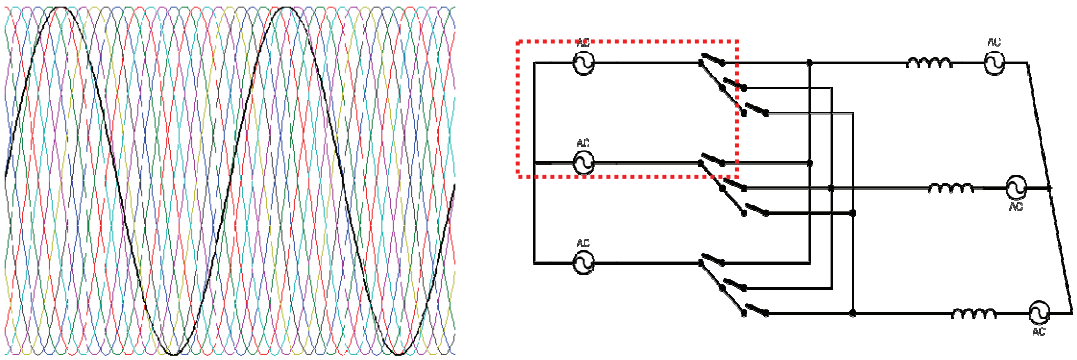


Fig. 2.1 – Illustration of direct frequency conversion and associated converter structure

The general structure of converter used for direct frequency conversion is given in Fig. 2.1 (right). Each output phase can be connected to any input phase. Generally the output is considered as a current source that should not be interrupted and the input is considered as voltage sources that should not be short-circuited. A PWM sequence does not require more than three input phases since the resolution of the output voltage or current is ensured by appropriated filters made feasible by the high switching frequency. The 'line-commutated'-like commutation sequences (*CWC*, s*lowCWC*), i.e. sequences with commutation frequency being a close multiple of the input frequency, ensure the resolution of the output waveform by a sufficient input phase number, noted *m*. Whatever commutation sequence is used, PWM or line-commutated, the output current has to be commutated from one input phase (outgoing) to another (incoming). The commutation cell, the part of the circuit that contains both outgoing and incoming input phases, as highlighted in Fig. 2.1 (right), is a key concept to understand in order to say if a commutation sequence is feasible and working

properly. As a reminder or for clarity of this chapter, the next section briefly exposes the basic commutation cell principle and properties.

2.2 Basic commutation cell

2.2.1Transient response of commutation cell

The commutation cell highlighted in Fig. 2.1 (right) is isolated from the whole converter circuit and drawn in Fig. 2.2. Again, the nature of the input and output source is considered voltage and current resp. They are real sources and have an internal impedance. This impedance will help the commutation process in some situations, in other situations it will be a problem to be addressed. As can be seen in Fig. 2.2, DC sources are used in this basic cell to represent the circuit during the commutation. For this approximation to be valid, the commutation duration must be short compared to the period of the input period. No precise numerical limits are given here since it depends on a lot of parameters.

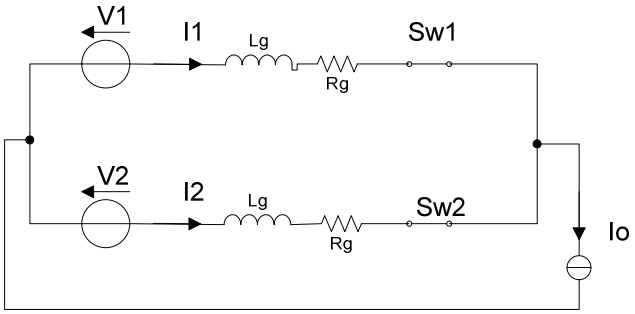


Fig. 2.2 – Basic commutation cell with outgoing (V_1) and incoming (V_2) input phases

The closing of one switch does not lead to any violation of the basic rules of power electronics. However, when opening a switch which was conducting a current, one must ensure that there is a free-wheel path for this current, otherwise we do not respect one interconnection law. This free-wheeling path is normally ensured by closing the incoming switch (SW_2 , new generator phase). As switching (on and off) duration is not instantaneous both outgoing and incoming sources are short-circuited. The short-circuit between two real voltage sources composed of one ideal voltage source plus one series internal impedance (resistive inductive), lead to a short circuit current $I_c=\Delta V/(2R)$. Generally R is such that $I_c>>I_o$ The time constant of the transient phenomena just after the short circuit of both input phases is L/R. ΔV is the voltage difference V_1-V_2. There are two possible responses to this short-circuit, which are illustrated in Fig. 2.3 and commented here.

If ΔV and I_o are both positive or negative, then the situation is not helping the commutation (increase of current in outgoing phase, decrease of current in incoming phase). However if ΔV and I_o are of opposite signs, the outgoing current decreases and the incoming current increases. Hence, the current in the outgoing phase will cross zero. If using unidirectional switch with a blocking capability at current zero crossing, this process will automatically stops and the desired commutation is done. It is called a **natural commutation** which is largely used in NCC. The basic commutation cell is a very simple model of the input source with a given fixed internal impedance (L and R). In reality, especially

if the input source is a SM or ASM, the internal impedance to consider is not necessarily constant and can vary with time. In this regard there is a more detailed analysis about proper conditions for natural commutations in [3] but for the present study in this work, the above condition will be considered as good enough for the case studied.

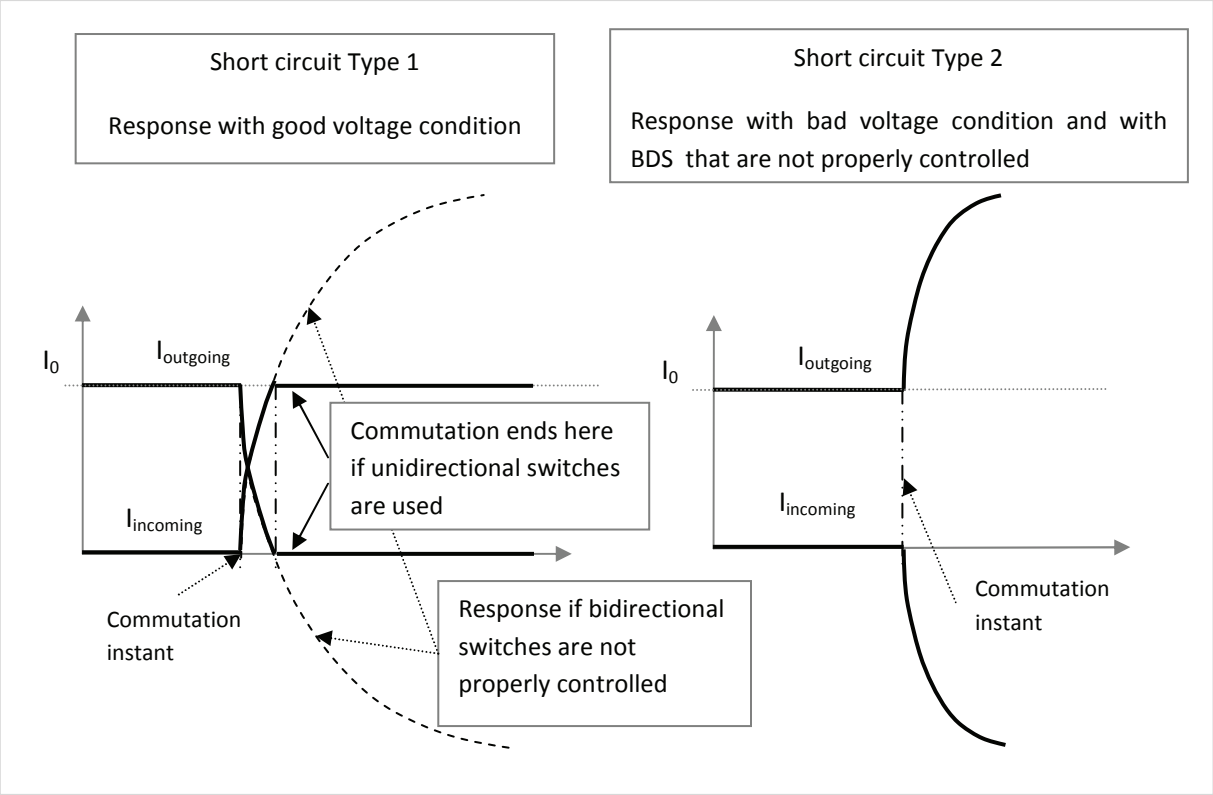


Fig. 2.3 – Types of short circuit between two input phases of the basic commutation cell

2.2.2 Nature of switches

Historically, the high voltage switches were only achievable with thyristors. When thyristors are employed, the blocking capability during current reversal is intrinsic. Thus natural commutation is possible without control. it is besides not necessary for security of the commutation to know the sign of ΔV before starting the commutation. When ΔV is positive, nothing will happens since the thyristor cannot start conducting a negative current and it is negative bias. However when thyristors are used it is required to implement a management of the zero-crossing of the load current (circulating or circulating-free current are two possibilities). Nowadays, it is more and more possible for high power to build turn-off capable bidirectional switches (BDS). They are build from transistors, usually, IGBT or IGCT arranged with power diodes as depicted in Fig. 2.4. There are several combinations which all have advantages and disadvantages. To choose the appropriate combination, one should assess the main trade-off of number of switches vs. number of *pn* junctions in the current path, which influences the conduction losses. When such transistor-based BDS are used as valves for the frequency converter, the control must be appropriated to avoid short circuit of type 2 (see Fig. 2.3) between both input phases involved in commutation cell . Besides, depending on the gating signals

control, the reverse blocking capability is not guaranteed. It is however not necessary to control the zero crossing of the load current.

The two left most composition of transistor-based BDS of Fig. 2.4 (common source and common drain) offer the possibility to independently control each direction of the current however the control of the firing signals is more complicated than the diode bridge composition (right most in Fig. 2.4). For the common source or drain configuration, a special gating signals control can guaranty the automatic blocking capability at current reversal, which secures the commutation and avoids short circuits of type 2 (see Fig. 2.3). Control of commutation with real BDS in matrix converters are well described in [20], [21] and [24]. The common source configuration is mostly used in matrix converters. With this BDS configuration, there are four gating signals involved in one commutation which are described in the next paragraph.

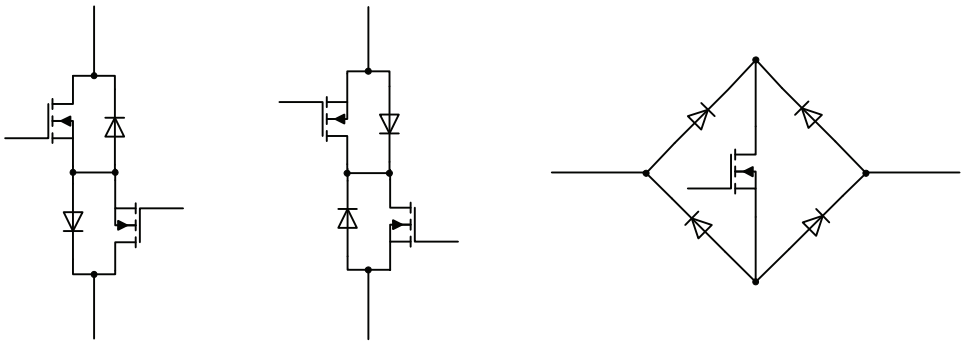


Fig. 2.4 – Transistor-based BDS: common source or emitter, common drain or collector, diode bridge (left to right)

2.2.3 Four steps commutation rule

Fig. 2.5 describes the four steps commutation rule, as described in [21] that will be used later in this work. The first step ensures blocking capability at current zero crossing. Step 2 prepares the free-wheeling path and commutation starts at this step if the conditions for natural process are met. If not, nothing happens. Step 3 finishes the commutation. In case of natural commutation, noting happens here provided that the delay between step 2 and step 3 was long enough to let the natural process finish. In case of forced commutation, the current is cut off by the switch itself. Consideration of the source impedance is mandatory here for practical implementation of forced commutation. Step 4 ensures the automatic current reversal through the switch in case the load current crosses zero during the conduction period of the phase U_2 of Fig. 2.5.

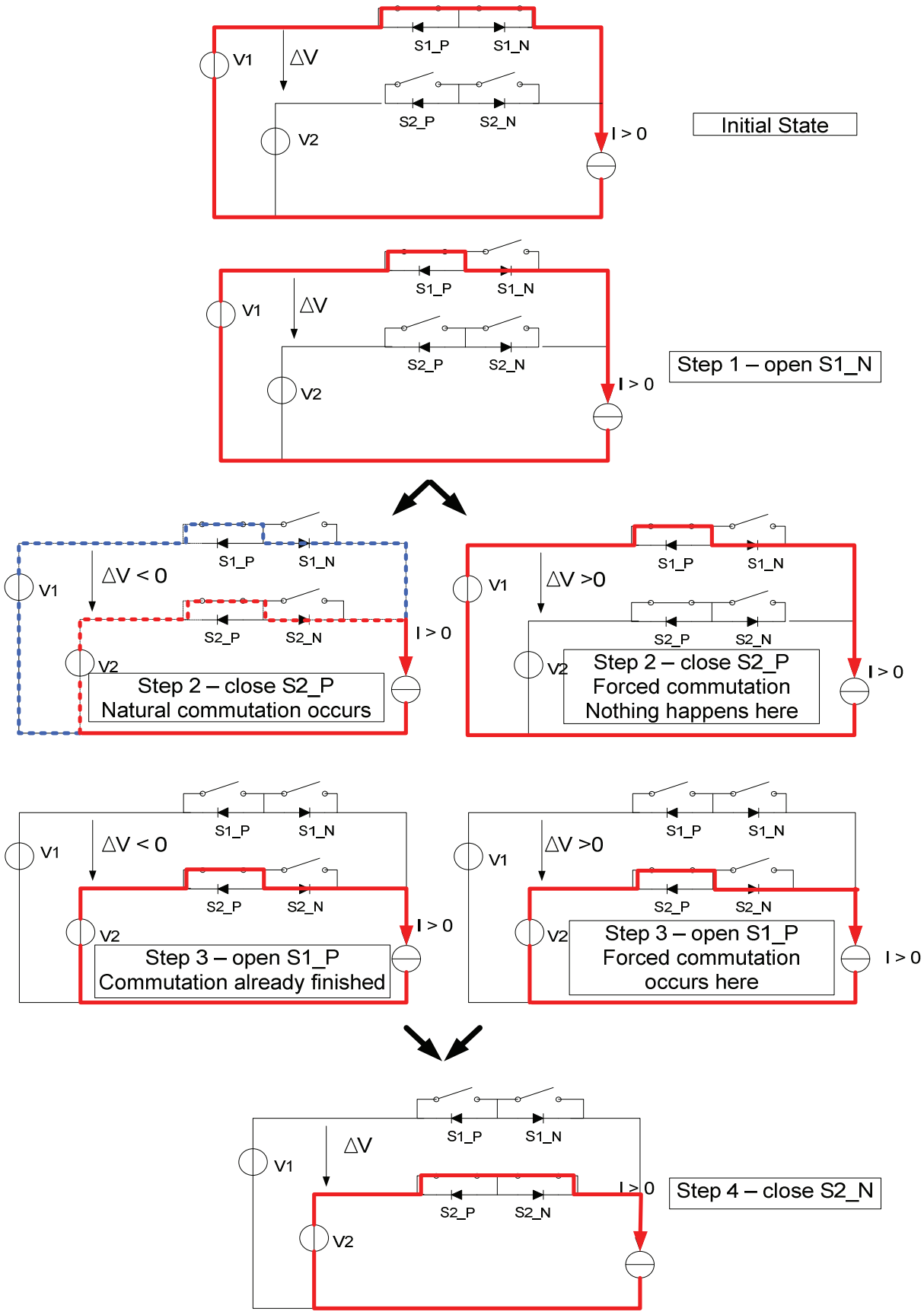


Fig. 2.5 – Four steps commutation rule of the basic commutation cell

2.3 Minimum error sequence

Before presenting already existing commutation sequences or modulation for direct AC conversion, this section shows one possibility which is very intuitive. Switches are assumed to be ideal, bidirectional and have turn-off capability.

Minimum error principle

Very intuitively, one would recommend to build the target curve from segment of the whole set of available input voltages, by each time, selecting the curve that is the closest to the target one. If the number of input phases is high enough we can get a quite good approximation of the target curve.

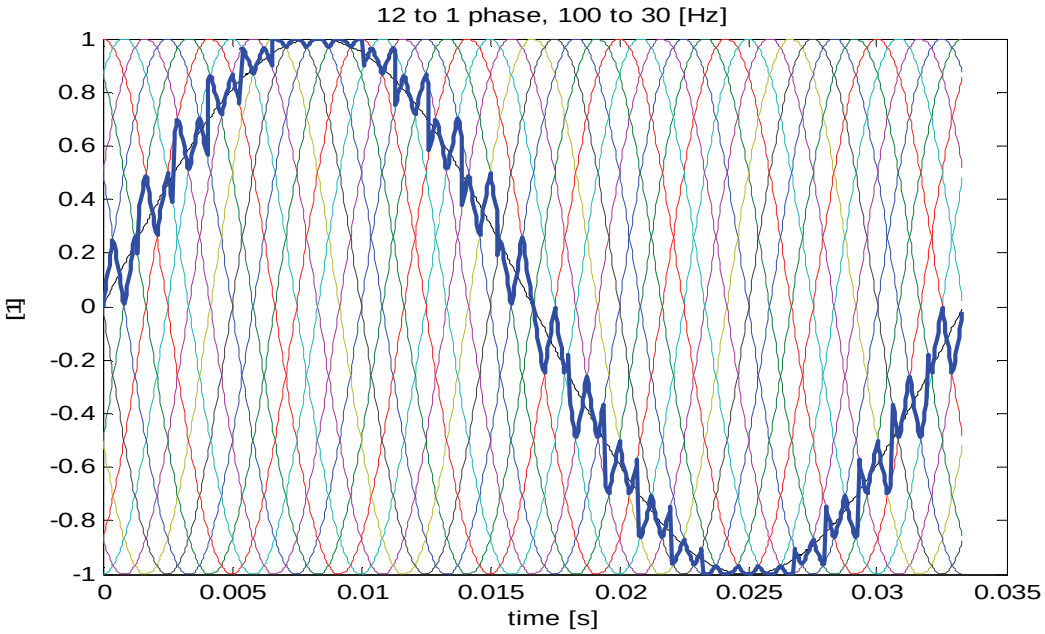


Fig. 2.6 - Output waveform of the minimum error sequence

Fig. 2.6 shows the output (bold blue) obtained when synthesizing the target curves (black) with the "minimum error" sequence from a set of twelve input phases. This algorithm delivers at first sight a quite good output curve, with a good shape. However, for further qualification of curve quality within this work, it is necessary to have criteria on which to base the assessment. Here are a few criteria for quality of a commutation sequence:

Assessment criteria

- Output THD
  The output THD is acceptable, compared to the other similar sequence presented later. The THD is independent of the frequency ratio, as can be observed in Table 2.1. There is no mathematical proof of this independency to frequency ratio for this minimum sequence. Only the numerical analysis of this sequence's waveforms shows this independency. The THD values are computed with a Matlab® script that generates the theoretical waveforms and then computes the frequency spectrum of the ideal output waveforms with an FFT algorithm. THD are deduced from the frequency spectrum. Table 2.1 gives a few numerical values:

Table 2.1 – Output THD of minimum error sequence

	98Hz to 50Hz	62Hz to 50Hz
12 input phases	**11%**	**11%**
24 input phases	**5%**	**5%**

- Degree of freedom
  The degree of freedom here is complete, both frequency and magnitude can be modulated

- Commutation frequency
  Higher than a line-commutated sequence but lower than a PWM sequence

- Type of commutation (hard/soft)
  Mix of both, statistically 50% each

- Complexity of algorithm
  Easy. It is a comparison between the set of input curves and the target.

- Input THD
  Fig. 2.7 represents the time evolution of the index of the input phase connected to the output. There are different commutation frequencies and the index jumps is always a different value, jumping forward and backward. In practice, the input is either multi-phase transformer or a generator, hence the input source has limitation in the acceptable frequency of the input current to guarantee its proper working. As can be qualitatively deduced from Fig. 2.7, the spectrum of an input current would contain some high frequency harmonics that are surely not acceptable for a generator as input source. High input current harmonics lead to high circulating currents in the damper cage and high ripple torque.

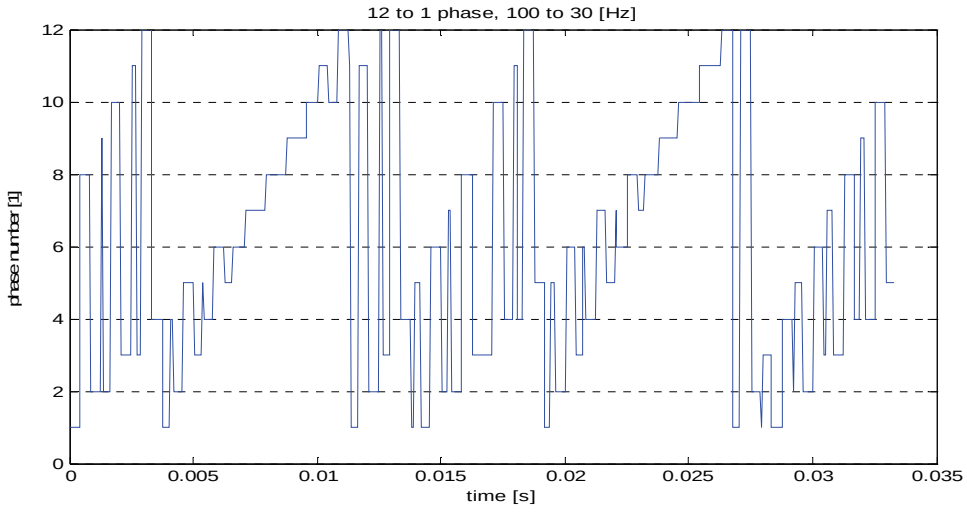


Fig. 2.7 – Input phase index evolution of minimum error sequence

2.4 Cosine Waveform Crossing (CWC) sequence

Historically, the only switches available for high power, which usually means also high voltage, were thyristors. As seen in section 2.2, with thyristors it is only possible to perform natural commutations. The *Cosine Waveform Crossing* (*CWC)* sequence has been then especially developed for thyristor-based line commutated converters, named Naturally Commutated Cyclo-converter (NCC). The *CWC* is presented here because the commutation sequence that will be under study along this work, called *slowCWC*, is very near to the *CWC*. A very well known reference about *CWC* can be found in [5]. Fig. 2.8 (top and bottom) shows two ideal waveforms of the *CWC* sequence for two different output power factors. Intuitively, one can observe that the *CWC* is the minimum error sequence with restriction to natural commutation only.

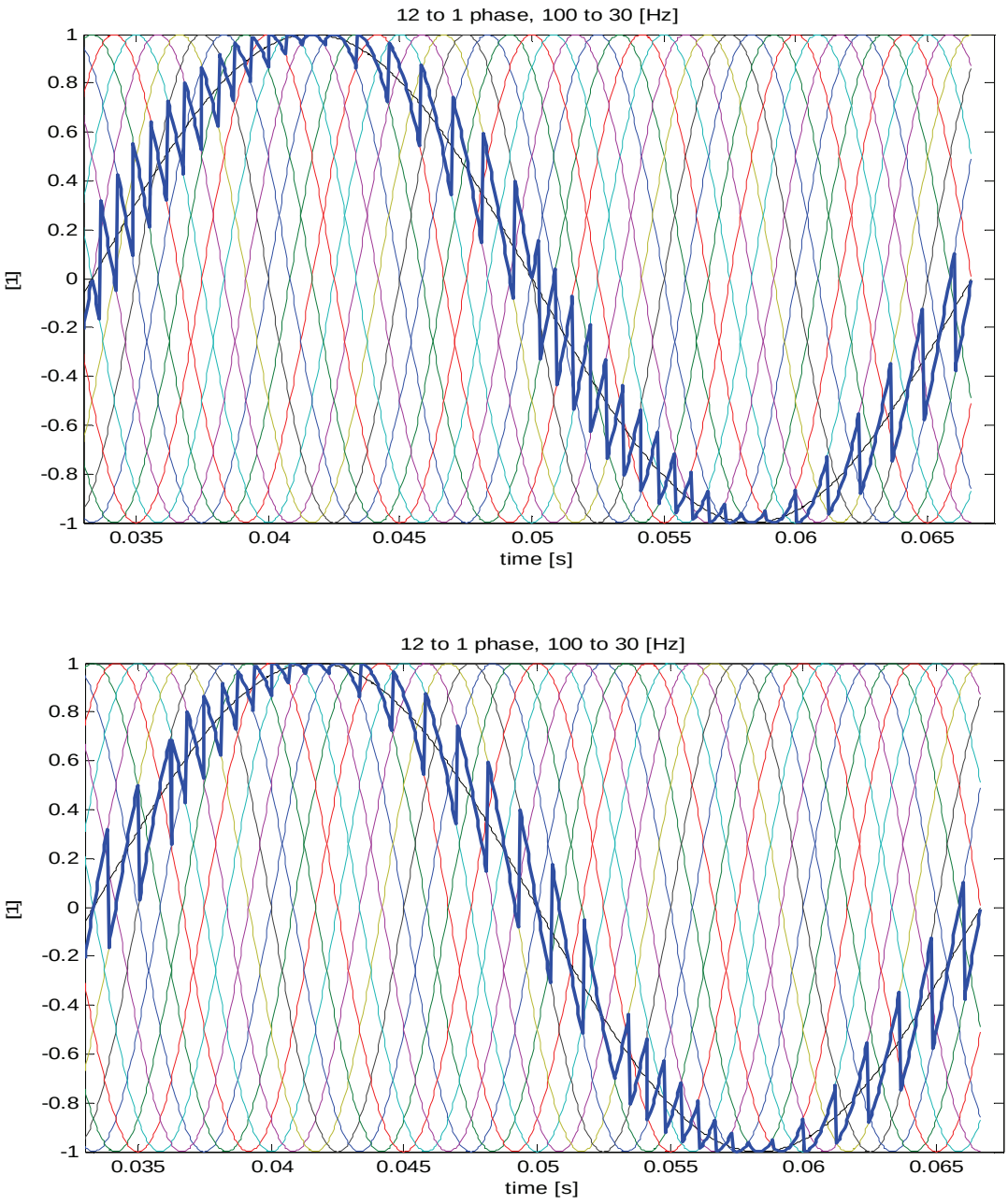


Fig. 2.8 – Output waveform of CWC sequence with unity power factor (top) and 0.85 lagging power factor (bottom)

CWC principle

The CWC sequence is itself derived from the phase-controlled rectifiers control sequence. The DC mean output voltage of such a phase-controlled rectifier depends on the angle α (the phase of the control) and is given by Equ. 2.1.

Equ. 2.1 $$V_{omean} = A\cos(\alpha)$$

where *A* is the magnitude of the generator phase scaled down by a coefficient smaller than one, that depends on the number of input phases. Fig. 2.9 shows the output of a phase controlled rectifier and the place of the angle α.

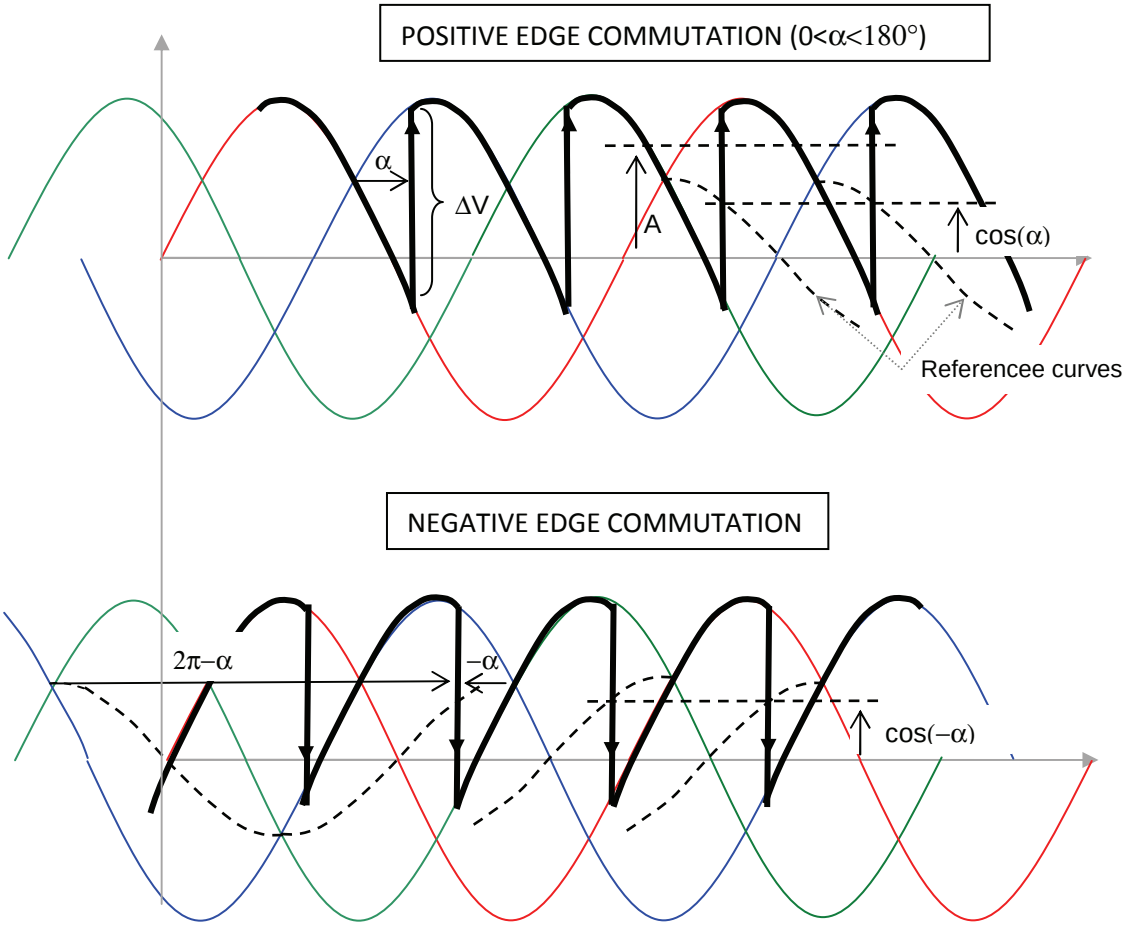


Fig. 2.9 – Positive and negative edge type waveform of a phase-controlled rectifier

As can be seen in Fig. 2.9, for the same V_{0mean} there are two possible waveforms types denoted by *positive edge* and *negative edge*, where the edge refers to the jumps from the outgoing phase to the incoming phase. As this rectifier works with natural commutation, as exposed in section 2.2, the requirement is that ΔV and the load current have opposite sign, hence depending on the load current sign, either the positive or the negative edge must be used to produce the desired $V_{omean.}$ For a similar V_{omean}, Equ. 2.2 (left) gives the relation between the α of the positive edge (α_{pos}) and the alpha of the a negative edge (α_{neg}). The idea to create a sinusoidal waveform at the output is simply to modulate the phase angle α along the time. If α increases linearly with the time, as given by Equ. 2.2 then V_{omean} is a sine waveform of desired frequency F_o. Theoretically there are no limitation on F_o, but in practice, the fundamental of the output waveform should remain the dominant component, hence usually $F_o < \frac{1}{3}F_{in}$, with F_{in} being the input frequency.

Equ. 2.2 $$\boldsymbol{\alpha_{neg} = 2\pi - \alpha_{pos}} \qquad \boldsymbol{\alpha(t) = 2\pi F_o t}$$

As the current is also be sinus, half of the output waveform will be of positive edge type and the other half of negative edge type. In practice, there are two half bridges, one being dedicated to the positive load current and the other to the negative load current. As visible in Fig. 2.9 for the same V_{omean}, instantaneous voltage of both bridges are not equal. Both positive and negative bridges are commanded to have the same mean output voltage but only one has its firing pulses enabled, depending on the sign of the output current (target value). There is also the possibility to use a midpoint inductor that reduces the circulating current between both bridges if their firing pulses are simultaneously enabled. With the circulating current mode, the zero crossing management of the load current is not necessary.

According to Fig. 2.9, a commutation must occur each time that the target output voltage V_{omean} crosses a reference voltage, which is $(v_{in,k}+v_{in,k+1})/2$, which is the mean between the conducting input phase and the next one. Fig. 2.10 (top and center) shows half a period of a target output waveform V_{omean} waveform with superimposed portion of the real converter output waveform with positive edge and negative edge type for both possibility of load current polarity (here output power factor is unity). To produce this output waveform α must vary linearly back and forth between 90° (V_{omean}=0) and 0° (V_{omean}=A), as depicted in Fig. 2.10 (top). As a consequence of the back and forth modulation of the phase angle α, the output waveform of the CWC has two distinct commutation rates, that can be easily observed in the ideal waveform of Fig. 2.8. The construction of the CWC output waveform can be translated into a spatial vector diagram where the reason for those two commutations frequencies becomes very clear.

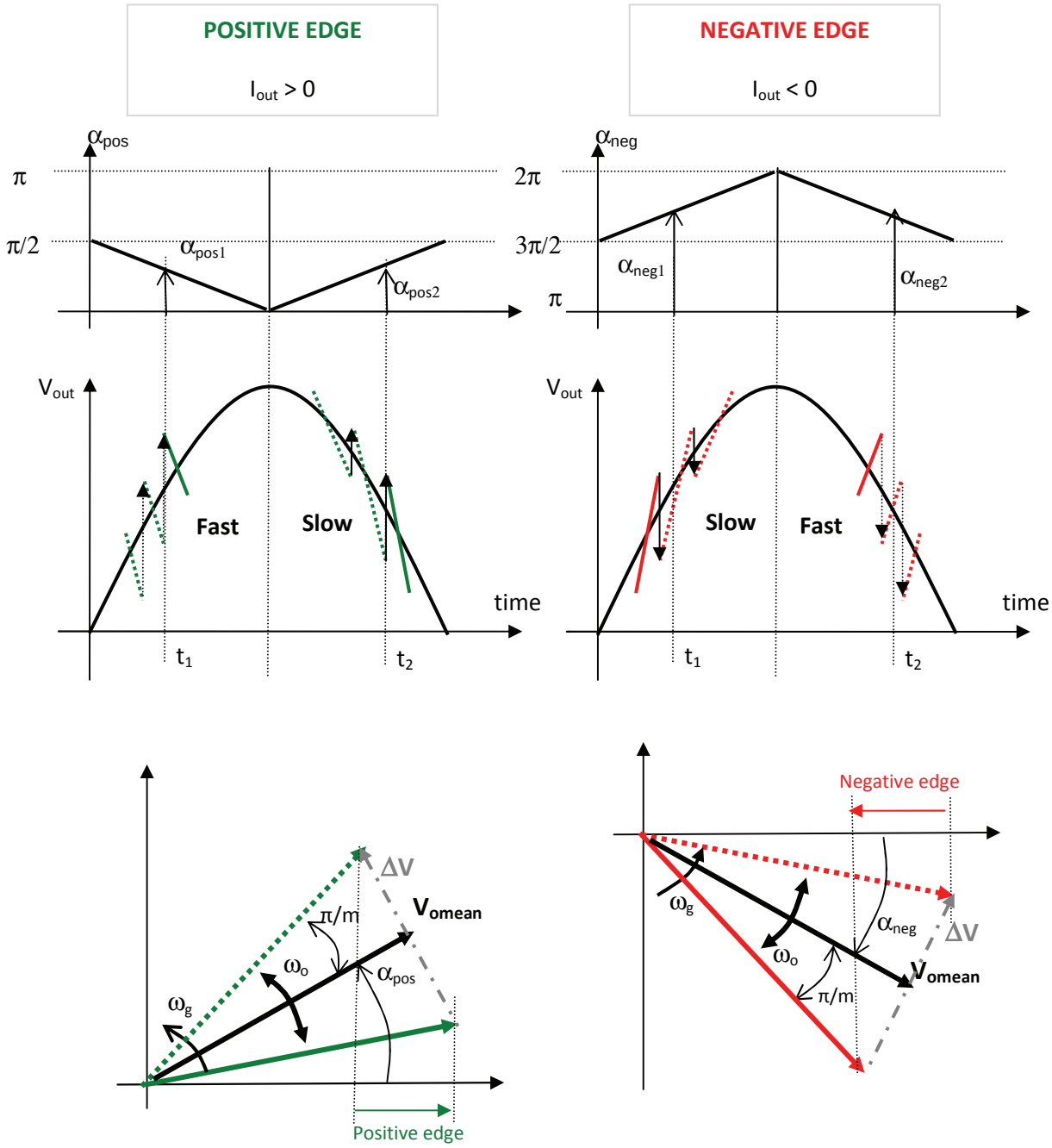


Fig. 2.10 – Type of edge and commutation frequency of CWC sequence

Normally, there should be *m* vectors representing the *m* input phases which vectors are rotating in the counter-clock wise direction with a given speed ω_g. The spatial vector diagrams of Fig. 2.10 (bottom) are however drawn for two distinct commutation instants, denoted by t_1 and t_2 and only the involved two input phases are represented. The target output voltage $V_{omean}(\alpha_{pos})$ can be represented by a spatial vector too. Now depending on the sign of the derivative of α_{pos}, this spatial vector rotates in a counter-clock-wise or clock-wise direction, for an increasing or decreasing slope of α resp. The rotating speed of this target vector is the desired output pulsation ω_o. According to the

CWC sequence, a commutation occurs at a crossing of the reference curve and the target, as depicted in Fig. 2.9. In the spatial vector diagram, this means that a commutation occurs each time the angle difference between the target and the conducting input phase is greater than π/m because the reference vector is in the middle of the conducting input phase and the next one. This is illustrated in the bottom left diagram of Fig. 2.10. Hence depending on the direction of the rotation of the target spatial vector which is similar or opposite of the input vector rotation, those crossings will occurs either proportionally to the sum or the difference of ω_g and ω_o. This gives rise to both commutation frequencies of the CWC sequence as expressed in Equ. 2.3.

Equ. 2.3

$$F_{C,\,fast} = m\left(F_{in} + F_{out}\right) \qquad F_{C,slow} = m\left(F_{in} - F_{out}\right) \quad [Hz]$$

The development is similar for negative edge type, see Fig. 2.10 (bottom right). The proportion between fast and slow depends on the power factor. One can then deduce the mean commutation frequency as expressed in Equ. 2.4.

Equ. 2.4

$$F_{C,mean} = m\left(F_{in} - \left(1 - pf\right)F_{out}\right)$$

where *pf*, the power factor of output, is accounted positive if the load current lags the output voltage.

Assessment criteria

- Output THD
  The output THD is also acceptable, compared to the other similar sequence presented later. The THD is independent of the frequency ratio. Table 2.2 gives a few numerical values, also computed with the similar Matlab® script as for the minimum error sequence:

Table 2.2 – THD of CWC output waveform

	98Hz to 50Hz	62Hz to 50Hz
12 input phases	**15%**	**15%**
24 input phases	**7%**	**7%**

  Compared to the minimum error sequence, those THD values are a bit higher for equivalent number of input phases.

- Input THD
  Fig. 2.11 represents the time evolution of the index of the input phase connected to the output. Here also, the two distinct commutation frequencies can be observed. Indeed, there are two distinct slopes of the index time evolution. The index normally jumps forward with unity steps except when switching from one bridge to the other (positive to negative or vice versa). Compared to the minimum error sequence, the input quality is better and there are surely less harmonics. The increase of the output THD is compensated here with better input quality. However it will be shown later that the input displacement factor is not satisfying.

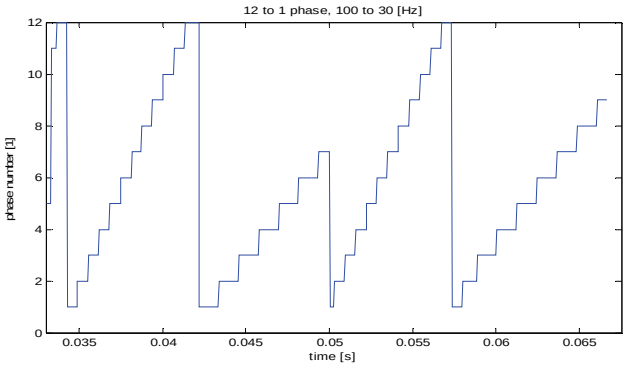


Fig. 2.11 – Input phase index evolution of the CWC sequence

- Degree of freedom
  The degree of freedom here is complete, both frequency and magnitude can be modulated.

- Commutation frequency
  Fully determined. It depends on the output power factor, on the difference between input and output frequency. Lower than the minimum error sequence.

- Type of commutation (hard/soft)
  100% soft because restrictions to natural commutations

- Complexity of algorithm
  In principle easy but there are technical issues that are listed below

Technical issues of CWC

The CWC sequence is used for NCC which uses thyristors as valves. There are some technical difficulties for practical realization of a NCC that are to be mentioned here:

- Zero crossing or bank Selection
  The valves are composed of two anti-parallel thyristors acting like two half bridges, one for each half cycle of the load current (no circulating current configuration). It is not an easy task to find the right moment when to select the time to switch from one bridge to the other. It is especially difficult if the ripple in the current is strong or in case of a leading power factor. The usual dead time at the zero crossing leads to distortion of the load current. Method and handling of that problem can be found in [5].

- Unsuccessful commutations
  In reality, a natural commutation lasts a certain time or angle, often denoted as μ overlapping angle. An unsuccessful commutation is a commutation that starts in correct conditions but during which, or shortly after, the driving voltage ΔV changes its sign. The current derivatives in each active phase reverse as well. Consequently, the current of the outgoing thyristor will not cross zero and the commutation cannot finish properly. The supposed outgoing phase will then continue to conduct the load current until a proper action is taken to mitigate this phenomenon. Proper action to take when entering a short circuit state will not be discussed here but are described in [5] and especially [13]. The location of commutation for which this danger could appear starts with α_{pos} near the 180° limits, that is, when the converter acts as a inverter. For this risk to appear, the power factor has to reach

low values (lagging) near 0. Of course the precise determination of this depends on numerical values of μ. It is usual to find a practical limit to α_{pos} of 150°, which correspond to a limitation of power factor of 0.5 lagging. Similarly the limit imposed on α_{neg} to avoid unsuccessful commutation is 210°.

- Reverse recovery phenomenon of thyristors
  Thyristors do not turn-off as soon as the current reverses but need a recovery time from the instant of zero crossing to eliminate accumulated charges in their *pn* junction. The consequence is that they effectively turn off when the current is already negative. The precise determination of that value is complex and beyond the scope of this chapter but it is usually not negligible and the current can reach a non negligible opposite value when the device turns off. There is usually an inductive component involved in the leg where the device turns off and this leads to voltage surge. Snubber is required to limit the *dv/dt* and the peak value of the surge. Also, the thyristor after having turned off needs to be impressed a negative voltage for a given duration before a forward can be reapplied otherwise the thyristor might fire again itself. This is usually ensured in normal operating mode of a NCC but this is not the case of leading power factor operating mode. Particular care must be paid for leading power factor when using a NCC.

- Unsymmetrical input phase connection & multiple feeding of network phase
  With the CWC sequence, for a three phase load, there are instants when a given input phase is selected to feed two load phases simultaneously. The issue is an overload of the given input phase which could be a problem. Also, the input source is never connected in a symmetrical configuration. For a generator, this unbalanced mode might be a drawback and might inject current harmonics that lead to losses in the damping cage.

2.5 The *slowCWC* sequence

2.5.1 Principle of the *slowCWC* sequence

The *slowCWC* sequence is very similar to the CWC presented in the previous section. The *slowCWC* sequence, as introduced in [1] and [2], suggests to follow the output wanted component **only** with the slow switching rate of the CWC scheme, that is $F_{C,slow}$. Fig. 2.12 compares a waveform of CWC (left) and a waveform of the *slowCWC* sequence, in order to clearly and intuitively understand the similarities of both types. In Fig. 2.13, shows the time evolution of the input phase index. Here also, the unique switching frequency can be observed when compared to Fig. 2.11.

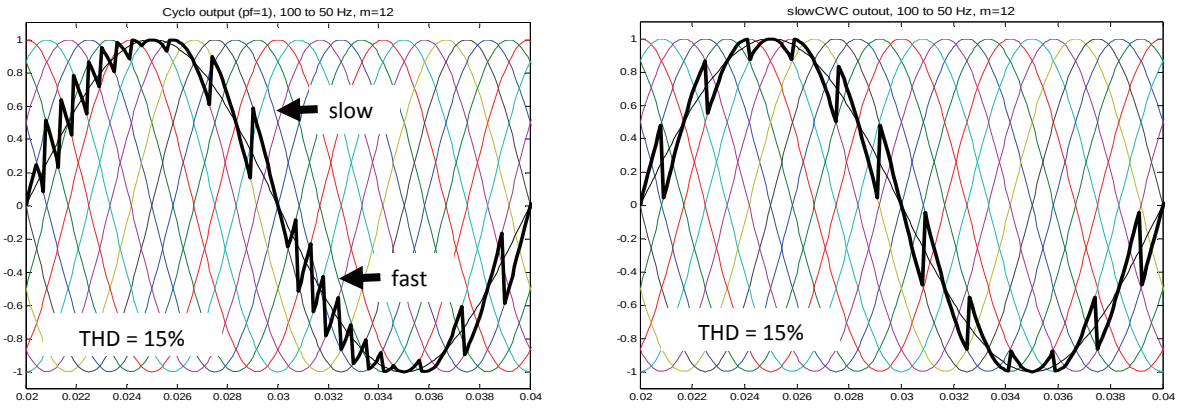


Fig. 2.12 - Ideal output voltage (bold) of cyclo-converter (left) and slow switching scheme (right)

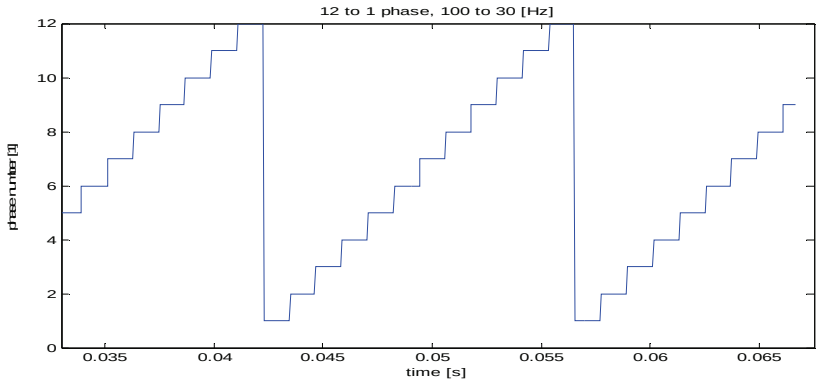


Fig. 2.13 – Input phase index evolution of the *slowCWC* sequence

Determination of commutation instant can be done similarly as CWC with the phase angle α or in the spatial vector plane. As can be observed in Fig. 2.14, only positive slopes of α_{pos} and α_{neg} are used for the *slowCWC*, which guarantees the slow commutation frequency. Consequently, the edge type (positive or negative) is not always compatible with the sign of the output current which implies that some commutations do not respect the power requirement to be natural and must be forced. This sequence is only feasible if the available valves are turn-off capable. Fig. 2.14 shows the zones of forced and natural commutations for a unity power factor. The forced commutation zones appear where the sign of the edge type (positive or negative) does not correspond to the load current sign. For other power factor, the width of the commutation and natural zone will vary in a complementary manner. This varies linearly with the power factor angle φ_{PF}. For a 90° lagging phase angle, there will be 100% of natural commutation. Similarly, for a 90° leading phase angle, there will be 100% forced commutations. In Fig. 2.14, the target output voltage is a sine waveform with a frequency F_{out}. The commutation driving voltage, ΔV, is the voltage between two generator phases that allows commuting the currents from the outgoing to the incoming phase. From the spatial vector representation of Fig. 2.10 it can be shown that ΔV at commutation instant t_c can be represented by a sine waveform of same pulsation as the target curve, but with a phase shift of $+\pi/2$. The magnitude of ΔV depends on the input phase number. The trigonometric relation that links ΔV and input phase magnitude will be presented in chapter 3. In Fig. 2.14, the commutation type zone of the corresponding two other output phase S and T of the converter are also represented. This shows that, for this unity power factor, there are moments during which there are two forced commutations and one natural commutation, and some other moments where there are two natural commutations and one forced. For this to be valid, natural commutations must be enabled by the control of the gating signals, i.e. delay between step 2 and step 3 must be set long enough to let the natural commutation proceed.

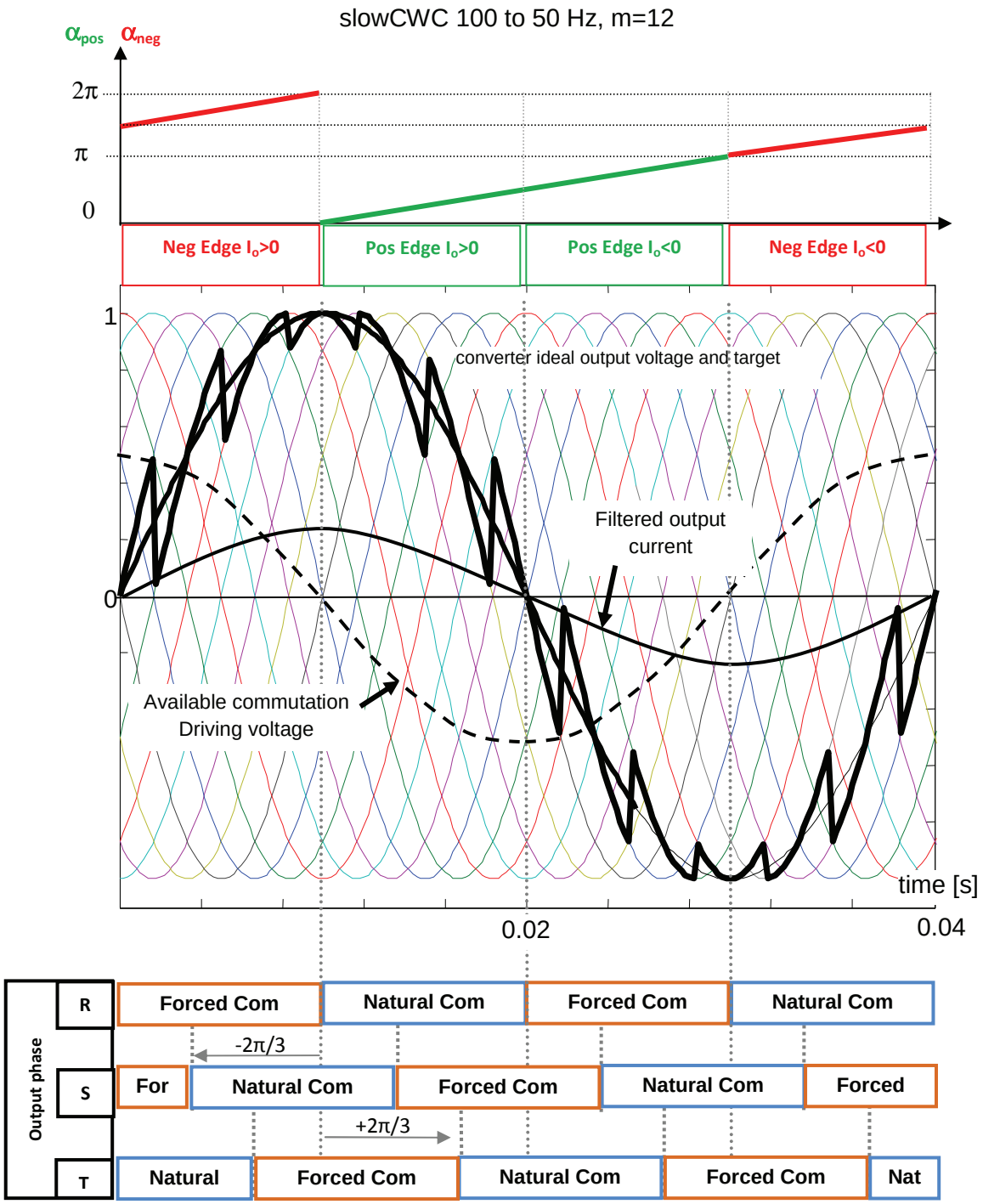


Fig. 2.14 - Driving voltage in function of commutation instant along the target output voltage

2.5.2 Pros and cons of the *slowCWC* sequence

Advantages of *slowCWC* over *CWC*

- Lower commutation rate with equivalent output THD
  For the slow switching scheme, the mean switching frequency is obviously $F_{C,mean} = F_{C,slow}$. The gain in commutation number per output period between CWC and *slowCWC* can be relevant. For example at unity power factor with a frequency ratio $F_o/F_{in} = 0.5$, *slowCWC* uses 50% less commutation than CWC for a similar output THD.

- Zero input displacement factor of the converter
  As will be shown in the next section about waveform spectrum properties, the converter is transparent in term of reactive power. It means that the input displacement factor of the converter is identical to the load power factor. The converter with *slowCWC* does not introduce an additional lag between the voltage and current fundamental of the input phases, as opposed to the NCC which can introduce up to an additional lagging angle of 30°.

- Technical benefits
  Technical benefits will be detailed when introducing the PPMC in chapter 3 but the main advantages compared to the NCC is that there is no bank selection or zero crossing management (or much easier) and there are no danger of unsuccessful commutation because the BDS are and must be fully controllable (on and off).

Drawbacks of *slowCWC*

- Forced commutation
  As will be detailed in chapter 3 and 4, the forced commutation introduces commutation losses in the switches and requires protection hardware to limit voltage surge due to inductive components in the commutation loop.

- No modulation depth
  Due to the nature of *slowCWC* sequence there is no choice in the magnitude of the output voltage whereas with CWC this one can be varied by varying the magnitude of the target curve in the waveform crossing algorithm. However in our application, the voltage magnitude will be controlled via the excitation of the generator. This will imposes dynamic limitation when it comes to current control and difficulties in designing the current controller.

- Technical issues
  Availability and price of turn-off capable switches (IGBT's, IGCT's) for equivalent voltage/current rating with thyristors. Chapter 4 will analyze the consequences of additional losses due to the use of snubber circuits.

2.5.3 Note about *slowCWC* limited to natural commutations

The *slowCWC* sequence, as written in chapter 1, has been suggested several times in the literature. However, the *slowCWC* has always been suggested along with a matrix converter using thyristors (NCMC) restricted to natural commutations (no additional circuitry to force off thyristors). As shown above, the *slowCWC* sequence cannot be executed entirely with natural commutations except for specific output power factor (lagging 0). If it is still required to work with natural commutations, then some commutations must be delayed, leading to a distorted output waveform. Reference [13] gives an exhaustive study of such a converter and especially the procedure to avoid unsuccessful

commutation. Although, as seen in section 2.4, the occurrence of unsuccessful commutation for the *slowCWC* sequence can be well located by analyzing the waveform of Fig. 2.14, reference [13] suggests to locate them in real-time to take into account transients operating points of the converter that Fig. 2.14 does not consider. However, considering only steady state operation the following can be observed. When entering a forced commutation zone, the load current will cross zero and the conducting thyristor blocks. It is then still possible to fire the same thyristor of the same input phase but opposite bridge (does not work for all power factors). Then a commutation to the next phase has to be delayed until the conditions for natural commutation are again met, when the conducting phase and the next adjacent crosses. From this time it is again possible to commute. This is what is shown in Fig. 2.15, where the effective output waveform differs from the target curves at each beginning of forced commutation zones. This situation is better with a decreasing lagging power factor and gets worse for a decreasing leading power factor.

As can be observed in Fig. 2.15, this waveform, although distorted compared to the target curve to follow, approaches a square wave shape, which corresponds in a third harmonics in the spectrum. If the load is three phase system, the application of this distorted output will still give rise to nice current waveform because the third harmonics will cancel due to the zero sequence component. If converter imposes the line voltage to the load, then the phase voltage will not have the third harmonics, and hence the load current either. The homo-polar component however implies that there will be non negligible voltage excursion of either the load neutral point or the input source neutral point. If there is the possibility for this neutral point to be floating with non negligible voltage then this method could be used. This method, besides imposing insulation of the neutral point, also imposes restriction to given frequency ratios. The frequency ratio cannot be chosen freely but must match given discrete values. This complicates the control of the power generation set. Both of these drawbacks make this solution non eligible for this thesis but should be studied in other work because the economic profile of this solution might be really interesting.

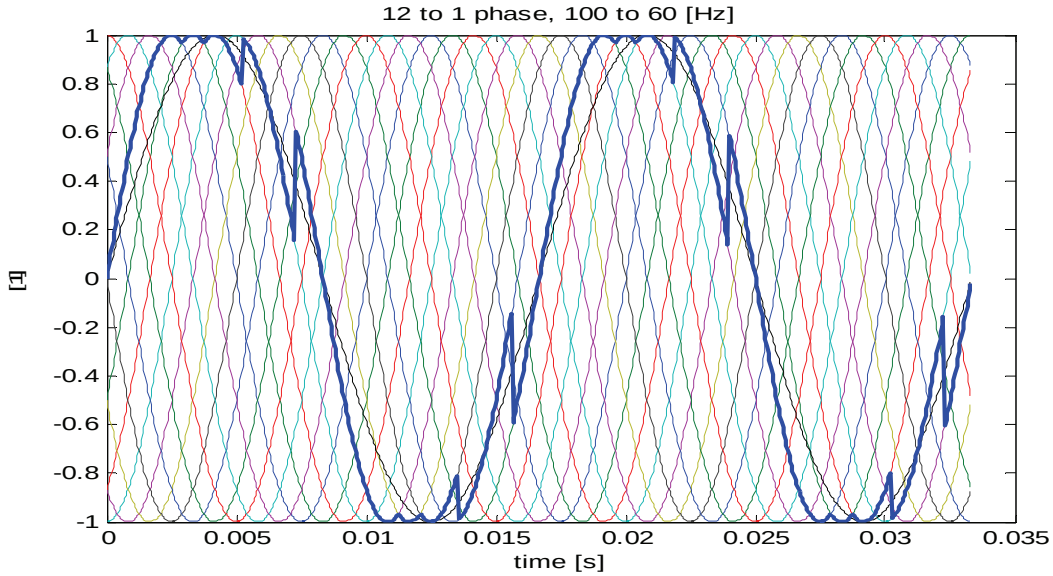


Fig. 2.15 – Output waveform of *slowCWC* sequence limited to natural commutation

2.6 Input and output waveforms properties

As written previously in this chapter, the spectral contents of the converter output voltage and input current is a key criterion in comparing commutation sequence among them. Besides, knowledge of the spectrum helps understanding and analyzing the systems and the design of the optional filtering passive components. There are two methods to obtain the spectrum of a waveform, either analytically or numerically. As this work focuses on the *slowCWC* sequence, special effort has been put into the development of an analytical expression of the spectrum of its output voltage. This will be presented in the second paragraph of this section, paragraph 2.6.2. Then, the following paragraphs will expose numerically computed frequency spectrums of *CWC* and *slowCWC* for output voltage and input current. Especially, the THD values and the displacement factor will be pointed out and compared between both sequences. The frequency spectrums are obtained numerically with a Matlab® script that generates ideal three phase output voltage waveforms and *m* phase input current waveforms. Then a FFT algorithm is applied to those ideal waveforms. Before going into details, paragraph 2.6.1 gives a few definitions of waveforms properties.

2.6.1 Definitions of spectrum properties and assumptions

Load current and input voltage

For all the developments or computations of section 2.6, the load current and the input voltages are assumed to be purely sinusoidal.

Repetition frequency (F_{rep})

The repetition frequency is the frequency with which the converter output voltage repeats itself. As seen, the output voltage of frequency F_o is built from segments of input of frequency F_g where F_g is not necessarily an integer multiple of F_o . So the repetition frequency is not necessarily the output frequency F_o, also denoted wanted frequency. The repetition frequency F_{rep} is easy to determine when the frequency F_g and F_o are integer values. In this case it is given by the GCD between F_g and F_o. For example: F_{rep} of a 100Hz to 30Hz conversion is GCD(100,30)=10Hz. When the frequencies F_g and F_o are rational numbers, it is still possible to find F_{rep}, which might be much smaller than F_o. If F_g and/or F_o are not rational, then F_{rep} is not defined. In practice, influence and detection of F_{rep} will be strongly affected by other phenomena and distortion of the output voltage. With the numerical method used here, which also generates the waveforms analyzed with FFT, the mean value over each output period has been computed as a check. In general for *m* greater than 6, this mean value is below 0.1%.

FFT method

The FFT is applied to a sample of 1s duration of the waveforms. As only integer frequency ratio will be used, this ensures an integer number of repetition periods T_{rep} and this reduce the leakage phenomenon of due to DTFT. This sets the FFT resolution to 1Hz, which is sufficient for the needed accuracy of this application. There are no windowing method applied to the waveforms sample as a preprocessing before the FFT.

Harmonics and THD

Rigorous definition of the harmonics implies that the harmonic frequencies are integer multiple of the fundamentals or wanted component. However, as will be seen later, the frequency spectrum of

CWC and *slowCWC* waveforms show harmonic frequencies that are not necessarily integer multiple of the fundamental (wanted) components. Throughout this work, the definition of the harmonics is widened so that the term refers to any other frequencies than the output or wanted frequency. The definition of the THD is the square root of the ratio of the power of all harmonics to the power of the fundamental, as given by .Equ. 2.5.

Equ. 2.5

$$\boldsymbol{THD = 100 \times \sqrt{\frac{\sum \|X_{harmonics}\|^2}{\|X_{wanted}\|^2}}}$$

where $||X||$ is a the real part of complex components of the spectrum of a signal *x(t)* which can be either a current or a voltage. Of course, when using numerical method and FFT, there are non null values for all frequency bins of the FFT results since there are leakage phenomena appearing due to DTFT. However, it is assumed here that number of T_{out} period taken for the FFT is high enough to keep the leakage phenomena low.

Displacement factor or angle

This is the angle between the fundamentals of a voltage and a current. This is equivalent to the power factor when considering only the fundamentals of voltage and current.

Distortion factor

The distortion factor is the ratio of the total rms value of a signal to the rms of its fundamental of wanted component.

Power factor

The power factor is the ratio of the active power referred to the apparent power. If the THD is null for the voltage and the current, displacement factor and power factor are equal.

2.6.2 Analytical frequency spectrum of *slowCWC* output voltage

With a traditional pure Fourier series development, one would like to analyze the waveform on one repetition period where the meaning of fundamental is that the analyzed function repeats itself exactly with this period. In the case of an output waveform of the sequence *slowCWC* the repetition period differs from the wanted component and depends on the frequency ratio. In some cases, this fundamental frequency can be much lower than the wanted component or even be null. This would render the classical Fourier development tricky. The same remark is valid for the CWC sequence. Therefore, as can be found in [5] the method presented here bypasses this difficulty by extracting the Fourier series from a stage deeper into the low level of the construction principle of the output waveform of the *slowCWC*. It uses the switching functions that are the building blocks of the output waveform of the *slowCWC* sequence. The output waveform is then the sum of the multiplication of each switching function by its associated sinusoidal input. This is illustrated in Fig. 2.16 (left and right) for a visible case with six input phases (*m*=6). Fig. 2.16 left shows the available input sinusoidal waveform and the output waveform built from those. The frequency spectrum of this waveform is wanted. Fig. 2.16 right shows the switching functions and their associated input sinus.

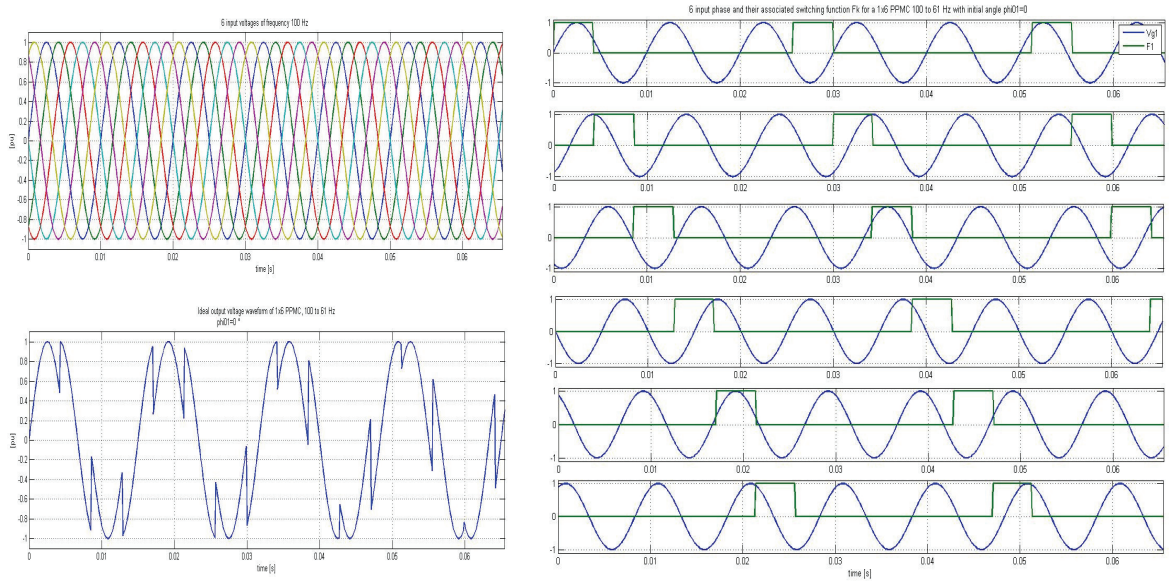


Fig. 2.16 – Input phases (left top), output waveform (left bottom) and switching functions (right) of *slowCWC*

Fig. 2.17 shows the first input sinus, its associated switching function and the multiplication of both along with some important parameters used later.

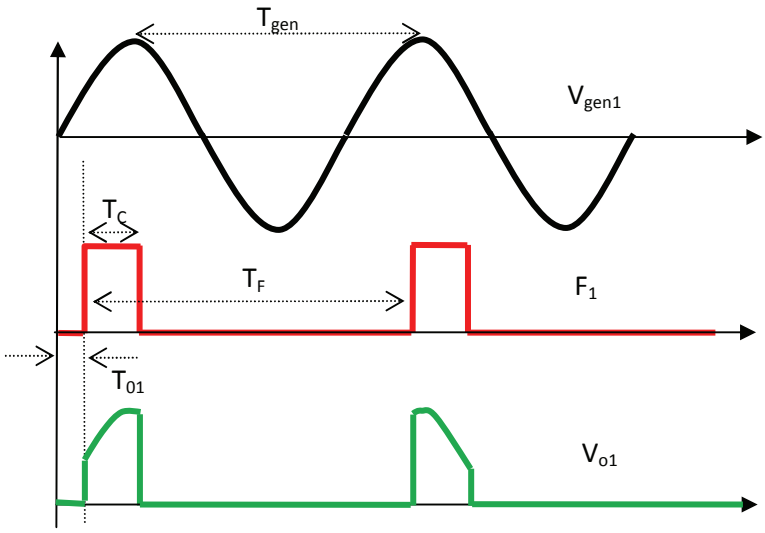


Fig. 2.17 – Details of switching function related parameters

The method to derive the spectrum of the output waveform first derives the spectrum of the switching functions and then derive the Fourier series of the output voltage of the PPMC by a frequency shifting of the switching function's spectrum because the output waveform is the sum of multiplication of a sine waveform by its corresponding switching function. Derivation of the spectrum of the switching function is easy because those are only square wave with a given width and a given period T_c. Of course, with this method, the spectrum of the real output waveform on one output period is not obtained. Especially the low frequency and the mean value will not appear. But precise

determination of those is difficult because it will be different for each output period. In practice, the avoidance of those low frequency components is performed through dedicated current control.

The details of the spectrum derivation using the switching function method are not presented here. Only the result and the general shape of the spectrum are shown.

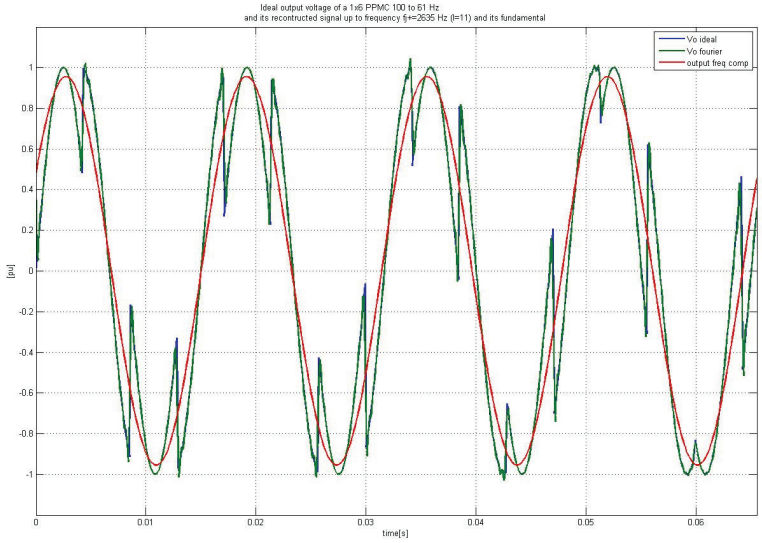


Fig. 2.18 – Reconstruction of *slowCWC* output waveform from theoretical spectrum

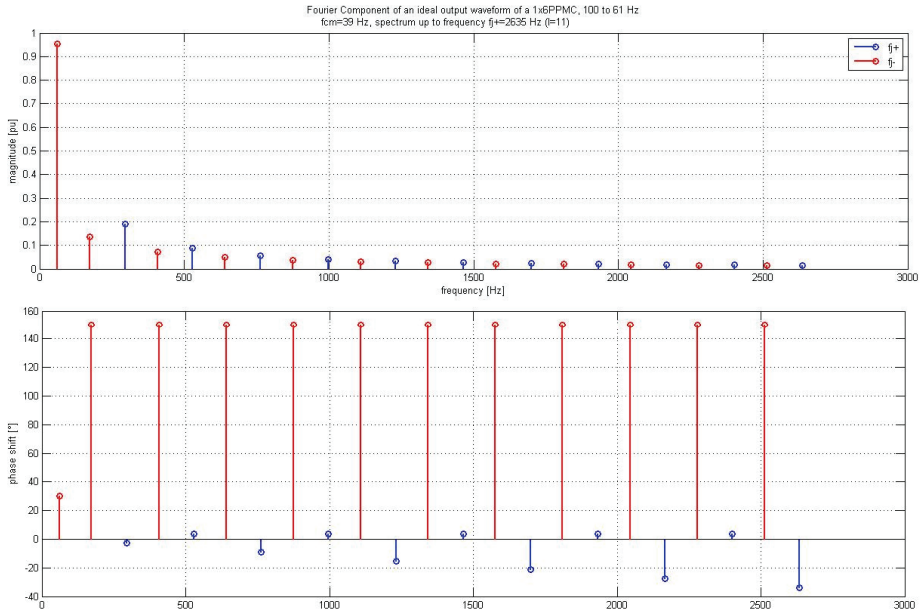


Fig. 2.19 – Theoretical frequency spectrum of *slowCWC* output waveform

Fig. 2.19 shows the ideal waveform of the sequence *slowCWC* superimposed with the reconstructed signal from the theoretical spectrum derived analytically with the method of the switching function. This spectrum (magnitude and phase) is shown in Fig. 2.19. The blue data are the positive component and the red one are the negative (except the first peak which is the wanted component). Fig. 2.20 explains the theoretical construction of this frequency spectrum.

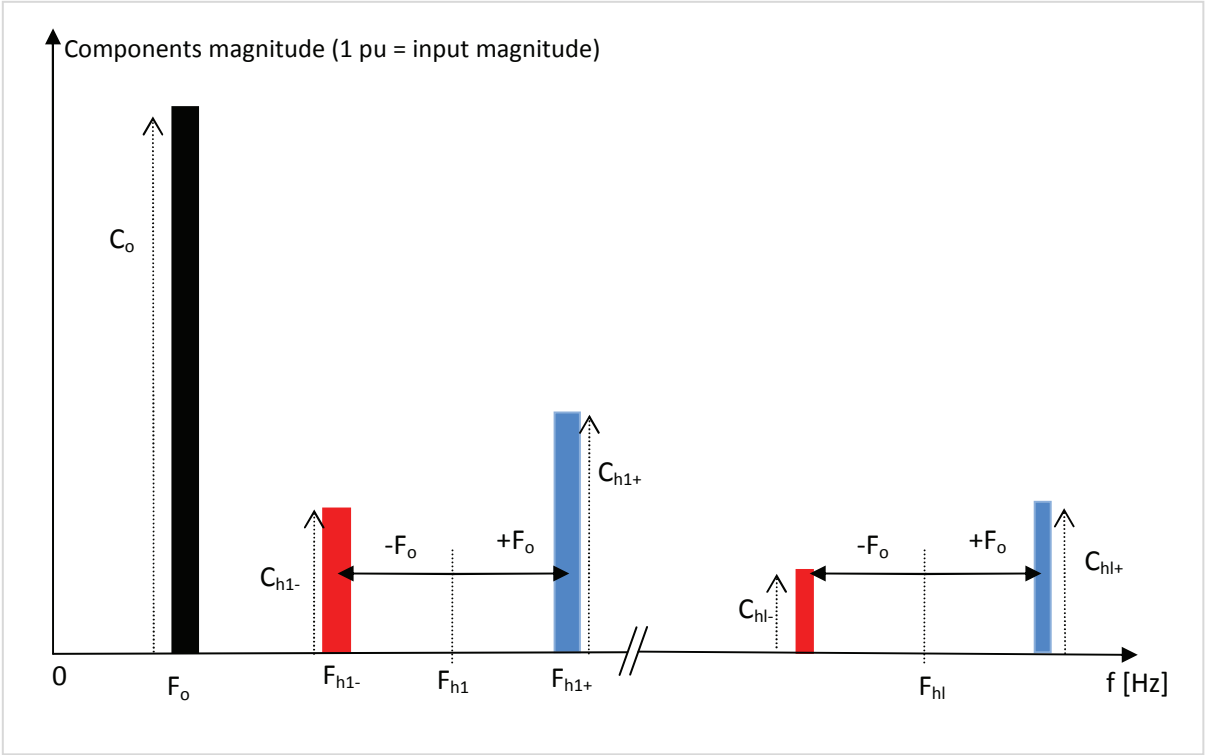


Fig. 2.20 – Construction of theoretical frequency spectrum of *slowCWC* output waveform

F_o is the wanted component or the output frequency. F_{hl+} and F_{hl-} are the harmonics frequencies. The term harmonics must see its definition widen because those frequencies are not necessarily integer multiple of F_o. F_{hl+} and F_{hl-} are centered on F_{hl} with a $+F_o$ and $-F_o$ shift respectively. The value of F_{h1} depends on the frequency difference F_g-F_o and on the input phase number m. F_{hl} are integer multiple of F_{h1}.

Equ. 2.6

$$\boldsymbol{F_h = m(F_g - F_o) \;\; and \;\; F_{hl} = lF_{h1} \;\; and \;\; F_{hl\pm} = F_{hl} \pm F_o}$$

The magnitude associated to each of the harmonic depends on m and are given by Equ. 2.7. This is expressed in p.u. where 1 p.u. is the magnitude of the input source.

Equ. 2.7

$$\boldsymbol{C_{h+} = \frac{m}{(lm-1)\pi}\sin\left(\frac{\pi}{m}\right) \;\; and \;\; C_{h-} = \frac{m}{(lm+1)\pi}\sin\left(\frac{\pi}{m}\right)}$$

The phase of each harmonic component can also be expressed analytically but is of a small interest here and will not be presented. Value of the output component, or wanted component is given by Equ. 2.8. Numerical values are given in Table 2.3.

Equ. 2.8

$$\boxed{\boldsymbol{C_o = \frac{m}{\pi}\sin\left(\frac{\pi}{m}\right)}}$$

Table 2.3 – Wanted or fundamental component magnitude of *slowCWC* output waveform

m	**3**	**6**	**9**	**12**	**15**	**18**	**21**	**24**	**27**	**30**
C_o 1 p.u. = input magnitude	0.827	0.955	0.980	0.989	0.993	0.995	0.996	0.997	0.998	0.998

The phase of the wanted component, not expressed here, shows that it is in phase with the target voltage used in the determination of commutation instant, as described in the previous section.

Table 2.4 shows numerical values of harmonics magnitude m=27. The wanted component or output frequency, is always given by the first negative side component (Cj- l=0).

Table 2.4 – Magnitude of positive (top) and negative (bottom) side harmonics of *slowCWC* output spectrum

C_{j+} (1 p.u. = input magnitude)																				
m/l	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
	+	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**
27	3.84	1.88	1.25	.932	.745	.620	.531	.464	.412	.371	.337	.309	.285	.265	.247	.231	.218	.206	.195	.185

C_{j-} (1 p.u. = input magnitude)																				
m/l	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**
	+	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**	**+**	**-**
27	**99.8**	3.56	1.81	1.22	.915	.734	.612	.525	.460	.409	.368	.335	.307	.283	.263	.246	.230	.217	.205	.194

Table 2.5 gives the relative frequency values of the harmonics for *m*=27, where the reference is the output or wanted component F_o. Table 2.5 gives results for two distinct frequency ratio F_g/F_o : 1.2 and 2, which correspond to 60Hz to 50Hz resp. 100Hz to 50Hz conversion. As one can see, the harmonics are not necessarily integer multiple of the wanted frequency neither of the input frequency but integer multiple of the difference. However, for grid code compatibility, the requirement are often expressed as a tolerance for harmonics where this term here refers to integer multiple of the grid frequency (wanted component). Grid code compatibility might be complicated by this behavior.

Table 2.5 – Frequency of the positive (top) and negative (bottom) side harmonics of the *slowCWC* spectrum

F_{j+}/F_o																					
	l	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
m	F_g/F_o																				
	1.2	6.4	11.8	17.2	22.6	28	33	39	44	50	55	60	66	71	77	82	87	93	98	104	109
27	**2**	28	55	82	109	136	163	190	217	244	271	298	325	352	379	406	433	460	487	514	541

F_j/F_o																					
	l	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
m	F_g/F_o																				
	1.2	4.4	9.8	15.2	20.6	26	31	37	42	48	53	58	64	69	75	80	85	91	96	102	107
27	**2**	26	53	80	107	134	161	188	215	242	269	296	323	350	377	404	431	458	485	512	539

By looking at the spectrum of Fig. 2.20 – Construction of theoretical frequency spectrum of *slowCWC* output waveform one can see that depending on the parameter *m* and *l*, there could be natural sub-harmonics, i.e. frequency F_h below the wanted component. The condition for this not to happen is given by Equ. 2.9.

Equ. 2.9

$$\frac{F_g}{F_o} > \frac{2}{m} + 1$$

Table 2.6 – Minimum frequency ratio to avoid theoretical sub-harmonics

m	**3**	**6**	**9**	**12**	**15**	**18**	**21**	**24**	**27**	**30**
F_g/F_o min	1.67	1.33	1.22	1.17	1.13	1.11	1.10	1.08	1.07	1.07

Usually the frequency ratio will not go below 1.2 (60 to 50 Hz), and the input phase number will be greater than 9 for THD compatibility, therefore in most cases there won't be any natural sub-harmonics.

Table 2.7 – Theoretical THD of *slowCWC* output waveform

m	**3**	**6**	**9**	**12**	**15**	**18**	**21**	**24**	**27**	**30**
THD	67.2	30.6	20.1	15.0	12.0	10.0	8.5	7.5	6.6	6.0

From the theoretical frequency spectrum of the output waveform of *slowCWC*, one can deduce the THD. Numerical values are given Table 2.7 for several values of *m*. We can see the great enhancement in THD when going from *m*=3 to *m*=9. This enhancement is still interesting from *m*=9 to *m*=21 but then benefit of increasing the input phase number must be balanced with other criteria as the cost, number of elements etc. This optimization procedure is beyond the scope of this work since it requires specific machine design skills.

2.6.3 Numerical Output waveform property for *CWC* and *slowCWC*

Table 2.8 – Computed THD of *CWC* and *slowCWC* output waveforms

Output Voltage *)Fundamental magnitude in per unit of the input voltage (Line to Neutral) **)Zero-crossing management makes those values different for CWC and slowCWC				
m	THD [%]		Fundamental*)	
	CWC	*Slow CWC*	*CWC*	*Slow CWC*
3	**65****	**68**	**0.84**	**0.83**
6	**29****	**31**	**0.97**	**0.95**
12	**14****	**15**	**1.0**	**0.99**
18	**10**	**10**	**1.0**	**0.99**
24	**8**	**8**	**1.0**	**1.0**
27	**7**	**7**	**1.0**	**1.0**

Table 2.8 gives THD values of converter output voltage for the *CWC* and *slowCWC* sequence. The THD is independent of the frequency ratio. One can see that the numerically computed values of Table 2.8 for the *slowCWC* sequence are very near the theoretical values expressed in the previous section paragraph. One can also see that THD between CWC and *slowCWC* are quasi similar, the differences can be explained by the choice of the zero crossing management of the CWC sequence and by the numerical error introduced by the limited repetition period used for FFT computation.

2.6.4 Numerical Input waveform properties for *CWC* and *slowCWC*

The input waveforms properties which are of interests are listed below. There are expressed in per unit in order to ease the comparison of both sequences *CWC* and *slowCWC*. They are also always computed for a star and delta (polygon) connected input source. All cases are based on a same three phase output power and same output power factor (for the fundamental). The following table, Table 2.9, summarizes those results, which are commented below it.

Table 2.9 – Summary of computed input properties of CWC and *slowCWC* sequences

Source type	I_{inRMS}/I_{oRMS}		I_{1inRMS}/I_{oRMS}		Displacement Factor (unity load pf)		Distortion factor		Power factor	
	CWC	Slow CWC	CWC	Slow CWC	CWC	Slow CWC	CWC	Slow CWC	CWC	Slow CWC
Polyg. (all *m*)	0.68	0.58	0.57	0.48	**0.86**	**1**	82%	83%	**0.71**	**0.83**
Star (*m*=27)	0.33	0.34	0.13	0.11	**0.86**	**1**	39%	33%	**0.33**	**0.33**

- **Input current rms value**, referred to the output rms current.
  It can be observed that the input current rms is always smaller for *slowCWC* than for *CWC.* For the polygon connected source, this value is obviously constant whatever input phase number. For *slowCWC* it is 58% and for *CWC* it is 68% of the output rms current. *CWC* requires a 1.17 times higher input rms current than *slowCWC*, for polygonal connected source. For star connected sources, the ratio is rather similar.

- **Input current fundamental rms value**, referred to the output rms current.
  It can be observed that the fundamental input rms current is always smaller for *slowCWC* than *CWC*. For the polygon connected source, this value is obviously constant whatever is the phase number. For *slowCWC* it is 48% and for CWC it is 57% of the output rms current. CWC requires a 1.18 times higher fundamental input current than the *slowCWC,* for polygonal connected source. For star connected source, this ratio is similar.
  As all cases have similar output active and reactive power, the observation about the input fundamental current implies that the input displacement factor is smaller for *slowCWC* than for *CWC*.

- **Input displacement factor**
  The numerical values of the input displacement factor confirm the prediction made from the input current fundamental values. The input displacement factor is independent of the source connection. For *CWC*, the input displacement factor is 0.86 and for *slowCWC* it is 1. This shows one of the main interests of the *slowCWC* sequence, i.e. its transparency in term of reactive power. For the same output apparent power, the generator has to be designed for a larger apparent power if *CWC* is used. The over-sizing is 116%. The consequences of such an over-design of the generator in terms of cost and losses are not discussed here since it is quite complex and need to be handled by machines specialist.

- **Input current distortion factor**
  The distortion factor for the *CWC* and the *slowCWC* sequence are quite similar. For a polygonal source, this means that the fundamental rms value is 83% of the total rms value. Obviously, with a star connected source, this factor drops since the individual sources are less used in terms of utilization factor. Only 39% resp. 33% of the total rms current is in the fundamental. This is an argument to use the polygonal connected source.
- **Input power factor**
  As expected, the input power factor is lower for *CWC* than for *slowCWC* for the polygonal connection of the source. The input power factor cannot be unity by definition for a static converter since there must be harmonics in the input current due to the oscillation of the instantaneous output power. For a star connected source, the input power factor degrades a lot compared to the polygon, for both *CWC* and *slowCWC* sequence.

Chapter 3 - The Poly-Phased Matrix Converter (PPMC)

3.1 Introduction to the PPMC

The topology of the PPMC that will be studied from now on is depicted in Fig. 3.1. This topology must be considered with the input and output sources that are respectively a polygonal poly-phased generator (SM) and an three-phase AC grid into which the converter must inject power with a given power factor through a connection impedance.

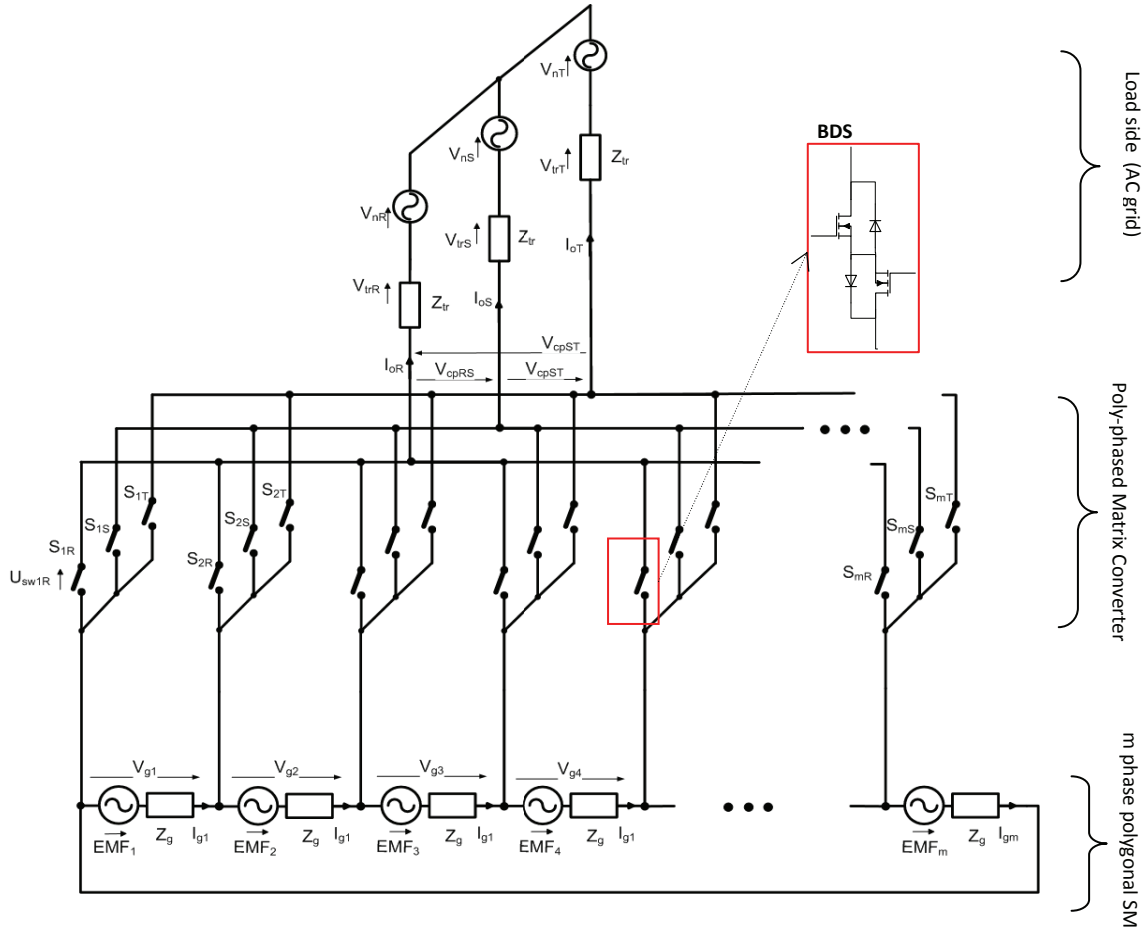


Fig. 3.1 - PPMC and the associated polygonal SM and three phase grid connection

3.1.1 PPMC

As described in chapters 1 and 2, the converter must interface the generator of electrical frequency F_g with the grid of frequency F_o, with $F_g > F_o$. It is a direct converter with a full matrix configuration of the valves. This topology, as explained in Chapter 1 and 2, is derived from the NCMC [4]. It uses bidirectional switches (BDS) instead of thyristors in order to comply with the *slowCWC* commutation sequence, presented in Chapter 2. In the BDS, similarly to conventional matrix converters [20], the diode in anti-parallel to the transistor protects it when a reverse voltage is applied, by limiting it to V_{Fdiode}. Besides, the diode provides the automatic turn-off behavior required for natural commutations. This configuration of the BDS allows controlling independently both current directions. Details of the four steps commutations will be given in paragraph 3.4.2.

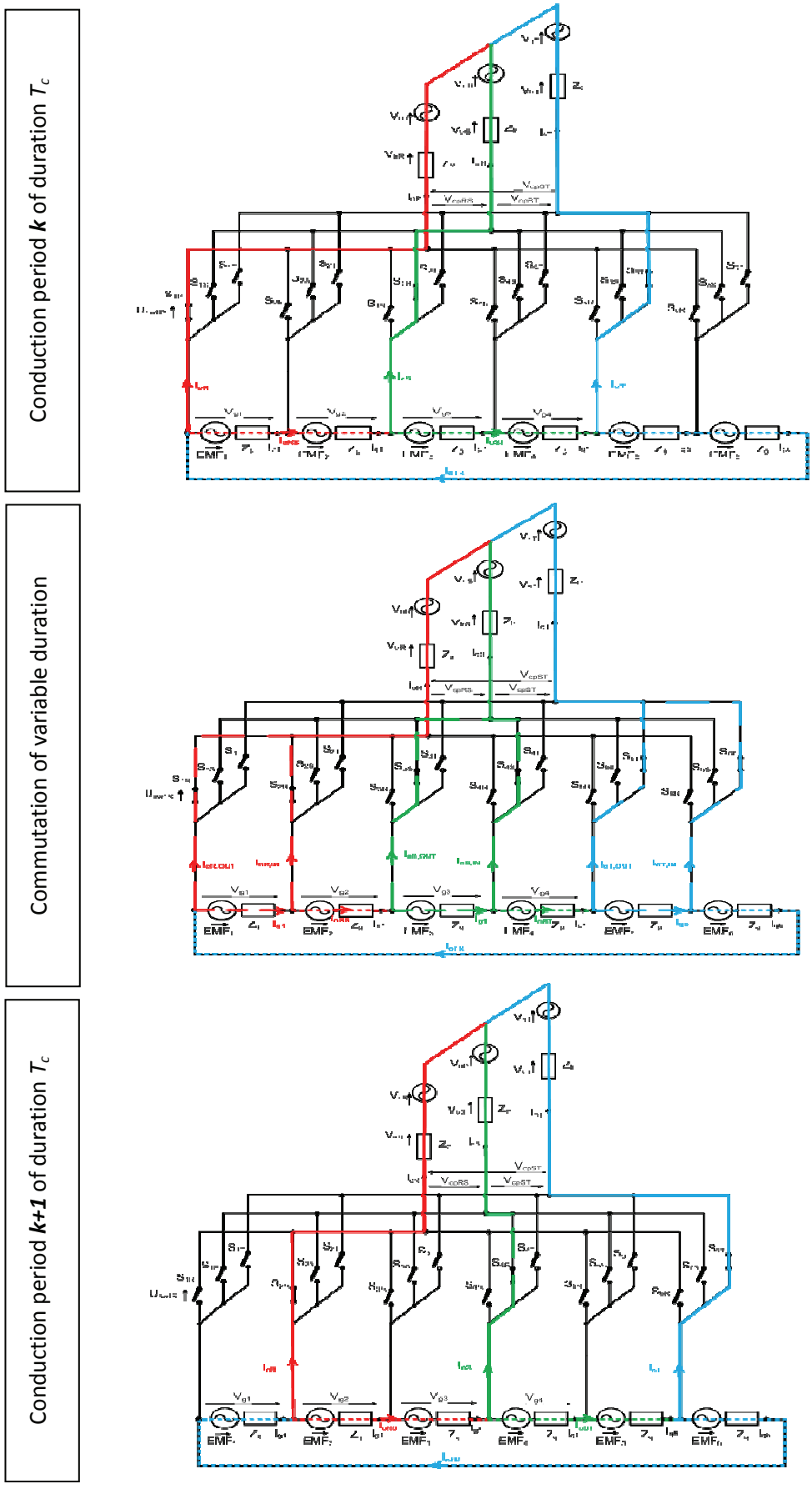


Fig. 3.2 – currents paths during three concomitant commutations of the PPMC

The precise nature of the switch, IGBT, IGCT or MOSFET, is not determined at this stage and is of a small interest at this stage of the study. The technology used will highly depend on the nominal values of the application. The high voltage will force the choice of IGBT or IGCT, even more because the switching frequency is not high.

The converter is run with the *slowCWC* commutation sequence. The commutations occur at a given fixed frequency $F_c=m(F_g-F_o)$. During a conduction period $T_c=1/F_c$, three BDS are closed and connect three input phases *[a,b,c]* with the three phase load. During the commutation, the respective three output currents are commutated from one input phase set *[a,b,c]* to the next adjacent one *[a+1,b+1,c+1],* with a modulo *m* cyclic behavior. At the end of the commutation, the new input phase set conducts the load currents for the new conduction period T_c, and so on. This is illustrated in Fig. 3.2. Advantages of the *slowCWC* sequence on others have been pointed out in chapter 2. Mainly, the converter has an input displacement factor equals to the load power factor.

3.1.2 Load

The load, a three-phase AC grid with frequency F_o, is modeled here as a three phase symmetrical stiff voltage system. In order to inject power into this grid, it is necessary to insert an impedance between the output of the converter and the grid. By applying a voltage drop across this impedance, it is then possible to inject power. The transformer, often required in order to adapt the voltage level between generator and grid, is also modeled as simple impedance (the short circuit model). Usually it is included in the connection impedance.

3.1.3 Generator

The generator is a poly-phased machine. Its stator is constituted of *m* windings that are all connected in series to form a polygonal *m* phase symmetrical voltage system. The rotor has one winding fed by a DC excitation current to create the necessary magnetic field to induce voltages in the stators windings. This is similar to a synchronous machine. Throughout this work, the generator's stator windings will be modeled with an ideal AC electromotive force (EMF) in series with a winding resistance R_g and a winding leakage inductance L_g, which is here the direct sub-transient inductance of the generator. In practice, the machine is more complex than this simple representation. Especially, the stator currents have an influence on the EMF. A finer modeling of the machine is beyond the scope of this work. For more details, the reader can refer to [43]. Fig. 3.3 is a spatial vector representation of the polygonal ideal EMF with *m=27*. The load is connected to a set of three generator phase [a,b,c] through the converter BDS. Hence, the converter imposes the line voltages on the load. The line voltages applied to the load is also symmetrical, as described by the spatial vector of Fig. 3.3 in green. The spatial vectors in blue represent the corresponding load phase voltage. With Fig. 3.3, it is easy to find the relations between a connection set [a,b,c] and the produced output voltage and the position of EMF_a. Also, as explained in chapter 2, in order to follow a target output sinusoidal waveform, a commutation is requested each time that the angular error between the target voltage and the converter output voltage is bigger than π/m. Fig. 3.3 shows precisely a commutation instant. This shows the position of the driving voltage ΔV at this instant with respect to the target voltage. ΔV is always in advance of $\pi/2$ rad on the target voltage. Straightforward trigonometry also gives the ratio between polygonal side (EMF) and the radius of the polygon V_{cp}.

Equ. 3.1

$$\left|\vec{V}_{c,R}\right| = \frac{\left|\overrightarrow{EMF}\right|}{2\sin\left(\frac{\pi}{m}\right)} \quad and \quad \left|\vec{V}_{c,RS}\right| = \sqrt{3}\left|\vec{V}_{c,R}\right|$$

Table 3.1 – Conversion ratio star to polygon in function of *m*

m	3	6	9	12	15	18	21	24	27	30
Star to Polygon	1.73	1.00	0.68	0.52	0.42	0.35	0.30	0.26	0.23	0.21
Line to Polygon	1.00	0.58	0.39	0.30	0.24	0.20	0.17	0.15	0.13	0.12

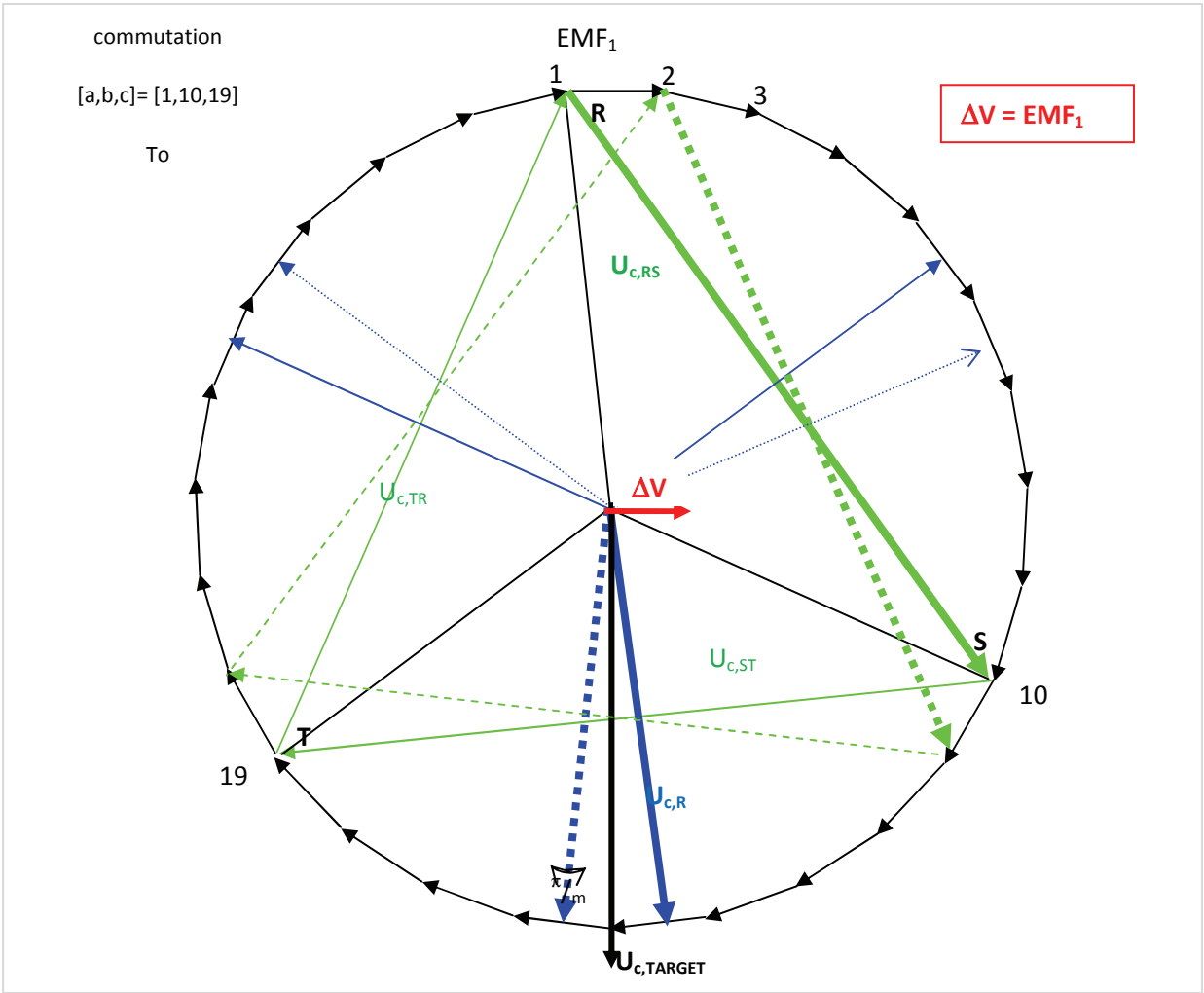


Fig. 3.3 – Ideal space vector of generator and converter output

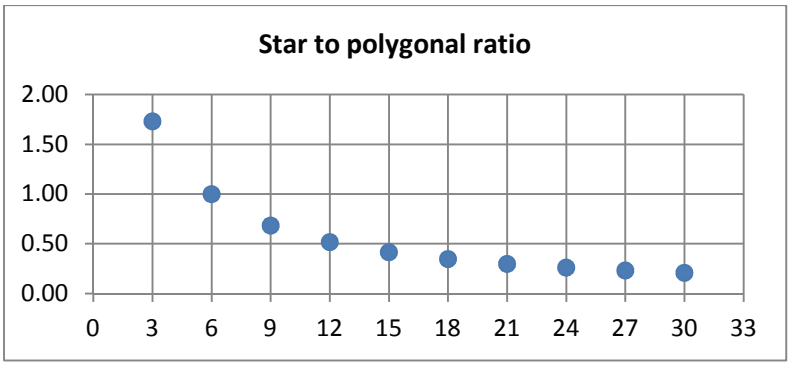


Fig. 3.4 - Motivation for polygonal connection vs star.

The polygonal connection allows to design input voltage sources with smaller nominal voltage than for star connection for the same output voltage V_c. This effect is particular relevant when going from 6 to 21 phase. Beyond the effect decrease its intensity according to Equ. 3.1. This is also visible in Fig. 3.4.. Provided that the excitation current is similar, the turn number of a stator winding is smaller for the polygonal connection than the star connection, which could be useful to gain space. The choice of polygonal connection also means a better utilization factor of each generator phase. Consequently, the total rms current per stator winding is higher by a factor of about 2 for the polygonal connection than the star connection according to the value found in chapter 2.

3.1.4 Switch voltage constraints

The blocking voltage constraint is the double of the polygons radius, as given by Equ. 3.2.

Equ. 3.2

$$\boldsymbol{maxSwitchVoltage = \frac{|\overrightarrow{EMF}|}{\sin\left(\frac{\pi}{m}\right)} = 2V_{cR}}$$

This can be easily deduced from Fig. 3.3. Nominally, V_c must meet the grid line voltage. For power regulation, V_c then is adjusted by roughly ±10% around its nominal value, through the magnitude of EMF. EMF is itself adjusted with the excitation current of the rotor winding.

3.1.5 Converter three phases equivalent model

Fig. 3.5 represents a simple model of the converter as a three phases controllable delta source with internal impedance Z_{gRST} and ideal voltage source $V_{c,ideal}$. Z_{gRST} is simply given by Equ. 3.3.

Equ. 3.3

$$\boldsymbol{Z_{gRST} = \frac{m}{3} Z_g}$$

This converter is connected to the three phase AC grid via a connection impedance Z_t, which contains the transformer impedance. If the load currents I_{oR}, I_{oS} and I_{oT} constitute a three phase symmetrical balanced current system, so are the delta currents of the converter, I_{gRS}, I_{gST} and I_{gTR}. The spatial

vector diagram of Fig. 3.5 gives the relation between I_o and I_g. The ratio of the magnitude I_o/I_g is $\sqrt{3}$ and I_g is in advance of 30° on I_o.

Equ. 3.4 $$\boldsymbol{I_{oR} = I_{gTR} - I_{gRS} \ and \ I_{oS} = I_{gRS} - I_{gST} \ and \ I_{oT} = I_{gST} - I_{gTR}}$$

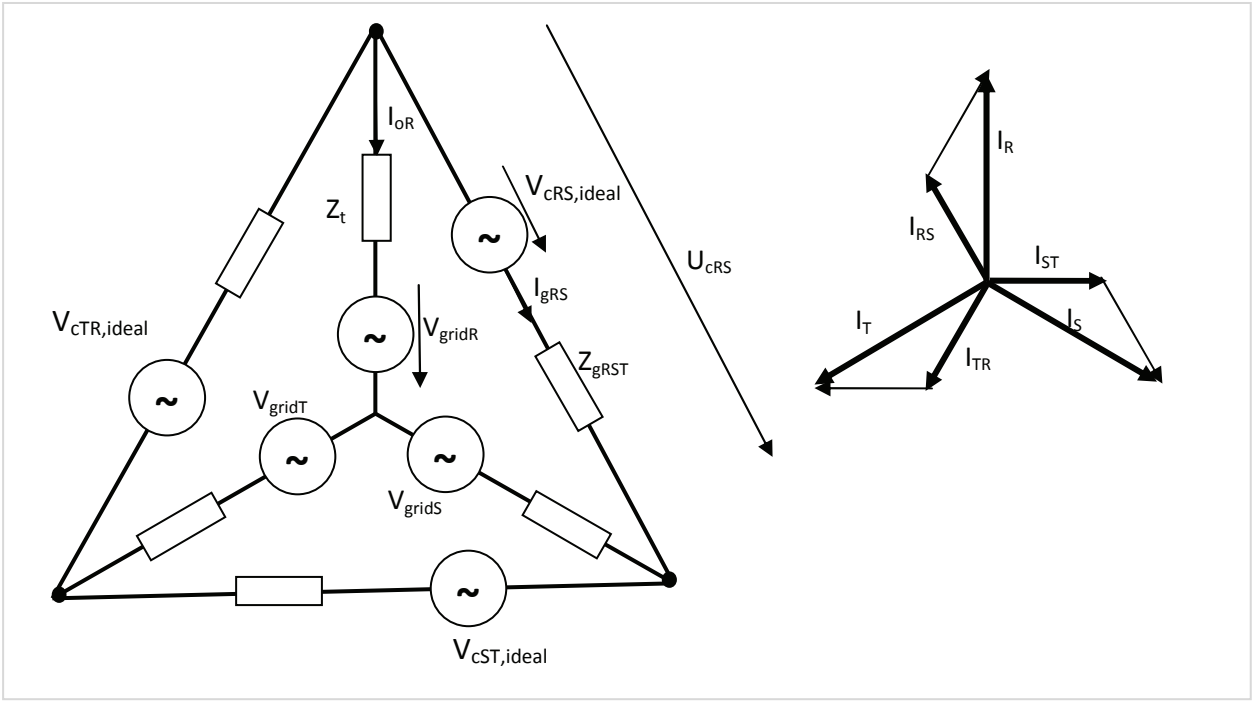


Fig. 3.5 – Three-phase equivalent model of the PPMC

3.1.6 Power injection method

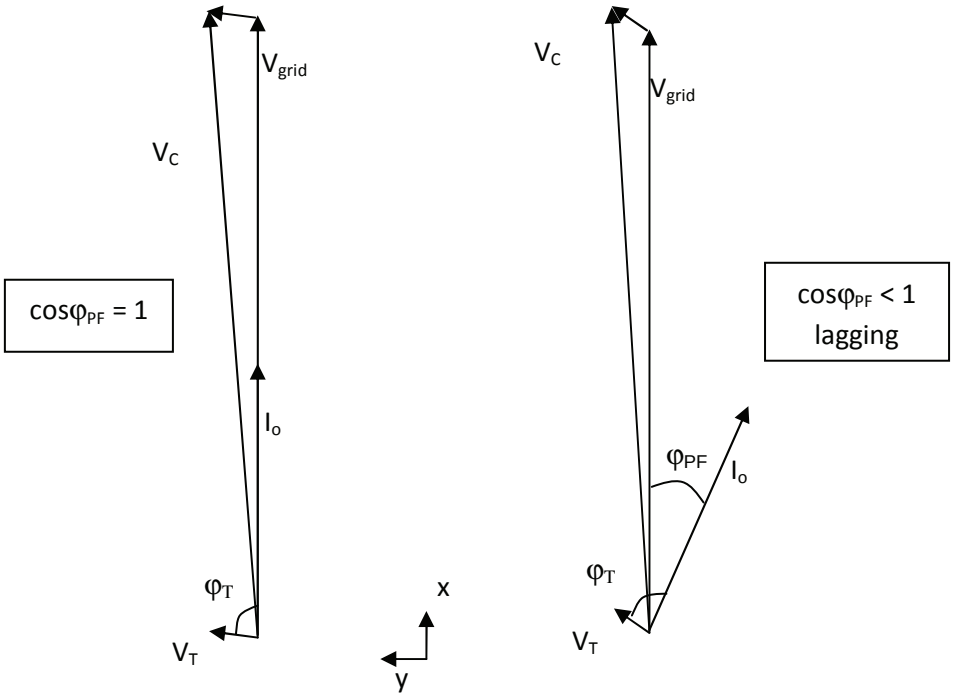


Fig. 3.6 – Power injection spatial vector diagram

V_T is the voltage drop across the transformer and connection impedance Z_T, with $Z_T = |Z_T| e^{i\varphi_T}$ V_c is build from V_{grid}, I_o, and V_T knowing φ_{PF} and φ_T. It is assumed here that $Z_{gRST} << Z_t$. Depending on the nature of the load (lagging or leading) magnitude of V_c must be greater or smaller than V_{grid} respectively. From Fig. 3.6 and with trigonometric relations, one can express the magnitude of V_c in function of the power factor. For a fixed apparent power, Equ. 3.5 gives the magnitude of V_c relative to V_{grid}.

Equ. 3.5
$$\left|u_{Cp}\right| = \sqrt{1+u_T^2+2u_T\cos\left(\varphi_T-\varphi_{PF}\right)}$$

where u_T is the relative magnitude of the voltage drop across the transformer and connection impedance with the nominal current. This value is usually situated around 0.1pu. Anyway, from Fig. 3.6 it is obvious that v_c will not exceed $1+v_T$. This occurs when V_T is in phase with V_{grid}.

3.2 The forced commutation issue

As described in chapter 2 there are two types of commutations: either a natural commutation or a forced commutation. The type depends of the position of the commutation along the output period. The input of the converter is an AC source with internal impedance. In the case of a natural commutation, this internal impedance allows the natural phenomenon. When the commutation has to be forced, this internal impedance causes trouble because of its inductive nature. The current derivative imposed by the switch at the turn-off is very steep compared to the generator's nominal regime and induces a non tolerable voltage surge across the generator's coil and also across the switches included in the commutation cell. This is not acceptable and in practice would lead to the destruction of the switches of the commutation cell or even the breakdown of winding insulation of the generator. There must be a free-wheeling path for this generator leg which should also limits the over voltage to a tolerable value for the generator and the switches. The capacitor is a simple and passive element that is selected as a first solution for the free-wheeling path. Among other means, there are Varistors or diode/capacitor arrangements, which should also be evaluated in another study. Here we will focus on the simple capacitive elements with a resistive component for damping the oscillations. This resistive-capacitive element will often be denoted by RC snubber in the following paragraphs. There are different places to insert the RC snubber within the converter in order to control the voltage excursion when the current is cut. Fig. 3.7 shows both possibilities. On the left, the RC snubber are connected directly across the switches. On the right, the RC snubber are connected directly across the stator windings

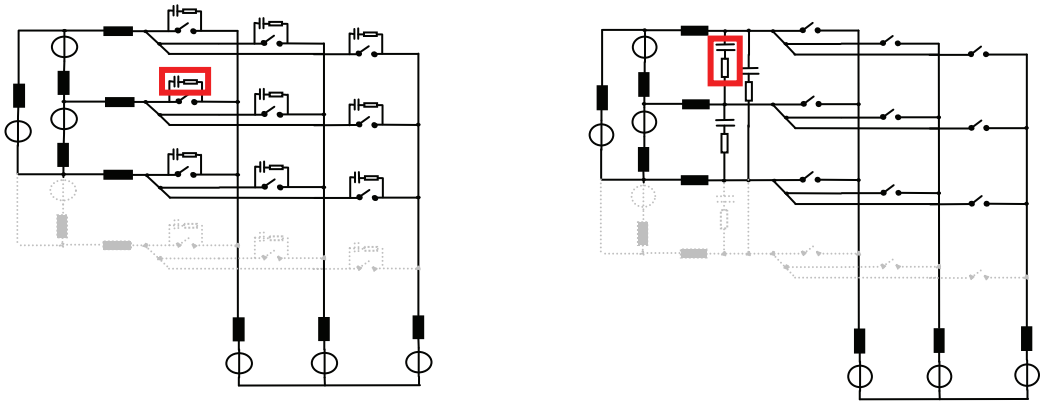


Fig. 3.7 - Generator with snubber across the switches (left) or the stator windings (right)

The configuration on the right will be retained for the following development. The advantage of connecting the snubber directly to the stator is obvious. There are three times less snubbers than the star configuration. However the capacitance is split into two capacitors if snubber are connected across the switches. Still, the stator connection leads to 2/3 of the installed capacitance for the switch connection. As illustrated Fig. 3.8, a capacitor is connected between each generator's windings.

Another drawback of the PPMC with *slowCWC* is that there are commutation losses in the silicon devices for the hard commutations. This will be developed in section 3.8.

In conventional matrix converter, depending on the commutation scheme, which is usually a PWM, there is also the possibility of forced commutations. In most of the cases, the input of a matrix is an AC grid and a LC filter is included in between in order to filter out the high current harmonics. Usually those filters are designed with criterion on a harmonic content limitation. In the AG application, it is the instantaneous value of the voltage across the coil that should not overpass a given value. For the PPMC, the filter approach is not adequate because it is based on steady state AC waveforms. For the PPMC, another approach based on damped second order response is required because it is wished that the transient response of the forced commutation is damped before the next commutation. Besides, the poly-phased nature of the source makes the usual three phase spatial vector approach of filter design more complex. References [28], [30] and [39] give examples of snubber design approach based on transient second order response. The first reference [28] however will not be used for the PPMC for the following reason. This reference gives some design rules to optimise the RC snubber, on the base of a reference circuit valid for many types of dc/dc converters and possibly indirect ac/ac converters. Reference [30] focuses on the minimization of the switching losses across the switch by damping the ringing phenomenon but does not consider the peak voltage, and assumes that the switch can withstand the peak voltage also without the snubber. This way of doing is not very appropriate for the PPMC because the main task of RC snubber will be first to reduce peak voltage to ensure the switch safety and then an assessment of the switching losses will occur. Assessment of losses in the resistor of the snubber will of course also be a part of the PPMC snubber design approach, developed in chapter 4.

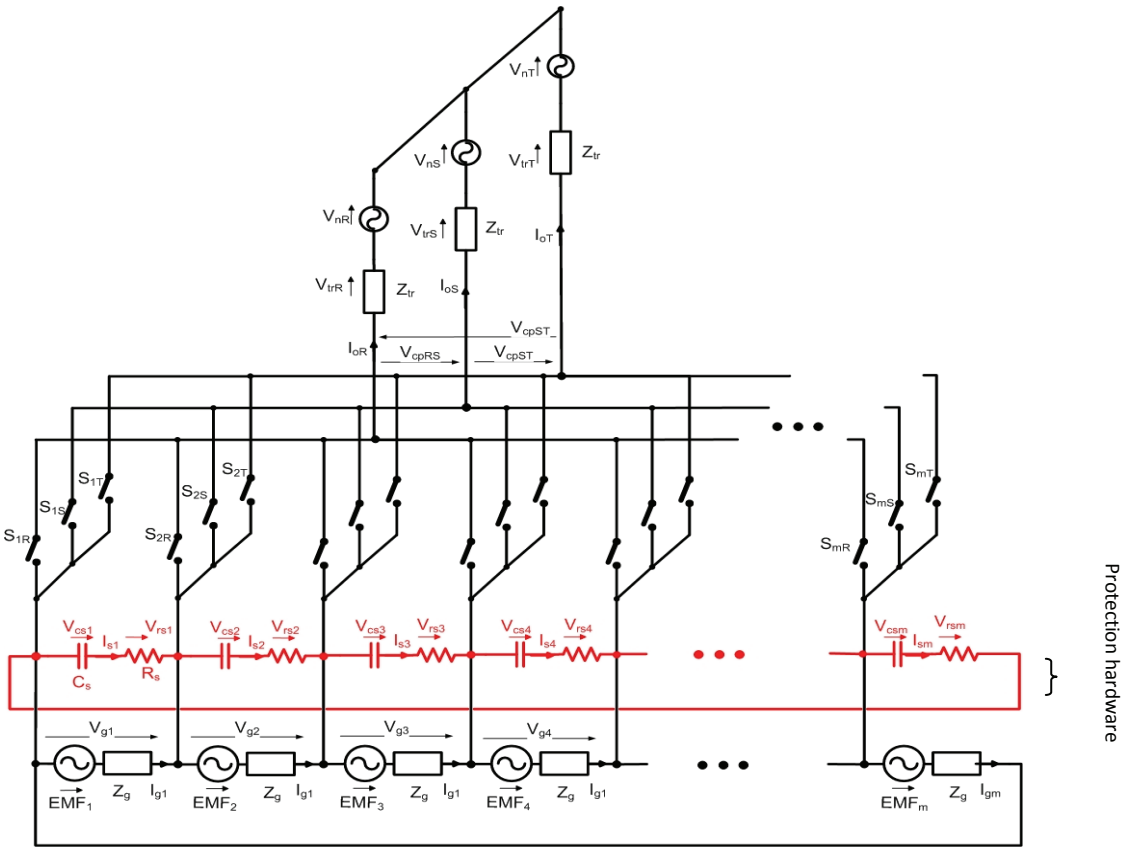


Fig. 3.8 – The PPMC and its associated passive protection circuits

Fig. 3.9 shows two simulation results to highlight the forced commutation issue. Those simulation results are taken from the case study, described in the next section. Fig. 3.9 left and right show two simulation results with two different snubber capacitor and resistor values, i.e. two different snubber designs. It shows the converter output voltage and output current as well as the voltage across one generator leg protected by a RC snubber. The voltage surge at each commutation where this generator phase is involved can clearly be observed in both cases left and right. The higher capacitor value in Fig. 3.9 right gives way to a smaller overvoltage, obviously. The precise design method of the snubber with given criteria is developed in chapter 4, which is entirely dedicated to the RC snubber. However in the present chapter, some parameters related to the snubber design will be introduced in the paragraph 3.3.2.

Also, in the present chapter, the modified commutation cell (with an RC snubber) will be studied because it is a key knowledge in the determination of commutation type which is used in the assessment of the losses of the snubber. Two properties of the commutations are also studied: the natural commutation duration and the false natural commutation phenomenon.

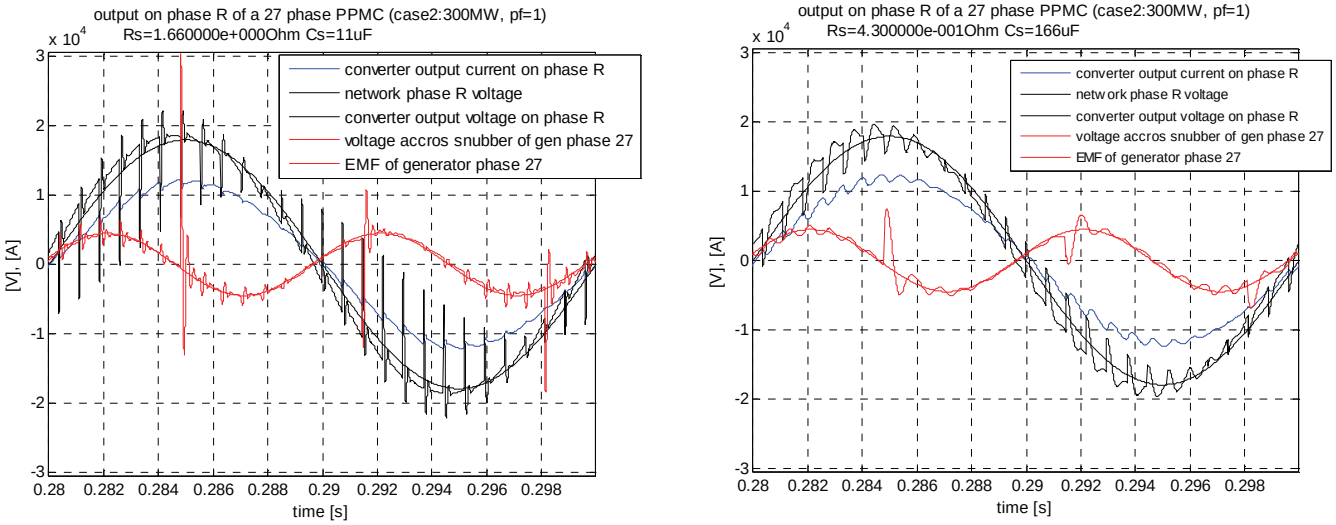


Fig. 3.9 – Simulation results of a PPMC to illustrate the forced commutation issue

3.3 Case study - introduction

Throughout this chapter, simulation results of a case study will be showed in order to illustrate and prove the statement developed analytically.

3.3.1 Note about simulation

Independently of the author's will, the simulation tool has changed two times during this work. The simulation tools used are: Simplorer® 7, Simplorer® 8 and Portunus®. Results shown throughout this work can come from one of those three simulators. We will not give any screen shot of simulation tool here and it must be said that the development of a simulation tool was not the aim of this thesis. More emphasize has been put in the realization of the experimental set-up, in chapter 6.

The model of the generator windings is an ideal AC voltage source in series with a inductor and a capacitor. The model of the transformer is simply its short circuit impedance. BDS have been built as in reality, with two anti series transistors, each of them in anti parallel with a diode. The static characteristic of the diode and the transistor is linear, with a given on resistance, an off resistance and optionally a forward voltage in on state. The control command block has been implemented in two sub blocks: a DSP-like block and a FPGA-like block each of them with given user defined sampling time, independent of the integration time step of the simulator. In this way it represents pretty well a real digital control platform. The DSP block has the control-command algorithm described in chapter 5, and the FPGA block contains the logic that produces the four gating signals necessary for the four steps commutation rule, as described in 3.4.2. The delay between step 2 and 3 can be varied on run time. The command is OPEN LOOP. This makes the setting of an operating point quite tricky, which explains that the waveforms shown in this work do not match the precise nominal operating point.

It can be said that the implementation of the 27x3PPMC is quite complex and lots of efforts have been put to make the simulation file as modular as possible. The number of variables is big which results in non negligible simulation length (order of magnitude : 30min for 0.2s).

There is a method that could reduce the simulation time drastically. This method takes advantage that, in fact, only three BDS are closed during conduction period T_c, and only six BDS are involved in the commutation process. The other BDS are simply in open state. Usually, the user is not interested in the current/voltage across those opened BDS. Thus, one conduction period T_c and the consecutive commutation transient regime could be simulated with a simplified circuit that only implements those six BDS. For the next conduction period T_c, this same circuit can be used but initial conditions of state variables (inductor currents and capacitor voltages) must be updated with the last values of the preceding simulation. This needs some code to execute this circular shifting of initial values and to rebuild the total simulation time from those portions of length T_c. An attempt to implement this method has been done in the Matlab® environment with the power electronic toolbox "PLECS". The reduction of the system dimension of this method led to a reduction factor of simulation time of five, which is not a negligible reduction factor. However, the implementation of this method in Matlab® environment suffers from one problem. It is necessary to compile the simulation file at the beginning of each simulation, so for each block of length T_c. The overhead time necessary for this compilation kills the effect of system size reduction. Due to lack of time and because simulation tool for the PPMC is not the main topic of this work, the development of this fast simulation method has been stopped here, however, the author is convinced that there is a simple mean to bypass the need of recompiling the simulation file at each beginning of T_c period. This is either realizable in Matlab® environment or it requires to write a dedicated simulation tool or find a simulation tool that allows access to the simulation matrix.

3.3.2 Per Unit system

For a more general study and portability of the results and development presented throughout this thesis, most of results will be presented in per unit system. This section briefly set the references values.

General reference impedances

The reference impedance $Z_{N,m}$ is given by Equ. 3.6.

Equ. 3.6

$$\boldsymbol{Z_{N,m} = m\frac{V_N^2}{S_N}}$$

Where S_N is the nominal apparent power of the system under study, i.e. the apparent power that the generation set should inject into the grid. V_N is the nominal rms phase voltage and m the number of phase of the system. As there are two different sides with different number of phases, two nominal impedances are defined, one on the grid side and one on the generator side.

$$Z_{N3} = 3\frac{V_{N,grid}^2}{S_N} = Z_{N,grid} \qquad Z_{Nm} = m\frac{V_{N,gen}^2}{S_N} = Z_{N,gen}$$

As is shown above, the generator is connected in polygon. The relation between $V_{N.grid}$ and $V_{N,gen}$ is imposed, as given by Equ. 3.7.

Equ. 3.7

$$\boldsymbol{V_{N,gen} = 2V_{N,grid}\sin\left(\frac{\pi}{m}\right)}$$

In run time, the generator voltage will have to vary about 10% to be able to inject power with given power factor. The ratio between both impedances is given by Equ. 3.8 with the numerical values given in Table 3.2.

Equ. 3.8

$$\frac{Z_{N,gen}}{Z_{N,grid}} = \frac{m4\sin^2\left(\frac{\pi}{m}\right)}{3}$$

Table 3.2 – Numerical values of ratio of generator reference to grid references

m	3	6	9	12	15	18	21	24	27	30
$\frac{V_{N,gen}}{V_{N,grid}}$	$\sqrt{3}$ =1.73	1	0.68	0.51	0.42	0.34	0.29	0.26	0.23	0.21
$\frac{Z_{N,gen}}{Z_{N,grid}}$	3	2	1.40	1.07	0.86	0.72	0.62	0.55	0.48	0.44

Example of a numerical value for the nominal impedance of a high power installation, with S_N equal to a few hundreds of MVA:

$$Z_{N,grid} = 1.37\ [\Omega]$$

Generator per unit system

For the generator it is also practical to express some characteristics in a p.u system. A simple generator model is described in section 3.1. One stator winding impedance is constituted of a winding resistance R_g and a direct sub-transient inductance L''_d. So $L_g=L''_d$ For practical reason that will become clearer later, the reactance $X_g=\omega_g L_g$ and the resistance R_g can be expressed as a fraction of the generator impedance Z_g:

Equ. 3.9

$$x_g = \frac{X_g}{Z_g} \quad and \quad r_g = \frac{R_g}{Z_g} \quad with \quad Z_g = R_g + jX_g$$

Warning! x_g and r_g are not to be confounded with a more common notation of the electrical machines, where the reactance is referred to the nominal impedance of the machine, i.e. $Z_{N,gen}$.

The nominal short circuit current is defined as

Equ. 3.10

$$I_{N,short} = \frac{V_{N,gen}}{Z_g}$$

The p.u. nominal short circuit current, referred to the converter output nominal current $I_{N,o}$ is defined as

Equ. 3.11

$$i_{N,short} = \frac{I_{N,short}}{I_{N,o}} = \frac{3Z_{N,gen}}{2m\sin\left(\frac{\pi}{m}\right)Z_g} = \frac{2\sin\left(\frac{\pi}{m}\right)Z_{N,grid}}{Z_g}$$

It is more common in the description of the electrical machines to speak about per unit dirtect sub-transient winding reactance, which is referred to the nominal impedance of the machine, i.e. $Z_{N,gen}$. This notation was not used in the development of this thesis because it was not well adapted for the

developed formula. However, the value $i_{N,short}$ reflects the common per unit winding direct sub-transient reactor x''_d and the relation between $i_{N,short}$ and x''_d is given by Equ. 3.12.

Equ. 3.12

$$\boxed{x''_d \cong \frac{0.48}{i_{N,short}}}$$

Snubber p.u. system

Two reference values, or base values are defined:

Equ. 3.13

$$R_{base} = \frac{\Delta V_{peak}}{I_{o,peak}} \qquad C_{base} = L_g \left(\frac{I_{o,peak}}{\Delta V_{peak}}\right)^2 = \frac{L_g}{R_{base}^2}$$

which are respectively the base resistance and the base capacitor. ΔV_{peak} is the peak voltage across the generator phase and according to the assumptions, where the voltage drop across generator impedance are neglected in steady state, it is then EMF_{peak} . $I_{o,peak}$ is the peak load output current.

It is interesting to express the link between R_{base} and a nominal impedance.

Equ. 3.14

$$R_{base} = 2\sin\left(\frac{\pi}{m}\right) Z_{N3}$$

It is also interesting to express the base capacitance in function of the nominal impedance

Equ. 3.15

$$C_{base} = \frac{L_g}{R_{base}^2} = \frac{\frac{x_g Z_g}{\omega_g}}{4\sin^2\left(\frac{\pi}{m}\right) Z_{N,3}^2} = \boxed{\frac{x_g}{\omega_g i_{short}} \frac{1}{2\sin\left(\frac{\pi}{m}\right) Z_{N,3}}}$$

From those base values, the per unit snubber capacitor and resistor c_s and r_s are defined:

Equ. 3.16

$$c_s = \frac{C_s}{C_{base}} \qquad r_s = \frac{R_s}{R_{base}}$$

3.3.3 Case study - numerical values

Table 3.3 to Table 3.5 gives the numerical values of the parameters of the case study presented throughout this chapter and chapter 4.

Table 3.3 – Grid numerical values

3 phase Network	
$U_{N,3}$	**12.7 kVrms**
F_{grid}	50 Hz
L_T	364 µH
R_T	8.23 mΩ
X_T	114 mΩ
$\|Z_T\|$	115 mΩ
φ_T	85.9°

Table 3.4 – Operating point numerical values

Nominal Operating point			
P_N	**300 MW**	$\|z_T\|$	0.1 [pu]
PF	**0.85 (lagging)**	U_T	1.3kV
S_N	**353 MVA**	**u_T**	**0.1 [pu]**
φ_{PF}	37.8°	**Ucp**	**13.5 kVrms**
$\omega_{\gamma\rho\iota\delta}$	377 rad/s	u_{cp}	1.06 [pu]
I_o	**9.3 kArms**	maxUcp	14 kVrms
Z_{N3}	**1.37 Ω**	**EMF**	**3.1 kVrms**

Table 3.5 – Generator numerical values

27 phase delta Generator				
Parameters	**Case 1 and Case 2**	**Parameters**	**Case 1**	**Case 2**
Nominal EMF	2.949 kVrms	L_g	117 µH	58 µH
Nominal 3~ star voltage	12.7kVrms	X_g	73.5mΩ	36.4mΩ
Nominal 3~ line voltage	22kVrms	Z_g	73.5mΩ∠89.5°	36.4mΩ∠89.1°
$Z_{N,m}$ **(m=27)**	0.67 Ω	z_g	0.11	0.055
F_g	100Hz	$\lvert I_{short} \rvert$	40,1kArms	80,9kArms
R_g	575 µΩ	i_{short}	4.3	8.7
		r_g	0.00782	0.0157
		x_g	0.999969	0.999875

Table 3.6 – Typical snubber design values

Design constraint v_{sMax} **[1]**	c_s **[1]**	r_s **[1]**	$Z_{N,grid}$ **= 1.37 [Ω]** C_s [mF] per circuit
8	0.01	5	0.01
3	0.16	1.3	0.16
2	0.65	0.65	0.65

3.4 Commutation cell within the PPMC

3.4.1 Defining the commutation cell of the PPMC

The *slowCWC* sequence requires that the commutation instants are identical for the three output phases. This property of the control could be a problem when it comes to the current control because it diminishes the degree of freedom to control more accurately the three load currents but on the other side it guarantees the symmetry of the voltage applied to the load. In chapter 2, the basic commutation cell and the four steps commutation rule have been presented. This commutation cell is upgraded with the addition of the snubber, a RC leg, across the generator coil. An important assumption is that there is only one snubber involved in the commutation cell, which is the one across the outgoing generator phase. Due to symmetry, the voltages across all snubbers that are not involved in a commutation cell should not vary during the commutations. Compared to the basic cell of chapter 2, the arrangement of the current sources is different, it is a polygon. This does not change the behavior of the commutation cell. It only adds two current sources, called I_{oTR} and I_{oRS} for the output phase R, on each side of the generator coil involved in the commutation cell. Also, the generator voltages are not in star as described in chapter 2 but in polygon. The driving voltage available at the commutation instant is then simply the generator phase voltage and not the difference between incoming and outgoing.

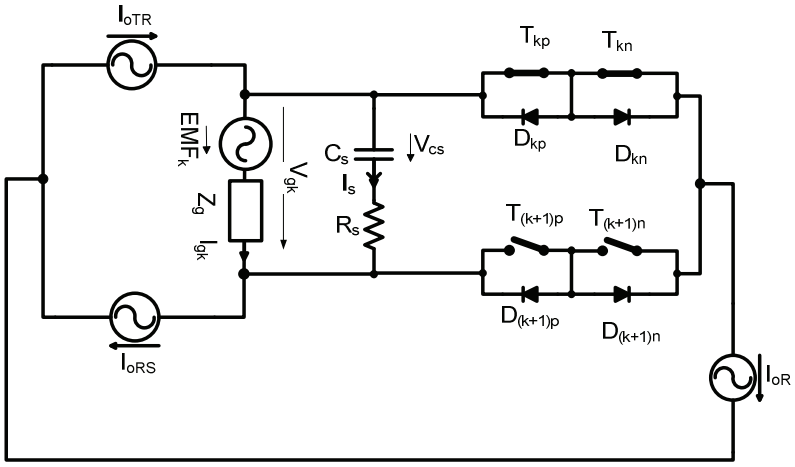


Fig. 3.10 – Commutation cell of the PPMC

The four steps commutation rule described in chapter 2 also works with the circuit of Fig. 3.10. However some details change and need to be described. Fig. 3.11 illustrates those four steps with the modified basic commutation cell. For each of those steps, simulation results from the case study are used to illustrate the described phenomenon.

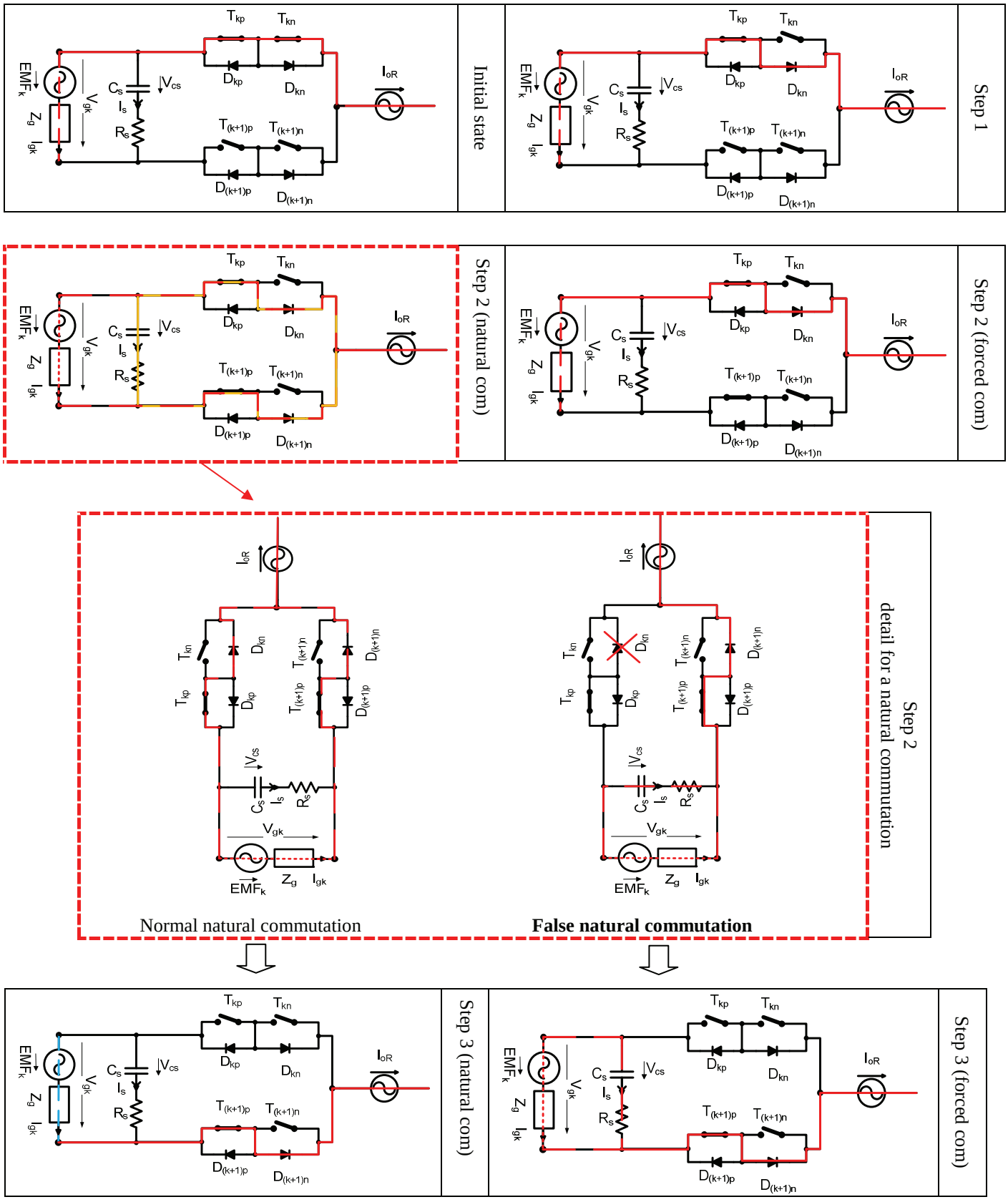
3.4.2 Four steps within the PPMC commutation cell

Step 1: on the outgoing phase, opening of the transistor T_k of opposed polarity than the current. Nothing is different here than in chapter 2.

Step 2: closing of the incoming transistor T_{k+1} of same polarity than current.

Forced commutation: in case of forced commutation, nothing happens here similarly to the basic cell of chapter 2.

Natural commutation: the RC leg is short circuited. Thus a discharge current, I_{dis}, flows through BDS_{k+1} and BDS_k, in the opposite direction of the output current to commutate. The net current flowing through BDS_k will be smaller than I_o. Depending on the value of the peak snubber discharge current, it may occur that this net current through BDS_k becomes negative, what would turn off the conducting diode D_k. If the diode is turned off, it will then remain turned off because it will be reverse biased (voltage across RC should be negative). Under this condition the commutation enters a similar situation as the forced one. So this natural commutation remains natural from the point of view of the switch constraints but from the point of view of the RC snubber, this commutation is a forced one. Such a commutation will be denoted by **"false natural commutation".**



Step 4 is straightforward and similar for natural and forced commutation

Fig. 3.11 – Four steps commutation rule for the commutation cell of the PPMC

Step 3: opening of transistor T_k of same polarity than load current.

Forced commutation: when opening the T_k, the generator current of the outgoing phase can flow through the capacitor leg into the load, through the previously closed switch of the incoming generator phase T_{k+1}. The capacitor's voltage will increase and induce a negative derivative of the current in the generator's outgoing phase. In order to damp the oscillations of the started LC regime, a resistor is inserted in series with the capacitor. We assume that switches withstand any rate of current and voltage rise, a constraint that will have to be reconsidered when dealing with real switches. The precise study of the transient regime is studied in the chapter 4.

Natural commutation: if the natural commutation was not stopped previously by the capacitor discharge current, and if the instant of step 3 is chosen accordingly to the duration of the natural commutation, nothing happens at step 3.

Step 4: closing of transistor T_{k+1} of opposite polarity than load current for automatic current reversal.

It is obvious that two parameters are important to know for the commutation cell of the PPMC. First, the duration of the natural commutation in order to place step 3 after the end of the natural transient. This is important for the practical implementation of the four steps procedure. The second parameter to know is the discharge current in order to know if the natural commutation is a true or a false one. This is important in the evaluation of the losses within the resistor of the snubber. Details of those two parameters are presented in section 3.5 and 3.6.

3.4.3 Natural commutations waveforms

This paragraph illustrates by simulation the natural commutations as presented in Fig. 3.11. Those simulation results are related to the parameters described in Case 2 of Table 3.5, with a 3p.u. snubber design.

Fig. 3.12 illustrates the case of a natural commutation occurrence (at time 125.35ms) within the PPMC. Fig. 3.12 (top) shows the general view and the position of the commutation within one output period and Fig. 3.12 (bottom) shows a zoom of the natural commutation. As predicted, the natural commutation occurs in the natural zone, positive current, negative driving voltage. It is a commutation from input phase 1 to input phase 2, on the output phase R. One can observe that the expected ideal converter output waveform is hard to distinguish. The transient regime due to commutation is not negligible in terms of fundamental modification. Even though there are ripples on the current, it will still be considered as a very good approximation of an ideal sinus waveform. In Fig. 3.12 (bottom), one can clearly observe the outgoing (blue trace) and incoming (green trace) currents. One can also see the current through the outgoing BDS and the effect of the discharge of the snubber capacitor. This discharge current I_{dis} is never higher than the current flowing through the outgoing BDS hence the natural commutation is not shortened. At the time when the outgoing current becomes null, the outgoing BDS's diode blocks and the snubber capacitor recharges to the value of a final value which is the generator winding voltage V_g.

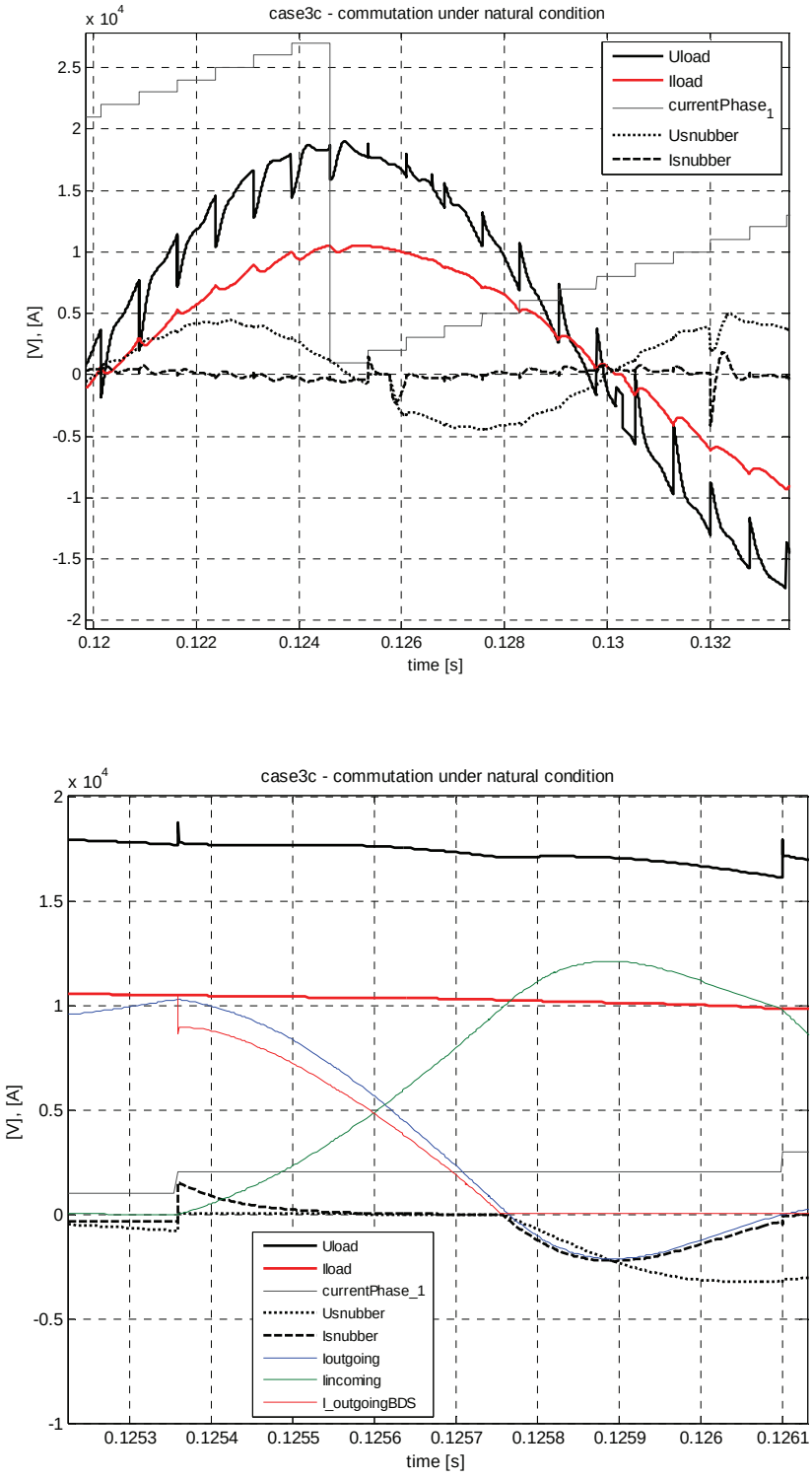
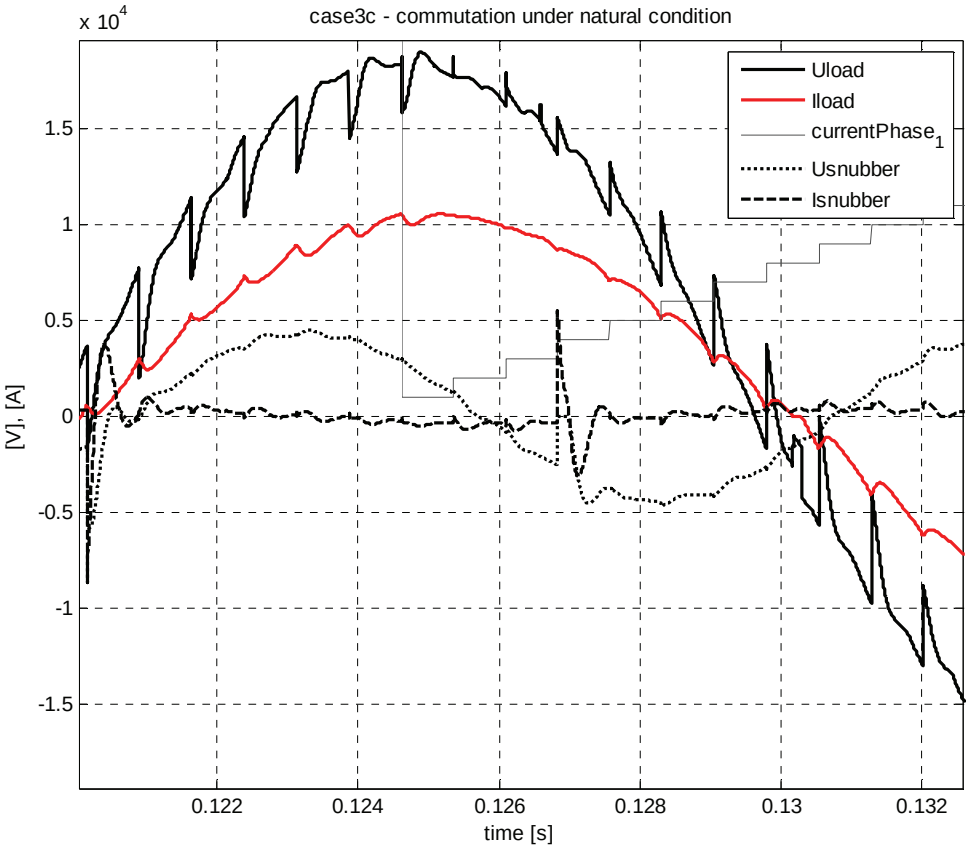


Fig. 3.12 – Simulation result showing a natural commutation occurrence

This can be observed in Fig. 3.12 by the second order transient started as $I_{outgoing}$ reverses. One can see that this transient is not completely damped until the occurrence of the next commutation, at time=126.1 ms

The duration of this natural commutation is about 400µs. Referred to the generator electrical period T_g (10ms) this gives a relative duration of 4%.



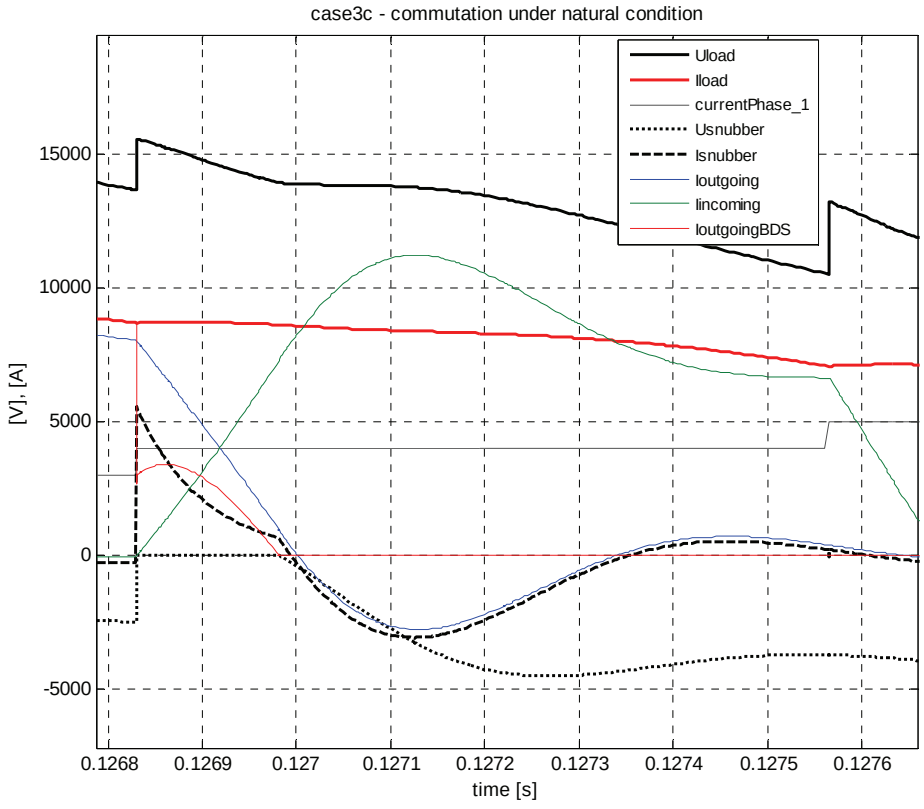


Fig. 3.13 – Simulation result showing a shortened natural commutation occurrence

Fig. 3.13 illustrates another natural commutation, which, if observed carefully, is shortened near its natural end. This is a premature commutation case and the handling of this case will be detailed in the section 3.6.3. This case will however still be considered as a natural commutation in a first approximation. In Fig. 3.13 (top) this commutation also occurs in the theoretical natural zone. In Fig. 3.13 (bottom), a zoom on this commutation, the effective current in the BDS is shown with the fine red trace and again, the discharge effect of the capacitor is highlighted when comparing the red trace with the outgoing current (blue trace). The small cut-off occurrence advance can be observed but remain small in comparison with the commutation duration. Once the diode of the outgoing BDS has turned off, again, it is a second order transient response that is started. It can be remarked that the duration of the commutation, is shorter than in previous case of Fig. 3.12. This is because the driving voltage available for this occurrence is higher than for the previous example.

Duration of this natural commutation: 170µs, which is 1.7% of T_g.

3.4.4 False natural commutation waveforms

This paragraph illustrates by simulation the false natural commutations as presented in Fig. 3.11. Those simulation results are related to the parameter described in Case 2 of Table 3.5, with a 3p.u. snubber design.

Fig. 3.14 illustrates an occurrence of a false natural commutation. This commutation also takes place in the natural zone but as can be observed, the transient response is different than the previous cases. The voltage V_g is not null as it should be during a natural commutation. Besides, one can see the peak value of the discharge current which is the same magnitude as the output current, meaning that the net current in the outgoing BDS is negative, as can be more precisely observed in Fig. 3.14 (bottom). This is a limit case and on the Fig. 3.14 (bottom) it is hard to see that the peak discharge was slightly bigger than the output current, however it is the case and the diode of the outgoing BDS has turned off. Right at the turn off instant, the rise of the voltage across snubber ensures the application of a reverse voltage on third diode as long as the snubber voltage remains negative. It is clear that if this voltage jump is higher than the snubber capacitor voltage, V_g might become positive and forward bias the diode that just turn-off, which result in a reopening of this diode. This could then lead to a natural commutation case again. The precise description of the complex phenomenon will not be part of this thesis because it is considered to be too complex and occurrences to scarce. This would require more accurate models of the transistor and diode, with dynamic behavior and not only static behavior.

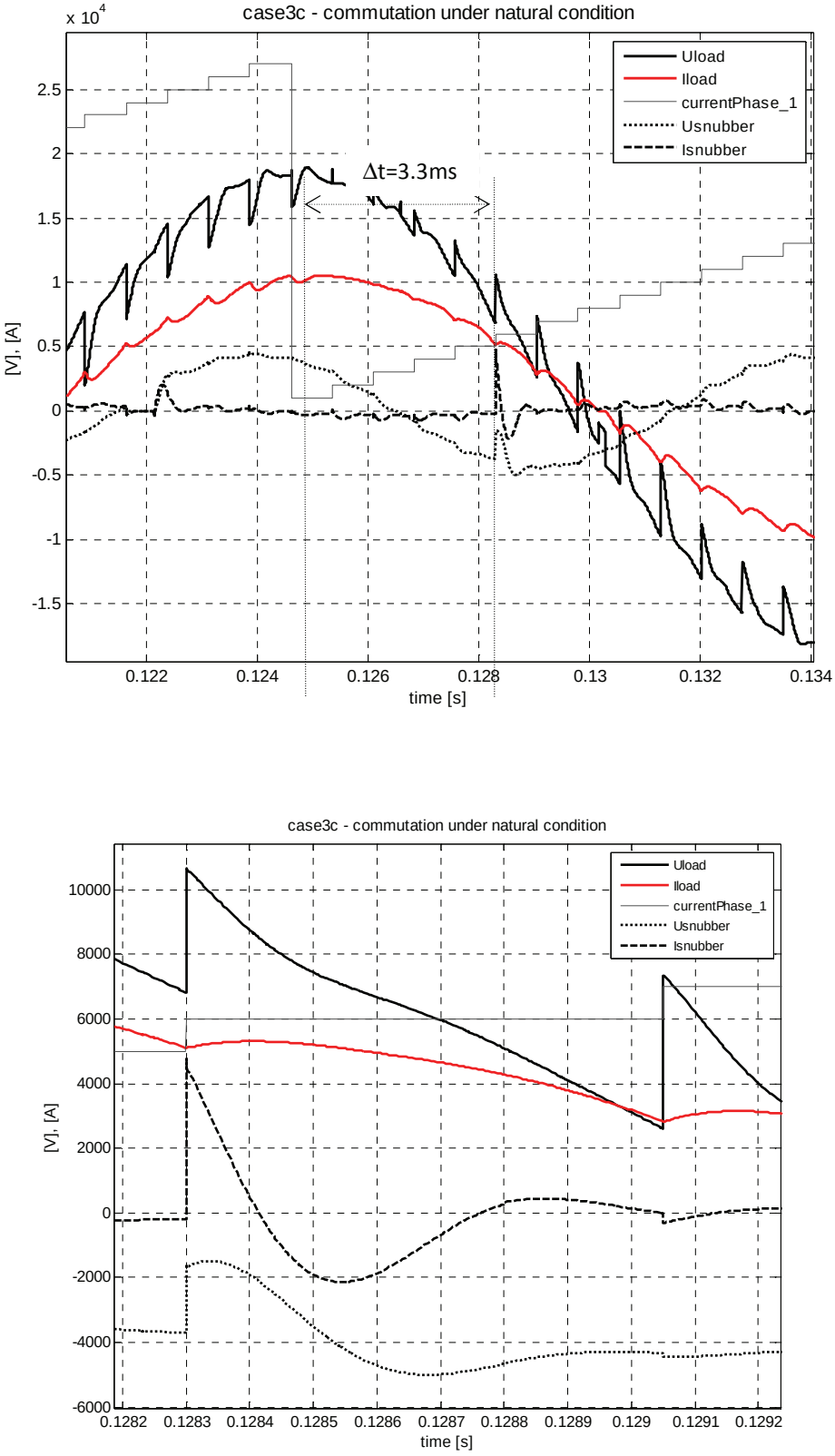


Fig. 3.14 – Simulation result showing a false natural commutation occurrence

Fig. 3.15, an extra zoom of Fig. 3.14, shows that the static model of the transistor and diode, used in the simulation is not sufficient to clearly describe the details of the commutation and turn-off behavior of diodes. It can be observed that the simulator, at step 2, computes a current jump and directly change the states of the diode to off. Also, the modeling of the commutation cell is not accurate enough and should include parasitic inductors that would represent the physical limit of rate of rise of the current in the RC leg. Altogether, a more accurate model of switches and snubber leg and generator would be necessary to investigate precisely the turn-off phenomenon for false natural commutations. This is not the goal of this work because a general and less accurate study of the PPMC must first be performed before going into such details.

This commutation occurs at an angular position related to the output voltage given by Equ. 3.17.

Equ. 3.17

$$\frac{3.3ms}{20ms} \times 360° + 90° \cong 150°$$

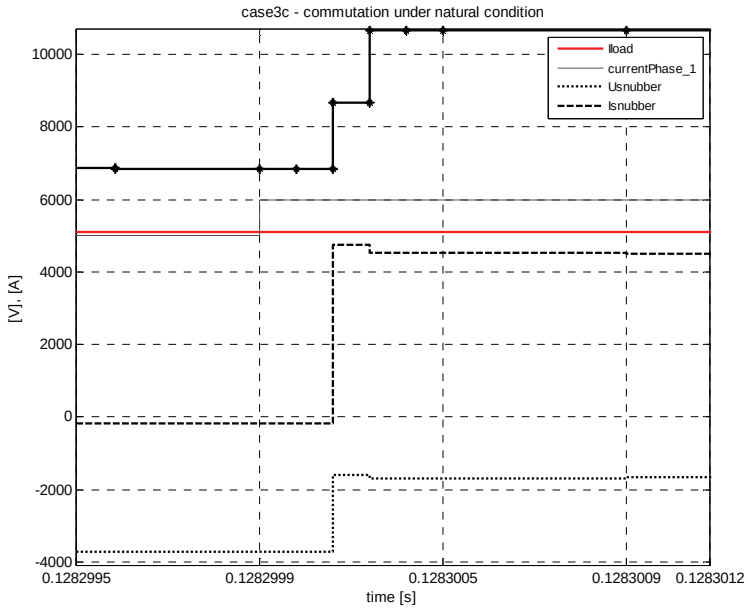


Fig. 3.15 –Closer view of Fig. 3.14

3.5 The duration of natural commutation

3.5.1 Introduction

This section gives a brief overview and numerical values about natural commutation duration. According to the four steps commutation rule, it is necessary to know the duration of the natural commutation in order to set the correct delay between step 2 and step 3, otherwise the natural commutation cannot finish properly and become forced.

In [13], the computation of the commutation duration is performed because the control also needs this value, moreover in real time. In [13], one can find the analytical expression of the current of the outgoing input phase from the time t_0 when the natural commutation is started, that is from instant of step 2 translated into the four steps rule. This expression is derived from a commutation cell identical to the commutation cell of the PPMC (Fig. 3.10). From this expression, the time needed for this outgoing current to reach zero is deduced. As seen in the previous section, the commutation cell of the PPMC presents an additional leg, the RC snubber leg. As explained, for natural commutation occurrences, the presence of the snubber does not affect the behavior of the currents in the incoming and outgoing input phases, it only affects the current in the BDS involved in the commutation cell. Therefore, the equation expressed in [13] will be reused here. The commutation cell from which this equation is derived assumes a time varying driving voltage ΔV and but still a constant load current. In [13] comparison of commutation duration computed with simulation model and calculated from this analytical expression have shown that model level of this commutation cell is fine enough. It is reasonable to assume the same for our case since the studied converter in [13] is very similar to the PPMC.

3.5.2 The relative natural commutation duration

This section aims at working out this expression in order to present results where the commutation duration is expressed in a relative quantity (per unit). Especially, the commutation duration will be expressed as a fraction of the generator electrical period T_g, where the generator parameters are already expressed in the per unit system. Besides, it is wished to express the commutation duration in function of the natural commutation position along the "natural zones" of the output period T_o.

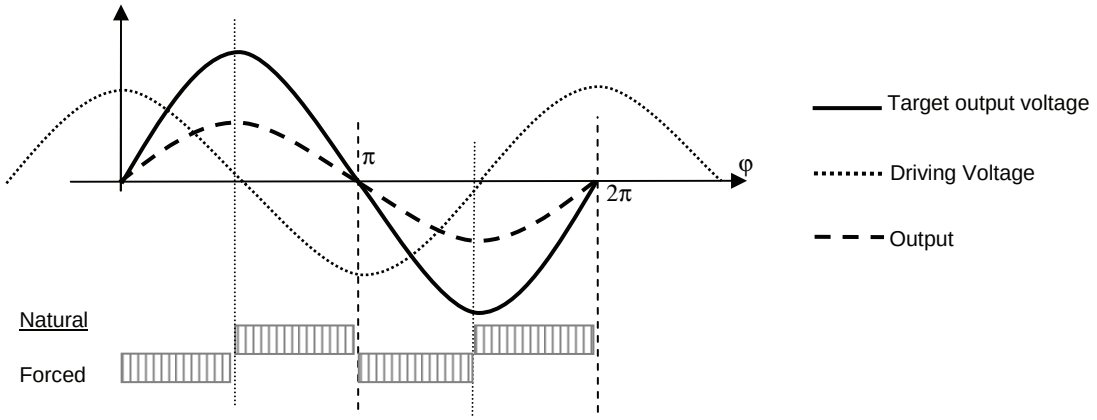


Fig. 3.16 – Position and width of commutation types zones (forced and natural)

As the computation of the commutation duration is only relevant for natural commutation, the commutation positions that are relevant are between $\frac{\pi}{2}$ and π for unity power factor for the positive half wave. For leading power factor, this range still starts at $\frac{\pi}{2}$ but stops at $\pi - \cos^{-1}(PF)$. Similarly, for lagging power factor the range is $\pi + \cos^{-1}(PF)$. Output current and initial driving voltage can be expressed easily in function of φ according to Fig. 3.16.

Expression of [13] is completed with the information about driving voltage waveform at commutation start and this leads to Equ. 3.18.

Equ. 3.18
$$\boldsymbol{I_{outgoing} = e^{-\frac{R_g}{L_g}t}\left[I_o - \frac{\widehat{\Delta V}}{L_g}\frac{\omega_g \sin(\varphi)+\frac{R_g}{L_g}\cos(\varphi)}{\left(\frac{R_g}{L_g}\right)^2+\omega_g^2}\right] + \frac{\widehat{\Delta V}}{L_g}\frac{\frac{R_g}{L_g}\cos(\omega_g t+\varphi)+\omega_g \sin(\omega_g t+\varphi)}{\left(\frac{R_g}{L_g}\right)^2+\omega_g^2}}$$

where φ is the position of the beginning of the natural commutation along one output period. Several interesting ratios can be pointed out:

$$\frac{R_g}{\sqrt{\left(R_g^2+\left(\omega_g L_g\right)^2\right)}} = \frac{R_g}{|Z_g|} \quad and \quad \frac{\omega_g L_g}{\sqrt{\left(R_g^2+\left(\omega_g L_g\right)^2\right)}} = \frac{X_g}{|Z_g|} \quad and \quad \frac{\widehat{\Delta V}}{|Z_g|}$$

where Z_g is the generator winding impedance. The next setps use the per unit system for the generator parameters presented in paragraph 3.3.2. Besides, the outgoing current is expressed in per unit, referred to the current at commutation start, as showed by Equ. 3.19.

Equ. 3.19
$$\boldsymbol{i_{outgoing}(t) = \frac{I_{outgoing}(t)}{I_{outgoing}(0)} = \frac{I_{outgoing}(t)}{\widehat{I}_o \sin(\varphi+\varphi_{pf})}}$$

Finally, the following variable change is used: $t=sT_g$. All this results in Equ. 3.20, which gives the outgoing current in function of the time for given p.u. generator parameters (see Table 3.7) and operating point parameter and commutation position.

Equ. 3.20
$$i_{outgoing}(s) = e^{-2\pi\frac{rg}{xg}s}\left[1 - \frac{i_{short}}{\sin(\varphi_{comm}+\varphi_{PF})}\left(x_g \sin(\varphi_{comm}) + r_g \cos(\varphi_{comm})\right)\right]$$
$$+ \frac{i_{short}}{\sin(\varphi_{comm}+\varphi_{PF})}\left[r_g \cos(2\pi s+\varphi_{comm}) + x_g \sin(2\pi s+\varphi_{comm})\right]$$

Table 3.7

x_g	r_g	i_{short}
0.999969	0.00782	4.3
0.999875	0.0157	8.7

Fig. 3.17 shows commutation duration for several lagging power factors with the per unit generator parameters of Table 3.7. The leveling off that can be observed for φ around 100° is artificially introduced. This level corresponds to the time between two commutation (T_c) for *m*=27 and a frequency conversion from 100Hz to 50Hz. For a unity power factor, the commutation duration is then non negligible in front of T_c for the first 40° of the natural commutation zone. However compared to T_g, those are still below 10%. For the first 40° of the natural zone, commutation duration decrease with decreasing lagging power factor, as expected. But, situation is reversed for commutation angles from 140 up to the end of the zone.

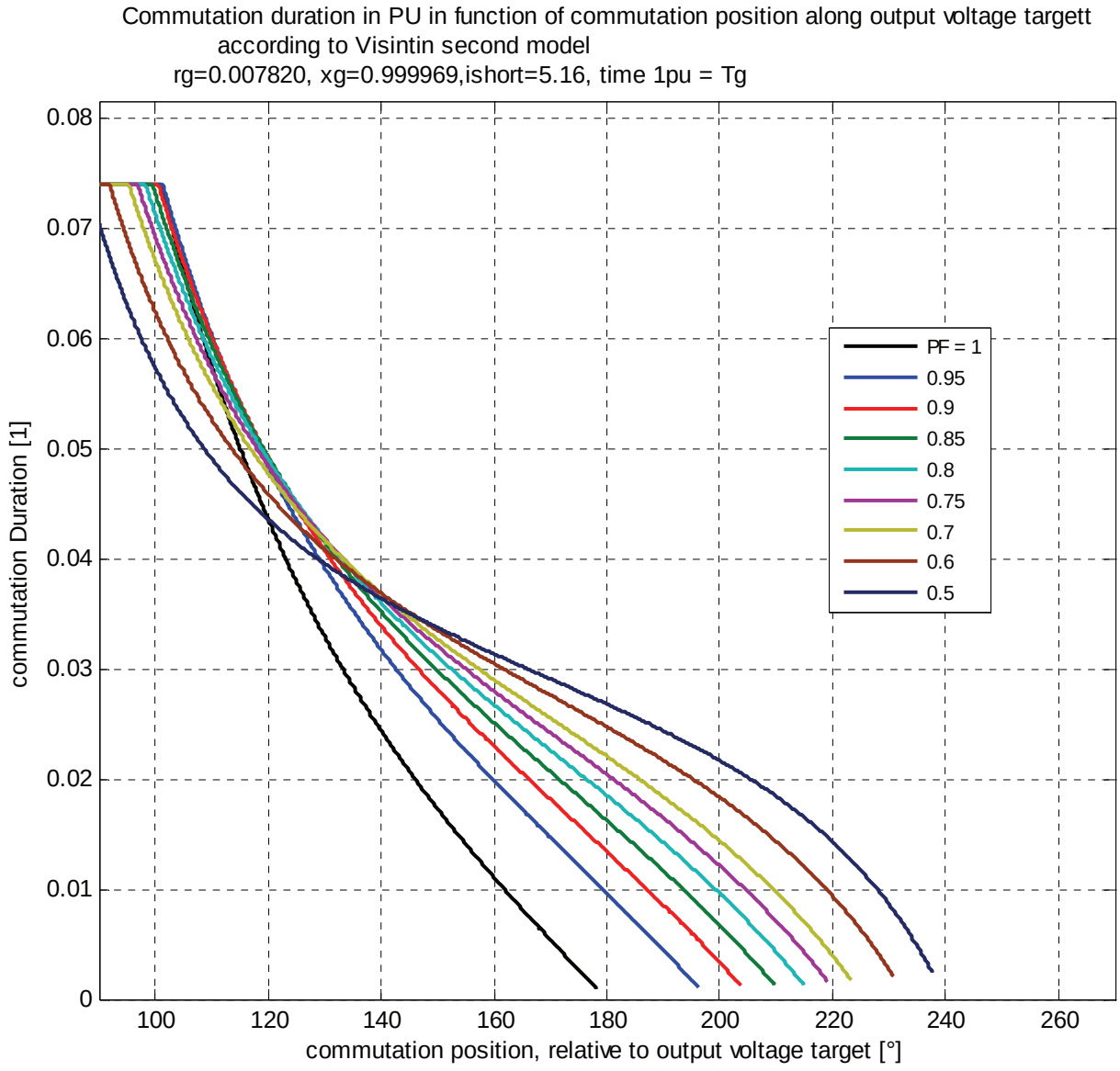


Fig. 3.17 –Commutation duration in function of commutation position for several power factors

Fig. 3.18 is similar to Fig. 3.17 but for a different design of the machine's inductance, leading to a short circuit current that is doubled (from 5 p.u. to 10 p.u.). General behavior of commutation duration in function of commutation position and power factor is similar than Fig. 3.17. Only the overall duration are lowered.

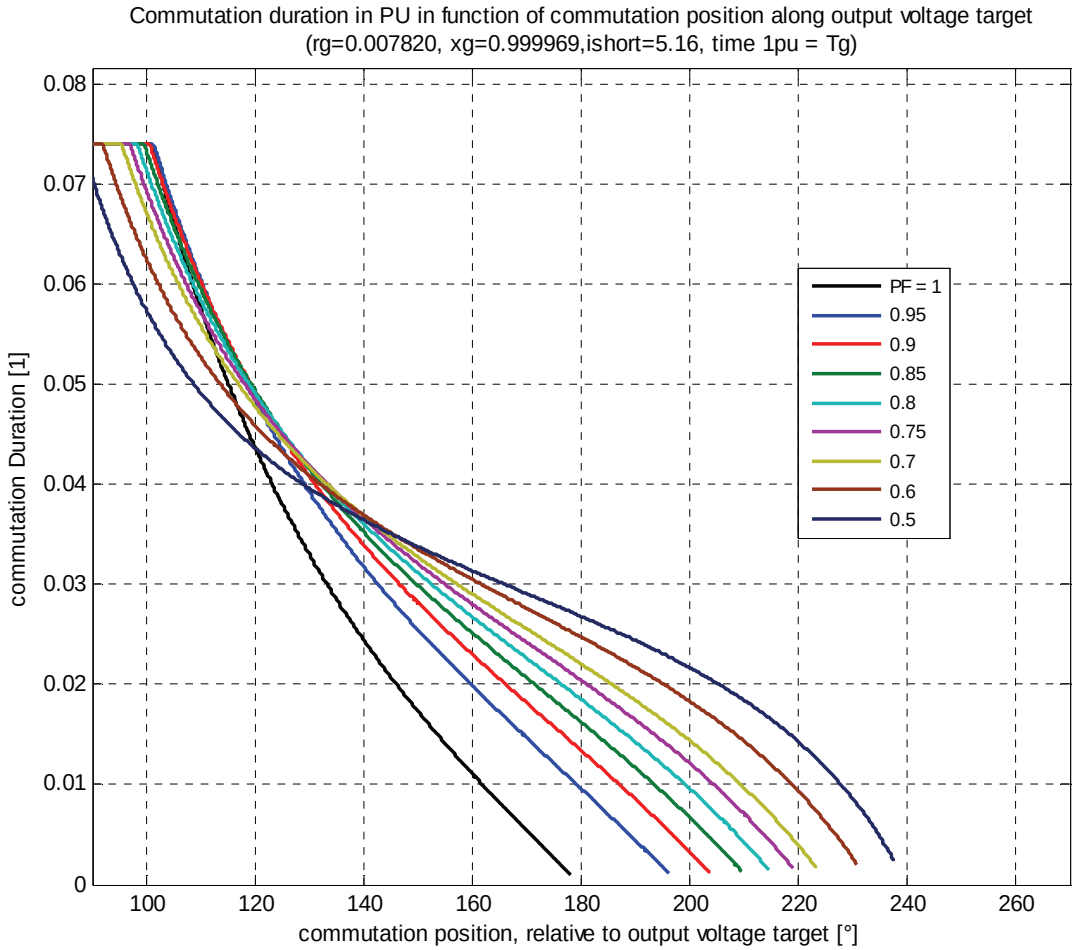


Fig. 3.18 - Commutation duration in function of commutation position for several power factors

Fig. 3.19 shows the effect of i_{short} with the same generator parameters r_g and x_g as Fig. 3.17 and Fig. 3.18, for unity power factor. I_{short} plays a critical role in commutation duration.

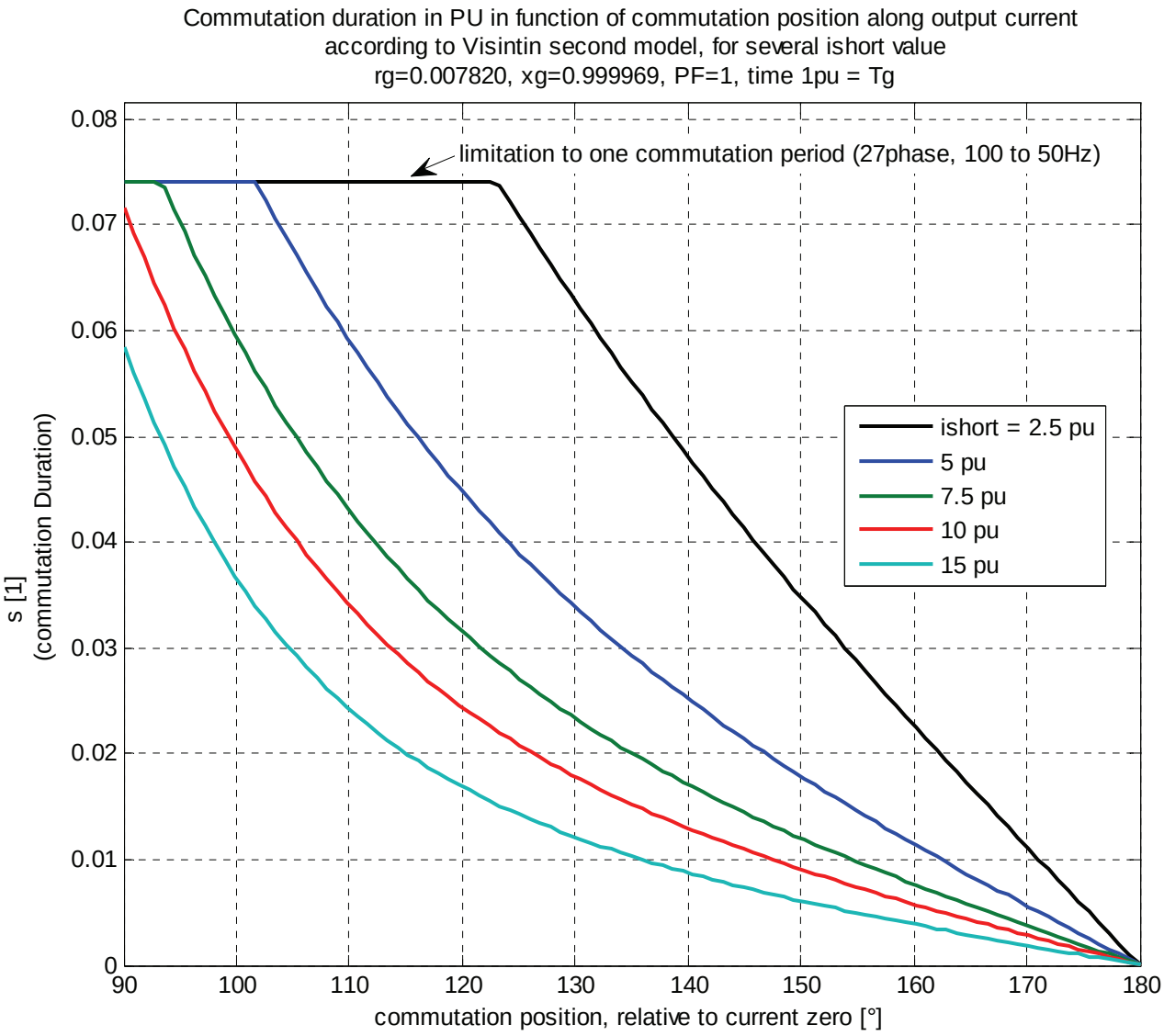


Fig. 3.19 - Commutation duration in function of commutation position for several values of i_{short}

Fig. 3.20 shows a variation of the parameters r_g and x_g with a given i_{short} value of 5p.u.. When modifying r_g, x_g is adapted to keep Z_g constant. This shows that the precise value of r_g and x_g do not influence commutation duration as much as the parameter i_{short}. Here, doubling r_g only slightly affects the commutation duration.

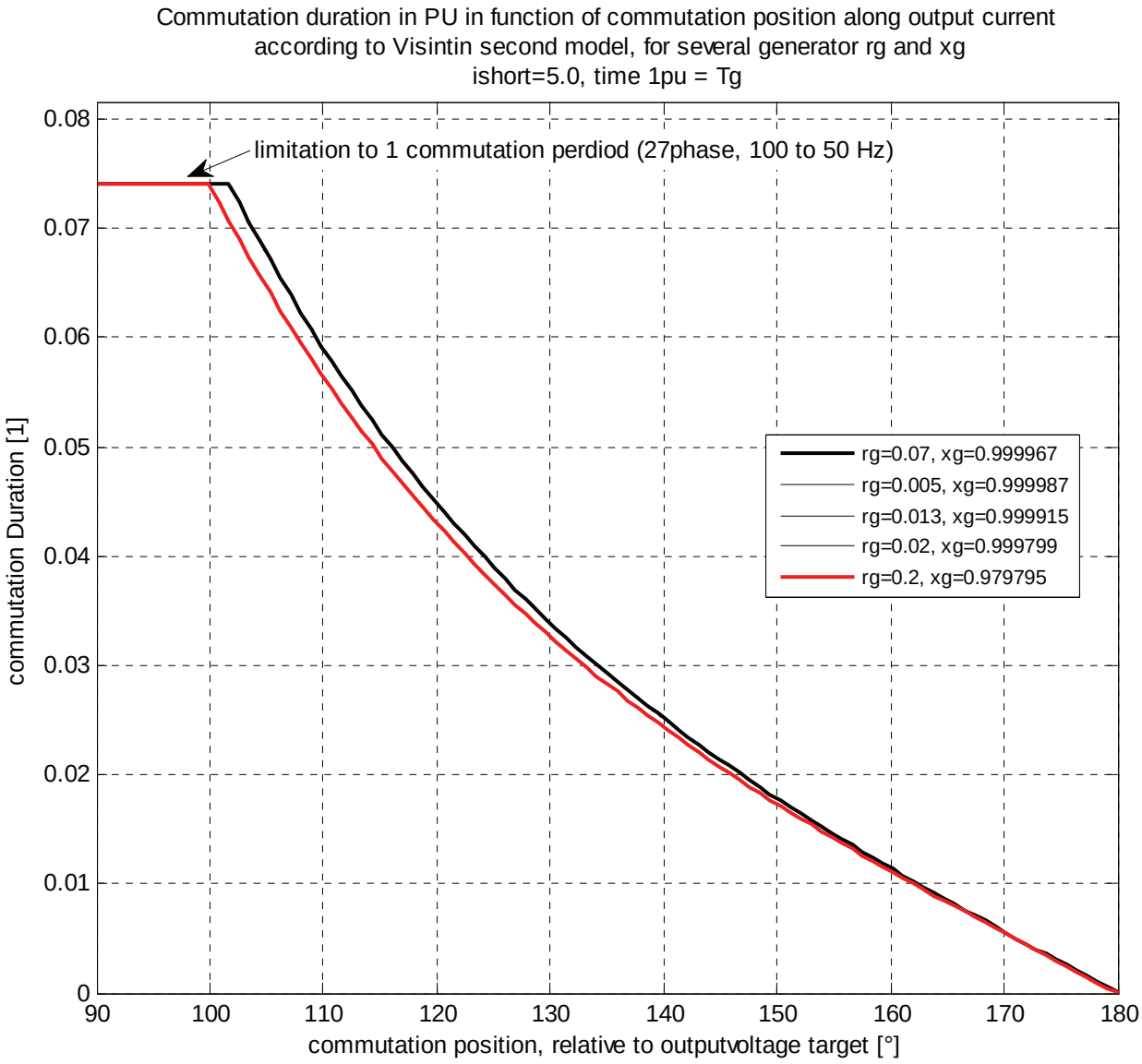


Fig. 3.20 - Commutation duration in function of commutation position for several values of x_g and r_g

As a conclusion of this p.u. analysis of natural commutation duration, performed on the basis of simplified machine model, one can say that for the typical generator p.u. parameter given above, most natural commutation can entirely exist within the commutation period T_c. Especially at the beginning of the natural zone, their duration is not negligible in front of T_c and might affect strongly the shape of the converter output voltage. Forcing the commutation with appropriated gating signal control for those cases might be necessary. It also shows that the key parameter for existence of natural commutation is the parameters i_{short}. Usually, this parameter is kept to a given value in order to limit destruction in case of permanent short circuit and also, if generator is connected to power electronics, this short circuit parameter should be kept to a low limit in order to match short circuit capability of the silicon device.

3.6 Existence of natural commutation

As shown in Fig. 3.16, the zone of forced commutation and natural commutations along one output period are clear and depends on the power factor. Section 3.4.2 has detailed the four steps commutation for the commutation cell with a RC snubber and it has highlighted that the discharge current occurring at the step 2 of a natural commutation could turn off the outgoing BDS and transform this natural commutation in a forced commutation, from the point of view of the transient response. This section aims at defining the area of false natural commutations.

3.6.1 Three cases

Here are three figures that show the current flowing through the outgoing BDS and both of its components – the natural negative slope due to natural commutation phenomenon and the RC response of the discharge, as expressed by Equ. 3.21.

Equ. 3.21

$$I_{BDSout}(t) = I_o - \frac{\Delta V}{L_g} t - \hat{I}_{dis} e^{-\frac{t}{RC}}$$

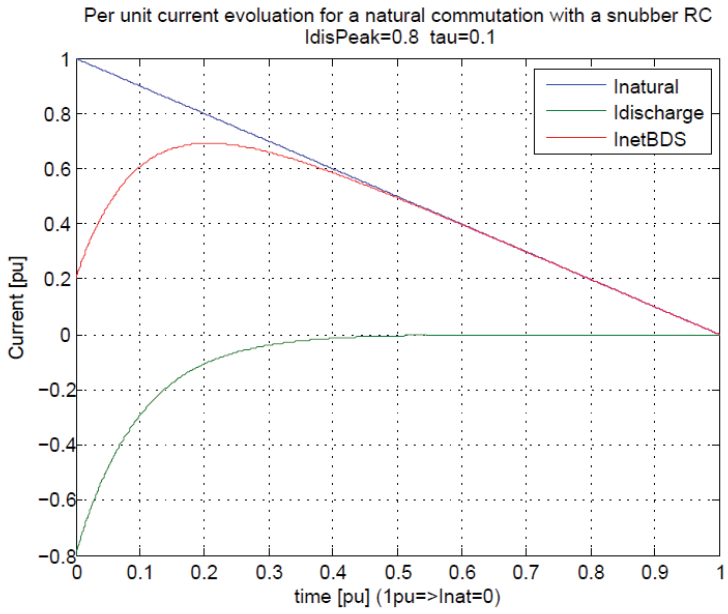


Fig. 3.21 – Decomposition of BDS current into its both components for a natural commutation

The first figure, Fig. 3.21 shows a normal natural commutation, where the discharge current of the capacitor does not affect the location of the BDS current zero crossing. At the closing of the incoming switch, current in the outgoing phase decrease with a given rate that can be approximated to $\Delta V/L_g$. Besides, the capacitor of the snubber discharges until zero. The peak discharge current is smaller than I_o and the discharge time constant $T_s=R_sC_s$ is much smaller than the natural commutation duration t_{off}. Fig. 3.21 to Fig. 3.23 are plotted in p.u., that is the natural commutation duration is 1 and the initial current I_o is 1. When the current of the outgoing BDS crosses zero its diode turns off. At that instant, there is should be a transient response of the RLC circuit of this commutation cell

because the snubber capacitor voltage must recharge to its equilibrium voltage ΔV. This transient response is not shown in Fig. 3.21 which stops at the zero crossing of I_{BDS}.

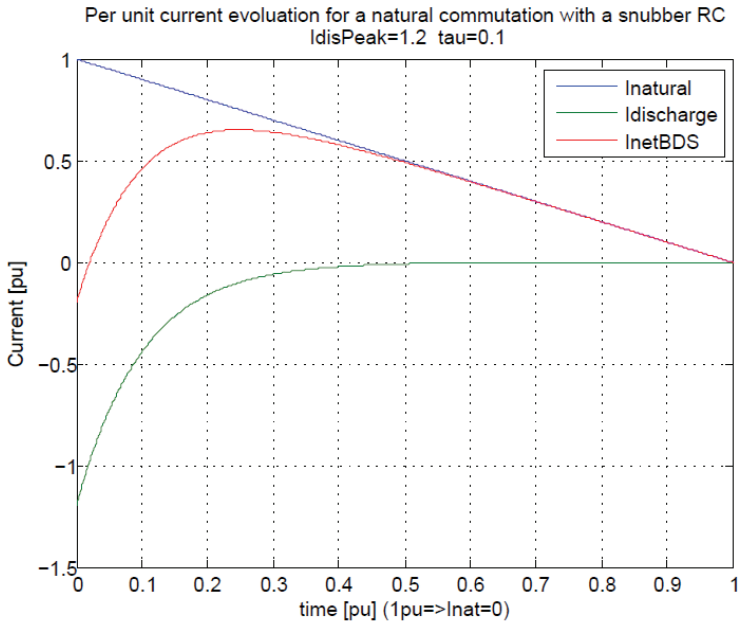


Fig. 3.22 - Decomposition of BDS current into its both components for a false natural commutation

Fig. 3.22 illustrates a false natural commutation. The initial discharge current is greater than the output current. Therefore, the diode should turn off. So the curves in Fig. 3.22 are not representative of the real commutation. It only shows how the current in BDS evolves without considering the diode. The description of the transient response occurring when the diode has turned off is as follows. The snubber voltage, with the initial capacitor voltage which is negative, instantaneously increases to reach the value $\Delta V + R_s I_o$. Then there is a transient oscillatory response and the snubber voltage stabilize again on a value given by ΔV (t_{end}). Here, the transistor of the outgoing switch is still on. If during the transient response, the snubber voltage crosses zeros and become positive, what can possibly occur, it will forward bias the diode of the outgoing switch which will conduct again. Then the commutation regime is again the one of a natural commutation, with the current decreasing derivative $\Delta V/L_g$

Fig. 3.23 represents a middle case, between normal and false natural commutation, called early or premature cut-off.

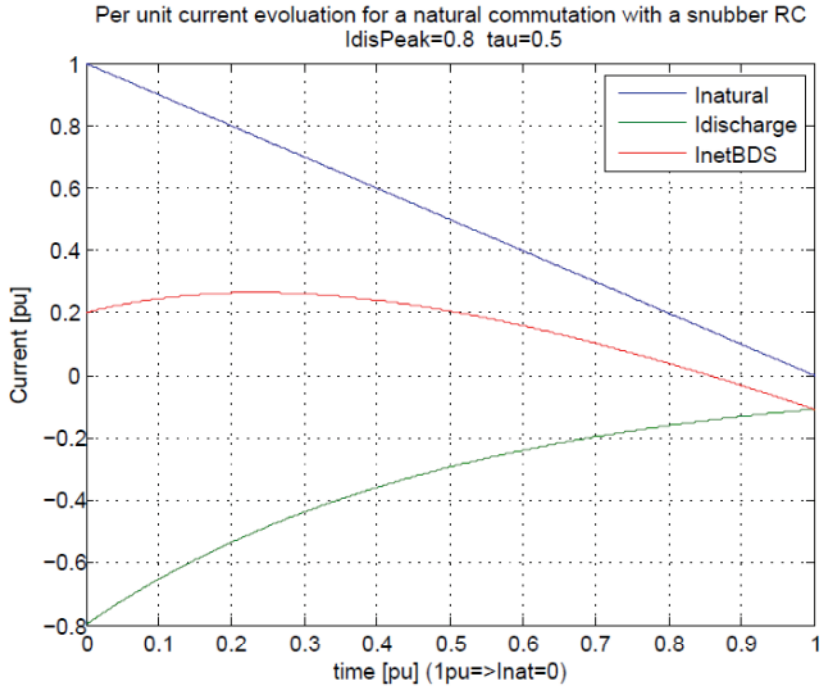


Fig. 3.23 - Decomposition of BDS current into its both components for a early cut-off

Even if the initial discharge current is smaller than the output current, the time constant of the discharge makes the net current in the BDS smaller than the current in normal natural commutation, thus it will cross zero before 1 p.u.

3.6.2 Occurrences of false natural commutations

The condition to test if commutation is false or not is the peak discharge current $I_{dis,peak}$ that must be greater than the current to commute I_o as given by Equ. 3.22.

Equ. 3.22

$$\hat{I}_{dis} = \frac{\Delta V}{R_s} > I_o$$

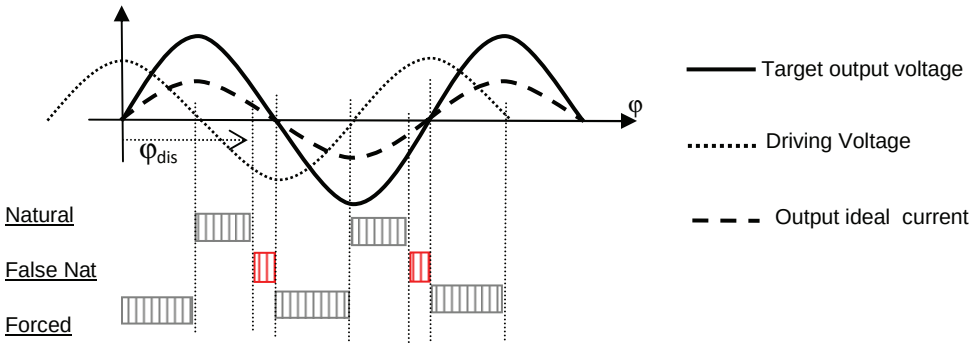


Fig. 3.24 – Schematic representation of appearance of zones of false natural commutation

Using Fig. 3.24 to express the relation between ΔV and I_o, one can find the angle φ_{dis}, along the natural commutation zone, from which the condition of Equ. 3.22 is reached. φ_{dis} can be computed from Equ. 3.23. This brings out the per unit resistor of the snubber (see paragraph 3.3.2). The design method of the snubber gives the necessary values of r_s. r_s plays a key role in determining occurrences φ_{dis}.

Equ. 3.23

$$\boldsymbol{\varphi_{dis} = \tan^{-1}\left(\frac{\frac{1}{r_s}+\sin(\varphi_{pf})}{-\cos(\varphi_{pf})}\right)}$$

Fig. 3.25 plots the value of φ_{dis} in function of the power factor angle φ_{pf}, for several design values of r_s. For natural commutation above this angle, the i_{dis} >1 and hence commutations are false natural.

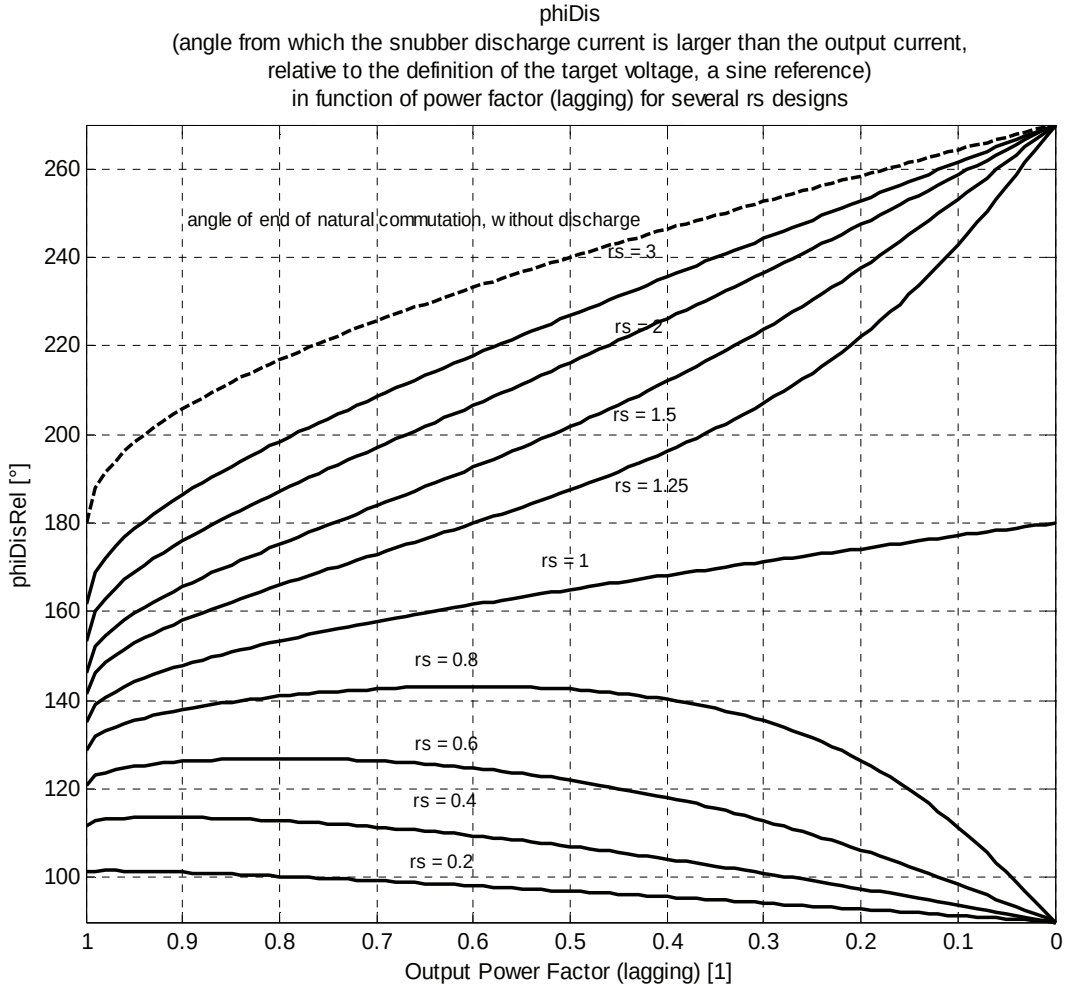


Fig. 3.25 – False commutation zone starting angle in function of lagging power factor for several r_s

On Fig. 3.25, the bipolar behavior that can be observed for low power factor near 0 comes from the instability around the value r_s=1. For r_s<1, the argument of the $\tan^{-1}$ function is negative, for r_s>1, the argument of the $\tan^{-1}$ is positive, which explains the 180° divergence between curve with r_s<1 and r_s>1. Physically this has the following meaning: for null lagging power factor, depending if r_s is below or above 1, the whole zone of natural commutation will be replaced by false natural commutation or

not at all resp. In practice, of course, such a divergence will not be so sharp and other phenomena will influence the response, so attention must be paid for those cases in practice.

In case of a false natural commutation, it can be noted that, with the values of c_s and r_s given by the design method, the overvoltage will not forward re-bias the diode.

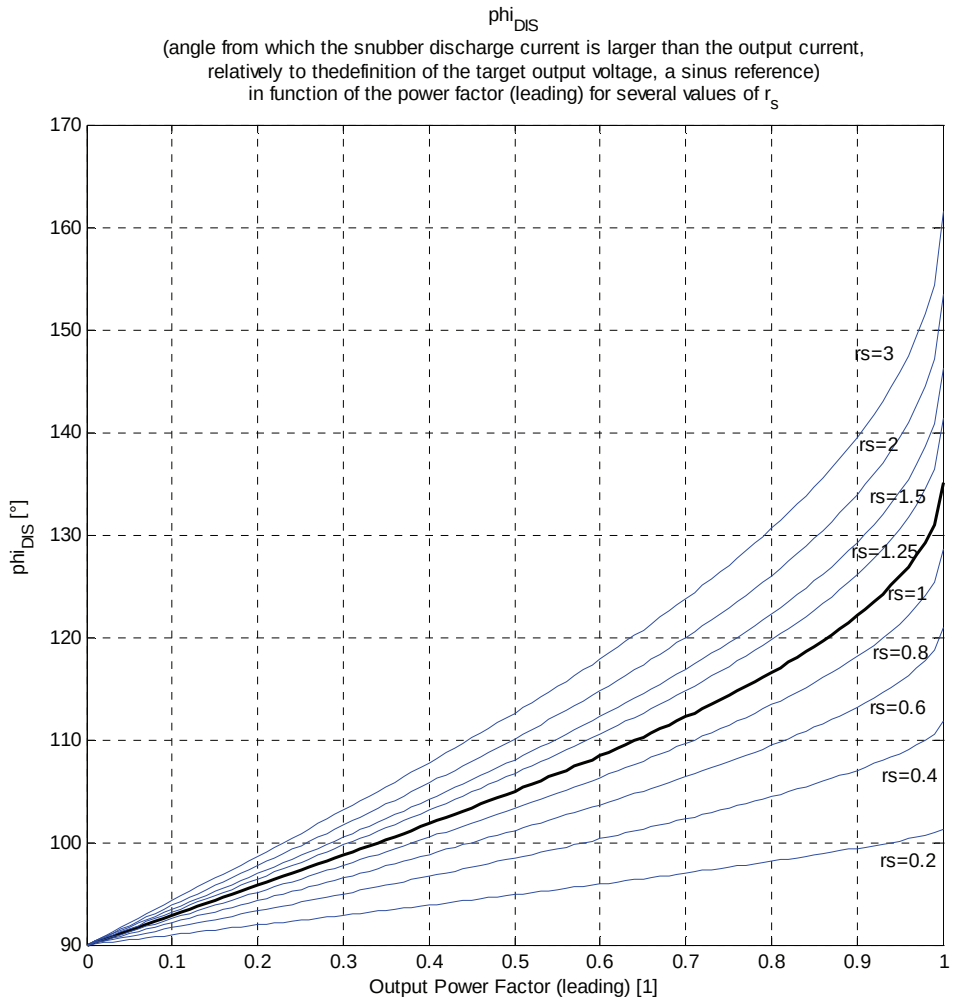


Fig. 3.26 - False commutation zone staring angle in function of leading power factor for several r_s

Similarly to Fig. 3.25 but for leading power factors, Fig. 3.26 plots the angle φ_{dis}. For leading power factors, the behavior of φ_{dis} is more intuitive and the role of snubber design through r_s is much less significant than for lagging power factor. With decreasing leading power factor, the zone of natural commutation reduces, so the impact on knowing if it is a true natural commutation or a false commutation is less and less important.

3.6.3 Occurrences of early cut-off phenomenon

If the assumption is made that the outgoing current derivative is linear, then it is easy to say if the natural commutation will be early (prematurely) stopped, when and how. For a worse case, i.e. the magnitude of the discharge current is equal to the load current to commutate, this only depends on

the ratio of the snubber time constant to the natural commutation duration t_μ (t_μ=μ/360*T_g).In Fig. 3.27, several current evolutions are plot for several T_s/t_μ ratios. For the ratio up to 0.4, the advance of the zero crossing of the current is such that the current cut–off occurs at 10% of the starting value.

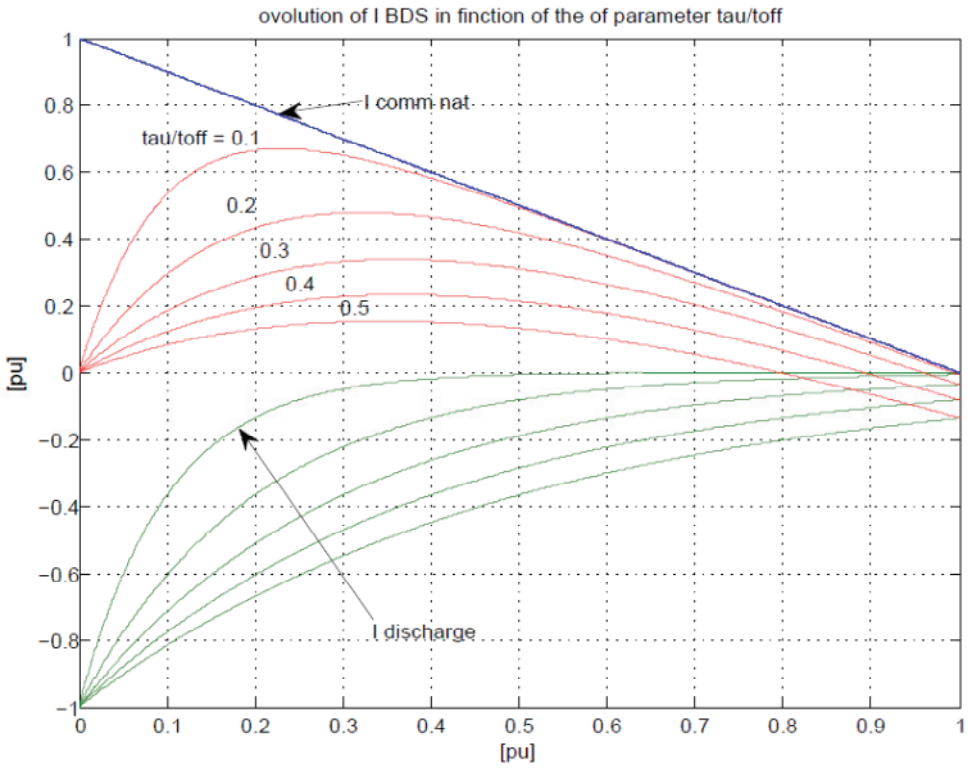


Fig. 3.27 – Occurrences of early cut-off current in function of relative snubber time constant

The occurrence of early cut-off depends on snubber design. Besides, the natural negative slope of the outgoing current is not linear. A more refined approach to state the occurrences of premature cut-off is briefly presented here.

$$I_{dis}(t) = \hat{I}_{dis} e^{\frac{-t}{T_s}}$$

with snubber time constant $T_s = R_s C_s$

Change of time variable $t = sT_g$

$$I_{dis}(s) = \hat{I}_{dis} e^{\frac{-sT_g}{T_s}} = \hat{I}_{dis} e^{\frac{-s}{\tau_s}}$$

with $\tau_s = \dfrac{T_s}{T_g}$

Expression of τ_s with known p.u. parameters

$$\tau_s = \frac{R_s C_s}{T_g} = \frac{r_s R_{base} c_s C_{base}}{T_g} = \frac{r_s c_s L_g}{T_g R_{base}} = \frac{r_s c_s X_g}{2\pi R_{base}}$$

$$X_g = x_g \left| Z_g \right| = x_g \frac{V_{N,gen}}{I_{short,nom}} = x_g \frac{V_{N,gen}}{i_{short,nom} I_o} = \frac{x_g}{i_{short,nom}} R_{base}$$

$$\Rightarrow \tau_s = \frac{r_s c_s}{2\pi} \frac{x_g}{i_{short}}$$

So, the current in the outgoing BDS, referred to the nominal load current

$$i_{BDS}(s) = i_{outgoing}(s) - i_{dis}(s)$$

where s is the relative time and where $i_{outgoing}$ can be computed with the equation of section 3.5

From the p.u. expression is the current through the outgoing BDS, i_{BDS}, the time of zero real zero crossing of net current of BDS is computed and the corresponding outgoing current at that time is deduced. This shows the effective value of $i_{outgoing}$ as the BDS turns off. This value is called $i_{outgoing\_off}$. In case where no early cut-off occurs, this value is also 0. Table 3.8 gives typical values for snubber design and for generator parameter i_{short}.

The value $i_{outgoing\_off}$ can be computed for each commutation position, and for several power factors and several snubber designs. For one power factor with a given snubber design, one can take the maximum value $i_{outgoing\_off}$ among all commutation positions. This gives the value $i_{outgoing\_offMAX}$.

Table 3.8 – Typical snubber design and generator parameters and relative snubber time constant

Snubber design	r_s	c_s	$r_s c_s$	τ_s with i_{short}=5	τ_s with i_{short}=10
3pu	1.3	0.166	0.22	0.006	0.003
2pu	0.65	0.65	0.42	0.013	0.007

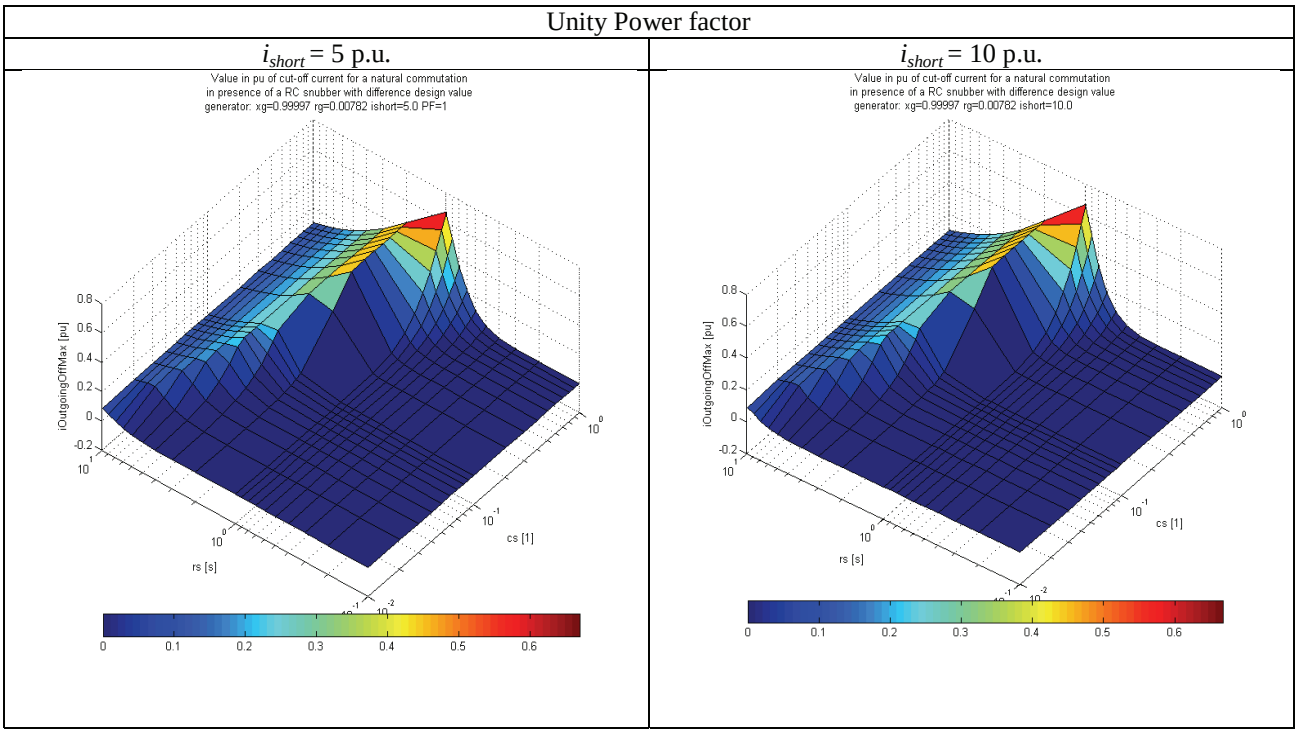


Fig. 3.28 – Plot of $i_{outgoing\_offMax}$ in function of snubber design, with unity power factor, for i_{short}=5p.u. and 10p.u.

Fig. 3.28 to Fig. 3.30 show some numerical values for $i_{outgoing\_offMAX}$. Fig. 3.28 represent a unity power factor, Fig. 3.29 a lagging power factor of 0.9 and Fig. 3.30 a lagging power factor of 0.8. It can be concluded that for a standard generator and standard snubber design, the value of the outgoing current at cut off for natural commutation is below 0.05 p.u., where 1 p.u. is the peak value of the output current. This means that the early cut-off phenomenon can be neglected and that a natural commutation is either false or purely natural.

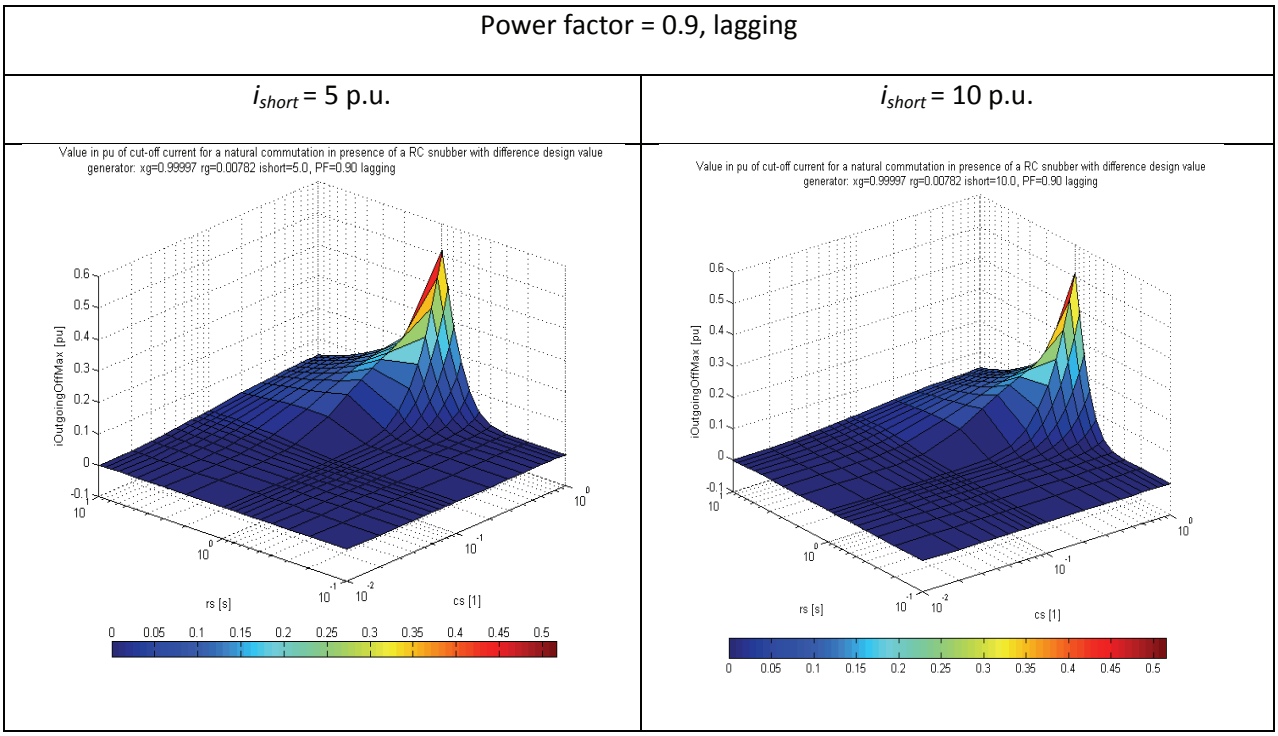
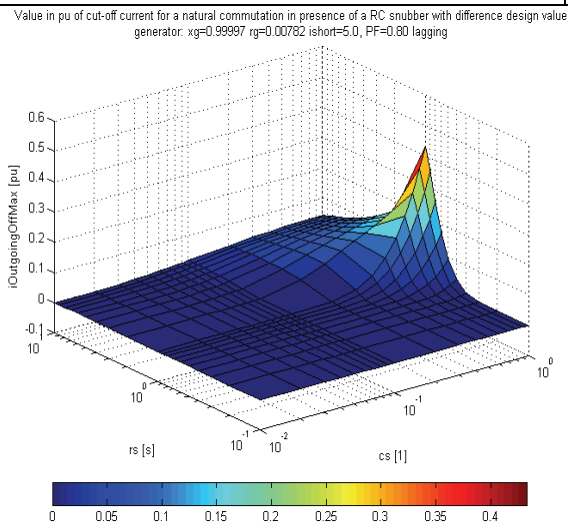


Fig. 3.29 - $i_{outgoing\_offMax}$ in function of snubber design, with power factor 0.9 lag, for i_{short}=5p.u. and 10p.u.

Power factor = 0.8 (lagging)	
i_{short} = 5 p.u.	i_{short} = 10 p.u.



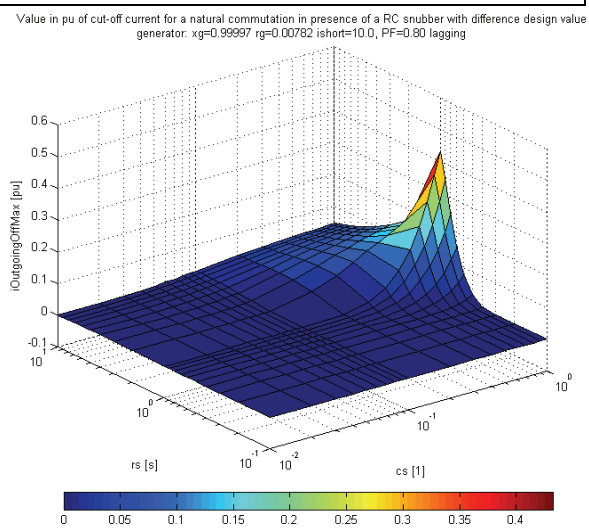


Fig. 3.30 - - $i_{outgoing\_offMax}$ in function of snubber design, with power factor 0.8 lag, for i_{short}=5p.u. and 10p.u.

However the shapes of Fig. 3.28 to Fig. 3.30 present a zone where the early cut-off phenomenon is not negligible and $i_{outgoing\_off}$ takes values that goes beyond 0.5p.u. This is where the relative time constant τ_s is high because of C_s and R_s. But this area of high value of $i_{outgoing\_offMax}$ strangely decreases when further increasing R_s. This is because when Rs increases, the discharge current of capacitor decreases and hence, even if discharge time is long, it does not lead to significant early cut-off phenomenon. Anyway, those area of high $i_{outgoing\_offMax}$ values are out of usual snubber design.

Finally, it can be observed that the shapes of Fig. 3.28 to Fig. 3.30 do not significantly change when comparing for each both cases i_{short} = 5 p.u. and i_{short} = 10 p.u.. When increasing i_{short}, the relative snubber time constant decreases but the commutation duration too. All in all, the parameters i_{short} for a given power factor, has a small influence.

3.7 Conduction losses

The conduction losses of the PPMC are evaluated with a relatively simple model and linear static characteristic of the silicon devices. From the static characteristic of one transistor, the equivalent static characteristic of the half a BDS is built from the number of series and parallel connections required to comply with total voltage blocking capability and current rating. The diodes in parallel of each transistor are neglected in this conduction losses evaluation. It is assumed that this omission brings conservative results.

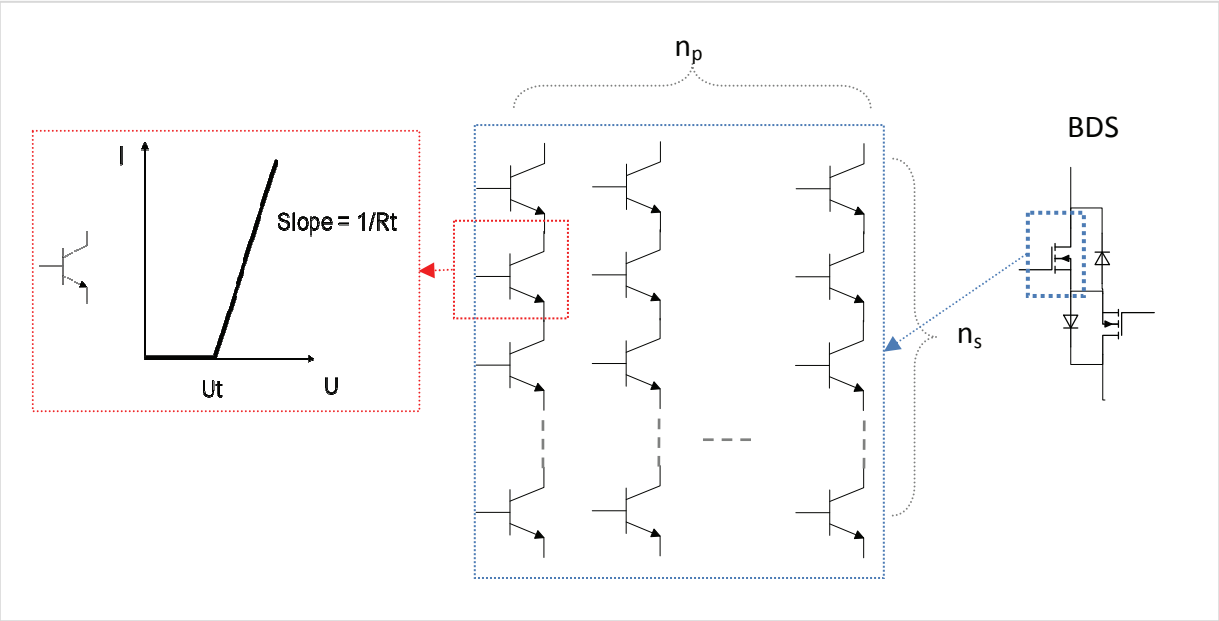


Fig. 3.31 – Decomposition of the BDS into the elementary switches

The instantaneous power dissipated through one half of a BDS is given by Equ. 3.24.

Equ. 3.24 $$P_{cond}(t) = U_{t,equ}|I_o(t)| + R_{t,equ}I_o^2(t) \quad with \quad U_{t,equ} = n_s U_t \qquad R_{t,equ} = \frac{n_s}{n_p}R_t$$

The mean power over one output period dissipated through one BDS for the three output phases is given by Equ. 3.25.

Equ. 3.25 $$\overline{P_{cond}} = 3\int_0^{T_o} P_{cond}(t)\,dt = \boxed{6\left(\frac{2}{\pi}U_{t,equ}I_o + R_{t,equ}I_{oRMS}^2\right)}$$

For more global results, the relative dissipated power is expressed in Equ. 3.26.

Equ. 3.26 $$p_{cond} = \frac{\overline{P_{cond}}}{P_o} = \frac{1}{\cos(\varphi_{pf})}\left[\left(\underbrace{\frac{4\sqrt{2}}{\pi}}_{=1.8}\frac{U_{t,equ}}{U_{n,rms}}\right) + \left(2R_{t,equ}\frac{I_{oRMS}}{U_{n,RMS}}\right)\right]$$

Table 3.9 – BDS total voltage and current rating

P_o [MW]	U_n [kV]	I_o [kA]	BDS blocking voltage requirements [kV]	BDS current capability [kA]
300	12.7	7.9	36	12

Table 3.10 – Computation of conduction losses for several samples of IGBT

Rated Voltage	Rated Current	switch Base impedance	U_t	u_t (%)	R_t (@125°C)	r_t (%)	n_s	n_p	n_{sw}	$p_{BDS,Rt}$ (%)	$p_{BDS,Ut}$ (%)	P_{BDS} (%)
1700	2400	0.71	1.2	0.071	0.00050	0.07	22	5	110	0.28	0.38	**0.66**
1700	1800	0.94	1.2	0.071	0.00075	0.08	22	7	154	0.30	0.38	**0.68**
1700	800	2.1	1.2	0.071	0.00180	0.08	22	14	308	0.36	0.38	**0.74**
3300	1500	2.2	1.5	0.045	0.00100	0.05	11	8	88	0.18	0.25	**0.43**
3300	1200	2.7	1.7	0.052	0.00180	0.07	11	10	110	0.24	0.25	**0.49**
4500	1000	4.5	1.7	0.038	0.00220	0.05	8	12	96	0.18	0.20	**0.38**
4500	650	6.9	1.7	0.038	0.0036	0.05	8	18	144	0.20	0.20	**0.40**
6500	600	10.8	3	0.046	0.0044	0.04	6	19	114	0.18	0.26	**0.44**
6500	400	16.3	3	0.046	0.0063	0.039	6	28	168	0.16	0.26	**0.42**

Table 3.10 gives some numerical results for the AG application with nominal values of case study given in 3.3.3. For this, numerical parameters of a few available high voltage switches are used. The technology used for this study is IGBT although the assessment should also handle IGCT. The goal here is only to have an estimation of the conduction losses for the PPMC in order to compare them with commutation losses and snubber losses. The choice of IGBT will deliver conservative results since it can be admitted that the on-state resistance of IGBT is higher than IGCT. However, IGCT turn-on or -off time might be longer than for IGBT, which will strongly influence the commutation losses as developed in next section.

Globally, it can be deduced from Table 3.10 that conduction losses for the PPMC stay in a reasonable range and are a small fraction of the output delivered power that stays below 1%. All values of Table 3.10 are given for a unity power factor. There are four main blocks which represents each time a given voltage blocking capability of one IGBT. For each block, several current ratings are handled. The number of series and parallel connections of switches, necessary to build one half valve of one BDS, is computed on the base of the maximum voltage that the switches must withstand. One can consider the huge number of total elementary IGBT that only one BDS requires. The practical realization of those BDS is surely very complex and should be a research work in itself. This will obviously not be handled here.

As given by Equ. 3.24, the reduction of n_s directly reduces the conduction losses due to the voltage drop U_t. The value of the voltage drop relative to the blocking capability of one switch is not linear hence the utilization of high blocking capability is recommended however only up to 4500V. A reverse tendency is observed for the 6500V devices. For the choice of the current ratings, it is

obviously the highest available that gives the better result because improvement of R_t with the increasing of the current rating outpace the reduction of R_{tequ} due to paralleling of switches (n_p). The best design choice for conduction losses reduction is highlighted in Table 3.10 and corresponds to a blocking voltage of 4500V with a current rating of 1000A. It leads to conduction losses of 0.38% which is still 1.1MW for the case study. This power is to be distributed among the 3x27 BDS, which results in 14kW per BDS. This is largely below the power dissipation that would be achievable for a BDS made out of the silicon device of Table 3.10.

3.8 Switching losses

This section roughly assesses the switching losses of the PPMC. First, it is necessary to model the dynamic behavior of the BDS. This is not the goal of this work to go into details of dynamic behavior of the silicon device. Simple constant dv/dt for the Collector-Emitter voltage of transistors is assumed when turning on. Let us analyze the commutation cell of Fig. 3.11 in order to spot which switch dissipates energy when turning on or off.

3.8.1 Losses for one forced commutation

When analyzing the four steps commutation process with forced commutation conditions, there will be no power dissipated at step 1, step 2 and step 3 since the transistors are turned on and off under null voltage or current conditions. To be more precise, it is not really null voltage but a forward voltage of the parallel diode, which we will consider as negligible because the power dissipated for those 3 steps will be much smaller than the power dissipated at step 3.

At step 3, the load current is interrupted in the outgoing leg because the transistor turns off. The load current will then flows through the free-wheeling path, which is the snubber leg. For this to be possible, the diode of the incoming BDS must first be forward bias. Until step 3 it is negative biased and approximately support the voltage ΔV. So the transistors must first rises its collector-emitter voltage V_{CE} to ΔV before anything can happen. So it is a rising of its V_{CE} under constant current with the value of the load current I_o. Now, assuming that dV_{CE}/dt is constant and that, then, the opening of the diode is infinitely short, the energy dissipated for this turning off process is given by Equ. 3.27.

Equ. 3.27

$$E_{BDS,1forced} = \frac{\Delta V \cdot I_o}{2} t_{off}$$

where t_{off} is the time needed for V_{CE} to reach ΔV.

3.8.2 Losses for one natural commutation

When analyzing the four steps commutation process with natural commutation condition. There will be no power dissipated for step 1, step 3 and step 4 since it will be on or off transitions under zero voltage or zero currents. Diodes are assumed to be very fast without recovery phenomenon.

Until step 2 the incoming transistor is blocking the voltage ΔV. When it turns on, the situation goes towards the short circuit of the generator outgoing phase. This transistor reduced its VCE voltage until it reaches zero. If there was no snubber, this will be a turn on under zero current because the increase of the current in the incoming leg is much slower than the time for the transistor to turn on (t_{on}). This is correct when looking at the natural commutation time constants described in section 3.5.

However, on the PPMC topology there is the presence of the snubber, which is assumed to instantaneously react to the negative dV_{CE}/dt, since it has per definition no inductive component. Hence this will be a turn on under increasing current. With the assumption that the dV_{CE}/dt is constant, the energy dissipated for such a commutation is given by

Equ. 3.28
$$E_{BDS,1\,Nat} = \frac{\Delta V^2}{6R_s} t_{on}$$

where R_s is the resistor of the snubber.

3.8.3 Overall conduction losses under mix mode operation

Both previous paragraphs give an expression for the commutation losses of one forced, resp. natural commutation under given initial conditions ΔV and I_o with given commutation opening, resp. closing duration t_{off} resp. t_{on}. This paragraph aims now at expressing the total commutation losses of the converter for one output period T_o. According to figure Fig. 3.16, ΔV and I_o can be expressed in function of the angular position φ_c along the output period, also in function of the power factor angle φ_{PF}. With the same method as the truncated sinusoidal waveform, which will be presented later in section 4.2.9, the overall losses can be expressed for different power factor in function of frequency ratio and phase number. As in chapter 4, the losses are expressed relatively to the losses when all commutations are full forced, which appears for a null leading power factor. One important assumption is that the opening time t_{off} and closing time t_{on} are equal, what can in practice be discussed. Besides, it is also assumed that t_{off} and t_{on} are independent of the voltage under which the switch must open or close. In this case, the commutation losses are given by Equ. 3.29.

Equ. 3.29
$$E_{BDS,full\,forced} = \frac{3N\Delta V_{RMS} I_{oRMS}}{2} t_{off} \qquad with \qquad N = \frac{T_o}{T_c}$$

where N is the number of commutations period T_c per output period T_o. Equ. 3.30 gives then the relative commutation losses, relative to $E_{BDS,full\ forced}$, in function of the power factor angle and for different values of the relative snubber resistance r_s.

Equ. 3.30
$$e_{BDS} = \underbrace{\frac{1}{\pi}\left[\cos(\varphi_{pf}) + \sin(\varphi_{pf})\left(\frac{\pi}{2} + \varphi_{pf}\right)\right]}_{forced\ com\ contribution} + \underbrace{\frac{1}{3\pi r_s}\left[\frac{\pi}{2} - \varphi_{pf} - \frac{1}{2}\sin(\varphi_{pf})\right]}_{natural\ com\ contribution}$$

Fig. 3.32 is a graphical representation of Equ. 3.30. So, as expected, for leading null power factors, the losses are 1 pu. Then for the other extreme, null lagging power factor, where there are only

natural commutations, the losses are either bigger or smaller than 1 p.u. depending on the snubber resistor, as expressed by Equ. 3.30. As will be seen later on, for typical design values of r_s, $e_{BDS}=1$ is a good general conservative commutation losses estimation.

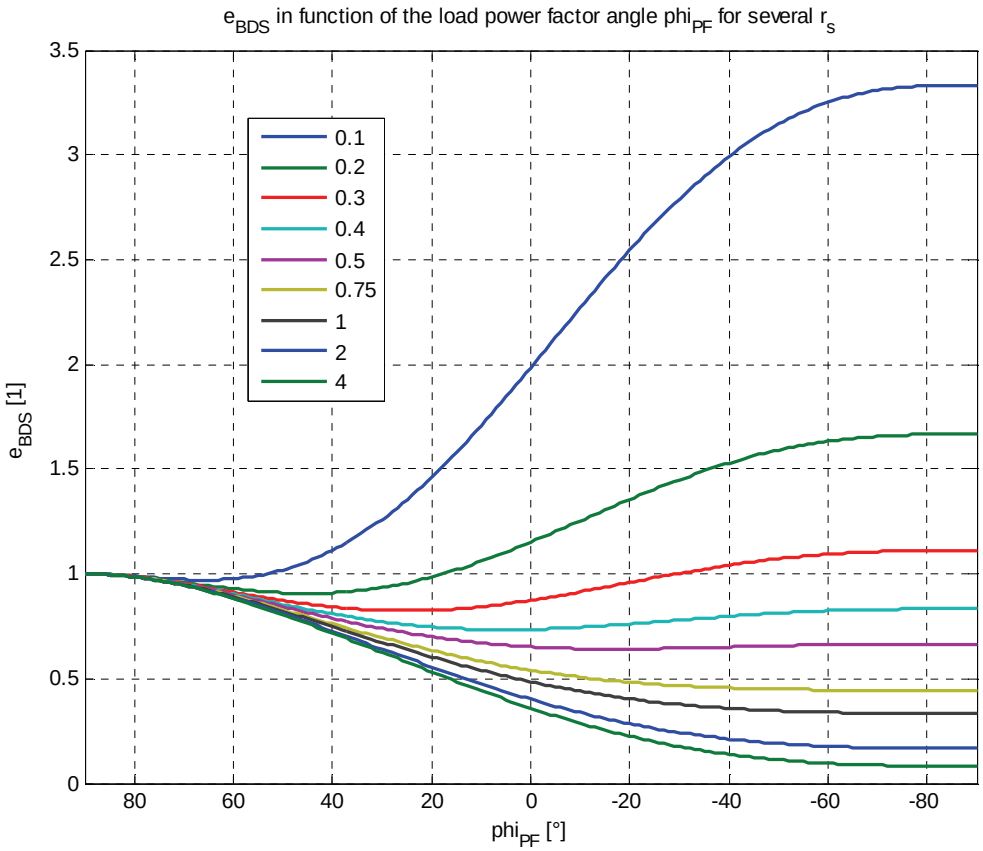


Fig. 3.32 – Relative switching losses when referred to full forced mode of PPMC

To conclude about the commutation losses of the PPMC, they have to be expressed relatively to the delivered output energy of the converter for one output period. This value is denoted by $e_{BDS/o}$ and is given by equation Equ. 3.31.

Equ. 3.31 $$E_o = 3T_o U_{nRMS} I_{oRMS} \cos(\varphi_{pf}) \qquad e_{BDS/o} = \frac{E_{BDS,full\ forced}}{E_o} = \boxed{\frac{\sin\left(\frac{\pi}{m}\right)}{\cos(\varphi_{pf})} \frac{t_{off}}{T_c}}$$

This rather simple expression is of course only an estimation that could suffer from the above mentioned assumption about t_{off} and t_{on}. It is used in this work only to have an idea about the order of magnitude of the commutation losses and to compare them with the conduction losses and, later, to the snubber losses. There are two components in the expression of $e_{BDS/o}$. First, the effect of input phase number. The more input phases, the smaller is ΔV is comparison with U_n and therefore the smaller the commutation losses.

Table 3.11 – PPMC efficiency drop due to switching losses in the BDS

m	6	9	12	15	18	21	24	27
$\sin(\pi/m)$ or $e_{BDS/o}$ with $t_{off}/T_c=1$ and pf=1	0.5	0.34	0.25	0.2	0.17	0.15	0.13	0.11

Table 3.11 gives simply the value of the first component for unity power factor. This would be the losses if the ratio t_{off}/T_c was equal to 1. The second component is the ratio of the commutation time t_{off} over the commutation period. Of course, when varying m, with similar frequency ratio, T_c also varies and direct comparison of $e_{BDS/o}$ for different input phase number must be made with caution here. The precise value of t_{off}/T_c is hard to determine here and is very related to the practical implementation of the converter. However, for a conversion of 100Hz to 50Hz with m=27, T_c=740µs. Assuming a possible value of 7µs for t_{off}, this gives $t_{off}/T_c \approx 0.01$. $e_{BDS/o}$ would then become about 0.1%. In another way round, Table 3.11 can be used to set requirement on the ratio t_{off}/T_c in order to guaranty a maximum value for the commutation losses. It can be concluded that for all m, commutation losses of the PPMC relative to the delivered output power will remain around 0.1%. From this, it can be concluded that the commutation losses are not a big issue for the PPMC topology.

3.9 The two stages topology

In this section, the ”two stages” topology of the PPMC will be briefly studied to determine the voltage constraints of the switches and the possible reduction in number of switches compared to the one stage topology. The two stages topology, with grouped generator phases, is described in [13] Fig. 3.33 shows this topology with thyristors, but the same circuit can be used for our PPMC with BDS. There are two benefits of using the two stages topology. First, it reduces the number of valves of the topology and hence the number of gating signals. This is straightforward when looking at Fig. 3.33.

The equations Equ. 3.33 and Equ. 3.32 give the expression of the number of required valves for the one stage and the two stages topology respectively.

Equ. 3.32
$$N_0 = 6m$$

Equ. 3.33
$$N_{2stages} = N_{1st} + N_{2nd} = 2m + 6m_{2nd}$$

where m_{2nd} is the number of phases in the second stage. From the *slowCWC* sequence, during normal operation of the PPMC, only three generator phases conduct the three-phase load currents so that there is always a distance m/3 between each of the three conducting generator phases. So the grouping suggested here above is perfectly possible, let’s say up to m/3 generator phases per group. This number will be named $n_{grouped}$ (number of generator phases per group, for the first stage).

$$n_{grouped} \leq \frac{m}{3} \quad and \quad m_{2nd} = \frac{m}{n_{grouped}} \geq 3$$

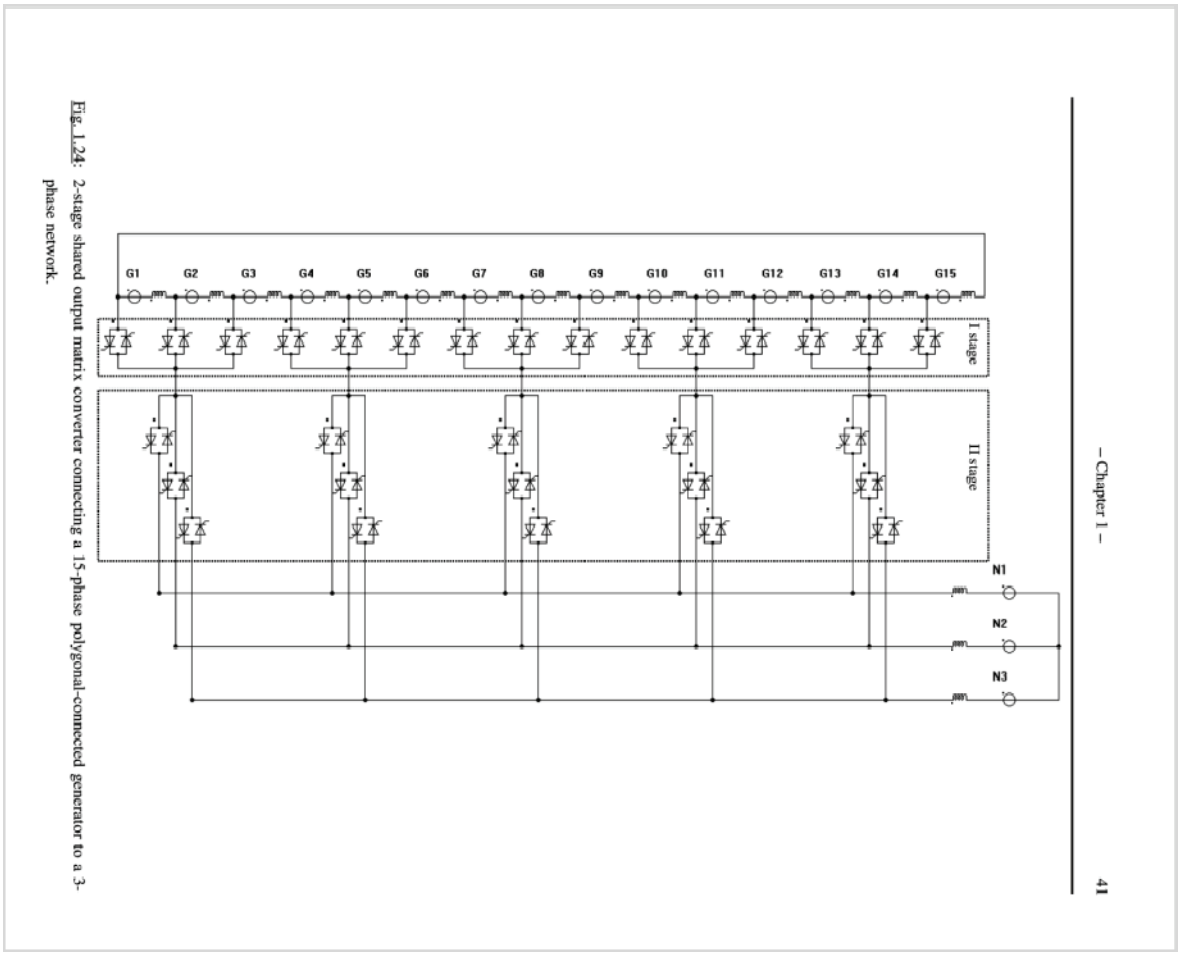


Fig. 3.33 – Schematic of the two stages topology applied to a NCMC (source [13])

The interest of grouping valves in the second stage compared to the full matrix topology is given by Equ. 3.33. Table 3.12 illustrates, with numerical examples, the potential of reduction of number of valves of the two stages topology.

Equ. 3.34

$$\frac{N_{2stages}}{N_0} = \frac{1}{3} + \frac{1}{n_{grouped}}$$

Table 3.12 – Reduction of number of valves from one stage to two stages topology

$n_{grouped}$	2	3	4	5	6	7	8	9
N_2/N_0	0.833	0.66	0.5833	0.533	0.5	0.476	0.45833	0.44
m_{min}	6	9	12	15	18	21	24	27
N_0 for m_{min}	36	54	72	90	108	126	144	162
N_2 for m_{min}	30	36	42	48	54	60	66	72

But the interest of the two stages topology effect is reinforced when analyzing the voltage constraint on the switch of each of both stages. Indeed, the two stages topology can reduce the voltage constraint on the valves. This effect is only interesting for high voltage applications where the valves

are constituted of the series connections of several switches of a given blocking voltage rating to meet the total voltage blocking requirement. For the one stage topology, the constraint on the valves is $2V_{N,grid}$. In normal operation of the two stages topology, this constraint can be reduced to $V_{n,grid}$ which is a considerable improvement. In practice, however, there are some abnormal operations where this constraint could go up to $2V_{N,grid}$. In this case there is no reduction of the voltage constraint with the two stages topology. The precise determination of the voltage constraint of the two stages topology is beyond the scope of the present work and is suggested as a perspective in chapter 7.

3.9.1 Application of two stages topology to the PPMC

Basically, it seems that the two stages topology should also be applicable to the PPMC running with the *slowCWC* sequence. When commutations are performed within a group of the first stage, the commutation cell is similar to the one stage topology and operation remains the same. For intergroup commutations, the synchronism of gating signals between the two stages is important in order to avoid abnormal voltage constraint ($>V_{N,grid}$). If the voltage constraint is already set to a worst case $2V_{N,grid}$, then this precise synchronism is not relevant anymore.

Mix valves principle with two stages topology

One drawback on the PPMC is that it requires transistor-based BDS valves. Is it the case for the two stages topology? Obviously, it is necessary that the valves of the first stage are BDS valves as described in first section of this chapter. But the valves of the second stage do not have to be totally turn-off capable. They do not need to be turn off but it is also not possible to build them out of thyristors since for a forced commutation case, it would be impossible to close the free-wheeling path because the thyristors would be reverse biased at that moment. As for high power applications the valves are build out of series and parallel connections of switches, one could build for the second stage a valve with a mix of thyristors and transistors in parallel. The transistor would only play the role of free-wheeling path for a short duration, until the thyristors in parallel are fired. This would only work if the voltage drop across the conducting transistors is high enough to forward bias the thyristors.

Chapter 4 – Design and properties of the snubber circuits

4.1 Introduction

In chapter 3, the necessity to add a protection and free-wheeling path across each generator stator phase is presented. The simple passive resistive-capacitive leg is chosen among possibilities and denoted as RC snubber. This chapter focuses on the design of this RC snubber and presents a simple design method based on algebraic equations describing the PPMC during three concomitant forced commutations. Those equations help assessing the losses that take place in the resistive component of the RC snubber. This is presented in the second part of this chapter. In a third part, other fee-wheeling path solutions are briefly assessed.

4.2 Design of RC snubber circuits

4.2.1 Transient response of three concomitant forced commutations

In order to simplify the study, the circuit will be reduced, according to a few assumptions, to an equivalent RLC circuit. From this simplified circuit, analytical formula for the design of the capacitive and resistive component will be found. It is assumed that there are three concomitant forced commutations because of the three output phases, which means that the PPMC is run is full forced mode. In chapter 2, it is shown that, if PPMC is run in mix mode, then there are some instants with two forced commutations and one natural commutation and other instants where there are two natural commutations and one forced commutation. Those cases will not be handled in this work. It is assumed that, in case of mix mode operation of the PPMC, the transient response of one forced commutation is not significantly affected by the type of the two other concomitant commutations on the other two output phases.

Equivalent circuit

It is assumed that there are always three commutations simultaneously, which is the case if the PPMC is operated in full forced mode. As can be seen the complete electrical circuit of the PPMC has many components and it would be a huge but not necessarily useful job to solve analytically the complete circuit in order to extract the expression of the voltage across the capacitor of the snubber, in order to design the value of C in function of the requirement. The symmetry property of the circuit is used to simplify it.

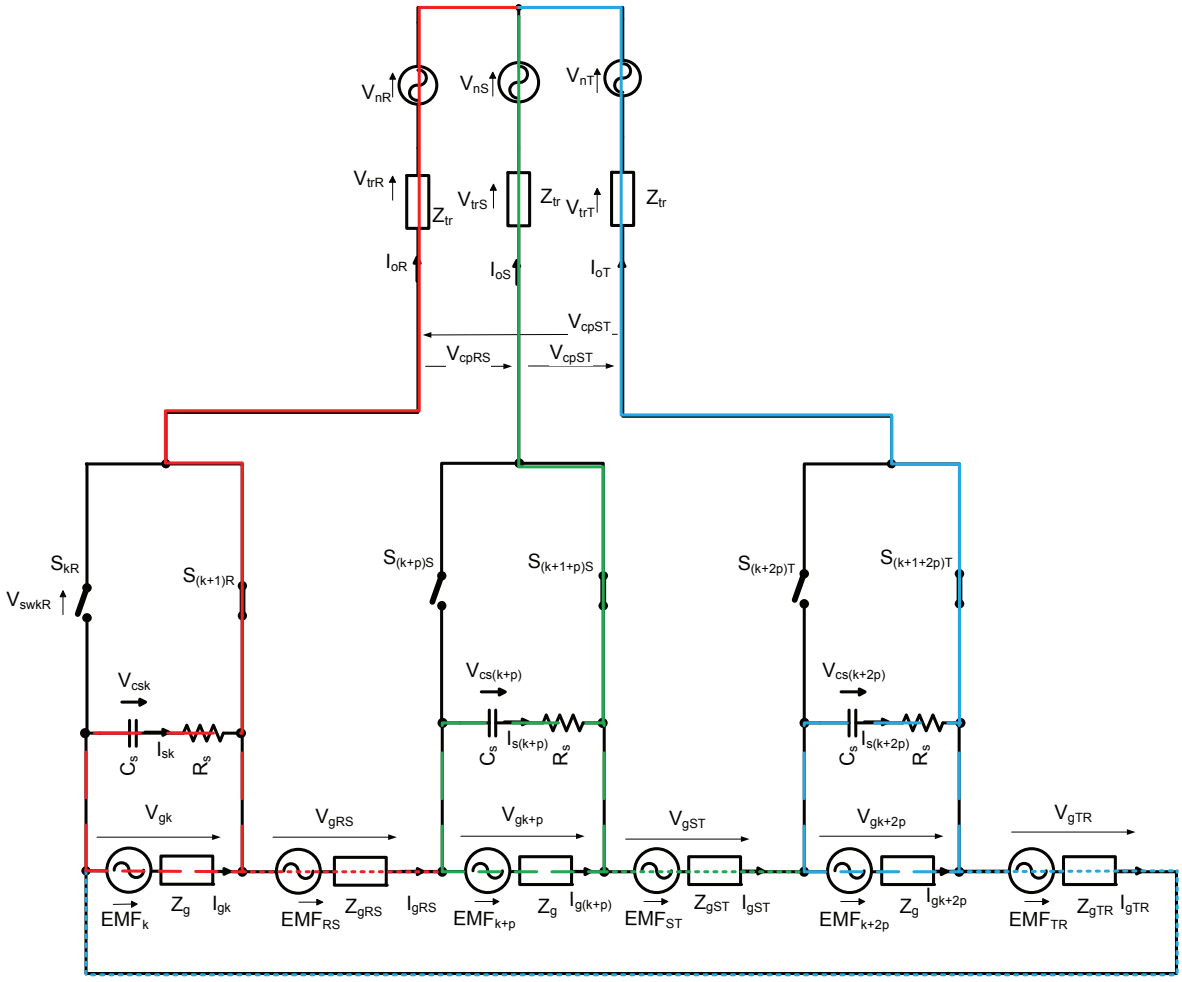


Fig. 4.1 – Simplified PPMC circuit for three concomitant forced commutations

The assumptions leading to this simplified circuit are:

- For each of the three output phases there is only one RC snubber involved in the commutation, the one between the two generator phases included in the commutation. This means that the current flowing into both the adjacent RC legs is negligible in comparison with the commutated current
- EMF and load current are DC. The load is replaced by three current DC sources. The assumption here is that the transient response studied is much faster than the period of the generator and load period, T_g and T_o resp.
- The switches are ideal. No voltage drop nor capacitive behaviour of the switches is involved into the commutations. Also, closure and aperture of SW_k and SW_{k+p} is simultaneous.
- Symmetrical initial conditions. The initial condition of the capacitor and inductor is assumed to be the values at steady state of the circuit. We assume that at the initial instant t_0, the converter is at steady state, which means that the last transient response is fully damped. The initial voltage across the three capacitors involved into the commutation are symmetrical, it means that their sum is null. Their initial value is defined as the value of the

corresponding EMF. U_{sck0}=EMF_k. This can be justified by the fact that in steady state, the voltage drop across L_g and R_g is negligible in front of EMF. Besides, the no load snubber current is small enough so that the voltage drop across R_s is negligible in front of EMF.

Clearly, all those assumptions can be discussed and are subject to contestations. But, for instance, the first development of the design procedure is based on the circuit of Fig. 4.1. This circuit is valid for any number of generator phase, *m,* with *m* being a multiple of 3 and *m*>3. Therefore, there are three loops with the three generator phases involved in the commutation. Those three loops are bound together by a leg that is an equivalent generator phase composed of (*m*-3)/3 series connection of generator phases. The parameters of this equivalent generator phase are given in Equ. 4.1 and Equ. 4.2.

Equ. 4.1
$$\boldsymbol{L_{gRS} = L_{gST} = L_{gTR} = \frac{(m-3)}{3} L_g = L_{gRST}}$$

Equ. 4.2 $\boldsymbol{\overrightarrow{EMF_{RS}} = \sum_{j=k+1}^{k+p-1} \overrightarrow{EMF_J}}$ $\boldsymbol{\overrightarrow{EMF_{ST}} = \sum_{j=k+p+1}^{k+2p-1} \overrightarrow{EMF_J}}$ $\boldsymbol{\overrightarrow{EMF_{TR}} = \sum_{j=k+2p+1}^{k+3p-1} \overrightarrow{EMF_J}}$

$$\boldsymbol{with\ p = \frac{m}{3}\ \ and\ \ j = j - m\ \ if\ j > m}$$

Solution of the circuit – capacitor voltage V_{sc}

With a quick glance at the circuit of Fig. 4.1, taking into account the assumptions made above, one could intuitively deduce that the three commutation loops have a transient response that is independent of each other. This is indeed the case and it is mathematically briefly shown in this paragraph. The Kirchhoff current and voltage equations are completed with the constitutive laws of each leg which leads to the following system of three second order differential equations where the unknown functions are the three capacitor voltages V_{sc}.

(Equ. 4.3)

$$\begin{cases} EMF_k + L_g \frac{C_s}{m}\left(\frac{d^2V_{sc(k+p)}}{dt^2} + \frac{d^2V_{sc(k+2p)}}{dt^2}\right) - L_g C_s \left(1 - \frac{1}{m}\right)\frac{d^2V_{sck}}{dt^2} - R_s C_s \frac{dV_{sck}}{dt} - U_{sck} = 0 \\ EMF_{(k+p)} + L_g \frac{C_s}{m}\left(\frac{d^2V_{sc(k)}}{dt^2} + \frac{d^2V_{sc(k+2p)}}{dt^2}\right) - L_g C_s \left(1 - \frac{1}{m}\right)\frac{d^2V_{sc(k+p)}}{dt^2} - R_s C_s \frac{dV_{sc(k+p)}}{dt} - U_{sc(k+p)} = 0 \\ EMF_{(k+2p)} + L_g \frac{C_s}{m}\left(\frac{d^2V_{sc(k)}}{dt^2} + \frac{d^2V_{sc(k+p)}}{dt^2}\right) - L_g C_s \left(1 - \frac{1}{m}\right)\frac{d^2V_{sc(k+2p)}}{dt^2} - R_s C_s \frac{dV_{sc(k+2p)}}{dt} - U_{sc(k+2p)} = 0 \end{cases}$$

In order to solve this system and find the solution of the differential equations, this system is transformed into the Laplace domain with the Laplace transform.

Equ. 4.4
$$\boldsymbol{\mathcal{L}\{V_{scj}\} = V_{scj}(s) \quad \mathcal{L}\left\{\frac{dV_{scj}}{dt}\right\} = sV_{scj}(s) - V_{scj0}}$$

Equ. 4.5
$$\boldsymbol{\mathcal{L}\left\{\frac{d^2V_{scj}}{dt^2}\right\} = s\left(sV_{scj}(s) - V_{scj0}\right) - \left.\frac{dV_{scj}}{dt}\right|_0 = s^2V_{scj}(s) - sV_{scj0} - \frac{I_{sj0}}{C_s}}$$

Where V_{scj0} is the initial voltage on the capacitor j and I_{sj0} the initial first derivative of V_{scj}, i.e. the initial current flowing through the capacitor. Those initial values are all known.

Solving this system gives

Equ. 4.6

$$\begin{cases} V_{sck}(s) = -\dfrac{D_{k0}}{-L_g C_s s^2 - R_s C_s s - 1} - \dfrac{EMF_k(s)}{-L_g C_s s^2 - R_s C_s s - 1} = 0 \\ V_{sc(k+p)}(s) = -\dfrac{D_{(k+p)0}}{-L_g C_s s^2 - R_s C_s s - 1} - \dfrac{EMF_{(k+p)}(s)}{-L_g C_s s^2 - R_s C_s s - 1} = 0 \\ V_{sc(k+2p)}(s) = -\dfrac{D_{(k+2p)0}}{-L_g C_s s^2 - R_s C_s s - 1} - \dfrac{EMF_{(k+2p)}(s)}{-L_g C_s s^2 - R_s C_s s - 1} = 0 \end{cases}$$

where the term D_{j0} is a constant that contain information about initial conditions related to the commutation cell *j* itself only. This result shows that the voltage response of each of the three capacitor voltages are independent of each other. So the circuit of the converter during a forced commutation can be reduced to three independent RLC circuits and the expression of the capacitor voltage V_{sc} is given by Equ. 4.7.

Equ. 4.7

$$\boldsymbol{V_{sck}(t) = EMF_k + e^{-\alpha t}\left((V_{sck0} - EMF_k)\cos\omega t + \left((V_{sck0} - EMF_k)\left(\frac{\alpha}{\omega}\right) + \frac{I_{sk0}}{\omega C_s}\right)\sin\omega t\right)}$$

Equ. 4.8

$$\boldsymbol{\alpha = \frac{R_s}{2L_g} \quad \frac{1}{L_g C_s} = \omega^2 + \alpha^2}$$

where α is the damping rate and ω the oscillation frequency of this second order response.

For the convenience of the next steps, the sine and cosine are merged into one cosine as given by Equ. 4.9.

Equ. 4.9

$$\boxed{\boldsymbol{V_{sck}(t) = EMF_k + A_{sck} e^{-\alpha t}\cos(\omega t - \varphi_{sc})}}$$

With

Equ. 4.10

$$\boldsymbol{A_{sck} = \sqrt{(V_{sck0} - EMF_k)^2 + \left((V_{sck0} - EMF_k)\left(\frac{\alpha}{\omega}\right) + \frac{I_{sk0}}{\omega C_s}\right)^2}}$$

Equ. 4.11

$$\boldsymbol{\varphi_{sck} = \tan^{-1}\left(\frac{\left((V_{sck0} - EMF_k)\left(\frac{\alpha}{\omega}\right) + \frac{I_{sk0}}{\omega C_s}\right)}{(V_{sck0} - EMF_k)}\right)}$$

4.2.2 The snubber overvoltage

In order to calculate the expression of the maximum voltage across the snubber leg, here are the main steps. Here the k index is dropped out in order to make the equations clearer. The voltage across the snubber leg (or across both BDS involved into the commutation) is given by Equ. 4.12.

Equ. 4.12

$$\boldsymbol{V_s = R_s I_s + V_{sc} = R_s C_s \frac{dV_{sc}}{dt} + V_{sc}}$$

Hence, V_s is given by Equ. 4.13

Equ. 4.13 $$\boxed{V_s = A_{sc}e^{-\alpha t}[\cos(\omega_a t - \varphi_{sc} - \varphi_s)] + EMF}$$

With

Equ. 4.14 $$\varphi_s = -\sin^{-1}(RC\omega_a)$$

However the maximum of V_s is the point of interest here. To find the maximum, the zeros of dV_s/dt are calculated which gives a collection of instants. Among those instants, the global maximum occurs at t_{max}. Then $V_s(t_{max})$ is expressed to find V_{sMax}. The first time derivative of Vs is given by Equ. **4.15**. The collection of local maximum instants is given by Equ. 4.18.

Equ. 4.15 $$\frac{dV_s}{dt} = -A_{sc}e^{-\alpha t}\left[\sqrt{\alpha^2 + \omega_a^2}\cos(\omega_a t - \varphi_{sc} - \varphi_s - \beta)\right]$$

Equ. 4.16 $$\beta = \tan^{-1}\left(\frac{\omega_a}{\alpha}\right)$$

Equ. 4.17 $$\frac{dV_s}{dt} = 0 \quad \Leftrightarrow \omega_a t - \varphi_{cs} - \varphi_s - \beta \ = \frac{\pi}{2} \pm k\pi$$

Equ. 4.18 $$\boxed{t_{max} = \frac{\varphi_{cs} + \varphi_s + \beta + \frac{\pi}{2} \pm k\pi}{\omega_a}}$$

with *k* any integer value. This expression gives a collection of time corresponding to local maximum of V_s. Equ. 4.19 gives V_{sMax} when the Equ. 4.18 is introduced in Equ. 4.13

Equ. 4.19 $$V_s(t_{max}) = EMF - A_{cs}e^{-\alpha\frac{\varphi_{sc} + \varphi_s + \beta + \frac{\pi}{2} \pm k\pi}{\omega_a}}[\sin(\beta \pm k\pi)]$$

Only the first peak with positive t_{max} corresponds to the global maximum of interest here. This will be developed in the next paragraph.

4.2.3 The relative snubber overvoltage

The p.u. system used from here is introduced in chapter 3. It is briefly repeated here.

Two references (base) values are defined in Equ. 4.20

Equ. 4.20 $$R_{base} = \frac{\Delta V_{peak}}{I_{o,peak}} \qquad C_{base} = L_g\left(\frac{I_{o,peak}}{\Delta V_{peak}}\right)^2 = \frac{L_g}{R_{base}^2}$$

which are the base resistance and the base capacitor. ΔV_{peak} is the peak voltage across the generator phase and according to the assumptions, it is then EMF_{peak} and $I_{o,peak}$ is the peak output current. From those base values, the p.u. snubber capacitor and resistor c_s and r_s are defined, as in Equ. 4.21.

Equ. 4.21

$$\boldsymbol{c_s = \frac{C_s}{C_{base}} \quad r_s = \frac{R_s}{R_{base}}}$$

Besides, the initial conditions, i.e. the initial capacitor voltage and the initial current of the inductor, depend on the position of the commutation along one output period T_o. Equ. **4.22** gives the expression of those initial conditions in function of the base values. The relation is a ratio for each, i.e. r_v, r_I and r_{sc0}.

Equ. 4.22

$$EMF = r_v \Delta V_{base} \quad I_{s0} = r_I I_{obase} \quad V_{sc0} = r_{sc0} EMF$$

Also, the classical damping ratio ς of a second order response is given by Equ. **4.23** and expressed in function of r_s and c_s

Equ. 4.23

$$\boldsymbol{\frac{\alpha}{\omega} = \frac{\varsigma}{\sqrt{1-\varsigma^2}} = \frac{1}{\sqrt{\frac{1}{\varsigma^2}-1}} \qquad \varsigma = \frac{r_s\sqrt{c_s}}{2}}$$

With the help of the p.u. system defined in chapter 3, the maximum peak voltage in function of the base voltage value, ΔV_{base} is derived and shown in Equ. 4.24.

Equ. 4.24

$$\boxed{\frac{V_s}{\Delta V_{\text{base}}} = v_s = a_{sc} e^{\left(-\frac{1}{\sqrt{\frac{1}{\varsigma^2}-1}}\varphi\right)} [\cos(\varphi - \varphi_{sc} - \varphi_s)] + r_v}$$

With

Equ. 4.25

$$a_{sc} = \sqrt{\left(r_v(r_{sc0}-1)\right)^2 + \left(\frac{1}{\sqrt{\frac{1}{\varsigma^2}-1}}\right)^2 \left(r_v(r_{sc0}-1) + 2\frac{r_I}{c_s r_s}\right)^2}$$

Equ. 4.26

$$\varphi_{sc} = \tan^{-1}\left(\frac{1}{\sqrt{\frac{1}{\varsigma^2}-1}}\left(1 + 2\frac{r_I}{c_s r_s r_v(r_{sc0}-1)}\right)\right)$$

Equ. 4.27

$$\varphi_s = -\sin^{-1}\left(2\varsigma\sqrt{1-\varsigma^2}\right)$$

For given initial conditions, v_s is obviously defined by the only choice of r_s and c_s. Similarly, the expression of V_{smax} can also be expressed in the p.u. system, as shown by Equ. 4.28.

Equ. 4.28

$$v_s(t_{max}) = v_{sMax} = 1 - a_{cs} e^{\left(-\frac{1}{\sqrt{\frac{1}{\varsigma^2}-1}}\varphi_{max}\right)} [\sin(\beta \pm k\pi)]$$

With

Equ. 4.29 $$\boldsymbol{\sin(\beta) = \sqrt{1 - \varsigma^2}}$$

and

Equ. 4.30 $$\boldsymbol{\varphi_{max} = \varphi_{cs} + \varphi_s + \beta + \frac{\pi}{2} \pm k\pi}$$

4.2.4 Optimal design of the snubber

The base case, i.e. $r_v=1$ and $r_I=1$ and $r_{sc0}=1$, is taken as a base for the design of the snubber. Consequences of this way of doing will be analysed in the next paragraphs. For this particular case, Equ. 4.25 and Equ. 4.26 are expressed and rewritten in Equ. 4.31 and Equ. 4.32 resp.

Equ. 4.31 $$a_{sc} = \frac{2}{c_s r_s}\sqrt{\frac{1}{\left(\frac{1}{\varsigma^2}-1\right)}} = \frac{1}{\sqrt{c_s}\varsigma}\sqrt{\frac{1}{\left(\frac{1}{\varsigma^2}-1\right)}} = \frac{1}{\sqrt{c_s}}\sqrt{\frac{1}{(1-\varsigma^2)}}$$

Equ. 4.32 $$\varphi_{sc} = \tan^{-1}(+\mathrm{Inf}) = \frac{\pi}{2}$$

In order to find φ_{max} and the correct value $k\pi$ that points to the first peak, an analysis of the slope of V_s is required as well as the knowledge of the numerical values of φ_s and β in order to spot a positive t_{max}. φ_s and β depends only on the damping ratio. From this analysis, a damping ratio ς up to 0.5 gives an initial positive derivative of V_s. For higher values of the damping ratio the first derivative is negative. This is due to the fact that the initial voltage drop across R_s becomes dominant as R_s is increased. Even if the current through the capacitor increases its voltage, the decrease of current, i.e. the voltage drop across the R_s, is dominant. Only the response with ς between 0 and 0.5 are now considered because the case where the voltage across R_s is responsible for the maximum of V_s seems not to be a clever design. From those observations, Equ. 4.33 gives the value of φ_{max} of Equ. 4.28.

Equ. 4.33 $$\varphi_{max} = (\varphi_s + \beta)$$

The final expression for v_{smax} becomes

Equ. 4.34 $$v_{SMax} = 1 + \frac{1}{\sqrt{c_s}}\, e^{\overbrace{\left(-\frac{1}{\sqrt{\frac{1}{\varsigma^2}-1}}(\varphi_s+\beta)\right)}^{exponential\ term}}$$

Equ. 4.34 shows that the maximum peak voltage depends on $\frac{1}{\sqrt{c_s}}$ and on the exponential term. This factor only depends on the damping ratio ς. So for any value of c_s, there is a ς that gives an optimized V_{smax}, i.e. for any c_s an optimized value of r_s can be found. Fig. 4.2 shows

the evolution of the exponential term in function of ς. It shows the value of ς that gives the minimum v_{smax}. Fig. 4.3 shows $v_{smax,opt}$ for a range of values of c_s and the corresponding optimal snubber resistance r_s.

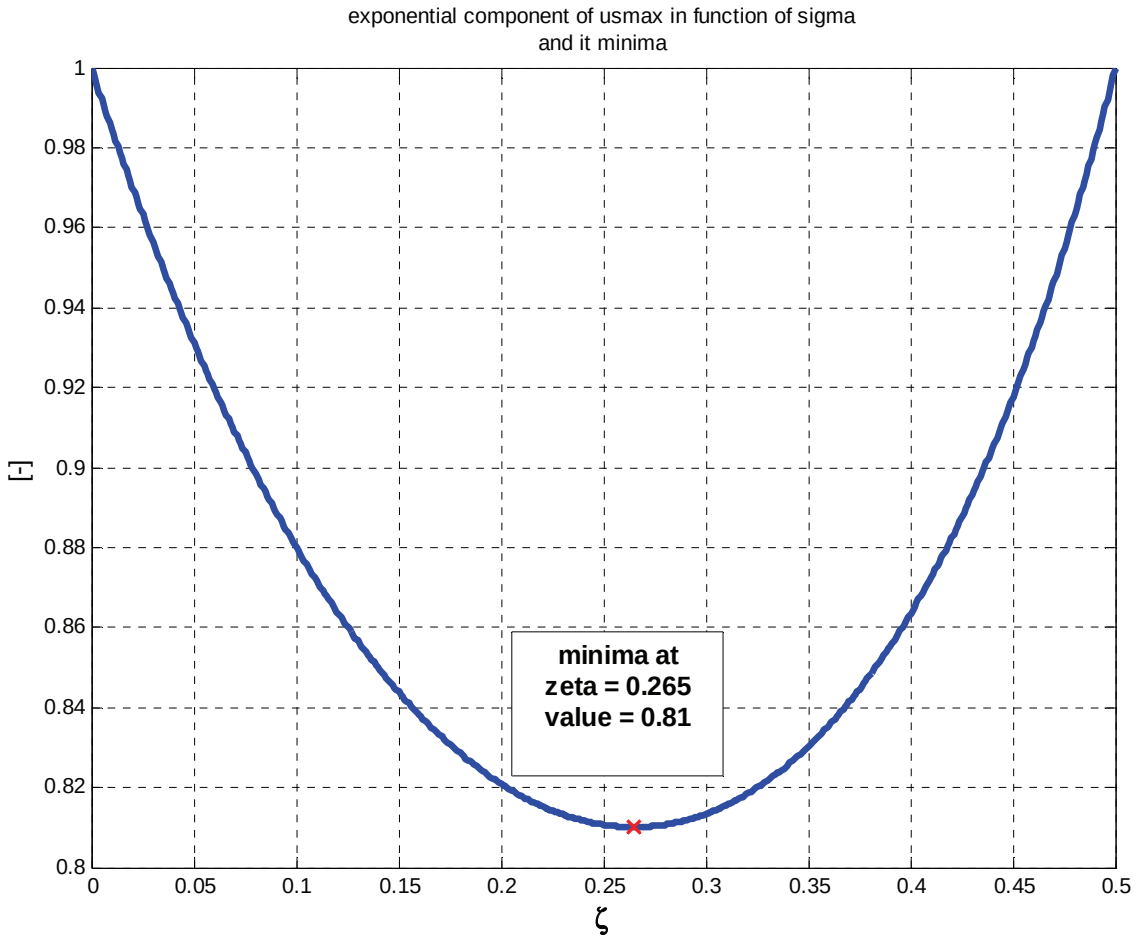


Fig. 4.2 – Exponential term of u_{smax} in function of the damping ratio ς

For a given capacitor, the best reduction of the snubber peak voltage is obtained for an optimum resistor R_{sOpt} which corresponds to a damping ratio zeta of 0.265. The reduction of the peak voltage compared to a case without resistor is about 19%. So the role of the resistor R_s in diminishing the peak is not very significant. However, the main role of R_s is to damp the oscillatory response in order to recover a steady state for the next commutation instant.

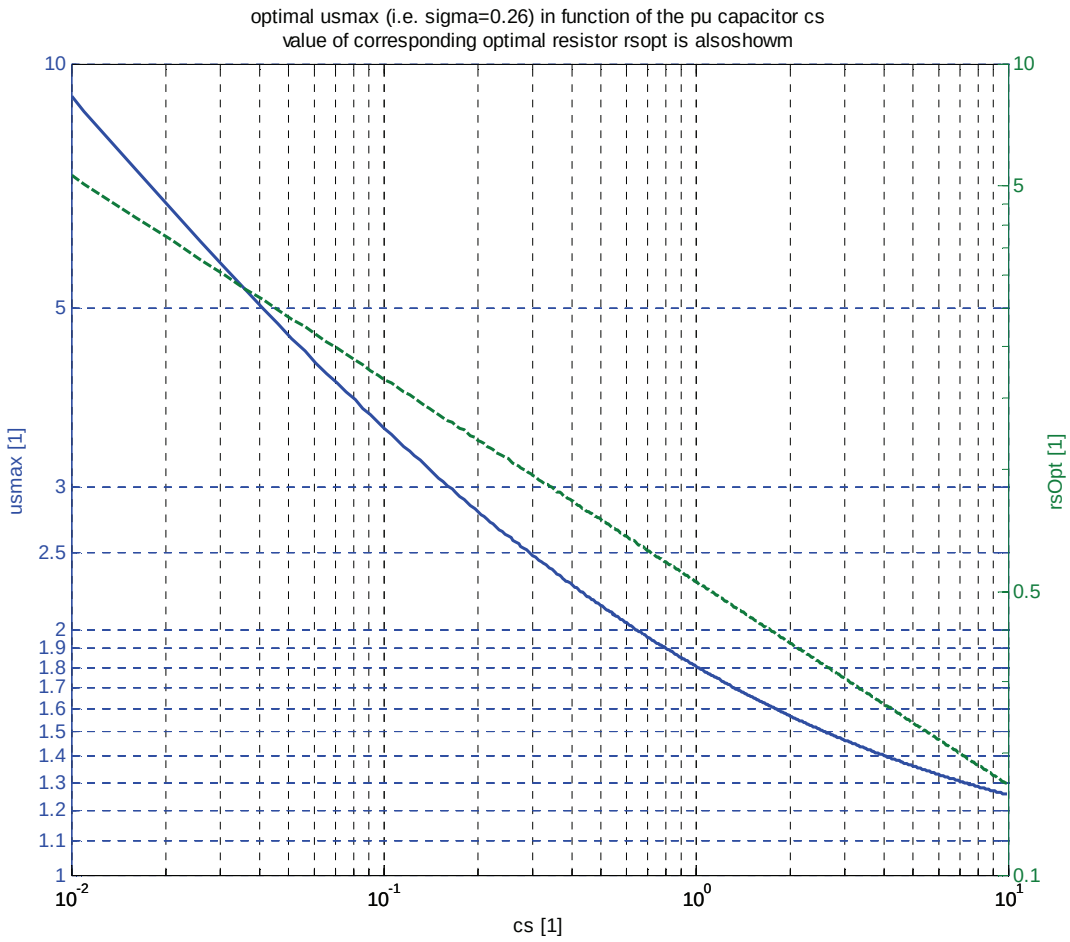


Fig. 4.3 – Snubber design abacus

The minimum necessary c_s in function of a given maximum peak value for V_s is directly given by this curve of Fig. 4.3. This figure is called "snubber design abacus". The base capacitance C_{base} (i.e. c_s=1) would lead to a maximum peak snubber voltage of 1.8p.u. and requires a r_s of about 0.5. For example a peak voltage constraint of 2p.u. would require a c_s of 0.65. The constraint to impose on v_{smax} is not discussed here and depends of the topology. It is discussed in section 4.6.2.

4.2.5 Effective snubber overvoltage

The previous section showed the derivation of the peak snubber voltage for a forced commutation occurring at initial conditions with $\Delta V=EMF_{peak}$ and $I_o=I_{o,peak}$. This is the base or nominal case. When looking at the figure 2.14 in chapter 2, which shows the available driving voltage ΔV in function of the target output voltage along with the target output current, it is clear that this base case only occurs for a null power leading factor, i.e. when the current leads the output converter voltage by $\frac{\pi}{2}$. When the output current lags the converter output voltage by $\frac{\pi}{2}$, this extreme case is also met but ΔV and I_o have opposite sign, hence the peak voltage corresponds to a voltage decrease across the involved generator coil and not an overvoltage. It can be reasonably assumed that the converter will run more often with a power factor in the range of -0.86 to 0.86 (in generator mode) so that the base case developed above for snubber design will scarcely be met. It is then necessary to assess what is the

effective maximum peak voltage that the generator coil will see for a given power factor and a nominal optimal snubber design. For any set of initial conditions, according to the Equ. 4.22 v_{smax} can be expressed as:

Equ. 4.35
$$\boldsymbol{u_{sMax}(r_v, r_I) = r_v + \frac{r_I}{\sqrt{c_s}} e^{\left(-\frac{1}{\sqrt{\frac{1}{\varsigma^2}-1}} \varphi_{max} \right)}}$$

Equ. 4.35 shows clearly the contribution of the initial current to the peak voltage. This is proportional to r_I . Depending on the commutation position φ_c and the power factor φ_{PF}, the ratios r_v and r_I are linked and vary in a sinusoidal manner, as Equ. 4.36.

Equ. 4.36
$$\boldsymbol{r_v = \cos(\varphi_c) \quad and \quad r_I = \sin(\varphi_c + \varphi_{pf})}$$

if the target output voltage V_{cR} is proportional to $\sin(\varphi_c)$ and with φ_{PF} negative when output current lags output voltage. Introducing these relations into Equ. 4.35 gives the effective snubber peak voltage for each commutation position.

Equ. 4.37
$$\boldsymbol{u_{s,peak}(\varphi_c) = \cos(\varphi_c) + \sin(\varphi_c + \varphi_{PF}) \frac{1}{\sqrt{c_s}} \overbrace{e^{\left(-\frac{1}{\sqrt{\frac{1}{\varsigma^2}-1}} \varphi_{max} \right)}}^{E}}$$

In Equ. 4.37 the same exponential term as in the base case appears. It is denoted by *E* here. *E* is modulated by the values r_I and r_v.

Equ. 4.38
$$\boldsymbol{u_{s,Max,effective} = max\left(u_{s,peak}(\varphi_c)\right) = max(\cos(\varphi_c) + \mathbf{E} \cdot \sin(\varphi_c + \varphi_{PF}))}$$

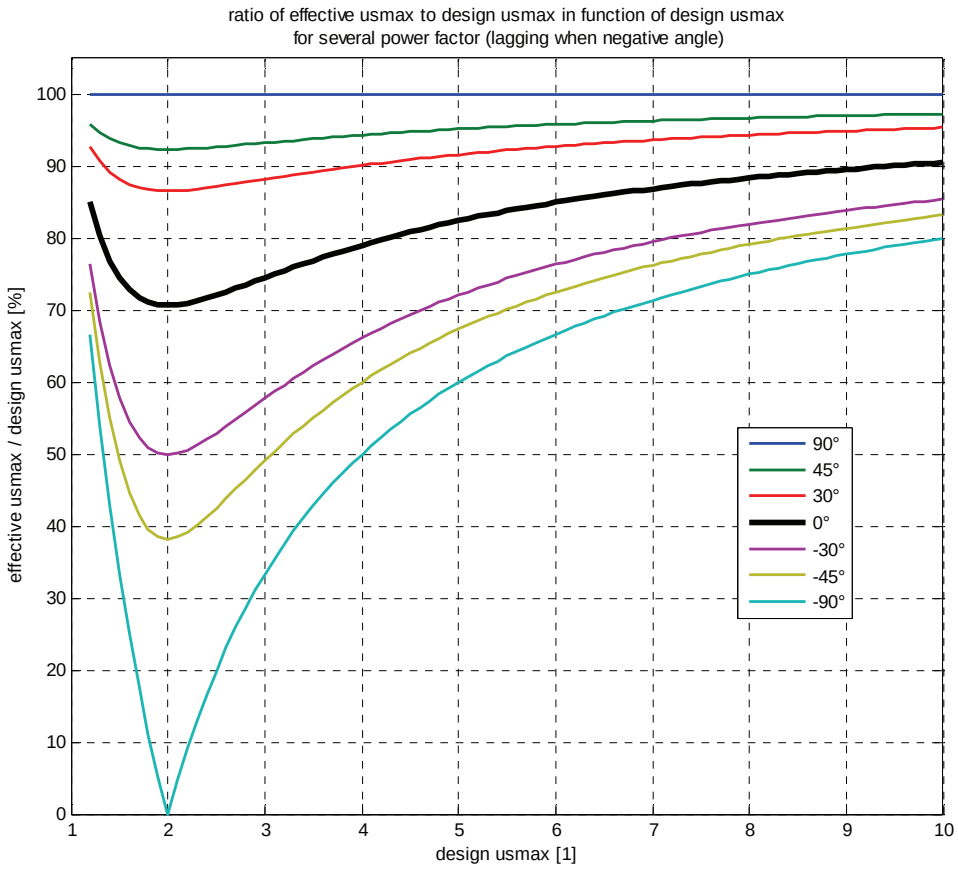


Fig. 4.4 – Effective maximum snubber voltage in function of design and operating point

Fig. 4.4 shows the effective maximum snubber voltage (Equ. 4.38) in function of the design value of maximum snubber voltage. The design is based on the base case where maximum EMF is in phase with maximum current. This only occurs for operating point PF=0 leading. When the power factor increases towards 1 and then decrease again in the lagging domain, the situation goes away from the worst case. It means that the effective maximum snubber voltage v_{smax} is smaller than the one set by the design. This tendency can be observed in general in the Fig. 4.4, for all values of design v_{smax}. Besides another effect is observed, that is the drastic decreasing of effective $v_{smaxeffective}$ around design v_{smax} =2 for all power factor, especially for lagging power factor. This is an artefact related to the definition of over voltage here. There are commutations were the sign of the current and the EMF are opposite, the peak voltage of the transient regime then effectively decrease the voltage across the snubber. If design v_{smax} is too small, this decrease is not important, if the design v_{smax} is too big the voltage across the snubber reverse its sign and become again an overvoltage but in any case never overpass the design value. In the extreme case of PF=0 lagging, the design value of 2 is so that the peak value of all overvoltage is always null, because the transient response always compensate EMF at its peak value. So the design of the snubber based on the base case leads to an over protection. It is interesting to quantify in term of over capacitance to measure the"cost" of this design method. Fig. 4.5 precisely quantifies the additional installed capacitance due to the base case design method. With this method, to a given design maximum snubber voltage v_{smax}, corresponds a capacitance to install in the snubber. Fig. 4.5 states how much bigger this capacitance is compared to the one that could be installed with the same protective effect. This depends of course on the power

factor of the output. For a null leading power factor this over capacitance is obviously null. From Fig. 4.5, one can conclude that for usual power factor angle (-30° to 30°), the over capacitance is not significant and are anyway comparable to the tolerance and the security factor that would appear in a practical design of the snubber. Therefore, the base case design method is declared to be suitable.

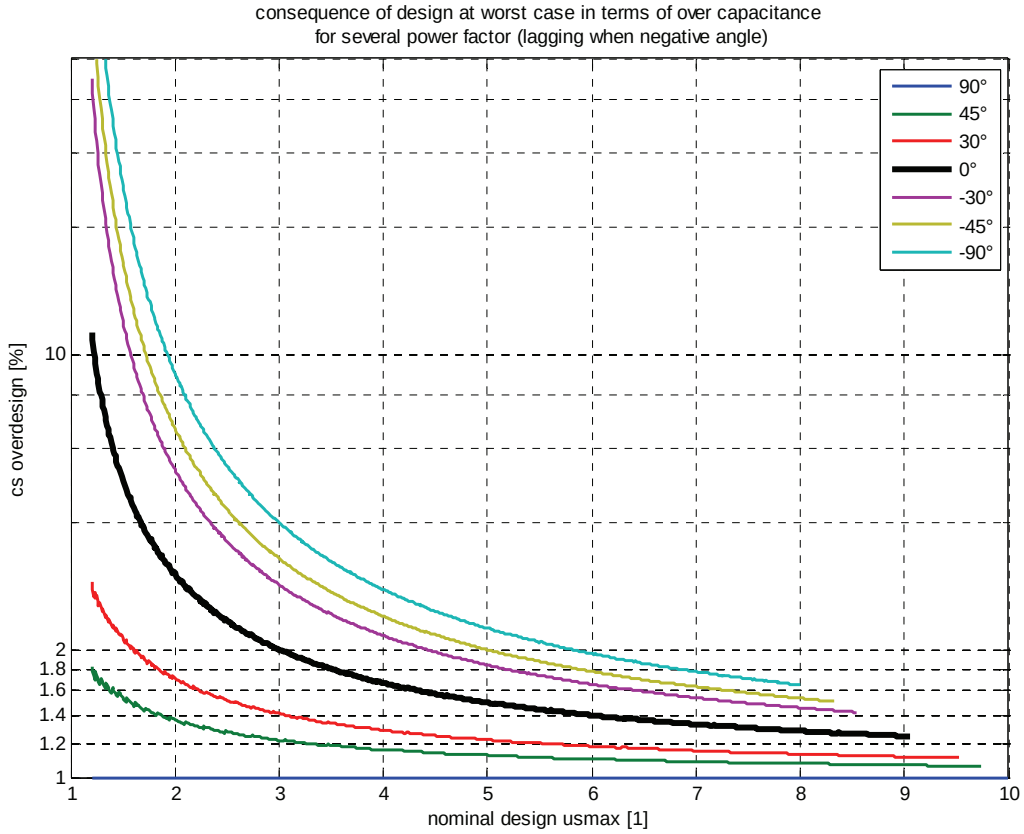


Fig. 4.5 – Consequence on installed snubber capacitor of the base design method

4.2.6 Damping time constraints

As said previously, it is wished that the transient regime induced by a forced commutation is damped as quickly as possible or at least before the next commutation occurs in order to have an output voltage that is controllable. If this is not the case, the assumption made above for the snubber design are not valid, especially the assumption about the initial condition on C_s. It is also wished that this transient response is damped as soon as possible in order to decrease the additional distortions of the output voltage. This means that there is a constraint on a minimum value of R_s for a given damping time and given damping level. In a first time, this issue is developed on the transient response of the worst case, i.e. r_v=1 and r_i=1. The damping of the oscillatory (or free) response of the regime is given by Equ. 4.39.

Equ. 4.39 $$a_{sc}e^{-\alpha t}$$

A value must be specified that acts as a threshold under which the free response is considered damped enough. As Equ. 4.39 is already in p.u., an example would be that the free response is considered damped when its value is below 0.05 p.u. From this, it is possible to deduce the time

when the free response is set under this threshold, which is the settling time t_s. t_s depends on the damping rate α. This parameter cannot only be expressed in term of non-dimensional characteristic of the circuit. However Equ. 4.42 shows that t_s is inversely proportional to a parameter α_{base}. So computation of t_s with α_{base}=1, base settling time t_{sbase} is shown in Fig. 4.6 and Fig. 4.7. For computation of the real t_s for a given application, simply divide t_{sbase} by the value α_{base}.

Equ. 4.40

$$\alpha_{base} = \frac{1}{2C_{base}R_{base}} \qquad \alpha = \frac{R_s}{R_{base}}\alpha_{base} = r_s\alpha_{base}$$

Equ. 4.41

$$\boldsymbol{a_{sc}e^{-\alpha t_s} = \frac{x_s\%}{100}}$$

Equ. 4.42

$$\boldsymbol{t_s = -\frac{\ln\left(\frac{\left(\frac{x_s\%}{100}\right)}{a_{sc}}\right)}{\alpha} = -\frac{\ln\left(\frac{\left(\frac{x_s\%}{100}\right)}{a_{sc}}\right)}{r_s\alpha_{base}} = -\frac{\ln\left(\frac{\left(\frac{x_s\%}{100}\right)}{a_{sc}}\right)\sqrt{c_s}}{2\varsigma\alpha_{base}} = -\frac{\ln\left(\frac{\left(\frac{x_s\%}{100}\right)}{\left(\frac{1}{\sqrt{c_s}}\sqrt{\frac{1}{(1-\varsigma^2)}}\right)}\right)\sqrt{c_s}}{2\varsigma\alpha_{base}}}$$

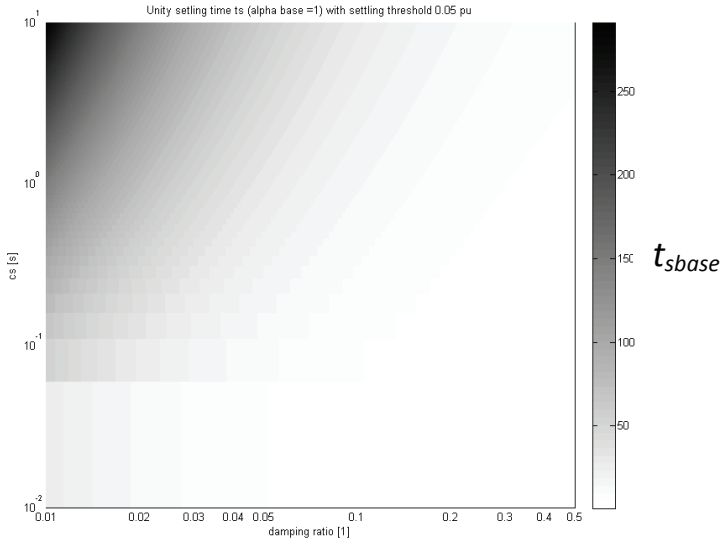


Fig. 4.6 – Base settling time (5%) of the transient response of a forced commutation

Fig. 4.6 shows the general map of t_{sbase} in function of the snubber capacitor c_s and in function of the damping ratio ς. Of course, t_{sbase} increases drastically for low damping ratio. The following Fig. 4.7 is more useful. It shows t_{sbase} in function of the damping ratio for a few values of c_s. By knowing C_{base} and R_{base}, one can directly estimate ts for a given damping ratio and compare with its requirement $T_c = \frac{1}{m(F_g - F_0)}$

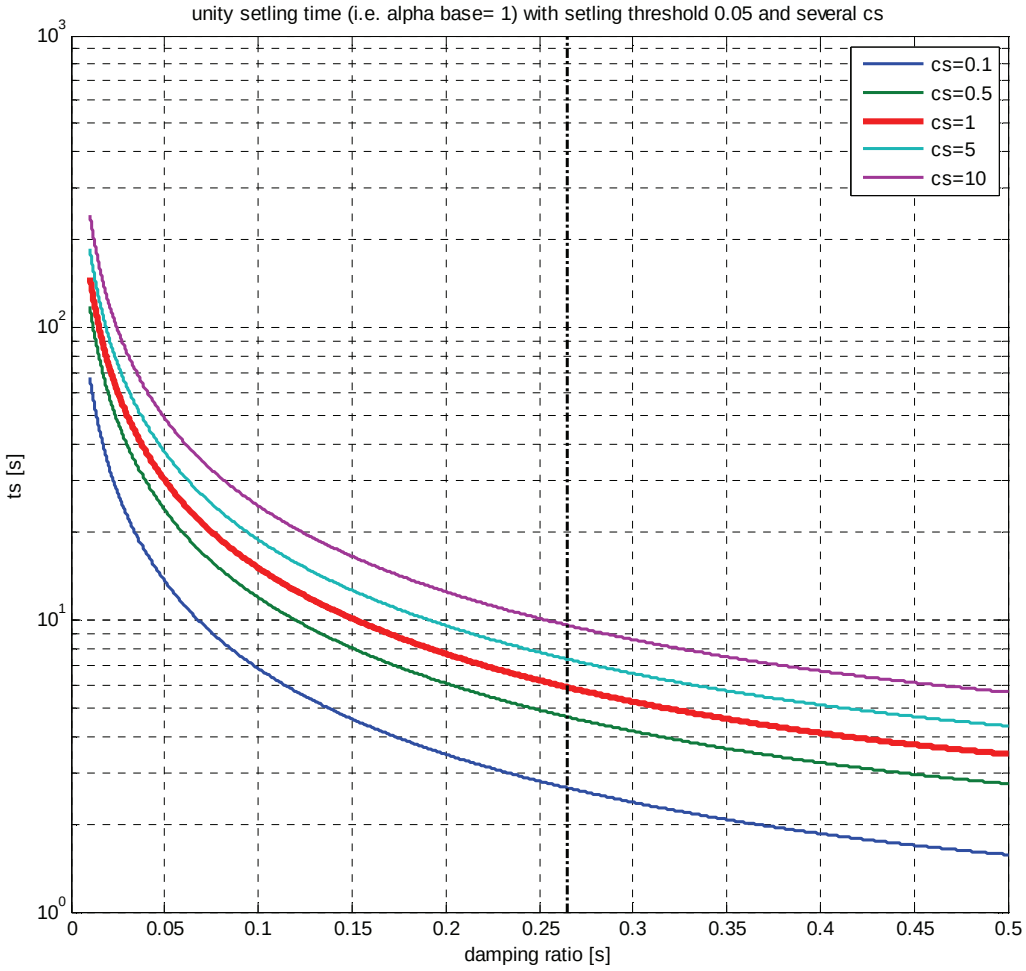


Fig. 4.7 – Base settling time (5%) in function of the damping ratio for several snubber design

4.3 The effect of the forced commutations at the output of converter

The converter line to line output voltage during a three concomitant forced commutations transient response is given by Equ. 4.43.

Equ. 4.43
$$V_{cRS} = EMF_{RS} + L_{gRST}\frac{dI_{gRS}}{dt} + V_{sc(k+p)}$$

According to the electrical circuit of Fig. 4.1. $\frac{dI_{gRS}}{dt}$ is still to be determined. The detailed development are not given here but it can be found that $\frac{dI_{gRS}}{dt}$ is null, similarly for $\frac{dI_{gST}}{dt}$ and $\frac{dI_{gTR}}{dt}$. Hence Equ. 4.43 becomes Equ. 4.44.

Equ. 4.44
$$V_{cRS} = \left|\sum_{j=k+1}^{k+p-1}\overrightarrow{EMF_J}\right| + V_{sc(k+p)}$$

The peak value of V_{cRS}, in the p.u. system is given by Equ. 4.45.

Equ. 4.45

$$v_{cRSMax} = 1 + 2\sin\left(\frac{\pi}{m}\right)\frac{1}{\sqrt{c_s}}e^{\left(-\frac{1}{\sqrt{\frac{1}{\varsigma^2}-1}}\varphi_{max}\right)}$$

where 1 p.u. corresponds to the peak value of the line output voltage applied to the load by the converter, i.e. $\left|\sum_{j=k}^{k+p-1}\overrightarrow{EMF_j}\right|$. From this formula, we clearly see the effect of the polygonal connection . An overvoltage on the generator side is repercuted with the factor $2\sin\left(\frac{\pi}{m}\right)$ on the converter output line voltage. Fig. 4.8 illustrates v_{rsMax} in function of optimal snubber design and for several input phases number (*m*).

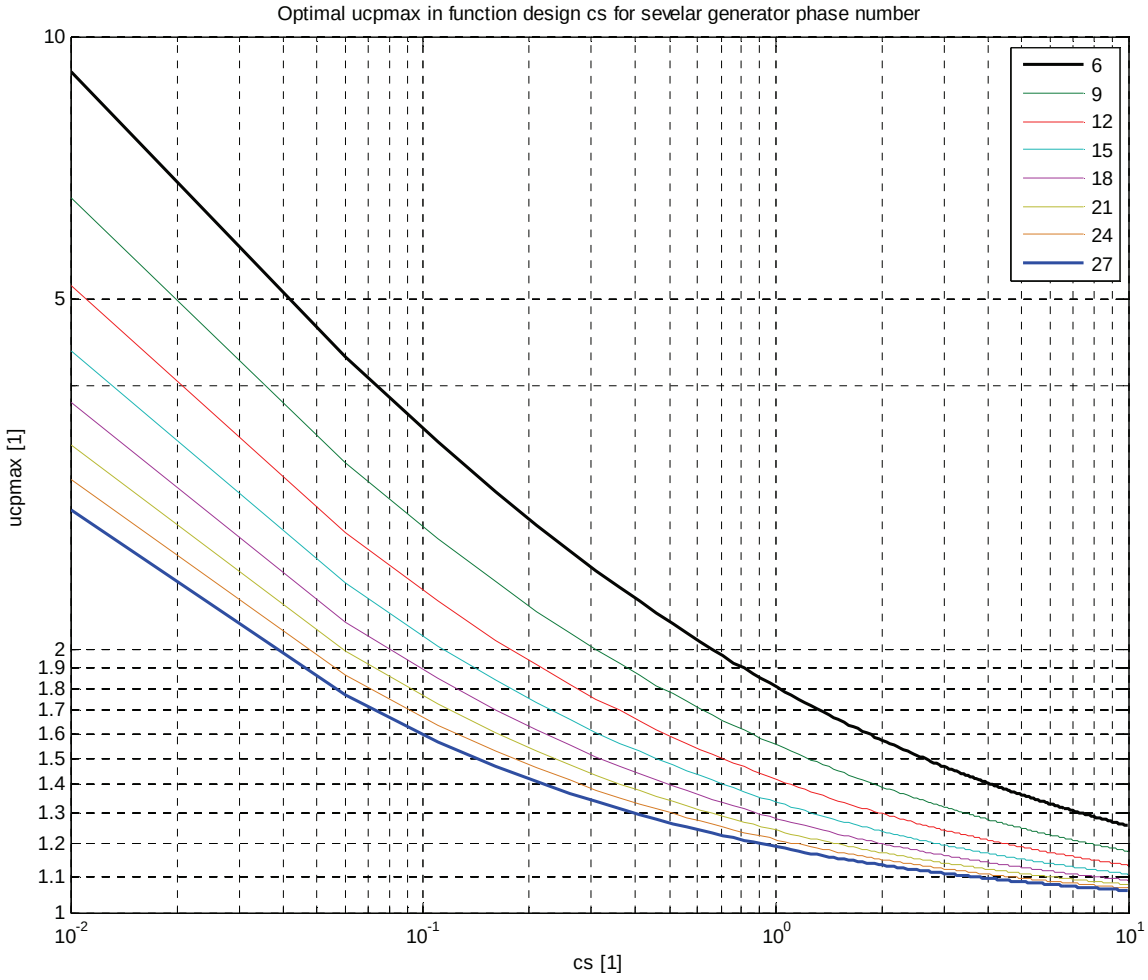


Fig. 4.8 – Converter peak output line voltage in function of optimal snubber design and for several *m*

The same analysis as section 4.2.5 (effective maximum) can be done here but is not performed since it would not bring much new information about snubber design.

4.4 Evaluation of the dimensions of snubber capacitors

The evaluation of the weight and volumes that the snubber capacitor and resistor would represent for a real installation of case 1 or case 2 is briefly approached in this section to give an insight. However, per unit analysis to expand results to other cases is not performed here since it requires knowledge about behaviour of volume specific capacitance in function of the capacitance, the voltage rating and current rating of the capacitor. This is complex and depends on the technology which is used to build the capacitors. This is beyond the scope of this work. For this section, only a few capacitors have been selected in a data base to give the order of magnitude. This section does not gives design rules of the capacitors. There are three main requirements that must be met by the physical capacitor: voltage rating, current rating (rms), peak current or maximum dV/dt, and meet the required capacitance value. The voltage rating constraint, the peak current constraint as well as the capacitance value, are straightforwardly deduced from the developments of this chapter. The current rms constraints is not developed in this chapter.

Table 4.1 – Snubber capacitor requirements

Target Capacitance per phase [mF]	0.2
RMS voltage [kV]	4
Max voltage [kV]	13.2
RMS current [kA]	0.4
Max current [kA]	12
Number of snubber	27

The capacitor samples presented here do not match any of those constraints. In fact it is hard to find a unique component that matches the requirements of case 1. It is therefore necessary to build the needed capacitor with series and parallel connections of discrete elements. In terms of volume specific capacitance (m^3/F), the series connection to reach the voltage requirement is a killer because it multiplies the volume specific capacitance by the square of the number of series connection. The paralleling of capacitor does not affect the volume specific capacitance of the paralleled elements. The reasoning is similar for the weight specific capacitance (Kg/F). The three capacitor samples are presented in Table 4.2. The rated voltage is particularly low compared to the requirements, but they are standard available products.

Table 4.2 – Capacitor samples specifications

	Technology	C [mF]	rated V RMS [kV]	rated rms current[kA]	peak current [kA]	Volume specific [m^3/mF]	weight [kg]
1	Plastic film	0.2	0.48	0.05	2.8	0.0022	1.7
2	Plastic film	0.005	3.4	0.12	7	0.172	3.2
3	Plastic film	0.02	2.1	0.12	8	0.043	3.2

Table 4.3 – Total dimension of capacitor snubber from samples of Table 4.2

	Series / parallel for voltage/current rating		Elements per phase	Total volume for 1 Phase [m^3]	Total volume for m Phase [m^3]	specific capacitance [m^3/mF]	Total number of elements	Total weight [kg]
1	20	1	400	0.178	4.82	0.9	10800	18360
2	3	40	360	0.309	8.35	1.5	9720	31104
3	5	10	250	0.215	5.80	1.1	6750	21600

Table 4.3 shows the details of the determination of the total volume and weight of the capacitors for the snubber made from series and parallel connection of capacitors of Table 4.2.

Table 4.3 does not specify parallel connections to meet the current rating requirements since the parallel connection to meet the capacitance ensures correct current ratings. In

Table 4.3 one can see the dramatic effect of the parallel connection on the volume specific capacitance. It can be conclude that this way of building the required capacitors for the PPMC of case 1 is not suitable and lead to non feasible capacitor weight whereas the total volume could still be feasible however the connections of the snubber would not be very close to the generator stator and the inductive component of the necessary cables would probably raise serious issues. Further research of capacitor with higher voltage rating is necessary to find a more feasible solution for the snubber. Practical issue of equilibrium of voltage sharing among the capacitor chains should also be addressed. The evaluation of the volume required by the resistors Rs should also be done.

4.5 Energy and efficiency considerations

4.5.1 Relative no-load snubber current

Due to the presence of the RC snubbers, the generator is permanently connected to a capacitive load. The reactive current flowing in the generator at no load (converter in off state) should be limited to reasonable value, which limits the capacitor value to a maximum. Fig. 4.9 shows the circuit of the generator (polygonal connection) connected to the *m* RC snubbers, at no load. The steady state solution of this circuit, with the hypothesis of symmetry of the EMF voltage system and impedances, leads to the expression of the current flowing through the generator in function of the generator's EMF and the circuit impedances, as shown in Equ. 4.46 and Equ. 4.47 where Z_g is the impedance of one generator phase, Z_s the snubber impedance and Z_L a possible connection line impedance, which will be neglected in the following developments.

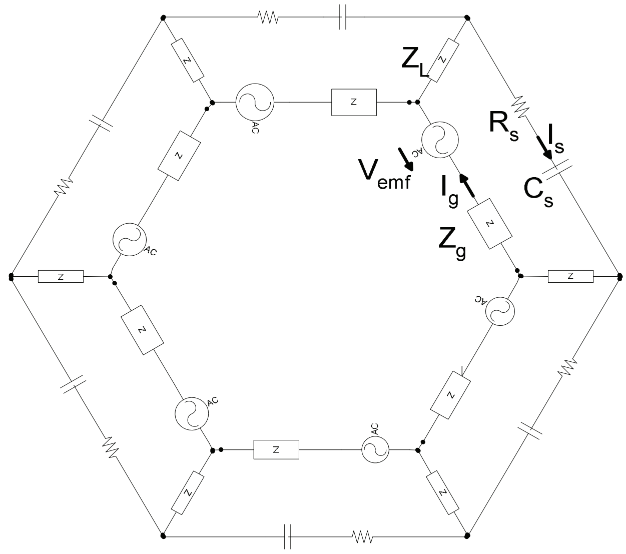


Fig. 4.9 - Calculation of no load generator current due to the RC snubber

Equ. 4.46
$$\vec{I}_g = \vec{I}_s$$

Equ. 4.47
$$\vec{I}_g = \frac{\vec{V}_{emf}}{\left[2\left(1-\cos\left(\frac{2\pi}{m}\right)\right)\vec{Z}_L+\vec{Z}_g+\vec{Z}_s\right]} \cong \frac{\vec{V}_{emf}}{\vec{Z}_g+\vec{Z}_s}$$

The reactance X_s of the snubber impedance Z_s can be expressed in function of the nominal impedance $Z_{N.grid}$

Equ. 4.48
$$X_s = \frac{1}{\omega_g c_s C_{base}} = \frac{i_{short}}{x_g c_s} 2\sin\left(\frac{\pi}{m}\right) Z_{N,3}$$

The snubber impedance Z_s can also be expressed in function of $Z_{N,grid}$. As seen in section 4.2.4, the relation between rs and cs is fixed for an optimal design. This ratio is ς. Finally, the snubber impedance becomes

Equ. 4.49
$$\underline{Z_s} = 2\sin\left(\frac{\pi}{m}\right) Z_{N,3}\left(\frac{2\varsigma}{\sqrt{c_s}} - j\frac{i_{short}}{x_g c_s}\right)$$

Z_g can also be expressed in function of $Z_{N,grid}$

Equ. 4.50
$$\underline{Z_g} = \frac{2\sin\left(\frac{\pi}{m}\right)Z_{N,grid}}{i_{short}}\left(r_g + jx_g\right)$$

The total no-load impedance Z_{noLoad} is

Equ. 4.51
$$\underline{Z}_{noLoad} = Z_g + Z_s = 2\sin\left(\frac{\pi}{m}\right) Z_{N,3}\left(\left(\frac{2\varsigma}{\sqrt{c_s}} + \frac{r_g}{i_{short}}\right) + j\left(\frac{x_g}{i_{short}} - \frac{i_{short}}{x_g c_s}\right)\right)$$

With the fact that $x_g \approx 1$, i_{short} is in the range [2:20], c_s is in the range [0.1:2] and $r_g<0.01$, the principal components of Z_{noLoad} are given by R_s and C_s. The snubber design will then have a direct influence on

the no load current. Given the relation between $V_{N,gen}$ and $V_{N,grid}$ (see in chapter 3), the no load current I_{noLoad} flowing through the generator or the snubber is given by Equ. 4.52.

Equ. 4.52

$$\frac{\boldsymbol{I_{noLoad}}}{\boldsymbol{I_{N,grid}}} = \boldsymbol{i_{noLoad}} = \left\| \left(\frac{2\varsigma}{\sqrt{c_s}} + \frac{r_g}{i_{short}} \right) + \boldsymbol{j} \left(\frac{x_g}{i_{short}} - \frac{i_{short}}{x_g c_s} \right) \right\|$$

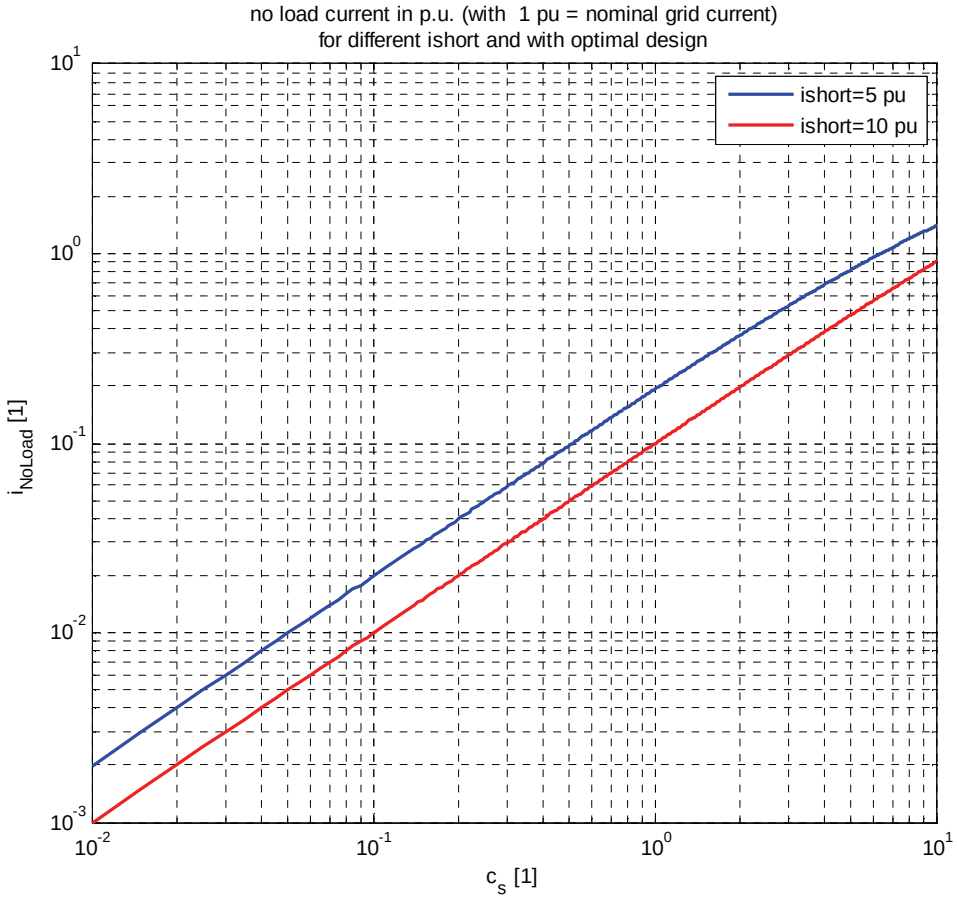


Fig. 4.10 – No load current in p.u. for several snubber design

Fig. 4.10 represents i_{noLoad}, the per unit magnitude of the no load current, in function of the optimal snubber design (ς=*0.265*) and for two generator parameters. The value i_{noLoad} is not significantly influenced by the value of ς. Even if ς is set to its maximum value of 0.5, this does not have a significant influence on the no load current magnitude, i.e. the resistor R_s cannot be used to increase the no load impedance if it is wished to stay within the maximum value of ς. From Fig. 4.10, it can be conclude that for most snubber design, the no load current is kept within reasonable margin, generally below 0.1 p.u. of the nominal load current $I_{N,grid}$. For snubber design with c_s greater than 1, the no load current takes a critical value and particular attention and consideration should be paid if such designs are required. However, it is not sufficient to have the magnitude of i_{noLoad} to say if most snubber designs are acceptable. It is necessary to extract the active and reactive part of this no load current. The next paragraph about no load input properties handles this.

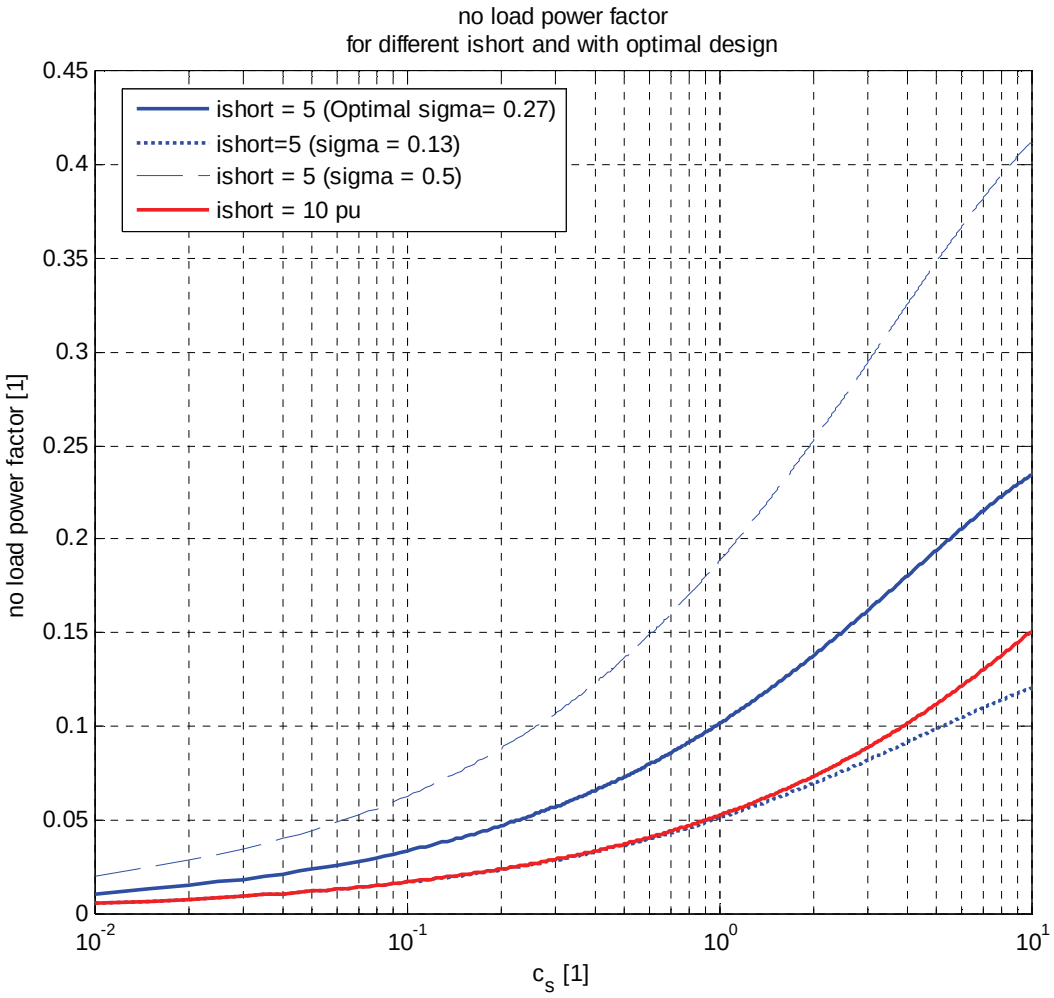


Fig. 4.11 – No load power factor

4.5.2 No load input properties

Fig. 4.11 shows precisely the no load power factor in function of the optimal snubber design and for two generator i_{short} parameters. Globally, the no load current is mostly reactive and for usual snubber design the power factor does not go beyond 0.1. However, particular attention must be paid here to the parameter ς, which directly influences the power factor. Indeed, the resistive part of the no load impedance is directly proportional to ς and as the power factor are small, with the small angle approximation, ς directly influences the power factor. This can be observed in Fig. 4.11.

It is useful at this point to express the input displacement factor due to the snubber, in function of the snubber design. Fig. 4.12 gives an illustrated definition of the input displacement factor due to the no load snubber current. As seen in chapter 2, the CWC sequence leads to an input displacement factor of 0.86. It is necessary to show here that for most snubber design, the additional no load current does not lead to such a poor input displacement factor. For this, one should know the fundamental value of the current through one generator phase expressed in function of the load current. According to the numerical results of chapter 2, the fundamental input current is 0.48 p.u

where 1 p.u. is the nominal load current. This value could also be reached by playing with nominal impedances $Z_{N,grid}$ and $Z_{N,gen}$. From this, it is possible to express the input displacement factor in function of the snubber design (c_s and ς), for two values of the generator parameter i_{short}. Fig. 4.13 and Fig. 4.14 give the no load input displacement factor in function of the snubber design for i_{short} = 5p.u. and i_{short} = 10p.u. resp.

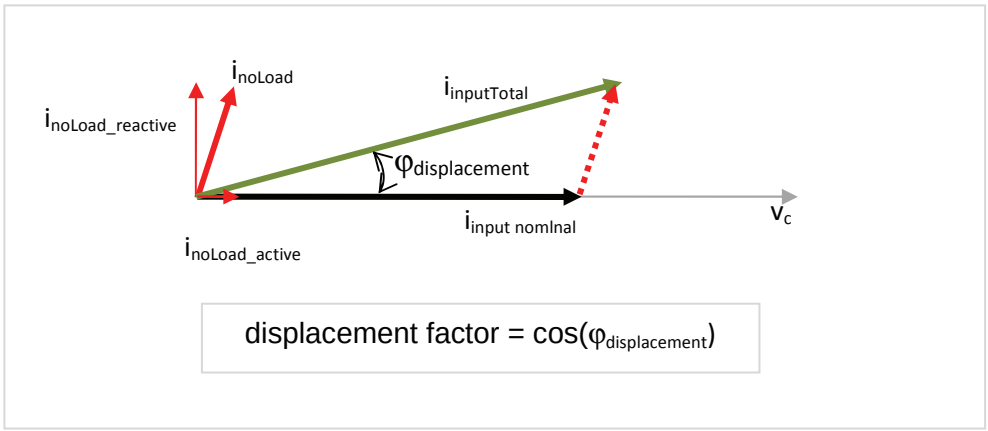


Fig. 4.12 – Definition of the input displacemtn angle due to snubber no load current

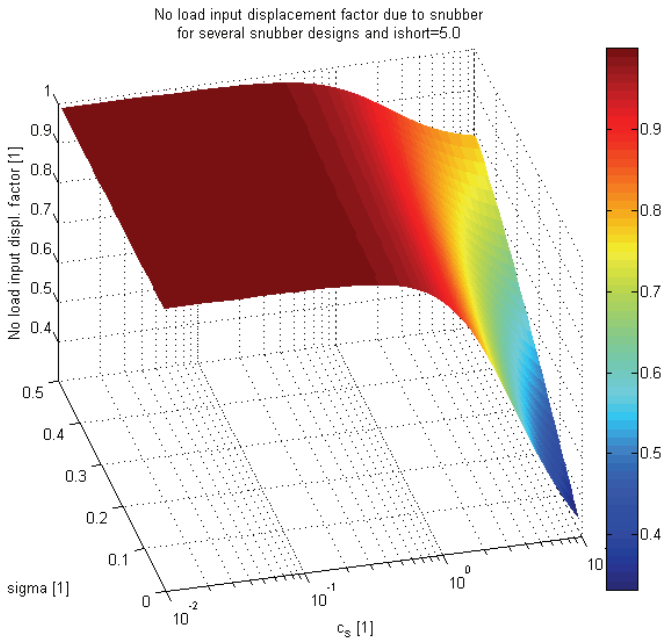


Fig. 4.13 – No load input displacement factor in function of snubber design for i_{short}=5pu

From Fig. 4.13 and Fig. 4.14, it can be observed that the no load input displacement factor is very close to 1 for most snubber designs. It can be concluded that the *slowCWC* theoretical unity input

displacement factor (see chapter 2) is not significantly affected by the presence of the snubber capacitor. The *slowCWC* sequence has hence better input quality as the *CWC* sequence.

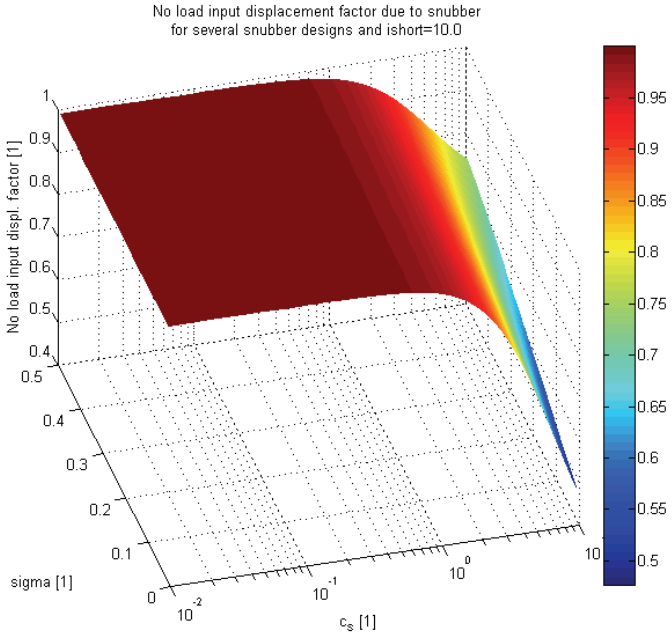


Fig. 4.14 - No load input displacement factor in function of snubber design for i_{short}=10pu

4.5.3 No load losses

in addition to the input displacement factor, which measures the influence of the capacitor on the input properties, it is important to assess the power dissipated in the snubber resistor due to the no load current. For relevant information, this power must be referred to the nominal output power. This is equivalent to ratio:

Equ. 4.53

$$p_{noLoad} = \frac{i_{noLoad\_active}}{i_{input,nominal}}$$

Fig. 4.15 and Fig. 4.16 illustrate the no load losses as given in Equ. 4.53, in function of the snubber design for two values of the generator parameter i_{short}. It can be deduced that for most snubber design, those no load losses are no significant in comparison to the nominal power of the converter. However, there is a fast transition zone around c_s=1 where those losses quickly reach non significant values. The scale in Fig. 4.15 and Fig. 4.16 is limited between 0% and 1%, however, the red zones contain higher values than 1%.

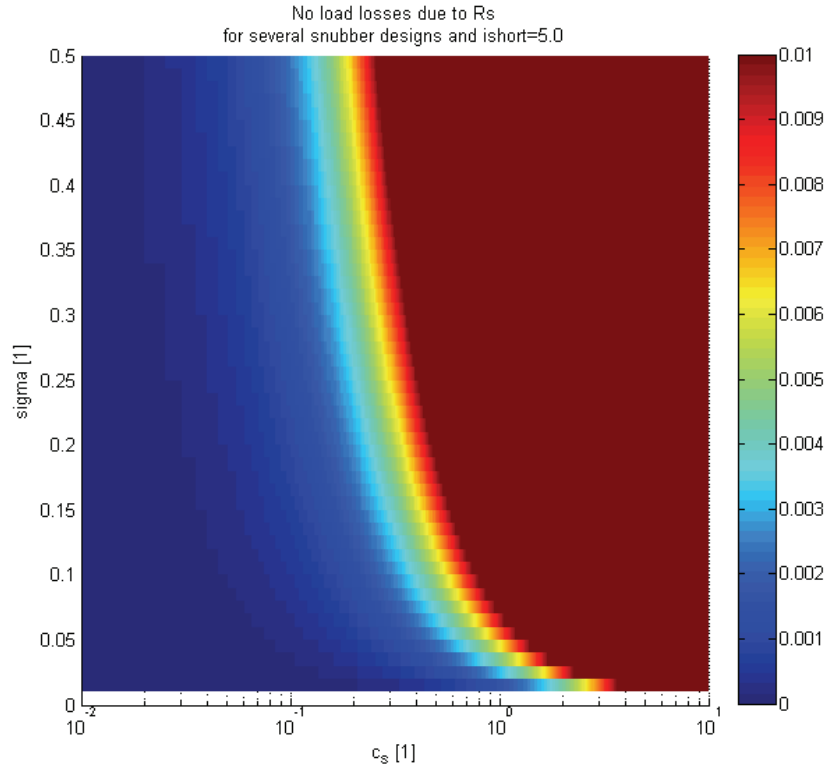


Fig. 4.15 – Per unit no load losses in function of snubber design and for i_{short}=5p.u.

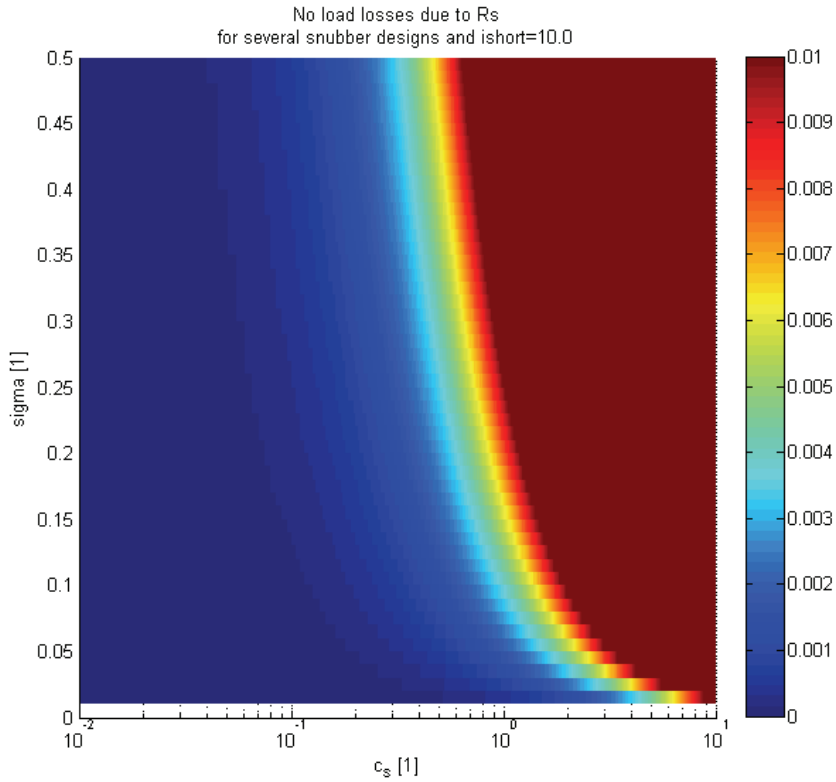


Fig. 4.16 – Per unit no load losses in function of snubber design and for i_{short}=10p.u.

4.5.4 Snubber losses for one forced or one natural commutation

In chapter 3, the conduction losses and switching losses in the BDS of the PPMC have been assessed and those values lied within reasonable and feasible margins. In paragraph 4.5.3, the no load losses due to snubber resistor have also been assessed and for most snubber design, those losses also stay within feasible margins. It is important at this stage to assess the losses in the snubber resistor due to the forced commutation and natural commutations. This is developed throughout this section which constitutes the base for the development of section 4.5.5.

Forced commutation

The theoretical calculation to obtain the losses through the resistor R_s of the snubber is given by Equ. 4.54.

Equ. 4.54
$$E_{lossOFF} = R_s \int I_s{}^2 dt$$

However, in order to simplify the calculations, the energy balance method is used. This energy balance is written for the equivalent RLC circuit valid during a forced commutation, for one commutation cell. The energy contained in the system between the start point (E_1) must be equal to the energy of the system at the end of the transient phenomena (E_2) plus the energy of the sources active during this transient response, as given by Equ. 4.55.

Equ. 4.55
$$E_1 = E_2 + E_{lossOFF} - E_{in} \qquad E_{lossOFF} = E_1 - E_2 + E_{in}$$

where E_{loss} are the losses in the systems (here only through R_s) and E_{in} is the energy injected by the voltage source. The lost energy can be deduced from Equ. 4.56 to Equ. 4.57 and is given by Equ. 4.58.

Equ. 4.56
$$E_1 = \frac{1}{2} L_{eq} I_0^2 + \frac{1}{2} C_s U_{cs0}^2 \qquad E_2 = \frac{1}{2} C_s \Delta V^2$$

Equ. 4.57
$$E_{in} = \int \Delta V I_s dt = \Delta V \int I_s dt = C_s \Delta V \int \frac{dU_{cs}}{dt} dt = C_s \Delta V \left[U_{cs} \right]_0^{\infty} = C_s \Delta V \left[\Delta V - U_{cs0} \right]$$

Equ. 4.58
$$E_{lossOFF} = \frac{1}{2} L_{eq} I_0^2 + \frac{1}{2} C_s U_{cs0}^2 - \frac{1}{2} C_s \Delta V^2 + C_s \Delta V \left[\Delta V - U_{cs0} \right] = R_s \int I_s{}^2 dt$$

Equ. 4.58 shows that the losses are not dependent on the value of R_s, for a given C_s. By assumption, the initial capacitor voltage is equal to the final value and is equal to the driving voltage ΔV at the commutation instant. The expression of the local losses simplifies in Equ. 4.59.

Equ. 4.59
$$E_{lossOFF} = \frac{1}{2} L_{eq} I_0^2$$

Natural commutation

If there are natural commutations, losses in R_s also appear because C_s will discharge to 0 and charge again to a final value ΔV_{end}, as described in chapter 3. The analysis of the local losses in R_s in case of a natural commutation is slightly more complex than in the case of the forced commutation. Indeed,

because of the configuration of the BDS, some natural commutations may be prematurely ended and induce a similar transient response as the forced commutations. Besides, some natural commutations have a duration that is not negligible in front of the period of the generator EMF which results in a more complex evaluation of the losses. The simplest way to calculate the losses through R_s for a natural commutation is to assume that the commutation duration (μ) as well as the discharge charge time constant R_sC_s are negligible in front of the generator EMF period T_g. In this case, final value of $\Delta V_{end} = \Delta V$ and the DC model can be used. In this case, for one natural commutation under ΔV, the losses in R_s are given by equation Equ. 4.60.

Equ. 4.60
$$E_{loss,1nat} = C_s \Delta V^2$$

The three phenomena described hereafter will modify this simple expression. This will be developed in paragraph 4.5.6 to 4.5.8.

Commutation duration effect (or μ effect)

In reality, μ is not always negligible in front of T_g. The final capacitor voltage (after recharge) will not be the same as the initial value because ΔV will evolve during this time. The simple formula given by Equ. 4.60 is not valid anymore and must be split into two parts: one part for the losses during discharge and one part for the losses during recharge, as expressed by

Equ. 4.61
$$\boldsymbol{E_{loss,1Nat} = \frac{1}{2} C_s \Delta V^2_{discharge} + \frac{1}{2} C_s \Delta V^2_{recharge}}$$

This requires the knowledge of the commutation duration to express ΔV_{end} in function of the initial capacitor voltage ΔV_{init}. For this, the development of chapter 3 will be used.

Premature cutt-off

The premature cut-off phenomenon is described in chapter 3. In case of a premature cut-off, losses should also be divided into two components: the partial discharge and then the losses of forced commutation under starting condition that have to be defined. As discussed in chapter 3 it is assumed that occurrences of such commutations are very scarce and this phenomenon will be neglected.

False natural commutation

The false natural commutation phenomenon is described in chapter 3. The losses in case of a false natural commutation are considered similar to a forced commutation. In the chapter about type of commutation, it is shown which conditions give rise to false natural commutations.

Other effects

There are still other effects that could be taken into account when assessing the snubber commutation losses, like the preliminary current cut-off due to too slow discharge compared to the natural rate, or small RLC time constant compared to the variation of EMF. However, those effects are considered to be negligible for the desired accuracy of the theoretical prediction.

4.5.5 Snubber commutation losses over one output period – full forced mode

This section is about the computation of the commutation losses of the whole snubber system (*m* RC elements) over one output period. Two operation mode of the PPMC are considered, the full forced commutation mode and the mix mode. In the full forced mode, thanks to an adjustable delay between step 2 and 3 of the four steps commutation rule it is possible to force all commutations, even when proper condition for natural commutations are met. In the mix mode, this delay is adapted to enable the natural commutations.

Equ. 4.59 gives the local losses for one forced commutation. As the output current Io is assumed to be sinusoidal, it is possible to write the losses for an "average" forced commutation. It is given by Equ. 4.62 (a), where the rms value of the output current appears. As there are *N* commutations per output period and per output phase, the overall losses are given by equation Equ. 4.62 (b).

Equ. 4.62
$$\overline{E}_{loss,1com} = \frac{1}{2} L_{eq} I_{oRMS}^2 \quad \text{(a)} \qquad E_{loss,hard} = 3N \frac{1}{2} L_{eq} I_{oRMS}^2 \quad \text{(b)}$$

Another approach to justify this expression is given hereafter and illustrated in Fig. 4.17.

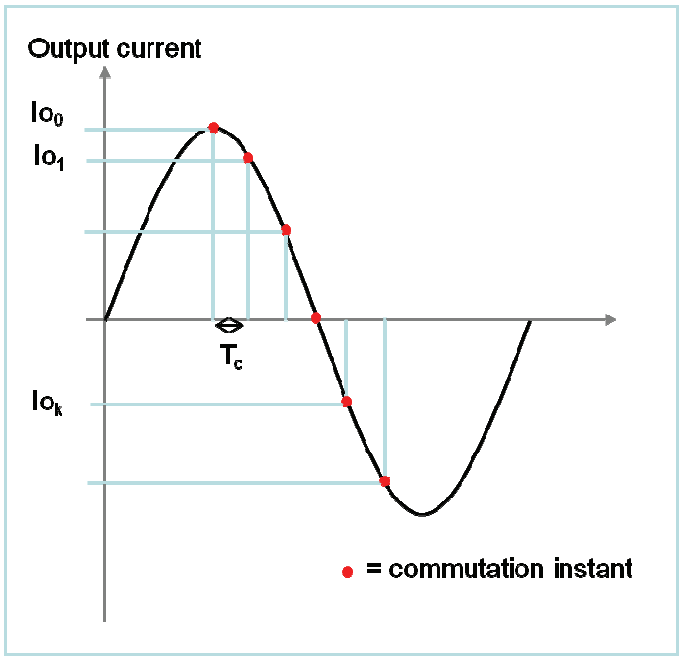


Fig. 4.17 – Discrete behavior of forced commutation overall losses

Equ. 4.63
$$N = m\left(\frac{F_g}{F_o} - 1\right) \quad N_{inf} = \lfloor N \rfloor$$

Equ. 4.64
$$E_{loss,hard} = \frac{1}{2} L_g \hat{I}_o^2 \sum_{k=0}^{N_{inf}-1} \cos^2\left(k\frac{2\pi}{N} + \varphi\right) = \frac{1}{4} L_g \hat{I}_o^2 \sum_{k=0}^{N_{inf}-1} 1 + \cos\left(k2\frac{2\pi}{N} + 2\varphi\right) = \frac{1}{4} L_g \hat{I}_o^2 \left(N_{inf} + \underbrace{\sum_{k=0}^{N_{inf}-1} \cos\left(k\frac{4\pi}{N} + 2\varphi\right)}_{\approx 0} \right) \cong \boxed{\frac{N}{2} L_g I_{oRMS}^2}$$

Equ. 4.63 gives the number of commutation per output period in function of the frequency ratio and the number of input phases. For the discrete calculation of Equ. 4.64, one need an integer value of N. N_{inf} is the integer part of N. Equ. 4.64 computes the total losses for one output phase over one output period by summing the N_{inf} commutation local losses. In Equ. 4.64 it must still be justified that the sum $\sum_{k=0}^{N_{inf}-1} \cos\left(k2\frac{2\pi}{N} + 2\varphi\right)$ is null.

- For integer values of N, N_{inf}=N, and if N>2, this sum is null. If N=1 or N=2, this describes a stationary case and the value of this sum is given by Ncos(2φ).
- For non integer values of N but if N can be expressed as a rational number d/q with d>2q, then this sum is not necessarily null but if N_{inf} is redefined to a new value of q*N_{inf} which means that the rms value is really correct if losses are assessed on q time the output period. N=inf(d/q) + e/q with e being an integer. Hence an evaluation of the sum on q*N_{inf} made it null (repetition period).
- If N is not a rational number, then the repetition period is infinite.

From those results we accept that the RMS value is a good approximation of an average commutation. However, as the regime will, in practice, never be stationary (frequency ratio almost never a rational number), from a statistical point of view, the RMS approximation will be accepted for the theoretical prediction. Besides, as there are three symmetrical output phases, the approximation of Equ. 4.64 is even more true.

4.5.6 Snubber commutation losses over one output period – mix mode

Earlier it has been shown that the ratio of forced and natural commutation depends on the output power factor. The equivalent mean value of losses for a forced commutation, given by Equ. 4.62 (b), can also be expressed in function of I_{oRMS} for the mix mode but it must be modulated by a factor that represents the reduced number of forced commutation over one output period. The idea is to compute the rms value over one output period T_o of a truncated sinus as depicted in Fig. 4.18. Fig. 4.18 shows how the truncated sinusoidal output current is deduced, depending on the output power factor, where φ_{pf} is the output displacement angle, accounted positive when output currents lags voltage. The portion depends on the zones of forced commutation. The calculation of the rms value of this truncated sinusoidal current leads to the expression of the mean losses for a forced commutation. Then the effective losses due to forced commutations are just the multiplication of this value by N. Equ. 4.65 gives the expression of the losses due to forced commutation in mix mode in function of the output power factor angle.

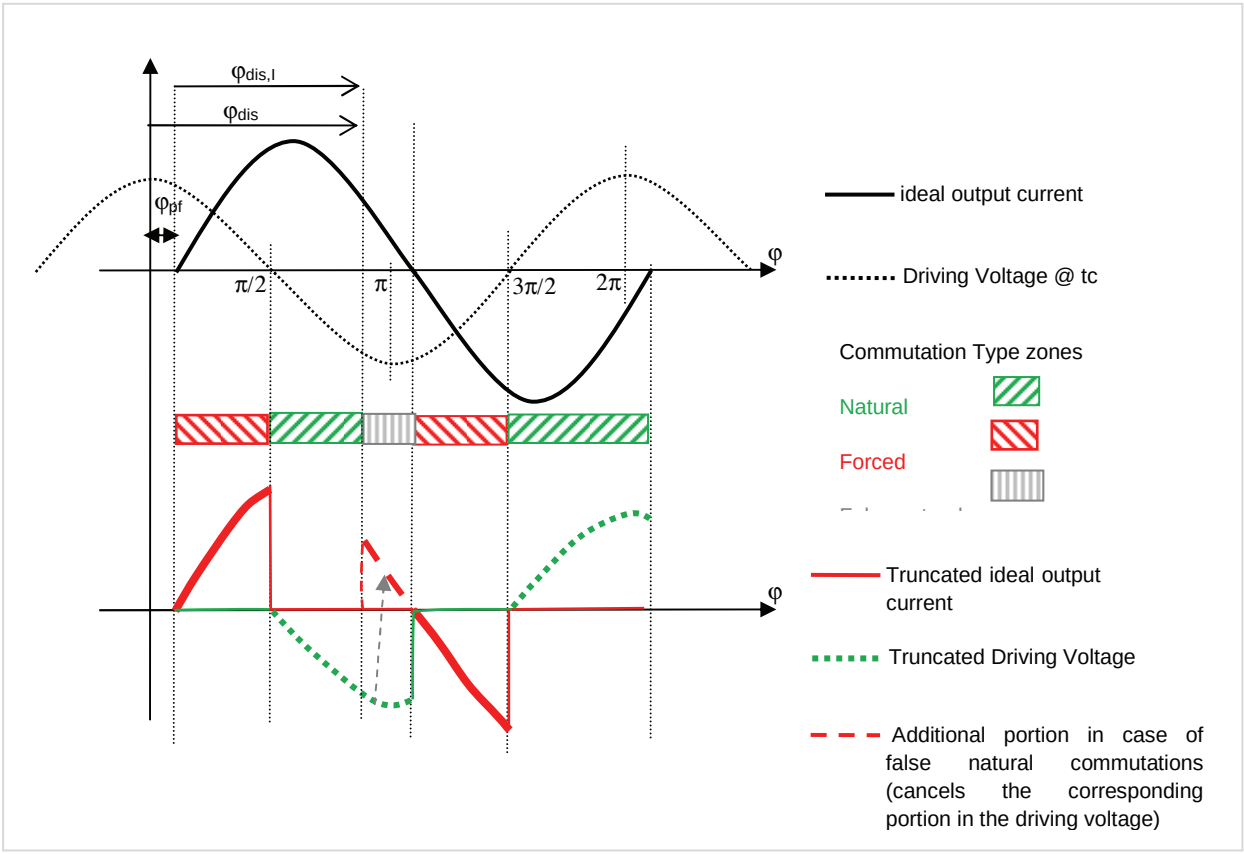


Fig. 4.18 – Truncated sinus waveforms method for expression of snubber losses in mix mode

A similar development as for the forced commutations brings the formula for natural losses in function of φ_{pf}, which is given in equation Equ. 4.66.

Equ. 4.65
$$\boldsymbol{E_{loss,forced} = \frac{3}{2} N L_g I_{oRMS}^2 \left[\frac{1}{2} + \frac{\varphi_{PF}}{\pi} + \frac{\sin(2\varphi_{PF})}{2\pi}\right]}$$

Equ. 4.66
$$\boldsymbol{E_{loss,nat} = 3NC_s EMF_{oRMS}^2 \left[-\frac{1}{2} - \frac{\varphi_{PF}}{\pi} - \frac{\sin(2\varphi_{PF})}{2\pi}\right]}$$

The total losses in R_s are simply the sum of Equ. **4.65** and Equ. **4.66**.

Equ. 4.67 gives the total snubber losses for the mix mode but in a p.u. system where the reference is Equ. 4.62 (b), i.e. the losses in full forced mode.

Equ. 4.67
$$\boxed{\boldsymbol{e_{loss} = \frac{1}{2}(1 + 2c_s) + (1 - 2c_s)\left(\frac{\varphi_{PF}}{\pi} + \frac{\sin(2\varphi_{PF})}{2\pi}\right)}}$$

So from $E_{loss,100\%\,forced} = 3N\frac{1}{2}L_{eq}I_{oRMS}^2$ one can quickly evaluate the losses through R_s in function of the snubber design and the expected operating points. This value depends of course on φ_{pf} but also on the design of the snubber, in particular the ratio c_s. Fig. 4.19 is the plot of Equ. **4.67** for several snubber design. The p.u. expression is valid for a constant apparent power and varying power factor,

hence constant output current. In this way I_{oRMS} does not depend on the power factor. However, in practice EMF_{rms} does depend on the power factor even by constant output current, hence the value of R_{base} changes and consequently c_s also depends on the power factor. The reader, if any, must then read the following snubber losses abacus with caution and take into account that when shifting from one power factor to the other, the value of c_s changes and it is required to jump from one curve to another. The user has always to know the base value with which the snubber has been designed. However, in practice, the variation of EMF should be in the range of +-10% hence the variation of c_s in the range of 20% since C_{base} depends on the square of EMF. When observing the curves for each c_s value in the following snubber losses abacus, it can be deduced that a 20% variation of c_s does not lead to significant variation of snubber losses except for small lagging power factor.

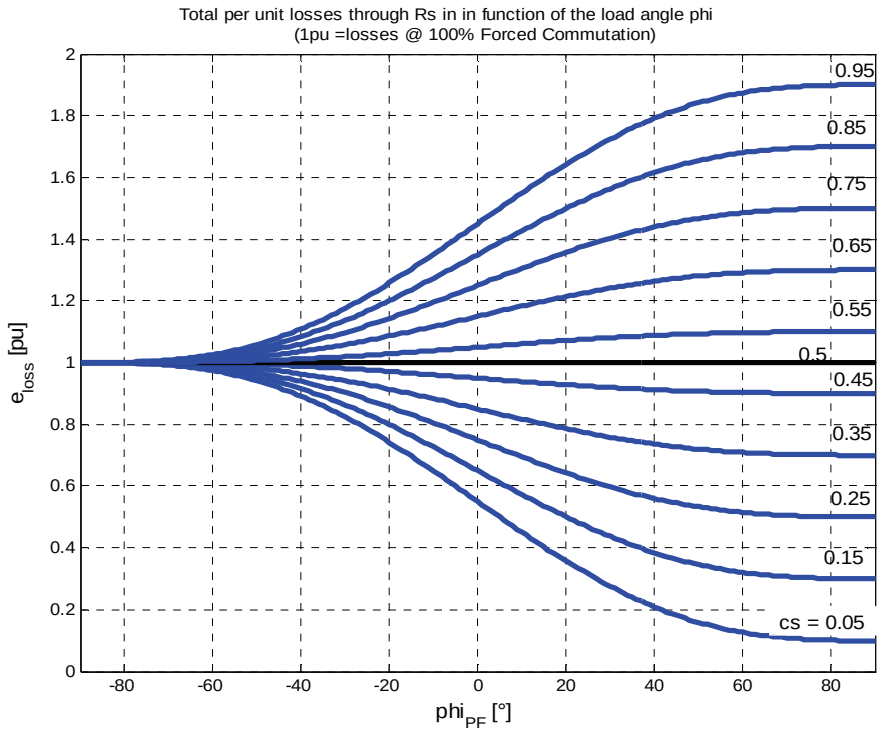


Fig. 4.19 - Relative overall losses through R_s in function of output power factor and snubber design (1 pu are losses @ 100% forced commutations)

Fig. 4.19 shows the obvious consequence on running the converter with a null lead power factor. In this case, every commutation is forced hence the expected losses are equal to the full forced mode, i.e. 1pu. On the other extreme side, when running the converter with a null lagging power factor, all commutations are natural and losses directly depend on the capacitor value, that is c_s. The variation of losses between both extreme points is smooth as can be observed. The design case of c_s=0.5 gives similar losses as the full forced mode. For usual power factor between ±40° the choice in design of snubber can have significant impact on the snubber losses. Because of this, it is interesting to investigate the prediction of snubber losses one step further and take into account a phenomenon described in chapter 3 and repeated in paragraph 4.5.4, the false natural commutation.

4.5.7 The effect of false natural commutations on the snubber commutation losses

As said above, there is the phenomenon of false natural commutation. In chapter 3 it is detailed the angular position related to the output target waveform from which the false natural commutation phenomenon takes place. This angle was named φ_{dis}. It depends on the output power factor and on the snubber design value r_s. In Fig. 4.18 another angle is shown, it is $\varphi_{dis,I}$ defined by

Equ. 4.68 $$\varphi_{dis,I} = \varphi_{dis} + \varphi_{PF}$$

It is the limit angle related to the angular position of the sinusoidal target output current. This has simplified a bit the formula. In order to determine the snubber losses taking into account this false commutation phenomenon, the method of truncated waveforms is also used, as described by Fig. 4.18, but the truncated output current has a new portion at the place of the false commutation zone. Equ. 4.69 and Equ. 4.70 give the expression of the losses due to forced commutations and natural commutations resp. with the false natural phenomenon taken into account, in function of the output power factor angle and the angle which defines the false natural commutations zone. Chapter 3 has developed the expression of φ_{dis} in function of φ_{pf}.

Equ. 4.69 $$\boldsymbol{E_{loss,forced} = \frac{3}{2} N L_g I_{oRMS}^2 \left[\frac{3}{2} + \frac{(\varphi_{PF} - \varphi_{dis,I})}{\pi} + \frac{(\sin(2\varphi_{dis,I}) + \sin(2\varphi_{PF}))}{2\pi}\right]}$$

Equ. 4.70 $$\boldsymbol{E_{loss,nat} = 3NC_s EMF_{oRMS}^2 \left[-\frac{1}{2} - \frac{(\varphi_{PF} - \varphi_{dis,I})}{\pi} + \frac{\sin\left(2(\varphi_{dis,I} - \varphi_{PF})\right)}{2\pi}\right]}$$

with φ_{PF} negative when lagging output power factor, and $\varphi_{dis,I}$ positive as in Fig. 4.18. The total losses are simply the addition of the forced and natural contribution. $\varphi_{dis,I}$ is related to the output current waveform where I_o=sin(φ)

Equ. 4.71 $$\boldsymbol{E_{loss} = E_{loss,forced} + E_{loss,nat} \qquad e_{loss} = \frac{E_{loss}}{E_{loss,FULLforced}} = \frac{E_{loss}}{\frac{3}{2} N L_g I_{oRMS}^2}}$$

Again, it is wished to express those losses in per unit were the reference is always the full forced mode.

$$\boldsymbol{e_{loss} = \frac{(3 - 2c_s)}{2} + \frac{(\varphi_{PF} - \varphi_{dis,I})}{\pi}(1 - 2c_s) + \frac{(\sin(2\varphi_{dis,I}) + \sin(2\varphi_{PF}))}{2\pi} + c_s \frac{\sin\left(2(\varphi_{dis,I} - \varphi_{PF})\right)}{\pi}}$$

Equ. 4.72

Fig. 4.20 shows the p.u. losses of Equ. 4.72 for several snubber optimal snubber designs. As said for the previous snubber losses abacus, in Fig. 4.18. those abacus have to be read and interpreted with caution when comparing two power factors for a same snubber design. Indeed, the value c_s varies when power factor varies because EMF must be adapted. As the snubber design can a priori be based on any power factor wished, those abacus do not take into account the dependency of c_s on the power factor, it is the job of the user to jump to the corresponding adapted c_s curve. This is especially important for the small lagging power factor.

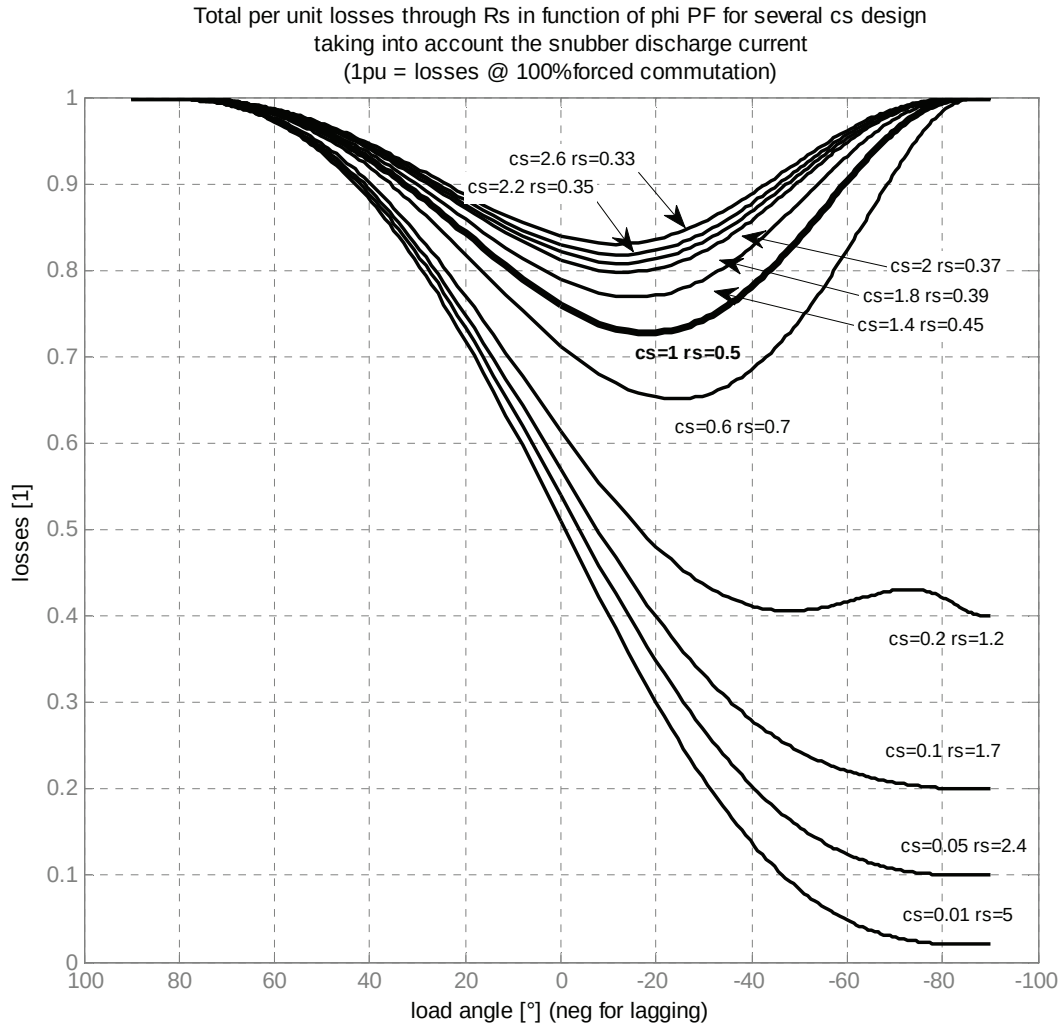


Fig. 4.20 – Relative snubber losses abacus for the mix mode operation with false commutations

The behaviour of those curves is not fundamentally intuitive. It must be kept in mind that those curves are drawn always for an optimal set of snubber design values c_s and r_s. So for each c_s the r_s and hence the limit angle φ_{dis} are set. This angle φ_{dis}, (or $\varphi_{dis,I}$) are given in Fig. 3.25 and Fig. 3.26. The reader of this work, if any, should keep this figure in mind when analysing Fig. 4.20. Also, this figure can be understood from Fig. 4.19 above.

For unity power factor, first, where the ideal split between forced and natural commutation is 50%, it was mentioned for Fig. 4.19 that for a c_s=0.5, both of the contribution of forced and natural commutation to the total losses were equal hence e_{loss}=1. In Fig. 4.20, for cs=0.5 this is not any more the case because the false natural commutations induce less losses than if those losses were natural. This is obvious because the false natural commutation occurs when the driving voltage ΔV reaches the neighbourhood of its peak value. Besides, for the design with c_s=0.5, r_s=0.73 and according to the chart giving φ_{dis}, the zone of false natural commutation has a non negligible width compared to the normal 90° hence the benefit of false natural commutation in terms of losses reduction is sensible in the Fig. 4.20. With increasing c_s, the losses due to natural commutations increase directly proportionally whereas the widening of the false commutation, through decreasing of r_s, does not grow as fast. Besides, the effect of the growing of the false natural commutation zone is less

interesting in terms of losses reduction because those natural commutations are replaced by forced commutation with a cut-off current more and more near to the peak value I_{opeak}. All in all, it makes the increasing of c_s less efficient in term of losses reduction. This can also be observed in Fig. 4.20. On the contrary when decreasing c_s, r_s increases, which reduces the false natural commutation zone and the situation tends to be similar to Fig. 4.19.

For lagging power factor, it appears that there are two tendencies among the curve representing distinct snubber design. There are the curves that follow the same tendency as in Fig. 4.19 for obvious reasons. These are the curves corresponding to a r_s above 1. There are the curves which tend to the value 1p.u. for decreasing lagging power factor. These are the curves with a r_s below 1. This separation is exactly the same as the separation into two groups of tendency for the variable φ_{dis} (Fig. 3.26). Normally, the decrease of a lagging power factor widens the natural zones but r_s above 1 also reduce it by widening the false natural commutations. All in all, the situation tends to the full forced commutation situation.

For decreasing leading power factor, the zone of the natural commutation reduces and all the effects of the false natural commutations have less and less importance in the determination of snubber losses. This is clearly shown in Fig. 4.20.

Generally it is to be remarked that in comparison with Fig. 4.19, where the false natural commutation is not taken into account, the losses are in all cases smaller when this phenomenon is taken into account which means that for most cases, the mix mode operation of the PPMC is interesting in order to reduce the snubber losses, especially if the snubber design asks for large values of c_s. But the author is not yet satisfied with this model of the snubber losses and wishes to extend this model to one more and last detail, presented in the next paragraph.

4.5.8 The effect of natural commutation duration on snubber commutation losses

As said in paragraph 4.5.4, Equ. 4.61, the formula for the local losses of a natural commutation is split into two parts, one for the discharge and one for the recharge of the snubber capacitor. Expression of the discharge part, for one output period, is easy and is given by Equ. 4.73, already in the relative form.

Equ. 4.73
$$e_{\text{lossNatDis}} = c_{\text{s design}} \left[\frac{\left(\varphi_{\text{disRel}} - \varphi_{PF}\right)}{\pi} - 0.5 + \frac{\sin\left(2\left(\varphi_{\text{disRel}} - \varphi_{PF}\right)\right)}{2\pi} \right]$$

The expression of the recharge in an analytical formula is more complex because it depends on non linear and non sinusoidal functions. Therefore this is numerically integrated in the computation of the overall losses but, because everything can be expressed in per unit, the results are still general.

The method used to express the local losses at the recharge in function of a given initial discharge voltage $\Delta V_{discharge}$ is also based on the expression of a mean local loss via the expression of the rms value of a truncated signal. However for the recharge, the signal that will be truncated is not a sinus waveform, as it is for the signal $\Delta V_{discharge}$. For given generator parameters (r_g, x_g and i_{short}), a given

output operating point and a given initial capacitor voltage $\Delta V_{discharge}$, chapter 3 shows how to compute the natural commutation duration μ. Therefore, from the sinus waveform $\Delta V_{discharge}$ and the value $\mu(\Delta V_{discharge})$ one can compute the waveform of the recharge voltage $\Delta V_{recharge}$. When this waveform is computed, its truncated rms value can also be computed in order to express a mean local loss for the recharge. The snubber overall losses of snubber, for different design and output operating points, which takes the natural commutation duration into account is drawn in Fig. 4.21 and Fig. 4.22 for two values of generator parameter i_{short} (5 p.u. and 10 p.u. resp.).

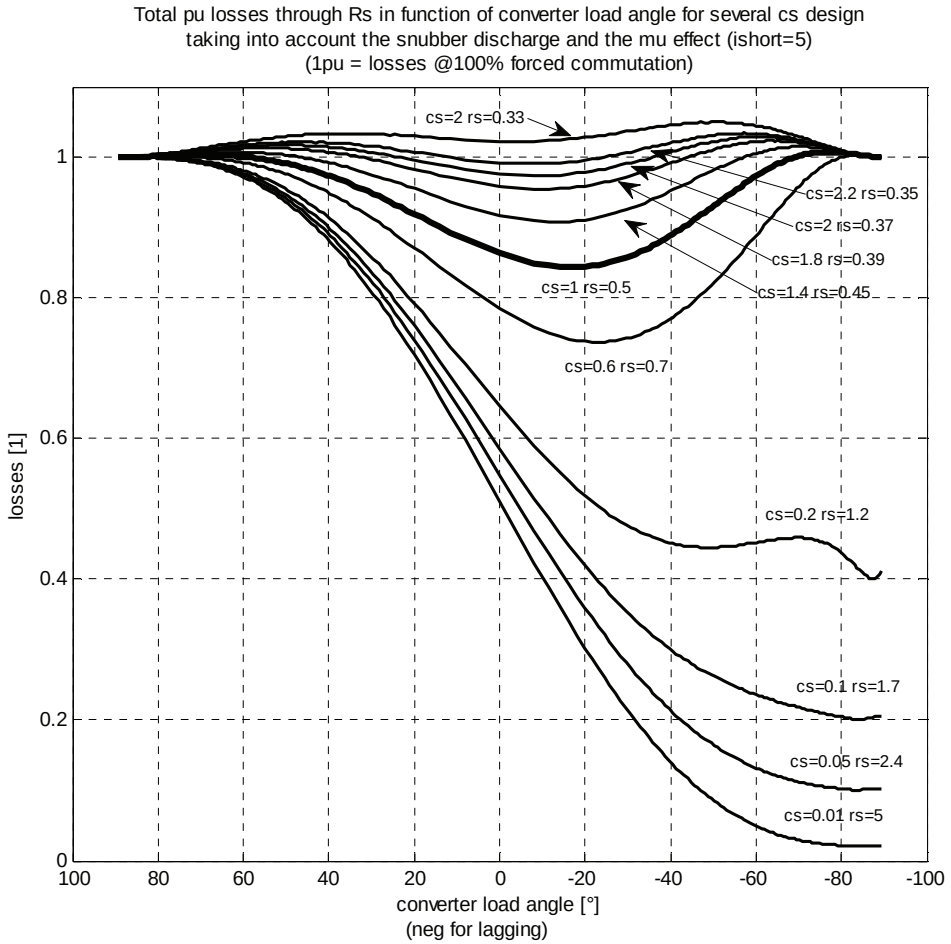


Fig. 4.21 - Relative snubber losses abacus for the mix mode with false com. and µ effect (i_{short}=5p.u.)

Generally speaking, the effect of the natural commutation duration on the snubber overall commutation losses is not very significant, compared to the false commutation effect. The µ effect only slightly modifies the tendencies of the Fig. 4.19 and Fig. 4.20. Obviously, this effect is more visible for small values of i_{short}. Also, this effect is more significant for large values of snubber design c_s since this means a higher capacitor value and more energy stored. To conclude with the relative snubber losses, one can accept that the m effect is no significant for most snubber designs. Moreover, the relative losses remain under the value of 1 p.u. but do not move far away from this

reference, except for extreme output lagging operating points. Therefore, in the next section, the reference value Equ. 4.62 (b) is taken for the expression of the snubber overall commutation losses relatively to the converter output power.

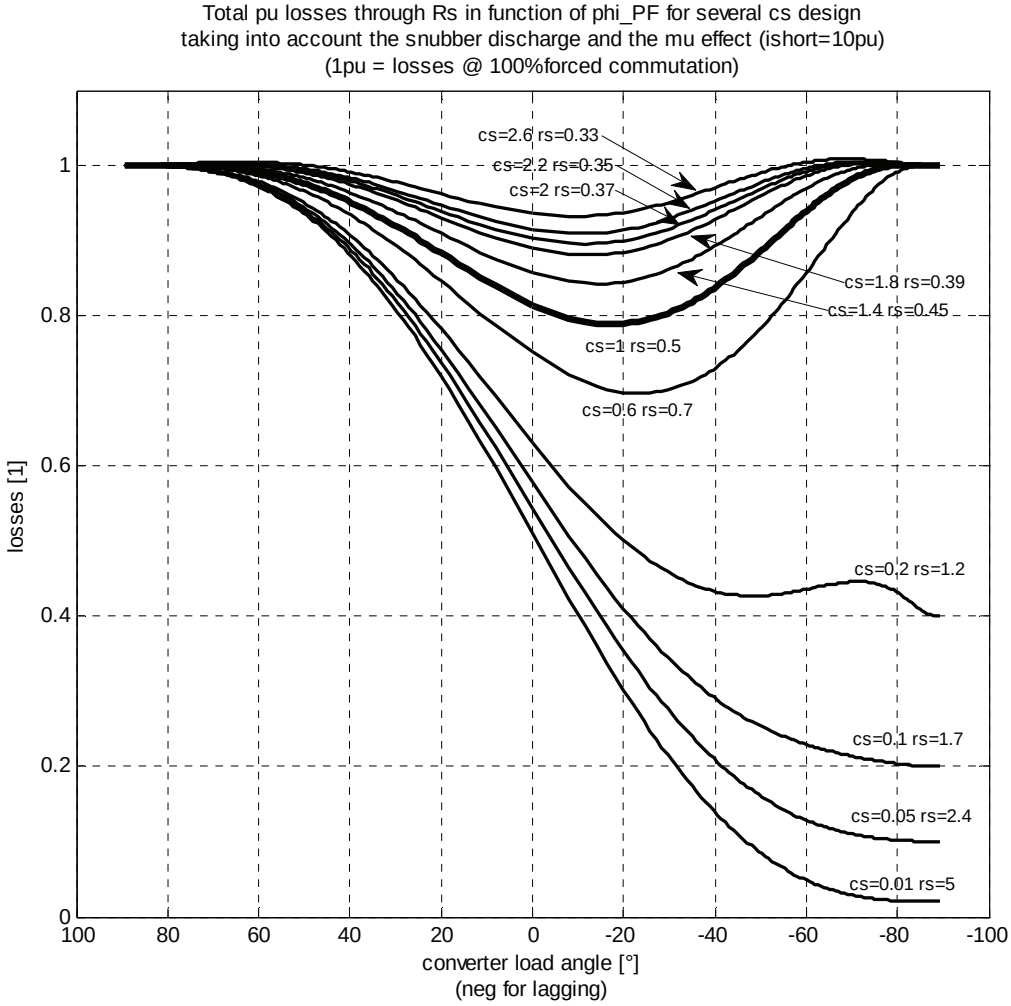


Fig. 4.22 - Relative snubber losses abacus for the mix mode with false com. and μ effect (i_{short}=10p.u.)

4.5.9 PPMC efficiency drop due to snubber commutation losses

In the previous section, comparison and contribution of forced commutations and natural commutation to the overall snubber commutation losses are expressed. They can always be expressed as a fraction of the reference full forced mode snubber losses. So, this reference value is used to express the ratio of those losses function of the output power of the converter. This leads to the contribution of the snubber to the converter efficiency drop-off.

The output power is given by Equ. 4.74.

Equ. 4.74
$$\boldsymbol{P_o = 3V_{grid,rms} I_{oRMS} \cos \varphi_{PF}}$$

The ratio of the snubber commutation losses to the converter output power is given in Equ. 4.75.

Equ. 4.75

$$\frac{E_{loss,fullForced}}{P_o T_o} = \frac{3NL_g I_{oRMS}^2}{6V_{grid,rms} I_{oRMS} \cos\varphi_{PF}}$$

By using the definition of N given by Equ. 4.63 and the collection of p.u. expressions of generator parameters given in chapter 3, and repeated hereafter, one can obtain the ratio of Equ. 4.75 in a full p.u. representation as shown by Equ. 4.76.

$$N = \frac{T_c}{T_o} \qquad X_g = x_g Z_g \qquad I_{N,short} = \frac{V_{N,gen}}{Z_g} \qquad V_{N,gen} = 2\sin\left(\frac{\pi}{m}\right) V_{N,grid}$$

Hence

Equ. 4.76

$$\boxed{\frac{E_{loss,fullForced}}{P_o T_o} = \frac{m\left(1-\frac{F_o}{F_g}\right) x_g \sin\left(\frac{\pi}{m}\right)}{2\pi i_{short,nominal} \cos\varphi_{PF}}}$$

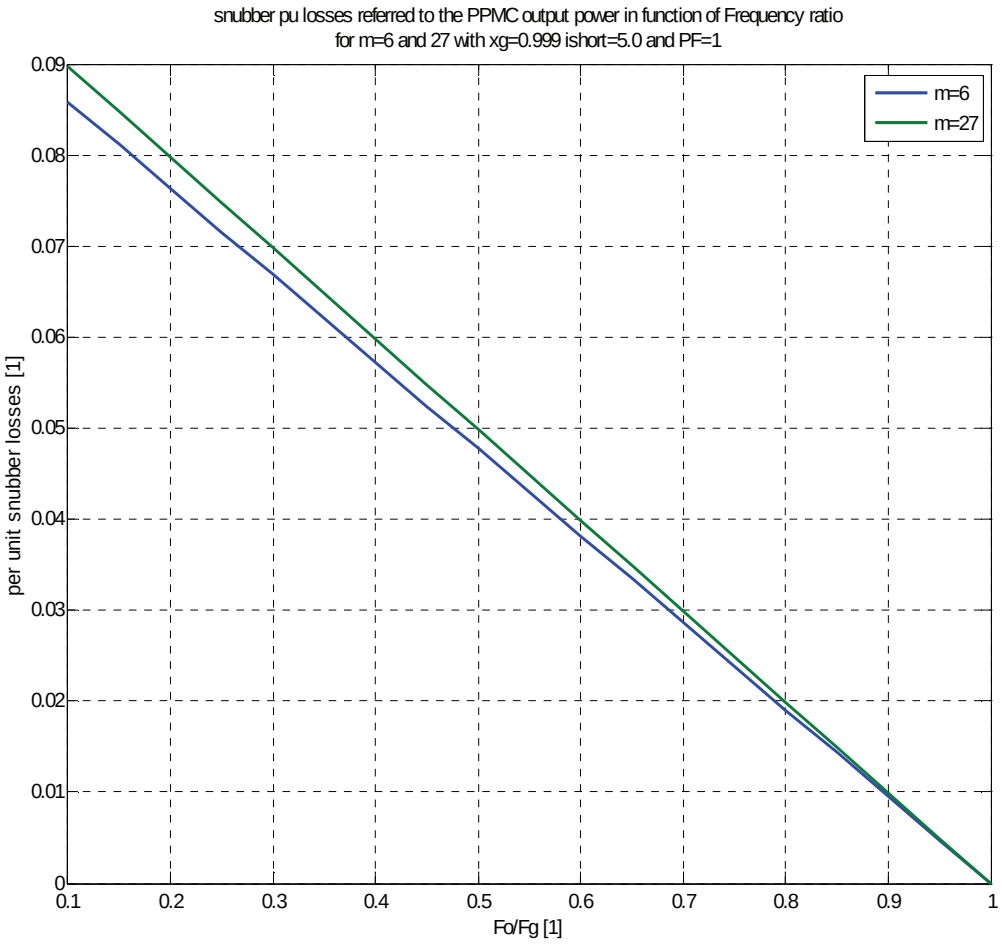


Fig. 4.23 – PPMC efficiency drop due to overall snubber commutation losses

Fig. 4.23 illustrates Equ. 4.76 in function of the frequency ratio of the PPMC, for two values of input phase number *m* (6 and 27), with the generator p.u. parameters i_{short} set to 5p.u and x_g set to 0.99p.u. and for unity power factor.

The effect of *m* is not really significant except for low frequency ratio where 0.5% of efficiency could be gained if a six phases machine was used instead of a 27 phases, however this analysis is only valid for the snubber efficiency and no conclusion can be drawn for the global PPMC efficiency. The parameter *m* directly influences the number of commutations, i.e. the losses, but the analysis compares cases with similar relative short circuit current i_{short}, hence when changing *m*, the windings inductance L_g must be adapted, this is why the effect of *m* is not direct in the Fig. 4.23.

The effect of the frequency ratio F_o/F_g is linear and directly observable on Fig. 4.23. the effect of other parameters, the power factor and the relative generator windings reactance, are straightforward and not discussed here.

Generally, it can be deduced that the effect of snubber commutation losses on the PPMC efficiency drop is not negligible and ranges between 7% and 1% for usual frequency ratio. From those numerical value, the feasibility of the PPMC could be a serious matter of discussion. However, the influence of the parameters i_{short} is direct and modification of the generator design rules could shift the snubber losses into a feasible range.

4.6 Case study to illustrate the snubber design rules

As a first example of snubber design, the case study 1 and 2 are used. In a first time, the case design performed on the bases of the nominal parameters given in chapter 3 in the introduction to the case study. However, the simulation case operating points differs from the nominal operating point. The active power is still 300MW but the power factor is unity. As a consequence the peak current to cut is a bit below the nominal current. This deviation from the nominal operating point is taken into account in the analysis that follows.

4.6.1 Snubber design-base values

The nominal values of case study are given in chapter 3 for case 1 and for case 2. The design of the snubber is done on the case 1. However, there is one slight modification in the computation of R_{base}. The value of ΔV_{peak} is not the peak nominal generator EMF but the peak EMF when EMF is adapted for the nominal operating point. It means that EMF must be slightly increased to create the voltage drop across the load impedance. By doing so, the design is really based on the worst base case. In practice, this increased generator EMF usually does not overpass 10% of the nominal value.

$$I_{o,peak} = 13.2kA \quad \Delta V_{peak} = 4.4kV \quad \Rightarrow \boxed{R_{base} = \frac{\Delta V_{peak}}{I_{o,peak}} = 0.33\Omega}$$

Base capacitor for case 1

$$L_g = 117\mu H \quad \Rightarrow \boxed{C_{base} = \frac{L_g}{R_{base}^2} = 1.1mF}$$

Base capacitor for case 2

$$L_g = 58\mu H \Rightarrow \boxed{C_{base} = \frac{L_g}{R_{base}^2} = 0.53mF}$$

4.6.2 Snubber design - Choice of overvoltage

It is required now to set a maximum admissible for the snubber voltage V_s. According to the properties of the PPMC, its switches must be able to withstand the double of the converter peak star voltage $2V_{cR}$. This would be a reasonable constraint for the maximum snubber voltage. However the constraint of the generator windings should also be taken into account. A second approach is to say that the generator windings have a limited insulation value. This is beyond the scope of this work to know the value of those insulations. It is assumed that the generator windings can withstand up to three times $\Delta V_{peak,}$ i.e. a 3p.u. design rule.

Here are the numerical values for both of those design options

- Switch constraint design - $V_{smax} = 2V_{cR}$

  Using the star to polygon ration $V_{cR}=4.35\Delta V_{peak}$ for *m*=27 hence $\frac{V_{s,max}}{\Delta V_{\text{peak}}}$ =8.7p.u.

  According to the optimal design abacus of Fig. 4.3

  $$c_s=0.011 \quad and \; r_s=5.0$$

- Generator windings constraint design – V_{smax}=3p.u.

  According to the optimal design abacus of Fig. 4.3

  $$c_s=0.16 \quad and \; r_s= 1.3$$

Table 4.4 gives a summary of the snubber parameters numerical values-

Table 4.4 – Numerical values of snubber design for case study

Parameters		Values	
		Case 1	Case 2
R_{base} [Ω]		0.33	0.33
C_{base} [mF]		1.1	0.53
α_{base} [1/s]		1377	2859
Switch design (v_{smax}=8.7p.u.)	c_s=0.011 r_s=5.0		
	C_s [µF]	12	5.8
	R_s [Ω]	1.6	1.6
	t_s (5%) [ms]	0.73	0.36
	no load losses [%]	< 0.3	
Generator winding design (v_{smax}=3p.u.)	c_s=0.16 r_s= 1.3		
	C_s [µF]	176	85
	R_s [Ω]	0.43	0.43
	t_s (5%) [ms]	2.2	1.1
	no load losses [%]	< 0.3	

The no load losses of both designs are acceptable or reasonable. However, damping constraint of the second design is not compatible with the constraint that is the commutation period T_c, since T_c for a 100Hz to 50Hz conversion with m=27 is 740µs. To adjust this constraint, one could increase the damping ratio ς to 0.4 but in a first time, this is not done and the simulation will be performed with the values of the design as in Table 4.4.

4.6.3 Simulation parameters

As said above, the first simulation result presented here does not reproduce the nominal operating point accordingly to the one given in chapter 3. It is a nominal power but unity power factor. It means that the effective load current is lower than the nominal current and the EMF is also slightly lower than the one required for the nominal operating point. This changes the base values and it is possible to express the effective p.u. values of c_s and r_s for this specific case.

Case 1, 300MW pf 1

$$I_{o,peak} = 11.2kA \quad \Delta V_{peak} = 4.2kV \quad \Rightarrow \quad \boxed{R_{base} = \frac{\Delta V_{peak}}{I_{o,peak}} = 0.38\Omega}$$

Correction factor

$$\epsilon = \frac{R_{base}}{R_{base,design}} = \frac{0.38}{0.33} = 1.14$$

$$r_s = \frac{R_s}{R_{base}} = \frac{R_s}{\epsilon R_{base,design}} = \frac{r_{s,design}}{\epsilon}$$

$$C_{base} = \frac{L_g}{R_{base}^2} = \frac{L_g}{\epsilon^2 R_{base,design}^2} = \frac{C_{base,design}}{\epsilon^2}$$

$$c_s = \epsilon^2 c_{s,design}$$

This correction does not affect the optimal design according to the following expression.

$$\varsigma = \frac{r_s\sqrt{c_s}}{2} = \frac{r_{s,design}\sqrt{\epsilon^2 c_{s,design}}}{\epsilon 2} = \varsigma_{design} = 0.26$$

Table 4.5 – Correction of snubber design parameters due to different operating points

	Nominal operating point design			Operating Point 1 (P_N,pf=1) => ε=1.14		
	c_s	r_s	v_{smax}	c_s	r_s	v_{smax}
Switch design	0.011	5.0	8.7	0.014	4.4	7.9
Generator winding design	0.16	1.3	3	0.21	1.1	2.7

4.6.4 Simulation results analysis

Simulation result of case 1 with the snubber designed with the switch constraints and the operating point 1 of Table 4.5 are shown in Fig. 4.24. This figure shows one converter output voltage V_{cR} applied to the load phase R (black curve) along with the network corresponding phase voltage V_{gridR}. The corresponding load current can also be viewed (blue trace). Finally, the voltage across one generator phase (number 27 here) $V_{s(27)}$ and the corresponding EMF_{27} are represented in red. The effect of the no load current can be viewed as the difference between V_s and EMF when no commutation occurs. The voltage drop across Z_g due to this no load current is negligible and, in steady state, EMF and V_s can be confounded. On Fig. 4.24, there are three occurrences of commutations on V_{s27} that can be observed. The time between each should be $1/3(F_g-F_o)$ which is 6.66ms which is the case in Fig. 4.24. The first commutation that can be observed on V_{s27} is linked to the output phase R and is the one of interest here because output phase R load current and phase voltage are traced also on this graph. This commutation occurs at the peak value of output current I_{opeak}, but with an initial snubber voltage that is null because power factor is unity. This does not prevent to do an interesting analysis though. In a general manner, it can be observed that for the commutations adjacent to this one the transient response is much smaller. This shows that the main assumption of "single active snubber per commutation cell" is reasonable. Fig. 4.24 also well illustrates the fact that for unity output power factor or close to unity, the overvoltage due to the forced commutations have a corresponding effect on the converter output voltage V_{cR} that goes towards a voltage reduction in absolute value. The worst peaks on V_{cR} are negative for the positive half wave of V_{cR} and positive for negative half wave of V_{cR}.

Fig. 4.25 shows a closer view over the commutation of interest. The peak value of V_{s27} for this commutation is about 30.05kV. If referred to the ΔV_{peak} of 4.2kV this gives a u_{smax}=7.1pu. According to the theory developed in section 4.2.5 about effective peak voltage, v_{smax} for this commutation occurring at φ_c=90°, v_{smax}=6.9pu. The error is 3% which will be acceptable because of incertitude about exact current at commutation time and because this value differs from the theoretical target value. One could add another analysis by computing the exact base resistance R_{base} related to this commutation. From this effective base resistance, one can compute a correction factor ε and then compute effective r_s and c_s. Finally, according to Fig. 4.3, one can deduce the effective v_{smax}. This analysis is given here:

$$R_{base,effective} = \frac{4.2kV}{12kA} = 0.34\Omega \;\Rightarrow\; c_{s,effective} = 1.08 \cdot c_{s,design} \;\Rightarrow\; v_{smax,effective} = 7.5$$

This gives an error of 5%. This error is mostly due to the fact that the commutation does not exactly occur at φ_c=90° but a bit later, around 97°. By taking this into account and again using the facts of section 4.2.5, this gives v_{smax} effective of 7.3 reducing the error to 3%.

The settling time of the transient response can also be compared with the theoretical prediction. Only the order of magnitude is of interest here. For case 1, with this snubber design, t_s is theoretically equal to 730µs, which is almost a commutation period $T_{c.}$ at a first glance at Fig. 4.25, this value is correct.

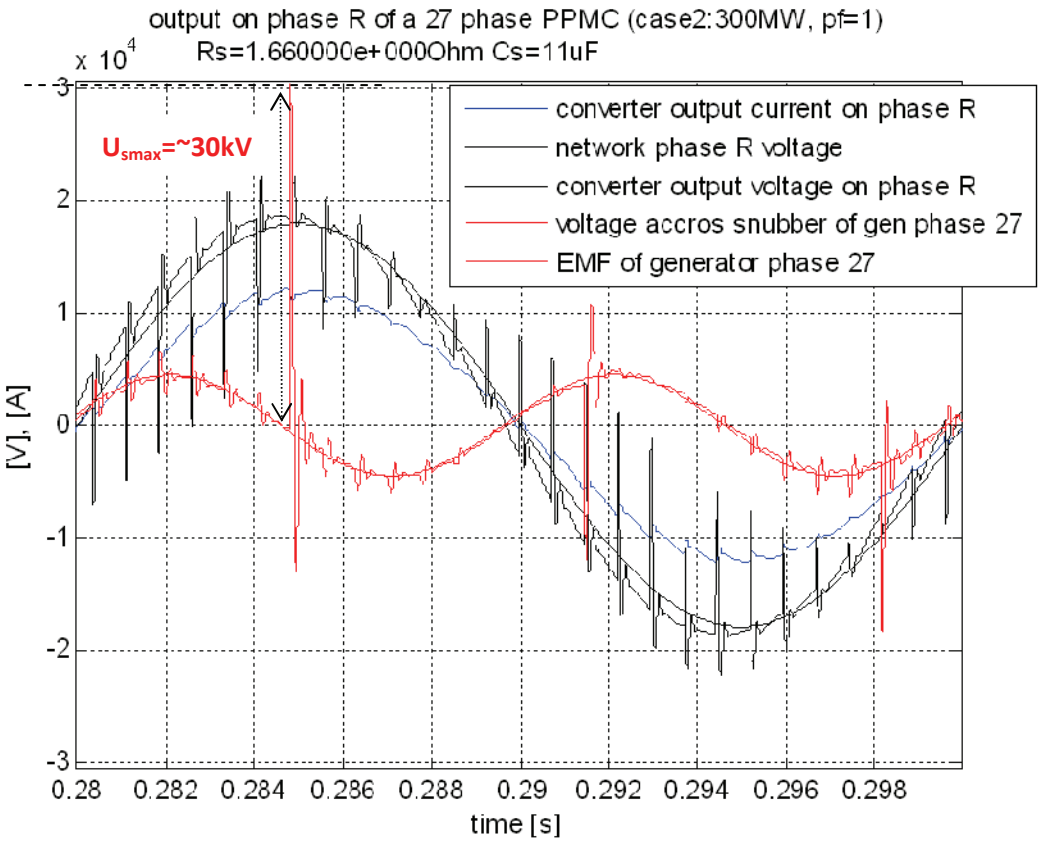


Fig. 4.24 – General simulation results for case 1, "switch" design and operating point #1

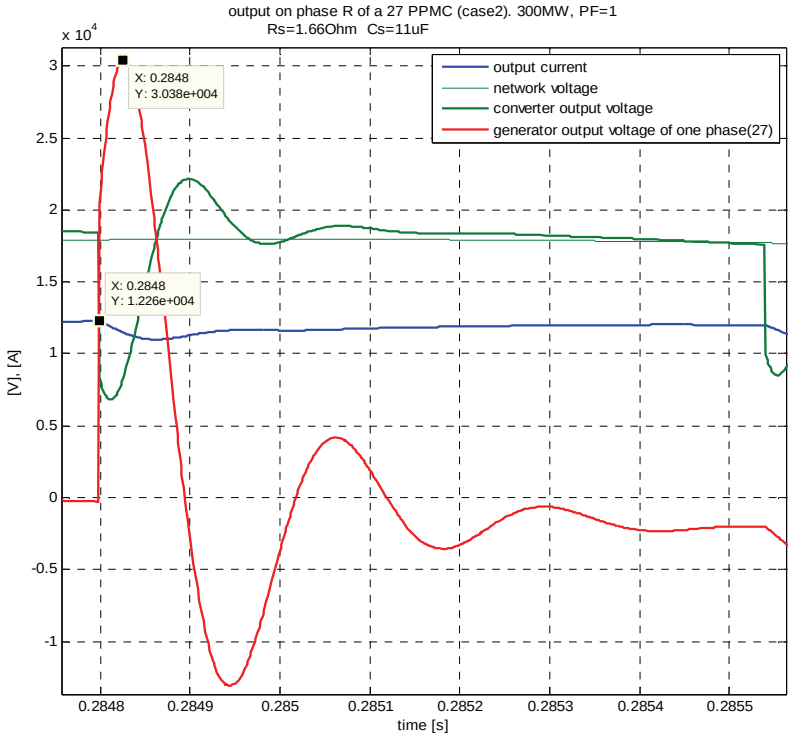


Fig. 4.25 – Closer view on forced commutation of Fig. 4.24

A second simulation result for case 1 with a snubber designed with the ”generator winding” constraint and operating point 1 is shown is Fig. 4.26. The legend of Fig. 4.26 is the same as for Fig. 4.24. Again, the first commutation that is be observed on V_{s27} is linked to the output phase R and is the one of interest here. This commutation occurs at the peak value of output current I_{opeak}, but with an initial snubber voltage that is null because power factor is unity. Again, it can be observed that for the commutations adjacent to this one the transient response is much smaller. This shows that the main assumption of “single active snubber per commutation cell” is reasonable.

Compared with the results of Fig. 4.24, it can be observed that the more severe snubber design of Fig. 4.26 effectively reduces the magnitude of peak snubber voltages which also reduces the magnitude of the ripples on the converter output voltage V_{cR}. However, the transients are less damped which lead to longer responses that still affect sensibly the output current and also the converter fundamental output.

Fig. 4.27 shows a closer view over the commutation of interest. The magnitude of the peak for this commutation is about 7400V. If referred to the ΔV_{peak} of 4.2kV this gives a v_{smax}=1.76pu. According to the theory developed in section 4.2.5 about effective peak voltage, for this commutation occurring at φ_c=97°, v_{smax} should be equal to 1.55p.u. The error is 13% which is not satisfying. This is probably due to the error on the current at commutation time which is higher than the expected target value. Again, an analysis on the effective base resistance is performed here.

$$R_{base,effective} = \frac{4.2kV}{12.4kA} = 0.338\Omega \;\Rightarrow\; c_{s,effective} = 1.05 \cdot c_{s,design} \;\Rightarrow\; v_{smax,effective} = 1.98$$

By taking into account the correction of section 4.2.5 with φ_c=97°, $v_{smax,effective}$ is 1.83p.u.shifting the error to a reasonable value of 4%.

The settling time of the transient response can also be compared with the theoretical prediction. Only the order of magnitude is of interests here. For case 1, with this snubber design, t_s is theoretically equal to 2.2ms, which is almost three commutation period T_c. At a first glance at Fig. 4.26 this value is correct.

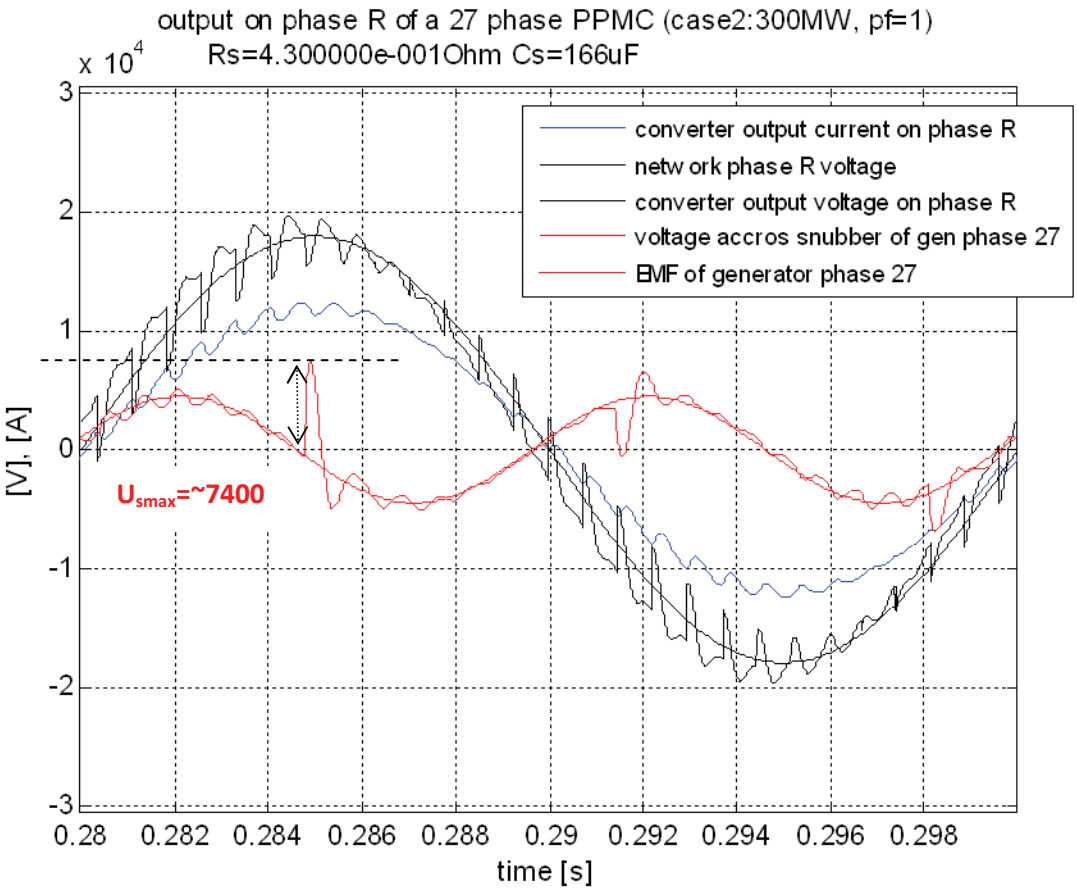


Fig. 4.26 - General simulation results for case 1, "generator" design and operating point #1

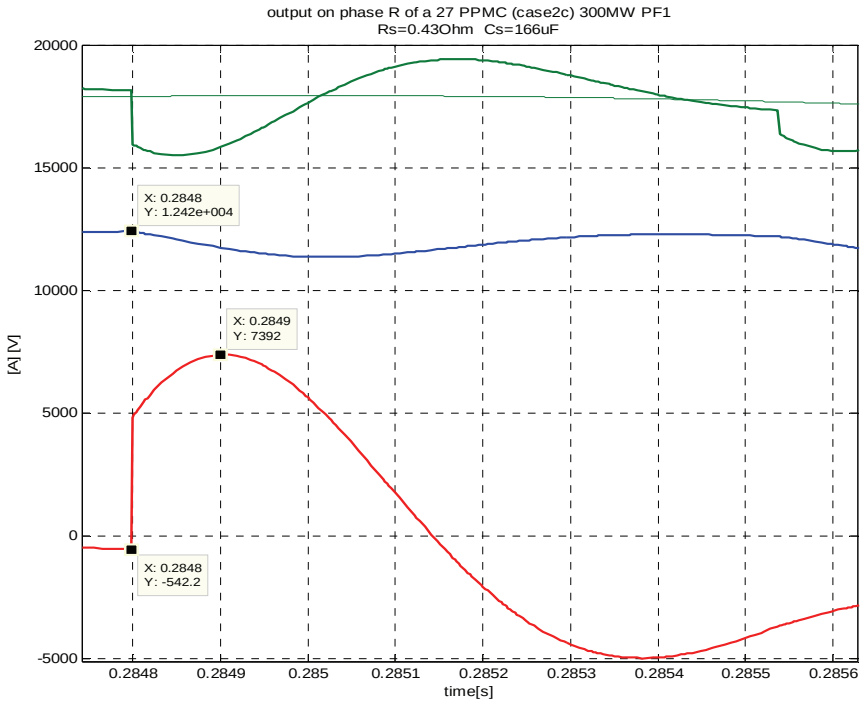


Fig. 4.27 – Closer view on forced commutation of Fig. 4.26

A third simulation result is shown in Fig. 4.28. This time, it is a simulation of case 2 with the "generator" constraint for the snubber design and with operating point #1. The forced commutation of interest is the same as in both previous results. It can be observed that the peak value of Vs is similar as case 1 with same snubber design constraints. Therefore the analysis of the peak value will not be repeated here but it can be concluded that the design method is robust when generator parameters are changed. Besides, it can be observed that the settling time of the transient response after a forced commutation is divided by two compared to case 1 with identical snubber design constraints. The theoretical value if t_s is 1.1ms, i.e. one and a half commutation period T_c, which is the case that can be observed on Fig. 4.28. In a qualitatively way, the aspect of the converter output voltage V_{cR} is better for case 2 than for case 1 for the same snubber design constraint, just because of the higher damping rate of the response after a forced commutation. Hence, reducing the parameters L_g (or increasing i_{short}) of the generator helps to reduce the installed capacitor and also helps to reduce the distortion of the converter output.

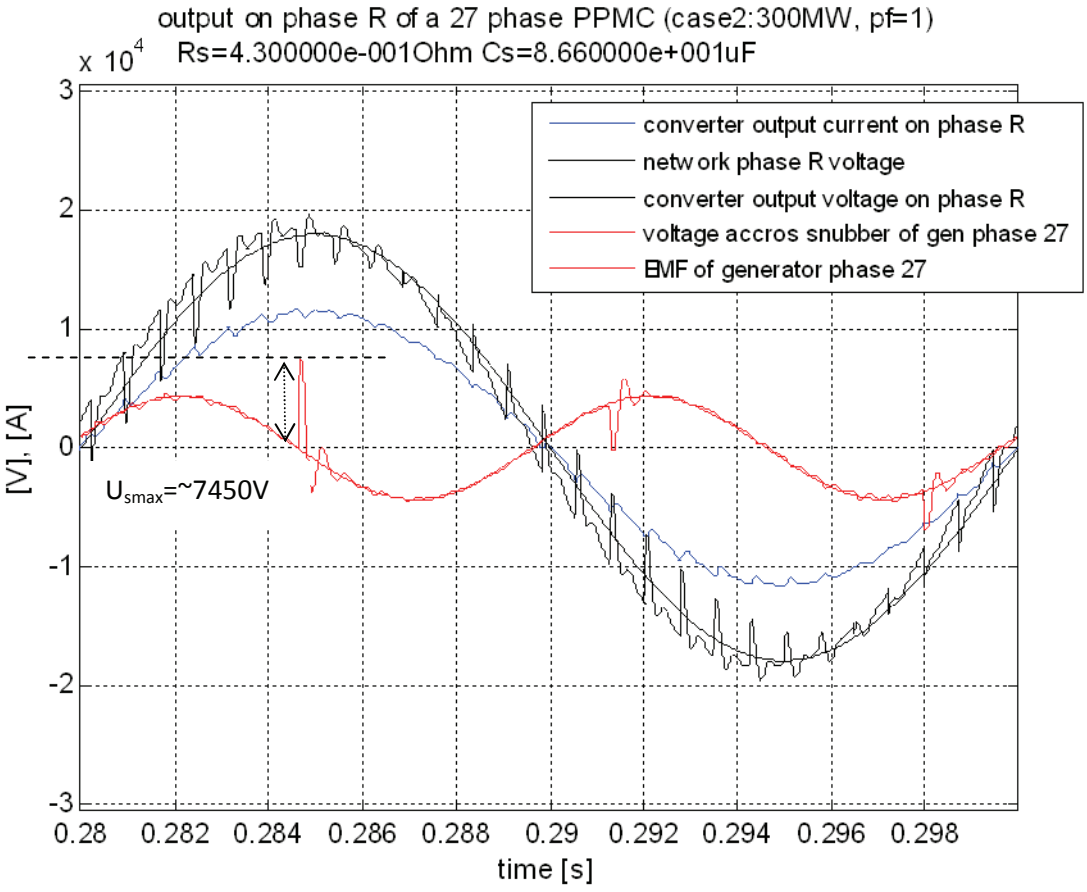


Fig. 4.28 - Simulation results for case 2, "generator" design and operating point #1

4.7 Case study to illustrate the energetic properties of the snubber

The theoretical predictions of section 4.5.5 are checked with the simulation results of the case study. Both the full forced mode and the mix mode are handled in the next two paragraphs.

4.7.1 Full forced mode

Table 4.6 presents a comparison of losses prediction and the losses computed with the simulation results. The local losses and the overall losses are shown. For computation of local losses, the waveforms as depicted in Fig. 4.29 are used. The integral of the snubber square current is computed for the duration of the transient, i.e. the integral is computed for the whole period T_c. Then this integral is multiplied by the snubber resistor Rs. For the snubber overall losses this is the same procedure but the integral of the square snubber current are calculated for each 27 snubber and along three output period T_o, which helps to cancel power oscillations and low sub-harmonics phenomena.

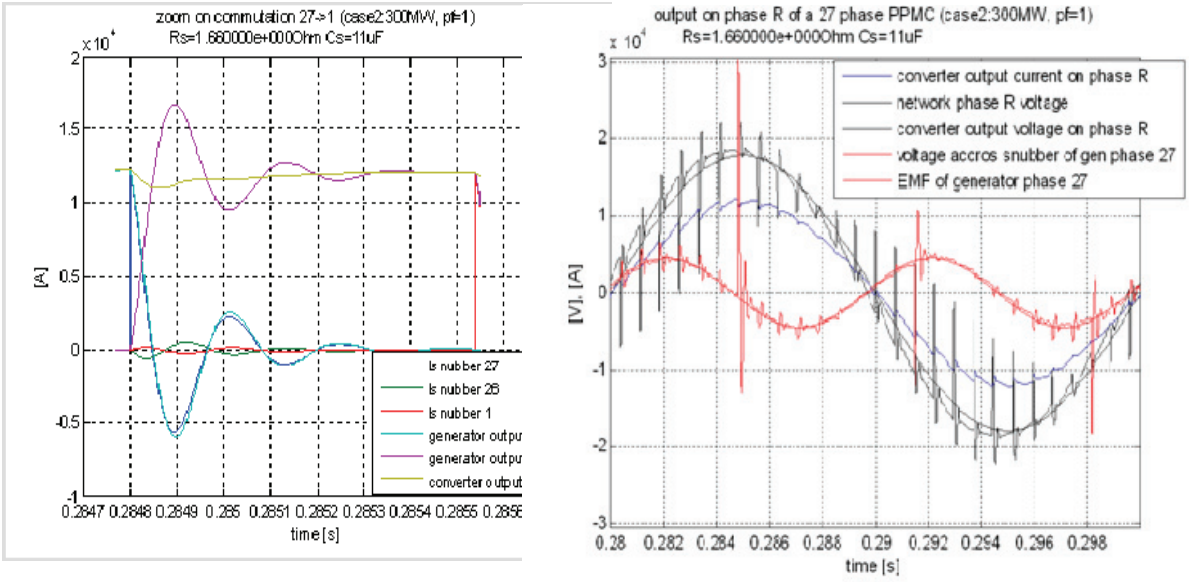


Fig. 4.29- Example of waveforms from simulation results used for snubber losses evaluation

Table 4.6 presents four simulation results. The results a) and b) corresponds to generator parameters case 1 (see chapter 3). Result a) has a snubber design with the "switch" constraints. In result b), only the design of the snubber changes and takes the "generator windings" constraints. More precisely, in b) v_{sMax} is 3p.u. instead of 8p.u.. This increases C_s and decreases a bit R_s but, as the theory predicts, it does not change the losses (only the no load losses). In c) the generator leakage inductance L_g is two times smaller than in a) and b), which is generator parameters case 2 (see chapter 3). The design of the snubber still imposes v_{sMax} to 3p.u. Consequently, losses are divided by two, as the theory predicts. The last result d), design of snubber and L_g similar to b) but with half load. Consequently, losses are divided by 4 compared to the nominal case.

Table 4.6 – Losses analysis. Comparison between theory and simulation

	Op. Point [MW] (pf=1)	Lg [μH]	No load current [Arms]	I_{o1rms} simulation fundamental [kA]	I_{oMax} simulation [kA]	**Local losses in R_s (1 commutation at I_{oMax}) [kJ]**		**No load losses [MW]**	**Losses in all Rs for 1 ouput period** (100% forced com, N=27, T=0.02s) [kJ] | [MW] | **[%** of the load**]**	
						Theory (@ meas. I_{oMax})	Simulation		Theory (@ meas. I_{o1rms})	Simulation
a	317	117	21	8.3	12.2	8.3	7.7	0.02	314 | 15.7 | **5.0**	333 | 16.6 | **5.3**
b	322	117	325	8.5	12.4	8.6	7.8	1.25	354 | 17.7 | **5.5**	385 | 19.3 | **6.0**
c	308	58	168	8.0	11.7	3.8	3.7	0.33	152 | 7.6 | **2.5**	166 | 8.3 | **2.8**
d	137	117	325	3.6	5.3	1.6	1.5	1.25	85 | 4.3 | **3.1**	93 | 4.6 | **3.3**

Those tendencies are observed for the local and the overall snubber losses. Although there is a satisfying match between theory and simulation, there are some systematic errors. For local losses, the simulation is systematically about 8% lower than the theory. Besides, one main assumption is that 100% of the load current flows through the active snubber of the commutation. However, in practice this is not the case and there is always a part of this current that flows through the adjacent snubber. Hence the theoretical local losses are always higher however this is a conservative behavior that is accepted here. Another less significant explanation for this systematic error is probably due to the fact that, due to design constraints, the value of R_s does not guarantee enough damping of the transient until the next commutation, what is not considered by the theoretical formula.

The overall snubber losses computed from the simulations are systematically greater than the theoretical calculations (which also includes the no load losses). This is due to the fact that the commutations do not occur on the fundamental value of the output current but on the real output current value, containing ripples, which are slightly higher than the value of the fundamental, whereas the theoretical calculations are based on the fundamental of the output current. The ripples of the output current can be observed in Fig. 4.29 right.

Finally, Table 4.6 gives the losses of the snubber relatively to the delivered output power. Fig. 4.30 shows the output power, delivered to the grid and the power oscillations due to transient response of forced commutation and their consequence on the load current. Consequence and significance of those power oscillations in terms of power quality and acceptability are not discussed here even though this is a critical point. Simply, the mean output power is taken for the calculation of the relative snubber losses. It can be that the relative snubber losses shown in Table 4.6 corresponds well to the theoretical calculation of Fig. 4.23.

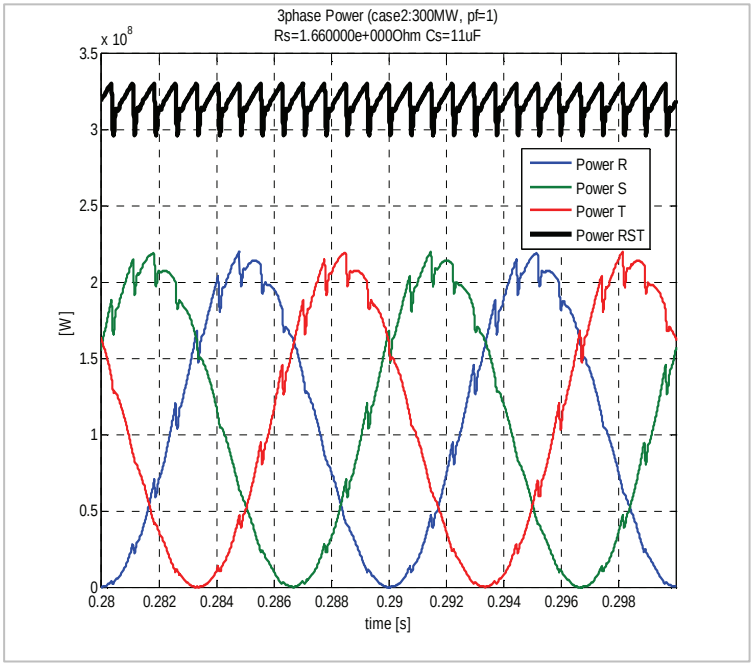


Fig. 4.30 – Waveforms of total converter output power and each of the three components

4.7.2 Mix mode operation

The next simulation result illustrates the mix mode operation of the PPMC. The simulation results are used here to extract the local and overall snubber losses to compare them with theoretical calculations. Before analysis of the snubber losses it is important to give a few words about mix mode operation of the PPMC. For this mode it is necessary to have a variable delay between step 2 and step 3 of the four steps commutation rule. It must be variable because it must be adapted to the type of commutations. For the forced commutations, this delay is set to a small value which is a dead time for safety of the switches. For the natural commutations, this delay must be set at least equal to the duration of the natural commutation. In the following simulation, the value of the delay for the natural commutations has been set to 500µs, according to calculation about the natural commutation duration in chapter 3. An example of a simulation of the PPMC running in the mix mode is depicted in Fig. 4.31. This simulated case have the same nominal values as the case study introduced in chapter 3. The generator corresponds to case 2 (i_{short}=10p.u.). However, the design of the snubber is a bit different than the design based on the "generator windings" constraint. The constraint on v_{sMax} has been set a bit lower for the present case. It is set to v_{sMax}=2.5p.u.The corresponding relative snubber capacitor c_s is equal to 0.3. There are no particular consequences due to this severe snubber design however, it can be said that this design reaches the beginning of the zone where early cut-off phenomenon have value that could reach 10% of the nominal current. This phenomenon can be observed in figure Fig. 4.32. The results of the overall snubber losses analysis will show that even with this phenomenon, the theoretical calculations are satisfying.

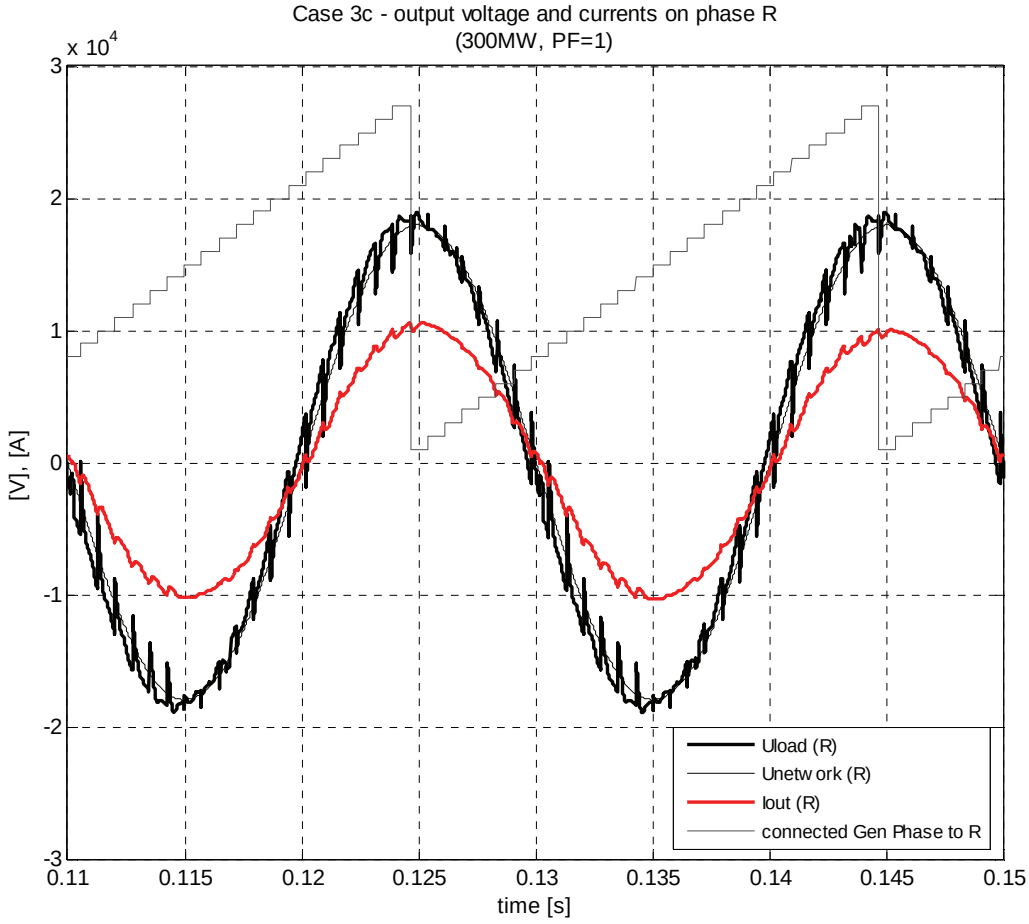


Fig. 4.31 – Simulated output waveforms of PPMC running in mix mode

Local losses of snubber under natural commutation

A natural commutation is chosen with a driving voltage that is half of the peak value. Fig. 4.32 (top and bottom) shows the details of this natural commutation. The numerical results of the losses analysis for this commutation are presented in Table 4.7. There are two parts to consider for the losses evaluation of a natural commutation: the discharge and the recharge of the capacitor of the snubber. To compute the local losses of this commutation, for both parts, the integral of the square of the snubber current involved in the commutation is computed from the simulation results. Then a multiplication by R_s gives the energy lost in it. For the theoretical calculation, the simple formula of the energy in a capacitor is taken (Equ. 4.61). However, a special attention must be paid when determining the value $\Delta V_{discharge}$ since this commutation is an early cut-off occurrence. Indeed, the discharge is not totally finished at the turning off instant of the outgoing diode, and the residual energy in the capacitor at the end of the discharge period is taken into account and deduced from the result of Equ. 4.61. For the recharge part, the value of the final capacitor voltage $\Delta V_{recharge}$ is taken as the driving voltage at the instant (126.98ms) of beginning of the recharge response, i.e. 3000V. This is an approximation because, as it can be observed in Fig. 4.32 (bottom) the transient response of the recharge has not a negligible duration compared to the generator period T_g, the real final recharge voltage of the capacitor is higher than 3000V, it is 3800V. However, for the calculation of the energy lost in R_s it is only the free response of the transient regime that is of interest and not

the forced response, the forced response being accounted in the snubber no-load losses. Also, for the recharge, the fact that the capacitor has not a null initial voltage is taken into account for the specific theoretical calculation of these losses. Indeed, the losses through R_s for a recharge with a non null initial voltage cannot simply be computed with the difference of initial and final energy since the voltage source that drives the recharge also takes part of the process. If initial voltage is given as a fraction of the final voltage $V_{final}=\varepsilon V_{init}$ the losses through Rs are given by Equ. 4.77. This method is used for the calculation of the result presented in Table 4.7

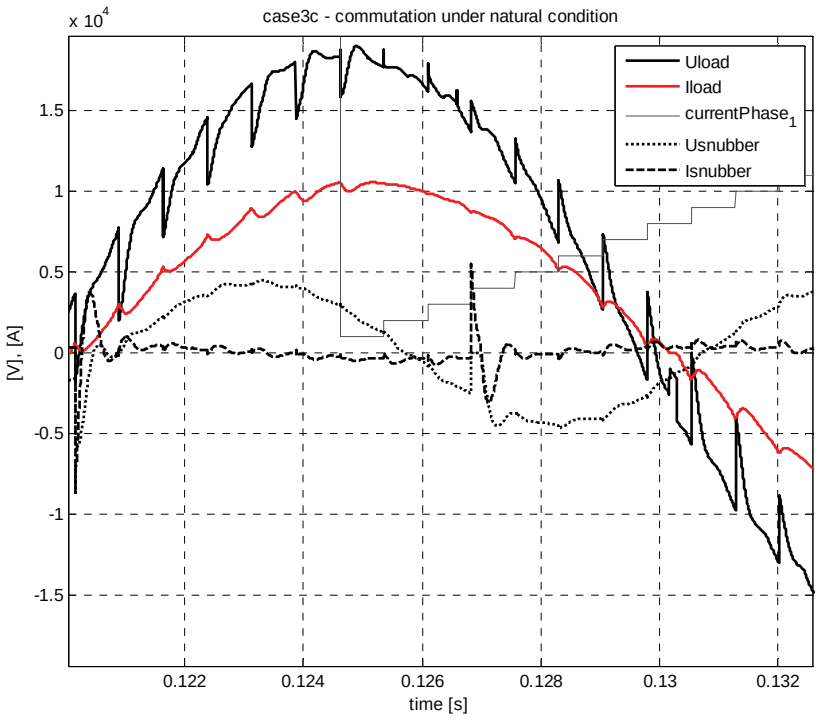
Equ. 4.77

$$E_{loss,recharge} = \frac{1}{2} C V_{final}(1 + \varepsilon^2 - 2\varepsilon)$$

Table 4.7 – Numerical values of parameters and results of local snubber losses analysis

	Initial V_s [V]	Initial snubber current [A]	Initial capacitor voltage [V]	Final capacitor voltage [V]	E_{loss} [J]	
					Theory	Simulation
Discharge	2515	300	2386	274	468	445
Recharge	0	638	274	3000	616	673
Total					**1084**	**1118**

As can be observed from Table 4.7, the correspondence between theory and simulation is satisfying although there are some discrepancies. Concerning the discharge, the theory is 5% above simulation. Concerning the recharge, the theory is 10% below the simulation. The error for the discharge can be partly explained by the fact that the value computed from the simulation also contains energy losses due to the no load current. However it is not wished to push the local analysis further since the overall losses are more important to verify.



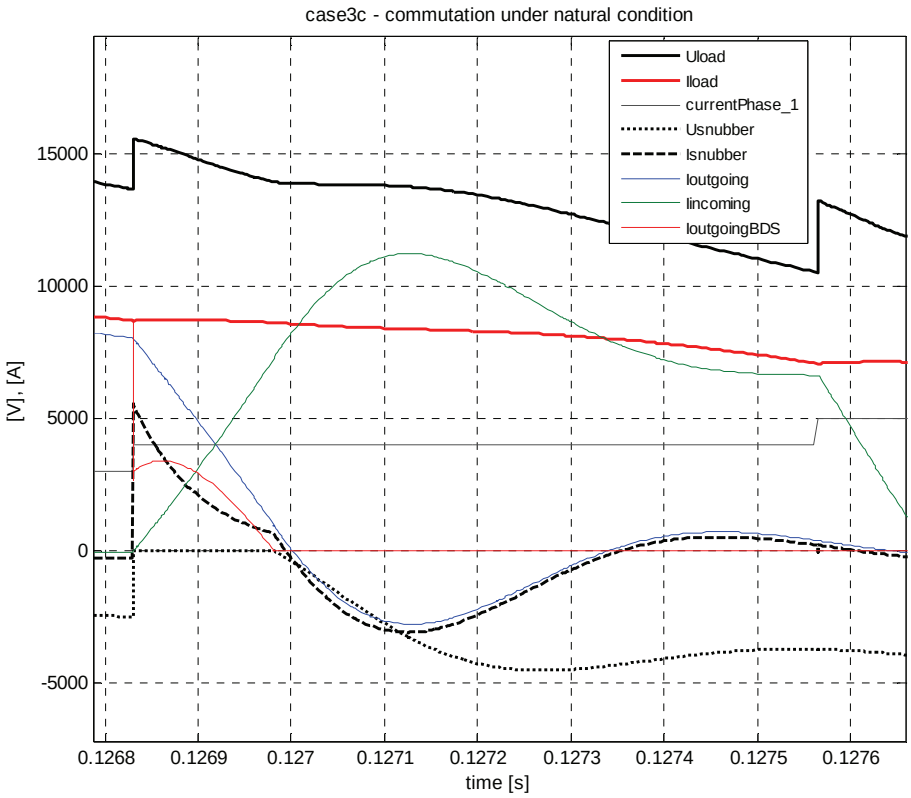


Fig. 4.32 – Waveforms of natural commutation used for local losses analysis

For the overall losses, as in the previous paragraph, for each snubber current, the integral of the square of its current is computed for three output periods, multiplication by R_s gives the lost energy through all 27 R_s. The total snubber lost energy computed with simulation is **112.9kJ.** In these losses are included the no load losses, which are about 1.13MW per output cycle of 0.02s which corresponds to an energy of 22kJ. One particular comment can be done about the distribution of losses among the 27 snubbers, which is given by Fig. 4.33. The simulated case has a precise and integer frequency ratio of 0.5, which corresponds to a stationary case. The discrepancies of losses per snubber can reach a ratio of 2, which means that in practice, such an operating frequency ratio should be avoided or the snubber thermal properties must be designed for a worst case.

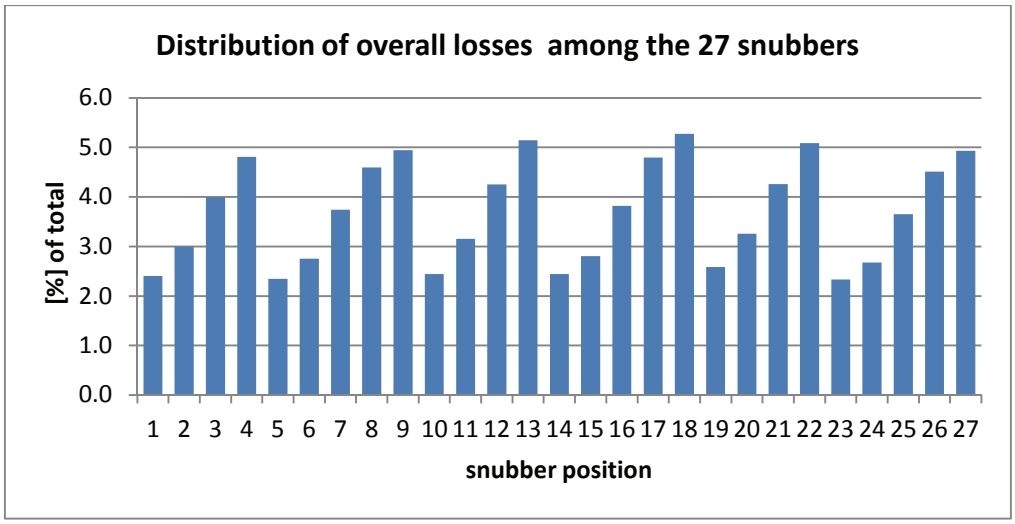


Fig. 4.33 – distribution of overall losses among the 27 snubbers

The theoretical predictions are calculated in two steps, as proposed by Table 4.8. The first step consists in calculating the losses as if the converter was running in full forced commutation mode. The rms value of the fundamental output current is computed from the simulation results. Knowing the inductor L_g and using Equ. 4.62 (b), the losses in full forced mode are straightforward. The second step is to determine a correction factor that represents the mix mode operation. This correction factor comes from an abacus similar to Fig. 4.22 but specially computed for the specific values of the snubber design. This specific abacus is shown by Fig. 4.34 and the correction factor read from it is equal to 0.72. Table 4.8 gives the numerical value of the corrected losses, which is equal to 90kJ.

Table 4.8 – Numerical values and steps for theoretical calculation of snubber losses in mix mode

Full forced E_{loss}	
I_{orms} [A]	7260 (value taken from simulation results)
N	27
L_g [µH]	58
$E_{loss\ fullforced}$ [kJ]	**124**
Correction factor for mix mode Eloss	
EMF_{rms} [V]	3060 (value taken from simulation results)
R_{base} [Ω]	0.42
C_{base} [µF]	325
C_s [µF]	166
R_s [Ω]	0.43
c_s	0.51
r_s	1.02
$c_{s,design}$	0.3
$r_{s,design}$	1.3
$v_{sMax,design}$	2.5
Loss correction for mix mode	0.72
Eloss, mix [kJ]	**90**

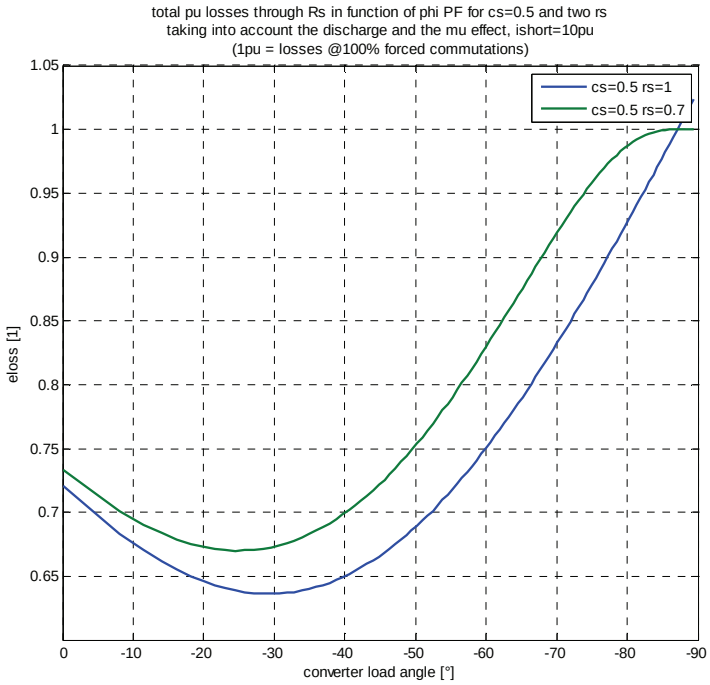


Fig. 4.34 – Losses correction factor for mix mode operation, specific for case study

Finally, Table 4.9 compares the theoretical results with the simulation results with the fraction of the losses into no-load and commutation part. Table 4.9 shows an excellent concordance between theory and simulation.

Table 4.9 – Comparison of overall snubber losses obtained with theory and with simulation

Overall snubber losses E_{loss} [kJ]		
	Theory	**Simulation**
No-load	22	22
commutation	**90**	**90**
Total	112	112

4.8 Alternative solution for snubber circuits

In chapters 3 and 4, the free-wheeling path required for the forced commutation is a resistive-capacitive leg. This is a simple passive solution. There are however many other possibilities that can be imagined. The RC snubber solution is simple but there is no way to recover the energy contained in the generator inductance Lg, which is entirely dissipated through the snubber resistor for each forced commutation. There is another category of free-wheeling path that can be called “rectifying bridge” free-wheeling path that can allow a energy recovery. An example of this solution is illustrated in Fig. 4.35 for a 6x3 PPMC. It is an *m* pulse rectifying diode bridge that rectifies the m generator phases to a DC voltage V_{DC}.

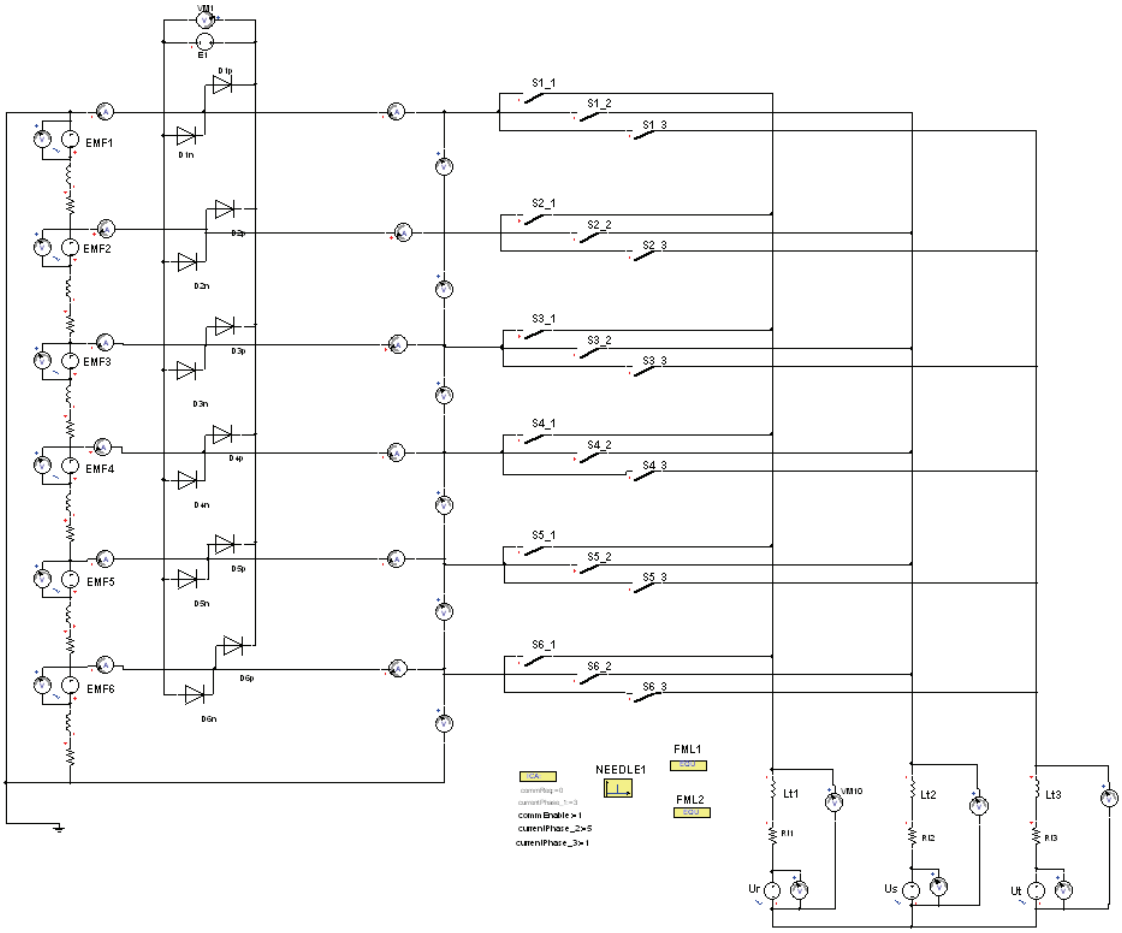


Fig. 4.35 – Active rectifying bridge as protection circuit for the PPMC

When a forced commutation occurs on one generator phase, the two diodes of the bridge involved in the commutation cell will close and conduct the load current. The voltage V_{DC} provides the necessary driving voltage that decreases the outgoing current and increase the incoming current to perform the commutation. This is illustrated in Fig. 4.36.

On the DC side, if an inverter is connected, the energy injected in the DC link at each forced commutation could be re-injected into the grid via an inverter. Therefore, it is interesting to evaluate the available power that could be re-injected.

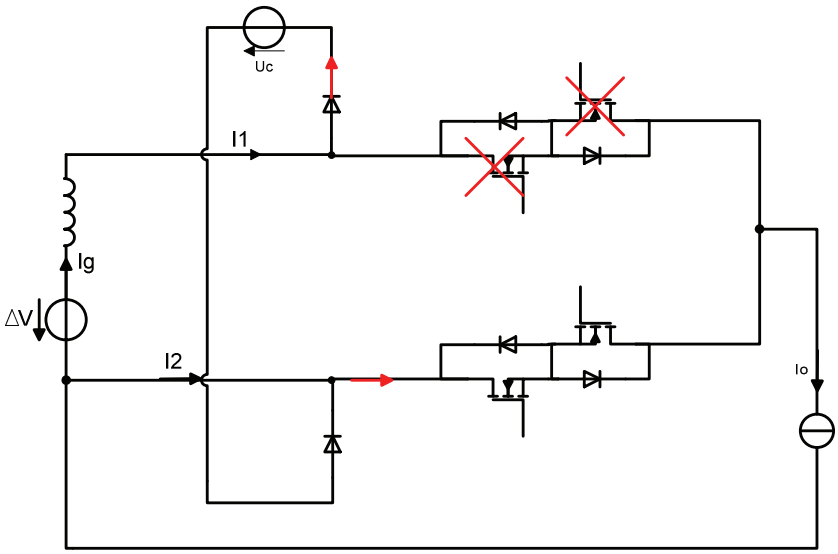


Fig. 4.36 – Commutation cell with active rectifying bridge

As it is a rectifying bridge, the DC voltage V_{DC} is at least equal to $2V_{c,peak}$, two times the peak value of the generator phase voltage $V_{c,peak}$. For a high value of m, e.g. 27, this means that $V_{DC} \approx 8\Delta V$. The voltage VDC is supposed to be constant, this implies in practice a regulation of this voltage by the optional injecting inverter or by a DC/DC converter. With those two assumptions, the current derivative of the outgoing, resp. incoming current is constant because the variation of ΔV in front of the constant V_{DC} is negligible. The estimation of the energy that is injected into the constant VDC source during one forced commutation is then straightforward.

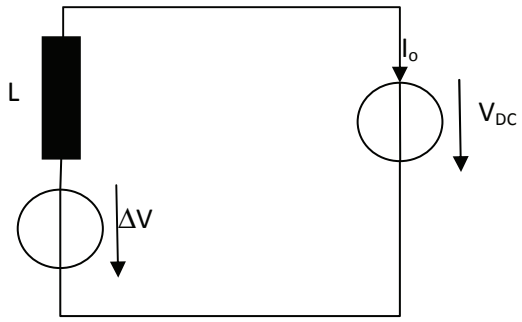


Fig. 4.37 - Circuit with split emf and snubber sources

At the beginning of the transient regime, t_0, the initial current of the inductor is I_o. The transient regime stops at t_{end} when the current in the inductor is null. Developpement for the case Us=emf+ ΔUs:

Determination of Δt

$$U_{emf} - Us - L\frac{dI}{dt} = 0$$

$$\frac{dI}{dt} = \frac{-\Delta Us}{L}$$

$$I(t) = \left(\int_{t0}^{t} \frac{dI}{dt}\,dt\right) + Io = \int_{t0}^{t} \frac{-\Delta Us}{L}\,dt + Io = \frac{-\Delta Us}{L}(t - to) + Io$$

$$I(tf) = 0 = \frac{-\Delta Us}{L}(\Delta t) + Io \Leftrightarrow \boxed{\Delta t = \frac{IoL}{\Delta Us}}$$

energy through Us during Δt

$$(Uemf + \Delta Us)\frac{1}{2} Io\Delta t = \frac{(Uemf + \Delta Us)}{\Delta Us}\frac{1}{2} LI_0^2 = \boxed{\left(\frac{Uemf}{\Delta Us} + 1\right)\frac{1}{2} LI_0^2} \geq \frac{1}{2} LI_0^2$$

In case an active snubber is used, maintaining V_s to emf+ΔV_s constant during the commutation we see that the energy dissipated through Us is more that $0.5LI^2_0$, the rest is furnished by EMF.

In practice, things are more complicated for the rectifying bridge than the simplified circuit of Fig. 4.37. When there are three concomitant forced commutations, there are six diodes that are active. The derivatives of the current in these diodes are not all equal. The assumption above considered that the current derivative is proportional to the V_{DC}. However, each of the six derivatives are modulated by their corresponding EMF hence, within one pair of diodes of one commutation cell, one of them will turn off before the other. As a consequence, the circuit must be redefined and the derivatives are all different than the initial situation. The simplified evaluation of the energy that could be re-injected is not valid any more. The precise evaluation of the injected energy is complex and heavy in calculation and a lot of different cases must be handled. It will not be detailed here. Briefly, the time when a diode of the bridge turns off must be calculated, each turn-off event defines a section. For each section one must find the derivative of the diode current.

Besides, in practice, if V_{DC} is set to $2V_c$, the rectified generator voltage, the above estimation of injected energy is not valid. The diodes of the rectifying bridge that are connected to the adjacent generator phases of the one involved in the commutation cell will spontaneously turn on. These generator phases will start to inject power also in the DC link and can considerably increase the injected power compared to the simple estimation made above. In order to avoid this forward bias on the adjacent diode it is necessary to increase the DC link voltage. The detailed resolution that provides the constraints on the V_{DC} to avoid this phenomenon is not detailed in this report but it can be stated here that V_{DC} must be greater than $3U_c$. In theory, the fact that the injected power in the DC link is higher than simple prediction given above is not a problem since this power will be returned to the grid. However, the inverter responsible for this energy recovery will have to be designed according to the power to transmit and this should be kept as low as possible. Also, in theory, the increase of the voltage V_{DC} to avoid the phenomenon of diodes spontaneously turning on is not a problem. However, in practice, the increase of voltage has a cost in insulation and material.

Here is a simulation result of a PPMC with a rectifying bridge as a free-wheeling path.

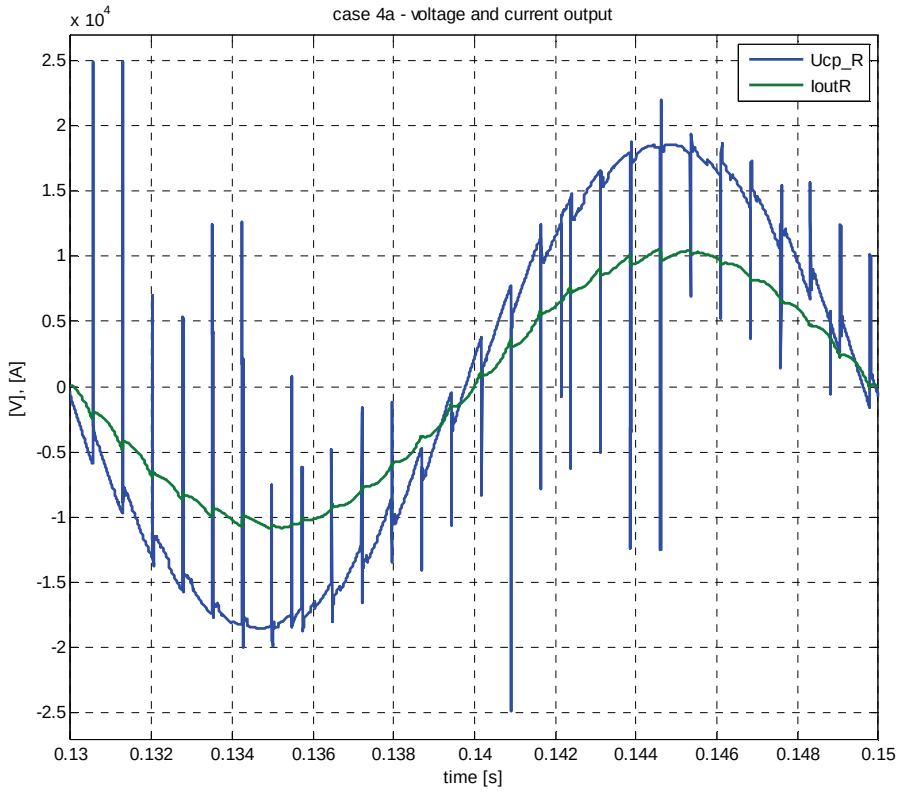


Fig. 4.38 – Simulation results of the PPMC with an active rectifying bridge

Fig. 4.38 shows the general view of the converter output phase voltage and the output current. As can be seen the overvoltage have a high magnitude that is influenced by V_{DC}. The determination of the overvoltage on the output voltage of the converter when a rectifying bridge is used has not been developed within this work. The peaks have high values but the duration of the phenomenon is relatively short, anyway shorter than when a simple, RC snubber is used. Qualitatively, the influence of those voltage excursions on the fundamental is surely weaker than those due to a simple RC snubber. The magnitude of U_{cpeak} is 18.5kV.

Fig. 4.39 and Fig. 4.40 show the dc link voltage V_{DC} along with the current flowing through this bridge. Fig. 4.40 is a zoom of Fig. 4.39. V_{DC} is constant and set to 37.2 kV. The shape of the DC link current, I_{DC} is particularly interesting and illustrates the comments made above. Each peak represents a commutation instant. It is clear that the free-wheeling path is working properly and the current derivatives are quite high, thus the commutation is quite fast in comparison with the commutation period T_c. However, it can be observed that from a certain time after the commutation instant, the slope of I_{DC} quickly decreases sand I_{DC} reaches zero only after a time that, in some situation, is similar with T_c. This makes the simple evaluation of the injected power wrong. Qualitatively, the area under the I_{DC} curve is significantly bigger than if the derivative of I_{DC} stayed constant.

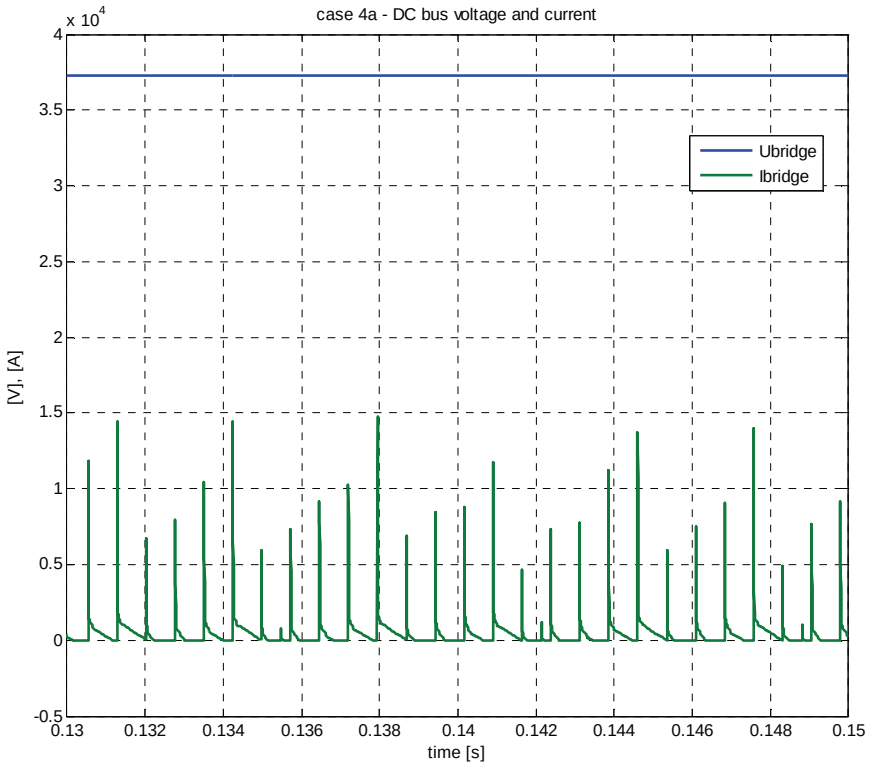


Fig. 4.39 – Waveforms of the current through the DC link of the rectifying bridge

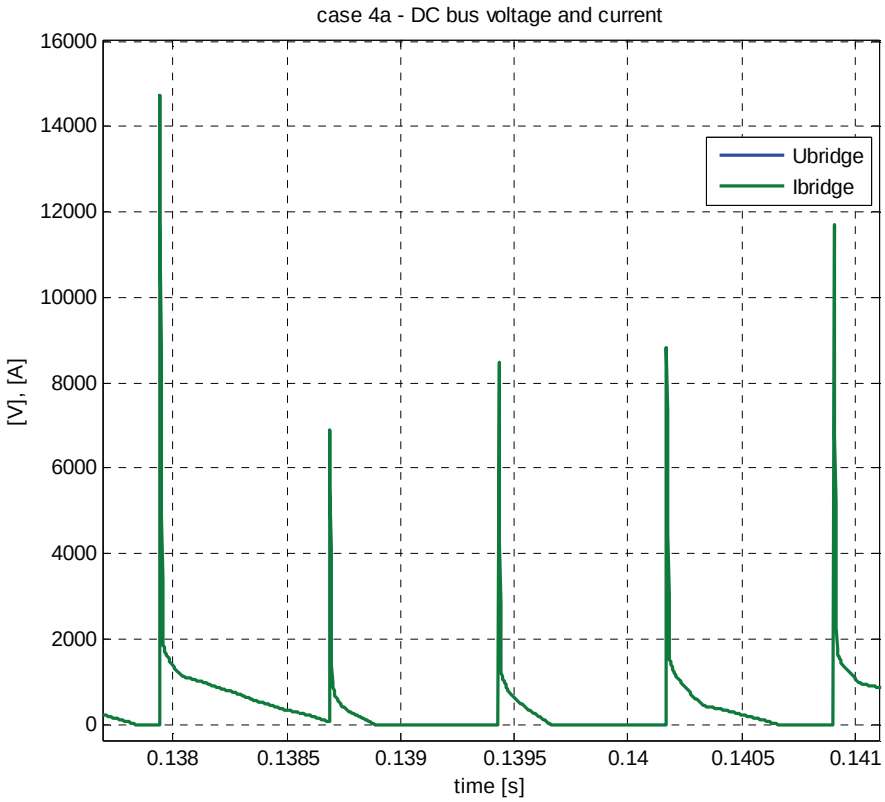


Fig. 4.40 – Closer view of Fig. 4.39

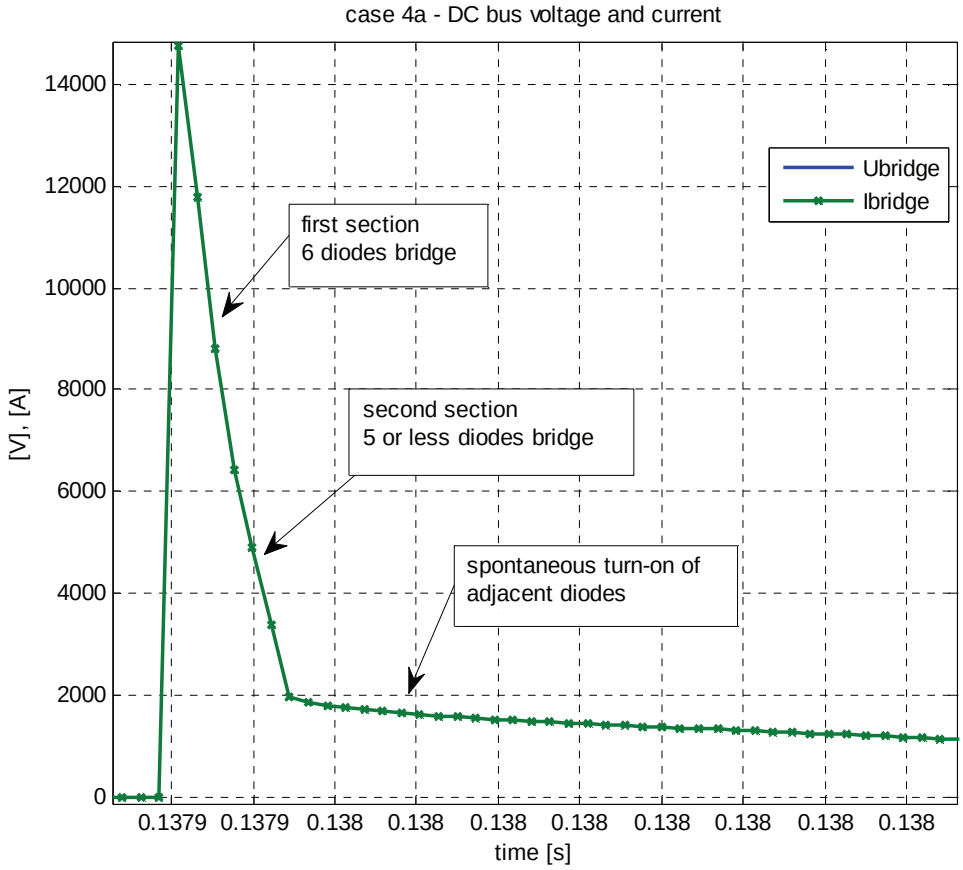


Fig. 4.41 – closer view of Fig. 4.40

Finally Fig. 4.41 shows another zoom of Fig. 4.39 to highlight both phenomena that influence the simple evaluation of the injected energy in the DC link. In Fig. 4.41, three sections can be observed. The first one, with a high slope of I_{DC} is the normal operation of the rectifying bridge, with six diodes active. The second section, that starts at an elbow on the I_{DC} curve, corresponds to the turning-off of one or several diodes because the current crossed zero. The third section, which beginning is marked by a serious slope change on the IDC curve, illustrates the spontaneous turning on of the some adjacent diodes. These diodes turn on even if V_{DC} has a greater value than $2U_C$. This creates additional current that is injected in the DC link. This current evolves with the frequency of the generator, which explains that this phenomenon lasts much longer than the commutation phenomena.

4.8.1 Active snubber

A more intelligent free-wheeling possibility would be to have an active snubber that would act as a controlled voltage source which could emulates the RLC response for example but would re-inject this power through inverters with, of course, an isolation stage in-between. The potential of energy that would be re-injected is given by Equ. 4.62 (b) where the right term is a low limit. This solution is not developed in this work but will be a part of the future work mentioned in the conclusion, chapter 7.

Chapter 5 – Command and control of the PPMC

5.1 Introduction

As in the AG configuration the converter is placed directly between the generator and the load, it is required that the converter controller is able to impose an operating point onto the load which is an AC grid. In other words, the converter must impose independently the active (P) and reactive (Q) power levels as the operator of the power plant wishes. A positive P is a power that goes from the AG to the network (generating mode). A positive Q means that the load is consuming reactive power, i.e. the output current lags the grid voltage. If the frequency converter is responsible for the control of P, this gives an operating speed for the GT, which is computed to obtain the best efficiency out of the GT. This speed must be controlled via a speed controller that will command the gas and/or air inlets aperture to act on the mechanical torque of the GT. However this chapter will only handle the control of the frequency converter. Coordination of converter controller and GT controller is beyond the scope of this work. Fig. 5.1 illustrates this control configuration of the generation set.

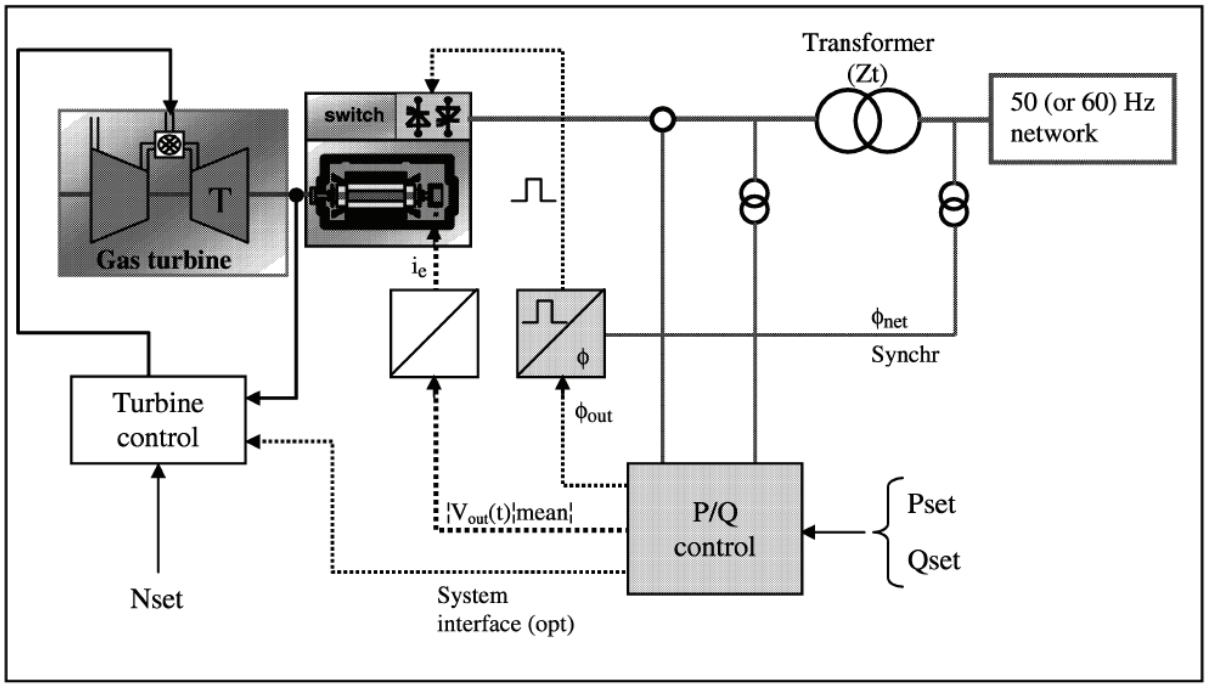


Fig. 5.1 – General control scheme of a AG generation set (source : [13])

The electrical model of the point of connection between the AG and the grid is the short circuit model of the transformer, which short circuit impedance is a known parameter, as presented in chapter 3. Besides, if the value of the transformer impedance is not enough, a connection impedance, mostly inductive, is added. As the total connection impedance is known and the grid spatial vector voltage supposed to be constant, a first power control, in open loop, is to compute through a spatial vector diagram the required converter output voltage $\vec{V_c}$, as presented in chapter 3. Then, the converter control must position its output voltage with the calculated phase shift and set the generator excitation current accordingly to get the calculated magnitude on the converter

output, taking into account the ratio between fundamental of the converter output and magnitude of the EMF. To be more accurate, one could include the internal impedance of the generator and other auxiliary impedances like voltage drop across switches to compute a more accurate target converter output voltage $\vec{V_c}$. However this relies on parametric knowledge of those impedances, that can only be measured with a given accuracy. If the accuracy is not satisfying, there is clearly a need for a closed loop control. Especially because transformer impedance is such that small error in phase shift between converter and network could result in non tolerable error on the output power. The closed loop can act on the converter output voltage or on the output current.

The closed loop strategy acting on the converter output voltage has been proposed and implemented by [13] on a NCMC, a converter that is very similar to the PPMC and also running with the *slowCWC* sequence (see chapter 1 and 2). It has been implemented and seems to work however precise evaluation of the performance of this strategy are not clear because of other issues specific to the NCMC, especially the delaying of some commutation instants (see chapter 2).

The closed loop strategy acting on the output current will be described in the section 5.3. Knowing the grid phase or line voltage magnitude, the required output current $\vec{I_o}$ to match a given P and Q operating point is straightforward. This gives the set values of the closed loop control. Then the controller sends the required set values $\vec{V_c}$ to the converter.

Generally, the second strategy is preferred for the following reasons:

1) The current control is less sensitive to precision on transformer parameters. It only affects the dynamics of the regulator but not the steady state error between wanted value and measured power. In the voltage control, only the voltage magnitude and phase of the converter's output are controlled to match the target value, but it does not guarantee that the output current match the wanted value since it depends on the transformer impedance. The voltage control would require a second control loop on the power wanted component to ensure the correct output power
2) For the PPMC, measurement of output current is easier than output voltage since its ripple components are already filtered by the transformer and connection impedances.

For the PPMC, the current control strategy is advised here. The complete solution and design of the controller will not be presented in this thesis. Only the nature of the problem will be reported here and a first solution developed during a master project at LEI. Those elements can then be used as starting point to go further in a future work on control strategy for PPMC.

As the control algorithm is closely related to the command block of the converter, next section presents the command algorithm of the PPMC. This command algorithm can be used for an open loop control of the operating point.

5.2 Command algorithm of the PPMC

5.2.1 General view of command algorithm

It has been stated in the previous section that the converter must be able to position its output voltage with a given phase shift with respect to the grid voltage. Besides, it must set the excitation of the generator accordingly to obtain the required fundamental magnitude of the converter output voltage. Fig. 5.2 shows the command algorithm to achieve this open loop positioning of the converter output voltage against the grid voltage.

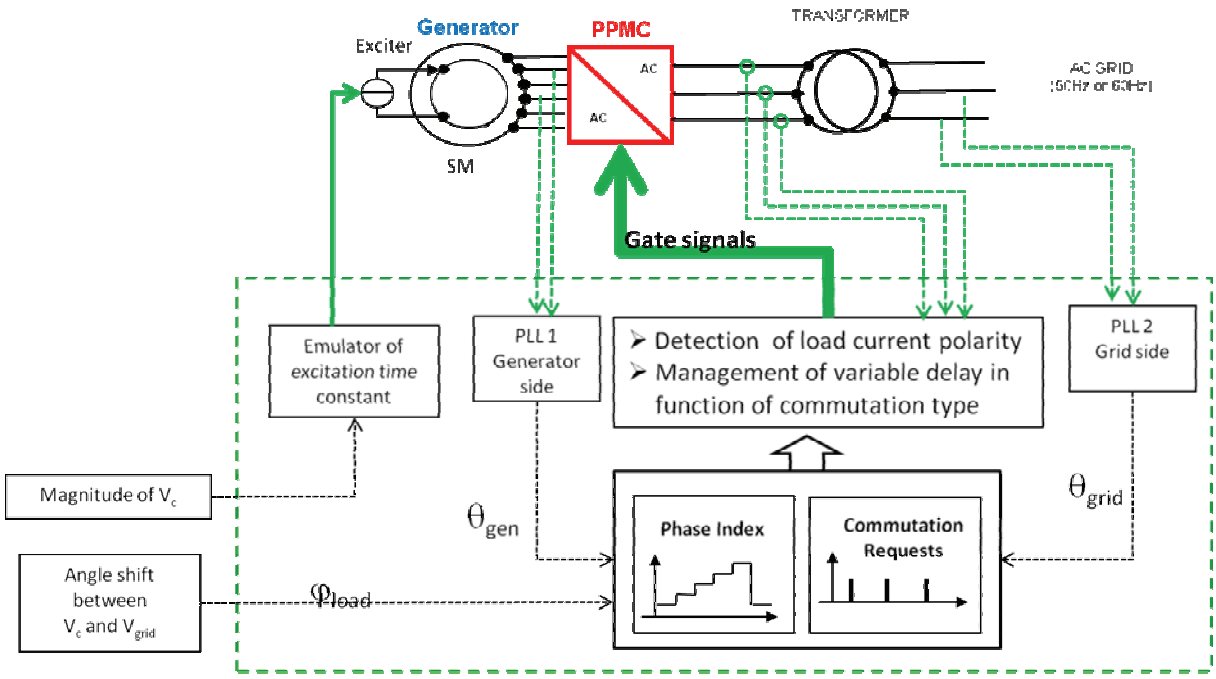


Fig. 5.2 – Command algorithm of the PPMC

As has been described in chapter 2, for ideal waveforms, the position of the fundamental of the converter output voltage is directly linked to the determination of the commutation instant. Here we remind the spatial vector chart which is used to determine the commutation instant of the slow CWC sequence. The angle error between the three phase voltage system V_{cRST} (given by the set [a,b,c]) and the target three phase voltage V_{target} should not be greater than π/m in absolute value (or be within $\pm\pi/m$). Knowing V_{cRST} and V_{target} and the fact that there is a constant phase shift of $2\pi/m$ between each set [a,b,c], one can easily compute, at any time, which set [a,b,c]) gives $V_{c,RST}$ closest to V_{target}. In order to synchronize the converter output voltage and the grid voltage, and optionally introduce a given phase shift, the target V_{target} to follow must itself be synchronized with the grid voltage. Hence, obviously, two fundamental values to know are the angular positions of the grid voltage three phase system and the generator poly-phased voltages system. For this purpose, two PLL are introduced here and will be used in the command algorithm.

5.2.2 PLL

In order to track the angular position of a three phase voltage system, one could simply measure one of them, compute the arccosine function of its p.u. value and on the base of its sign determine the angular position between 0 and 2π. However, this would be far too sensitive to noise and perturbations. Filter could be used but then the introduction of phase shift could be an issue. Zero

crossing detection could be used but is also sensitive to noise and only use two points per period. PLL is a suitable tool to track angular position of a three-phase voltage system because it gives a null steady state error and can be protected against signal perturbations.

There are plenty of PLL algorithms available, each of them with pros and cons. Usually it is a trade-off between bandwidth and dynamics performances and also computation burden. For a first command algorithm of the PPMC, a simple PLL algorithm has been chosen. It is also largely used in practice. It is a closed loop with a PI controller inside. The detailed design of the PI parameters is not given here. It is only useful to state that for the PPMC command, it is possible to find satisfying trade-off between bandwidth and dynamic response. PLL Principle block diagram is given in Fig. 5.3 left. Structural diagram of linearized PLL around locked position is given in Fig. 5.3 right.

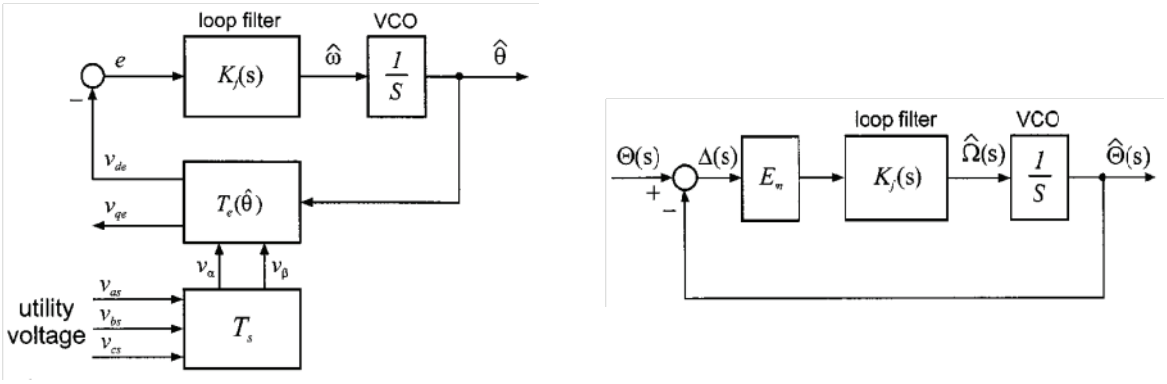


Fig. 5.3 – Block diagram (left) and linearized model (right) of PLL algorithm (source [37])

As Fig. 5.3 shows, this PLL uses three phase system, or, in case of balanced system, only two voltages could be measured and the third can be reconstructed internally. Consequences of this simplification will not be discussed here.

The reference three phase line voltages that are to be followed by the converter are known thanks to the PLL on the network side.

Let us precise how to use this PLL with the poly-phased voltage system of the generator side, since a PLL is also used on this side. A requirement for the *slowCWC* sequence is that *m* is a multiple of 3. Hence it is always possible to find a three phase voltage subsystem out of the poly-phased voltage system. This is what is done in the command algorithm of the PPMC. The PLL on the generator side is always locked to a given three phase subset $[a_0,b_0,c_0]$, for example

$$\left[1;\left(1+\frac{m}{3}\right);\left(1+2\frac{m}{3}\right)\right]$$

This PLL gives then the angular position of the corresponding three phase output line voltage produced by the converter if this set represents the active phase connected to the load.

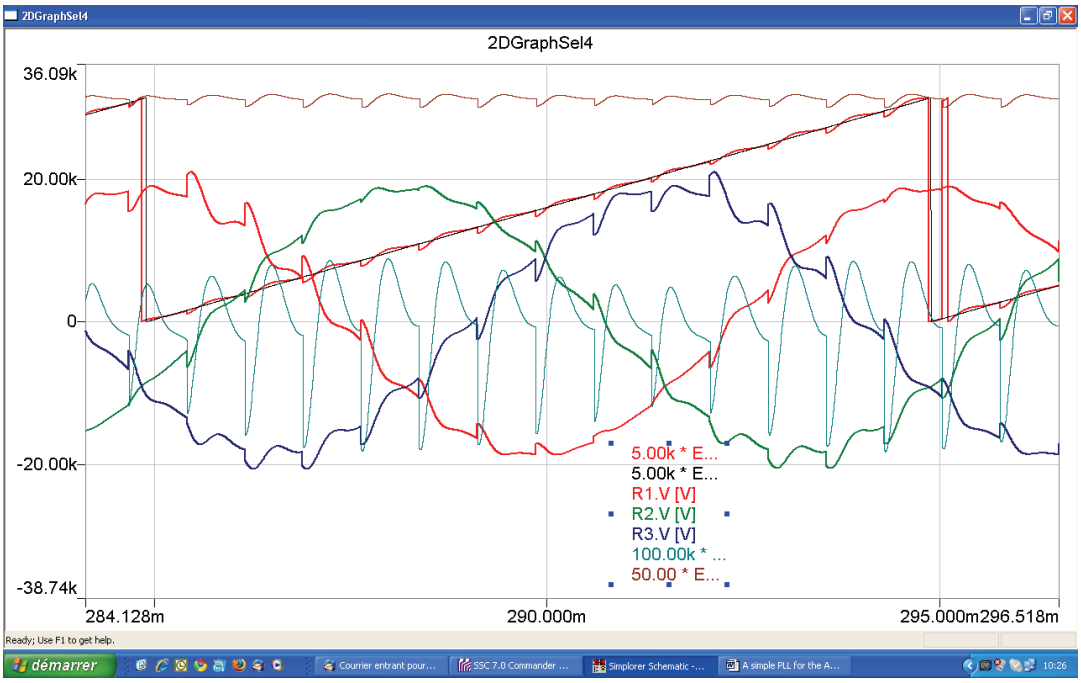


Fig. 5.4 - Output with ω_n=100Hz

In simulation, one could lock the PLL 1 (generator side) on a set [a,b,c] of ideal EMF of the generator. However, in practice, those EMF are not accessible and physically not measurable. However, the fact that the PLL 1 is locked on set [a,b,c] of the real stator voltages is better since it represents the real angular position of the converter output. Besides, it will automatically adapt to the effect of the voltage drop and phase shift across stator winding impedance Z_{gRST} due to load current.

5.2.3 Determination of input phase index

The converter command has to choose the set of connection [a,b,c] that gives the three phase line system the closest to the target three phase line voltage, the closest in terms of **angle**. This is equivalent to say that the angular error between the target and the selected generator phases must be within the interval $\left[-\frac{\pi}{m};\frac{\pi}{m}\right]$. From the output of both PLL based on the set $[a_0,b_0,c_0]$ it is possible to compute the error $\Delta\theta_{gen0}$. The other (m-1) angular errors are simply deduced from this one by adding $j\frac{2\pi}{m}$ with 0 < j < (m-1), an integer number. The algorithm simply has to compute the value of j that shifts $\Delta\theta_{gen}$ within the $\left[-\frac{\pi}{m};\frac{\pi}{m}\right]$interval. j gives the shift to add to the PLL set $[a_0,b_0,c_0]$ to obtain a V_{cRST} in phase with the reference V_{target}.

$$a = mod(a_0 + j, m) \quad b = mod(b_0 + j, m) \quad c = mod(c_0 + j, m) \quad \text{(Equ. 5.1)}$$

$$\frac{\pi}{m} > \Delta\theta_{gen} + j\frac{2\pi}{m} > -\frac{\pi}{m} \Leftrightarrow \frac{1}{2} - \frac{\Delta\theta_{gen}}{\frac{2\pi}{m}} > j > -\frac{1}{2} - \frac{\Delta\theta_{gen}}{\frac{2\pi}{m}}$$

In practice for clarity and avoidance of uncontrolled sudden jumps of $\Delta\theta_{gen}$ from negative to positive values and also obtain only positive values of j between [0;m], $\Delta\theta_{gen}$ is always mapped into the interval [0: -2π[as depicted by Fig. 5.5.

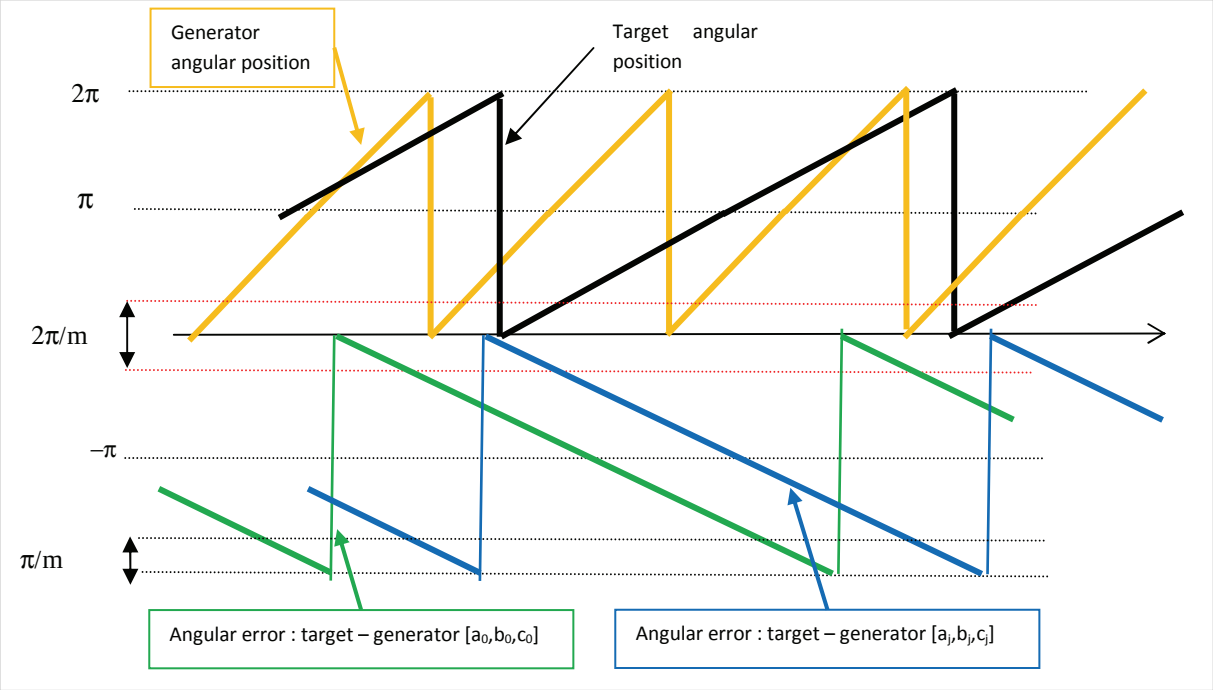


Fig. 5.5 – Construction of angular error between target and the generator for phase index determination

This algorithm is very easy to implement and execution time is equal for any input phase number *m*. Fig. 5.6 gives an example of output of this algorithm and an example of implementation is shown hereafter:

```
%Current_Phase determination

   deltaThetaGen1(k)=theta_ref(k)-thetaEst_g(k);

   if (deltaThetaGen1(k)>0)

       deltaThetaGen1(k)=-two_pi+deltaThetaGen1(k);

   end

   phaseShiftIndex=ceil(0.5-m*deltaThetaGen1(k)/two_pi);
```

```
current_phase(k)=mod(phaseShiftIndex,m);
```

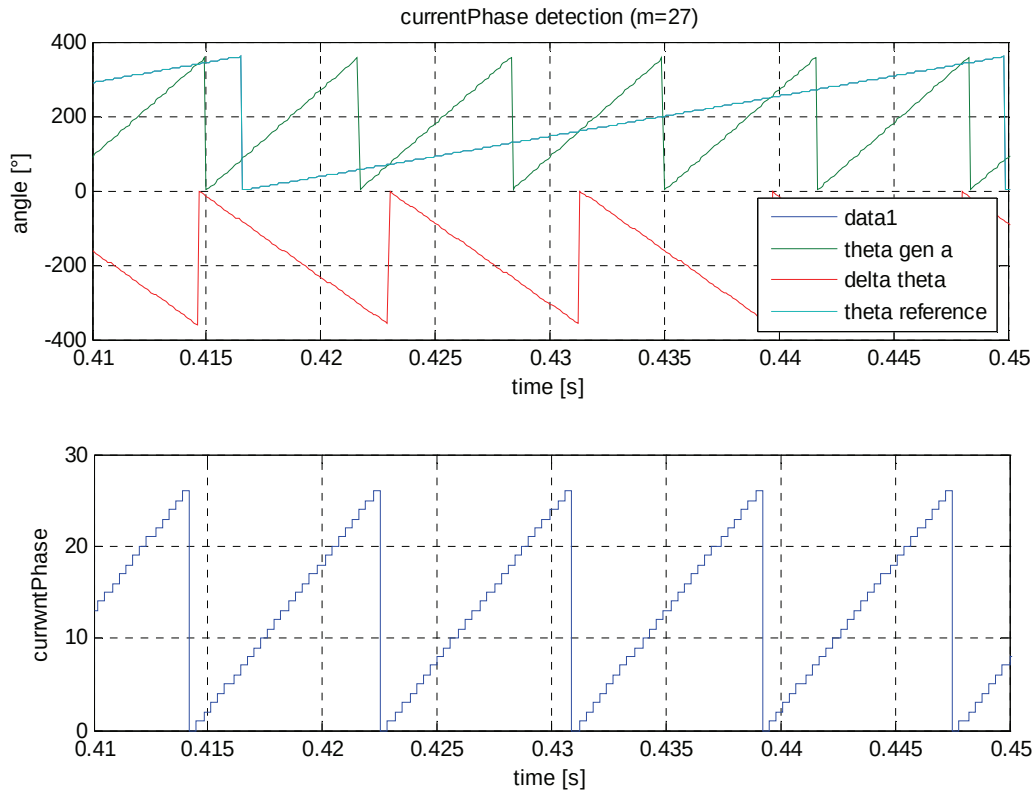


Fig. 5.6 – Phase index generation on the basis of the angular error signal

5.2.4 Dynamic limitation of converter output due to *slowCWC* constraints

The *slowCWC* sequence only allows commutations from one input phase system [a,b,c] to the following adjacent one [a+1, b+1,c+1], in other words, only positive unity phase jumps are allowed. The algorithm presented above does not guarantee this condition simply because any sudden jumps in one of the angular references (on V_{cabc0} or on V_{target}) would lead to a phase jump *j* higher than 1. It is assumed that output of both PLL do not present sudden phase shift and that their slopes are continuous. This assumption can be considered correct because the design of the PI controller of the PLL. This design has not been optimized at all for transient on the grid side. This task is beyond the scope of this thesis and would be a research subject itself. However, it is always possible to get a sudden discontinuity in the target angular reference if the target angular shift between grid and converter output changes its values upon a user action to change P and Q set points. The algorithm must limit the derivative of the target angular reference. If no backwards commutations are allowed neither phase jumps higher than 1, the maximum angular speed at which the phase shift between grid and converter output can change is ω_g-ω_o. This when the connection set [a,b,c] does not change, that is no commutation is requested. On the other extreme, the converter's lowest output frequency is DC. In this case, the angular speed at which the phase shift can occur is $|0-\omega_o|=\omega_o$. The command algorithm must then impose one of those limit slopes on the target angular reference. The choice

between the null slope or the maximum slope depends on the sign of the target phase shift. This limitation is illustrated by Fig. 5.7 to Fig. 5.10.

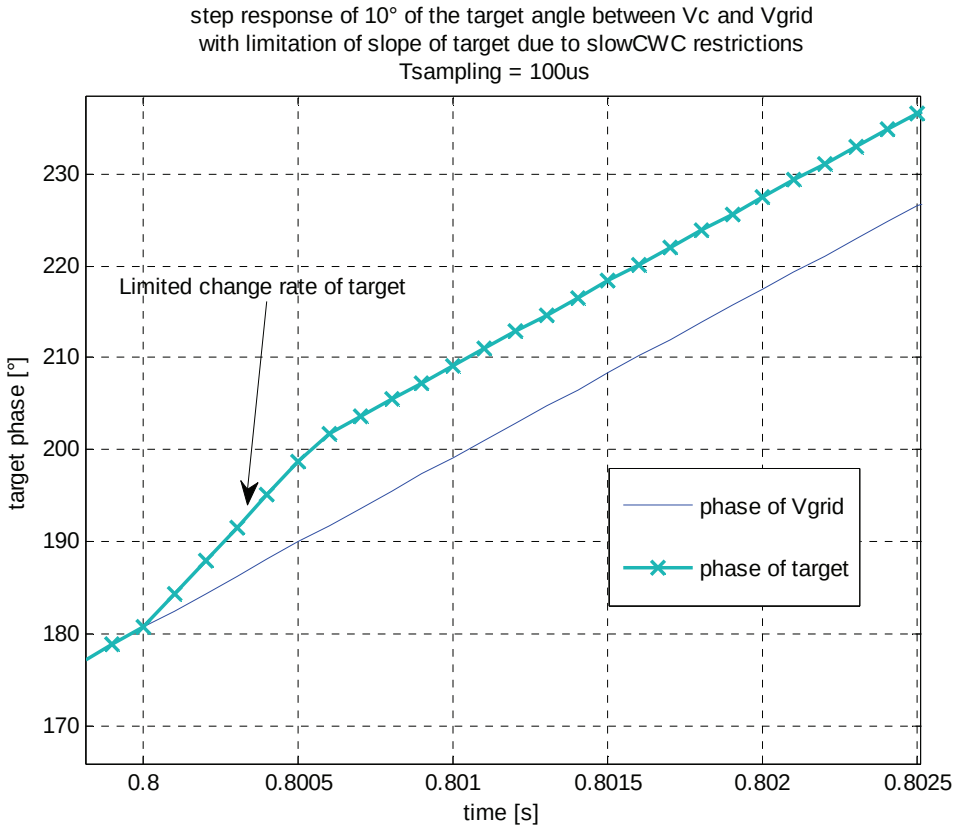


Fig. 5.7 – Step change of target phase shift between Vc and Vgrid with dynamic limitations

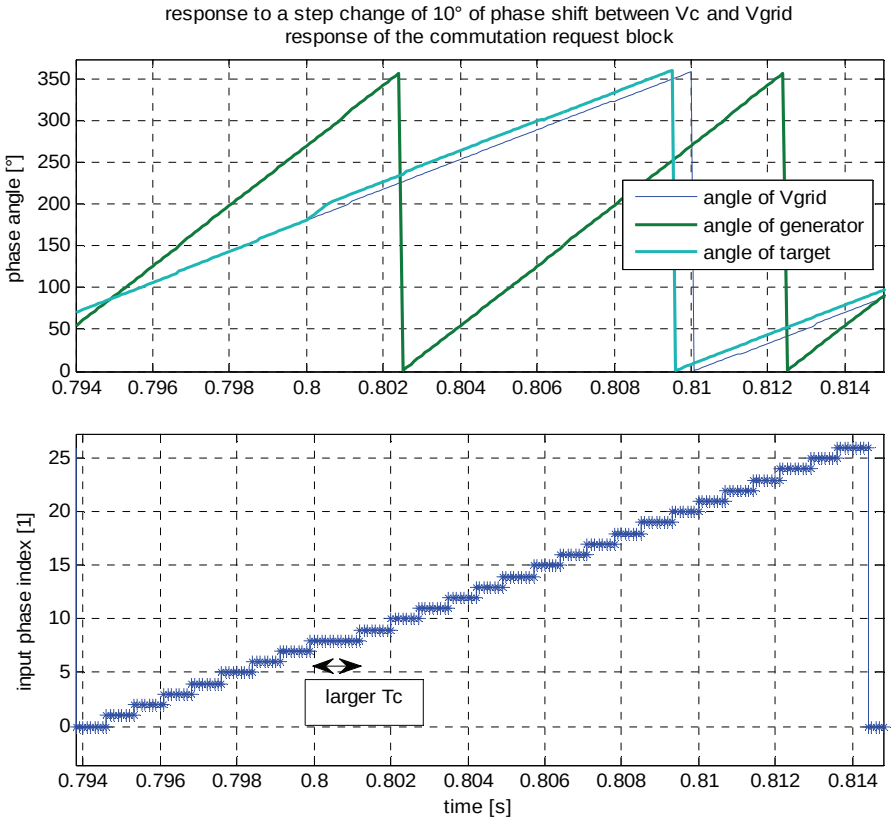


Fig. 5.8 – Step change $\Delta\varphi_{shift}$ and effect of the phase index evolution (larger commutation period)

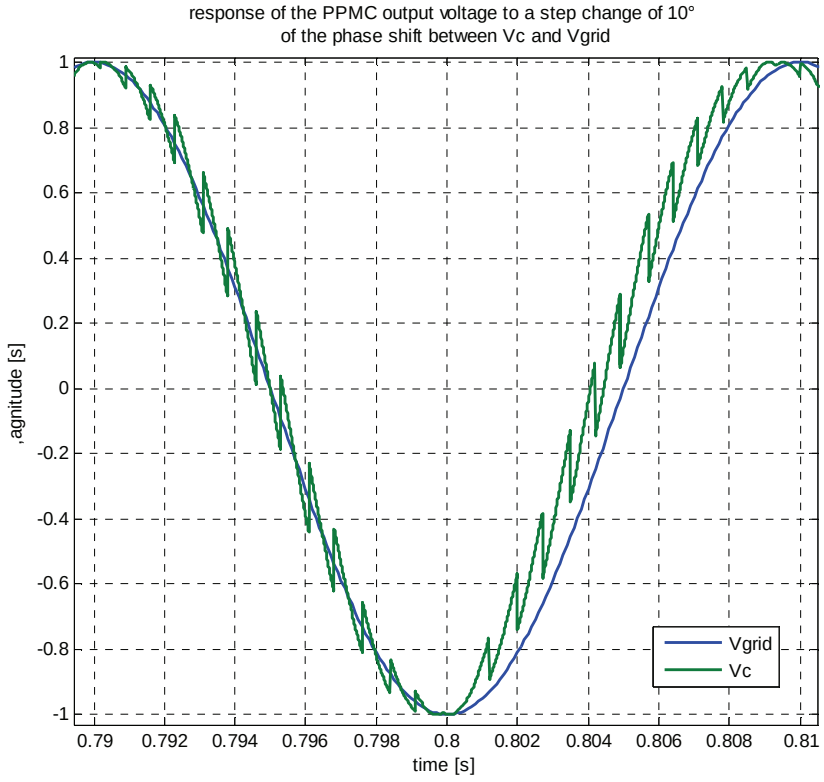


Fig. 5.9 – Response of V_c upon the positive step change $\Delta\varphi_{shift}$

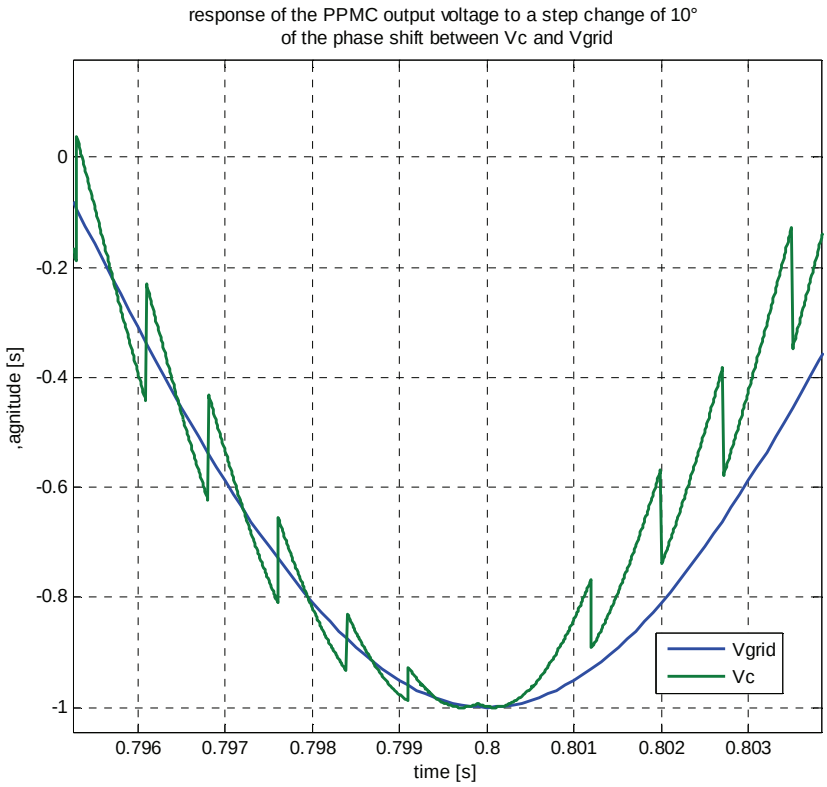


Fig. 5.10 – Closer view of previous Fig. 5.9

The dynamic limitation imposed by the command to the derivative of the phase shift between converter output V_c and grid voltage V_{grid} are here to guaranty only unity forward phase index jumps. The only way to modify the phase shift between V_c and V_{grid} is to increase or decrease the synchronous commutation period T_{c0} by ΔT_c. When T_{c0} is decreased, it must be limited to the minimum value T_{cmin} which produce a DC voltage V_c. for a given step change of the target phase shift $\Delta\varphi_{shift}$ there will be a ΔT_c that is proportional to $\Delta\varphi_{shift.}$ For a positive ΔT_c, i.e. the slope of the angle of the target is set to ω_g. It means the next commutation instant will be delayed by

$$\Delta T_{c+} = \frac{\Delta\varphi_{shift+}}{\omega_g - \omega_o}$$

This can be verified in the figures of the example above.

For a further work, where a current controller must be designed for the PPMC, the characterization of the dynamics of the command is a key knowledge. From a causal point of view, it can be accepted that whenever there is a step change $\Delta\varphi_{shift}$ which corresponds to a positive ΔT_c, the response of the converter voltage phase position to this step change is delayed by a time $T_{command}$ that must be characterized. If the step change $\Delta\varphi_{shift}$ occurs just before a synchronous commutation instant, then this delay $T_{command}$ will be $\Delta T_{c.}$ Now, if $\Delta\varphi_{shift}$ occurs just after a synchronous commutation instant, then $T_{command}$ is the sum of ΔT_c and T_{c0} since the effective change of phase will occur from the time when the next synchronous commutation instant will be delayed by ΔT_c. This is a causal point of

view. If a heuristic point of view is taken now, it can be assumed that the step change $\Delta\varphi_{shift}$ will occur with equal probability within the synchronous period T_{c0} . A mean value of $T_{command}$ would then be

$$T_{command+}(\Delta\varphi_{shift+}) = \frac{T_{c0}}{2} + \Delta T_{c+}(\Delta\varphi_{shift+})$$

A slightly different analysis can be done for a negative step change $\Delta\varphi_{shift-}$ that would lead to a negative ΔT_c in order to find a mean value of delay of the command.

5.2.5 Importance of the sampling time of the command algorithm

The sampling time of the command algorithm is critical. It must be set small enough in comparison with the commutation period T_c otherwise the error in phase angle position of the fundamental of V_c significantly influence the output current and consequently the operating point. Furthermore, if $T_{sampling}$ is not small enough, there are oscillations of the output power. Fig. 5.11 shows a comparison of simulation results of three different sampling time of the command algorithm for similar set points. The conversion here is 100Hz to 50Hz with 27 input phases for which the commutation period T_c is 740µs.

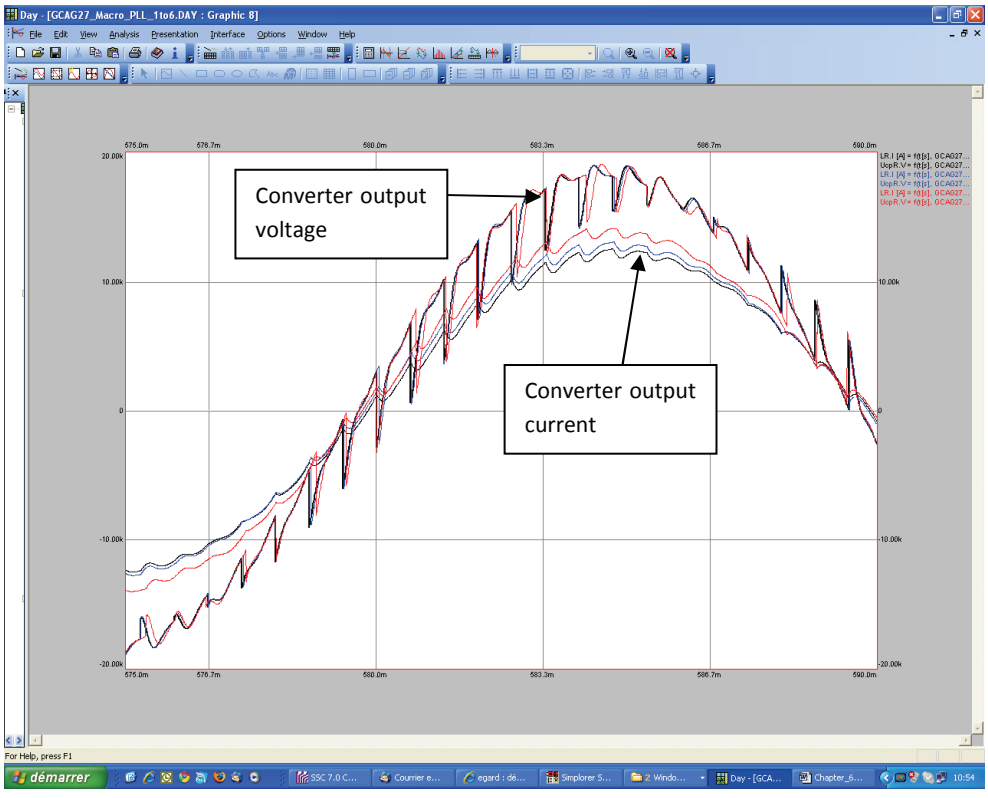


Fig. 5.11 – PPMC output with different $T_{sampling}$ (red : 200µs blue: 50µs black 5µs)

Fig. 5.12 and Fig. 5.13 illustrate power output of PPMC for case study 2 with two distinct command sampling time $T_{sampling}$, 5µs and 1µs resp. Those two results illustrate the PPMC running in full forced mode. Power oscillations are significantly sensitive to $T_{sampling}$. This could be better if the connection impedance was increased.

The question is now, is it possible to find a current controller, or closed loop algorithm, that can get rid of those power oscillations and release the constraints on the $T_{sampling}$? If the constraint on $T_{sampling}$ is too severe for the available digital controller, the above command algorithm has to be split into too tasks. One of these task would be only responsible for the generation of the commutation request instants upon the measurements data and PLL results received from a second task which could run with a higher sampling time. Generation of commutation request instants and detection of the phase index could easily be implemented in an FPGA however a PLL algorithm as used here is perhaps more difficult. Moreover, the PLL does not need to work with a sampling time constraint as high as the block responsible for commutation request. This splitting into two tasks is illustrated in Fig. 5.14.

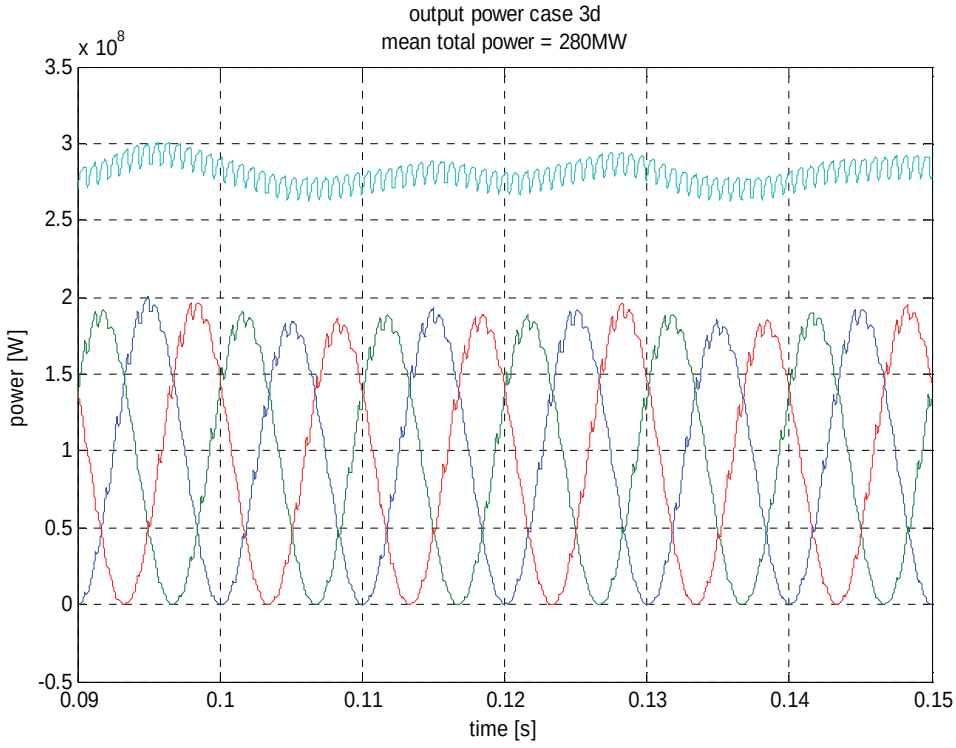


Fig. 5.12 – Output power of PPMC (study case 2) with $T_{sampling}$ = 5µs, full forced mode

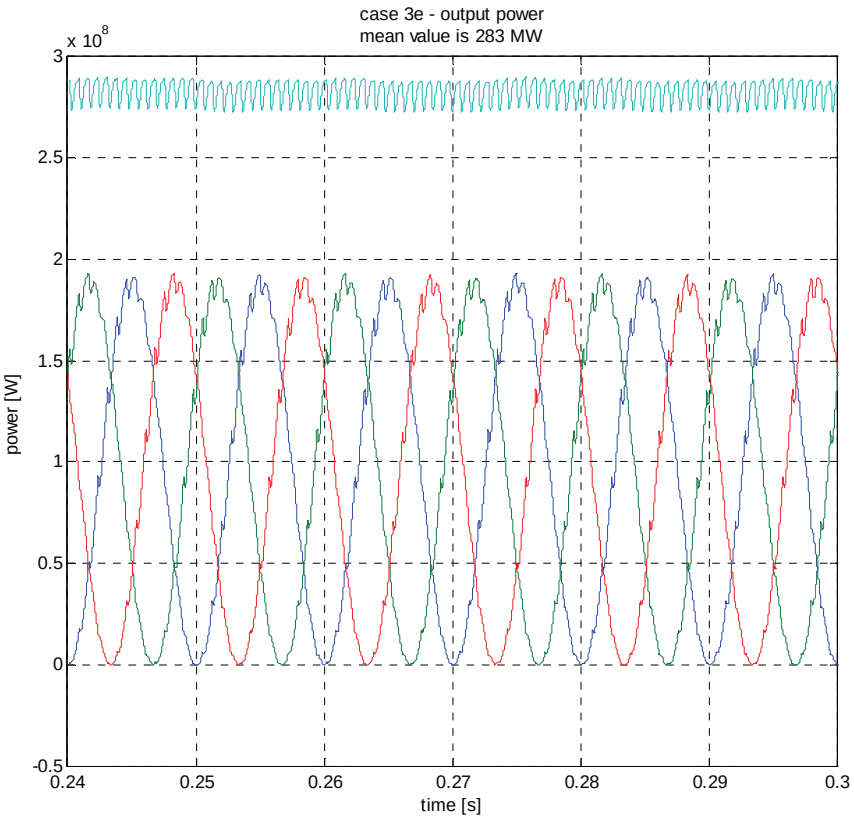


Fig. 5.13 - Output power of PPMC (study case 2) with $T_{sampling}$ = 1µs, full forced mode

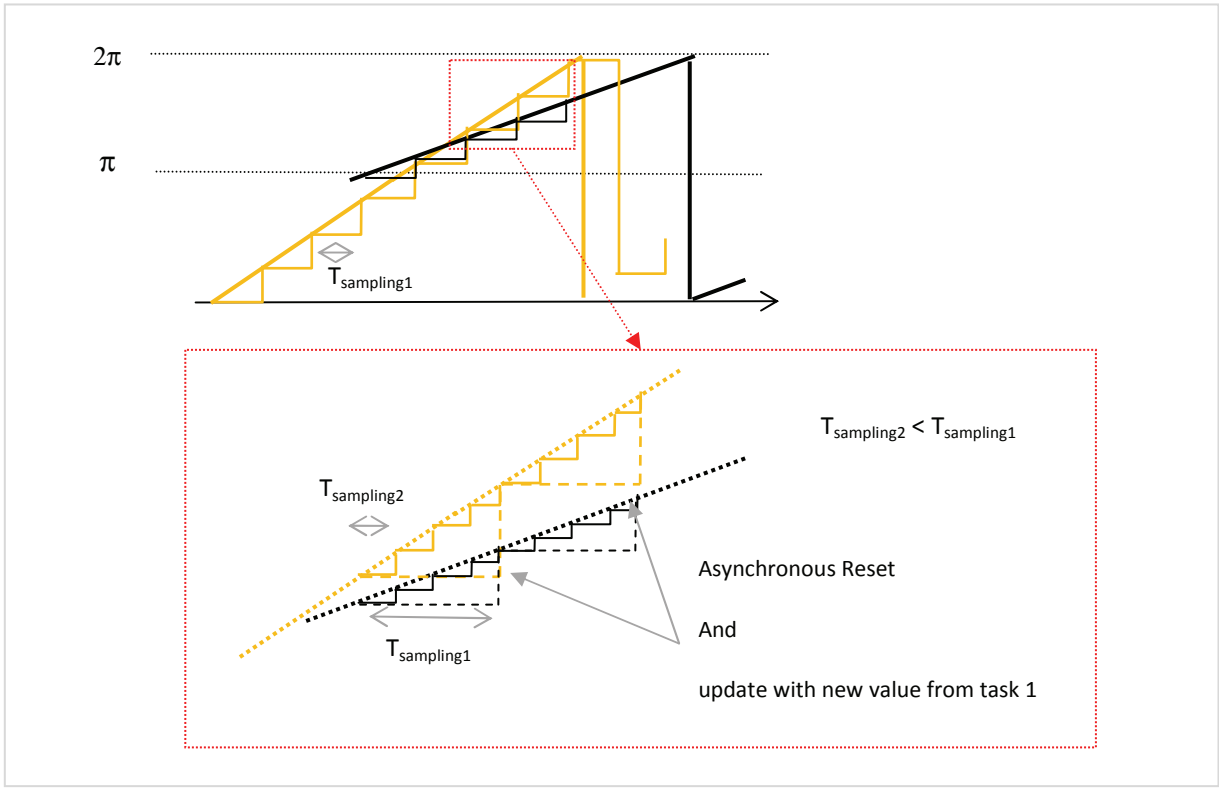


Fig. 5.14 – Split of the command algorithm into two tasks with different sampling period

5.3 Current control

5.3.1 Summary of existing controller design methods

Here is a brief summary of the method usually used to design current control of a power electronic converter. This method is taken from [45]. First of all, the controller design, i.e. the computation of the coefficients, is made with a pseudo-continuous approximation. It means that the discrete behavior of the digital controller as well as the discrete intervention possibilities of the command of the converter are assumed to be fast enough in comparison with the output dynamics and nominal frequencies to be considered as continuous. This is in practice very often the case. Sampling rate of digital controllers must follow the Nyquist frequency criteria and the converter usually works in pulse mode (PWM) with a switching frequency higher than 1kHz, which is far above the nominal frequencies of the load (50Hz or 60Hz). With the pseudo-continuous approximation, the load, the converter and its command and the controller can be modeled with continuous equations that can themselves be transformed into the Laplace domain. The Laplace domain, besides simplifying differential equations representation, has the advantage that the dynamics performance of the closed loop control can simply be chosen by positioning poles of a characteristic polynomial expression. The complexity of this characteristic polynomial expression depends of course on the complexity of the transfer functions of the blocks constituting the whole system.

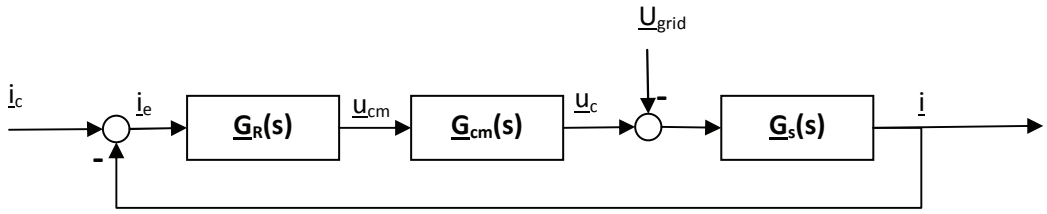


Fig. 5.15 – Transfer functions block diagram of closed-loop current control

If a multi-variable control is required, this method of transfer function becomes less efficient, especially if the variables are coupled together, then it is not possible to design independent controllers without losing control quality. For a number of variables of 2, however, the reference [45] still uses the transfer function method by defining “complex transfer functions” which contains information about the coupling of both variables to control by dedicating real part to the direct transfer characteristic and the imaginary part to the coupling characteristic. With this complex transfer function method, it is possible to design PI controller with decoupling capability. The decoupling capability can be reached if the closed loop transfer function is real. For more than 2 variables, it is necessary to follow other multivariable controller methods.

For AC/AC or DC/AC converters, the load, as it is the case here, is a transformer which secondary side is connected to the grid, considered as a stiff voltage source. There are then three variables to control, I_{oR}, I_{oS} and I_{oT} which are sinusoidal currents with a given frequency ω_o. Usual controllers, like PI controllers, can be designed to track DC references. Therefore, in power electronics, a change of static reference frame (α,β) to synchronous reference frame (d,q) is often performed in order to work with DC references values to control. This is indeed quite easy to implement in our case because there is already a PLL on the load side that can be used to create the rotating reference frame. Besides, the spatial vector representation of the three phase systems is often used to reduce

the number of variables to control from 3 to 2. Hence the method of complex transfer function is suitable for the design of a PI controller for most power converters. When expressing the complex transfer function of the AC load consisting of the transformer and the stiff grid, into the rotating reference frame, a coupling factor between both axis d and q appears. The variation of the load current I_{od} influences the load current I_{oq}, and vice versa. This coupling term is not appreciated since I_{od} and I_{oq} are representative of the active and reactive power resp. Therefore, it is required that the controller cancels this coupling actively. Reference [45] and [46] gives extended design of PI multivariable controllers with decoupling capabilities applied to VSC. For such design, the transfer function of the block converter-command in the rotating frame must be known. In the cases handled by those references, usually, the transfer function of the command-converter in the rotating frame is very simple and a very important assumption even makes this transfer function purely real.

Generally, like in [45], the transfer function of a converter, in a static frame, is given by Equ. 5.2.

Equ. 5.2

$$\frac{\underline{u_{cm}}}{\underline{u_c}} = G_{cm} = \frac{K_{cm}}{1+sT_{cm}}$$

with u_{cm} the command signal coming from the controller and u_c the converter output voltage. K_{cm} is the static gain and T_{cm} a small time constant that represent a mean delay due to the discrete intervention possibility of the command (due PWM finite frequency). When expressing this transfer function into the rotating frame, the appearing coupling term can be neglected by assuming that T_{cm} is much smaller than the period of the load T_o.

5.3.2 Analytical approaches of PPMC current control

In a first approach of current control for the PPMC, before redeveloping a control theory, the author wished investigate the possibility to apply the described theory, briefly summarized in the paragraph 5.3.1, to the PPMC. This requires to find an expression of the transfer function of the command-converter block for the PPMC. This task has revealed itself to be quite complex and the fact that the PPMC is not a high switching frequency type converter makes some usual assumptions a hard life.

The first task is to find the complex transfer function of the command block of the PPMC, which transforms command signal $\underline{V}_{cm}$ into a converter output voltage $\underline{V}_c$. Reference [45] does not handle converter that are similar to the PPMC. At most, one could inspire himself with the example of a six pulses current rectifier handled by [45]. A first issue that comes out with the command of the PPMC is the fact that it does not work in axes d and q but acts on the magnitude and the phase of V_c, as described above in section 5.2. Thus expressing its transfer function into the d and q axis implies to linearize the trigonometric relation between d,q axes coordinates and the corresponding polar coordinates. Thus a different transfer function should be found for different operating points. Besides, as seen in 5.2, the time constant of the command block, on a first approximation, is in the order of $T_{c0}/2$. Depending on the frequency ratio, this time constant could be or not negligible in front of the output period T_o, thus the approximation and simplification of the transfer function of the command block, often performed for standard methods found in [45], are not possible here. Besides, there appears also a coupling between axis d and q through the model of the generator-converter block.

5.3.3 Numerical approach of PPMC current control

In parallel, the study that can be found in reference [47] has delivered empiric results and at least showed that it is possible to control the PPMC and decouple in a certain limit both axes. Because the expression of the transfer function of the command-converter block is hard, the approach of [47] is numerical and uses identifications to extract a suitable transfer function of second order. From this second order transfer functions the author of [47] designs a theoretical controller to meet decoupling and given dynamic performance. The theoretical controller is too complex to be implemented and [47] extracts a simplified version similar to a PI. [47] has also used extended numerical approaches, which in one step, perform identification and delivers optimized coefficients of a controller with preliminary defined structure (PI, decoupling). Because the first method suffers from simplification, the second approach has shown better results in terms of dynamics performances. However, those fully numerical methods have a lack of transparency that makes hard to state on their robustness. In order to give the reader an idea of the performances of such a control, Fig. 5.16 sows a simulation result extracted from [47].

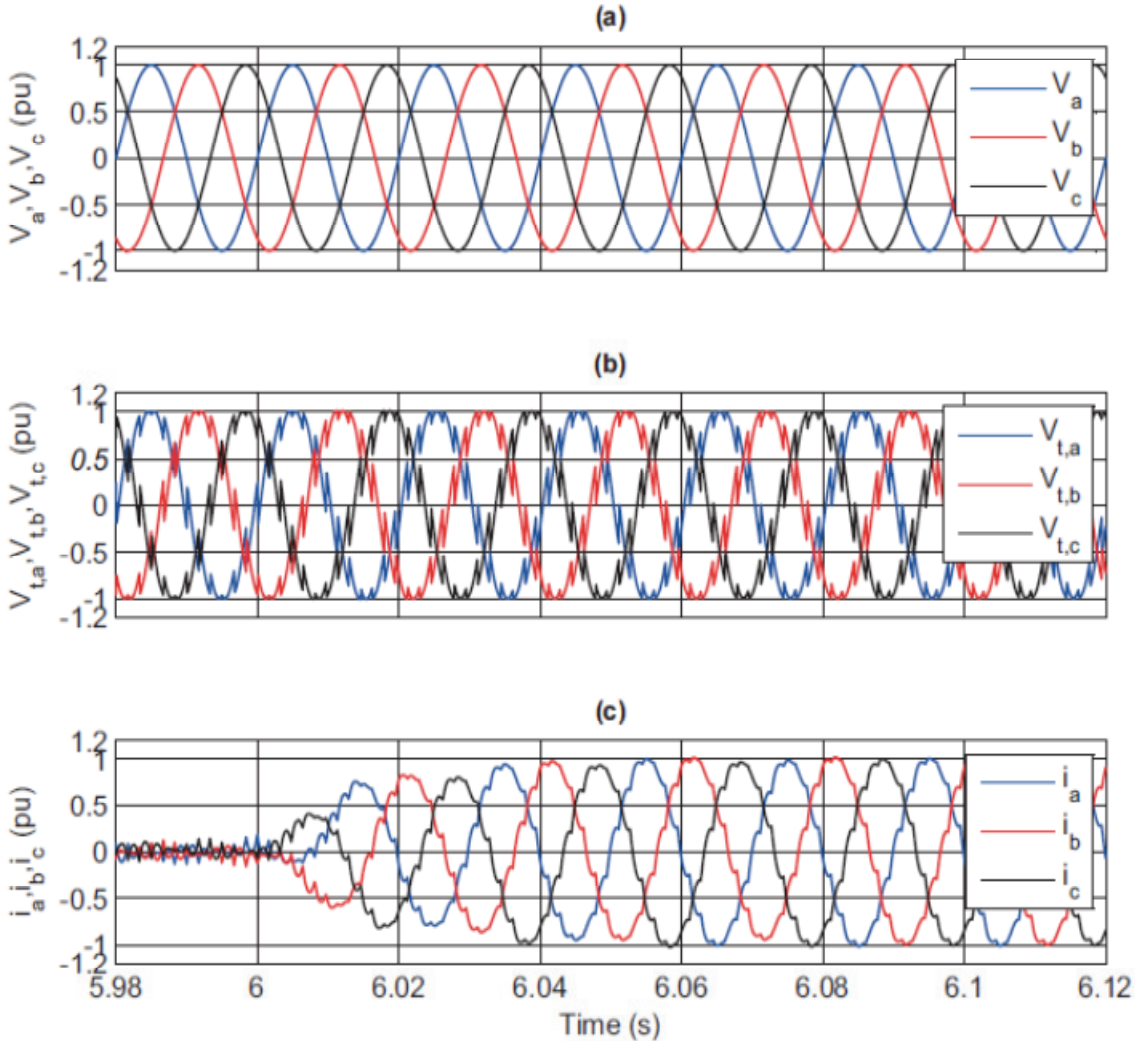


Fig. 5.16 – Response to a d component step with an OMCC (source [47])

Chapter 6 – Small scale experimental set-up

6.1 Experimental set-up principle

The scaled PPMC set-up presented in this chapter has been realized for the development and test of the control circuits of the original converter. Real-time operation of the model is in the foreground. The experimental set-up is also used to verify the analytical predictions of snubbers' peak voltage and the losses in the snubbers' resistor. The targeted nominal power is about 1kVA. The frequency ratio of the conversion can be varied so that the set-up is able to emulate variable speed (variable frequency) of the generator. In order to focus on the frequency converter itself, simplify the set-up , reduce the cost and increase security, it has been decided that this set up would not use any rotating mechanical parts. Thus the poly-phased generator is emulated with a *Poly-phased generator Emulator*. Details about the building blocks of the set-up are given below. Fig. 6.1 shows the four main building blocks of the set-up and their connections.

1. Poly-phased Generator Emulator
2. PPMC
3. Load
4. Control

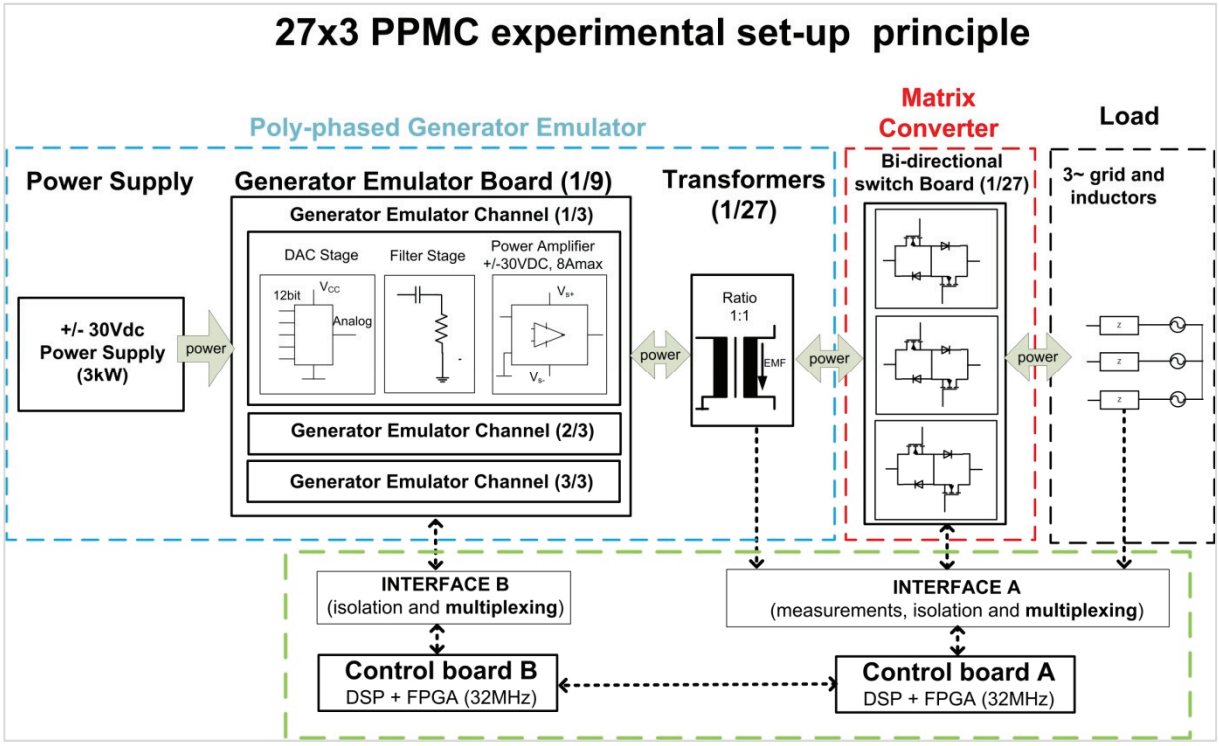


Fig. 6.1 – 27x3 PPMC experimental set-up principle and components

6.1.1 Generator emulator

The nominal frequency of the generator emulator is 100Hz but can be varied from 30Hz to 400Hz. Amplitude of induced voltages can be varied from 0 to 30V_{peak} which allows a maximum "polygon voltage" (largest line-to-line) of 224 V_{peak} for 27 phases (i.e. maximum V_{cRS}=224V). Fig. 6.3 shows the experimental set-up, where all modules and transformers are placed on a circle, allowing symmetric leakage inductances for the connections of each transformer to the other, as well as symmetric coupling to each module. With this generator emulator, the PPMC can easily be studied with the

desired input phase number, without the burden of rotating mechanics. Here are details about the components of the generator emulator.

Transformer

The particularity of this set-up is that the poly-phased generator stator winding is emulated with 27 single-phase transformers, whose secondary windings are connected in delta (polygon) as the original generator is. Those single phase transformers have unity transformation ratio with nominal apparent power of 100VA under nominal voltage of 25V. They have a nominal frequency of 100Hz. They have been designed for that application by a Swiss company and are not standard components. However, to stay with an affordable price, the degree of freedom in the choice of the leakage inductance and winding resistance is limited. That is why we do not have perfectly matching p.u. values between the set-up and the high power case study described in chapter 3.

Push-pull class B amplifier stage

The induced sinusoidal voltages (EMF) of the generator are applied to each primary winding of the 27 transformers through analogue power amplifiers (class B push-pull) located on the Generator Emulator board. Each of those nine boards contains three channels. The Class B push-pull power amplifier operates with a maximum bipolar DC voltage of ±30V and can stand up to 8A for a unity power factor. Details about heat sink sizing are not given here but it has been calculated that they require forced air cooled heat sink with a thermal resistance of about 1.1 K/W. The three channels of one board are mounted on the same heat sink.

Waveform generators

For each channel, the $1/27^{th}$ of the generator's period shifted signals of the induced voltages (EMF) are generated from a DAC by a dedicated IC. Those IC are configured once at start-up where they receive the frequency to generate and their own phase shift. Then, in run time, they only receive a synchronous clock signal from which they generate the desired sinusoidal waveform. The reference synchronous clock signal is set to 50kHz and the resolution of the DAC that generate the sinus waveforms is 10bits.

Signal shaping

Because the output of those waveform generators is unipolar, a signal shaping and filtering stage is necessary before feeding the input of the push-pull class B amplifiers. This stage transforms the output of the waveform generator into a bipolar signal. It filters out the harmonics due to digital waveform generation and realizes a first amplification with variable gain. It also contains a feedback loop that cancels any DC component at the output of the push-pull class B amplifier. This is indeed important since the load is a primary winding of a transformer and hence very sensitive even to small DC component in the voltage applied, that could bring the magnetic circuit into saturation and produce high currents. A simpler passive capacitor for canceling the DC component could also have been used but this capacitor has to be designed for the nominal current and hence take some additional place. No details are given for the design of this signal shaping stage but it can be highlighted that the requirement on the tolerance of the phase shift introduced by the filter is not negligible. Indeed, for filters, resistor and capacitors are used and those elements have given

tolerance. It is easy to find 1% or 5% tolerance for resistor however the tolerance of capacitors, with reasonable price, is minimum 5%. If such components are used, then the tolerance on the phase shift introduced by the filter can take values that are near the $1/27^{th}$ phase shift between two generator phases even if the cutting frequency of the low pass filters is one decade higher. So it is required to put the cutting frequency at least two decade higher that the nominal output frequency which implies that the sampling frequency of the waveform generator to be high. That is why there is one waveform generator for each channel and not one central unit sending data to 27 DAC. The required time to send data to the 27 DAC at each sampling time would put a limit in the sampling frequency.

Control board B and decoding interface

The initial configuration data for the IC of the DAC stage is sent through SPI link to the 27 channel from a control board. This control board has two main components, a DSP and an FPGA. In run-time, this control board only sends the synchronous Clock signal and a voltage reference that can be varied whenever wished to modify the EMF magnitude. In order to emulate the excitation circuit of a real synchronous machine, there is a limitation on the rate of rise of the reference voltage. In run-time the control board could also be used to modify in real time some parameters of some channels if desired.

Between the control board B and the generator channels, there is a decoding interface board for the SPI communication. This interface also realize a galvanic isolation through opto-coupling devices for all signals that goes to the generator emulator boards, since the ground of those board is also the power ground of the whole set-up.

DC power supply

This ±30V DC power supply is built from the series connection of two 30Vdc power supply each with a current capacity of 60A unidirectional. So the total available power is 3.6kW. The target nominal power of the converter is about 1kW. As we use the class B amplifier to emulate the generator, then at least half of this power will be lost at this stage, therefore the minimal power of the DC supply is 2kW.

6.1.2 Frequency Converter - PPMC

The PPMC itself has been realized with 27 power boards, equipped each with three bidirectional switches. The required resistive-capacitive snubbers (see chapter 3 and 4) are also mounted on those power boards. The semiconductors used to build the bidirectional switches are two IGBTs (600V) with integrated reverse diode. They are connected in anti-series, as depicted in Fig. 2.4 (left) (common source or emitter). Each of the 27 power boards can connect one generator phase to each of the three phases of the load. The gating signals are galvanically isolated by using opto-coupling devices. The gate drivers are simple and do not send error signal back to the control. Both gate drivers of a bidirectional switch are supplied with a small integrated isolated DC/DC converter which converts the 5V logic power supply to 15volts. Then a small circuit creates +12V and -3V with the 0V connected to the middle point of the bidirectional switches. In order to spare the number of required power supply of the gate drivers, the bidirectional switches could have been in common drain or collector mode but with the common source or emitter mode any configuration of the converter can

be imagined. Because of the low duty cycle of the switches and because their current rating is much higher than the effective current of this set-up, there was no need to mount any heat sinks on the switches.

6.1.3 Control and gating signals generation

Control board A

The control board is denoted “David board” and has been used in the lab for about 10 years. It is not the last digital hardware available but it has the advantage to show that even with a 10 years old digital hardware it is possible to control this pretty large converter. We deduce that this will not be an issue with today’s available digital controllers. The *David* board contains a DSP (Analog Device, floating points, 40MHz, 100MFlops) and a FPGA (Xilinx XC4010, 10’000 logic gates, 32MHz). The DSP is responsible for generation of commutation requirement instants from the measurements and some auxiliary tasks. The control board is used to generate the gating signals, acquires and process measurements and control the output power in open loop for instance, however closed loop current control is under investigation at LEI (see chapter 5).

The FPGA, upon a commutation request from the DSP, generates the gating signals according to the four steps commutation rule described in chapter 2 and 3. These gating signals are sent to the decoding interface. Also, the FPGA is able to set the delay between step 2 and step 3 of the four steps commutation rule in order to run the converter in mix mode operation if wished so, as explained in chapter 2 and 3.

Decoding interface

In order to address the 162 gating signals (27x3x2) with a standard control board of limited numbers of digital output, a special interface has been realized for this application. The states (on/off) of each of the 162 switches are stored on this interface, in flip-flop memory units. Each of this memory unit has a unique address, hence the term “decoding Interface”. The FPGA is responsible to write the correct value to those flip-flops. For convenience this interface is built out of four identical boards, each one containing eight channels. Each channel is constituted in three time two flip-flops. Those two flip-flops store the gate states of the positive and negative poles of one BDS. The splitting of the decoding interface into four boards allowed to use standard logic 4 to 16 decoders and to design a reasonable size of PCB. Each board must be assigned a unique ID (0 to 3). There are in total 192 available gating signals with those four boards, however only 162 are used here. The interface could be used for a PPMC up to 32 input phases. Fig. 6.2 shows the principle of the decoding interface but only with three time six channels.

This interface has also the possibility to clear instantaneously all flip-flops, and hence, open all switches, in case a error signal is raised upon failure detection (e.g. over current). But this must be done with precaution since sudden opening of all switches could be destructive if no protective dispositions are taken (e.g. Varistor on inductive load side).

Measurement interface

In order to generate the commutation requirement instants and perform safe commutation the following values must be measured with reasonable sampling rate.

1. Two generator voltages (2 delta or 2 star or two polygonal sides with 2π/3 phase shift)
2. Two load voltages, line or phase voltage (only in case active load with synchronization needed)
3. Three load currents

The measurement board used here has been realized at LEI for other projects and can be plug-and-play with the *David* control board. It contains eight channels that perform signal shaping because the ADC of the *DAVID* board are unipolar. All measurements are performed with Hall-effect sensors for galvanic isolations. The input of the measurement interface are current-inputs, which is compatible with most Hall effect sensors with current output mode. This guarantees good signal to noise ratio when transporting the measurement signals from the sensors to the measurement interface. This interface also provides hardware security functions. It can raise an error signal as soon as an instantaneous measurement overpasses a given limit. Over-current or over-voltage are very quickly detected.

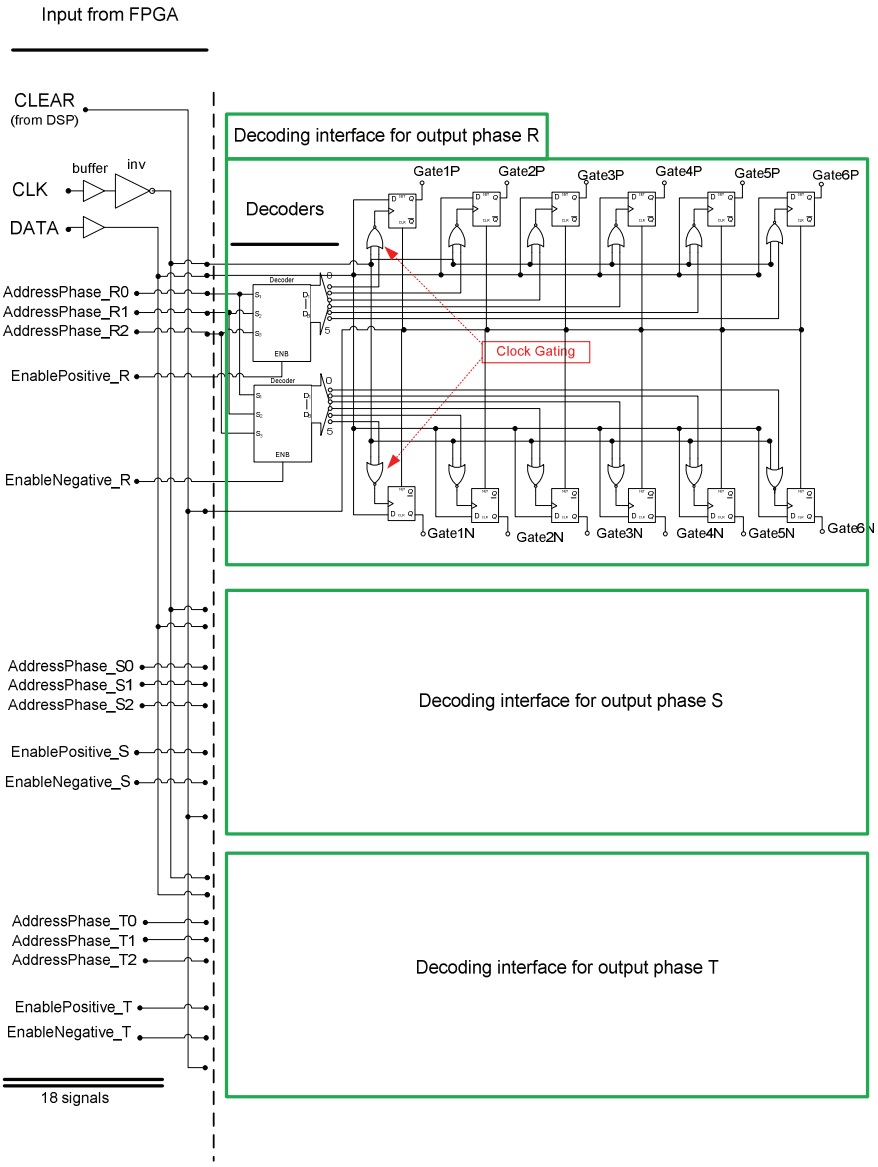


Fig. 6.2 – Principle of the decoding interface

6.2 Realization of the experimental set-up

For the realization of the 27x3 experimental set-up presented in the previous section, the control boards and the measurement interface were already available in the laboratory. However, the generator emulator boards, the power boards and both decoding interfaces (A & B) had to be specially designed and built for this set-up. Those PCB have been engineered and mounted manually at LEI. This experimental set-up represents about one year of one person workforce, from design of first PCB to first run on a passive load. The design of this 27x3 PPMC set-up has been inspired by a first version of a 6x3PPMC set-up also realized in the frame of this thesis, which represented six months of one person workforce. The author realized himself most of the presented set-up, as well as the 6x3PPMC set-up that is not presented here. However, the author got student help in redesigning the second version of the generator emulator boards and power boards. The author also got permanently a one person help for the mounting of the PCB and the cabling of the 27x3 set-up.

Fig. 6.3 gives a general view over the 27x3 experimental set-up. One can observe the importance of the cabling task. The cabling and connector strategy is a key point in the design of such a set-up. In this aspect, this design presents some weakness. But optimization of mounting time was not in the scope of this thesis. The proposed circular geometry has several advantages. First, it ensures a perfect symmetry of the circuit, especially leakage inductances are equal when jumping from one phase to the next adjacent one. Second, the control can be placed in the center, hence propagation time of all signals to the generator emulator boards and power boards are rather comparable. Third, it has a didactic role and the cyclic properties quickly appear to the viewer. A drawback of this circular geometry is certainly its exposure to electro-magnetic perturbation and ground currents, however, in this sense, special care have been brought to avoid grounding loops. Fig. 6.4 and Fig. 6.5 give detailed view of the generator emulator boards, power boards and decoding interface resp.

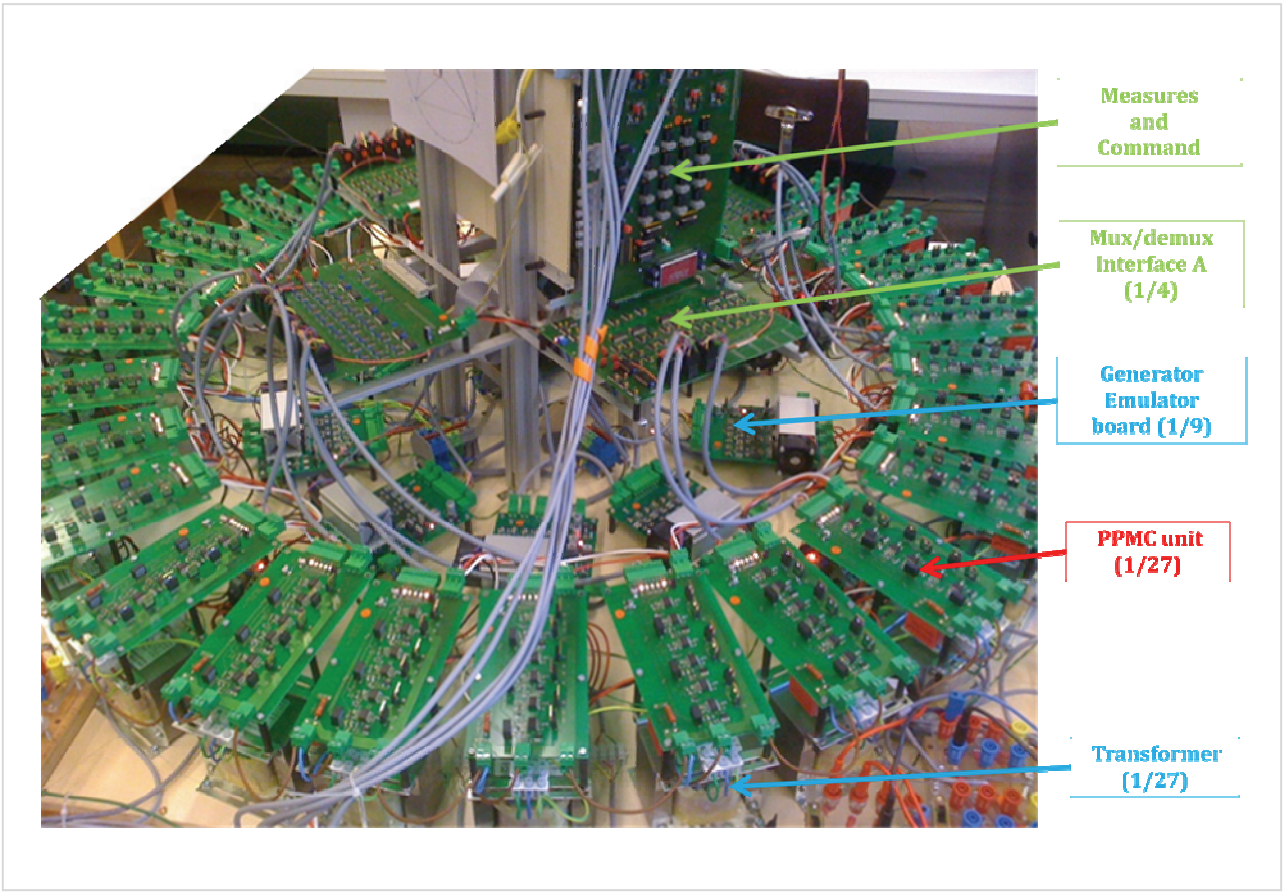


Fig. 6.3 – General view of the 27x3 PPMC experimental set-up

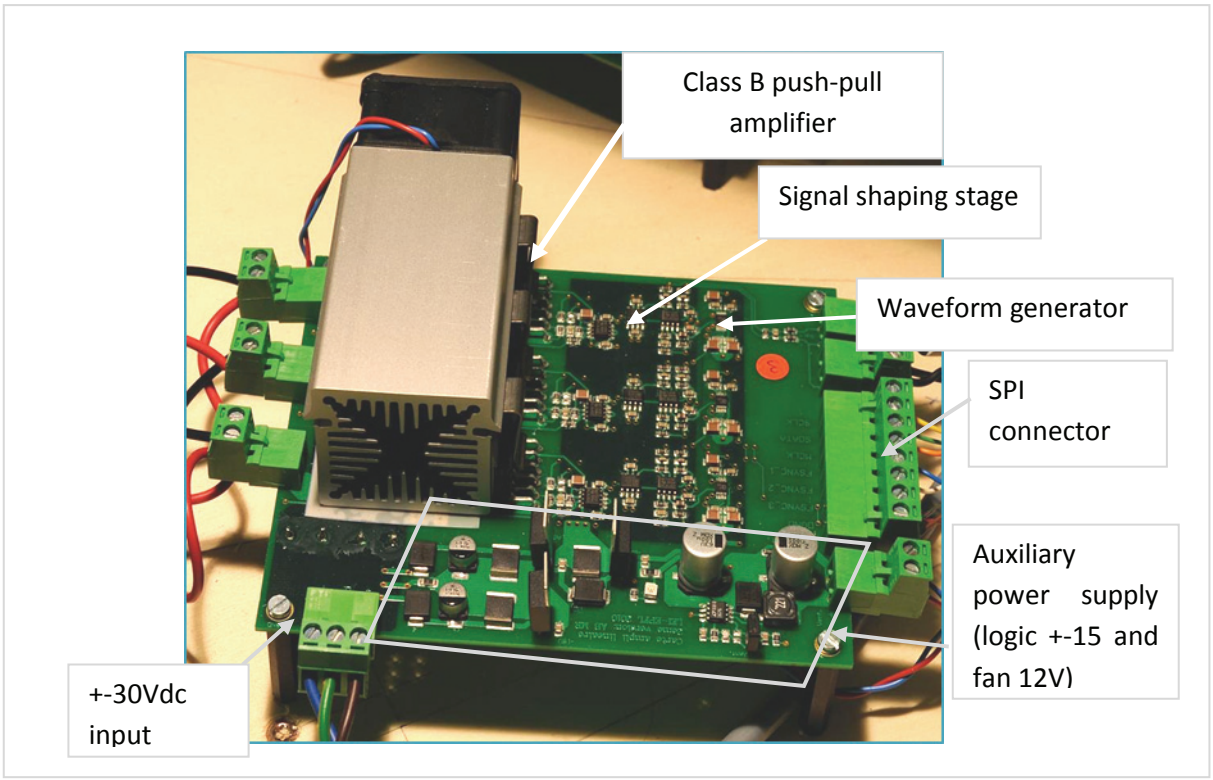


Fig. 6.4 – View of a generator emulator board with its three channels and the heat sink

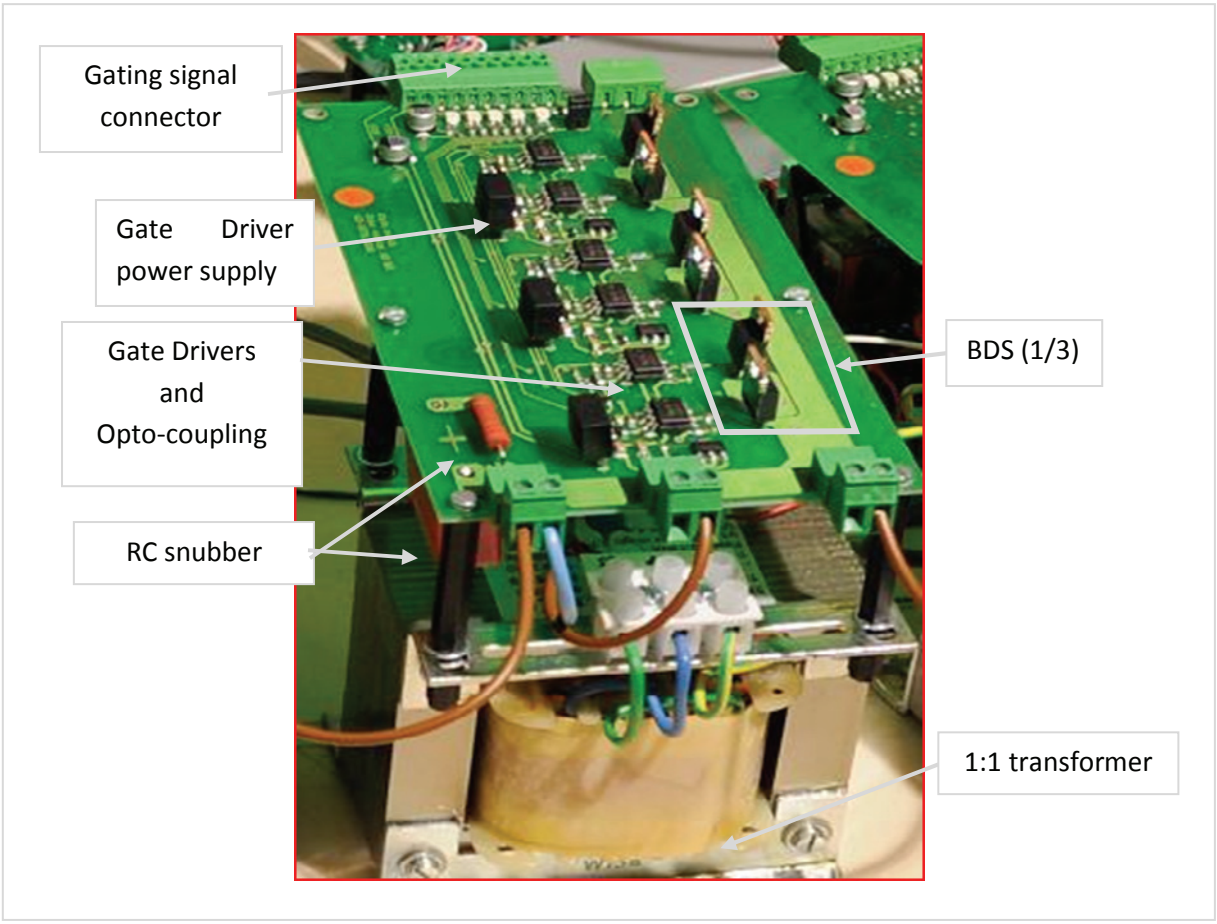


Fig. 6.5 – View of a power board and its associated transformer acting as one generator stator phase

6.3 Experimental results

The actual setup is connected to a passive load, but is foreseen for an interface to a 3 phase transformer connected to the lab's low voltage grid. The first tests documented below are performed on a R-L passive load, where three inductors of 25 mH and three variable resistors are connected in star. First obtained waveforms are described. Then, a FFT (fast Fourier Transform) analysis is performed on some waveforms in order to extract properties and relations between current and voltage fundamentals.

6.3.1 DSP execution time of the command algorithm

The detailed control algorithm implemented in the DSP is presented in chapter 5. With the DSP used for this set-up (Analog Device, Sharc, 40MHz, 100Mflops), an execution time of 80us has been measured. This execution time is short enough because it is smaller than the commutation period T_c but it is not satisfying because the error in commutation requirement instant is, for the 100Hz to 50Hz case :

$$\frac{80\mu s}{740\mu s} = 0.108 \;\; that\ is\ about\ 11\%$$

In practice, the sampling period of the DSP must be taken a bit higher than the execution time, for safety reason. For this set-up, it has been set to 100us. The effect of this error can, in conjunction with other tolerances, can be observed in the results, as shown later on. However, this is only an issue related to the relatively old digital control hardware used here. With a more up-to-date digital controller, this execution time could be easily divided by two.

6.3.2 No Load Waveforms

Table 6.1 - Parameters of the no load case

Generator frequency (Fg) [Hz]	Load frequency (Fo) [Hz]	Generator coil voltage (EMF) [V_{peak}]	Converter output line voltage U_{cpRS} [V_{peak}]
100	50	20	150

Fig. 6.6 a) shows the three output line voltages of the frequency converter, generated by the 27 x 3 PPMC. Fig. 6.6 b) shows two line output voltages of the converter, together with one of the generator voltages running at approximately 100 Hz. Because of the final operation with power exchange with the grid, one of the voltages of an external 50Hz grid is also represented in Fig. 6.6. The magnitude of the converter output, set through the magnitude of the generator "induced" voltage, has the nominal value in both Fig. 6.6 a) and b), so that the magnitude of the fundamental matches the magnitude of the network. The control algorithm is able to position the converter output voltage with a given angle shift from the grid voltage to provide power control features in the near future. This positioning is achieved with two PLL, one on the generator side and one on the grid side, that allow the control to select the correct generator phase in order to produce the desired target converter output voltage.

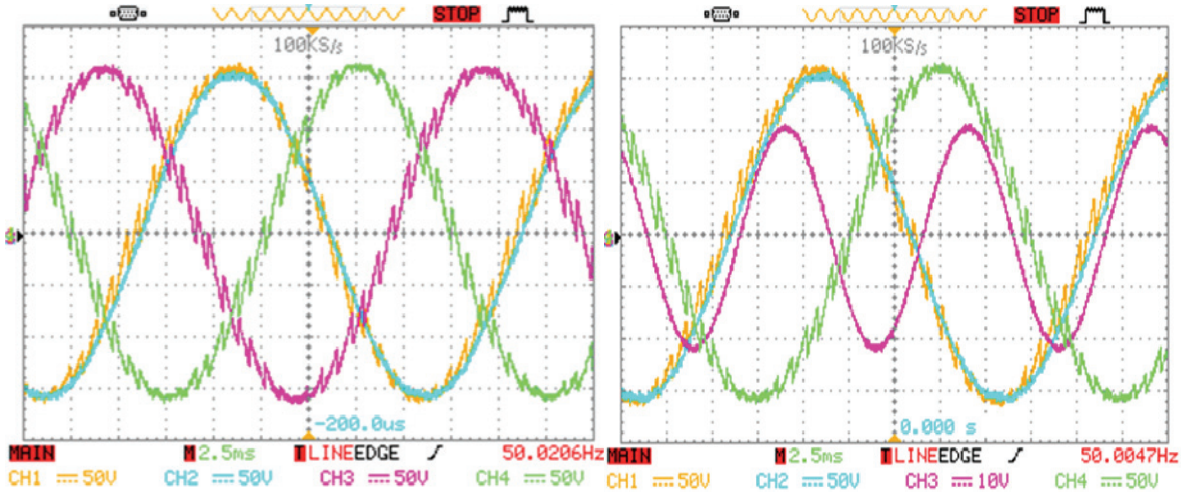


Fig. 6.6 – Waveforms of the no load case a)(left) three phase converter output voltages. b)(right) converter output voltage with generator phase voltage of higher frequency.

6.3.3 Light load waveforms

Table 6.2 - Parameters of the light load case

Generator And net frequencies (Fg) [Hz]	Generator coil voltage (EMF) [V_{peak}]	Converter output line voltage U_{cpRS} [V_{peak}]	Converter output line current I_{oR} [A_{peak}]	Converter Output 3~ power [VA]	Converter Output power factor [-]
100 and 50	10	75	1	64	0.94 (20°)

The following figures show now a case with a passive R-L-Load. The delivered power of the converter remains low compared to the nominal value. The waveforms at full load are not yet available. However, the light load waveforms already show theoretically predicted properties of the PPMC.

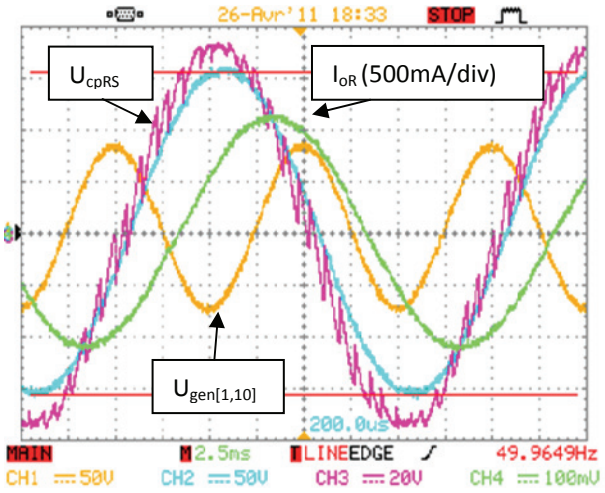


Fig. 6.7 – Waveforms of light load case

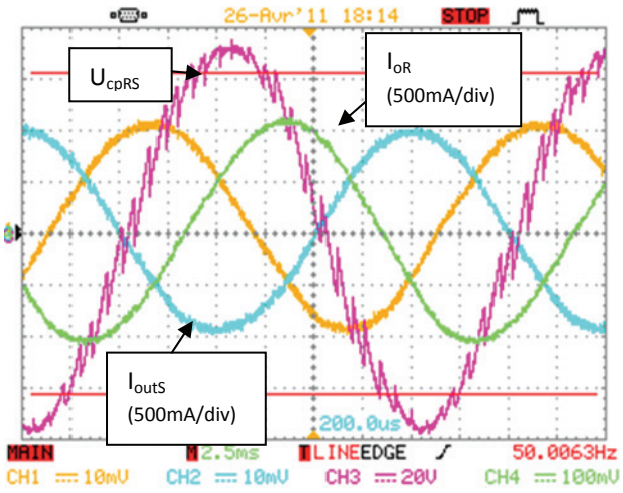


Fig. 6.8 – Three-phase output currents of the light load case

Fig. 6.7 shows one converter output line voltage (U_{cpRS}), one converter output current (I_{oR}), one network line voltage (U_n), one generator maximal line to line voltage ($U_{gen[1,10]}$, line to line voltage between phase 1 and 10).

Fig. 6.8, shows one converter output line voltage (U_{cpRS}) and the three converter output currents (I_{oRST}). The currents are quite smooth because the three phase load comprises 25mH inductors. In the case of a power injection directly into the network, the filtering inductor would have a value of about one sixth of the one used for the passive load here, for a voltage drop across it of about 10%, a common value for a current control to be stable. In the case of a nominal power injection into the network the output current magnitude would be about 6 times the magnitude showed below. Also the output voltage of the converter would be doubled which results in doubling the voltage ripple across the filtering inductor. So the relative current ripple for the nominal case would be the double of the those of Fig. 6.8, which is qualitatively still acceptable.

Fig. 6.9 a) shows one generator coil voltage (V_{gen}) and the generator coil current (I_{gen}) as well as the current through the snubber of this generator phase ($I_{snubber}$). We clearly see here that the current in one generator coil is a succession of portions of one of the three delta load current I_{oRS}, I_{oST} and I_{oTR} alternatively. There is a √3 factor between the peak value of the load line current and the peak value

of current in one generator coil because the generator is always connected to the load in delta configuration. This ratio can be observed between Fig. 6.8 and Fig. 6.9 a). In Fig. 6.9 a) the snubber current is also to be observed although it is very noisy because it has been measured through the voltage across the snubber resistor, which voltage has been measured by a voltage differential probe which voltage range is not adapted for such small magnitude. However, it is still possible to observe the base capacitive current through the snubber as well as the superimposed peak current due to the forced commutations. The base current can be approximated here to a quarter of a division in magnitude, that is 56mA$_{peak}$ which is close to the theoretical values of 46mApeak, the difference being in the measurement errors and the tolerance of the snubber capacitor and resistor values. The delivered capacitive power is then 0.28VAr.

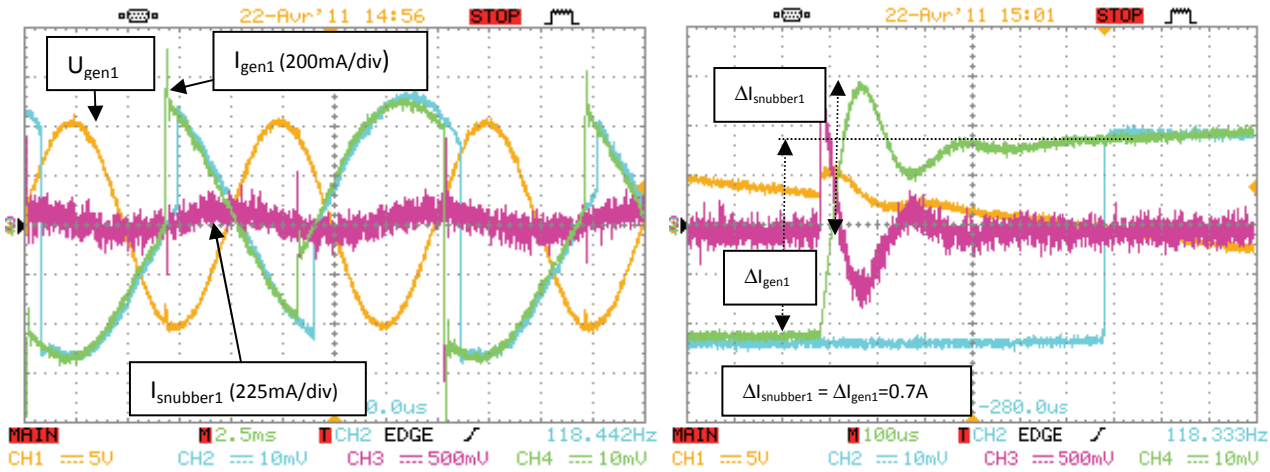


Fig. 6.9 - a)(left) Generator waveforms of light load case b)(right) Zoom of a)

Fig. 6.9 b) is a zoom of Fig. 6.9a) of one forced commutation. This shows the predicted RLC response. The ringing frequency and peak values are not compared here with the theoretical prediction because it is not the aim of this paper. Also to be observed in Fig. 6.9, the RLC transient is damped before the next commutation occurs. Fig. 6.9 b) shows that the jump of the generator's coil current (I_{gen}) does match the jump of the snubber current. This jump is about 700mA. The snubber plays the role of the free-wheeling path during the forced commutation.

Fig. 6.10 shows one generator coil current (I_{gen}) along with two snubber currents ($I_{snubber1}$ and $I_{snubber2}$). This figure mainly shows that only one snubber is active when a commutation occurs and that the adjacent snubber does not react or react in a very damped way. This was one assumption taken in the theoretical analysis of the converter for the design of the snubber. In Fig. 6.10, when a commutation occurs for generator phase 1, only its snubber sees a transient response. The current of snubber number 2 does not have any transient at this moment. Similar for the next commutation, only $I_{snubber2}$ will react.

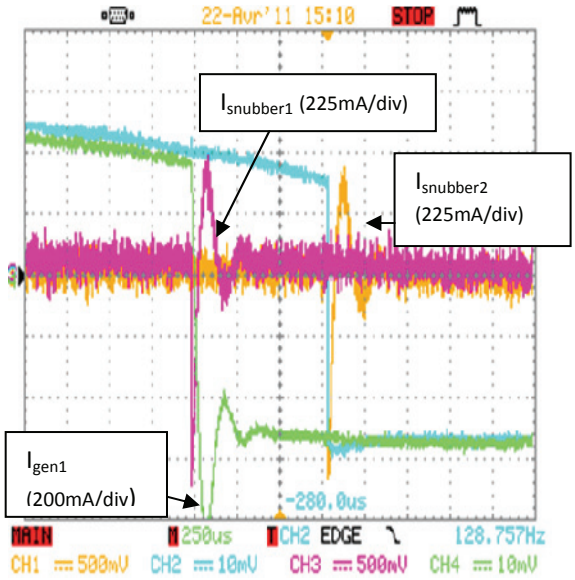


Fig. 6.10 - Two snubber current for two consecutive commutation

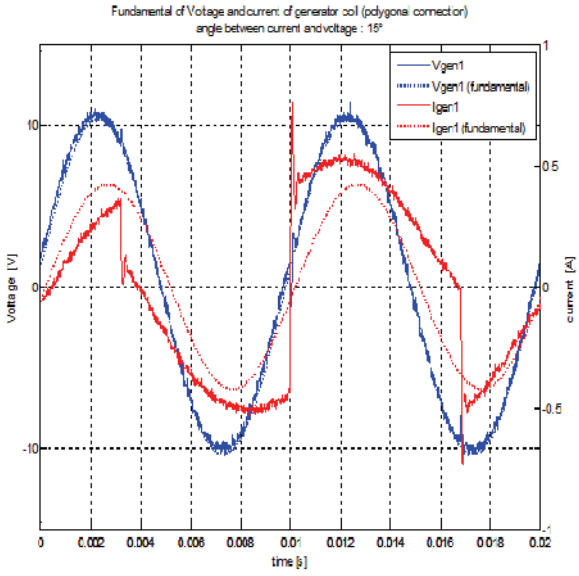


Fig. 6.11 - Generator phase voltage and current with their fundamentals

6.3.4 Spectral analysis

A FFT function allows to extract the frequency spectrum of some waveforms, especially the value of the fundamental and the Total Harmonics Distortion (THD) factor which are of interest here. The dataset used for the FFT are rectangular-windowed and sampled with a rate of 100kS/s. As the length of the data recorded are not very long compared to the fundamental period (about two times), the resolution of the Discrete Fourier Transform (DFT) is not very fine but fine enough for the analysis performed here. The width of the window is set to an integer number of the theoretical fundamental period of the signal so that the leakage effect is limited. For an output voltage of the PPMC performing a frequency conversion from a generator frequency F_g to a output frequency F_o, the theoretical repetition frequency of the output instantaneous waveform is the greatest common divider (GCD) of F_g and F_o. So the theoretical acquisition time required to perform a DFT of an output voltage of the PPMC could be very long compared to the load period ($1/F_o$). As in practice, F_g and F_o can take any real value, it can be that the required acquisition is infinite. So in the DFT performed here, we will not use the result of the FFT to discuss sub-harmonics.

Table 6.3 – FFT results

Signal	Fundamental Frequency [Hz]	Fundamental magnitude	THD measured [%]	THD Theory [%]
Network line voltage	50	156	1	0
Converter output line voltage (U_{cpRS})	50	158	7	7
Generator coil voltage (V_{gen1})	100	10.5	4	-
Generator coil current (I_{gen1})	100	0.42	66	68

One result of that the FFT analysis helps to compute is the displacement factor between generator's windings fundamental current and fundamental voltage, that is the power factor of the fundamentals. In Fig. 6.11, V_{gen1} and I_{gen1} of Fig. 6.9 a) are plotted along with their respective fundamental signals. The sign of the current has been changed in order to have a generator power convention (a positive instantaneous power means a power delivered by the source to the load). It can be computed that the power factor of the fundamental, or the displacement factor, is 0.965 (15°). This power factor should correspond to the power factor of the load of the converter that can be deduced from Fig. 6.8 and expressed in Table 6.2. It is a 0.94 power factor which corresponds to an angle of 20°. So there is a 5° difference between this value and the displacement angle of the fundamental in the generator coil. This difference, apart from the measurements errors, can be explained by the fact that the coil also consumes reactive power produced by the capacitor of the snubber connected to it. As estimated above in Fig. 6.9 a), this reactive power is about 0.28VAr. When this amount is added to the reactive power of fundamental in the generator coil, and when recalculating the power factor we obtained, we get closer to the 20° of the load. In Fig. 6.11 the VA are estimated at 2.48VA which correspond to 0.64VAr and 2.39W. When we add the 0.28VSAr due to capacitor we obtain a power factor of 21°.

This shows that the PPMC, which runs with the slow CWC commutation pattern, does not "consume" reactive power, as predicted by the theoretical ideal waveform. Of course the PPMC consumes also reactive power since there are the capacitive snubber connected to each generator coil, but the snubber design imposes low limit of this reactive that still allow feasible snubber, as shown in chapter 4.

Chapter 7 – Conclusion and perspectives

7.1 Conclusions on the new proposed topology

A new direct frequency converter for the Active Generator (AG) concept has been proposed in order to operate properly the existing *slowCWC* commutation sequence, whose valuable input and output properties have been highlighted in chapter 2. The new converter is a gate-commutated "Poly-Phased Matrix Converter" (PPMC). Chapters 3 and 4 have presented a detailed analysis of the process of commutations within the PPMC and issued general design rules for the required passive protection circuit. For a 27 input phases PPMC connected on one side to a poly-phased SM with a short circuit current (i_{short}) equal to 5p.u. (i.e. x''_d ≈0.096 p.u.) and nominal frequency 100Hz, and injecting power into a grid of nominal impedance $Z_{N,grid}$, the required capacitance for the protection circuit is given by:

$$C_s = c_s \frac{1.4}{Z_{N,grid}} \quad [mF]$$

where the relative capacitor c_s depends on the admissible overvoltage constraints. For a high power injection of several MW, a value for $Z_{N,grid}$ is about 1.4 Ω. The following table gives typical numerical values of installed capacitances for three overvoltage constraints.

Design constraint v_{sMax} [1]	c_s [1]	r_s [1]	$Z_{N,grid}$ = 1.37 C_s [mF] per circuit
8	0.01	5	0.01
3	0.16	1.3	0.16
2	0.65	0.65	0.65

Chapters 3 and 4 have also expressed the energetic performance of the PPMC which is a critical criterion in selecting a converter for the AG application, as mentioned in chapter 1. The conduction and switching losses of the PPMC remain within an admissible margin for the AG applications. The losses that come from the passive protection circuit are more critical. They are divided into two components: the no-load losses and the on-load losses due to commutations. The later components can be significantly influenced by the design of the passive protection circuit and by the operating mode of the converter, either the full forced mode or the mix mode. The analysis of the no-load losses has shown that they also remain within acceptable values for the AG application. Besides it has shown that the influence of the passive protection circuit on the input displacement factor is negligible for most design, hence the valuable input property of the *slowCWC* sequence is conserved.

The losses in the snubber vary in function of the frequency ratio and in function of the leakage inductance of the generator stator winding, represented through the relative generator parameter i_{short}. The next table gives numerical values of efficiency drop due to losses in the protection (or snubber) circuits.

Relative Losses in the protection (or snubber) circuit due to commutations i_{short}=5p.u. (i.e. $x''_d \approx 0.096$p.u.)		
Frequency ratio F_{in}/F_{out}	**Full forced**	**Mix mode**
2	5%	3.5%
1.2	3%	2.1%

Those values are not acceptable for power generation applications where the efficiency is a critical criterion in selection of a converter. However, the case study here above presents a possible generator design that was not specially designed for the PPMC. A reduction of the leakage inductance (x''_d) of two would already push the PPMC into a more eligible converter for the AG application. The design margins of the generator are not discussed here because this is beyond the scope of this work. However, it is clear to the author that reducing the leakage reactance of the stator winding is not obvious, moreover dividing it by two would require a considerable effort in the machine design. It should be the object of a study. As the SM is de-synchronized, there may be a collection of design constraints relative to stability of the machine connected to the grid that are no more relevant for the AG application.

7.2 Perspectives

This work has focused on the detailed understanding of the commutation cell of the PPMC that is influenced by the protection circuit. This study was necessary in order to express the energetic properties of the PPMC which is an important knowledge. There are of course a lot of other points of interests concerning this topology and other points to develop in order to compare it with other existing topologies. There are also some ideas in order to enhance the efficiency of the PPMC.

Improvement of PPMC

- **Investigate active protection circuits**
  In chapter 4, an alternative solution for the protection circuit was mentioned and briefly assessed. It was an active rectifying bridge that would allow to re-inject into the grid the energy losses for each forced commutation (except the switching losses). The active rectifying bridge has shown that it is working only under extended voltage constraints for the switches and for the generator, which makes this solution not eligible. However, the author suggests to use an active protection circuit that, similarly to the passive protection circuit, is connected across each generator phase, but would control actively the overvoltage by re-injecting part of the current into the network, thanks to small isolated inverters and dedicated control.
- **Understand deeper the constraints of the generator design for the AG application**
  The design of the generator connected to the PPMC plays a key role in the determination of the efficiency the PPMC using passive protection circuit. A deeper modeling of the generator and a redefinition of the design rules for a de-synchronized generator could lead to a better efficiency of the PPMC.
- **Extend feasibility evaluation of the two stages variant of the PPMC**

To drastically reduce the number of required switches for the PPMC, the two stages topology briefly presented in chapter 3, should be investigated in more details to state its feasibility.

Further investigations on PPMC feasibility

- **Evaluation of feasibility of BDS with high blocking voltage and high current capability.** Mainly the difficulty of series and parallel connections of discrete components to meet the total requirements. In particular, synchronous transmission of all gating signals and equilibrium of voltage sharing among the chains of IGCT/IGBT.
- Evaluation of feasibility of the passive protection circuit in terms of volume and weight.
- Evaluation of constraints on the current and voltage derivatives for EMC and limitations of silicon devices and capacitors.
- Completion of current control algorithm and associated output power dynamic performances
- Evaluation of fault tolerances and redundancy of PPMC topology

The small scale experimental set-up

- **Extend use of set-up for verification of theoretical calculations**
- Upgrade control hardware to meet execution time requirements
- Implement current control
- Improve security and packing for the use of the set-up as a didactic tool and for experimenting poly-phased converters.

AG project

- Comparison PPMC with other existing topologies
- Review the recommendation to use direct conversion. In particular, comparison of installed capacitor (and other passive elements) between PPMC and indirect converters (DC link)
- Economic comparison
- Assessment and use of emerging new topologies, e.g. the Modular Multi-level Converter (MMC)

The present PhD work will help go through those perspectives by constituting a base knowledge of the PPMC. Stakeholder of the AG project should however seriously consider the new emerging Modular Multi-level Converter (MMC) topology ([58], [31] and [32]) which has a very robust concept of sharing the voltage among high number of levels so that blocking voltages of valves are within reachable values for one discrete element, this sharing concept also delivers very good redundancies, a must in high power converters. The MMC uses in a clever way the silicium for high voltages. Therefore, for the AG project, a MMC topology should be used only on the high voltage side of the transformer, meaning that the frequency conversion is performed on the high voltage side. Hence, the converter deals with relatively low currents.

Nomenclature

Abbreviations

ADC	Analog to Digital Converter
AG	Active Generator
ASM	Asynchronous Machine
BDS	Bi-directional switch
CHP	Combined Heat and Power
CWC	Cosine Waveform Crossing
DAC	Digital to Analog Converter
DFIM	Doubly Fed Induction Machine
DSP	Digital Signal Processor
DTFT	Discrete Time Fourier Transform
EMC	Electro-Magnetic Compatibility
FFT	Fast Fourier Transform
FPGA	Field of Programmable logic Gate Array
FSC	Full Scale Converter
GCD	Greater Common Divider
GT	Gas Turbine
IC	Integrated Circuit
LEI	Laboratoire d'Electronique Industrielle
NCC	Naturally Commutated Cyclo-converter
NCMC	Naturally Commutated Matrix Converter
NPC	Neutral Point Clamped Converter
OMCC	Optimization-based Multi-variable Current Controller
PCC	Point of Common Connection
PI	Proportional Integral

PPMC	Poly-Phased Matrix Converter
RLC	refers to a resistive-inductive-capacitive circuit
rms	root mean square
SM	Synchronous Machine
SPI	Serial Port Input
VSC	Voltage Source Converter

Symbols related to generator

m	number of generator stator phases (or number of input phases)
EMF	Electro-magnetic force of the generator (ideal induced voltage of stator winding)
I_g	stator winding current
V_g	stator winding voltage
L_g	stator winding leakage inductance (sub-transient)
R_g	stator winding resistance
r_g	R_g relative to Z_g
F_g, ω_g, T_g	electrical frequency resp. pulsation resp. period
X_g	stator winding leakage reactance (sub-transient)
x_g	X_g relative to Z_g
Z_g	stator winding impedance R_g+jX_g
I_{short}	stator short circuit capability
i_{short}	I_{short} relative to load current I_o
$Z_{N,m}$	nominal impedance of poly-phase generator
x''_d	direct sub-transient stator winding reactance referred to $Z_{N,gen}$

Symbols related to snubber

V_s	Snubber voltage
I_s	Snubber current
V_{sc}	Snubber capacitor voltage
R_s	Snubber resistance
C_s	Snubber capacitance

R_{base} Base resistance for snubber design

C_{base} Base capacitor for snubber design

r_s relative snubber resistance

c_s relative snubber capacitance

I_{dis} capacitor discharge current (when short circuited)

$E_{loss,1forced}$ energy lost in R_s for one forced commutation

$E_{loss,full\ forced}$ energy lost in all m R_s during one output period with converter in full forced mode

$E_{loss,1Nat}$ energy lost in R_s for one natural commutation

E_{loss} energy lost in all m R_s during one output period with converter in mix mode

e_{loss} E_{loss} relative to $E_{loss,full\ forced}$

Symbols related to PPMC

I_o load or converter output line current

$I_{N,o}$ load or converter nominal output line current

$I_{outgoing}$ refers to the commutation cell, current of the outgoing phase

$I_{incoming}$ refers to the commutation cell, current of the incoming phase

$V_{cR,}$ V_{cS}, V_{cT} converter output phase voltage R, S and T (related to neural point of load)

V_{cRS} Converter output line voltage (between R and S)

F_c , T_c commutation frequency resp. period

Symbols related to load (AC grid)

V_{grid} grid phase voltage

F_o, ω_o, T_o grid electrical frequency, resp. pulsation, resp. period

$Z_{N,grid}$ nominal impedance

Z_t transformer impedance (short circuit model)

X_t transformer reactance (short circuit model)

R_t transformer resistance (short circuit model)

L_t transformer inductance (short circuit model)

pf, φ_{pf} load power factor and associated angle (at PCC)

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Curriculum Vitae

Antoine Béguin
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Experience

2007 – 2011	PhD student in the Laboratory for Power Electronics, Swiss Institute of Technology, Lausanne - Practical realization of a Poly-phased Matrix Converter (1kW) - Teaching assistant for student master projects and student exercise sessions
2007	Internship (6 month) at Alstom (CH) – Birr - Development of the control software of a power electronic installation
2006 – 2007	Assistant in the Laboratory for Electrical Machines – Swiss Institute of Technology, Lausanne - Development of a "hardware in the loop" simulation software

Education

2007 – 2011	PhD student in the Laboratory for Power Electronics, Swiss Institute of Technology, Lausanne
2001 – 2006	Master in Electrical and Electronic Engineering (specialization in energy) at the Swiss Institute of Technology, Lausanne Master project: *Battery Energy Storage Systems*. Optimisation and sizing of battery-based energy storage system for peak load shaving applications. Collaboration with the Laboratory for Power Sytems and ABB Corp. Research Center (Dättwill, CH)
2003 – 2004	3rd year of bachelor abroad at the University of Waterloo, Ontario, Canada

Conferences / Publications

A. Béguin, A. Rufer, *Poly-Phased Matrix Converter - A 27 input phases to 3 output phases experimental set-up running with hard and soft commutations,* EPE 2011, European Power Electronics Conference, Birmingham, UK.

A. Béguin, A. Rufer, A. Lacaze, *Convertisseur Matriciel Polyphasé pour générateurs synchrones de grande puissance – Dimensionnement de la protection contre les surtensions lors de commutations forcées*, EPF 2010, Conférence sur l'Electronique de Puissance du Futur, St-Nazaire, France.

A. Béguin, A. Rufer, A. Lacaze, *Poly-Phased Matrix Converter for large Synchronous Generators – Design of the Voltage Surge Protection,* EPE 2009, European Power Electronics Conference, Barcelona, Spain.

A. Béguin, P. Allenbach, S. Keller and J.-J. Simond. *Hardware-in-the-Loop Simulation Software for regulator tests and optimization,* Industry Applications Conference, 2007, 42nd IAS Annual Meeting, New Orleans, USA.

A. Oudalov, R. Cherkaoui and A. Béguin. *Sizing and Optimal Operation of Battery Energy Storage System for Peak Shaving Application,* IEEE Powertech, July 1-5 2007, Lausanne, Switzerland.

Languages	
French	mother tongue
English, German	fluent (B2 – C1)