Accumulation-Mode GAA Si NW nFET with sub-5 nm Cross-Section and High Uniaxial Tensile Strain

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***Abstract*— In this work we report dense arrays of highly doped gate-all-around Si nanowire accumulation-mode nMOSFETs with sub-5 nm cross-sections. The integration of local stressor technologies (both local oxidation and metal-gate strain) to achieve $\geq$ 2.5 GPa uniaxial tensile stress is reported for the first time. The deeply scaled Si nanowire shows low-field electron mobility of 332 cm^2/V.s at room temperature, 32% higher than bulk mobility at the equivalent high channel doping. The conduction mechanism as well as high temperature performance was studied based on the electrical characteristics from room temperature up to $\approx$400 K and a V_{TH} drift of -1.72 mV/K, V_{FB} drift of -3.04 mV/K and an ion impurity scattering-based mobility reduction were observed.**

I. Introduction

Lately, highly single-type doped Si devices such as accumulation-mode (AM) and junctionless (JL) MOSFETs are proposed as straightforward architectures to eliminate some technical limitations of the nano-scale MOSFETs such as ultra-abrupt junctions, allowing to fabricate even shorter channel devices [1]-[3]. Achieving a high driving current in heavily doped and especially in deeply scaled channels such as multi-gate nanowires and Fins is an engineering challenge due to the limitation of carrier mobility by ionized impurity scattering and the integration of mobility boosters such as local stressors for the suspended channels.

In this paper, we represent a fabrication process to make deeply scaled highly doped sub-5 nm Si nanowires from a top-down SOI platform and integrate it with the local stress platforms, local oxidation [4] and metal-gate strain [5], to include $\geq$ 2.5 GPa uniaxial tensile stress in the channel to boost the carrier mobility in highly doped AMOSFETs, without affecting the I_{ON}/I_{OFF} value.

II. Process flow to make GAA suspended uniaxially tensile strained Si nanowire n-AMOSFET

Fig. 1 represents the process flow. The fabrication process is started using 100 mm (100) Unibond SOI wafers (SOI/BOX= 340/400 nm) with intrinsic p-type doping and 525 μm thickness. The SOI layer was thinned down to $\approx$100 nm by sacrificial dry oxidation. The oxide layer was stripped by BHF and afterward, phosphorous ion implantation (20 keV, 5×10^{13} cm^{-2}) was done in the presence of a 20 nm thick LTO layer as the implantation mask on top of the SOI layer and followed by a 4 hour furnace annealing at 1000 °C to create a nominal 1×10^{18} cm^{-3} n-type SOI layer. Afterward, a hard mask including 15 nm SiO_2 and 80 nm LPCVD Si_3N_4 was grown/deposited on the wafer and later on, dense array ($\approx$8 NW/μm) of 10 parallel Si nanowires in <110> as well as <100> orientations, with 20-60 nm width and 0.5-3.0 μm length, together with the S/D pad patterns were written using e-beam lithography (150 nm thick negative tone XR-1541-006 HSQ, exposure parameters in Vistec EBPG5000: 100 keV, 3000 μC/cm^2 dose).

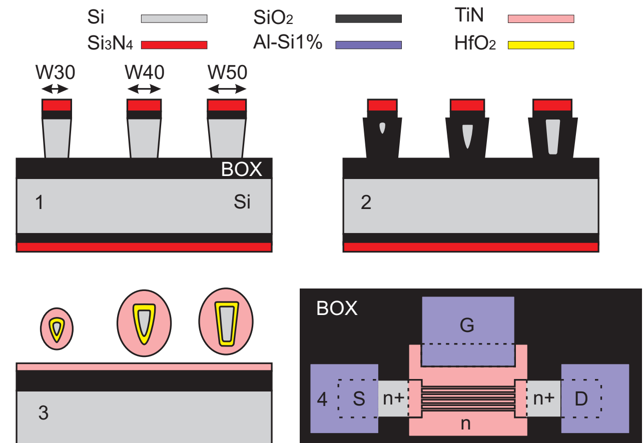

Fig. 1. Process flow to make GAA Si nanowire AMOSFETs. W30 represents the initial 30 nm nanowire width on the mask.

The hard mask was etched using an anisotropic fluorine based dry etching and afterward, the SOI device layer was etched using a HBr/O_2 based dry etching to create slanted Si side-walls to shrink the width further along the Fin to be able to deplete the highly doped channel properly (see Fig. 2). To reduce the Fin width even below 10 nm, round the sharp Si corners as well as accumulate uniaxial tensile stress in the suspended Si nanowire [4], a 7 hour stress-limited dry oxidation at 925 °C (0.500 L/min O_2, 10.00 L/min N_2), to consume nominally 9 nm of (100) Si, in the presence of the tensile nitride hard mask was done. It is worth mentioning that the Si consumption on the slanted Si side-walls was observed to be $\approx$40% higher than (100) Si surface. As Figs. 1, 3 and 4 represent, Si nanowires with triangular as well as trapezoidal cross-sections can be achieved based on the initial width of the Fins before oxidation.

Hot phosphoric acid (155 °C) was used to strip the nitride

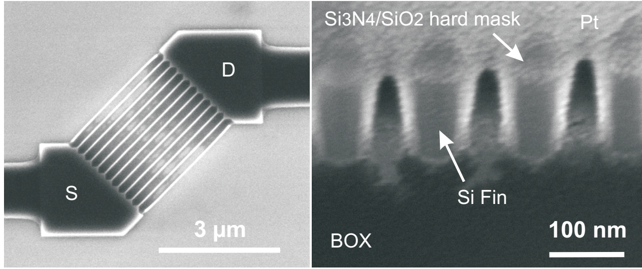

Fig. 2. SEM picture of a HSQ pattern including 3 μm long and 25 nm wide array of nanowires in <100> orientation (left); SEM picture of Si Fins with ≈88.6° slanted side-walls, obtained using HBr/O_2 chemistry (right).

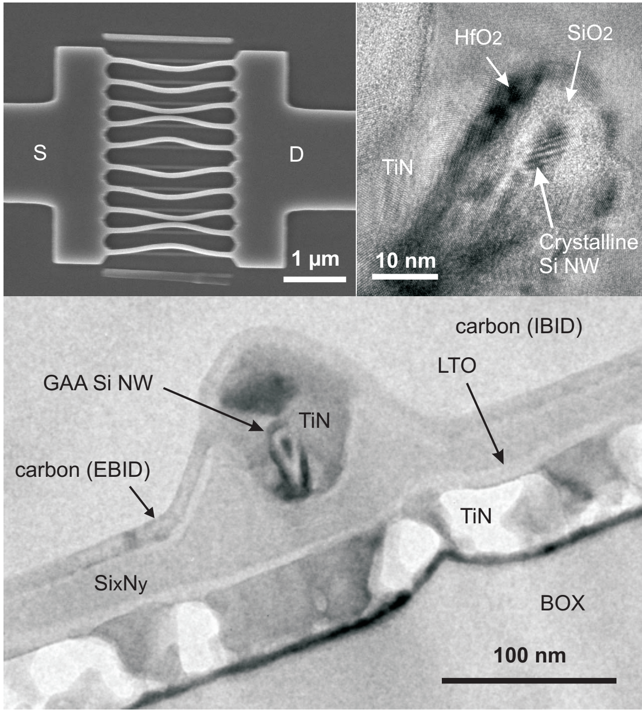

Fig. 3. SEM picture of a buckled array of GAA Si nanowires after the gate stack step (left); TEM picture from the channel (right); TEM picture from the cross-section of a GAA nanowire (bottom). The cross-section of the Si nanowire is triangular with $W_{top} \approx 4$ nm.

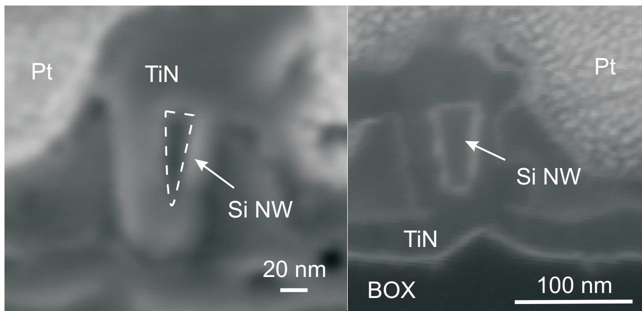

Fig. 4. SEM pictures from the cross-section of the GAA triangular (W40) and trapezoidal (W50) Si nanowires, after the gate stack step.

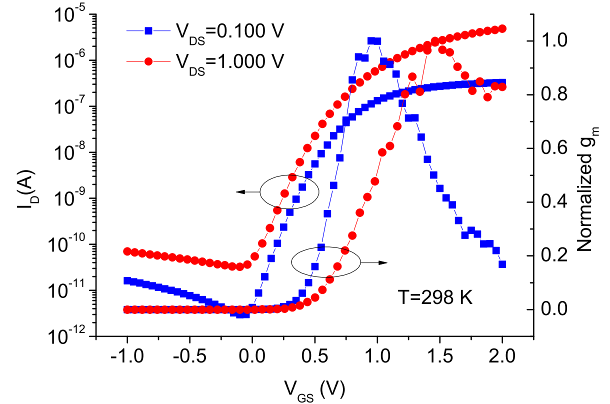

Fig. 5. Transfer and transconductance characteristics of a GAA uniaixially tensile *strained* Si nanowire AMOSFET at 298 K. The g_m values were normalized to the g_m peaks (3.8×10^{-7} and 5.0×10^{-6} S for V_{DS}=0.100 and 1.000 V, respectively).

hard mask. Afterward, RCA (including 8 min HF dip to strip the grown SiO_2 as well as suspend the nanowires from the substrate), 5 nm HfO_2 deposition by ALD, RTA annealing (600 °C, 15 min) and finally, 50 nm TiN deposition by sputtering were done to make the gate stack as well as accumulate more uniaxial tensile stress in the nanowires [5]. Fig. 3 represent an array of buckled Si nanowires right after the gate stack step, with the depicted TEM cross-sections. By assuming a Gaussian buckling profile along the Si nanowire, the average uniaxial tensile stress value is estimated to be ≥ 2.5 GPa, considering only the represented in-plane buckling. The actual stress level can even reach a higher value in the case of an out-of-plane buckling.

Gate patterning (including a 50/10 nm of LPCVD Si_xN_y/LTO mask, optical lithography and metal-gate/high-k etching), S/D ion implantation and annealing, metallization (Al-Si1%) and finally, post-metal annealing (450 °C, 30 min) were the further steps.

III. Electrical Characterization

The electrical characterization was carried out at different temperatures using a Cascade prober and a HP 4155B Semiconductor Parameter Analyzer. Figs. 5 and 6 represent the transfer, transconductance and I_D-V_D characteristic of a GAA AMOSFET including an array of 10 deeply scaled Si NWs in <110> orientation at room temperature. The <110> orientated Si nanowire devices were chosen simply to investigate the highest uniaxial tensile stress-induced performance [6]. The I_D-V_G characteristics of the same device at 298-398 K with a 25 K step were plotted in Fig. 7 (depicted TEM picture in Fig. 3), for further study of the conduction mechanism in the highly doped deeply scaled AMOSFETs.

IV. Extraction of Parameters and Discussion

A. Conduction mechanism in the accumulation-mode

As described in [7] and depicted in Fig. 8, both AM and JL MOSFETs are operating similarly in the subthreshold region

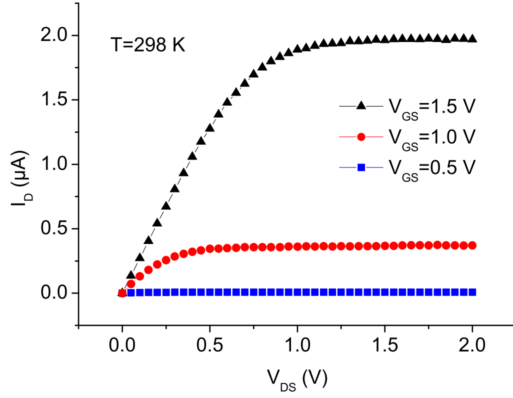

Fig. 6. I_D-V_D characteristics of a GAA uniaxially tensile *strained* Si nanowire AMOSFET at 298 K.

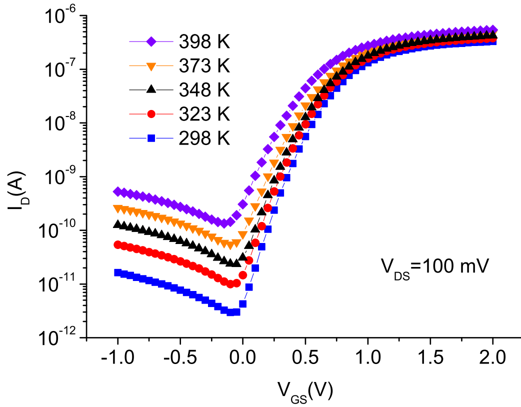

Fig. 7. Transfer characteristics of a GAA uniaixially tensile *strained* Si nanowire AMOSFET at different temperatures.

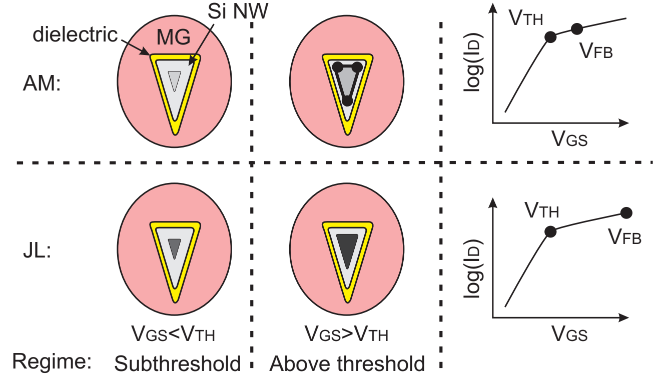

Fig. 8. The conduction path in GAA accumulation-mode and junctionless MOSFETs in different regimes.

($V_{GS} < V_{TH}$), considering the main conduction in the bulk channel (the middle of the nanowire). In an AMOSFET, the flat-band condition is pretty close to the threshold voltage and the accumulation layer will be created right after reaching the flat-band condition. On the other hand, a heavily doped JL MOSFET, due to having the main current in the bulk channel above the threshold voltage, mainly operates below the flat-band voltage and the flat-band condition will be reached after reaching the density of carriers on the surface to the donor doping concentration in the channel.

According to [8], the accumulation current in the linear regime ($V_{DS} < V_{GS} - V_{FB}$) can be calculated by:

$$I_D = \mu \cdot C_{ox} \cdot W_{eff}/L \cdot [(V_{GS} - V_{FB}) \cdot V_{DS} - 0.5 \cdot V_{DS}^2] \quad (1)$$

where μ, W_{eff}, L and C_{ox} are mobility, effective channel width, channel length and gate oxide capacitance, respectively. By assuming the accumulation current as the major current in the nanowire while operating in the linear regime (neglecting the conduction from the middle of the nanowire in comparison to the surface accumulation current) and considering the $I_D/\sqrt{g_m}$ method [9], the low-field mobility as well as the flat-band voltage can be extracted independent of series resistance and mobility attenuation factor. The extracted low-field electron mobility at V_{DS}=100 mV is 332 cm^2/V.s, 32% higher than bulk Si electron mobility at the same level of doping (1×10^{18} cm^{-3}) [10], which is an evidence of including uniaxial tensile stress in the channel, and possibly a higher level can be achieved in this level of stress [6] in the case of having optimum quality of the dielectric and dielectric-channel interface especially for the deeply scaled channels [11].

B. Scattering mechanism in a deeply scaled highly doped Si nanowire

Fig. 9 depicts the low-field electron mobility at different temperatures for a single deeply scaled AMOSFET device. According to [12], the carrier mobility is varying by temperature according to the following trend:

$$\mu(T)/\mu(T_0) = (T/T_0)^{-\gamma} \quad (2)$$

where T_0=298 K. According to Fig. 9, γ=0.966 which is quite lower than 2.5, reported for the GAA low doped Si nanowire MOSFETs [13], and in line with the previous reports for intrinsic or low-doped Si [14] being explained by the dominant role of ionized impurity scattering in highly doped Si MOSFETs, even for deeply scaled Si nanowires.

C. Flat-band and threshold voltage extractions

By considering (1), the flat-band voltage of an AMOSFET can be extracted using the $I_D/\sqrt{g_m}$ method [9], independent of series resistance and mobility attenuation factor. The threshold voltage of a MOSFET, in general, can be extracted using the transconductance change (TC) method [15], quasi-independent of series resistance and no need to any accurate analytical model. Interestingly, as shown in Fig. 10, the TC peak is located almost at the expected (theoretical) threshold voltage from the linear part of the transfer characteristic, providing systematically a smaller value than V_{FB} [7].

Fig. 11 represents V_{TH} drift of -1.72 mV/K (smaller than -2.1 mV/K, the prior reported value for a deeply scaled GAA low doped Si NW in [13]), V_{FB} drift of -3.04 mV/K and

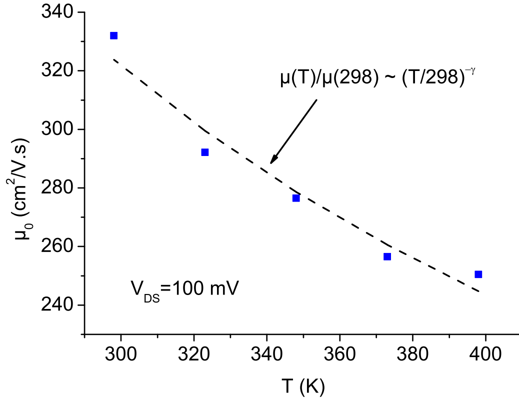

Fig. 9. Low-field electron mobility dependence on temperature for a GAA uniaxially tensile *strained* Si nanowire AMOSFET. The extracted γ is 0.966.

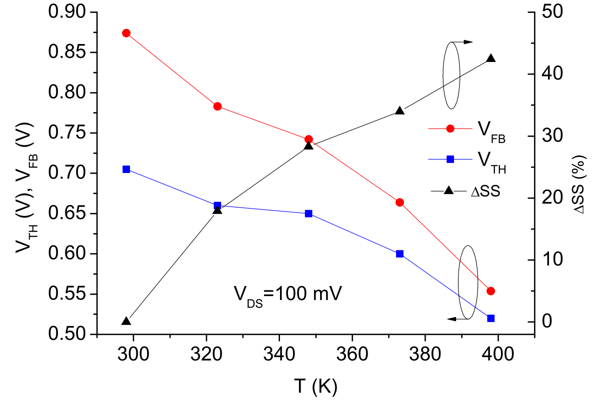

Fig. 11. Temperature dependence of threshold voltage, flat-band voltage and subthreshold slope of a GAA uniaxially tensile *strained* Si Nanowire AMOSFET.

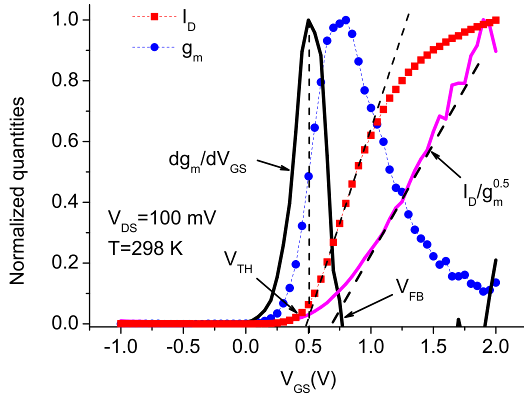

Fig. 10. V_{TH} and V_{FB} extraction of an AMOSFET using the transconductance change [15] and $I_D/\sqrt{g_m}$ [9] methods.

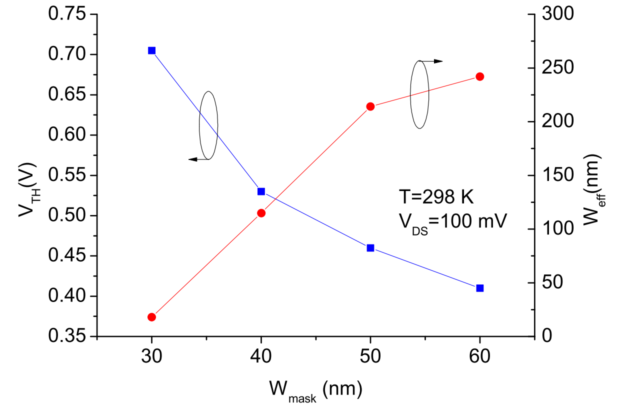

Fig. 12. Threshold voltage of different transistors with 2.0 μm long Si nanowires at room temperature and the effective width variation of the nanowire vs. the initial nanowire width on the mask.

subthreshold slope change of 0.404%/K (with subthreshold slope of 106 mV/dec. at room temperature). According to Fig. 11, the flat-band voltage is becoming closer to the threshold voltage at higher temperature. This observation needs further experimental investigation and device simulation to understand its origin.

Finally, as a comparison to the GAA deeply scaled Si NW AMOSFET, the transistors including the same channel length but wider Si nanowires were characterized at room temperature and the threshold voltage as well as the corresponding effective channel width per nanowire were plotted in Fig. 12.

V. Conclusion

We demonstrated the first accumulation-mode GAA Si nanowire nMOSFET with cross-section smaller than 5 nm on a SOI substrate with an electron mobility boost due to $\geq$ 2.5 GPa uniaxial tensile stress by local bending and reported its performance from 298 K to 398 K.

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