

Solution-deposited carbon nanotube network TFTs on glass and flexible substrates

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Abstract We have developed a process to produce carbon nanotube network thin-film transistors on glass and on flexible plastic substrates. The carbon nanotube network is deposited by spin- or spray-coating from surfactant solution which are both time- and cost-saving deposition techniques and can be applied to large area substrates. The TFTs reach on/off ratios of more than five orders of magnitude and effective charge carrier mobilities of above $1\text{cm}^2/\text{Vs}$. These values promise an application in active matrix liquid crystal displays (AMLCD) or flexible electronics. Issues that need to be addressed are the homogeneity and reproducibility of the electrical device properties.

1. Introduction

Like in conventional semiconductor technology the market of thin-film transistors is strongly dominated by silicon. The used processes have been developed and optimized over decades. The high investment and production costs and the desire to use flexible substrates have led many groups to research new materials and production techniques.

Organic semiconductors have received a lot of attention since they have a better compatibility to plastic substrates and can be deposited by evaporation or from solution with techniques like inkjet printing. Major drawbacks are degradation under ambient air and low charge carrier mobilities [1].

Carbon nanotubes (CNT), which were first discovered in 1991 [2], can act as a semiconductor as well. The first transistor based on a single nanotube was presented in 1998 by Dekker et. al. [3]. The special structure of the nanotubes gives them a unique combination of properties. High flexibility, the chemically very stable structure, operation at high frequencies [4] and charge carrier mobilities over $10.000\text{cm}^2/\text{Vs}$ in single semiconducting nanotubes [5] make them a promising candidate for thin-film electronics especially on flexible plastic substrates.

We have developed a process to produce thin-film transistors with carbon nanotube networks as the semiconductor [6]. The nanotubes are deposited vacuum free from solution by spin- or spray-coating which is very cheap and timesaving compared to deposition techniques like PECVD, which is com-

monly used in silicon thin-film production. The advantage of the process is that it can be applied to glass and flexible plastic substrates. Fig. 1 shows an image of a fully processed plastic substrate.



Fig. 1: Carbon nanotube network TFTs on a flexible $50\times 50\text{mm}^2$ substrate.

2. Carbon nanotubes

Single walled carbon nanotubes (SWCNT) can be described as a rolled up sheet of graphene, which is a monolayer of hexagonally ordered carbon atoms. Theoretically this can be realized in almost any diameter and with different chiralities. The electrical behavior of a single nanotube however depends strongly on its geometry. From all possibilities one third of the nanotubes behave like a metal, the other two thirds are semiconducting with an increasing bandgap for a decreasing diameter [7].

In the growth process the diameter range is confined to values between roughly 1-2nm, depending on the used method and parameters, with the aforementioned mix of metallic and semiconducting nanotubes. It was reported that certain growth conditions give preferred geometries [8], however until now it is not possible to grow only one type of nanotubes.

The separation of metallic from semiconducting nanotubes is of high interest for many applications and different methods have been presented in the last years [9] [10] [11]. Scalability, effectiveness, process stability and the degree of separation are still issues though. So far it is not possible to purchase solely semiconducting nanotubes.

3. CNT networks as semiconductor

The lack of techniques to reproducibly place nanotubes in a certain position and orientation makes it impossible to use single nanotube devices for low cost thin-film electronics or active matrix applications.

Random networks of carbon nanotubes in contrast can easily be deposited from solution with low cost techniques like spin- or spray-coating. Because of the usually higher amount of semiconducting CNTs a low density network of nanotubes can act as a semiconductor [12].

The density of the network needs to be adjusted so that current paths from one contact to the other always contain at least one semiconducting part.

4. Preparation of the CNTs

Due to high Van-der-Waals forces carbon nanotubes tend to form bundles, so called ropes. To separate the nanotubes they are dispersed in an aqueous surfactant solution using ultrasound. The surfactant forms micelles around the nanotubes. Because of positive charges at the outer side of the micelles the nanotubes are kept separated and the dispersion is stable over months.

Bigger bundles and other impurities like clusters of carbon or metal particles from the growth process are removed by ultra-centrifugation and decanting of the supernatant.

We are using single walled carbon nanotubes produced by the arc-discharge technique.

5. Device fabrication

As substrate we are using display grade glass or polyethersulfone (PES) foils in the size of $50 \times 50 \text{mm}^2$. An upscaling to larger area substrates is planned for future work. The design of the produced devices is bottom gate, top contact. Therefore the first step is the deposition of the gate metal. Sputtered aluminum is used and patterned by standard lithography.

The gate dielectric of aluminum oxide is formed on top of the metal by anodic oxidation in an electrolyte [13]. A voltage is applied between the metal as the anode and a cathode, hydrogen peroxide is used as electrolyte. The thin natural oxide layer grows by a transport of ions from the metal into the oxide and negative charged oxidizing ions from the electrolyte into the oxide. Joining positive and negative ions form the gate oxide which grows in both directions [14]. The thickness is determined by the applied voltage. The advantages are vacuum-free room-temperature processing, a high relative dielectric constant of $\epsilon_r \approx 9$ and a low roughness and defect density. The latter is because of the self adjusting, current driven process. At defects the current density is increased which leads to a faster growth of the oxide.

A self assembled monolayer (SAM) of 3-aminopropyltriethoxysilane is applied to the surface of the substrate in a bath to improve the adhesion of the nanotubes to the oxide.

The CNTs are then deposited from the surfactant solution by spin-coating. Since the micelles would impede the adhesion of the nanotubes to the substrate surface as well, a stream of an organic solvent is simultaneously applied, which removes the micelles. Fig. 2 shows the spin-coating setup.



Fig. 2: Spin-coating system with one stream of CNT-dispersion and one stream of organic solvent.

Another possibility is to spray-coat the nanotube layer. This can be done using an off-the-shelf airbrush. Heating the substrate to around 80-100°C accelerates the evaporation of the water and prevents the formation of bigger droplets.

Independent of the deposition technique the substrates need to be rinsed afterwards to remove the residual surfactant.

The source and drain contacts made of e-beam evaporated Palladium are formed on top of the nanotube layer by standard lithography and liftoff. The TFT channels have widths between 50µm and 200µm and lengths between 5µm and 100µm.

To minimize leakage currents the nanotubes outside the channels are removed. This is done by protecting the channels with patterned photoresist and cleaning the whole substrate with a CO₂ snowjet [15]. After the removal of the photoresist in an acetone bath the devices are ready for characterization.

Fig. 3 shows the concept of a carbon nanotube network TFT and a microscope image of an actual device.

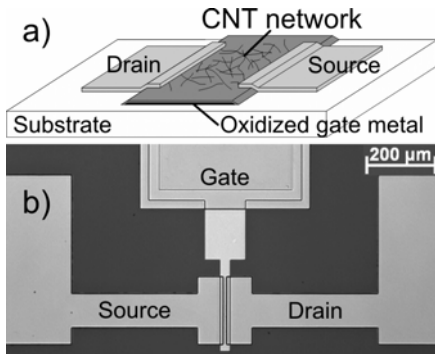


Fig. 3: a) Concept of the carbon nanotube network TFT b) microscope image of a TFT with $W=200\mu\text{m}$ and $L=10\mu\text{m}$.

6. Device characterization

We are using a radial design (see Fig. 1) where the channel from source to drain is either tangential or radial to the substrate center. With this design we are able to see if the spin-coating leads to a preferential alignment of the nanotubes and also gives us information about the radial dependency of the network density.

A Keithley 4200 semiconductor characterization system was used for TFT measurements. The values for the device charge carrier mobilities are calculated using Equation (1), where L and W are the

length and the width of the TFT channel, d is the thickness of the gate oxide, $V_{sd}=0,1\text{V}$ and $\epsilon_0=8,854\cdot 10^{-12}\text{F/m}$, in the linear region of the transfer characteristics.

$$\mu = \frac{L \cdot d}{W \cdot \epsilon_0 \cdot \epsilon_r} \cdot \frac{dI_{sd}}{dV_g} \cdot \frac{1}{V_{sd}} \quad (1)$$

Since the nanotube channel is composed of individual and mostly separated tubes instead of a bulk material that covers the area $L \cdot W$ the calculated value is relevant only in the context of comparing the TFTs to other devices with the same dimensions. The actual charge carrier mobility of the individual nanotubes themselves is much higher.

7. Results and discussion

The electrical performance of a CNT-network TFT can not only be influenced by the channel geometry, but also by the density of the network. A low density network which is just above the percolation threshold will give the biggest field-effect. Due to the small amount of paths the current can take, the maximum driving current will be limited though. The TFTs will have a high on/off ratio, but also a low device charge carrier mobility.

For higher network densities the current paths increase, but larger parts get shorted by metallic nanotubes which results in a higher off-current. Although the on-current increases as well the TFTs will have lower on/off ratios. The device charge carrier mobility on the other hand will rise since the current can take more paths in the channel region.

Fig. 4 shows on/off ratio vs. device charge carrier mobility for a batch with relatively dense spin-coated CNT-networks.

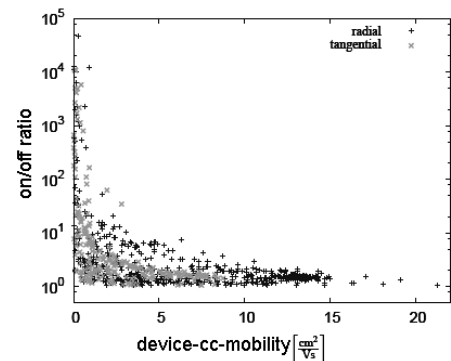


Fig. 4: On/off ratio vs. device charge carrier mobility for several devices with spin-coated higher density CNT-networks. The values are separated in two groups with source-drain channels tangential or radial to the spinning center.

The above mentioned correlation of the two properties can clearly be seen. The separation into devices with tangential or radial oriented channels shows only small differences. The devices with a tangential oriented channel tend to higher on/off ratios. As was reported in [16] this is the case for devices where the nanotubes are oriented along the channel from source to drain. Further analyses have to show if this is really the case.

Transfer characteristics for devices on glass and on plastic are displayed in Fig. 5a). The devices show on/off ratios of around five orders of magnitude and above, the channel geometry, device charge carrier mobility and subthreshold swing are noted in the plot. A transfer and output characteristic of a device on glass is displayed in Fig. 5b).

Reported values for mobility and on/off ratio for similar devices show that the overall performance can be improved even without the removal of metallic nanotubes [17].

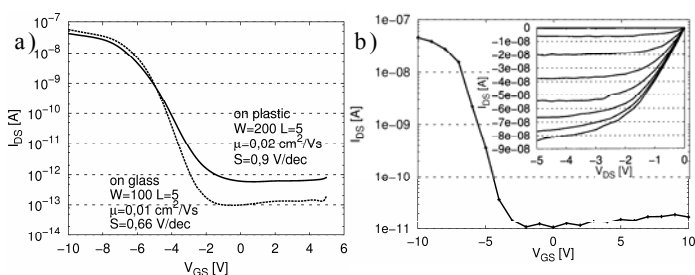


Fig. 5: a) Transfer characteristics of devices on glass and plastic with on/off ratios of $5 \cdot 10^4$ and $4 \cdot 10^5$ b) transfer and output characteristic of a device on glass with $W=200 \mu\text{m}$ and $L=100 \mu\text{m}$.

8. Conclusions and outlook

With our process it is possible to produce CNT-network TFTs on glass and flexible substrates. Apart from the metal deposition for source/drain and gate it involves only vacuum-free low-cost techniques that can be applied to large area substrates. Depending on the density of the nanotube network the devices show charge carrier mobilities of above $1 \text{cm}^2/\text{Vs}$ and on/off ratios of more than 10^5 . Metallic CNTs in the network prevent to get maximum values for both at the same time.

Problems that need to be solved are the homogeneity and reproducibility of the device characteristics as well as to get a high on/off ratio and device charge carrier mobility at the same time.

We expect that availability of separated

semiconducting nanotubes with a significantly reduced share of metallic nanotubes will solve these challenges in the near future.

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