Ambipolar silicon nanowire FETs with stenciled sub-µm metal gate

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Keywords: Schottky barrier, ambipolarity, Si nanowire, stencil lithography, FET, silicide.

Future technological innovations enabling ever higher circuit densities predicted by Moore's law will most likely be concentrated on novel materials, innovative device structures, and significant modifications of the traditional planar transistor design. Considering novel device structures, the nanowire (NW) channel transistor with FinFET construction has been demonstrated to be one of the best in terms of electrostatic control, thus enabling further device scaling [1]. Device ambipolarity can be exploited to pack more functions per chip, without the use of exotic materials such as CNTs or graphene [3]. We report on a fully CMOS compatible fabrication of ambipolar SiNW FinFETs by means of amorphous Si (a-Si) and low temperature LPCVD oxide (LTO), as for monolithic 3D integration [2]. FinFETs with stencilled Al gates are successfully co-fabricated with polysilicon gated devices. Stencil lithography [4] is envisaged as a key enabler for gate patterning on 3D structures, such as vertically-stacked nanowire transistors [5].

The fabrication process starts by oxidizing 500 nm of Si wafers in wet atmosphere. A 100 nm LTO layer is deposited, followed by a 100 nm a-Si deposition at low thermal budget. Lines of widths between 100 nm and 500 nm are patterned with diluted HSQ using e-beam lithography. The HSQ lines are used as mask for SiNW anisotropic etching. Then a 40 nm dry oxidation followed by a 50 nm LPCVD polysilicon deposition are performed. Polysilicon is patterned to form pad areas for electrical characterization as well as gates with lengths between 1µm and 10µm in 50% of all devices, the other half being designed for stenciled gate (see Fig 1). A bi-layer of 20nm Ti/55nm Ni is patterned with lift-off to form electrical contacts between the NWs and the pads. Then NiSi silicide is formed with a 400°C annealing to obtain mid-gap Schottky source/drain contacts as well as for a-Si possible crystallization [6]. The last step consists of depositing 100 nm thick Al on the remaining half of the devices through an aligned nanostencil , for gate lengths between 100 nm and 1 µm (see Fig.2).

Electrical characterizations are carried out with a HP4156C semiconductor parameter analyzer. The I_{ds}-V_{gs} curves (see Figs 3 and 4) demonstrate device ambipolarity for both polysilicon and Al gates with I_{ON}/I_{OFF} ratios of more than 6 orders of magnitude. The lower Schottky barrier for holes than for electrons is reflected into the higher current (I_{ON}) level for the p- branch than for the n- branch. The lower current for the n-branch in the Al gated devices might be due to metal gate-induced doping. The minimum peak of the conductance shows a shift that is attributed to the difference in gate work functions. Polysilicon gated inverter (see Figs 5 and 6) operation with a gain of 4 is demonstrated for different voltage biasing, enabling the construction of more complex circuits. Al gated inverters are currently under investigation.

In conclusion, a fully CMOS compatible fabrication flow using low temperature a-Si LPCVD and stencil lithography has been developed and proved suitable for SiNW FinFETs having ambipolar conductance. The stencil mask has been demonstrated to be a real option for sub-micrometer metal gate patterning for the first time. It is worth noting that the flexibility of this process enables the deposition of several gate materials, bypassing the conventional fabrication issues related to material etch selectivity. Finally, the excellent performance of individual FinFETs paves the way for the fabrication of more complex circuits.

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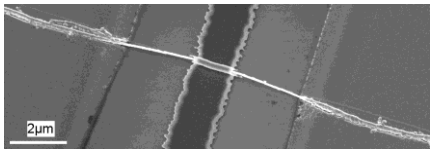

Figure 1. Si NW transistor with 100 nm x 70 nm channel cross-section and 2 µm polysilicon gate.

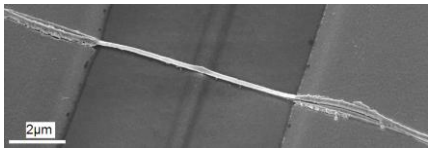

Figure 2. Si NW transistor with 150 nm x 70 nm channel cross-section and 700 nm stenciled Al gate.

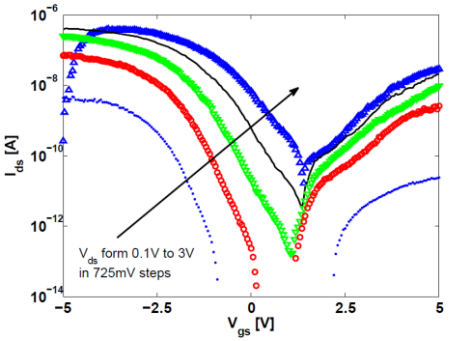

Figure 3. I_{ds}-V_{gs} curve of a FET with 1 µm long LPCVD polysilicon gate obtained by dry etching.

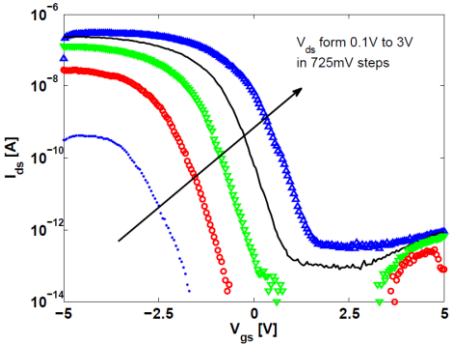

Figure 4. I_{ds}-V_{gs} curve of a FET with 1 µm long PVD Al gate deposited through a stencil.

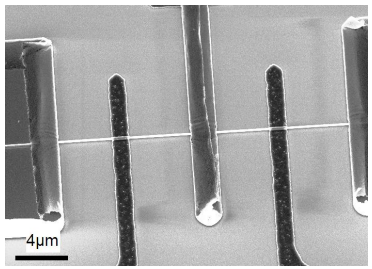

Figure 5. Inverter made with two parallel polysilicon gates and NiSi contacts.

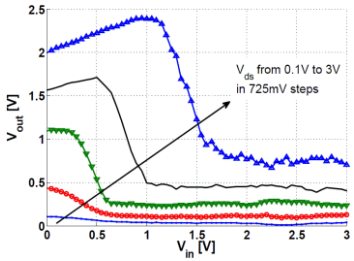

Figure 6. V_{out}-V_{in} transfer characteristic of a polysilicon inverter.