Design Methods and Tools for 3D Integration

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***Abstract*—The design of 3-dimensional integrated circuits requires new specialized tools, methods and flows. Whereas some tools are on the market and some design flows for standard ICs are extended to handle die stacking and through-silicon vias, much R&D has still to address relevant and crucial problems. We can roughly classify design problems and tools into three categories: i) synthesis of 3D structures, ii) analysis, verification and test support, and iii) thermal management. We briefly survey methods and tools addressing these problems.**

***Index Terms*—3D placement, 3D routing, Network on Chip, GALS, signal integrity, power integrity, thermal management.**

I. Introduction

The design and test of *3-dimensional* (3D) *integrated circuits* (ICs) requires specific tools, methods and flows [1]. Since there is a plethora of design tools for planar IC design, most tools for 3D are extensions of those used for planar (2D) integration. An overview of such tools and flows requires to categorize them according to the 3D technology being used and the application domain.

A coarse-grained classification of 3D integration technologies shows two major families: i) integration using chip stacking and *through-silicon vias* (TSVs) and ii) native 3D integration. The latter technology is still in its infancy, requiring specialized tools that are tightly coupled to the process (e.g., LETI's [2]). Thus, we focus on 3D design methods and tools with TSVs. There are various application domains for 3D integration, including, but not limited to, *memory systems*, *processor-memory systems*, and *heterogeneous integration*. These classes of applications differ mainly in the regularity and homogeneity of design, and thus they require tools and flows with specific flavors. Moreover, these applications differ according to the target market, e.g., servers, mobile applications, etc., because the power budget may vary widely. We survey tools and methods for 3D integration across application domains and grouped according to the various design phases.

II. Circuit Synthesis

From a physical design perspective, synthesis can be summarized as *partitioning, placement* and *communication synthesis*. For most current designs, a partition into layers (e.g., dies) is already given, but it is conceivable that future highly-complex digital designs will be split by CAD tools across layers. Placement and floorplanning have always enjoyed a major role in synthesis, as the interconnect length - and hence delay - depends on the placement. In 3D integration, unit-length delays in the horizontal and vertical directions differ, thereby imposing a different set of constraints onto the placement tools. If we look at this problem in more details, a connection between two units on different adjacent layers entails; i) buffering to increase driving capability, ii) a TSV, iii) horizontal wires. Thus, the delay depends much on the relative position of the two units, the TSV and the buffers. This problem is exacerbated by the fact that TSVs are relatively large objects (in the μm range) as compared to transistors and wires. 3D routing can be seen an extension of routing techniques to more layers and directions, while taking into account the anisotropy of the medium.

From a high-level (i.e., functional) standpoint, 3D design is achieved by using building blocks such as processing cores and embedded memories. Structured interconnect solutions for 3D systems involve advanced bus structures (e.g., crossbars) and *Networks on Chips* (NoCs) [3]. 3D NoC tools and flows allow designers to view communication in a 3D system in a structured way, and to distribute and tailor resources (e.g., switches) to optimize performance. Specifically some NoC design approaches support *quality of service* (QoS) bounds as well as trade-off performance with power consumption. Clocking and synchronization in 3D systems can be realized in various ways, ranging from centralized clocking, to multiple-clock domains that may be identified with the layers themselves, to *globally asynchronous, locally synchronous* (GALS) design styles. Overall it is interesting to remark that designing 3D stacks requires both high-level decisions of the computation and communication structure (e.g., NoC synthesis) as well as placement and routing in 3 dimensions.

III. Circuit Analysis

Analysis tools ensure the integrity of integrated systems and the satisfaction of design constraints. First and foremost *timing verification* tools, including *statistical timing analysis* provide us with path delays, detection of critical paths and their possible timing violations. *Signal integrity* is an important issue for 3D ICs due to the physical proximity of the circuits within a multi-plane stack. Although the separation of circuits in more than one plane can reduce substrate noise, coupling between the TSVs and the substrate must be treated carefully. *Reliable clock distribution* is another challenge due the different synchronization schemes that can be supported by 3-D

circuits. In addition to traditional criteria, such as the circuit wire length and area, clock skew variability due to process variations has been shown to considerably differ among the possible distributions of clock domains within a 3-D circuit [4]. This behavior, in turn, makes specific topologies useful for distributing the clock in 3-D ICs.

Power integrity is another critical issue for multi-layer circuits. The reduced footprint of the system (i.e., fewer power/ground pads), the TSVs, and the higher current densities further aggravate the problem of providing a robust power distribution network. Recent publications have suggested first-order models and methods to analyze the behavior of these networks [5], but a complete solution is still lacking. When a 3D stack has dies manufactured by different vendors, the information on the physical design of the layers may be very limited [6]. This restriction complicates significantly the analysis of the global power distribution network and thus new tools must cope with this limitation. Moreover the design of 3-D power distribution networks will be considerably challenged by high current densities and a significant part of the 3D IC may be used for power delivery.

IV. Thermal analysis and control

3D ICs require accurate thermal modeling, because the volumetric density of heat generated is higher (as compared to 2D ICs) and because heat dissipation is harder to achieve. TSVs, and *thermal* TSVs, play a major role in heat distribution and recent research has addressed their thermal modeling. Thermal simulators for 3D systems are much in need. Recent tools [8], [9] use finite-difference methods to generate compact thermal models. The 3D-ICE [10] simulator is specifically designed for transient thermal analysis of 3D stacks, possibly with interlayer liquid cooling, and it supports a detailed interconnect model to evidence the effects of interconnect self-heating.

Early work on thermal control of 3D ICs addressed design-stage optimization, such as thermally-aware floorplanning [11] and integrating thermal TSV planning in the 3D floorplanning process [12]. Recent work has considered the use of dynamic thermal management. Zhu et al. studied several policies for task migration and *dynamic frequency and voltage scaling* (DVFS) for 3D ICs [13]. They explore thermal profiles of adjacent processing elements on the same vertical column (interlayer adjacent) or within the same layer (intralayer). Coskun et al. [14] propose a temperature-aware scheduling method specifically designed for air-cooled 3D systems, which takes into account the thermal heterogeneity among the different layers of the system with any number of tiers. Cooling by fluid convection in microchannels was recently introduced by IBM and others [7]. This technology requires specific tools for analysis and for *dynamic thermal management*. Recent research tools addressed design and evaluation of thermal management policies with fixed/variable flow-rate value [15]. Sabry et al. [16] extended this approach by developing an integral fuzzy controller to handle DVFS and variable flow-rate control. This work combines fuzzy control with a thermal-aware job scheduler to correctly stabilize the temperature on the die (i.e., variations of less than 5 degrees on the die), thus improving the cooling efficiency of dynamic thermal management for 3D ICs without affecting performance.

V. Commercial tools

Commercial vendors are starting to provide offerings for this emerging market. Synopsys has been focusing on specific extensions to their place & route (`IC Compiler`), layout extraction (`StarRC`) and test (`DFT MAX`) tools. Extensions include handling "landing points" (e.g., pads for bumps, TSVs) in place & route, special routing needs, extensions to boundary scan to enable testing a set of chips, modeling parasitic effects of TSVs, etc.. Magma's suite include the `Titan` layout editor, that can handle TSV layout and multiple dies simultaneously. Titan is linked to the `Quartz` 3D layout verification suite, supporting various styles of TSVs and TSV design rules as well as different bonding schemes. Cadence is extending its `Encounter` system to deal with 3D floorplanning (with TSVs), power distribution and timing verification. Other efforts address thermal modeling and circuit extraction. A few other companies, including Atrenta, Docea, Presto and R3Logic, provide (or plan to provide) tools for 3D design. The combination of commercial and research tools address several important problems. Nevertheless integrated tool flows will be necessary to support the growth of the 3D IC market.

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