

Where A_C is the contact area of the source to channel junction, F the electric field across the Schottky barrier, A the Richardson's constant, h the Plank's constant, m the electron rest mass, q the elementary electron charge, ϕ_{Beff} the effective Schottky barrier height, T the temperature, V_a the applied voltage across the Schottky junction, k the Boltzmann's constant.

5. ELECTRICAL CHARACTERISTIC

Ambipolar behavior

All the following measurements investigate the electrical behavior using the handle layer of the wafer as the back gate and the top gate at the source end (gate 1 in Figure 1) for a 20 μm long Schottky barrier Si nanowire FET with 100 nm channel diameter (Figure 1(b)).

A V_{gs} sweep ranging between -5 V and +5 V has been performed at different V_{bg} voltages. Large subthreshold slopes are expected in this kind of devices since the total current is determined by a thermionic emission and a tunneling components (equation (1-3)), giving rise to two distinct subthreshold regimes. We can indeed improve the quasi-static characteristic of the device by exploiting the back-gate to limit the conductance of one type of carrier. As suggested by Lin et al. [5] for a carbon nanotube Schottky barrier FET, a back gate voltage is capable to turn the device from an ambipolar to a unipolar behavior. As shown in Figure 2 the device has an ambipolar behavior, with unbalanced p- and n-branches. Since the gate length of the top gate is shorter compared to the back gate, the main effect we observe by changing V_{bg} is a modification of the ambipolar curve, in particular a modulation of the subthreshold swing together with a strong modulation of the n-branch current by lowering the I_{OFF} current contribution from holes injection at low V_{gs} . Nevertheless, if on the one hand the V_{bg} can be used to improve the ambipolar $I_{\text{ds}}-V_{\text{gs}}$ curve, on the other side the lower I_{OFF} becomes more sensitive to temperature variation, which is suitable for temperature sensing applications.

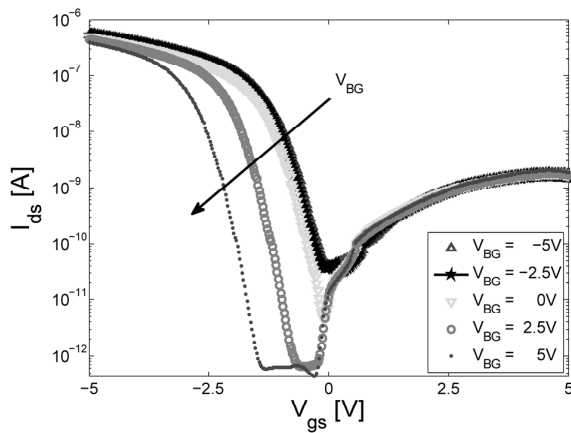


Figure 2: Effect of the back-gate voltage V_{bg} on the ambipolar $I_{\text{ds}}-V_{\text{gs}}$. The ambipolar curve is shifted toward more negative voltages for increasing V_{bg} . The n-branch swing for $V_{\text{bg}}=5\text{V}$ is improved compared with the other cases. This is attributed to partial suppression of the holes conductance at low V_{gs} .

Temperature effects on the electrical characteristic

The $I_{\text{ds}}-V_{\text{gs}}$ dependence with T is mainly attributed to the I_{th} , however T also influences the I_{tunnel} since hotter carriers pass through a narrower Schottky barrier, leading to an increasing current level [6]. The I_{OFF} current is increasing exponentially with temperature and, as suggested by equation (3), its main contribution is a thermionic emission component. A different behavior has been observed for the I_{ON} current. Increasing the temperature makes the I_{ON} current to decrease until the temperature reaches 55°C and then it rise exponentially with linear increase of T . At lower temperatures tunneling and trap-assisted tunneling are more important than thermionic emission. Rising T up to 70°C makes the charges trapped into the gate oxide to un-trap, reducing the I_{tunnel} component. A different behavior is observed for the I_{ON} currents for 70°C $\leq T \leq$ 115°C. In this range, the I_{ON} exponentially increases with T . This effect is evidence of two main current components, for which the I_{ON} changes from a tunneling to a thermionic emission dominated regime.

A set of $I_{\text{ds}}-V_{\text{gs}}$ curves (Figure 3) taken at different temperatures at constant $V_{\text{ds}} = 100$ mV and $V_{\text{bg}} = 5$ V are used to extrapolate the Arrhenius plot shown in Figure 5. The constant $V_{\text{bg}} = 5$ V is used to set the device operation more favorable for electron conductance at low V_{gs} . Constant subthreshold swings ≈ 110 mV/dec are observed independently from the temperature (see Figure 4). Low negative V_{gs} voltages ranging from -1 V to 0 V show an almost linear slope with inverse of temperature and can be correlated to a thermionic-emission regime. However, for this V_{gs} range the current level is on the order of fAs, which is comparable to the background noise, and it cannot be used to extrapolate the Schottky barrier height. Another distinct regime is observed for $-0.3\text{V} \leq V_{\text{gs}} \leq -0.5\text{V}$, for which the slopes are greatly affected by tunneling. This regime shows a dominant tunneling component for the two lowest temperatures. Finally, an exponential dependence with T is observed again for $V_{\text{gs}} \geq 0$ V with the exception of the lower temperature. All these regimes demonstrate that the current in our device is mainly thermionic for $T \geq 70^\circ\text{C}$ and that the tunneling contribution is trap assisted.

The slopes from the Arrhenius plot are then used to extract the effective Schottky barrier height ϕ_{Beff} with the activation energy E_a method. As shown in inset A of Figure 6, an average effective barrier height $E_a \approx 450 \pm 5$ meV is found over a large range of $V_{\text{gs}} \geq 0.2$ V. However, these values cannot be taken as Schottky barrier height since in this regime the device has both tunneling and thermionic components. As suggested by Svensson et al. [7], a better evaluation of the Schottky barrier height can be taken at the maximum of E_a for low current levels. As shown in the inset B of Figure 6, this maximum corresponds to $V_{\text{gs}} = -0.45$ V and gives a $\phi_{\text{Beff}} = 525$ meV, confirming the mid-gap Schottky barrier height.

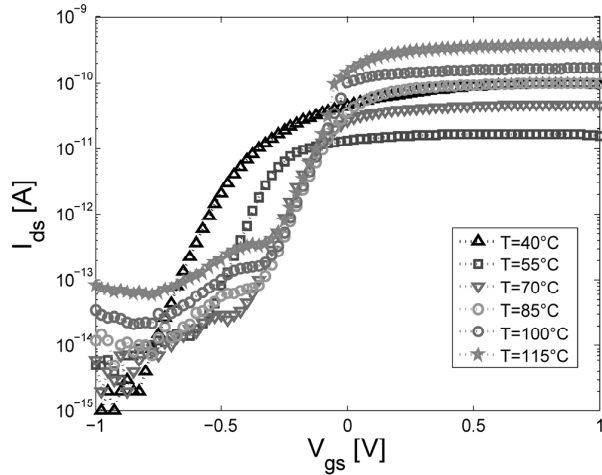


Figure 3: Effect of the temperature on the ambipolar $I_{ds} - V_{gs}$ at $V_{ds} = 100\text{mV}$.

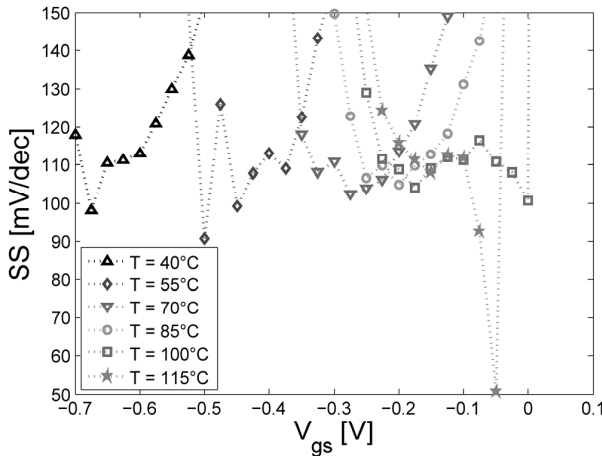


Figure 4: Subthreshold swings associated with the $I_{ds} - V_{gs}$ plots from Figure 3. Very low swing minima are measured at 100°C and 115°C close to threshold voltages. Notice the voltage shift with temperature increase and the extremely low minima of 50mV/dec for the highest temperature.

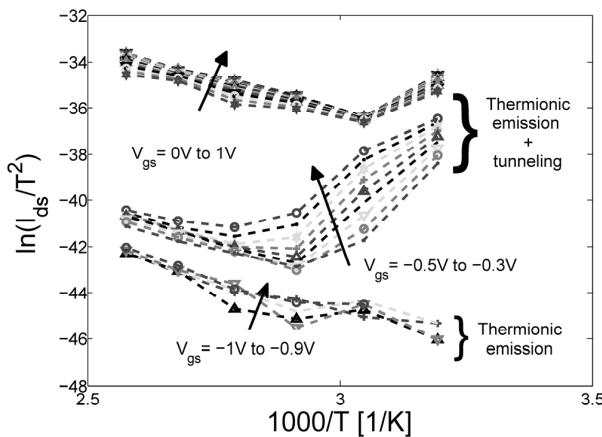


Figure 5: Arrhenius plot for different V_{gs} extracted from the plots of Figure 3 showing both thermionic emission and tunneling mechanisms. The linear decreasing slopes are associated with thermionic emission regimes.

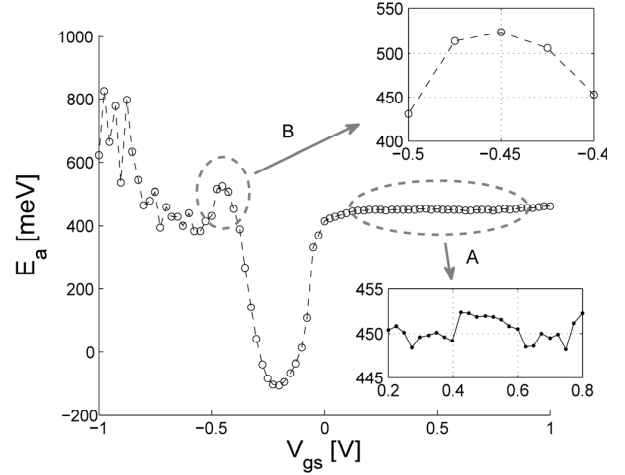


Figure 6: Extracted E_a over a large range of V_{gs} . The inset A shows a constant $E_a = 450 \pm 5\text{meV}$ over $-0.2\text{V} \leq V_{gs} \leq -0.8\text{V}$. Inset B shows the maximum of $E_a = 525\text{meV}$ which is associated to the ϕ_{Beff} .

6. SILICON NANOWIRE SCHOTTKY BARRIER FET FOR SENSING

pA current sensing

Current biasing the devices with a constant I_{ds} current makes the device to behave as a pseudo-inverter configuration with hysteretic transfer function. Thanks to the ambipolarity, the $V_{\text{out}} - V_{\text{in}}$ curves shift linearly with the applied current bias. For instance in Figure 7, low pA current levels can be either read from the high-to-low or the low-to-high transition voltage with sensitivities of 17mV/pA . A similar biasing scheme for polysilicon nanowires has been previously characterized by the authors show a similar trend. In Figure 8, forward and reverse threshold voltages for currents between 100fA and 500fA show a linear increase with current (adapted from [8]).

Temperature sensing

Another application is temperature sensing. Upon application of increasing temperature of operation, the hysteresis window observed in pseudo-inverter biasing scheme shrinks.

The crystalline Si nanowire Schottky barrier FET shows different sensitivities at different temperature regimes, depending on which mechanism dominates the conductance. Since the hysteresis is attributed to the storage of charges in either gate oxide and/or at the Schottky barrier junctions [9], an increased hysteresis window is expected for the lowest temperatures. The highest sensitivity of $40\text{mV}/^\circ\text{C}$ is found in the T range around 40°C at which the trap tunneling mechanisms dominates. For temperatures higher than 55°C the sensitivity tends to saturate according to the dominance of thermionic current contribution, leading to lower sensitivity of $10\text{mV}/^\circ\text{C}$. In Figure 9 the hysteresis window shrink for increasing T when $70^\circ\text{C} \leq T \leq 100^\circ\text{C}$ is shown.

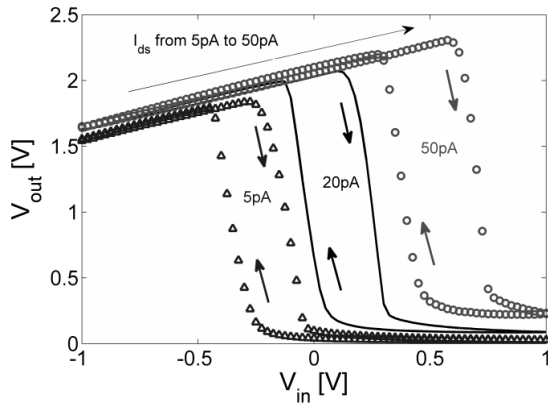


Figure 7: Measured input-output transfer characteristics of a hysteretic inverter based on a single Si nanowire FET with low current bias, showing current-dependent thresholds.

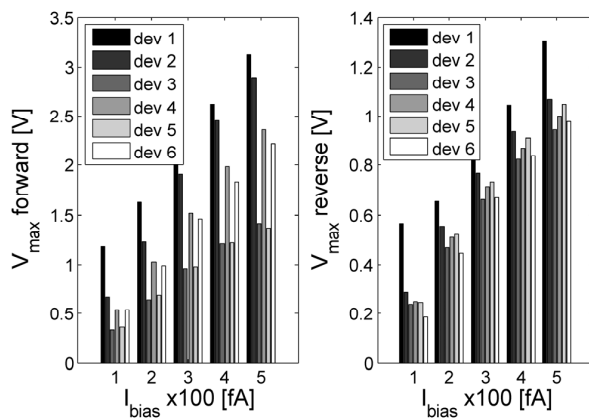


Figure 8: Forward and reverse threshold voltages for polysilicon Schottky barrier FETs under constant current biasing from 100 fA up to 500 fA (adapted from ref. [8]).

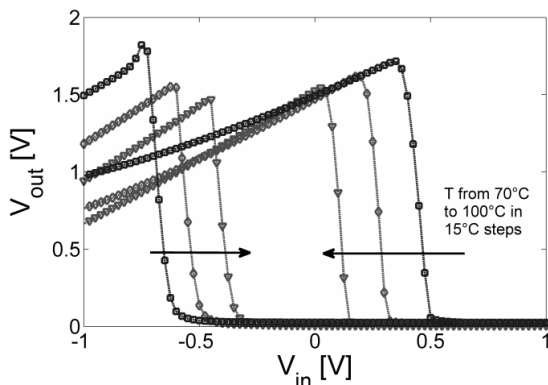


Figure 9: The hysteresis window shrinks with increasing temperature. Within this T range, the temperature sensitivity of 10 mV/°C is related with the thermionic current regime.

7. CONCLUSIONS

The Schottky barrier Si nanowire FET has been demonstrated suitable for precise current and temperature sensing. Sensitivities ranging in between 17 mV/pA and 40 mV/pA for current sensing and in between 10 mV/°C and 40 mV/°C for temperature sensing associated with the different current conductance

mechanisms are reported. The compatibility of Si nanowires for both sensing and logic applications makes these structures suitable for heterogeneous integration within the same fabrication platform scheme.

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