High-efficiency silicon heterojunction solar cells:
From physics to production lines

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Abstract

Silicon heterojunction technology (Si-HJT) consists of thin amorphous silicon layers on monocrystalline silicon wafers and allows for photovoltaic solar cells with energy-conversion efficiencies above 20 %, also at industrial-production level. This article reports how this may be achieved. First, we focus on the surface-passivation mechanism of intrinsic and doped amorphous silicon films in such solar cells, enabling record-high values for the open-circuit voltage. Next, the industrial upscaling in large-area reactors of such film deposition is discussed, including the fabrication of solar cells with energy-conversion efficiencies as high as 21%.

1. Introduction

Semiconducting hetero structures are attractive to use for electronic junction formation in crystalline silicon (*c*-Si) wafer-based solar cells. The key point of these structures is the displacement of highly recombination-active (ohmic) contacts from the crystalline surface by insertion of a film with wide bandgap. To reach the full device potential, the hetero-interface state density should be minimal. Practically, hydrogenated amorphous silicon (*a*-Si:H) films of only a few nanometer thin are appealing candidates for this: their bandgap is wider than that of *c*-Si and, when intrinsic, such films can reduce the *c*-Si surface state density by hydrogenation. In addition, these films can be doped relatively easily, either *n*- or *p*-type, allowing for the (lithography-free) fabrication of contacts with record-low values for the saturation-current density. Impressive large-area (> 100 cm^2) energy-conversion efficiencies (~23%) have been reported by Sanyo, Japan for such devices [1].

A sketch of a complete heterojunction solar cell is given in figure 1. The basic device features on the front (illumination) side successively an intrinsic *a*-Si:H passivation layer and a *p*-doped amorphous silicon emitter both deposited by plasma enhanced chemical vapor deposition (PECVD). On top of the silicon layers,

an antireflective transparent conductive oxide (TCO) is deposited by physical vapor deposition (PVD) and the charge collection is made by a screen-printed metallic contacting grid. On the back side, the stack is realized of an intrinsic *a*-Si:H passivation layer, a back-surface field (BSF) layer made of *n*-type amorphous silicon both deposited by PECVD, a TCO layer and a metallic contacting layer.

In this article, we briefly review the passivation properties of such films and discuss upscaling of deposition technology to an industrial level.

2. Intrinsic and doped *a*-Si:H film passivation

For any high-efficiency solar cell, surface passivation is of extreme importance. The *c*-Si solar cells with the highest energy-conversion efficiency reported to date featured thermally grown silicon-oxides passivation films for this. Efficient silicon-based light-emission was found with similar technology [3]. Films of *a*-Si:H have attracted considerable attention as well for surface passivation [4], and have proved to be on par with the
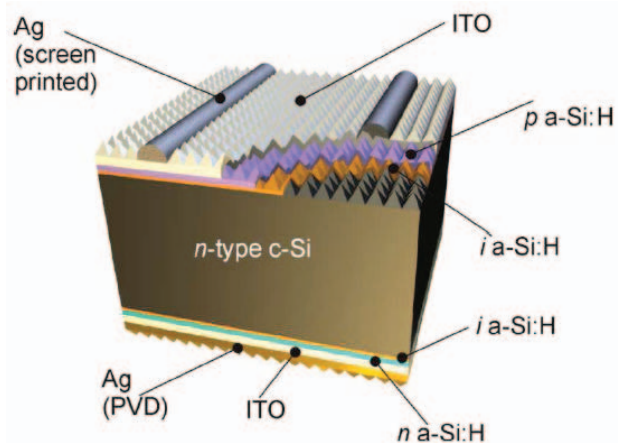

Figure 1. Structure of a silicon heterojunction (Si-HJT) solar cells made from *n*-type monocrystalline silicon substrate. Figure taken from [2].

best dielectric films. For intrinsic films, a necessary condition for good passivation is that the interface is atomically sharp for flat [5], but also for textured substrates [6].

Usually, carrier recombination via defects is assumed to happen via a Shockley-Read-Hall two-charge state level. However, the defect state responsible for interface recombination is much more likely the silicon dangling bond. At equilibrium, according to the position of the Fermi level, this defect is either in a neutral, positively, or negatively charged state, accommodating respectively 1, 0, and 2 electrons. Based on this amphoteric behavior (and introducing certain simplifications allowing for closed-form recombination rates [7]) a new interface recombination model has been introduced and experimentally verified for a-Si:H / c-Si structures [8].

Post-deposition annealing offers in a straightforward way a single parameter to vary both electronic and material properties of the samples under study, which may be exploited to gain physical insight. At low temperatures, this has proved to be quite beneficial for the electronic interface passivation quality of such interfaces [5]. As an example, figure 2 shows how the value for the effective carrier lifetime, τ_{eff} changes over time when bifacially a-Si:H passivated c-Si wafers are subjected to isothermal annealing. It can be seen that irrespective of the film deposition temperature, T_{depo}, the
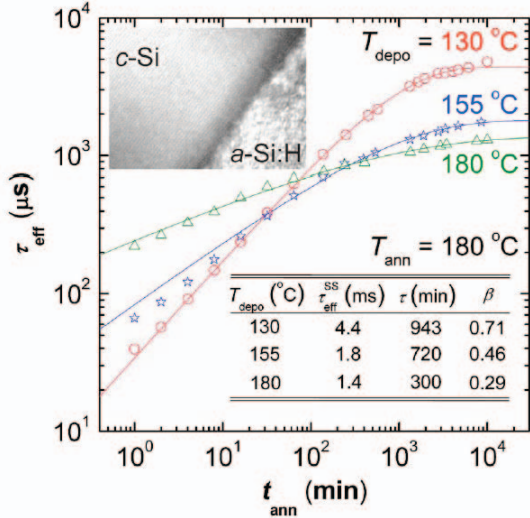

Figure 2. Measured values for τ_{eff} as function of t_{ann} for a ~3.0 Ω.cm FZ wafer bifacially passivated by ~50 nm a-SiH(i) films. The cases for three different deposition temperatures are shown. Evaluation was performed at $\Delta n = \Delta p = 1.0 \times 10^{15}$ cm^{-3}. The annealing temperature was fixed at 180 °C. Symbols represent measured data. Solid lines represent stretched-exponential fits to the data. Values for the fitting parameters are given in the inset table. The inset HR-TEM micrograph is taken from one of the interfaces of a mirror-polished c-Si(100) sample featuring a-Si:H films for which $T_{depo} = 200$ ºC. Data taken from [9].

shown data can be fitted with satisfying accuracy to stretched exponentials of the form

$$\tau_{eff}\left(t_{ann}\right) = \tau_{eff}^{SS}\left[1 - \exp\left[-\left(\frac{t_{ann}}{\tau}\right)^{\beta}\right]\right], \qquad (1)$$

where β is the dispersion parameter ($0<\beta<1$), and τ effective time constant, respectively [9]. For bulk a-Si:H material, defect reduction following a similar law has been explained as arising either from dispersive (i.e. time dependent) hydrogen diffusion [10], or from retrapping included hydrogen motion [11]. For the a-Si:H(i) / c-Si interface, based on the latter interpretation, it can be argued that the annealing induced passivation originates from a transfer of hydrogen from a higher hydride state in the a-Si:H film (close to the interface) to a monohydride c-Si surface state [9]. Consequently, the a-Si:H(i)/c-Si interface passivation needs to be attributed to chemical surface state passivation, rather than a field effect [9].

To fabricate hetero-junction devices, doped films are required, either for emitter or for back surface field formation. However, although such films may yield a field effect at the interface, their electronic passivation properties are often found to be inferior, compared to those of their intrinsic counterparts. This is shown in figure 3: Panel (a) gives the change in surface passivation quality, expressed by τ_{eff}, as a function of an isochronal stepwise annealing treatment for respectively a few nm thin intrinsic, n^+-, and p^+-doped single film a-Si:H / c-Si hetero-structures. Whereas annealing up to 260°C has a beneficial effect on the surface passivation properties of a-Si:H(i) films, the same treatment is seen to result immediately in losses for the a-Si:H(p^+) case [12]. For a-Si:H(n^+) films, initially an improvement in passivation quality can be seen. Nevertheless, annealing above 220°C results also here in losses. Panel (b) of the same figure shows how the optical bandgap, extracted from spectroscopic ellipsometry measurements, of these films changes during the annealing treatment. Interestingly, for all three cases, the onset of passivation degradation (if present) seems to coincide with a collapse of the optical bandgap. This may point at defect generation in the amorphous host matrix, and was also confirmed by thermal desorption spectroscopy measurements [13]. The latter phenomenon is attributed to the position of E_F within the bandgap, influencing the generation of (native) compensation defects in the semiconductor, counteracting intentional doping.

Fundamentally, as the bandgap of a semiconductor increases, often it becomes increasingly difficult to dope it in a symmetric way (both n- and p-type). This may originate from the generation of compensation defects, depending on E_F, according to the relation:
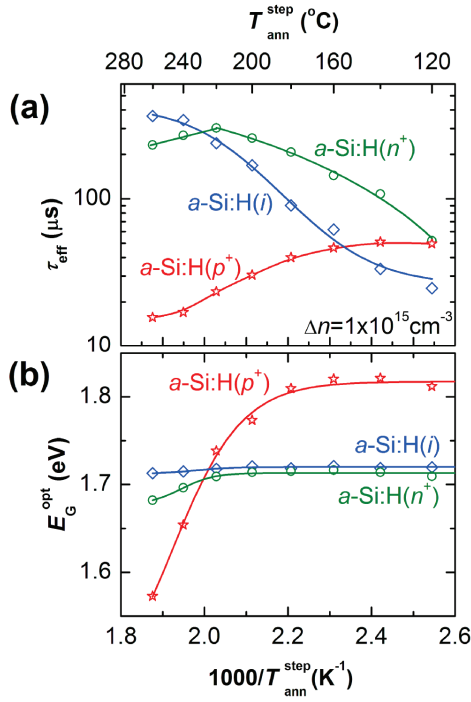
Figure 3. (a) Influence of stepwise annealing on a few nm thin single film a-Si:H / c-Si interface passivation quality, expressed by τ_{eff} (at $\Delta n = \Delta p = 1.0 \times 10^{15} \text{cm}^{-3}$). No intrinsic buffer layers are present underneath the doped films. (b) Influence of stepwise annealing treatment on the optical bandgap $E_{\text{G}}^{\text{opt}}$ for similar films as in (a), extracted from spectroscopic ellipsometry measurements. Symbols represent experimental data, the lines are guides for the eye. Data taken from [12].

$$\Delta H^{(D,q)}\left(\mu, E_F\right) = q E_F + n_D\left(\mu_D - \mu_S\right) + \Delta E_b, \quad (2)$$

describing the formation enthalpy of dopant D of charge state q in host semiconductor S [14]. Here, μ_D and μ_S are the chemical potentials of the dopants and host, $\Delta E_b = E$(host+defect) – E(host), and E is the total energy. Deliberate p-type (n-type) doping of the material by acceptors (donors) will shift E_F towards the valence band maximum (conduction band minimum) and decrease the formation energy of native donors (acceptors) to a point where they are created spontanously. Usually, E_F can not be pushed beyond this point (it will be pinned) due to the occuring electronic compensation. Consequently, in a-Si:H, the described E_F dependent defect generation may actually originate from its bandgap width as well. Here, the defect most likely formed by either type of doping is the amphoteric Si dangling bond, through Si-H rupture. For the surface passivation, creation of such defects will have two effects: In the bulk of the a-Si:H films, each additional defect will compensate an intentional dopant, leading to reduced effective doping and thus field effect. At the interface, such defects will lead to a reduced chemical interface state passivation.

It must be concluded that to simultaneously fulfill both the surface-passivation and the doping requirements is challenging. For this reason, typically, a few-nanometer thin intrinsic buffer layer is inserted between the c-Si surface and the doped a-Si:H films for device fabrication. Even in such a case, a careful assessment of thermal treatments of the devices is mandatory to warrant high performance.

3. Deposition-technology upscaling

For successful mass production of Si-HJT cells, PECVD and PVD large-area deposition reactors have to fulfill several criteria. The two most important are [2]:

- A very good uniformity, to achieve a narrow distribution in final cell performances.

- A very well-controlled discharge to guarantee inter-run reproducibility and a thickness control at the sub-nanometer level, since the layers are extremely thin (nanometer range).

For this purpose, a dedicated new generation large-area capacitively-coupled parallel-plate PECVD reactor has been designed and developed by Roth & Rau, the so-called S-$Cube$ reactor. A thickness uniformity below 5 % can be achieved over a $400 \times 400 \text{ mm}^2$ area [2]. Surface passivation is tested on polished n-type <100> FZ substrates (2-3 Ω.cm) after native oxide removal, with very thin (< 8nm) intrinsic a-Si:H films deposited on both wafer surfaces. In these reactors, carrier lifetimes as high as 9.6 ms are reached before any hot-plate annealing for such very thin films (Figure 4). Neglecting the bulk lifetime ($\tau_{\text{bulk}}=\infty$) for this material, surface recombination velocities as low as 2 cm.s^{-1} are
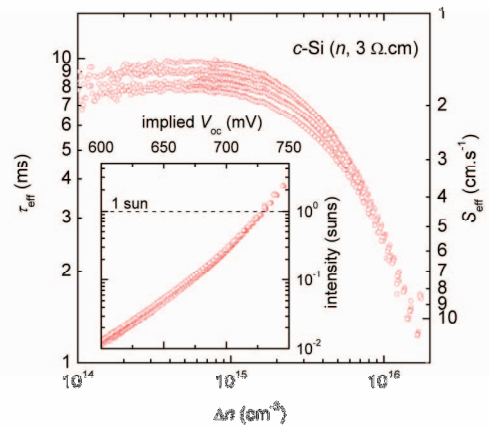

Figure 4. Lifetime measurements after co-deposition of 7 nm a-Si:H(i) on 5 FZ wafers. The inset shows the implied V_{oc}.

obtained in a wide carrier injection range. These results are on par with the best dielectric passivation films, and correspond to an implied V_{oc} of 730 mV at 1-sun, a very high value indeed. This is shown in the inset of figure 4. Both n- and p-type films have been developed in these reactors too.

For the complete process, to fabricate devices as shown in figure 1, properly cleaned random-pyramid textured wafers have been used. The PECVD films were deposited in the described *S-Cube* reactors. Indium tin oxide (ITO) has been used as TCO both at front and back side, and was deposited in a Roth & Rau magnetron sputtering system using a planar ITO ceramic target by pulsed direct current (DC) discharge. The front contact grid was fabricated by screenprinting of a low-temperature silver-based paste [2].

With this sequence, complete solar cells have been fabricated on FZ wafers, with aperture areas of 2×2 cm^2. The best device to date has an efficiency of 21.0 %, with a V_{oc} of 729 mV, a J_{sc} of 37.0 mA.cm^{-2} and a fill factor of 77.9 %, as summarized in figure 5. Note that these results include a loss due to illumination shadowing because of the front contact screen printed grid.

4.   Conclusions and outlook

In this article, the emerging technology of silicon heterojunction solar cells was discussed. First we explained how the record-high values for the V_{oc} are linked to the surface passivation properties of extremely thin amorphous silicon layers. Next, a new generation large-area plasma-enhanced chemical vapor deposition reactor was introduced for deposition of such amorphous silicon layers. It was shown that this new parallel-plate reactor is able to produce silicon films with uniformity
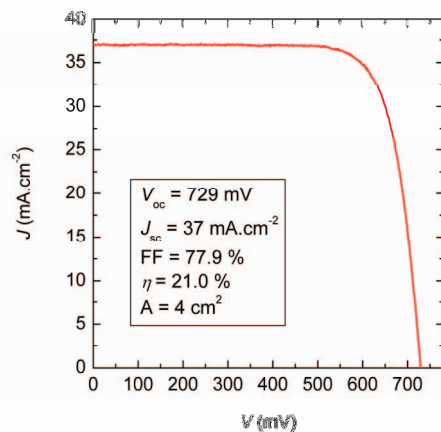
less than 5 %, both for intrinsic and doped layers. Moreover, the quality of the silicon surface passivation by intrinsic layers is comparable with the best reported results in the literature with carrier lifetimes as high as 9.6 ms on n–type polished substrate. These films were incorporated in 2×2 cm^2 aperture area solar cells, with as best result to date a device with a conversion efficiency of 21.0 % on textured n-type FZ Si substrates.

These results show that the Si-HJT technology holds indeed great promise to produce high-efficiency solar cells on an industrial scale.

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Figure 5. Light-IV measurement under 1 sun of a 2×2 cm^2 cell showing a conversion efficiency of 21.0 %. Note that the V_{oc} is similar to the implied V_{oc} at 1 sun shown in figure 4.