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Optimization of the wire grid size for differential routing: Analysis and impact on the power-delay-area tradeoff

Massimo Alioto [a,*], Stéphane Badel [1,b], Yusuf Leblebici [b,1]

[a] Department of Information Engineering, University of Siena, Italy
[b] Microelectronic Systems Laboratory, Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland

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ABSTRACT

In this paper, the impact of the wire grid size on the power-delay-area tradeoff of VLSI digital circuits with differential routing is analyzed. To this aim, the differential MOS current-mode logic (MCML) is adopted as reference logic style, and a complete differential design flow is used. Analysis shows that the choice of the grid size in differential routing has a much stronger impact on the power-delay-area tradeoff, compared to the usual single-ended case. Hence, the grid size is an important knob that must be carefully selected when differential routing is adopted. The dependence of power, delay and area on the grid size is discussed in detail through simple models, and introducing appropriate metrics. To validate the analysis and show basic dependencies in practical circuits, 30 benchmark circuits with an in-house designed MCML cell library were synthesized and routed in 0.18 μm CMOS technology. Results show that non-optimal choice of the grid size can determine a dramatic increase in power ($1.7\times$) and area ($1.3\times$). Interestingly, the grid size that optimizes the power-delay-area tradeoff is almost independent of the specific circuit under design; hence a generally optimum grid size exists that optimizes a very wide range of different circuits.

1. Introduction

Interconnects heavily influence the power-delay-area tradeoff in deep-submicron VLSI digital circuits, due to the strong contribution of their parasitics. The impact of interconnects is usually managed with automated CAD tools that perform interconnect-aware physical synthesis and place and route [1,2]. Such automated design flows are usually available for single-ended logic styles, whereas differential logic styles are not explicitly supported [3,4]. Accordingly, the adoption of differential logic styles requires further work to properly adapt commercial tools.

Until now, differential logic styles such as MOS current-mode logic (MCML) have been widely recognized to provide considerable advantages in terms of power supply noise compared to conventional CMOS logic [5]. From an application point of view, the reduced supply noise in MCML circuits enables a number of applications, such as digital signal processing or error correction in high-accuracy mixed-signal circuits, where substrate noise reduction is key to improving the dynamic range of noise-sensitive analog circuits. As another example, the low supply noise feature is very useful also in cryptographic devices with high level of security, since it makes differential power analysis (DPA) attacks much harder, thereby considerably increasing the level of protection of the secret key [6]. In these applications, the advantage offered by the MCML logic style over standard CMOS circuits has been experimentally demonstrated to be in the order of 2–3 orders of magnitude at least, although this comes at the cost of a power and area penalty [5,6]. In addition, to make MCML a practical option for commercial chips, the design effort has to be kept close to that of standard CMOS circuits, hence manual design of MCML digital blocks is not a viable approach. Accordingly, the use of standard-cell based automated design methodologies for MCML circuits is mandatory.

In differential logic styles such as MCML, each signal is carried by a pair of wires that switch in opposite directions, thus canceling out the power supply and substrate noise to a large extent [5–13]. The maximum benefits are obtained when each differential signal pair is routed as a bundle (usually named "fully differential pair"), in which the two complementary wires have exactly the same length [3–7,11]. Until now, a few methodologies have been developed to allow the implementation of fully differential logic circuits with standard CAD tools [3–7]. In the first step, these methodologies rely on a fictitious single-ended representation of differential signals, in order to allow for using commercial CAD tools. Then, in a post-processing step, the

* Corresponding author. Current adress: Berkeley Wireless Research Center, University of California, Berkeley, USA.
E-mail addresses: malioto@dii.unisi.it, alioto@eecs.berkeley.edu (M. Alioto), stephane.badel@epfl.ch (S. Badel), yusuf.leblebici@epfl.ch (Y. Leblebici).
[1] Tel. +41 21 693 69 22; fax: +41 21 693 69 59.

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fictitious single-ended cells and wires are turned into the fully differential and logically equivalent counterparts. In such methodologies, it was shown that timing integrity throughout all steps of the design flow requires a fully differential routing, which matches the lengths and parasitic of the two wires belonging to the same differential signal pair. In other words, the two wires belonging to the same pair must be always routed in parallel to each other, as will be discussed in detail in Section 2.

As is well known, automated routing of VLSI circuits is efficiently performed by restricting the possible decisions that the tool can make. In particular, the tool is allowed to place and route wires only at discrete positions in the die, according to a routing grid [8,9]. In single-ended design flows, the wire grid pitch (i.e., the grid step) is often set to the minimum value allowed by the technology in order to provide maximum integration density. Nevertheless, non-minimum wire grid pitch can bring limited benefits (in the order of 10%) in terms of speed and power consumption [10], since coupling capacitances between adjacent wires are reduced when their distance is increased. Moreover, current routing tools are able to automatically spread neighboring wires apart when routing space is available. Therefore, the choice of the wire grid pitch is not critical in the case of single-ended routing, and can bring only a modest improvement compared to the case of minimum pitch.

As opposite to single-ended design flows, the impact of wire grid pitch in differential design flows is expected to be strong, since wires belonging to the same differential pair are forced to be close to each other by necessity, and tools are not able to freely adjust their spacing. In addition, wires within the same pair always experience opposite transitions, hence their effective coupling capacitance is always increased by a factor of two due to the Miller effect [2,11–13]. For these reasons, the choice of the wire grid pitch is expected to be a critical design variable in differential design flows, and further investigation is needed.

In this paper, the impact of the wire grid size in fully differential design flows is analyzed. In particular, the impact of the wire grid pitch on the power-delay-area tradeoff is analyzed in detail through simple models and design considerations, adopting a differential MOS current mode logic standard cell library and a previously developed fully differential design flow. Simple design metrics to optimize the grid pitch are also introduced. According to the above premises, our analysis is focused on local wires that connect standard cells within the same module, hence effects typically associated with global wires (e.g., wire inductance) will not be considered.[2] Analysis of 30 benchmark circuits in 0.18-μm technology is performed to validate the above considerations. Results show that the proper choice of the wire grid pitch in differential design flows significantly reduces power and area for a given delay constraint. Interestingly, the optimum wire grid pitch was found to be almost independent of the specific circuit under design, hence pitch optimization can be performed only once and used for a large number of different designs.

The paper is structured as follows. In Section 2, a complete fully differential design flow is introduced. Qualitative considerations on the impact of the wire grid pitch and comparison between differential and single-ended routing are reported in Section 3, whereas a design metric is derived in Section 4. Validation and simulation results are discussed in Section 5, and conclusions are discussed in Section 6.

[2] Observe that issues related to global interconnects are completely different from local (intra-module) interconnects both in terms of the impact of wire parasitics and design issues. Indeed, local interconnects are mainly capacitive and easily prone to routing congestion, whereas global wires exhibit also resistive/inductive behavior and typically do not suffer from serious congestion [20].

2. Review of a fully differential automated design flow

In order to implement circuits based on differential logic styles, the two wires belonging to the same differential pair must be routed as a bundle [3–7], i.e. they must be routed in parallel to ensure that they have the same length and parasitics. This fully differential routing approach has obvious advantages in terms of signal integrity, which is an important aspect in nanometer technologies, especially in the case of low-swing differential logic styles with reduced noise margin [4,11]. However, the main reason for using fully differential routing is related to timing analysis. Indeed, in fully differential logic styles, the switching of logic gates is triggered by the variations in the differential input voltage; hence the timing arcs should relate input and output differential voltages during the timing analysis of the circuit. Unfortunately, current commercial timing analyzers are not able to model timing of differential signals, as they support only single-ended timing relationships.

The problem is illustrated in Fig. 1, where the switching of a pair of complementary signals is represented in the case of independently routed wires, i.e. with different length and parasitics, thereby violating the premise of fully differential design flows. Because of the difference in the parasitics associated with each wire, the transitions of the driving gate have different time constants. In other words, from Fig. 1 the two complementary signals *OUT* and *OUT'* cross the 50% threshold at different points in time, and the point in time where the difference of the two signals crosses the 50% threshold is located somewhere in between (in fact, it can be easily seen that it is close to the average of the two individual points, for small differences of the two time constants). Therefore, if the input-to-output delay is evaluated as the delay at only one of the two single-ended outputs (as allowed by current CAD tools), it underestimates or overestimates the actual delay evaluated on the differential waveform. These timing errors can accumulate and lead to considerable error when evaluating a path delay. Clearly, such timing errors are not acceptable in high-speed applications, since it is likely that the speed constraint will not be actually met. Analogously, such errors are not acceptable in low-power applications, since the delay overestimation clearly leads to a circuit overdesign, thereby degrading the power efficiency.

According to the above considerations, commercial CAD tools can accurately estimate the delay of differential logic gates only if the two outputs of a differential pair have exactly the same delay. This can be achieved by balancing the parasitics of the two wires

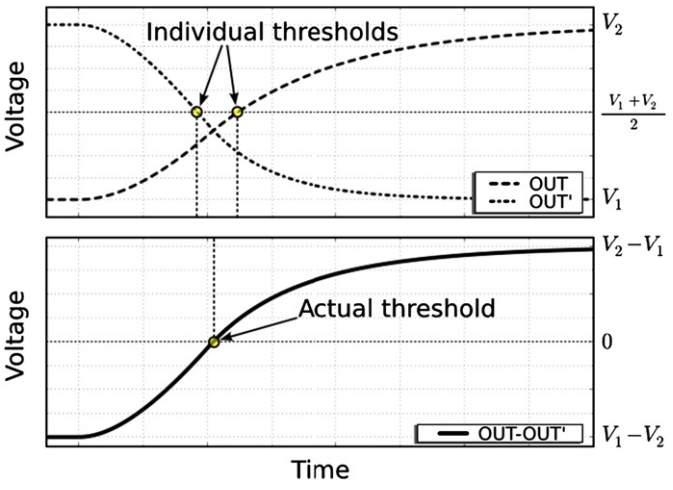

Fig. 1. 50% crossing points for two wires belonging to the same differential pair and the corresponding differential voltage.

within that same pair as much as possible, i.e. routing them as a bundle.

A complete fully differential design flow was recently developed, based on the above discussed concept [4]. With no loss of generality, in the following this design flow will be applied to a standard cell library based on MOS current-mode logic (MCML) style [14,15]. The design flow for differential MCML standard cells is briefly illustrated in the flowchart in Fig. 2. Essentially, two different views of the cell library are necessary: a logical view, where each pair of complementary signals (differential inputs and output of the cell) is represented as a single port, and a physical view which includes both polarities for each signal. Once the cell layouts are created, they are characterized for timing and power. Logical and physical models are generated for simulation, synthesis (timing library) and placement and routing (abstracts). Then, a number of variants are generated for each cell by inverting the inputs and output in all possible combinations, to take advantage of the free signal inversion available with differential cells (in differential cells, logic inversion is performed by simply swapping pins).

In the circuit automated design, wire capacitance values are properly evaluated to reflect the higher effective capacitance seen in differential wires (more details are provided in Section 3), in order to ensure accurate timing analysis throughout the flow. Based on a standard-cell logic library and a standard HDL description, circuits are then synthesized, placed and routed using standard tools. The resulting circuit is made of fictitious single-ended cells and wires, where each wire actually represents a pair

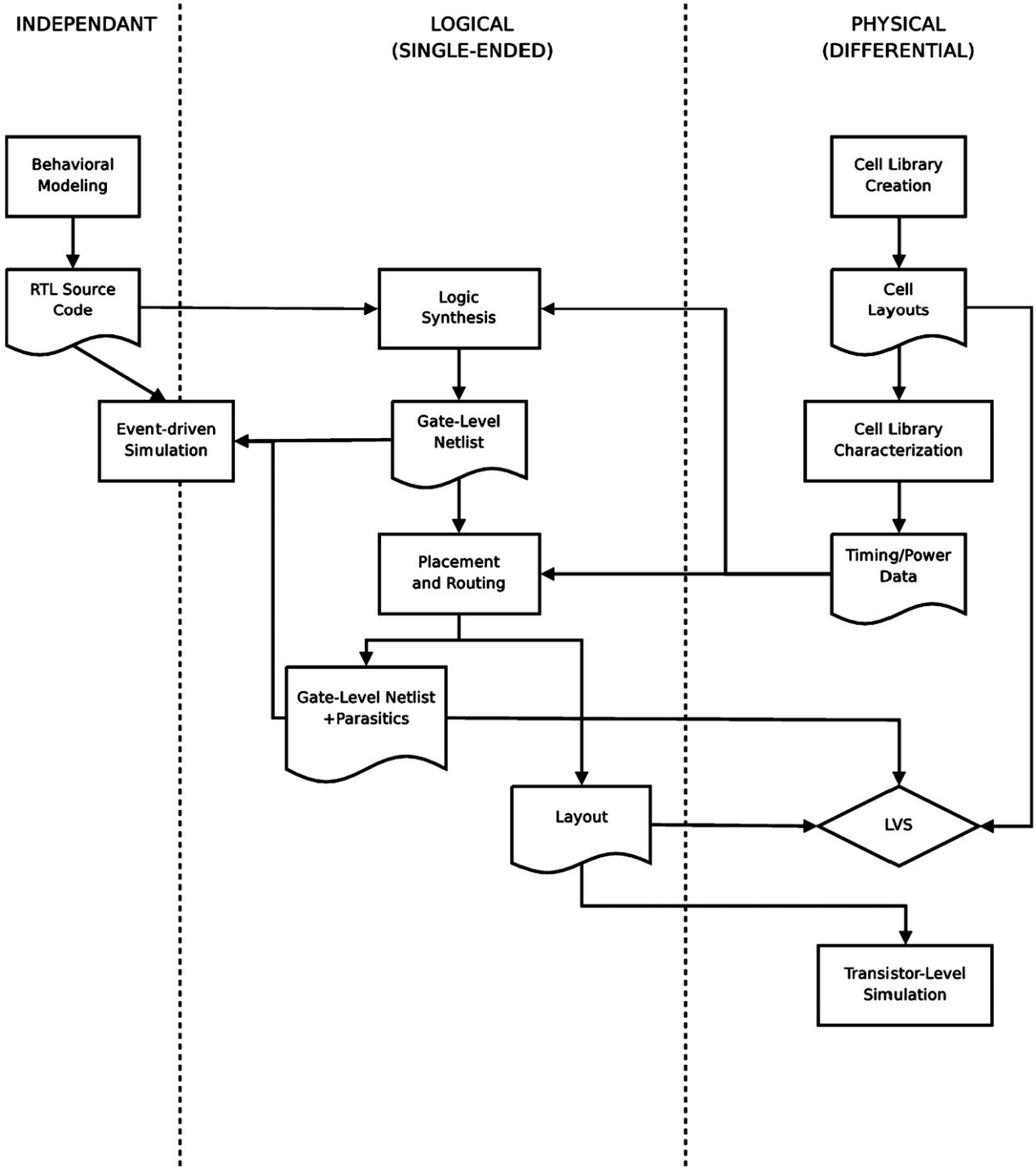

Fig. 2. Flowchart of the fully differential design flow [4].

of complementary signals, according to appropriate design rules that accommodate for the increased wire width. Then, a script translates the single-ended design into a physical equivalent differential design, by splitting each wire into a differential pair, and replacing each cell by its physical counterpart. To correctly connect each wire to the corresponding cell pins, the resulting design is fed back to the router to complete the connections.

Summarizing, thanks to the joint adoption of commercial CAD tools and appropriate scripts, the above design flow permits the automated design of differential digital circuits from their VHDL/Verilog description to their detailed physical-level design.

3. Understanding the impact of the routing grid pitch

When using a design flow that includes automated place and routing, the designer has to preliminarily choose the wire grid pitch. Unfortunately, until now no criteria or guidelines have been provided to assist this choice. For this reason, in the following the impact of wire grid pitch is analyzed in detail for fully differential routing, highlighting the interdependence of fundamental design parameters, such as speed, power consumption and area.

3.1. Analysis of the power-delay-area tradeoff versus wire grid pitch

In any type of automated routing, as shown in Fig. 3 the wire grid size is set by the pitch P, which is defined as the distance between the middle sections of the adjacent wires. In the same figure, capacitance $C_{coupling,INT}$ schematizes the intrinsic coupling capacitance between the considered wires, whereas C_{GND} represents the grounded capacitive contribution at each wire (i.e., the contribution of the bottom plate, as well as the fringing capacitance to ground of the lateral faces). For a given wire width, $C_{coupling,INT}$ and C_{GND} are proportional to the wire length L via the capacitance per unit length $c_{coupling}$ and c_{GND}, respectively (i.e., $C_{coupling,INT}=c_{coupling}L$, $C_{GND}=c_{GND}L$). Analogously, the external capacitance towards the adjacent wires $C_{coupling,EXT}$ in Fig. 3 is proportional to the overlap length L_{ov} (i.e., the length of the overlapping section of the adjacent wires) via the capacitance per unit length $c_{coupling}$ (i.e., $C_{coupling,EXT}=c_{coupling}L_{ov}$). In deep-submicron technologies, the capacitances associated with the lateral face (i.e., $C_{coupling,INT}$ and $C_{coupling,EXT}$) are well known to dominate over the grounded capacitance C_{GND}, as the lateral face area tends to down-scale slowly compared to the bottom face of wires [2].

It is useful to observe that the wires belonging to the same differential pair always experience opposite transitions, hence the in-between coupling capacitance $C_{coupling,INT}$ is always affected by the full Miller effect, i.e. it can be modeled as a grounded capacitance (in parallel to C_{GND}) equal to $2C_{coupling,INT}$ [11]. On the other hand, the full Miller effect takes place between the considered wire and the adjacent ones only if they switch at the same time, whereas no effect is observed if they switch in different points of time. Hence, the capacitive contribution between each wire of the differential pair and the adjacent one can be schematized as a grounded capacitance equal to $\alpha_{Miller}C_{coupling,EXT}$, being α_{Miller} the well-known Miller effect coefficient that results to 2 if full Miller effect takes place, and is lower than 2 if this effect occurs only partially [2]. Accordingly, the overall capacitance C_{wire} to ground associated with each wire of a differential pair is proportional to L via the wire capacitance per unit length c_{wire}, according to

$$C_{wire}=C_{GND}+C_{coupling,INT}+C_{coupling,EXT}=c_{wire}L \tag{1a}$$

$$c_{wire}=c_{GND}+2c_{coupling}+c_{coupling}\frac{L_{ov}}{L}\alpha_{Miller} \tag{1b}$$

Relationships (1a) and (1b) can be used to understand the impact of the wire grid pitch P on the wire capacitance, which is related to performance and power, and area. If the grid size P is small (i.e., close to its lower bound P_{min} set by the technology), $c_{coupling}$ and hence c_{wire} tend to be very high due to the short distance between adjacent wires, thereby degrading speed and power efficiency. At the same time, under low values of P, the maximum possible integration density is obtained. When P is increased with respect to P_{min}, capacitance $c_{coupling}$ tends to decrease. As an example, this is shown by the plot of $c_{coupling}$ versus P/P_{min} in Fig. 4, where the contribution capacitive contributions of intermediate-level (metal 2–4) layers in 0.18-μm CMOS technology is considered. This is easily explained by considering that an increase in P tends to spread the lateral faces of two adjacent wires apart, thereby reducing the capacitance associated with the parallel plates of the capacitor $C_{coupling,INT}$. At the same time, the small increase in P does not significantly affect the routing density, as long as no congestion occurs in routed wires, hence the wire length L is roughly unaffected[3] by P. Accordingly, from (1a) and (1b) the net effect of a moderate increase in P is a reduction in C_{wire}, which in turn improves both speed and power efficiency.

On the other hand, if P is strongly increased with respect to P_{min}, the distance between differential wires becomes so high that the routing density is severely degraded and routing congestion occurs. Due to congestion, wires follow longer paths than necessary, hence their length L tends to rapidly increase when increasing P. Hence, despite of the small reduction in c_{wire} (since $c_{coupling}\propto 1/P$ slowly reduces for high values of P), the fast increase in L determines an increase of C_{wire}, according to (1a) and (1b). This effect is further emphasized for high values of P, as the increase in C_{wire} forces the synthesis tool to increase the cell strength for a targeted speed, which in turn further increases the circuit area and hence the wire length.

The above discussed dependence of C_{wire} on the pitch P is summarized in Fig. 5, from which it is apparent that there is an optimum grid size P_{opt} that minimizes C_{wire}. Observe that this optimum choice of grid size improves speed and power at the same time, and can also slightly reduce the area occupied by the circuit (as was observed in note 1). In other words, speed, power and area are not conflicting requirements in the optimum choice of the grid size P: indeed, the optimum grid size improves the routing efficiency, thereby bringing benefits to speed, power and area at the same time.

3.2. Single-ended and differential routing: qualitative considerations and differences

Until now, some results have been published on the impact of the wire pitch only in the case of single-ended routing [10,16–18]. In particular, at the best of the authors' knowledge, only [10] explicitly discusses the optimization of the wire grid pitch herein considered. More specifically, [10] shows that an optimum pitch exists, and a modest improvement in power consumption and performance can be achieved (within 10%). Moreover, the optimum pitch is shown to significantly depend on the specific circuit under design. On the other hand, papers [16–18] do not explicitly consider the wire grid pitch optimization, but they target the design of interconnect hierarchy at the process level, and propose guidelines to select geometrical dimensions of wires. Results in these papers agree well with the qualitative

[3] Actually, area may even slightly reduced by moderately increasing P. Indeed, the reduction in C_{wire} allows the synthesis tool to reduce the cell strength and hence area.

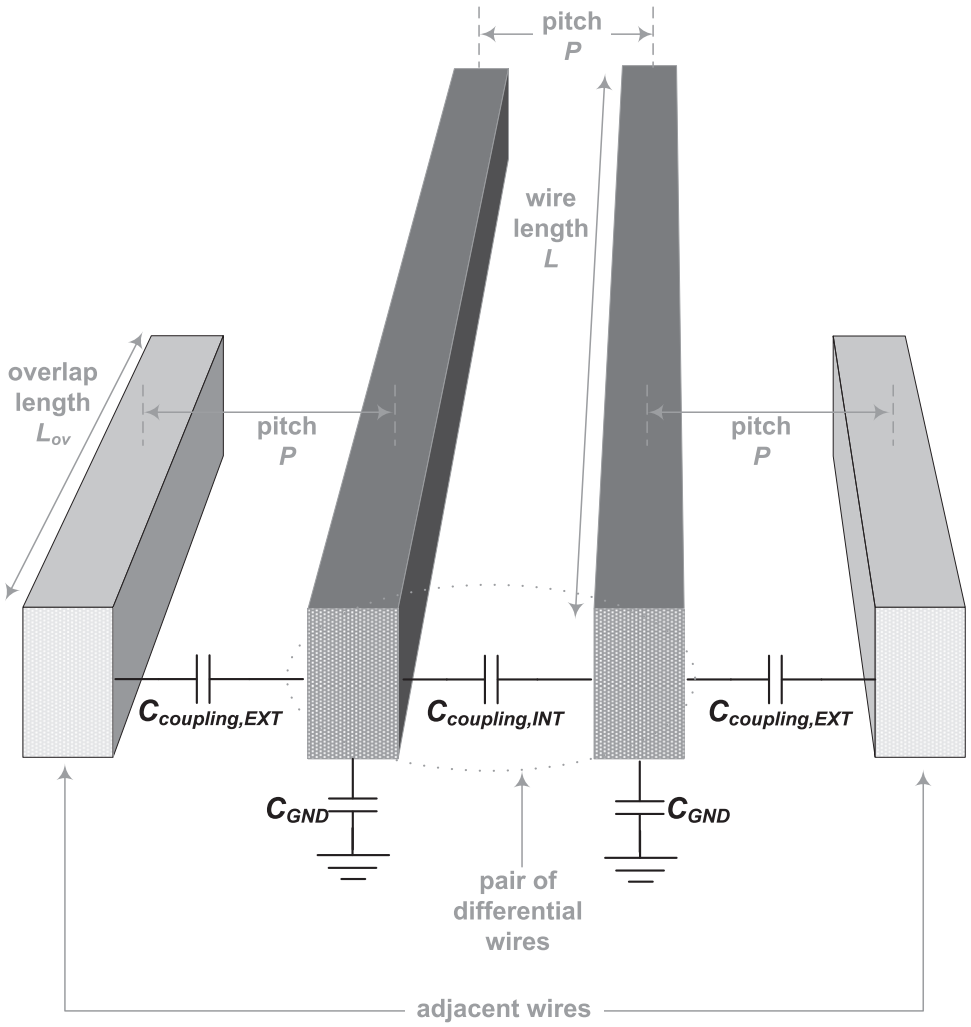

Fig. 3. Cross section of a differential pair of wires (dark grey) and two adjacent wires (light grey).

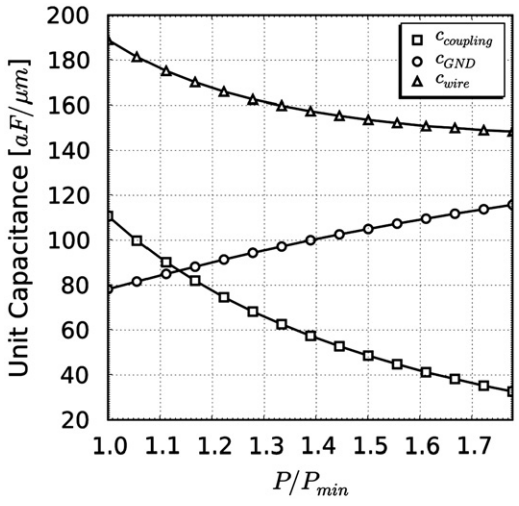

Fig. 4. Capacitance contributions per unit length as a function of the routing pitch P normalized to the minimum allowed by technology P_{min}.

considerations reported in the previous subsection, but they do not provide any information on how to size the wire grid pitch in differential routing, once the process is defined.

In general, it is expected that fully differential routing can also take advantage of the wire grid pitch optimization, although no work in the literature has been devoted to this particular case until now. To understand the differences with respect to the single-ended case, let us observe that the intrinsic coupling capacitance (i.e., the second term in (1b)) dominates over the external coupling capacitance (i.e., the third term in (1b)), since $L_{ov} \ll L$ in well-designed circuits.[4] Physically, this is because the external contribution is due only to the generally short overlap between adjacent wires belonging to different pairs, whereas the intrinsic contribution has the largest possible value (since every wire within a differential pair runs parallel to the complementary wire for its entire length). Interestingly, the intrinsic contribution is constant in the design since $c_{coupling}$ depends only on the process, whereas the external contribution depends on ratio L_{ov}/L, which clearly depends on the specific design. Since the latter contribution is negligible, it is expected that the wire capacitance per unit length in differential routing is almost design-independent; hence the wire grid pitch optimization impacts the capacitance of all wires almost in the same way, regardless of the considered design. In other words, the wire grid pitch optimization is expected to be almost unaffected by the specific

[4] Indeed, CAD tools try to avoid long wires running in parallel, hence the overlap length L_{ov} in Fig. 3 is usually kept much lower than the wire length L.

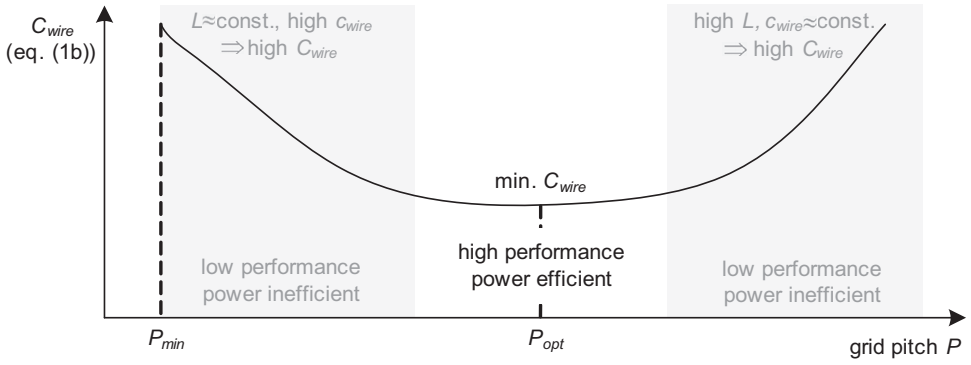

Fig. 5. Dependence of C_{wire} on the wire pitch P.

design, i.e. a design-independent optimum pitch can be found. This qualitative result will be shown to agree well with simulation results in Section 5.

From the above considerations, the intrinsic contribution in differential routing is significantly greater than that of single-ended wires, whereas the grounded contribution (i.e., c_{GND} in (1b)) is almost the same in both cases. Hence, the reduction of $c_{coupling}$ obtained with the pitch increase (see Fig. 5) has a stronger effect on c_{wire} when considering differential routing. Hence, the power/delay improvement achieved with the pitch optimization in differential routing is expected to be much greater than that of single-ended wires. This consideration will also be validated through comparison with simulations in Section 5.

Summarizing, the wire grid pitch optimization in differential circuits is expected to significantly impact the power-delay-area tradeoff, and the resulting optimum pitch is expected to be roughly design-independent, in contrast to previous results on single-ended routing.

4. Metrics to estimate the impact of grid size

As discussed in Section 3, a tradeoff between the wire capacitance C_{wire} and area exists in the choice of the wire grid pitch P. In the following, simple metrics that provide information on this tradeoff are discussed.

A reasonable metric that can express the capacitance–area tradeoff should include the product of capacitance and area, or a power of them if we want to put more weight on one of them. To achieve a general metric that permits to find the optimum wire grid pitch P_{opt} that leads to the best capacitance–area tradeoff (see Fig. 5), it is sufficient to derive a simple expression of capacitance and area that is valid for P lower than (or comparable to) the optimum pitch P_{opt}, according to Fig. 5. As was discussed in Section 3.1, in Fig. 4, for $P \le P_{opt}$ the wire length L is roughly constant, hence the dependence of C_{wire} on P in (1) is approximately due only to factor c_{wire}. In regard to area, from Fig. 3 the area occupied by a pair of differential wires is proportional to the grid pitch P and wire length L, the latter of which can be again assumed to be approximately independent of P when evaluating P_{opt}. According to these considerations, the dependence of the capacitance (area) on P is simply captured by c_{wire} (P). Hence, a suitable metric to describe the capacitance-are tradeoff is $c_{wire}^{i}P$, where exponent i is set to a value greater (lower) than unit if capacitance is more (less) important than area. In this regard, observe the wire area in the region of interest where $P \le P_{opt}$ is not a serious issue, since from Fig. 5 the wire length is independent of P, whereas reduction in c_{wire} is crucial. For this reason, more weight should be put on capacitance in the capacitance-area metric. This can be done by introducing an exponent $i=2$ in the term c_{wire}, thereby yielding the following capacitance-area figure of merit (*FOM*)

$$FOM = c_{wire}^{2}P \tag{2}$$

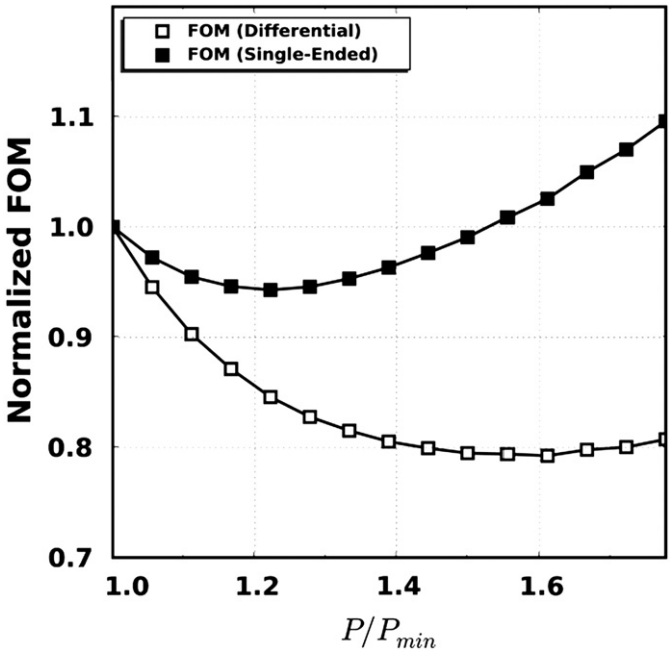

Fig. 6. Plot of *FOM* in (2) normalized to the case $P=P_{min}$ versus P/P_{min} for various values of i (differential and single-ended routing).

In (2), the dependence of the wire capacitance per unit length c_{wire} on P can be easily extracted from technology data or from simulations on 3-D field solvers [2]. For example, the dependence of c_{wire} on P is shown in Fig. 4 for the considered 0.18 μm CMOS technology, which has $P_{min}=0.72$ μm, and $c_{wire}=0.24$ fF/μm (0.19 fF/μm) for the differential (single-ended) routing under $P=P_{min}$ (this difference is due to the additional coupling capacitance contribution between the differential wire pair).

The resulting metric in (2) is plotted in Fig. 6 versus P/P_{min} for the differential and single-ended routing case. In this figure, c_{wire} and P are normalized to the values obtained for the minimum grid size P_{min} allowed by the technology. Fig. 6 reveals that the differential routing can provide significantly higher benefits from pitch optimization, compared to single-ended routing. This observation confirms that the optimization of P is crucial in differential routing, and agrees well with qualitative considerations that are reported in Section 3.2.

Inspection of Fig. 6 also shows that the figure of merit in (2) for the differential routing has a slightly flat minimum between $1.5P_{min}$ and $1.6P_{min}$, hence it is reasonable to set P to $P_{opt}=1.5P_{min}$ in circuits implemented with the considered technology. This flat minimum around P_{opt} ensures that designs around the optimum grid pitch are robust against moderate process variations. In Section 5, it will be shown that this value of P_{opt} agrees well with the optimum found experimentally in several designs.

Finally, it is interesting to compare results obtained for the differential routing with the single-ended case. From Fig. 6, *FOM* under single-ended routing is apparently less sensitive to P, i.e. the choice of the grid size in differential routing is more critical than in the single-ended case. This is due to the increased coupling capacitance associated with each differential wire pair, as discussed in Section 3.1, and agrees well with the qualitative considerations in Section 3.2. For the same reason, P_{opt} for single-ended routing is lower than that of differential case ($P_{opt}\approx 1.2P_{min}$ from Fig. 6), and is close to the minimum value allowed by technology.

5. Analysis of test circuits and validation

In order to evaluate the impact of routing grid size P on the power-delay-area tradeoff, 30 circuits (ISCAS 85 and 89) taken from the IWLS'2005 benchmark suite [19] were synthesized under different values of the grid pitch. The considered benchmarks are summarized in the first column of Tables 1–3.

Each test circuit was synthesized using Synopsys Design Compiler Topographical, which performs logic synthesis and physical optimization according to the wire technology parameters. Routing was performed using Metal-1 to Metal-4 layers. Each circuit was synthesized under several speed constraints in order to validate the results for different performance targets. To this end, each circuit was preliminarily characterized to obtain the minimum delay by performing five synthesis runs (with minimum grid size P_{min}), starting with very tight timing constraints, and updating the timing constraint for the next run with the result of the previous one. This allowed for obtaining the very minimum delay achievable in the critical path. Then, in order to evaluate the impact of the routing grid at different speed constraints, synthesis runs were then performed for a delay constraint of $1\times$, $1.25\times$, $1.5\times$, $2\times$ and $5\times$ greater than the minimum value, and with interconnect parasitic data corresponding to the various routing grid pitches adopted (ranging from P_{min} to $1.7P_{min}$). For each of these circuits and for each speed constraint, power and area were also evaluated. The resulting values of the critical path delay, area and power normalized to the case with minimum pitch are reported in Tables 1–3, which respectively refer to the case of $1\times$, $2\times$ and $5\times$ delay constraint.

To summarize the results in Tables 1–3, the average power consumption μ_{Power} (normalized to the case $P=P_{min}$) among the considered designs was evaluated to have an idea on the typical power saving obtained with pitch optimization. Analogously, the standard deviation of the power consumption σ_{Power} was evaluated to evaluate the typical spread of the power saving among different designs. Analogous parameters μ_{Area} and σ_{Area} were evaluated for area. Fig. 7a and b depicts μ_{Power} (μ_{Area}) under the $1\times$ delay constraint, as well as the typical range $\mu_{Power}\pm\sigma_{Power}$ ($\mu_{Area}\pm\sigma_{Area}$) indicated in light grey. Figs. 8a–b and 9a–b depict the same curves for a $2\times$ and $5\times$ delay constraint, respectively.

Table 1
Summary of results for $1\times$ delay constraint.

Design\pitch (μm)	Critical path length							Area							Power						
	0.72	0.80	0.88	0.96	1.04	1.12	1.20	0.72	0.80	0.88	0.96	1.04	1.12	1.20	0.72	0.80	0.88	0.96	1.04	1.12	1.20
s27	1.00	0.94	0.94	0.94	0.89	0.89	0.92	1.00	1.09	1.12	1.00	0.94	0.94	0.94	1.00	1.07	1.14	1.00	0.81	0.83	0.79
s208_1	1.00	1.12	1.02	0.93	1.07	1.02	0.98	1.00	0.85	0.95	0.82	0.92	0.84	0.87	1.00	0.80	0.94	0.79	0.90	0.78	0.82
s298	1.00	0.96	0.89	0.92	0.89	0.90	0.89	1.00	0.86	0.76	0.81	0.98	0.85	0.84	1.00	0.84	0.65	0.73	0.93	0.79	0.82
s349	1.00	0.96	0.98	1.01	0.96	1.01	1.00	1.00	0.80	0.64	0.69	0.65	0.63	0.69	1.00	0.70	0.52	0.59	0.48	0.46	0.57
s344	1.00	0.96	0.92	0.96	0.89	0.93	0.94	1.00	0.88	0.92	0.77	0.76	0.75	0.75	1.00	0.85	0.89	0.70	0.69	0.64	0.68
s386	1.00	0.99	0.97	0.95	0.93	0.95	0.99	1.00	0.87	0.76	0.65	0.70	0.58	0.66	1.00	0.90	0.70	0.56	0.61	0.50	0.59
s420_1	1.00	0.98	0.91	0.90	0.91	0.91	0.90	1.00	1.04	0.96	0.96	0.83	0.89	0.96	1.00	1.07	0.94	0.94	0.73	0.82	0.94
s713	1.00	0.95	0.86	0.83	0.84	0.85	0.89	1.00	1.10	1.33	1.07	0.95	1.06	0.90	1.00	1.11	1.40	0.99	0.86	0.97	0.82
s526n	1.00	1.01	0.99	1.00	0.96	0.96	0.98	1.00	0.96	0.75	0.73	0.69	0.88	0.87	1.00	0.93	0.65	0.60	0.56	0.81	0.83
s400	1.00	1.01	0.92	0.96	0.90	0.91	0.91	1.00	0.74	0.88	0.73	0.64	0.67	0.86	1.00	0.68	0.82	0.61	0.47	0.51	0.81
s526	1.00	0.90	0.98	0.91	0.90	0.90	0.96	1.00	0.85	0.85	0.76	0.75	0.77	0.95	1.00	0.78	0.77	0.67	0.59	0.66	0.89
s382	1.00	0.98	0.96	0.97	0.99	0.97	0.99	1.00	0.94	0.71	0.76	0.73	0.67	0.78	1.00	0.94	0.60	0.64	0.59	0.50	0.70
s444	1.00	0.94	0.95	0.92	0.93	0.92	0.95	1.00	0.65	0.74	0.71	0.77	0.66	0.71	1.00	0.53	0.65	0.56	0.66	0.54	0.61
s510	1.00	1.02	0.99	1.00	1.00	0.99	1.00	1.00	0.96	0.81	0.85	0.74	0.78	0.78	1.00	0.96	0.77	0.82	0.65	0.71	0.72
s641	1.00	1.06	1.00	1.01	0.98	0.98	1.02	1.00	0.86	1.06	0.84	0.76	0.80	0.78	1.00	0.85	1.01	0.76	0.67	0.76	0.67
s820	1.00	0.99	1.00	0.99	1.00	1.00	1.00	1.00	0.74	0.63	0.71	0.70	0.68	0.66	1.00	0.65	0.48	0.62	0.62	0.58	0.55
s832	1.00	0.99	0.99	0.99	0.97	0.99	0.98	1.00	0.90	0.79	0.56	0.72	0.72	0.72	1.00	0.86	0.73	0.44	0.62	0.63	0.62
s1238	1.00	0.98	1.06	0.96	0.89	1.00	1.05	1.00	0.93	0.81	0.79	0.81	0.74	0.70	1.00	0.85	0.71	0.64	0.68	0.62	0.55
s838_1	1.00	0.91	0.90	0.92	0.91	0.90	0.91	1.00	0.74	0.71	0.80	0.62	0.69	0.67	1.00	0.63	0.61	0.72	0.45	0.59	0.55
s1196	1.00	0.89	0.91	0.81	0.85	0.90	0.81	1.00	0.87	0.76	0.68	0.79	0.73	0.70	1.00	0.83	0.67	0.55	0.67	0.62	0.55
s1488	1.00	0.92	0.90	0.89	0.90	0.89	0.90	1.00	0.83	0.81	0.74	0.68	0.79	0.66	1.00	0.77	0.74	0.67	0.58	0.71	0.57
s1494	1.00	1.01	1.01	1.02	1.02	1.02	1.02	1.00	0.82	0.71	0.67	0.59	0.70	0.64	1.00	0.78	0.61	0.56	0.47	0.61	0.52
s1423	1.00	0.99	1.01	1.00	1.00	1.01	1.00	1.00	0.83	0.75	0.79	0.71	0.75	0.65	1.00	0.70	0.63	0.73	0.54	0.60	0.47
s5378	1.00	1.02	1.04	1.12	1.01	1.05	1.00	1.00	0.68	0.70	0.72	0.70	0.65	0.66	1.00	0.55	0.58	0.59	0.57	0.51	0.51
s9234_1	1.00	0.85	0.76	0.80	0.75	0.81	0.78	1.00	1.00	0.83	0.86	0.82	0.83	0.87	1.00	1.00	0.73	0.77	0.70	0.71	0.78
s13207	1.00	1.02	0.95	0.90	0.84	0.87	0.96	1.00	0.91	0.90	0.89	0.87	0.87	0.85	1.00	0.85	0.81	0.75	0.74	0.75	0.72
s15850	1.00	0.98	1.04	0.99	1.00	0.99	0.88	1.00	0.91	0.87	0.88	0.87	0.86	0.85	1.00	0.87	0.77	0.77	0.76	0.74	0.72
s38417	1.00	0.79	0.74	0.70	0.72	0.61	0.68	1.00	0.96	0.95	0.88	0.89	0.89	0.90	1.00	0.95	0.92	0.80	0.80	0.81	0.81
s38584	1.00	0.81	0.86	0.79	0.79	0.80	0.89	1.00	0.91	0.83	0.78	0.78	0.77	0.79	1.00	0.84	0.69	0.60	0.61	0.57	0.62
s35932	1.00	0.87	0.82	0.74	0.81	0.84	0.96	1.00	0.91	0.80	0.84	0.82	0.89	0.83	1.00	0.80	0.67	0.74	0.70	0.78	0.66
Average	**1.00**	**0.96**	**0.94**	**0.93**	**0.92**	**0.93**	**0.94**	**1.00**	**0.88**	**0.84**	**0.79**	**0.77**	**0.78**	**0.78**	**1.00**	**0.83**	**0.76**	**0.70**	**0.66**	**0.67**	**0.68**
Std. dev.	**0.00**	**0.07**	**0.08**	**0.09**	**0.08**	**0.09**	**0.08**	**0.00**	**0.11**	**0.15**	**0.11**	**0.10**	**0.11**	**0.10**	**0.00**	**0.14**	**0.19**	**0.13**	**0.12**	**0.12**	**0.13**

Table 2
Summary of results for 2 × delay constraint.

Design \pitch (μm)	Critical path length							Area							Power						
	0.72	0.80	0.88	0.96	1.04	1.12	1.20	0.72	0.80	0.88	0.96	1.04	1.12	1.20	0.72	0.80	0.88	0.96	1.04	1.12	1.20
s27	1.00	0.84	0.88	0.78	0.99	1.04	1.00	1.00	0.85	0.69	0.69	0.69	0.92	1.12	1.00	0.66	0.45	0.44	0.34	0.85	1.08
s208_1	1.00	1.11	1.06	0.99	1.05	1.09	1.00	1.00	0.86	0.93	0.83	0.79	0.87	0.79	1.00	0.79	0.91	0.72	0.65	0.81	0.66
s386	1.00	0.96	0.94	0.91	0.99	1.01	1.03	1.00	1.03	0.94	0.96	0.87	0.96	0.97	1.00	1.08	0.84	0.78	0.72	0.80	0.93
s298	1.00	1.04	1.01	0.95	0.96	1.04	1.05	1.00	1.15	1.05	0.91	1.01	0.99	0.93	1.00	1.36	1.15	0.80	0.98	1.06	0.79
s349	1.00	1.02	0.96	0.98	0.99	0.99	0.99	1.00	1.00	0.81	0.76	0.75	0.75	0.78	1.00	1.00	0.61	0.51	0.48	0.51	0.53
s344	1.00	0.95	0.99	1.00	0.90	0.94	0.94	1.00	0.83	0.88	0.83	0.83	0.88	0.85	1.00	0.68	0.77	0.63	0.64	0.70	0.65
s420_1	1.00	0.99	1.02	1.02	1.01	0.99	1.02	1.00	1.05	1.09	1.04	1.01	0.99	1.00	1.00	1.12	1.11	1.11	1.06	0.97	0.94
s400	1.00	1.02	1.08	1.06	1.02	1.04	1.04	1.00	1.01	0.98	0.87	0.89	0.90	0.86	1.00	1.10	0.97	0.74	0.78	0.79	0.73
s444	1.00	1.00	1.00	1.01	0.93	1.00	1.00	1.00	0.94	0.89	0.83	0.90	0.82	0.84	1.00	0.86	0.77	0.67	0.77	0.64	0.68
s526n	1.00	1.02	0.98	1.03	0.98	0.98	1.02	1.00	0.91	0.85	0.85	0.87	0.87	0.87	1.00	0.86	0.71	0.70	0.76	0.78	0.73
s526	1.00	1.01	1.00	0.99	1.01	0.99	1.01	1.00	0.94	0.93	0.90	0.85	0.84	0.81	1.00	0.90	0.84	0.78	0.75	0.71	0.65
s382	1.00	0.96	0.97	1.01	1.00	1.00	0.99	1.00	0.97	0.70	0.73	0.77	0.80	0.76	1.00	0.93	0.43	0.49	0.58	0.61	0.53
s713	1.00	1.01	1.00	0.98	1.00	1.01	1.02	1.00	1.06	1.01	1.01	0.90	0.92	0.91	1.00	1.12	0.89	1.10	0.85	0.86	0.81
s820	1.00	1.00	0.91	1.01	1.01	1.02	1.03	1.00	0.98	0.91	0.96	0.90	0.99	0.95	1.00	0.95	0.78	0.89	0.74	0.96	0.86
s641	1.00	1.02	1.02	1.03	0.96	1.03	1.01	1.00	0.75	0.73	0.71	0.71	0.76	0.75	1.00	0.55	0.50	0.47	0.49	0.60	0.54
s510	1.00	0.98	0.97	1.00	0.98	0.95	1.00	1.00	0.85	0.86	0.74	0.77	0.77	0.76	1.00	0.68	0.72	0.48	0.56	0.52	0.51
s832	1.00	0.97	0.99	1.00	0.98	1.00	0.97	1.00	0.97	0.92	0.86	0.83	0.84	0.83	1.00	0.93	0.86	0.71	0.67	0.68	0.67
s838_1	1.00	1.03	1.02	1.04	1.04	1.02	0.99	1.00	0.93	0.89	0.94	0.85	0.82	0.83	1.00	0.78	0.68	0.76	0.65	0.66	0.64
s1238	1.00	0.96	0.98	0.96	0.95	0.97	0.95	1.00	0.87	0.78	0.87	0.78	0.83	0.82	1.00	0.74	0.55	0.76	0.57	0.66	0.64
s1196	1.00	0.98	0.98	0.94	0.97	1.01	1.01	1.00	0.92	0.84	0.81	0.80	0.82	0.83	1.00	0.85	0.67	0.60	0.58	0.66	0.66
s1423	1.00	1.01	1.01	1.00	1.00	1.04	0.98	1.00	0.97	1.03	0.85	0.89	0.93	0.88	1.00	0.88	1.01	0.68	0.73	0.77	0.76
s1494	1.00	1.00	0.99	0.99	0.98	0.98	0.97	1.00	0.87	0.79	0.75	0.76	0.76	0.75	1.00	0.75	0.61	0.55	0.55	0.55	0.54
s1488	1.00	0.99	0.98	0.99	0.99	0.99	0.99	1.00	0.79	0.78	0.80	0.74	0.81	0.75	1.00	0.61	0.59	0.63	0.52	0.66	0.54
s5378	1.00	0.97	0.97	0.96	0.95	0.97	0.98	1.00	0.99	0.92	0.89	0.87	0.88	0.88	1.00	1.01	0.82	0.76	0.68	0.72	0.71
s9234_1	1.00	0.97	0.94	0.94	0.96	0.96	0.92	1.00	0.87	0.82	0.83	0.82	0.82	0.81	1.00	0.77	0.65	0.66	0.67	0.63	0.63
s13207	1.00	0.96	1.02	1.07	1.05	1.04	1.06	1.00	1.06	1.00	1.02	1.01	1.02	1.00	1.00	1.21	1.00	1.06	1.02	1.07	1.00
s15850	1.00	1.01	1.02	0.98	0.99	1.01	1.01	1.00	0.88	0.89	0.86	0.87	0.90	0.88	1.00	0.65	0.66	0.60	0.59	0.68	0.64
s38417	1.00	1.03	1.01	0.98	1.01	1.00	0.97	1.00	0.99	0.91	0.89	0.93	0.92	0.99	1.00	0.95	0.78	0.74	0.83	0.81	0.97
s38584	1.00	0.97	0.94	1.06	0.99	1.07	1.04	1.00	0.97	0.99	0.90	0.91	0.94	0.90	1.00	0.88	0.90	0.73	0.75	0.81	0.75
s35932	1.00	1.12	1.16	1.12	1.13	1.09	1.14	1.00	0.96	0.79	0.77	0.76	0.79	0.88	1.00	0.90	0.62	0.60	0.59	0.64	0.73
Average	**1.00**	**1.00**	**0.99**	**0.99**	**0.99**	**1.01**	**1.00**	**1.00**	**0.94**	**0.89**	**0.85**	**0.84**	**0.87**	**0.87**	**1.00**	**0.88**	**0.76**	**0.70**	**0.69**	**0.74**	**0.72**
Std. dev.	**0.00**	**0.05**	**0.05**	**0.06**	**0.04**	**0.04**	**0.04**	**0.00**	**0.09**	**0.10**	**0.09**	**0.08**	**0.08**	**0.09**	**0.00**	**0.19**	**0.18**	**0.17**	**0.16**	**0.14**	**0.15**

Table 3
Summary of results for 5 × delay constraint.

Design\pitch (μm)	Critical path length							Area							Power						
	0.72	0.80	0.88	0.96	1.04	1.12	1.20	0.72	0.80	0.88	0.96	1.04	1.12	1.20	0.72	0.80	0.88	0.96	1.04	1.12	1.20
s27	1.00	1.08	1.01	1.00	0.84	1.00	1.00	1.00	0.92	0.92	1.00	1.00	1.00	1.00	1.00	0.86	0.86	0.93	0.93	0.93	0.93
s208_1	1.00	0.92	0.81	0.80	0.76	0.82	0.76	1.00	0.94	0.91	0.91	0.93	0.91	0.91	1.00	0.80	0.71	0.72	0.75	0.72	0.73
s386	1.00	0.88	0.79	0.74	0.77	0.75	0.82	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.96	0.96
s298	1.00	0.82	0.88	0.84	0.84	0.83	0.82	1.00	1.00	0.99	0.99	1.00	0.98	0.98	1.00	0.99	0.84	0.84	0.87	0.83	0.83
s349	1.00	0.91	0.80	0.75	0.77	0.73	0.79	1.00	0.99	0.99	0.99	0.99	0.99	0.99	1.00	0.91	0.92	0.90	0.89	0.89	0.89
s344	1.00	1.19	1.35	1.22	1.16	1.32	1.11	1.00	0.94	0.89	0.91	0.93	0.93	0.85	1.00	0.86	0.67	0.75	0.72	0.83	0.67
s420_1	1.00	0.97	0.89	1.02	0.92	0.94	0.93	1.00	1.00	1.02	1.01	1.00	1.01	0.97	1.00	0.97	1.06	1.01	1.01	1.00	0.89
s444	1.00	1.00	1.04	0.90	0.86	1.01	0.82	1.00	0.99	0.96	0.94	0.95	0.97	0.96	1.00	0.92	0.78	0.78	0.81	0.86	0.81
s526n	1.00	0.91	0.99	0.88	0.97	0.86	0.88	1.00	1.00	0.99	0.99	0.99	0.99	0.99	1.00	0.97	0.93	0.88	0.89	0.91	0.89
s526	1.00	0.94	0.89	0.81	0.84	0.87	0.87	1.00	1.00	1.00	0.99	1.00	0.99	0.99	1.00	0.99	0.96	0.93	0.93	0.91	0.92
s382	1.00	1.02	0.97	1.04	0.96	1.00	0.91	1.00	0.86	0.86	0.85	0.85	0.85	0.84	1.00	0.55	0.60	0.54	0.55	0.56	0.51
s400	1.00	0.92	0.92	0.99	0.99	0.79	0.97	1.00	0.88	0.84	0.81	0.81	0.80	0.80	1.00	0.79	0.65	0.61	0.56	0.56	0.58
s713	1.00	0.93	0.98	0.95	0.99	0.88	0.87	1.00	0.95	0.90	0.81	0.80	0.86	0.83	1.00	0.89	0.74	0.56	0.51	0.64	0.56
s510	1.00	0.94	1.03	0.96	0.93	0.91	1.02	1.00	1.00	0.98	0.98	0.98	0.98	0.98	1.00	0.97	0.92	0.85	0.86	0.84	0.83
s641	1.00	1.02	0.96	1.02	0.94	0.98	0.98	1.00	0.84	0.79	0.78	0.77	0.79	0.77	1.00	0.58	0.48	0.45	0.41	0.47	0.42
s820	1.00	0.98	1.00	0.94	0.87	0.95	0.96	1.00	0.99	0.99	0.98	0.98	0.98	0.98	1.00	0.96	0.95	0.94	0.92	0.91	0.91
s832	1.00	0.92	1.03	1.02	1.00	1.00	0.98	1.00	0.97	0.97	0.96	0.96	0.98	0.96	1.00	0.87	0.88	0.83	0.84	0.96	0.86
s838_1	1.00	1.00	1.00	0.98	0.96	0.98	0.99	1.00	1.00	0.97	0.93	0.93	0.94	0.93	1.00	1.01	0.92	0.83	0.83	0.89	0.83
s1238	1.00	1.01	0.97	0.88	0.82	0.87	0.85	1.00	0.98	0.98	0.97	0.97	0.96	0.97	1.00	0.88	0.94	0.86	0.85	0.83	0.83
s1196	1.00	1.07	0.96	0.91	1.07	0.89	0.89	1.00	0.95	0.94	0.95	0.94	0.95	0.94	1.00	0.81	0.79	0.81	0.80	0.82	0.79
s1494	1.00	0.96	0.98	0.93	0.96	0.93	0.98	1.00	1.00	0.99	0.98	0.98	0.98	0.98	1.00	1.03	0.97	0.93	0.93	0.94	0.96
s1488	1.00	0.98	1.00	0.94	0.94	1.00	0.98	1.00	0.98	0.97	0.96	0.96	0.97	0.96	1.00	0.90	0.84	0.82	0.82	0.84	0.82
s1423	1.00	1.00	1.11	1.04	1.07	1.05	1.12	1.00	0.96	0.93	0.91	0.90	0.90	0.91	1.00	0.88	0.76	0.69	0.67	0.67	0.70
s5378	1.00	1.04	1.03	1.04	0.99	1.02	0.99	1.00	1.00	0.98	0.97	0.98	0.98	0.97	1.00	0.98	0.93	0.88	0.88	0.91	0.88
s9234_1	1.00	1.01	1.02	0.91	0.94	0.98	0.97	1.00	0.96	0.90	0.89	0.87	0.87	0.91	1.00	0.89	0.76	0.73	0.67	0.69	0.80
s13207	1.00	1.01	1.02	0.93	0.91	0.93	0.88	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.98	0.86	0.85	0.85	0.84	0.84
s15850	1.00	0.95	0.93	0.95	0.93	0.99	0.86	1.00	0.98	0.98	0.98	0.97	0.97	0.98	1.00	0.86	0.82	0.79	0.78	0.80	0.79
s35932	1.00	1.03	1.02	0.97	1.01	1.00	1.00	1.00	0.98	0.98	0.98	0.98	0.98	0.98	1.00	0.90	0.90	0.94	0.92	0.90	0.74
s38417	1.00	1.01	0.97	1.01	0.98	1.00	0.96	1.00	1.00	0.99	0.99	0.98	0.99	0.99	1.00	1.00	0.97	0.95	0.92	0.92	0.92
s38584	1.00	1.02	1.01	1.02	0.95	0.94	1.04	1.00	0.98	0.98	0.97	0.97	0.97	0.96	1.00	0.93	0.92	0.90	0.89	0.88	0.87
Average	**1.00**	**0.98**	**0.98**	**0.95**	**0.93**	**0.94**	**0.93**	**1.00**	**0.97**	**0.95**	**0.95**	**0.95**	**0.95**	**0.94**	**1.00**	**0.90**	**0.84**	**0.82**	**0.81**	**0.82**	**0.80**
Std. dev.	**0.00**	**0.07**	**0.10**	**0.10**	**0.09**	**0.11**	**0.09**	**0.00**	**0.04**	**0.05**	**0.06**	**0.06**	**0.06**	**0.06**	**0.00**	**0.11**	**0.13**	**0.14**	**0.15**	**0.13**	**0.13**

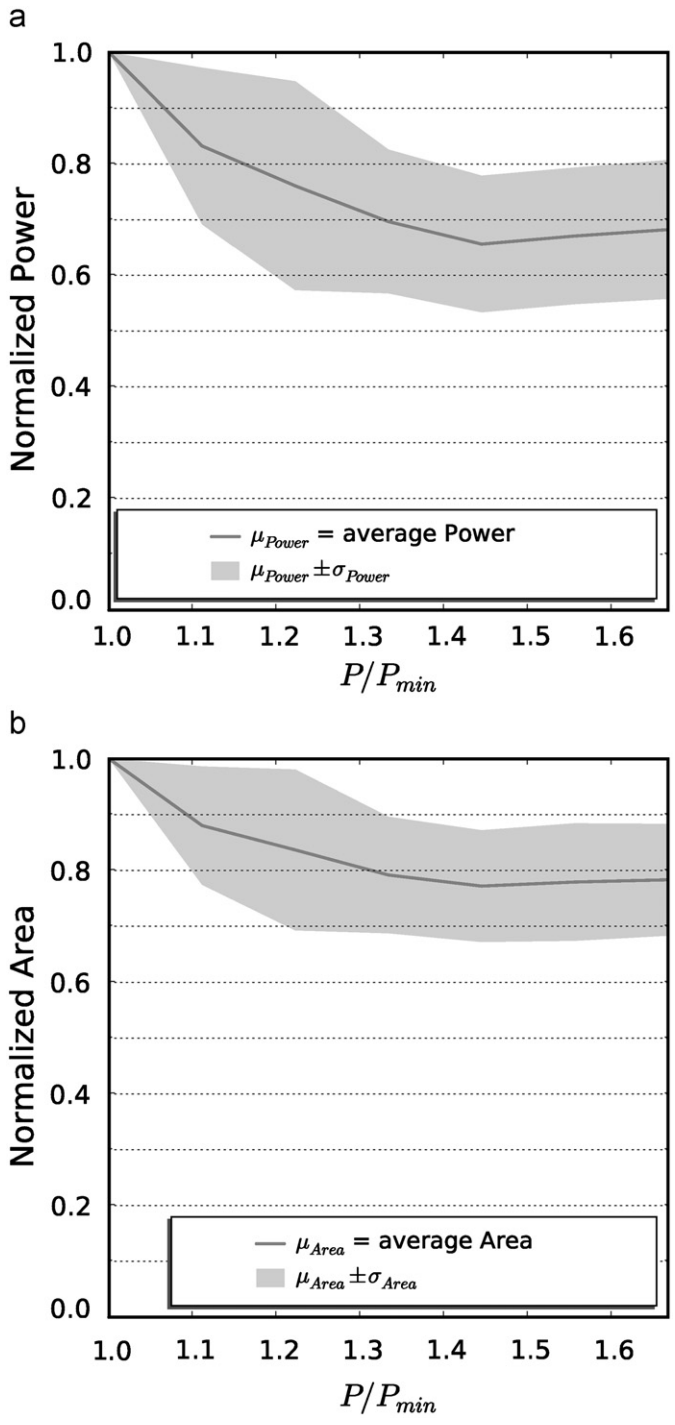

Fig. 7. (a) Normalized power versus P/P_{min}: average across the considered benchmarks and typical range (1 × delay constraint). (b) Normalized area versus P/P_{min}: average across the considered benchmarks and typical range (1 × delay constraint).

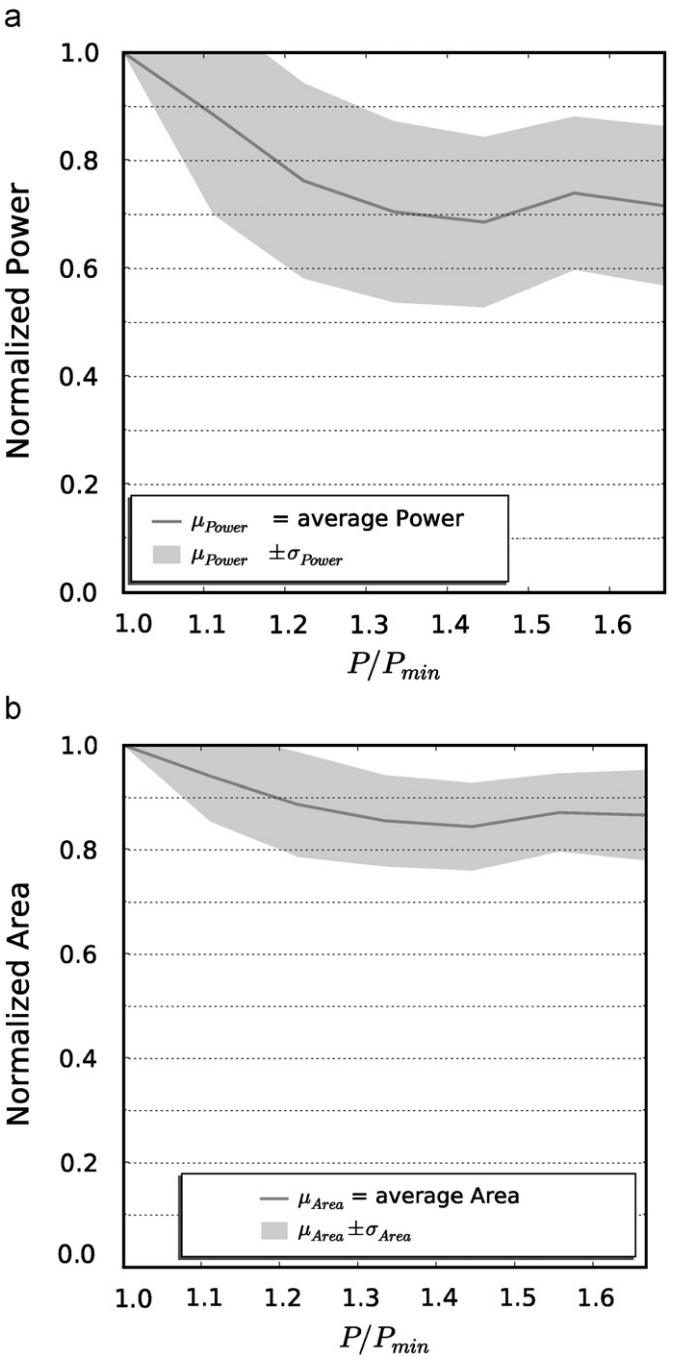

Fig. 8. (a) Normalized power versus P/P_{min}: average across the considered benchmarks and typical range (2 × delay constraint). (b) Normalized area versus P/P_{min}: average across the considered benchmarks and typical range (2 × delay constraint).

From Figs. 7–9, both power and area are always minimized for $P_{opt}=1.45P_{min}$–$1.5P_{min}$ under any design, which is close to the optimum value of $1.5P_{min}$ that was theoretically obtained in Section 4 from the minimization of the figure of merit in (2). Hence, the proposed metric in (2) consistently describes the power-delay-area tradeoff, and can be used for design purposes. Moreover, the optimum pitch is almost independent of the considered design, which agrees very well with qualitative considerations in Section 3.2. This is very interesting from a design point of view: indeed, this means that the optimum pitch can be found once and for all, then the same value can be used in different designs.

According to Fig. 7a, the adoption of minimum pitch leads to a 1.7 × increase in power and 1.3 × in area for the 1 × delay constraint, compared to the optimum case, thereby confirming that the optimization of P under differential routing is critical and has a strong effect on the power-delay-area tradeoff.

Comparison of Figs. 7–9 also shows that the optimum pitch is also independent of the delay constraint. However, the benefits of the pitch optimization tend to be reduced when the delay

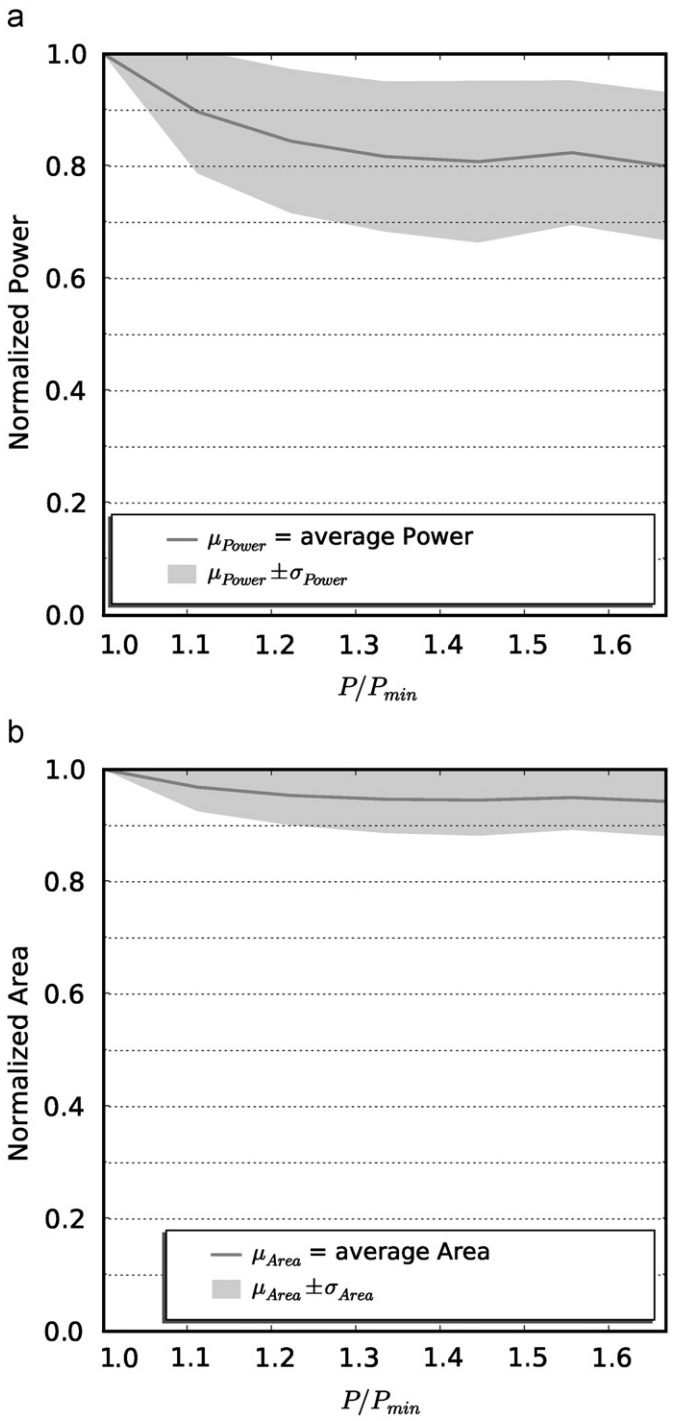

Fig. 9. (a) Normalized power versus P/P_{min}: average across the considered benchmarks and typical range (5 × delay constraint). (b) Normalized area versus P/P_{min}: average across the considered benchmarks and typical range (5 × delay constraint).

constraint is relaxed. Indeed, the power (area) under the optimum pitch is reduced by 20–45% (10–30%) when 1 × or 2 × delay constraint is assumed, compared to the minimum-pitch case. The power (area) saving reduces to 5–35% (less than 10%) when considering the 5 × delay constraint. This means that the pitch optimization is effective in reducing power and area for realistic cases where a high or moderate performance is required, whereas it is less advantageous in designs with very loose delay constraint. This can be intuitively explained by observing that, tight delay constraints force the synthesis tool to use high-strength cells, which suffer from high power consumption and area. Equivalently, when pitch is optimized, the resulting decrease in the wire capacitance leads to the adoption of cells with smaller strength, thereby significantly reducing the overall power and area (see note 1). On the other hand, under loose delay constraint, minimum-strength cells are usually adopted; hence the wire capacitance reduction due to the pitch optimization does not lead to a reduction in the cell power-area, because cells are already minimum-sized.

Finally, a moderate reduction of the gate count (in the order of 10%) was observed under the optimum pitch (curves are omitted for the sake of compactness). This can be explained by observing that, under minimum pitch, the wire capacitance is so high that it is advantageous to split each wire into several shorter wires, i.e. to use a larger number of gates. For the same above reasons, the gate count is largely independent of the grid pitch for loose delay constraints.

6. Conclusion

In this paper, the impact of routing grid pitch on the power-delay-area tradeoff has been analyzed in the case of intra-module fully differential routing. Analysis has showed that the wire grid pitch must be carefully set in circuits with differential routing, as opposite to traditional single-ended circuits, whose power-delay-area tradeoff is not so insensitive to the grid pitch. To quantitatively evaluate this tradeoff, a simple metric was introduced, and various interesting properties were derived from design considerations. The optimum grid pitch predicted by this metric agrees well with the optimum obtained in real designs, and is almost independent of the specific circuit under design. The design of 30 test circuits in 0.18 μm technology has shown that the pitch optimization can lead to a power and area saving at the same time, which, respectively, range from 20% to 45% and 10% to 30% for an assigned delay constraint. Reduced advantages are observed in circuits with very loose delay constraint.

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