LOW TEMPERATURE PYREX/SILICON WAFER BONDING VIA A SINGLE INTERMEDIATE PARYLENE LAYER

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ABSTRACT

We introduce a new low temperature (280 ºC) parylene-C wafer bonding technique, where parylene-C bonds directly a Pyrex wafer to a silicon wafer with either a Si, SiO_2 or Si_3N_4 surface with a bonding strength up to 23 MPa. The technique uses a single layer of parylene-C deposited only on the Pyrex wafer. Moreover, the process is compatible for bonding any type of wafer with small-sized micropatterned features, or containing microfluidic channels and electrodes. This technique can be an alternative for conventional bonding methods like anodic bonding in applications requiring a low temperature and diverse bonding interfaces.

KEYWORDS

Parylene bonding, microfluidics, packaging, 3D integration

INTRODUCTION

The conventional silicon-pyrex anodic bonding technique has been widely used in packaging of MEMS devices, fabrication of microfluidic channels and also for integration of electronics, fluidics and MEMS. The thickness and mechanical characteristics of the used materials in this technique give very high bonding strengths and the ability to withstand relatively large impacts. Unfortunately, electrode integration to devices that will undergo anodic bonding is challenging due to the high temperatures needed for the process. Although it has been shown that anodic bonding at low temperatures is possible [1], metal routing through the bonding interface is still not possible due to the fact that it is composed of refractory materials (single crystal silicon and Pyrex), for which topography represents a drawback for bonding. Hence, metallization is only possible with special techniques like three-dimensional (3D) metal integration and glass reflow, which increases stress on bonded wafers as well as fabrication complexity and cost. Moreover, the anodic bonding dictates that the silicon and Pyrex should come into contact for bonding, preventing straightforward integration of additional structures like microfluidic channels. A very popular example is integration of microfluidic channels for CMOS cooling, where a CMOS processed wafer has electrodes and a silicon nitride passivation layer on the surface.

Alternatively, bonding glass or silicon wafers with polymer glue is possible, even in the presence of topography, as the polymer layer is elastic and/or can be easily heated above its glass transition temperature. From the fluidic point of view, the main problem associated with polymer-bonded structures is that these polymers may be permeable to gasses like CO_2 and H_2. While this is a preventive drawback for hermetic packaging, gas permeation is favored in many biomedical and microfluidic applications. 3D integration schemes do not require hermeticity neither. As a consequence, polymer glue-bonded etched channels are very interesting for these types of applications.

Among different polymers used to perform polymer bonding, parylene-C has recently shown to perform the bonding operation based on the glass-transition mechanism [2-5]. An advantage of parylene-C is that it is depositable at room temperature, and it requires no thermal annealing and baking cycles during deposition [2-7]. In addition, low stress silicon/Pyrex wafer bonding is also possible by performing the bonding around the stress-free temperature of 270 °C [8], which is sufficiently low to be compatible with CMOS processing. On the other hand, demonstrated wafer bonding techniques using parylene as an intermediate glue layer require both of the wafers to be coated with parylene-C, after which the bonding is performed physically [2-3] between the two parylene layers.

Such approach with a double parylene layer has imposed certain limitations on the applicability of this technique as well as the bonding strength. Firstly, the physically formed parylene/parylene bonding interface has been reported to be the interface of fracture and avoiding this interface may increase bonding strength. This can be achieved if parylene-C could be bonded directly to wafers (Si, SiO_2 or Pyrex) or common layers used in silicon microfabrication process like SiO_2 and Si_3N_4. In this case, performing bonding with a single parylene-C layer to various silicon wafer-based surfaces has the advantage of easier processing when structural features like microchannels are to be realized in the parylene-C layer. In addition, both silicon wafers with CMOS devices having a silicon nitride passivation layer, and silicon wafers with released MEMS devices with or without SiO_2 layer can be bonded with no pre-processing. In fact, this may allow very easy 3D integration, the addition of high pressure-resistant microfluidic channels to CMOS and MEMS devices, and low-temperature packaging with common MEMS structures. In contrast, conventional techniques like anodic bonding neither provides flexibility to choose material in the bonding interface nor metal routing through bonding areas.

In accordance, we introduce a Pyrex/silicon wafer bonding method performed at 280 ºC with a single parylene-C layer deposited on the Pyrex wafer. Pull tests

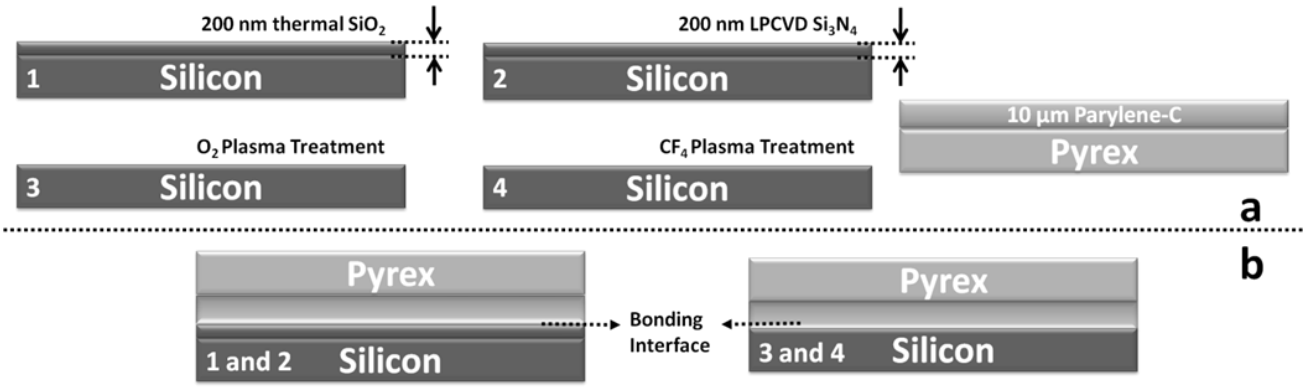

Figure 1 – Illustration of the bonding process. (a) The process uses a Pyrex wafer covered with a 10 µm thick parylene-C layer. 4 different silicon substrates have been prepared: (1) with 200 nm thermal SiO_2 , (2) with 200 nm LPCVD Si_3N_4, (3) application of an O_2 plasma to a bare wafer at 500 W, under 400 sccm O_2 during 5 min, (4) application of a CF_4 plasma to a bare wafer at 1800 W, under 20 sccm, during 30 s. (b) All of the bonding with parylene-C was performed at 280 °C under vacuum during 40 minutes while applying 1000 mbar pressure. Prior to bonding, Pyrex wafers were plasma-treated during 15 s at 200 W under 400 sccm O_2 flow for surface activation of the parylene-C layer.

demonstrated that parylene-C directly bonds to Si, SiO_2 and Si_3N_4 with a bonding strength up to 23 MPa, which is close to the typical anodic bonding strength of 40 MPa [1] and provides an order of magnitude increase when compared to existing wafer bonding methods with intermediate gluing layer [2-3].

FABRICATION

We have studied the bonding of Pyrex wafers via parylene-C directly to bare silicon surfaces after O_2 and CF_4 plasma application, as well as bonding to SiO_2 and Si_3N_4surfaces. These gases and surfaces are selected among the most widely used in conventional microfabrication. The fabrication process is summarized in figure 1.

Briefly, 4 different silicon substrates have been prepared for bonding: (1) a 200 nm thermal oxide and (2) a 200 nm LPCVD Si_3N_4 layer. Moreover, we also bonded bare silicon wafers treated with (3) an O_2 plasma at 500 W, under 400 sccm O_2 during 5 min, and (4) a CF_4 plasma at 1800 W, under 20 sccm, during 30 s. All of the Pyrex wafers are coated with 10 µm parylene-C using Comelec C-30-S parylene deposition system and they were subsequently O_2 plasma-treated at 200 W during 15 seconds for surface activation using a Tepla 300 plasma system under 400 sccm O_2 flow. Next, wafers were bonded at 280 ºC during 40 minutes under vacuum with a tool pressure of 1000 mbar (Suss SB6 vacuum bonder). Although parylene bonding with lower temperatures is possible [1-3], the selection of the temperature is done to be close (± 20 ºC) to stress-free bonding temperature of 280 ºC for silicon and Pyrex [8].

For cross-sectional SEM observation of the bonding interface, the bonded wafers are diced, polished and coated with 20 nm carbon to prevent charging. The carbon coating keeps sufficient contrast in SEM while preventing charging on the surface. Figure 2 is a SEM image, showing a parylene-C/Si bonding stack. The parylene-C/Si bonding interface is not different from the coating interface. Other bonding combinations also show no difference between the two interfaces.

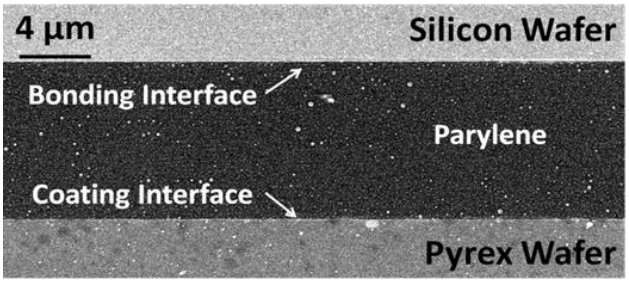

Figure 2 – SEM image of a cross-section of the bonding stack and the parylene-C/Si bonding interface. Cross-sections of the bonding stack were realized by dicing the wafers, followed by polishing and thermal evaporation of a 20 nm thick carbon layer for SEM observation. Other bonding combinations also show no difference in bonding quality between the two interfaces.

EXPERIMENTAL WORK AND RESULTS

Parylene Thickness

The thickness of the parylene-C layer after bonding may be of importance in certain applications like in microfluidics, where thickness defines the channel height, or like in electrical integration, where variations in thickness may result in changes in capacitive coupling between electrodes located at opposite sides. In order to determine the thickness change during bonding, the parylene-C thickness has been measured before bonding using a Nanospec AFT-6100 spectro-reflectometer at different locations. After bonding, cross-section SEM images for different samples at different locations are used to determine the parylene-C thickness. Figure 3 shows a comparative histogram of parylene-C thickness measurements: before bonding, measurements indicate a thickness of (9.77 ± 0.07) µm, while after bonding a thickness of (9.10 ±0.16) µm is observed, corresponding to a 7% thickness reduction on average.

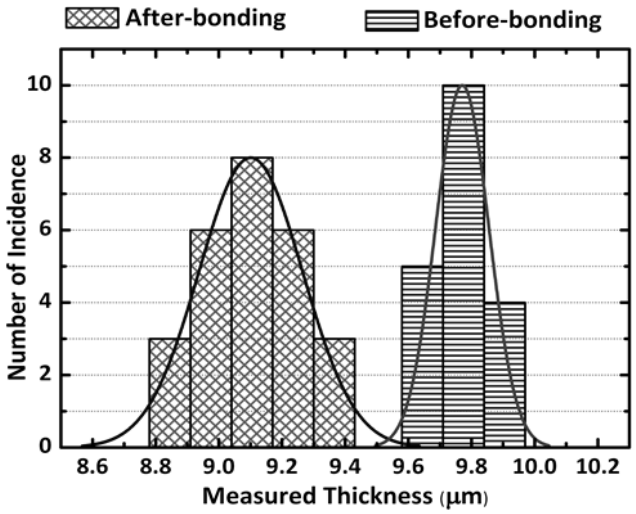

Figure 3 – Histogram of parylene-C thickness measurements before and after the bonding, obtained from cross-section observations. Before bonding, measurements indicate a thickness of (9.77 ± 0.07) μm, while after bonding a thickness of (9.10 ± 0.16) μm is observed, corresponding to a 7% thickness reduction on average.

Pull-tests and the Bonding Strengh

In order to determine the bonding strength, pull test measurements have been performed. First, bonded wafers have been diced into 95 mm^2 square dies. Then, aluminium pulling bars (3 cm x 1 cm x 1 cm) were used to fix the dies to the pull-test equipment (figure 4.a) by superglue. The tests were performed in a Zwick 100 kN

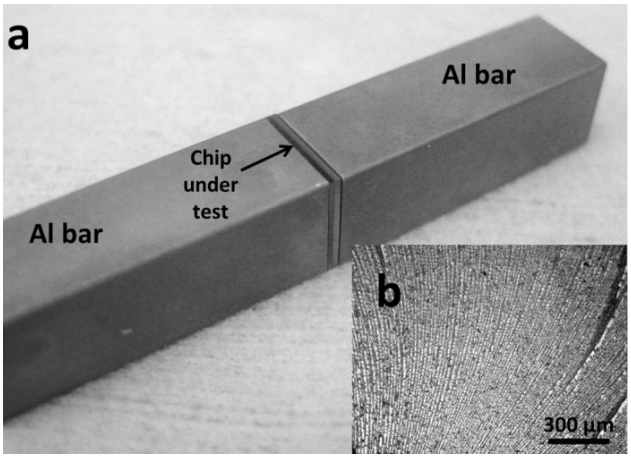

Figure 4 – Bonded samples for pull-testing. (a) Assembly of sample with aluminium pulling bars. (b) Optical microscope image of fractured interface after pull-testing. In general, fracture occurs in the form of cracks within the parylene-C layer.

electromechanical computer-controlled universal testing apparatus (Zwick GmbH, Germany) with 0.1 mm/min pull rate and the force was recorded via a computer-controlled interface. After mounting the sample, the force and torque were automatically adjusted for ensuring that the pull force was perpendicular to the die surface. With constant pull rate, the fracture point was calculated by the data point where the observed force suddenly decreases. Then, this force is divided by the die area to find the bonding strength. For each case, at least 6 samples were tested.

Figure 5 shows the results of pull test measurements in comparison with the achievement of existing techniques. The results suggest that the applied pretreatments and layers used for bonding parylene-C have greatly changed the bonding strength. Case (1) with the 200 nm SiO_2 film has demonstrated a mean strength of 10 MPa, while case (2) with 200 nm of Si_3N_4 has demonstrated a mean of 23 MPa, reaching a maximum of 27 MPa, an order of magnitude increase with respect to current parylene/parylene bonding techniques as well as other low temperature polymer glue bonding techniques. Case (3) with the O_2 plasma-treated bare Si wafer demonstrates a mean bonding strength of 8.8 MPa, while case (4) with CF_4 plasma-treated bare Si wafer shows a mean bonding strength of 12.3 MPa.

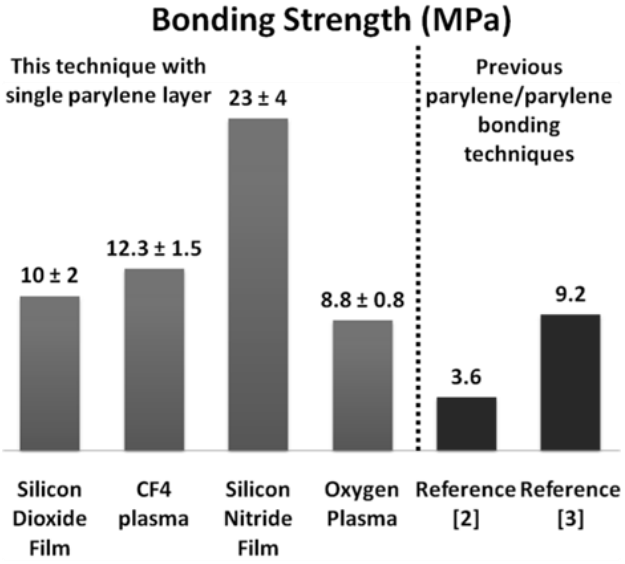

Figure 5- Results of the pull-test measurements for different cases and comparison with existing parylene/parylene bonding techniques. For this study, each bar corresponds to mean of at least 6 experiments. For comparison, anodic bonding results in a bonding strength around 30-40 MPa depending on the bonding temperature [1].

Figure 4.b shows a light-microscope image of a fractured interface, where the parylene-C is seen to be detached under formation of cracks. The fracture patterns were observed equally in the parylene-C layer as well as on the deposition interface, but never on the bonding interface. This suggests that the oxygen plasma treatment of the parylene-C layer before bonding generates carbon radicals and C-O linkages on the parylene-C surface [9], which convert to strong bonds with silicon compounds layer during the 280 ºC heating step, similar to siloxane bond formation in a silanization process.

CONCLUSIONS

We have demostrated a new low temperature (280 ºC) parylene-C wafer bonding technique, where parylene-C bonds directly to Si, SiO_2 and Si_3N_4 with high bonding strengths compared to existing polymer glue processing. The technique works for silicon wafers having a Si, SiO_2 or Si_3N_4 surface and uses a single layer of parylene-C deposited only on the Pyrex wafer. The ability to bond directly to these common materials using only a single layer of parylene-C increases the versatility of this technique when compared with conventional methods like anodic bonding. For example, ability to bond silicon nitride surfaces may allow straightforward 3D integration of CMOS circuits using their 'natural' passivation layer as well as simple integration of microfluidic channels, for example, for microchip cooling. By applying a single layer of parylene-C on several wafers, multiple wafer bonded stacks can also be formed simultaneously in a single bonding operation. In addition to these possibilities, the pull tests revealed that a bonding up to 23 MPa can be achieved, suggesting an order of magnitude increase with respect to existing double parylene/parylene bonding techniques and a bonding strength which is close the one achieved in anodic bonding. We anticipate that the demonstrated technique will open new perspectives in applications like microfluidics, packaging and 3D integration where bonding is inherently needed.

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