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# Mechanical failure analysis of thin film transistor devices on steel and polyimide substrates for flexible display applications

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ABSTRACT

The crack onset strain (COS) of 4-level thin film transistor (TFT) devices on both steel foils and thin polyimide (PI) films was investigated using tensile experiments carried out in situ in an optical microscope. Cracks initiated first within the $SiO_2$ insulator layer for both types of substrates. The COS was found to be equal to 1.15% and 0.24% for steel and PI, respectively. The influence of loading direction on failure of the TFT stack with anisotropic geometry was moreover found to be considerable, leading to recommendations for backplane design. The large difference in critical strain of the $SiO_2$ layer on the two substrates was analyzed using an energy release rate approach, and found to result from differences in layer/substrate mechanical contrast and in internal stress state. Based on this analysis a correlation between layer/substrate elastic contrast and tensile failure behavior was devised.



## 1. Introduction

Backplanes for flexible display devices, like organic light emitting devices (OLED) are multilayer structures comprising a thin polymer, glass or metal-based substrate on which several functional layers are deposited [1]. The reliability and admissible radius of curvature of the flexible devices is controlled by the mechanical properties of the multi-material assembly, and, more specifically by the cohesive properties of the material constituents and by their interfacial adhesion [2,3]. In the case of inorganic layers (oxides, nitrides) used as insulator, passivation and diffusion barrier coatings, the critical strain for layer cracking (crack onset strain, COS) is usually in the range from 0.8% to 1.8% [4–6]. Thin film transistor (TFT) devices on polyimide films were reported to fail at ~0.3% strain [3,7]. These strains, in combination with substrate height, result in critical radius of curvature in the range from 2 to 9 mm [7–9]. The COS is controlled by the energy released during the fracture event, which depends on layer toughness, layer thickness and layer/substrate elastic contrast [10,11]. The COS also depends on the residual stress state in the layer [12]. For a layer with given thickness and toughness, the COS will therefore depend on the substrate properties.

The objective of the present work is to analyze the critical strain for onset of tensile damage of brittle layers on steel and polyimide substrates [3]. The two substrate materials present markedly different mechanical contrast, with a stiffness ratio close to 20. Their thickness also differs considerably, the steel substrate being almost 20 times thicker. As a consequence, one

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may anticipate significant differences in terms of mechanical damage under stress for the two cases, and detailed information on this issue should be useful in terms of design of flexible devices like displays. In this work attention was paid to 4-level TFTs structured on $SiO_2$ insulator layers. In addition, since the geometry of the TFT devices is anisotropic, attention was also paid to the influence of the loading direction on the failure of the TFT structures.

## 2. Materials and experimental methods

Two substrates were investigated, namely a steel foil and a thin polyimide film, as detailed in the following two sections. Table 1 summarizes the elastic properties of relevant materials, together with elastic mismatch parameters discussed in following sections.

### 2.1. 4-Level low-temperature poly-silicon TFT on steel

A 152 μm thick stainless steel foil (annealed SS304 S15, Precision Micro, UK) was used with the following composition (wt.%): C: 0.08; Mn: 2.00; P: 0.045; S: 0.030; Si: 1.00; Cr: 19.00; Ni: 9.25; the rest being Fe. The foils were degreased in a soap solution, rinsed in deionised water, and dried. The steel foil was used without polishing. The process for the fabrication of the 4-level low-temperature poly-silicon (LTPS) TFT depicted in Fig. 1 comprised six steps. In step 1, a 500 nm thick $SiO_2$ insulator and a 80 nm thick a-Si layer were deposited by plasma-enhanced chemical vapor deposition (PECVD), which was followed by dehydrogenation and by crystallization of the a-Si layer using excimer laser annealing into poly-Si. In step 2, the poly-Si layer was patterned using lithography and dry etching to define active areas of the TFTs (first mask level). In step 3, the gate oxide (100 nm thick $SiO_2$) was deposited by PECVD and the gate metal (200 nm thick Al) was deposited using physical vapor deposition (PVD). In step 4, the gate was patterned by lithography (second mask level) followed by etching of the gate metal and gate oxide. Then p-type ion implantation was made using gate as mask (self-aligned process). Dopant activation was performed using excimer laser. In step 5, a 500 nm thick $SiO_2$ passivation layer was deposited by chemical vapor deposition (CVD) and patterned using lithography (third mask level) and etching to open contacts to the source, drain and gate electrodes. In step 6, the source and drain metals were deposited (30 nm thick TiW and 200 nm thick Mo) by PVD, and patterned (fourth mask level). The total thickness of the $SiO_2$ insulator layer outside of the TFT area was therefore equal to 1000 nm. Four different TFT geometries were produced with channel length $L$ equal to 3, 10, 50 and 100 μm and channel width $W$ equal to 100 μm.

### 2.2. 4-Level low-temperature poly-silicon TFT on polyimide

Prior to TFT fabrication, a 8 μm thick polyimide (PI) film was spin coated on a standard Corning Eagle APT glass carrier, baked on a hot plate and cured in an oven. This PI was released from the carrier after TFT fabrication using the proprietary EPLaR technology developed by Philips [13]. The process for the fabrication of the 4-level LTPS TFT comprised essentially the same steps as for the steel substrate case. The total thickness of the brittle layer outside of the TFT area is in the present case equal to 1280 nm. The same rectangular TFT geometries produced on steel were also produced on the thin PI substrate.

### 2.3. Experimental methods

Fragmentation tests were carried out under uniaxial loading at a nominal rate equal to 0.5 mm/min using a miniature tensile frame (MiniMAT, Rheometric Systems), in situ in an optical microscope (Olympus BX60) [9]. The evolution of crack patterns in the TFT structures was monitored as a function of the uniaxial strain applied to the substrate. The in situ observation enabled to accurately determine the locus of failure and the COS. Video-extensometry was used to measure strain, with an error of 0.04% [6].

Steel-based fragmentation test samples were cut from the steel foil by electro-machining, in form of dog-bone type samples with a reduced section of $10 \times 25$ mm. PI-based fragmentation test samples were cut with a laser into rectangular strips of 7 mm width and 50 mm length. For the steel substrate, two perpendicular orientations were considered, both parallel to the edges of the rectangular backplane foil, so that the rectangular-shaped TFTs could be loaded parallel and perpendicular to the main axis of the gate, defined as the direction parallel to the channel length $L$.

The process-induced residual stress state of the layered structures was not investigated. This analysis would require techniques to monitor the dynamics of stress build-up during process steps and numerical tools to simulate the thermo-mechan-

**Table 1**
Elastic mismatch parameters of $SiO_2$/substrate two-layer systems.

| $SiO_2$/substrate two-layer system | Young's modulus (GPa) | | Poisson's ratio | | Dundurs parameters | |
|---|---|---|---|---|---|---|
| | $SiO_2$ ($E_f$) | Substrate ($E_s$) | $SiO_2$ ($\nu_f$) | Substrate ($\nu_s$) | $\alpha$ | $\beta$ |
| $SiO_2$/steel | 80 | 195 | 0.17 | 0.3 | −0.445 | −0.208 |
| $SiO_2$/PI | 80 | 10 | 0.17 | 0.3 | 0.765 | 0.205 |

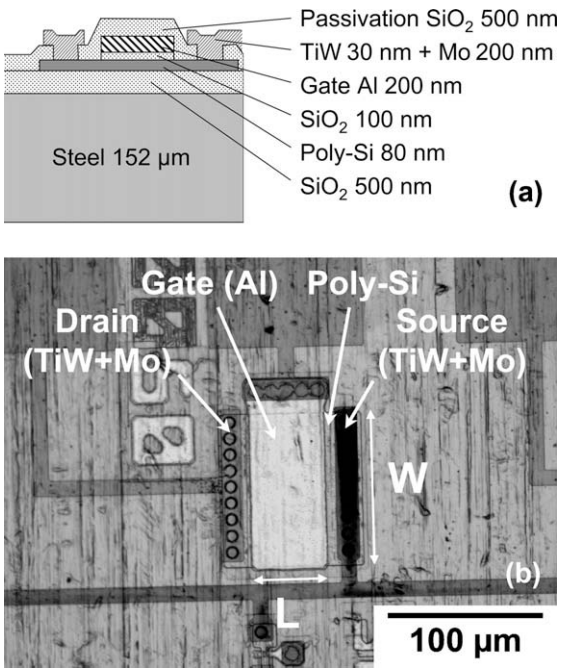


**Fig. 1.** Structure of a 4-level TFT device on steel (a) and top view of a device with gate length $L = 50$ µm and width $W = 100$ µm (b).

ical response of the complex three-dimensional architecture of the TFT structures, combined with experimental validation based on X-ray diffraction methods to probe the residual stress state of the crystalline materials present in the devices, all being outside of the scope of the present study. Since tensile damage initiated within the $SiO_2$ insulator as will be detailed in the next section, the stress state in this layer was estimated based on the thermal stress (one should be aware that the total stress also comprises an intrinsic contribution, usually compressive and, in case of polyimide substrate, an hygroscopic contribution, usually tensile [14]). The thermal strain in the $SiO_2$ layer on steel $\varepsilon_c$ was evaluated assuming that the coefficients of thermal expansion (CTE) of the steel ($17 \times 10^{-6}\,K^{-1}$) and of the $SiO_2$ ($5 \times 10^{-7}\,K^{-1}$) were independent of temperature between the maximum LTPS process temperature equal to 400 °C in the present work and the room temperature. It was found to be compressive and equal to −0.63%. The CTE of the thin PI film was unknown and the thermal stress could not be calculated. In fact, the residual stress in this case was also controlled by the shrinkage of the PI during cure, and a specific study is required on this topic.

The Young's modulus of the substrate materials was determined under tensile loading using a UTS Testsystem tensile testing frame for the steel substrate and an Instron 5566 universal testing machine for the PI film. The latter tests were performed in a controlled environment (21 ± 1 °C, 50 ± 5% RH). The Young's modulus of the $SiO_2$ insulator layer was assumed to be equal to that of similar layers, determined from the analysis of tensile test data [15]. The Poisson's ratio of the materials was taken from literature. The data are reported in Table 1.

## 3. Damage phenomenology of 4-level tfts on steel and pi under uniaxial tensile loading

### 3.1. Influence of substrate on critical strain for layer cracking

Fig. 2 shows the damage state at three strain levels in a 100 µm × 100 µm TFT on unpolished steel during tensile loading. At 0% strain, the roughness of the steel substrate is evident, but the layers and the TFT structure were intact. It should be noticed that the roughness state mainly comes from the grooves of the milling of steel sheets. Cracking of the $SiO_2$ layer was detected near the gate. The COS was found to be equal to 1.15 ± 0.05%. At increasing strain levels, cracks propagated on the gate (1.38% strain) and buckling of the $SiO_2$ layer was detected (1.40% strain) with formation of splinters probably coming from the $SiO_2$ layer (1.75% strain, not shown). At 2.03% strain several splinters resulting from extensive buckling of the $SiO_2$ layer are visible on the gate. The TFT structure appeared to be the most robust part of the whole layered thin film structure.

Fig. 3 shows a similar damage sequence in the case of the PI substrate. Again, the multilayer structures were intact prior to straining. Cracks also initiated in the $SiO_2$ insulator layer, at the location of metal lines. The COS was found to be equal to 0.24 ± 0.04%, a factor of 4.8 lower than that determined for the steel substrate case. Similar critical strain values (0.34%) have been reported for transistors on plastic substrates [7,16]. At 0.31% strain several cracks were found to have propagated in the

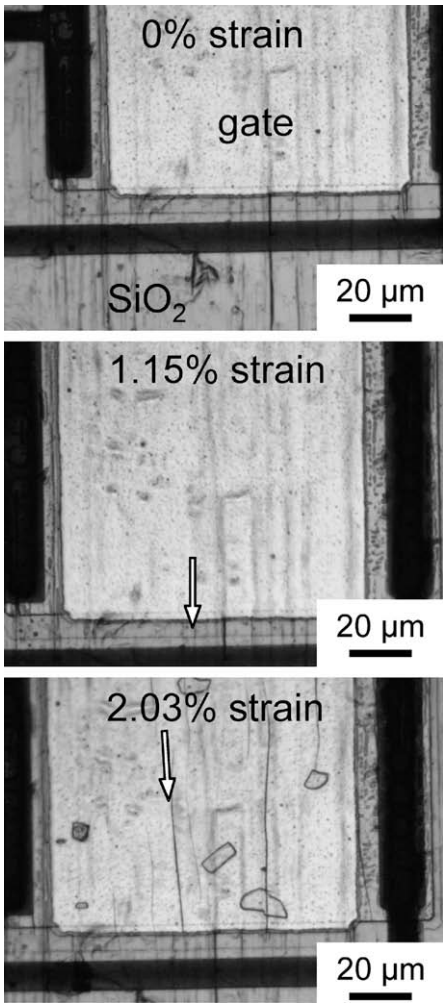


**Fig. 2.** Damage of a 100 μm × 100 μm TFT device on a 152 μm thick steel foil under uniaxial strain (with tensile axis parallel to the scale bars). The arrows indicate the location of a tensile crack which initiated and propagated in the $SiO_2$ insulator layer (1.15% strain) and in the TFT stack (2.03% strain).

$SiO_2$ layer, outside of the TFT stack first, and eventually within the stack around 0.7% strain. No buckling was detected, up to 0.9% strain.

The narrow distributions for the COS are in accordance with experiments presented in Chapter 6 of [1]. The fundamental reason for such narrow distributions is that the reported COS describes the steady-state crack propagation in a brittle layer on a compliant substrate. It is determined by the fracture toughness of the layer and the layer thickness. Both values are approximately constant and the scatter in COS values is consequently small. Note that cracks can only propagate when they are initiated first. In the present analysis sufficient crack initiation points are expected to be present. Only when the defect density is quite low, the practically observed COS might show large variations, as was reported in Chapter 6 of [1] and [17].

The reason for the considerable difference in COS of the $SiO_2$ layer on either steel or PI substrates should be sought in differences in mechanical contrast, i.e., specific influence of substrate thickness and stiffness, in addition to differences in residual stress state, which will be discussed in Section 4.

### 3.2. Influence of loading direction and TFT orientation

The influence of the loading direction and TFT orientation on damage processes is shown in Figs. 4 and 5 for the steel and PI substrates, respectively. The width $W$ of the TFT is constant (100 μm) and the length varies (3 μm $\leqslant L \leqslant$ 100 μm). The results clearly reveal the considerable effect of stress transfer phenomena in such layered structures. In case of 100 μm × 50 μm TFTs, the gate section of the TFT remained intact when loaded parallel to its length in contrast to when it was loaded perpendicular to its length, which resulted in severe damage with high crack density. This is the best example of the anisotropic behavior. In case of 100 μm × 10 μm TFTs, again, the gate remained intact when loaded parallel to its

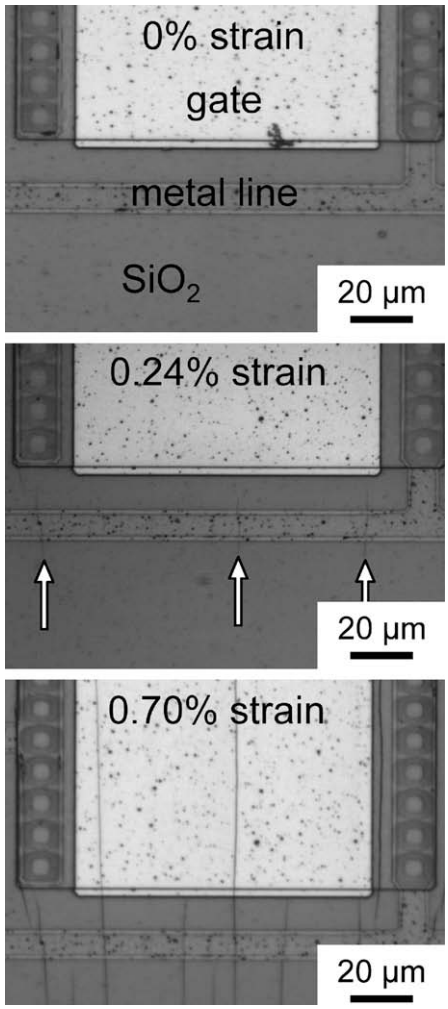


**Fig. 3.** Damage of a 100 μm × 100 μm TFT device on a 8 μm thick PI under uniaxial strain (with tensile axis parallel to the scale bars). The arrows indicate the location of initial tensile cracks found in the $SiO_2$ insulator layer in the vicinity of metal lines.

length, but was extensively damaged (cracking and buckling) in the perpendicular direction. In case of 100 μm × 100 μm TFTs (not shown in Fig. 4), the crack density on the gate was similar for both directions but spallation of the $SiO_2$ layer took place only in case loading was carried out parallel to the gate length, i.e. perpendicular to the preferred-orientation roughness due to the milling grooves. In fact, when loading was parallel to the gate length, the TFT with a 100 μm gate length was cracked while the TFT with a 50 μm or smaller gate length showed no damage on the grid. Fig. 5 shows similar findings for the PI substrate, in which the influence of the TFT geometry (varying gate length $L$, for a fixed gate width $W$) on cracking is evident. Similar to the case of steel substrate, due to stress transfer properties between adjacent layers, shorter gates are less susceptible to cracking providing that the loading direction is parallel to the gate length.

An estimate of the critical gate length below which cracking should not occur is obtained from the analysis of the crack density in the gate at high strain. Cracking of a layer on a substrate results from the transfer of substrate stresses to the layer through interfacial shear. The latter operates over the so-called critical stress transfer length, below which only a limited amount of substrate stress is transferred to the layer. In other words structured layers (e.g., TFTs) with a length smaller than the critical stress transfer length will not feel the substrate stress, hence will not crack. In practice, the critical stress transfer length is proportional to the inverse of the crack density (proportionality factor equal to approximately 1.5 [15]). For both steel and PI substrates, an average of ten cracks in the 100 μm long gate were detected at the highest investigated strain. The corresponding crack density is equal to $(10\ \mu m)^{-1}$, hence the critical length is equal to 15 μm. This means that devices of dimension less than 15 μm along the loading direction should not crack. Notice that this value is an estimate based on the analysis of an average spacing. An accurate analysis would require accounting for the multilayer structure of the devices, and details about the scatter in crack spacing should be considered for reliable device design.

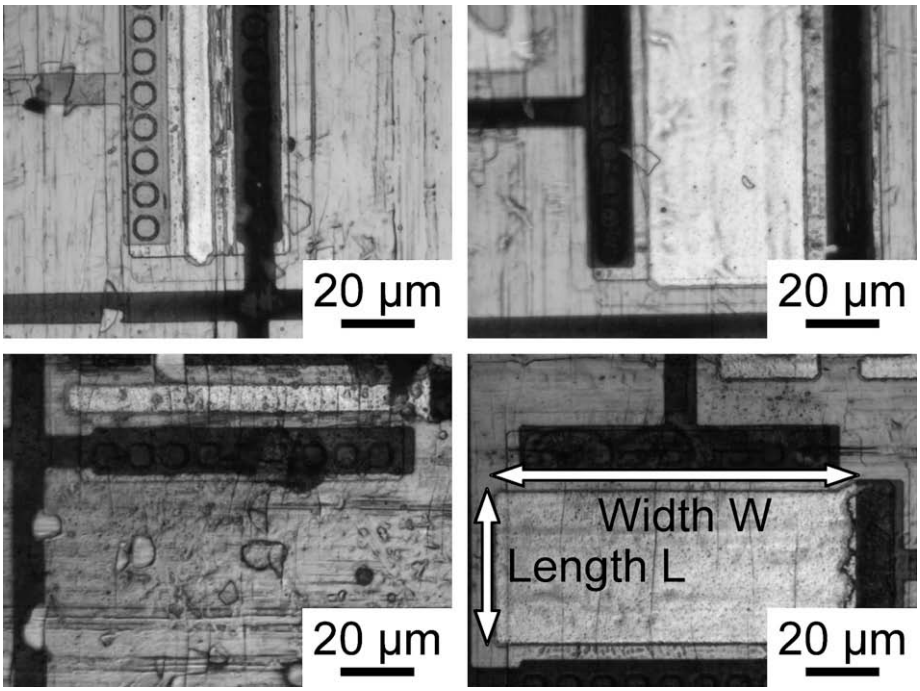


**Fig. 4.** Fragmented morphology of 10 μm × 100 μm and 50 μm × 100 μm TFT devices on 152 μm thick steel under 2% strain, loaded parallel (top) and perpendicular (bottom) to the gate length direction.

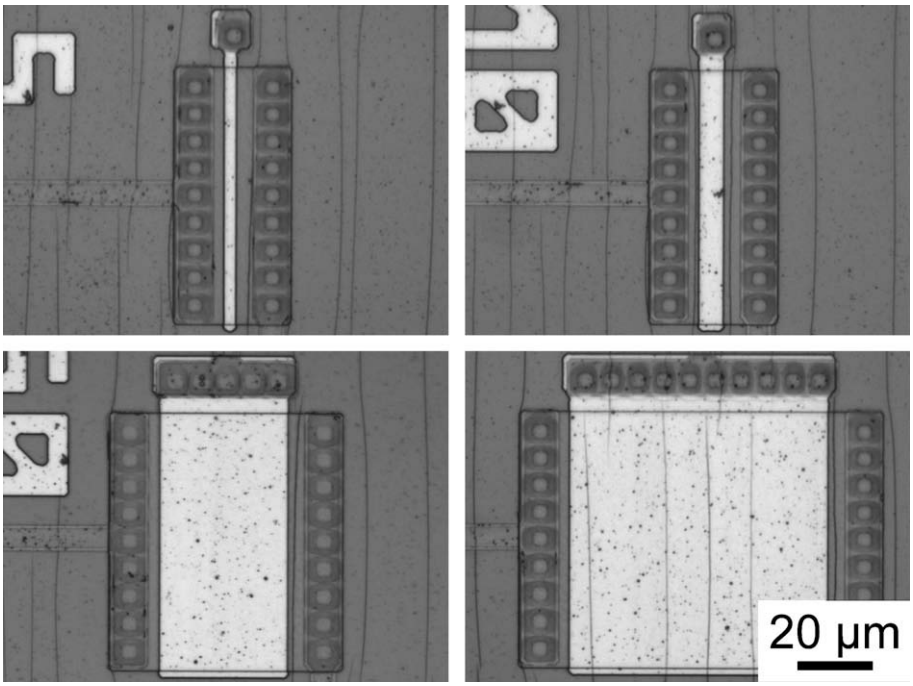


**Fig. 5.** Fragmented morphology of TFT devices with 3, 10, 50 and 100 μm channel length on 8 μm thick PI under 0.92% strain. The loading direction was parallel to the scale bar (i.e., parallel to the gate length).

The practical consequence of these results is in terms of backplane design: devices of anisotropic geometry should be preferably oriented with longest dimension parallel to the bending axis, and their shortest dimension should be smaller than approximately 15 μm.

## 4. Modelling of the influence of mechanical contrast

### 4.1. Elastic mismatch parameters

The Young's modulus of $SiO_2$ (80 GPa) is between that of steel (195 GPa) and PI (10 GPa). The $SiO_2$/steel and $SiO_2$/PI layered structures present opposite mechanical contrast properties between layer and substrate. Following fracture mechanics theories (e.g. [10]), such a difference in contrast is expected to contribute to the measured difference in COS. This was investigated using an energy release analysis of through-thickness channeling cracks in the $SiO_2$ layer. It was assumed that no delamination occurred at the COS, when initial cracks formed. Also, the TFT structures were not considered since cracks initiated and propagated first in the $SiO_2$ layer as was shown in Figs. 2 and 3. Two different two-layer systems were eventually analyzed, namely a 1 μm thick $SiO_2$ layer on a 152 μm thick steel substrate, and a 1.28 μm thick $SiO_2$ layer on a 8 μm thick PI.

The plane strain analysis of the crack opening displacement of a steady-state crack [10,12] was used to relate the steady state energy release rate $G_{ss}$ to the elastic parameters of the layer/substrate structure:

$$G_{ss} = \frac{1}{2}\frac{\sigma^2 h}{\bar{E}_f}\pi g(\alpha,\beta) \tag{1}$$

where $h$ and $\bar{E}_f = E_f/(1-\nu_f^2)$ are the thickness and plane strain modulus of the $SiO_2$ layer ($E_f$ and $\nu_f$ are the Young's modulus and Poisson's ratio of the layer) and $g(\alpha, \beta)$ is a function of the Dundurs parameters $\alpha$ and $\beta$ [18], which describe the elastic mismatch of the layer/substrate system. In the case of plane strain problems:

$$\alpha = \frac{\bar{E}_f - \bar{E}_s}{\bar{E}_f + \bar{E}_s} \text{ and } \beta = \frac{\mu_f(1-2\nu_s) - \mu_s(1-2\nu_f)}{2\mu_f(1-\nu_s) + 2\mu_s(1-\nu_f)} \tag{2}$$

where $\bar{E}_s = E_s/(1-\nu_s^2)$ is the plane strain modulus of the substrate ($E_s$ and $\nu_s$ are the Young's modulus and Poisson's ratio of the substrate), and $\mu_f = E_f/(2+2\nu_f)$ and $\mu_s = E_s/(2+2\nu_s)$ are the shear moduli of the layer and substrate, respectively.

For layers with same properties as their substrate, $\alpha = \beta = 0$. A stiff layer on a soft substrate results in $\alpha \to 1$, whereas a soft layer on a stiff substrate results in $\alpha \to -1$. The function $g$ is primarily dependent on parameter $\alpha$, which is therefore more representative of layer/substrate elastic contrast than parameter $\beta$. For most layer/substrate combinations $0 < \beta < \alpha/4$. The values of these parameters for the two systems considered are reported in Table 1.

### 4.2. Finite element model

A plane strain finite element model was developed based on the work presented in [19] to refine the calculation of function $g$. A special attention was paid to the thin PI substrate case, for which the semi-infinite substrate result ($g_\infty$, [10]) was expected to be inaccurate. Fig. 6 shows the geometry and the boundary conditions of the plane strain problem. The crack and the crack tip are indicated. The substrate has a finite thickness $H$ and is simply supported. The displacements in the $x$-direction were fixed along the left vertical boundary, and were prescribed along the right vertical boundary to account for the applied tensile strain $\varepsilon$ in the fragmentation experiments. Other boundary degrees of freedom were traction free. In this way a periodic set of parallel cracks with spacing $S$ was modeled. In order to arrive at $G_{ss}$ for a single crack on a semi-infinite substrate $S$ and $H$ had to be large enough. The finite element mesh was generated following the strategy outlined in [19]. The elements were concentrated in the crack tip area in such a way that the typical element size near the crack tip was approximately $h/1000$. Thirty elements were used in the vertical direction, both in the $SiO_2$ layer and in a top layer of the substrate of thickness equal to the layer thickness. Thirty elements were also defined in the horizontal direction in two vertical bands with a width equal to the layer thickness and adjacent to the crack faces. In the other regions the mesh was coarser, although still compatible with the densely meshed regions. The elements used were 8-noded quadrilaterals with quadratic interpo-

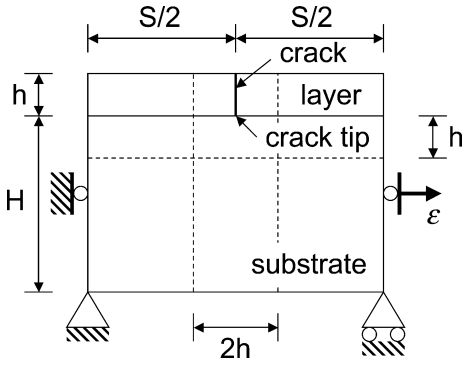


**Fig. 6.** Model geometry and boundary conditions.

lation functions. Near the crack tip the quadrilateral elements were collapsed to triangular elements; no attempt was made to move the mid-side nodes of these elements towards the quarter point position, which could have improved the accuracy of the results.

### 4.3. Model validation

It has been reported in [19] that the $G_{ss}$ values derived using the finite element approach will deviate more from the theoretical values in [10] as the elastic mismatch parameter $\alpha$ approaches 1 (i.e. when the substrate becomes more compliant with respect to the film). This was checked for values of $\alpha$ in the range 0.6–0.9 tabulated in [10], around the highest elastic mismatch value reported in Table 1. In order to model the condition of a single crack in a coating on a semi-infinite substrate, the crack spacing and the substrate thickness were progressively increased. The energy release rate $G_{ss}$ was found to reach an asymptotic value at a crack spacing $S/h$ equal to 500 and a substrate/layer thickness ratio $H/h$ equal to 80. As shown in Table 2, the model values deviate from theoretical values in a range from 0.7% for mismatch value 0.6 to a maximum of 6% for mismatch value 0.9, which was considered to be acceptable for the present application.

### 4.4. Role of elastic contrast on the difference in COS of $SiO_2$ on steel and PI

The steel substrate being much thicker than the $SiO_2$ layer was considered as semi-infinite. In this case the function $g$ was found to be equal to 0.891 (accounting for the finite thickness of the steel substrate gives the same result). In contrast, the very thin PI substrate could not be considered as semi-infinite. Fig. 7 compares simulated deformation states of $SiO_2$/PI and $SiO_2$/steel films with same $SiO_2$ thickness of 1.28 μm and same substrate thickness of 8 μm, in case $S/h = 75$. A significant bending effect is evident for the PI substrate (Fig. 7b) whereas the steel substrate nearly completely prevents bending (Fig. 7c). The function $g$ as a function of crack spacing for the 1.28 μm thick $SiO_2$ layer on 4, 8 and 16 μm thick PI is shown in Fig. 8 together with the value for a single crack on semi-infinite PI substrate, equal to 3.311. The maximum value of $g$ is reached at a crack spacing $S$ equal to 500 $h$, which validates the conditions at the COS (i.e. a single crack). For the 1.28 μm thick $SiO_2$ on 4, 8 and 16 μm thick PI the calculated value of $g$ was 5.882, 4.479 and 3.844, respectively. The measured COS of the $SiO_2$ layer on the 8 μm thick PI is equal to 0.24%. Using Eq. (1) and ignoring residual stresses the corresponding COS value for the same $SiO_2$ layer on a 4 and 16 μm thick PI would be equal to 0.21% and 0.26%, respectively, and would increase to 0.28% on a semi-infinite substrate. Interestingly, the major cause for the deviation from the semi-infinite value in Fig. 8 is the increase in energy release rate due to global bending of the substrate, and not the decrease in substrate thickness. This is shown in Table 3, where the $g$ values at $S/h = 500$ are tabulated for different values of $\alpha$ in case bending is allowed and in case the displacement of the bottom of the substrate is restricted in $y$-direction, and compared to the semi-infinite substrate case.

Assuming that the channeling cracks were fully developed and propagated under steady state conditions, and assuming equal toughness $G_c$ for $SiO_2$ on steel and $SiO_2$ on PI, one obtains using Eq. (1):

$$G_{ss} = \frac{\bar{E}_f \varepsilon_I^2 h_I}{2} \pi g_I = \frac{\bar{E}_f \varepsilon_{II}^2 h_{II}}{2} \pi g_{II} \tag{3}$$

where subscripts $I$ and $II$ refer to steel and PI, respectively, $\varepsilon_I$ is the COS of $SiO_2$ on steel (1.15%) and $\varepsilon_{II}$ is the COS of $SiO_2$ on PI (0.24%). Elaboration and substitution of the values found in the previous sections yields $\left(\frac{\varepsilon_I}{\varepsilon_{II}}\right)^2 = \frac{h_{II} g_{II}}{h_I g_I} = \frac{1.28 \cdot 4.479}{1 \cdot 0.891}$, hence $\varepsilon_I = 2.54 \varepsilon_{II}$. This means that in order to reach the same energy release rate 2.54 times more strain needs to be applied to the $SiO_2$ on steel system than to the $SiO_2$ on PI system.

This 2.54 ratio underestimates the measured COS ratio found to be equal to 4.8. The reason is the presence of different levels of process-induced internal stresses in the two cases, which impact the COS, hence the toughness derived from Eq. (1). The fracture toughness of bulk fused silica tested in inert environment is $K_{Ic} = 0.75$ MPa$\sqrt{}$m, corresponding to $G_c = 8$ J/m$^2$ ($K_{Ic} = (G_c \sqrt{\bar{E}})$). For $SiO_2$ insulator layers tested under non-inert environmental conditions, with composition and density that may deviate from the properties of fused silica, one may expect a slightly lower fracture toughness in the 0.45–0.75 MPa$\sqrt{}$m range, giving $G_c$ values in the 3–8 J/m$^2$ range [20]. For the 1.0 μm thick $SiO_2$ layer on steel with a COS equal to 1.15% and a function $g$ equal to 0.891 one obtains (Eq. (1)) $G_{ss} = 15.2$ J/m$^2$. If the expected compressive thermal strain $\varepsilon_c$ of −0.63% is taken into account, the intrinsic strain to failure of the $SiO_2$ layer (COS + $\varepsilon_c$) becomes equal to 0.52%, resulting in $G_{ss} = 3.2$ J/m$^2$. The presence of other sources of internal strain (process-induced intrinsic strain for instance) will also impact the value of $G_c$. For the 1.28 μm thick $SiO_2$ layer on PI the critical strain was equal to 0.24% and the elastic mismatch

**Table 2**
Comparison of theoretical $g_\infty$ [10] and numerical $g$ values for function $g(\alpha, \beta)$.

| $\alpha$ | $\beta$ | $g_\infty$ | $g$ | $g/g_\infty$ |
|---|---|---|---|---|
| 0.6 | $\alpha/4$ | 2.382 | 2.366 | 0.993 |
| 0.7 | $\alpha/4$ | 2.876 | 2.845 | 0.989 |
| 0.8 | $\alpha/4$ | 3.730 | 3.652 | 0.979 |
| 0.9 | $\alpha/4$ | 5.775 | 5.429 | 0.940 |

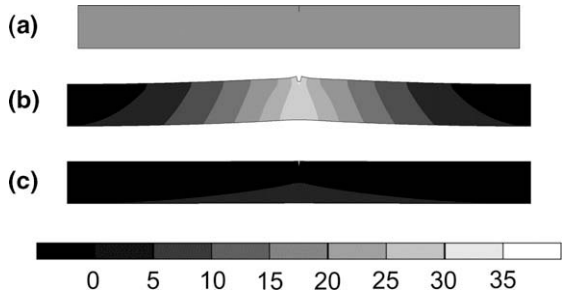


**Fig. 7.** Finite element simulation of 1.28 μm thick $SiO_2$ layers on 8 μm thick substrates at $S/h = 75$. The images show the unstrained film (a) and the PI (b) and steel (c) based films strained to 0.001. The grey levels indicate the out-of plane deformation in nm. The deformation is scaled by a factor of 50 in the images.

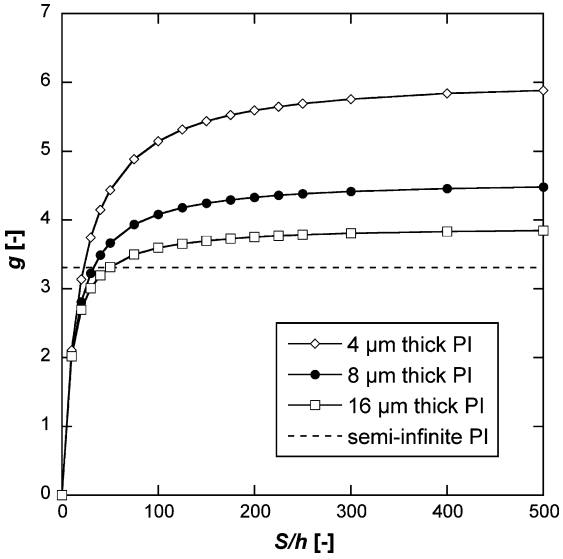


**Fig. 8.** Function $g$ vs. crack spacing for a 1.28 μm thick $SiO_2$ layer on various PI thicknesses.

**Table 3**
Values of function $g$ for 1.28 μm thick $SiO_2$ on 4, 8 and 16 μm thick PI at a crack spacing $S/h = 500$, for $\alpha$ equal to 0.6, 0.765 and 0.9, with the ratio $\alpha/\beta$ equivalent to the $SiO_2$ on PI system (Table 1) and for various boundary conditions for the PI substrate.

| PI substrate thickness (μm) | Boundary condition | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | $\alpha = 0.6$ | | | $\alpha = 0.765$ | | | $\alpha = 0.9$ | | |
| | Free bending | Fixed $y$-direction | Semi-infinite | Free bending | Fixed $y$-direction | Semi-infinite | Free bending | Fixed $y$-direction | Semi-infinite |
| 4 | 3.950 | 2.401 | 2.371 | 5.882 | 3.451 | 3.311 | 9.952 | 5.834 | 5.412 |
| 8 | 3.029 | 2.368 | | 4.479 | 3.362 | | 7.630 | 5.676 | |
| 16 | 2.636 | 2.363 | | 3.844 | 3.319 | | 6.575 | 5.531 | |

function $g = 4.479$, resulting in $G_{ss} = 4.3$ J/m$^2$. The $G_{ss}$ values derived here (3–5 J/m$^2$) agree well with fracture toughness data for bulk fused silica. Also for the $SiO_2$ layer on PI, the internal strain resulting from e.g. hygroscopic and shrinkage phenomena of the PI substrate will influence the COS, hence the actual $G_{ss}$ value. This will anyway be attenuated since the tensile stiffness ratio $\bar{E}_f h/\bar{E}_s H$ between the $SiO_2$ layer and the thin PI substrate is higher than 1 (equal to 1.2), which implies that $SiO_2$ carries the main part of the load.

### 4.5. Influence of layer/substrate thickness ratio on elastic contrast

In order to further evaluate the influence of geometry variations of the two-layer system (e.g. changes in $SiO_2$ layer or in substrate thickness) the function $g$ was calculated as a function of the ratio $\bar{E}_f h/\bar{E}_s H$, where $\bar{E}_f$ and $\bar{E}_s$ represent the plane

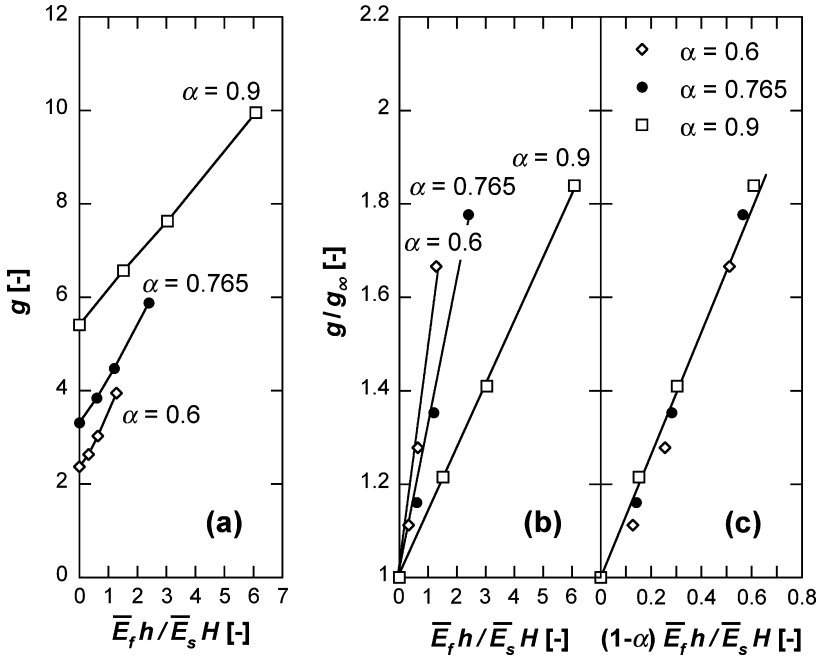


**Fig. 9.** Function $g$ vs. layer/substrate stiffness ratio $\bar{E}_f h/\bar{E}_s H$ for three values of $\alpha$ (a), normalized function $g/g_\infty$ vs. scaling factors $\bar{E}_f h/\bar{E}_s H$ (b) and $(1-\alpha)\bar{E}_f h/\bar{E}_s H$ (c).

strain Young's modulus of $SiO_2$ and PI. This ratio represents the load carrying contribution (or tensile stiffness) of the $SiO_2$ layer with respect to the substrate. The result is shown in Fig. 9a for $\alpha$ equal to 0.6, 0.765 and 0.9, with the ratio $\alpha/\beta$ equivalent to the $SiO_2$ on PI system (3.725). In all cases a quasi-linear relation is evident (the influence of the accuracy of the FEM analysis on the small departure from linearity was not checked). This finding suggests that there may exist a scaling behavior, which would permit the estimation of $g$ for any combination of layer and substrate stiffness and thickness, at least for positive $\alpha$ values. Such a derivation is beyond the scope of the present work. Nevertheless, an attempt towards such scaling is depicted in Fig. 9b where the $g$ data from Fig. 9a was normalized with the values $g_\infty$ for semi-infinite substrates and plotted against $\bar{E}_f h/\bar{E}_s H$. The slopes of the linear fits for each data set seem to scale approximately with a factor $(1-\alpha)$, which is reproduced in Fig. 9c where the scaling factor is $(1-\alpha)\ \bar{E}_f h/\bar{E}_s H$. A reasonable correlation is obtained, although the physical basis why this should work is lacking, particularly since the scaling parameter is based on plane-strain tensile stiffness and the deformation mode also includes bending effects. However, the empirical correlation depicted in Fig. 9c may be used in the range $0.6 < \alpha < 0.9$, which already represents a rather broad variety of thin films on polymer substrate combinations.

## 5. Conclusions

The mechanical integrity of 4-level TFT structures on both steel and PI substrates loaded under uniaxial strain was investigated. In the case of steel, cracks initiated at 1.15 ± 0.05% strain in the $SiO_2$ insulator. In the case of thin PI, cracks initiated at 0.24 ± 0.04% strain within the $SiO_2$ insulator layer. For both substrates, it was moreover observed that narrow TFT gates are less susceptible to cracking, when loaded parallel to the gate length direction, a consequence of stress transfer properties in the layered structure. The practical consequence of these results is in terms of backplane design: devices of anisotropic geometry should be preferably oriented with longest dimension parallel to the bending axis, and their shortest dimension should be smaller than approximately 15 μm. The large difference in critical strain for the $SiO_2$ layer on the two types of substrates was analyzed using an energy release rate approach. The value for $G_{ss}$ of the $SiO_2$ layer obtained in the present analysis agrees well with data for bulk $SiO_2$. Attention was paid to the influence of the finite substrate thickness, especially in the case of the 8 μm thick PI. The difference in critical strain between the two types of substrates was found to result mainly from the differences in layer/substrate mechanical contrast. Additional factors, such as differences in residual stress, also contribute to the difference in critical strain. Based on this analysis an attempt towards a master curve to relate elastic contrast to finite layer/substrate tensile stiffness ratio was proposed. The resulting empirical correlation lacks physical grounds but should be useful for practical purposes in case of thin and stiff films on thin compliant substrates.

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