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Gallium assisted plasma enhanced chemical vapor deposition of silicon nanowires

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Abstract
Silicon nanowires have been grown with gallium as catalyst by plasma enhanced chemical vapor deposition. The morphology and crystalline structure has been studied by electron microscopy and Raman spectroscopy as a function of growth temperature and catalyst thickness. We observe that the crystalline quality of the wires increases with the temperature at which they have been synthesized. The crystalline growth direction has been found to vary between ⟨111⟩ and ⟨112⟩, depending on both the growth temperature and catalyst thickness. Gallium has been found at the end of the nanowires, as expected from the vapor–liquid–solid growth mechanism. These results represent good progress towards finding alternative catalysts to gold for the synthesis of nanowires.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

One-dimensional nanostructures have attracted significant attention in the last few years, due to their potential in exhibiting new physical and chemical properties that could lead to novel devices in electronics, chemistry and biomedical applications [1–7]. In this context, nanowires are considered a model system for the study of one-dimensional structures. Silicon nanowires are especially interesting as they hold the promise of further electronics miniaturization [8, 9]. It has been shown that nanometer sized silicon can crystallize in structures different from the bulk diamond one, with effects on electronic properties [10–12]. Moreover silicon nanowires with very small diameters are expected to have a direct band gap [13], which could transform silicon in an efficient optical emitter.

Effective control over the diameter, position, crystalline phase and orientation as well as surface properties is necessary for enabling nanowire applications. Catalyst assisted growth of nanowires through the vapor–liquid–solid mechanism (VLS) has given the possibility to control the size and position of nanowires [14–17]. In the VLS process, the silicon impinges on the substrate in the form of a precursor gas, in our case silane. The gas is decomposed at the surface of the catalyst droplet, with which it forms an eutectic liquid alloy. Finally, reaching a saturation concentration, the silicon precipitates into a solid state silicon nanowire at the interface between the metal droplet and the substrate. Successful growth of nanowires through VLS has depended on the use of gold as catalyst [18–22]. Gold is, however, a deep level impurity in silicon that introduces electronic states almost in the middle of the band gap and degrades the carrier mobility [23, 24].

As a consequence, it is expected that the use of an alternative less polluting catalyst would improve the optical and electronic properties of the nanowires. To date, very few results have been obtained with other metals, due to the major difficulties in the efficiency of the catalyst activation in comparison with gold [25–28]. From this point of view, gallium is an interesting metal catalyst because of its low melting point (29.8 °C), which is at the same time the eutectic temperature for the binary system with silicon. This enables, in principle, the synthesis of silicon nanowires at very low temperatures and for the fabrication of nanowire arrays on plastic substrates. Additionally, due to the low solubility of gallium in silicon, it is not expected that its incorporation will reduce significantly the carrier mobility of silicon[7]. Gallium is a p dopant in silicon that creates an acceptor level 27 meV above the valence band edge [29, 30]. There is the possibility that gallium is incorporated in the silicon matrix in a substitutional site during growth. This would result in p-type doping of the nanowires. In order to determine the doping concentration, electronic transport measurements should be realized. Preliminary studies corroborate the potential of gallium as a catalyst for the synthesis of silicon nanowires [26, 27, 31, 32]. As an example, extensive carpets of nanowires have been realized by exposing a gallium coated silicon wafer to high power hydrogen plasma [31]. Silicon nanowires were also fabricated by a hydrogen radical assisted method [32]. These were precursor studies that highlighted the possibility of using gallium as a catalyst. However, to our knowledge a systematic study of the growth parameters and of the role played by the hydrogen radicals in enabling the synthesis of nanowires is still lacking. Moreover, the use of standard growth techniques for the industry, such as plasma enhanced chemical vapor deposition, has to date not been demonstrated yet.

In this work we use gallium as catalyst for the growth of silicon nanowires and study their morphology and their properties as a function of the growth parameters. We also point out the necessity of using hydrogen rich plasma for the growth of nanowires. The results constitute a step forward towards the synthesis of silicon nanowires with alternative catalysts.

2. Experimental details

Silicon nanowires were grown by plasma enhanced chemical vapor deposition (PECVD). The used PECVD system is a cold wall reactor in vertical layout with the process gases entering through the upper electrode. It consists of an evacuated stainless steel vessel holding two heated electrodes for plasma generation. The bottom electrode functions also as the sample holder. The process gases available are silane and hydrogen, controlled by two mass flow controllers, and the pressure during deposition can be regulated by a butterfly valve between the reactor chamber and the vacuum pumping system. The mass flow controllers had a maximum flow capacity of 10 and 200 sccm, respectively.

[7] The incorporation of dopants in the matrix of a semiconductor reduces the mobility only at high concentrations, e.g. $>1 \times 10^{18}$ cm^{-3}. See, for example, reference [29] for a detailed explanation.

For the nucleation and growth of the silicon nanowires, gallium was investigated as catalyst. Gallium layers with a thickness of 2 and 5 nm were deposited in an ultra-high vacuum (UHV) molecular beam epitaxy (MBE) chamber on epiready (001) oriented GaAs wafers. The deposition rate had been calibrated prior to deposition with RHEED (reflection high energy electron diffraction). The samples were then transferred in our PECVD chamber for the growth process. Once a vacuum of 5×10^{-6} mbar had been achieved, hydrogen was introduced in the chamber and the temperature of the substrate was increased to the growth temperature. The hydrogen pressure and flow were respectively 1 Torr and 100 sccm. Once the growth temperature was achieved, the substrate was exposed for 5 min to a 5 W hydrogen plasma. The purpose of this plasma was to clean the surface of the substrate from contamination and reduce the possible gallium oxide on the gallium surface. Then, without interrupting the plasma, 1 sccm of silane was introduced in the chamber. The measured silane partial pressure was $0.022\,50 \pm 0.0025$ Torr. The growth temperature ranged between 500 and 600 °C.

The morphology of the surface of the samples prior to growth was characterized by atomic force microscopy (AFM). The morphology and the structure of the grown nanowires were investigated by transmission electron microscopy (TEM), scanning electron microscopy (SEM) and scanning transmission electron microscopy (STEM) in high angular annular dark field (HAADF) or Z-contrast mode. To complement the structural information, Raman spectroscopy was performed at room temperature, using a microscope objective (50×) in backscattering geometry. The excitation wavelength was the 514.5 nm line of an Ar^+ laser. Special care was used to ensure that the nanowires were not heated by the laser. We realized an excitation power series and determined that in our experimental set up heating occurred for excitation powers larger than 2 mW. The calibrated incident power on the sample was always 0.5 mW, corresponding to a laser power density of 58 kW cm^{-2}. The scattered light was collected by an XY Raman dilor triple spectrometer with a multichannel charge coupled device detector. The localized chemical analysis at the nanoscale was obtained by means of electron energy loss spectroscopy (EELS).

3. Results and discussion

3.1. Nucleation

Before studying the growth mechanisms, the nucleation of the nanowires was studied. First, the surface morphology of the substrates after annealing and prior to growth was investigated. Gallium thin films with a thickness of 2 and 5 nm received the typical annealing treatment prior to nanowire growth. First, they were brought up to a temperature of 600 °C under a hydrogen atmosphere (1 Torr). Then a 5 min cleaning plasma was applied. AFM measurements of both samples after the treatment are shown in figure 1. About 10 AFM measurements were realized in order to extract the average droplet diameter and dispersion. We found that the droplet size distribution of the 5 nm Ga layer was monodispersed and centered at 19.3 ± 1.1 nm. In the case of 2 nm Ga the size distribution

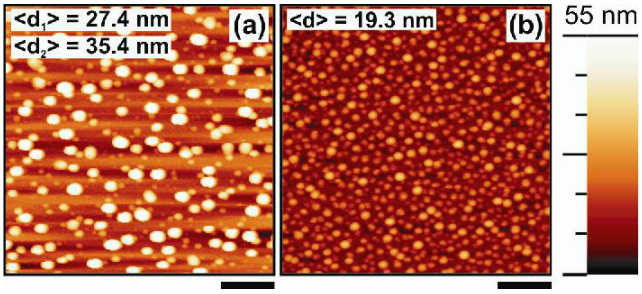

Figure 1. Typical AFM images ($1 \times 1\ \mu m^2$) of the surface of the samples after the annealing process, carried out at 600 °C in hydrogen plasma: (a) Ga of 2 nm nominal thickness and (b) 5 nm nominal thickness (on the right) on GaAs substrate. Scale bars are 200 nm.

presents two maxima at 27.4 ± 7.4 nm and 35.4 ± 10.9 nm. It is interesting to note that the Ga droplets do not seem to agglomerate to form larger droplets, as is observed with other metals like gold [33]. We believe the formation of smaller droplets might be due to the lower interface energy between Ga and GaAs. This should maximize the interface total area, to the detriment of the droplet surface area.

After annealing, the introduction of silane in the plasma always leads to the formation of gallium catalyzed silicon nanowires. The nucleation of nanowires derives directly from the formation of gallium droplets on the surface, as presented above. In order to monitor the initial growth of the nanowires, a series of growth runs was realized, increasing the growth time from 5 min up to 45 min. The SEM measurements of the samples grown in these intervals are shown in figure 2.

As shown in figure 2(a), the nucleation of nanowires has already started after 5 min of growth. The nanowires have similar lengths, indicating a uniform incubation time and growth rate. We also observe that the nanowires grow along certain preferential directions with respect to the underlying substrate. In this case, the growth direction coincides with the (111) directions of the underlying GaAs substrate. As the growth time is increased from 5 to 45 min, nanowires stay in their original orientations and just increase in length. The diameter at the top of some of the wires seems also to be reduced with the growth time, leading to slightly conical wires. We estimate that the growth rate is 14.5 nm min^{-1}. The diameter of the nanowires ranges between 20 and 40 nm, and depends linearly on the temperature. The diameter of the nanowires corresponds well with the diameter of the gallium droplets after annealing. We conclude therefore that the coarsening of gallium during growth is not significant, as is otherwise observed with other metals such as gold.

3.2. Temperature dependence

The effect of the growth temperature on the morphology of the silicon nanowires was studied. The growth runs were realized at 500, 550 and 600 °C. SEM measurements of the nanowires obtained after a 45 min growth are shown in figure 3. For these samples, a 5 nm layer of Ga was used as catalyst. We observe again that the nanowires tend to grow aligned with the crystalline orientations of the GaAs substrate. The degree of orientation increases with temperature. Indeed, at 600 °C, the nanowires form a very clear pattern on the substrate, while at 500 °C the orientations of the nanowires differ by some degrees from the ones at higher temperature, resulting in an increase of the disorder. By realizing cross-section SEM measurements, we determined the growth direction of the nanowires with respect to the substrate. We found that nanowires grow at

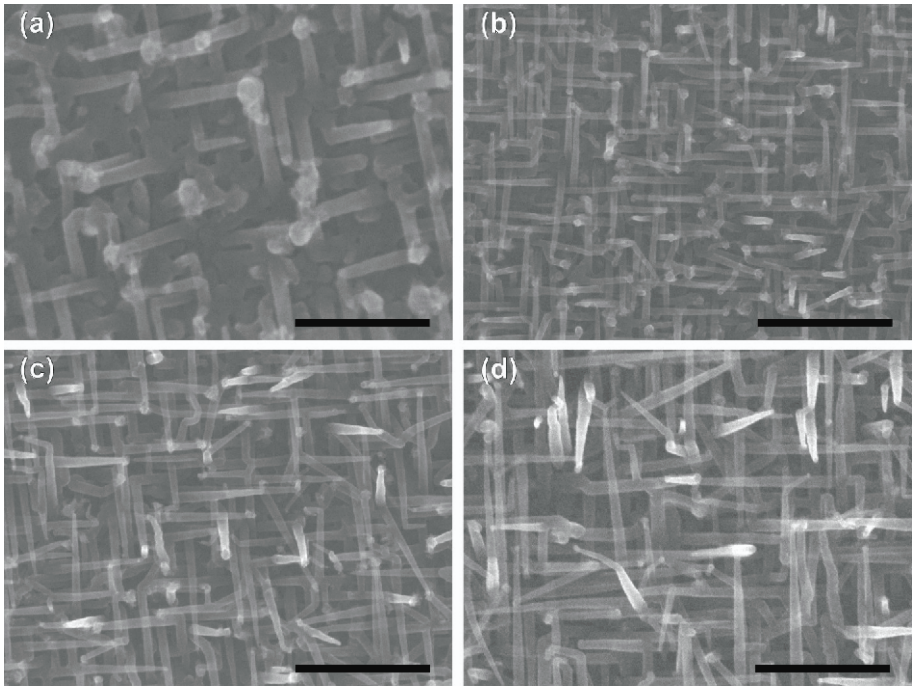

Figure 2. Top view SEM pictures of Ga catalyzed silicon nanowires grown at 600 °C for 5 min. (a), 15 min (b), 30 min (c) and 45 min (d). 5 nm of gallium were deposited on GaAs ⟨001⟩ substrate. Scale bars: (a) 200 nm; (b), (c) and (d) 500 nm.

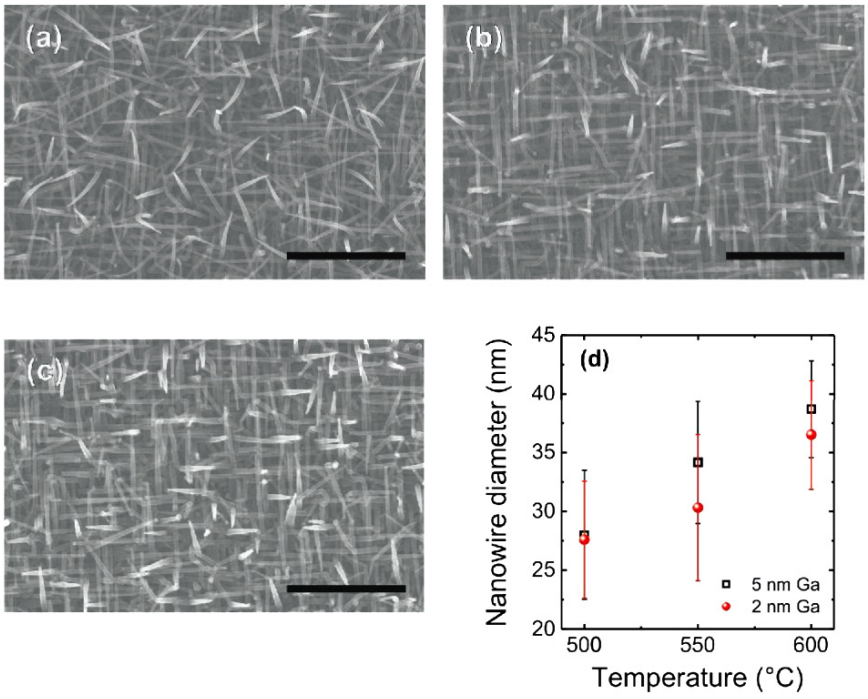

Figure 3. SEM measurements of gallium catalyzed silicon nanowires grown for 45 min at 500 °C (a), 550 °C (b) and 600 °C (c). The thickness of the gallium layer is 5 nm. Scale bars: 1μm. (d) The nanowire average diameter as a function of the synthesis temperature, the error bars represent the diameter dispersion as measured by SEM.

an angle of 35° and 20°–25° with respect to the surface. This would correspond to the directions ⟨111⟩ and ⟨112⟩ respectively. As will be shown in the following, the occurrence of each direction depends on the growth temperature.

From the SEM measurements we deduced the nanowire average diameter and dispersion as a function of temperature. The nanowire diameter tends to increase with the temperature, from 27 to ∼35 nm. The dispersion always stays below 5 nm. The slight increase in nanowire diameter may be attributed to a larger gallium surface mobility with the temperature, which should enhance the ripening of the droplets.

TEM analyses were performed to clarify the growth direction of the nanowires, as well as their crystalline structure. In particular, we were interested in understanding whether there was a heteroepitaxy relation between the nanowires' growth direction and the crystalline structure of the substrate. In good correspondence to what was observed in cross-sectional SEM measurements, we have observed that the crystalline growth direction of the nanowires depends on the temperature. For a fair comparison, we present the results on nanowires with the same diameter. The preferential growth direction of silicon nanowires grown at 600 °C was ⟨111⟩, while at 500 °C ⟨112⟩ was mostly observed. At 550 °C, a mixture of the two directions could be found. High resolution TEM measurements of nanowires obtained at 600 and 500 °C are shown in figure 4. The nanowires obtained at 600 °C present a cubic structure with the growth axis parallel to the $[1\bar{1}1]$ direction. Rotational twins perpendicular to the growth axis on the $(1\bar{1}1)$ planes are observed. Interestingly, twinning is also observed for the lateral {111} planes such as the $(\bar{1}\bar{1}1)$ and $(1\bar{1}\bar{1})$. Here we would like to add that the change in the growth direction cannot be explained by the decreasing size of the nanowires, since there is no significant change in the diameter of the nanowires which present a $\langle 1\bar{1}1\rangle$ growth direction from those presenting a ⟨112⟩ growth direction.

3.3. Effect of the catalyst thickness

Nanowires were also grown with a thinner gallium layer, namely 2 nm. Strikingly, we observed that the nanowires exhibited a much lower degree of orientation with respect to the substrate. SEM measurements on the grown samples are shown in figure 5. These nanowires were also investigated by HRTEM. For each growth condition at least ten nanowires were analyzed in order to have representative statistical information. We found that nanowires grown at 600 °C from 2 nm of gallium exhibit mainly the ⟨112⟩ growth direction, although some of them have been found also growing along the $\langle 1\bar{1}0\rangle$ axis.

As shown in figure 6 we even found that nanowires can change the growth direction during growth from [110] to [112]. The origin of this change in growth direction still remains unclear, but we suspect that both growth directions have a similar stability and therefore the silicon nanowire can oscillate between each other during growth.

HRTEM measurements on a large number of nanowires allowed us to observe the presence of twin defects in non-typical directions, as shown in figure 4. In particular for these samples, three different twin families have been detected, namely occurring along $(11\bar{1})$, $(\bar{1}11)$ and (111) planes.

A twin on a ⟨111⟩ plane itself can be considered as an Si IV (hexagonal) monolayer. The existence of such twins and

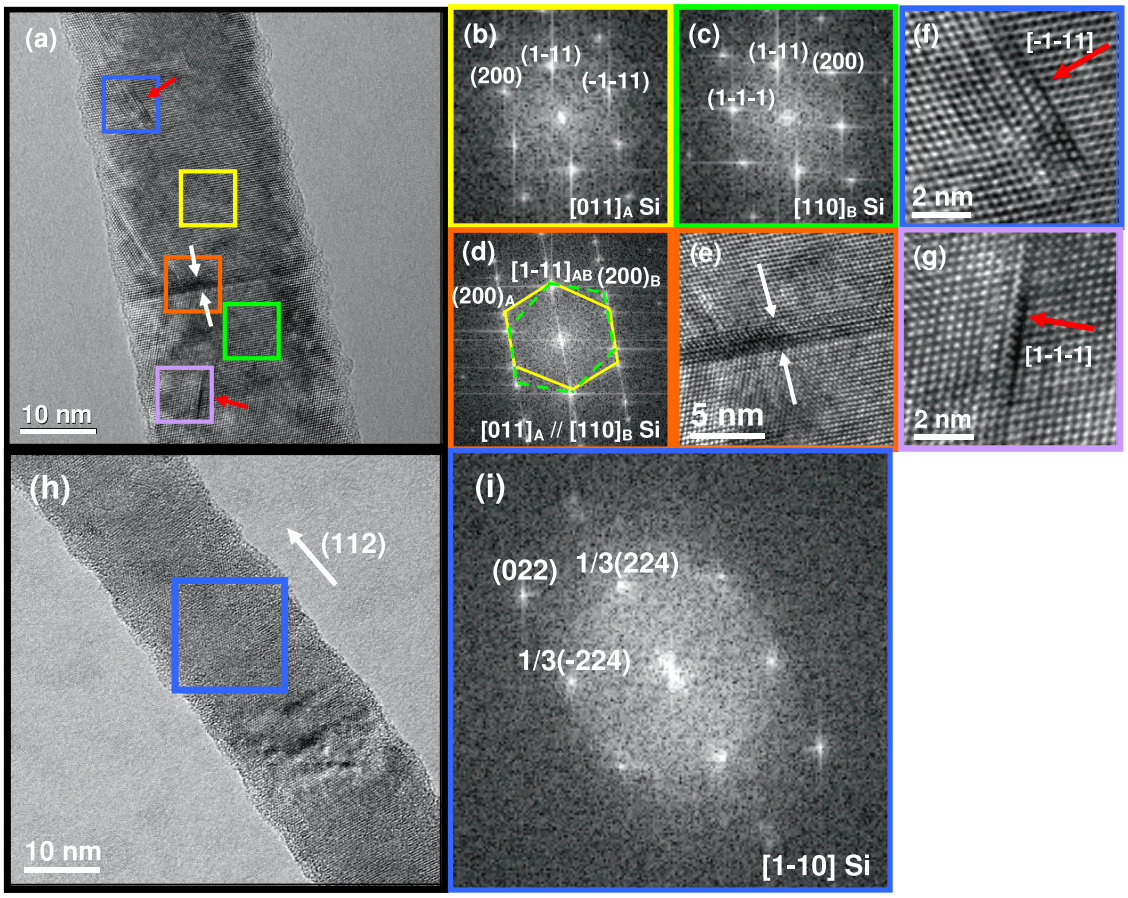

Figure 4. The image (a) corresponds to the HRTEM image of the NW grown at 600 °C from 5 nm of gallium on GaAs substrate. The set of images on the right (b)–(d) corresponds to the power spectra (fast Fourier transform, FFT) of the different squared regions with the corresponding colors in the HRTEM image in (a). The NW grows along the [1$\bar{1}$1] direction, and presents twin segments along the growth direction, as shown in the image (e). In addition, several regions of the NW also present twins and stacking faults along the [$\bar{1}\bar{1}$1] and [1$\bar{1}\bar{1}$] directions, as shown in images (f) and (g). The image (h) shows a NW grown at 500 °C from 5 nm of gallium on GaAs substrate along the [112] direction and (i) the power spectrum of the region squared in (h) confirming the crystallographic orientation.

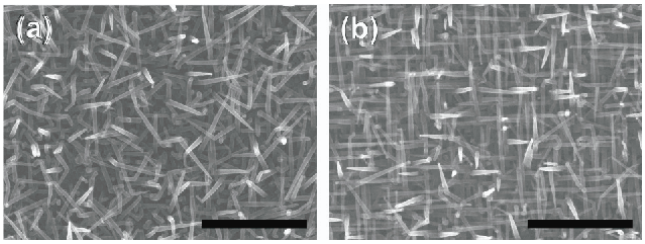

Figure 5. Top view SEM images of silicon nanowires grown using gallium as catalyst. The thickness of the gallium layer is 2 nm (a) and 5 nm (b) and both the samples were grown at 600 °C for 45 min. Scale bars: 1 μm.

even more extended hexagonal regions has been observed in previous works on ⟨111⟩ twinning on Si NWs grown by using Cu as catalyst as well as in III–V nanowires [11, 12, 34]. The existence of highly periodical and twinned regions leads to the formation of a local hexagonal structure. The synthesis of silicon nanowires in wurtzite crystalline structure by this mechanism has already been demonstrated [35–37]. A complete HRTEM analysis and three-dimensional (3D) atomic models of the twin defects and local hexagonal areas observed in the present samples will be published elsewhere.

The samples were also investigated by Raman spectroscopy, which is a powerful and nondestructive tool for the structural study of nanowires. Nanowire bundles were investigated. Measurements realized on nanowires grown at 500, 550 and 600 °C from 5 and 2 nm gallium layers are shown in figure 7. All the Raman spectra present a narrow silicon peak, with a full width at half-maximum (FWHM) of about 7 at 518 cm^{-1}, indicating the high crystal quality of the nanowires. The position and FWHM of the peak are also in good agreement with the theoretical ones already calculated in the literature [38]. The shift to lower wavenumbers can be due to the existence of stress or to the small size of the nanowires. The shift cannot be attributed to other effects such as heating, as heating effects such as a shift towards lower wavenumbers and asymmetric broadening appeared for an excitation power of 2 mW. Interestingly, a weak peak at 495 cm^{-1} is observed in some of the samples.

The 495 cm^{-1} feature is totally missing in the spectrum collected from the sample grown at 600 °C, while it increases for lower growth temperatures and it is present even in the

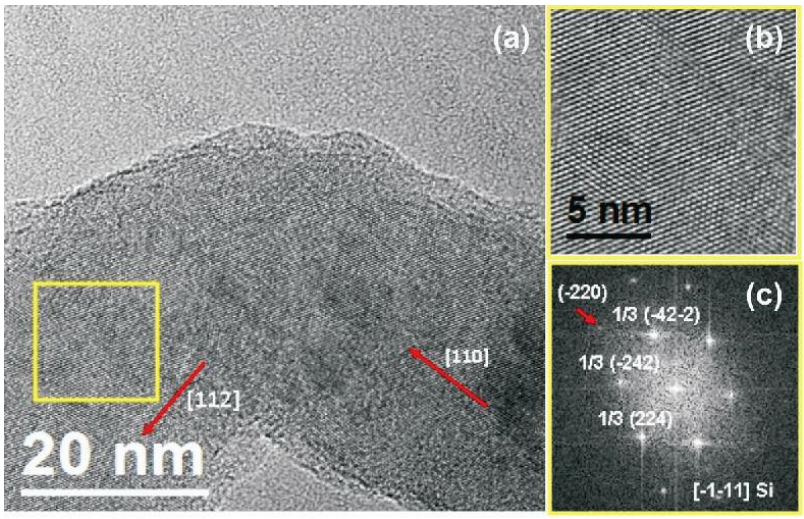

Figure 6. (a) TEM measurement of a nanowire grown at 600 °C from 2 nm of gallium on GaAs substrate. The nanowire kinks, changing growth direction from ⟨110⟩ to ⟨112⟩. The images (b) and (c) correspond to the magnification and to the power spectra (FFT) of the yellow squared region in (a).

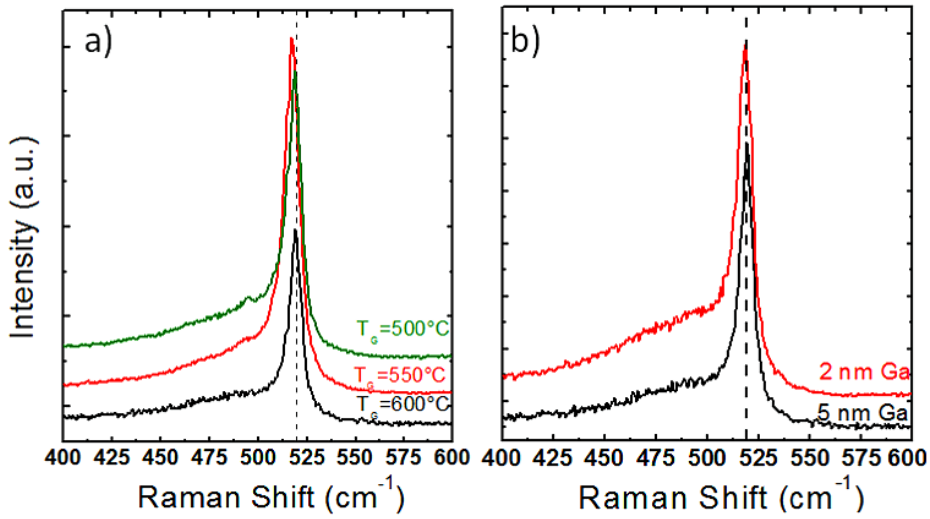

Figure 7. (a) Raman spectra of gallium catalyzed nanowires grown at different temperatures from a 5 nm Ga layer. (b) Raman spectra of 5 nm thick gallium catalyzed (black) and 2 nm thick gallium catalyzed (red) nanowires grown for 45 min at 600 °C.

sample with just 2 nm of gallium. We suggest that the appearance of this feature in the Raman spectra can be related to the presence of the periodically twinned regions in the cubic silicon I structure. In the sample grown at 550 °C (red one in figure 7(a)) a peak at 495 cm^{-1} arises and becomes more pronounced in the sample grown at 500 °C. A similar effect has already been observed and reported in the literature, even if in that case the peak corresponding to the Si–IV structure was at 506 cm^{-1} [36, 39]. The shift in the present work could be explained considering that these nanowires do not have pure Si–IV structure but just 'wurtzite nanodomains'.

3.4. Gallium segregation

We have analyzed the gallium content of the silicon nanowires by EELS. Typically, gallium is only found at the tip of the nanowire. However, in some rare cases, gallium segregation along the axis is observed. The EELS mapping of such a silicon nanowire grown at 550 °C is shown in figure 8. In figures 8(a) and (b) the scan line on a HAADF STEM micrograph and the spectral mapping are shown. Clearly, the gallium peak is present in discrete points of the nanowire surface (marked with red arrows on the HAADF micrograph and the spectrum image). We believe this diffusion or loss of gallium content on the catalyst seed occurs during growth. Indeed, we observe a pronounced tapering in the wires that present the gallium wetted surface. The loss of gallium during growth reduces the size of the catalyst at the tip of the nanowire, which at the same time has consequences by reducing the diameter of the nanowire. In some cases, the new gallium droplets formed on the facets give rise to the beginning of ramification on the wires (figure 9). This can be observed in the TEM micrographs of figure 9.

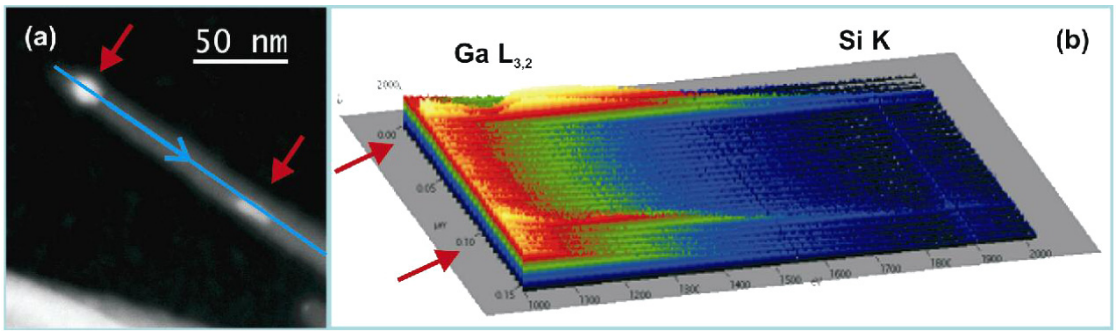

Figure 8. (a) HAADF image of an Si NW. (b) EEL spectra obtained in the NW along the line indicated in (a), which demonstrate the presence of gallium segregation along the nanowire.

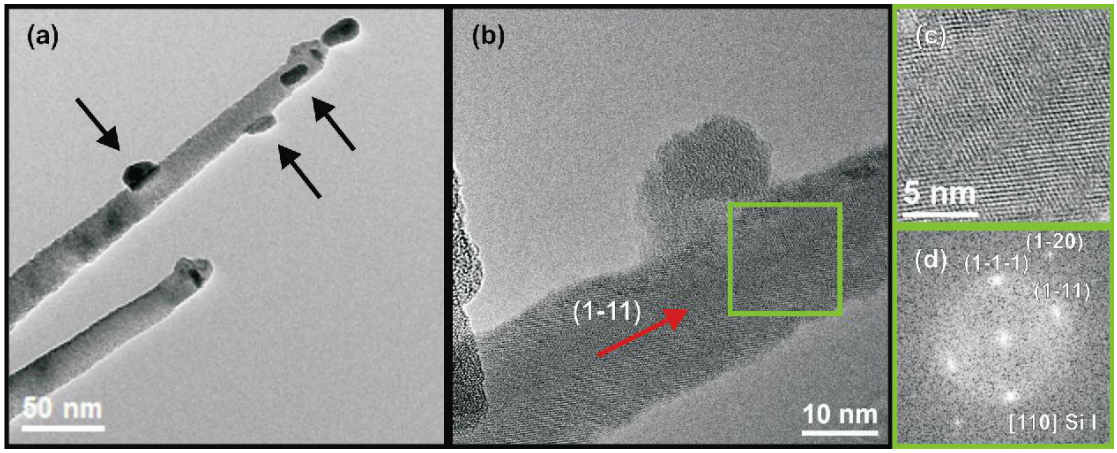

Figure 9. (a) TEM image of Si NWs grown at 550 °C from 5 nm of gallium; in some of them the catalyst seed diffuses along the nanowire, as indicated by the black arrows. (b) HRTEM image of a nanowire with cubic structure, grown along the $[1\bar{1}1]$ axis, with a ramification. (c) Detail from the squared region in (b) and (d) power spectrum and crystallographic analysis from the same region. We do not observe this gallium segregation in all nanowires grown under the same conditions. The reason still remains unclear and will be investigated in the future.

4. Discussion

The results presented above indicate that gallium can be used as a catalyst for the reproducible synthesis of large density silicon nanowire arrays. In order to determine the advantage of using hydrogen rich plasmas for the VLS growth, the following experiment was realized. First, we annealed the substrate under hydrogen pressure of 35 mTorr at a temperature of 640 °C. The morphology of the substrate can be observed in figure 10(a). The surface appears to be quite different, as no gallium droplets are observed. Annealing under these conditions does not seem to induce any morphological change. Then, we compared the growth of nanowires for substrates that had been submitted to hydrogen plasma annealing as described above. In one case (figure 10(b)) the plasma was interrupted for 10 min between annealing and growth, while for the second case the plasma was not interrupted (figure 10(c)). Very short nanowires are observed in the case where the plasma was interrupted. We attribute this to the reoxidation of the gallium particles during the pause of the plasma. As can be seen, the hydrogen rich plasma can reduce the gallium oxide again for a restart of the nanowire growth. We believe that the atomic hydrogen flux towards the surface will have an influence on the oxidation degree of the gallium. In this sense, by decreasing the flux one would be able to tune the efficiency of the gallium as a catalyst for the nanowire growth.

The benefit of using a plasma process for the synthesis is justified as follows. During annealing the hydrogen plasma produces hydrogen radicals (H^*) that reduce the gallium oxide of the surface droplet. This reduction activates the catalyst function of the gallium, as previously shown for indium tin oxide [40]. For the synthesis, a silane plasma highly diluted in hydrogen was used. In this kind of plasma, there is a large concentration of H^* and SiH_x^* radicals and ions. In this paper we deliberately chose plasma conditions with minimal ion bombardment to avoid damaging the silicon [41]. During deposition, the H radicals ensure that the surface of the gallium droplets does not oxidize despite using a standard PECVD system (not ultra-high-vacuum). The SiH_x^* radicals dissolve in the gallium droplet and contribute to the nanowire growth. For more clarity, this growth mechanism is schematized in figure 11.

The role of gallium as catalyst is further elucidated if one considers the growth rate of the nanowires in comparison to the growth rate of the film—obtained when no gallium is deposited on the substrate. It is known that high hydrogen

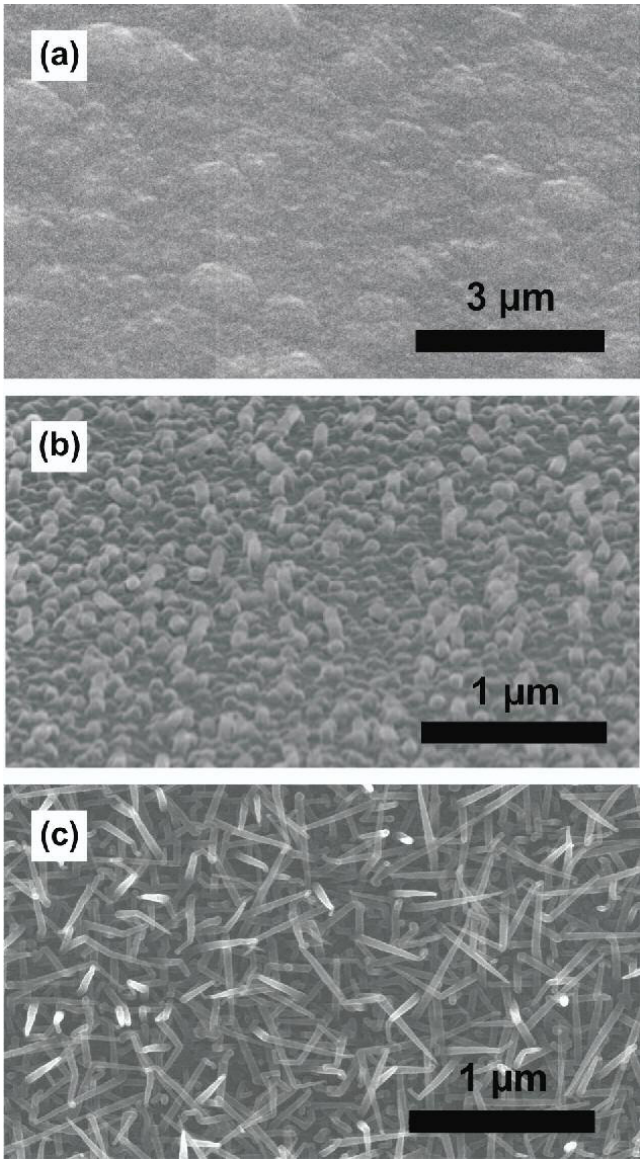

Figure 10. Effect of a hydrogen plasma on the growth of silicon nanowires with gallium as a catalyst: (a) SEM of 2 nm gallium annealed under H_2 pressure of 35 mTorr and 640 °C without a plasma, the surface is rough and no gallium nanodroplets are observed, differently from when plasma is used, as shown in figure 1(a); (b) and (c) nanowires obtained after 45 min of growth at 600 °C by introducing silane in the plasma. In (b) the plasma was stopped for 10 min, while in (c) there was no interruption between plasma annealing and growth.

diluted silane plasmas lead to the formation of microcrystalline silicon or thin films with nanocrystalline inclusions [42, 43]. Thin film grown under the plasma conditions used in this paper would lead to a growth rate of 1.3 nm min^{-1}. We have seen that the growth rate of the nanowires is of the order of 12 nm min^{-1}. This nine-fold increase in growth rate of nanowires with respect to planar growth is a common denominator of the VLS growth mechanism [44]. We can state here that clearly the non-oxidized gallium catalyst droplet acts as a catalyst by preferentially gathering and decomposing the SiH_x^* radicals.

An issue still to be solved is the understanding of the difference in growth directions. In the past, it has been shown that the growth direction of the nanowires depends on the diameter. For larger diameters (the critical diameter is 40 nm experimentally and 20 nm from theory) ⟨111⟩ is preferred, while for smaller diameters ⟨110⟩ and ⟨112⟩ are equally probable [45, 46]. To date, no satisfactory explanation of this correspondence has been given. A similar dependence of the growth direction with temperature has been observed in ZnSe nanowires grown on a GaAs substrate. In that case, it is the liquid–solid interface structure at the catalytic tip of the nanowires which controls the transition of the nanowire growth direction [47]. We plan to study the occurrence of growth directions and the synthesis conditions by exploring in more detail the interface between the nanowire and the catalyst droplet. We also intend to study the diameter dependence as a function of temperature in more detail, as well as the nucleation mechanisms.

5. Conclusion

Silicon nanowires were synthesized by plasma enhanced chemical vapor deposition by using gallium as a catalyst. The use of plasma prevents the oxidation of gallium during growth, thereby maintaining its role as a catalyst. The best crystalline quality of the nanowires was obtained for 600 °C. Transversal dislocations in the {111} planes were obtained, especially for the nanowires fabricated at the lowest temperature (500 °C). The growth direction of the nanowires was shown to be temperature and gallium thickness dependent. Gallium was detected at the end of the nanowires, thereby confirming its role in the nanowire growth. It was also found that gallium

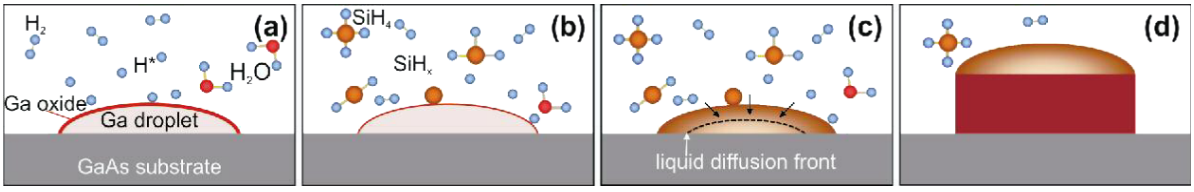

Figure 11. Schematic representation of the VLS growth mechanism of silicon nanowires in the presence of plasma. The H atoms are depicted by the smaller blue spheres, while the sSi atoms are the bigger brown ones. (a) During the annealing phase hydrogen radicals H* can reduce the oxide on the surface of the droplet, with the consequent formation of H_2O molecules; (b) when the silane is introduced, the plasma will induce the formation of SiH_x ions, which are more easily decomposed at the surface of the gallium catalyst droplet; (c) the silicon atoms can diffuse into the droplet, forming the eutectic alloy until the concentration of supersaturation is reached, and (d) the silicon can precipitate and the growth of the nanowires occurs at the interface between the droplet and the substrate.

tends to migrate along the nanowire facets, which can result in the nucleation of new nanowires.

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References

[1] De Franceschi S, van Dam J A, Bakkers E P A M, Feiner L F, Gurevich L and Kouwenhoven L P 2003 *Appl. Phys. Lett.* **83** 344
[2] Lu W, Xiang J, Timko B P, Wu Y and Lieber C M 2005 *Proc. Natl Acad. Sci.* **102** 10046
[3] Mårtensson T, Svensson C P T, Wacaser B A, Larsson M W, Seifert W, Deppert K, Gustafsson A, Wallenberg L R and Samuelson L 2004 *Nano Lett.* **4** 1987
[4] Thelander C, Nilsson H A, Jensen L E and Samuelson L 2005 *Nano Lett.* **5** 635
[5] Klauk H 2008 *Nature* **451** 533
[6] Wang X, Song J, Liu J and Wang Z L 2007 *Science* **316** 102
[7] Fontcuberta i Morral A, Arbiol J, Prades J D, Cirera A and Morante J R 2007 *Small* **19** 1347
[8] Schmidt V, Riel H, Senz S, Karg S, Riess W and Goesle U 2006 *Small* **2** 85
[9] Chan C K, Peng H, Liu G, McIlwrath K, Zhang X F, Huggins R A and Cui Y 2008 *Nat. Nanotechnol.* **3** 31
[10] Viera G, Mikikian M, Bertran E, Roca i Cabarrocas P and Boufendi L 2002 *J. Appl. Phys.* **92** 4684
[11] Arbiol J, Kalache B, Roca i Cabarrocas P, Morante J R and Fontcuberta i Morral A 2007 *Nanotechnology* **18** 305606
[12] Arbiol J, Fontcuberta i Morral A, Estrade S, Peiro F, Kalache B, Roca i Cabarrocas P and Morante J R 2008 *J. Appl. Phys.* **104** 064312
[13] Zhao X, Wei C M, Yang L and Chou M Y 2004 *Phys. Rev. Lett.* **92** 236805
[14] Wagner R S and Ellis W C 1964 *Appl. Phys. Lett.* **4** 89
[15] Givargizov E I 1975 *J. Cryst. Growth* **31** 20
[16] Kwak D W, Cho H Y and Yang W C 2007 *Physica* E **37** 153
[17] Seifert W *et al* 2004 *J. Cryst. Growth* **272** 211
[18] Wu Y, Cui Y, Huynh L, Barrelet C J, Bell D C and Lieber C M 2004 *Nano Lett.* **4** 433
[19] Cui Y, Lauhon L J, Gudiksen M S, Wang J and Lieber C M 2001 *Appl. Phys. Lett.* **78** 2214
[20] Schmidt V, Senz S and Gösele U 2005 *Nano Lett.* **5** 931
[21] Ross F M, Tersoff J and Reuter M C 2005 *Phys. Rev. Lett.* **95** 146104
[22] Kalache B, Roca i Cabarrocas P and Fontcuberta i Morral A 2006 *Japan. J. Appl. Phys.* **45** 190
[23] Kamins T 2007 Semiconductor nanowires for electronics and sensors *397 HE-Heraeus-Seminar; Semiconductiong Nanowires: Physics, Materials and Devices*
[24] Kamins T I, Stanley Williams R, Chen Y, Chang Y-L and Chang Y A 2000 *Appl. Phys. Lett.* **76** 562
[25] Iacopi F, Vereecken P M, Schaekers M, Caymax M, Moelans N, Banpain B, Richard O, Detavernier C and Griffiths H 2007 *Nanotechnology* **18** 505307
[26] Chandrasekan H, Sumanasekara G U and Sunkara M K 2006 *J. Phys. Chem.* B **110** 18351
[27] Sharma S and Sunkara M K 2004 *Nanotechnology* **15** 130
[28] Stelzner T, Andrä G, Falk F, Wendler E, Wesch W, Scholz R and Christiansen S 2007 *Nucl. Instrum. Methods Phys. Res.* B **257** 172
[29] Grundmann M 2007 *Introduction to Semiconductor Physics* (Berlin: Springer)
[30] Beadle W E, Plummer R D and Tsai J C 1985 *Quick Reference Manual for Silicon Integrated Circuit Technology* (New York: Wiley) p 2–71
[31] Sunkara M K, Sharma S, Miranda R, Lian G and Dickey E C 2001 *Appl. Phys. Lett.* **79** 1546
[32] Jeon M, Tomitsuka Y and Kamisako K 2008 *J. Indust. Eng. Chem.* **14** 836
[33] Hannon J B, Kodambaka S, Ross F M and Tromp R M 2006 *Nature* **440** 04574
[34] Bao J, Bell D C, Capasso F, Wagner J B, Mårtensson T, Trägårdh J and Samuelson L 2008 *Nano Lett.* **8** 3836
[35] Fontcuberta i Morral A, Arbiol J, Prades J D, Cirera A and Morante J R 2007 *Adv. Mater.* **19** 1347
[36] Prades J D, Arbiol J, Cirera A, Morante J R and Fontcuberta i Morral A 2007 *Appl. Phys. Lett.* **91** 123107
[37] Bandet J, Despax B and Caumont M 2002 *J. Phys. D: Appl. Phys.* **35** 234
[38] Wang R P, Zhou G W, Pan Y L S H, Zhang H Z, Yu D P and Zhang Z 2000 *Phys. Rev.* B **61** 16827
[39] Bandet J 2002 *J. Phys. D: Appl. Phys.* **35** 234
[40] Alet P-J, Yu L, Palacin S and Roca i Cabarrocas P 2008 *J. Mater. Chem.* **18** 5187–9
[41] Hamers E A G, Fontcuberta i Morral A, Niikura C, Brenot R and Roca i Cabarrocas P 2000 *J. Appl. Phys.* **88** 3674
[42] Fontcuberta i Morral A, Bertomeu J and Roca i Cabarrocas P 2000 *Mater. Sci. Eng.* B **69/70** 559
[43] Fontcuberta i Morral A and Roca i Cabarrocas P 2002 *J. Non-Cryst. Solids* **299–302** 196
[44] Schmidt V, Senz S and Gosele U 2007 *Phys. Rev.* B **75** 045335
[45] Wu Y, Cui Y, Huynh L, Barrelet C J, Bell D C and Lieber C M 2004 *Nano Lett.* **4** 433–36
[46] Schmidt V, Senz S and Gosele U 2005 *Nano Lett.* **5** 931–5
[47] Cai Y, Chan S K, Sou I K, Chan Y F, Su D S and Wang N 2007 *Small* **3** 111–5