Monolithic Integration of SEED's and VLSI GaAs Circuits by Epitaxy on Electronics

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***Abstract*—Using the epitaxy-on-electronics (EoE) process, self-electrooptic effect devices (SEED's) have been monolithically integrated with VLSI GaAs electronics. The EoE approach provides both depletion-mode and enhancement-mode MESFET's for large-scale, high-density optoelectronic circuits. The performance of SEED's grown by molecular beam epitaxy at a reduced temperature compatible with the EoE process is shown to be robust, and modulators with contrast ratios of 2.3:1 at 7.5-V bias have been integrated on commercially processed VLSI GaAs circuits. The EoE-SEED process offers potential improvements over the FET-SEED process, facilitating the applications of SEED's in free-space optical switching and computing.**

***Index Terms*—EoE-SEED, FET-SEED, MBE, MQW modulators, OEIC, optoelectronic integration, SEED.**

I. Introduction

Multiple-quantum-well (MQW) modulators and self-electrooptic effect devices (SEED's) have been demonstrated over the last decade. Their low power consumption and high modulation speed make them ideal for large-density optoelectronic switching and computing systems [1]. Many applications require integration of field-effect transistors with modulators. A hybrid integration using flip-chips and solder bonds has been demonstrated [2], and more recently it was used to bond SEED's to silicon CMOS circuitry [3]. A small-scale monolithic integration of modulators, MESFET's, and RTD's was achieved in so-called monolithic optoelectronic transistors (MOET's) [4], while a larger scale batch fabrication technology of monolithic integration of SEED's with MESFET's was developeded by AT&T and termed the FET-SEED process [5].

Monolithic integration is preferable to hybrid in the long run, but both the MOET and FET-SEED processes are limited in that they offer only depletion-mode FET's (DFET's), which makes circuit design more complicated and increases power consumption and, in turn, limits integration density. A larger pixel area and more parasitic capacitance also result since additional voltage rails are needed to provide the various bias levels [6]. As a practical matter, both of these approaches are also limited, at least presently, by the immaturity of the electronic circuit technology used, by the difficulties of achieving good electronic uniformity across a wafer, and growing and contacting the backgate shields used to isolate the MESFET's from the underlying MQW layers.

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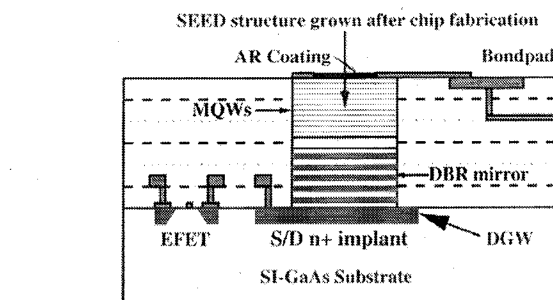

Fig. 1. Schematic illustration of the EoE-SEED process, where S/D n^+ implant is source/drain n^+ implant, AR coating is antireflection coating, DGW is dielectric growth well, DBR is distributed Bragg reflector, MQW is multiple quantum well, and EFET is enhancement-mode FET.

In this letter, we present the results of using a monolithic integration scheme called epitaxy-on-electronics (EoE) [7]–[10] to fabricate optoelectronic integrated circuits (OEIC's) containing MQW modulators integrated with VLSI density GaAs electronic circuitry (EoE-SEED). The EoE-SEED process allows one to design SEED circuits with both enhancement-mode and depletion-mode GaAs MESFET's, along with many other devices such as Schottky diodes and photodetectors. This technology offers better design flexibility and lower power consumption and can be easily extended to a full wafer fabrication process and greatly reduce the cost of OEIC's. A similar concept has been pursued by Cunningham *et al.* [11], [12], and the present work is the first demonstration of functional monolithically integrated EoE-SEED modulators.

II. Experiment and Results

A. EoE-SEED Process

Fig. 1 shows a schematic illustration of the fabrication process for EoE-SEED OEIC's. The SEED-specific electronics

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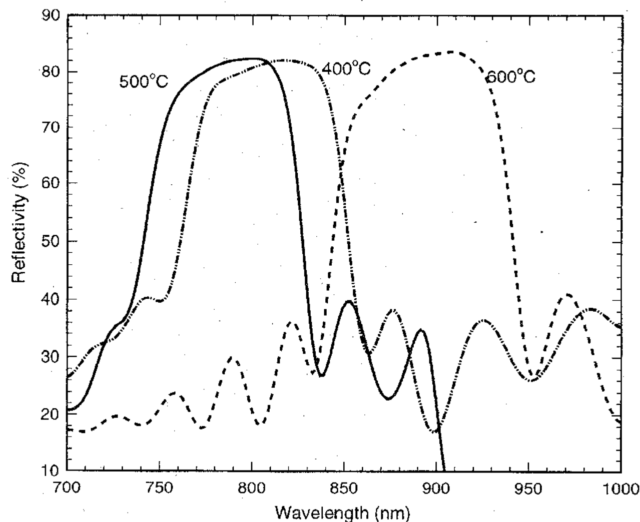

Fig. 2. Reflection spectra from 16-period $AlAs/Al_{0.11}Ga_{0.89}As$ DBR's grown at 600 °C, 500 °C, and 400 °C, respectively, under identical growth conditions.The stopband center wavelength shifts are due to thickness calibration variances.

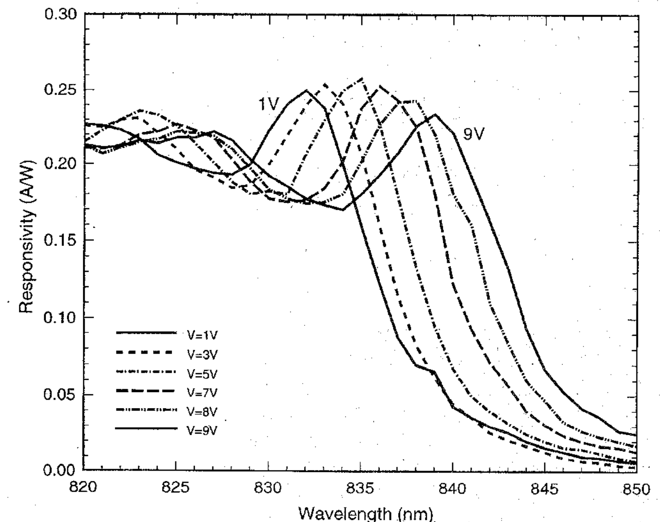

Fig. 3. Stark shift of $GaAs/Al_{0.30}Ga_{0.70}As$ MQW p-i-n photodiodes grown at the reduced temperature of 500 °C.

are designed using standard CAD tools. The growth regions for modulators, called dielectric growth wells (DGW's), are allocated during design and opened during fabrication. Once the circuitry is fully fabricated by Vitesse through MOSIS [9], the MQW modulator structures are grown by molecular beam epitaxy (MBE) in the cleaned DGW's. Post-growth fabrication turns the heterostructures into SEED's and interconnects them with the electronics on the same chip to form the final monolithic OEIC.

The EoE process imposes its own constraints on the growth and fabrication. The limits on growth time and temperature are set by the thermal stability of the underlying electronics [10]. To avoid circuit degradation, a low-temperature cleaning of the oxide on GaAs prior to the MBE growth and a growth temperature lower than 500 °C are desired for EoE-SEED's. Successful oxide removal using the electron cyclotron resonance Hydrogen plasma at 400 °C has been reported [12]. Restricting the growth temperature to under 500 °C remains an issue, since most conventional epitaxy of AlGaAs SEED heterostructures, is done in excess of 600 °C.

B. *EoE-SEED Design and Reduced-Temperature Growth*

SEED circuits were designed and fabricated as multiproject chips which include SEED receivers, transmitters, NOR gates, and other functional logic [9]. In addition, a 10×10 SEED optical "bump circuit" neuron array was designed [6].

Several MBE growths were conducted to prove that the constituent parts of the SEED structure can be grown at reduced temperature. To confirm that the reflectivity of distributed Bragg reflectors (DBR's) is not adversely affected, three 16-period $AlAs–Al_{0.11}Ga_{0.89}As$ DBR's were grown at various temperatures. Fig. 2 shows that the effect of growth temperature on DBR peak reflectivity and stopband width is insignificant to as low as 400 °C.

To confirm that the exciton peak is strong when grown at a reduced temperature, 75 undoped quantum wells, comprised of 90-Å GaAs wells and 35-Å $Al_{0.30}Ga_{0.70}As$ barriers, were grown in a p-i-n structure at 500 °C. The photoluminescence study indicated distinct and strong MQW peaks. The reverse bias characteristics showed less than 10 nA of dark current flowing at −15-V bias, which is typical for this kind of heterostructure. In Fig. 3, the Stark shift of the exciton peaks can be clearly seen when the applied voltage is changed.

C. *Monolithic Integration of SEED's with GaAs VLSI*

The residual dielectric layers in the growth wells need to be cleaned before the MBE growth. Reactive ion etching (RIE) was used to etch away a portion of the dielectric stack and an extended oxygen plasma etch was used to remove the RIE chloroflurocarbon residues in the DGW's. An aluminum mask was then used to protect the bond pads and the overglass on top of the circuitry. A combination of RIE/buffered oxide etch (BOE) was employed to remove the dielectric remaining in the wells. Upon completion, the substrate surface was exposed. The chips were loaded into the MBE system along with a GaAs control wafer. Following the oxide desorption (580 °C for 4 min), the modulator structure was grown at 500 °C. The total growth time for the 5.8-μm stack (10 h) was longer than typically required since only one Al cell was used for this growth. The material morphology in the wells was good except for some defects in a testing area where the substrate surface was not perfectly cleaned.

In the postgrowth fabrication, the polycrystalline material in the inter-DGW areas was etched using 1:1:5 H_3PO_4:H_2O_2:H_2O, resulting in a quasi-planar surface for further processing. The control wafer was doped n^+ and the bottoms of the growth wells on the chip were source/drain ion-implanted n^+; thus, only the top p-contact was needed. A shallow trench down to the intrinsic MQW region was etched in order to isolate adjacent devices. A silicon nitride passivation layer was then deposited using PECVD at 310 °C. Contact vias were plasma etched through the nitride, and AuZn–Au was e-beam evaporated and annealed at 410 °C.

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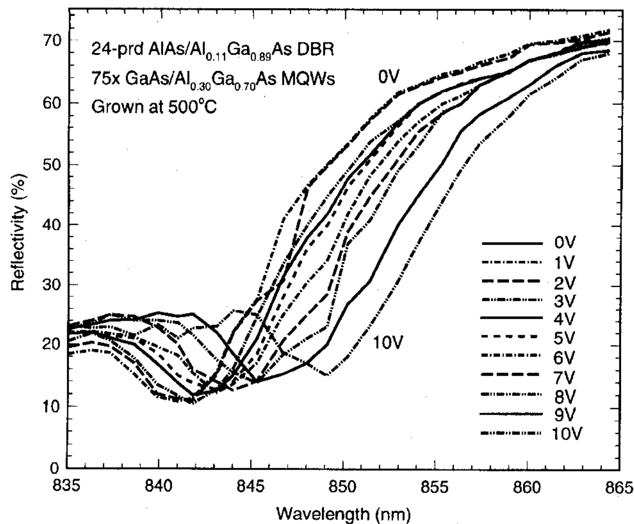

Fig. 4. The measured reflectivity of SEED's on the control wafer grown at 500 °C. Modulators on the EoE-SEED chip have almost identical responses except that the reflectivity is lower because the size of modulators on chip, $20 \times 20\ \mu m^2$, is smaller than the incident beam diameter, $40 \times 40\ \mu m^2$.

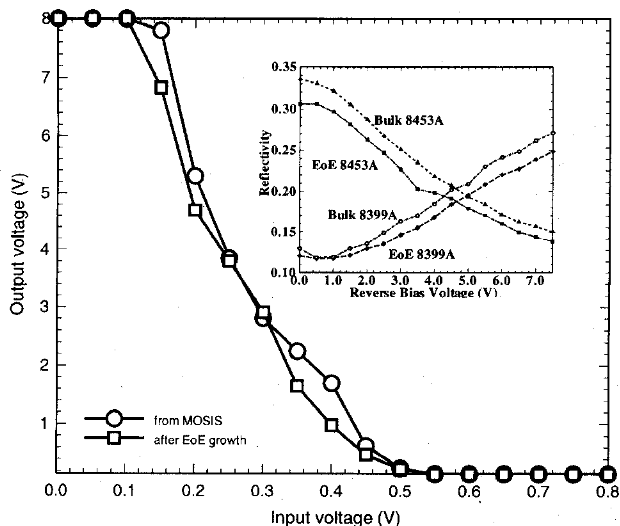

Fig. 5. Voltage control circuit performance before and after the EoE process. The inset shows the modulation of bulk and EoE SEED's at $\lambda_0 = 8399$ Å and $\lambda_1 = 8453$ Å.

Finally, an antireflection coating was sputtered on at room temperature.

D. EoE-SEED Testing

A Ti:sapphire tunable laser was used to test the devices. A contrast ratio of 2.3:1 for 7.5-V bias at 8491 Å was obtained from the EoE integrated SEED's (7.5 V is the upper limit designed for the integrated voltage control circuit). On the control wafer, a contrast ratio of 3.3:1 was obtained for 10-V bias at 8491 Å (Fig. 4). The modulation behavior is nearly identical for modulators on the control wafer and on the EoE-SEED chip (Fig. 5).

The SEED voltage control circuit worked almost as well as before the growth, as shown in Fig. 5. The bump circuit showed a small shift with wider bump response [6]. Such behavior can be eliminated by using a second Al cell to reduce the growth time and using a lower temperature oxide cleaning technique prior to the MBE growth [12]. Since the EoE-SEED's drew more current than the voltage control circuit was designed to provide [6], the present EoE-SEED measurement was driven by an external source in order to reach the bias target. Future circuit designs will include additional drive capability to avoid this problem.

III. Conclusion

We have realized MQW modulators monolithically integrated on VLSI GaAs electronics using the EoE process. MQW structures grown by MBE at a reduced temperature compatible with the EoE process have demonstrated good performance. The EoE-SEED approach provides the unique benefit of the availability of both enhancement-mode and depletion-mode MESFET's as well as other optoelectronic devices integrated with SEED's. These advances result in reduced power consumption and greater design flexibility of high-density SEED optoelectronic circuitry used for free-space optical switching and computing.

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