

# Regenerative Circuits for Rapid Biosensing

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**Abstract**—Integrated DNA-sensor arrays typically check for probe-target strand hybridization by analyzing the sensed capacitance changes, normally off-chip in software. However, many applications like portable medical devices require only the detection of an event or of a substance. We reduce the area, power and computational overhead for this task manifold with simple regenerative analog and mixed-signal circuits, including a 9-b low-power regenerative rail-to-rail comparator and a winner-take-all (WTA) circuit. Simulation of a design targeted for implementation in a 0.35 $\mu\text{m}$  CMOS process is presented.

## I. INTRODUCTION

Two main areas of research in VLSI biosensor arrays include piezoelectric DNA hybridization detection and impedance spectroscopy [1, 2]. Of these, fast solid state DNA sequencing using devices such as ion sensitive field effect transistors (ISFETs) is of particular interest due to the large number of fragments whose presence must be detected [3]. Fully electronic label free DNA sensors with on-chip analog-to-digital converters and fabricated in mainstream CMOS processes have proved their advantage over expensive and cumbersome fluorescence and vision based systems [4, 5]. There have been efforts to combine the two approaches, digital and optical, with limited success [6, 7]. The performance of digital DNA detectors for a given application can be improved by choosing the most appropriate architecture [8, 9]. Also, sub-components such as amplifiers and data converters can be made as efficient as possible and researchers have tended to favor delta sigma converters due to area and power considerations [10, 11].

In mobile or point of care medical applications it is often the case that the presence of a quantity of interest, such as a virus, is detected [12]. In this paper we show that a 1-b decision on the presence or absence of DNA hybridization can similarly be made on-chip with a simple regenerative comparator. Our approach has two main advantages over existing approaches: (1) it avoids on-chip data conversion and off-chip data analysis thereby saving the power, time and supporting H/W overhead and (2) it reduces the area used by electronics associated with a sensor site in an integrated biosensor array thus allowing for an increase in the density of the array, reducing its size or offering added space for more functionality. We illustrate our approach with a low power rail-to-rail comparator with 9-b resolution targeting a design

in 0.35 $\mu\text{m}$  CMOS process at 3V supply. We also propose the novel use of WTA and loser-take-all (LTA) circuits for such systems. Lastly, these techniques will be applicable at finer geometries and supply voltages down to 1V.

## II. SENSING PRINCIPLE AND METHOD

### A. Principle

In DNA sensor arrays a single type of probe strand is exposed at each site to solutions suspected of containing a target strand. Conversely there may be many different probes used to check the existence of different targets in a common solution. Depending on the extent of probe-target hybridization, if at all, there is a change in some electrical quantity, such as capacitance, which may be inferred from yet other quantities such as sensed voltage or current. The relation is not necessarily linear and in the case of capacitance and voltage it is inverse necessitating indirect approaches including frequency conversion [5]. Further, experimental variations necessitate many measurements.

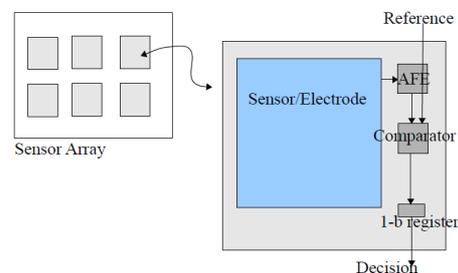


Figure 1. On-chip decision scheme reduces off-chip analysis.

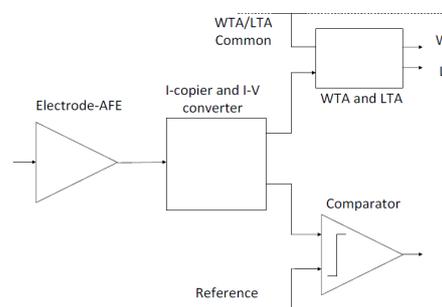


Figure 2. Block diagram of sensor cell electronics.

### B. Standard Method: On-chip A/D and Off-chip Analysis

Typically, the analog voltage detected is converted to 8-10 bits of digital data to be read out and its statistics analyzed off-chip [4]. The computational and time overhead of the supporting hardware and software is not an issue in scientific characterization in a lab setting with dedicated analog-to-digital converters (ADC) [14]. The analog front end (AFE) for signal conditioning at each site affects the size of the array as does the device matching requirement for multiple identical ADC's. Small-area delta-sigma ADCs help curtail power usage [11]. Some area is saved by reusing a single quantizer, but additional area is required by the control and doubling circuits and for sizing per accuracy requirements.

### C. Proposed Method: Decision On-chip

For many non-laboratory applications, particularly point of care or portable medical devices, the 1-b answer sought is whether or not the underlying distinctive hybridization has occurred and caused discernible change in capacitance. The answer must be robust against experimental variations and false positive cases like partial hybridization. Area and power are of prime importance. These goals can be met simply by using a single comparator (fig. 1) and setting its reference to a pre-determined or known level. The reading error within a cluster of sensors can be gauged quickly with WTA and LTA circuits (fig. 2). The main design limitation now is the matching amongst multiple comparators and a bound on their offsets.

## III. ARCHITECTURE

The most straightforward method of checking for hybridization on an array site is to compare it to a reference site "1-1" (fig. 3a). The reference site can have the same electrode and probe electronics but at which hybridization is impossible. Another technique is to compare multiple sites each with the same type of probe to a single reference (fig. 3b). This is a realistic scenario because it parallels the case of multiple sensors. This is a "many-1" setup where sensors with the same probe are clustered at one site or element in the array. Hybridization is sensed during an evaluation phase. Due to experimental variations the minimum and maximum of the measured quantities can yield valuable information. These statistics can be obtained during a characterization phase quickly via the WTA and LTA circuits. They can also emerge in a more detailed manner after interrogating each sensor and doing a data conversion by utilizing the combination of global reference from the multiplying digital-to-analog converter (MDAC) with the local comparator and associated switching digital logic circuits (fig. 4). The relatively low speed requirements in bio-sensor arrays permit longer settling times for the MDAC and hence 9-10 bit accuracy. As it ramps up, or down, the reference will trip the comparator at some point. The digital word for the reference-generating DAC represents the digitized value of one of the following: (1) the *min* and (2) *max* identified by the WTA or LTA or (3) any desired individual sensor reading.

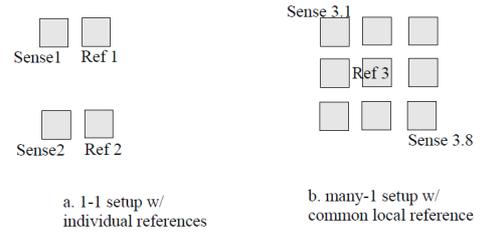


Figure 3. Comparator reference location.

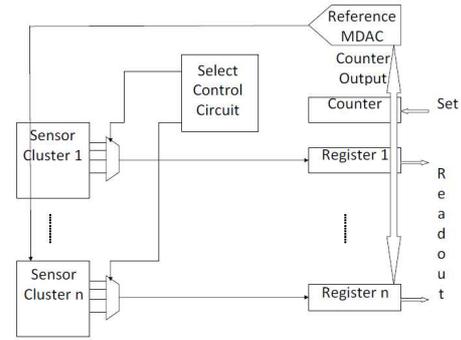


Figure 4. Architecture overview.

For simplicity every cluster has only one register so the register must be read out before querying the next quantity for that cluster. Hence, since there are effectively multiple ADC's, one at each site in the integrated sensor array, we still retain the ability to perform more complex off-chip analysis of the standard approaches for calibration or verification purposes. No useful information is lost with our approach.

## IV. CIRCUITS

### A. Comparator

To obtain the best SNR a rail-to-rail comparator is necessary [13]. We use a complementary input stage pre-amp coupled with a regenerative latch and output drive restorer (fig. 5). Fig. 6a shows the simplified half of the circuit dealing with low voltage inputs. Due to the non-linearity in the sensed quantity, i.e. the comparator's signal input, the dispersion over different parts of the input range can be great or small. The systematic resolution is critically dependent on the process-dependent value and variance of offset across multiple comparators. Offset correction mechanisms help obtain better results. Simulations with 3V supply show we can resolve 5mV within 200mV of each rail (fig. 7). This translates to 9-b accuracy. Fig. 8 shows the simulated comparator offset voltage due to load mismatch. It is technology dependent ( $\alpha, \beta$ ) and given [17] as:

$$\sigma(V_{\text{off}}) = (k_p \cdot (V_{\text{gs}} - V_t) / g_m \cdot L^2) \cdot (\alpha + (\beta/4) \cdot (V_{\text{gs}} - V_t)^2) \quad (\text{Eq. 1})$$

The comparator response time varies over temperature and is nominally about 4ns over a large range from 10-60 °C (fig. 9). However, it becomes excessively large at high temperatures. This is an important limitation because DNA biosensors are often subjected to heating and cooling cycles to facilitate hybridization.

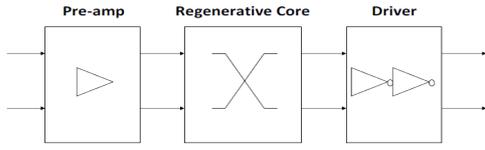


Figure 5. Comparator components.

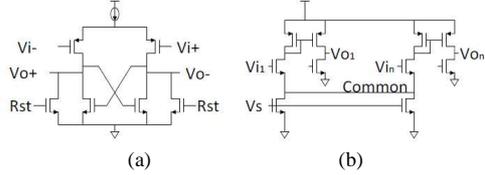


Figure 6. Core regenerative circuits (a) comparator, (b) WTA.

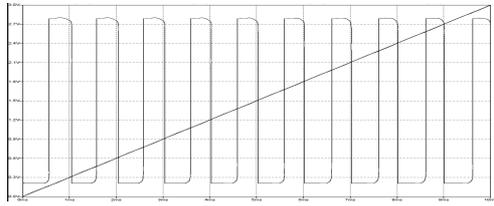


Figure 7. 9-bit rail-to-rail comparator operation SPICE result.

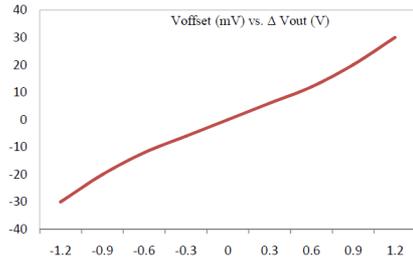


Figure 8. Simulated comparator offset.

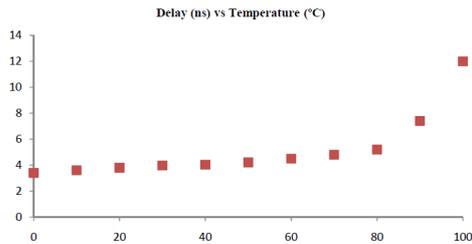


Figure 9. Response time variation with temperature.

## B. WTA and LTA

Calculating the minimum and maximum of sensed voltages within a cluster of sensors is useful for characterization purposes. The maximum,  $max$ , is obtained by ramping up a reference and noting at what reference value all comparator outputs switch to below reference. Similarly the minimum,  $min$ , is obtained by ramping down and noting what reference value all outputs are above reference. This information is normally obtained off-chip in software.

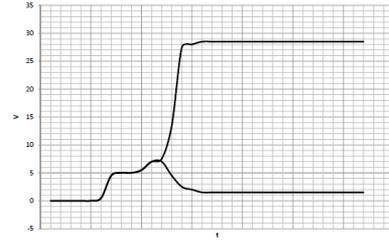


Figure 10. WTA operation simulation with 1 winner and 1 loser.

Alternate WTA-based on-chip techniques exist that offer speed and low power [15]. In our simulations (fig. 10), the output of the sensor's AFE is a current which is copied and fed to the WTA where there is another I-V conversion. We are able to resolve inputs more than 10mV apart which is worse than the comparator accuracy but acceptable. Due to the increased capacitive loading from multiple cells the WTA output waveform can quickly get corrupted so an output driver is necessary for our setup with 8 sensor sites per cluster. The WTA does not function except during characterization phase when it helps pinpoint the sensor site of interest. The re-use of a n-input WTA circuit with current mirroring for p-input for the converse minimum calculation is not preferred due to the accuracy degradation and additional power consumption [19]. We propose this method, however, because the accuracy is still sufficient and because the circuit runs only during characterization.

## V. RESULTS

Fig. 11 shows the clocking signals to operate the proposed system. For simulation purposes, different fixed capacitances were used at each of the different "electrodes." In a real lab experiment the electronics would initially be in a low power state (signal Eval=0) to allow enough time for hybridization. Subsequently (Eval=1) there would be three phases: (1) Normal: serially load each sensor comparator outputs serially into adjacent bits of corresponding 9-bit register for that cluster (2) Characterization: full-fledged AD conversion for sites flagged by one of (WTA, LTA or anything else chosen) and (3) Readout: take data from each of the cluster registers off-chip. We simulated two clusters of 8 sensors each. For clarity, Fig. 12 shows output voltages for 6 of the 8 sensors from a characterization run. In phase (1) above, the binary value at any bit position corresponds to whether the comparator has tripped at that sensor site indicating hybridization. In phase (2) the register value is the reference generating MDAC's counter stamp corresponding to the digital output of the AD conversion. The reference voltage in this example lay between  $max$  of cluster #2 and  $min$  of cluster #1. This case illustrates results when cluster#1 is very likely partially hybridized. We compared the simulated performance of each cell in a bio-sensor array using the on-chip method to the standard method in terms of (1) area, (2) current and (3) computational time (Table 1). The entries for the standard method [10, 11] assume an optimal delta-sigma converter [16]. We assume electrode sizes of  $200 \times 200 \mu m^2$  which are

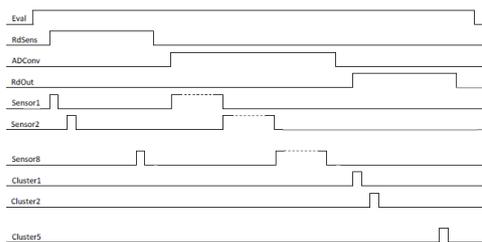


Figure 11. Clock waveforms for system simulation.

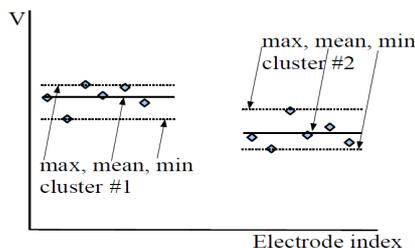


Figure 12. Output statistics from simulated sensors.

more realistic than the smaller  $50 \times 50 \mu\text{m}^2$  electrodes but which tend to dominate the area comparison. The cell electronics' area itself is not as small as hoped because of the required digital logic and storage registers. Current draw is listed instead of power consumption because the circuit techniques can be used at less than our 3V supply. Faster operation is possible for both methods with a large ratio maintained between the two. Adding off-chip computation time, or area and power to support such computation, would drastically alter the figures in favor of the on-chip decision method. At  $6 \mu\text{A}$  the current is 7.5x lower than standard and at a simulated 670ns the time is 9x faster. The figure-of-merit is proportional to the inverse of the product of area, current drawn and on-chip computation time. This yields a conservative merit advantage of 78.

## VI. CONCLUSION

We have presented simulations that show that, without loss of other useful information, a 1-b decision on the presence or absence of DNA hybridization can be made on-chip with simple regenerative comparators and WTAs. We thereby (1) reduce the attendant power and computation time and (2) reduce the electronics area for  $0.35 \mu\text{m}$  CMOS integrated biosensors to facilitate mobile applications such as health screening. Our approach can be extended to lower supply voltages as well as to dynamically tracking reactions.

TABLE 1: RESULTS SUMMARY.

Metric	Area ( $\mu\text{m}^2$ ) (circuits)	Area ( $\mu\text{m}^2$ ) (circuits+electrode)	Current ( $\mu\text{A}$ )	Compute Time (ms)
<b>A. Standard</b>	10,000	50,000	45	6
<b>B. This work</b>	3,000	43,000	6	0.67
<b>Ratio B:A</b>	0.3	0.86	0.13	0.11

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