The Effect of Interface Modification on the Properties of Organic Thin-Film Transistors

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Wissenschaft ist die Schwester des Witzes und des Kindes; wie diese versucht sie stets, alles in einem neuen Licht zu sehen und auf den Kopf zu stellen, um das Prickeln der Überraschung zu spüren. Weshalb sonst würden Kinder so gerne Worte verdrehen und einen Hut verkehrt aufsetzen?

*

Science is the soul brother of the joke and the child: they all love to look at things in a new way, to turn things upside down, to feel the thrill of surprise. Just watch children delight in jumbling words or putting on a hat backwards.

Gottfried Schatz,
Emeritus Professor in Biochemistry,
University Basel, Switzerland

Acknowledgement

Making a thesis takes time and energy. A bit more than three years ago, I started my thesis at LOMM; a new topic and a new language were waiting for me. Now, I have it written and there are many people who helped me to finish this project.

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Abstract

In organic thin-film transistors (OTFTs), the conducting channel is located near the interface between the organic semiconductor and the dielectric; this interface is crucial for transistor performance. The goal of this thesis is to study the effect of this interface, especially when it is modified either by surface treatments or self-assembled monolayers. For this purpose, OTFTs based on pentacene and doped silicon wafer gate electrode and gold top contacts are fabricated. The dielectric is either silicon oxide (SiO_2) or polyimide (PI).

The dielectric surface affects both the growth of the pentacene film on the top of it and the electric performance of the transistor. The pentacene film morphology is studied on treated and untreated SiO_2 and PI surfaces by AFM and water contact angle measurements. Depending on the nature of the dielectric surface, traps or charge transfer centers are introduced which then affect the performance of the transistor. The transistor performance is determined by measuring the drain current as it is dependent upon the drain and gate voltage. The contributions of the channel and the contacts are separated by 4-probe measurements (at floating and non-floating gate).

The transistors with untreated dielectrics are first characterized. The dependence on the channel length, the thickness and the morphology of the pentacene film is studied. The short channels ($2 - 20\mu m$) are patterned by stencil masks; the long channels ($100 - 600\mu m$) by steel masks. The results show that the transistors with a channel length of $20\mu m$ and smaller are limited by the contacts, while the transistors with a channel length between 100 and $600\mu m$ are dominated by the channel, and thus the traps and residual carriers in the channel. The pentacene film morphology has more influence on the contact resistance than on the channel behavior.

To study the effect of the interface modifications, the transistor behavior should be dominated by the channel and the contact effects minimized; hence, long-channel transistors are used. The dielectric surfaces are treated by plasma or pH solutions prior to the pentacene deposition resulting in a variety of defects. The defects are distinguished by those which lead to a change in the film growth and those which affect the electric performance by introducing traps or charge transfer centers.

To overcome the influence of the dielectric surface, the oxide dielectric is passivated by a self-assembled monolayer (SAM). The neutral SAM acts as a spacer between the dielectric and the pentacene film and thus enhances the transistor per-

formance. The polar SAMs also introduce a dipole moment. A series of molecules with a similar length, but different end groups, are used to investigate the effect of the dipole moment.

The main result of this study is that the nature and the quality of the gate and the contact interfaces are often more important for the performance of the transistors than the thin film morphology.

Keywords: Organic semiconductor, organic thin-film transistor, organic field-effect transistor, interface modification, dielectric treatment, self-assembled monolayer

Résumé

De nos jours, l'idée de fabriquer de l'électronique à bon marché à partir de matériaux plastiques suscite d'intéressantes voies de recherche technologique. Dans cette thèse, nous avons tenté d'explorer certains des processus-clé, qui déterminent la fabrication et l'optimisation des transistors organiques.

Dans les transistors organiques à couche mince (OTFTs), le canal conducteur est proche de l'interface entre le semiconducteur organique et le diélectrique. Cette interface est essentielle pour la performance du transistor. Le but de cette thèse est l'étude des effets de cette interface, surtout si elle est modifiée par un traitement de surface ou une monocouche auto-assemblée. A cette fin, nous avons fabriqué des OTFTs à base de pentacène, avec une électrode de grille en silicium dopé et des contacts de source et de drain en or. Le diélectrique est soit en oxyde de silicium (SiO_2) ou en polyimide (PI), traité ou non-traité.

La surface diélectrique influe à la fois sur la croissance du film de pentacène qui lui sert de substrat et sur la performance du transistor. Nous avons étudié la morphologie du film de pentacène sur les surfaces SiO_2 et PI traitées et non-traitées, au moyen de la microscopie à force atomique et des mesures d'angle de contact. Suivant la nature de la surface diélectrique et son degré d'ordre, des pièges ou des centres de recombinaison sont introduits dans le canal qui ont des conséquences sur les performances du transistor. Ces performances ont été évaluées dans la thèse à partir des mesures des caractéristiques électriques. Plus spécifiquement des mesures de la tension de fonctionnement ont été effectuées en deux points et quatre points pour séparer les effets du canal de ceux des contacts.

Nous avons d'abord travaillé sur des transistors dont la grille était une simple silice non-traitée. La dépendance des propriétés du transistor avec la longueur du canal, l'épaisseur et la morphologie du film de pentacène a ainsi pu être analysée au préalable. Les canaux courts ($2 - 20\mu m$) sont dessinés par la technique dite des masques stencil, les canaux longs ($100 - 600\mu m$) par des masques plus traditionels en acier. Les résultats montrent que les transistors à canaux courts voient leurs propriétés électriques limités par les contacts, tandis que les transistors à canaux longs sont dominés par les pièges et les centres de recombinaison dans le canal. Paradoxalement, la morphologie du film de pentacène a une plus grande influence sur la résistance des contacts que sur le comportement des porteurs dans le canal.

Pour analyser l'effet des modifications de l'interface, le comportement du tran-

sistor doit être dominé par le canal et les effets des contacts doivent être minimisés. Nous avons utilisé des transistors à canaux longs. Nous avons traité les surfaces diélectriques par des plasmas ou des solutions pH avant le dépôt du pentacène, pour faire varier les populations de défauts à la surface du canal. Nous avons pu ainsi séparer les défauts de l'oxyde ou du polyimide qui modifient la croissance du film de pentacène, de ceux qui introduisent dans le canal des pièges ou des centres de recombinaison.

Pour surmonter les influences néfastes de la surface diélectrique, nous avons passivé l'oxyde diélectrique par une monocouche auto-assemblée de molécules greffées sur l'oxyde (SAM). La SAM neutre agit comme séparateur entre le diélectrique et le film de pentacène et donc elle améliore la performance du transistor. Les SAMs polaires introduisent en outre un moment dipolaire. Nous avons utilisés une série de molécules de longueurs voisines, mais avec des groupements terminaux différents de manière à investiguer l'effet du moment dipolaire.

Le résultat principal de cette thèse traduit le fait que la nature et la qualité des interfaces de la grille et des contacts sont souvent plus importantes pour la performance des transistors que la morphologie du film mince.

Mots-clés: Semiconducteur organique, transistor organique à film mince, transistor organique en effet de champs, modification de l'interface, traitement de diélectrique, monocouche auto-assemblée

Zusammenfassung

Die Idee, günstige Elektronik aus Plastik herzustellen, ist heutzutage eine der interessantesten Bereiche der technischen Forschung. Die vorliegende Doktorarbeit untersucht einige der Schlüsselfragen, welche die Produktpalette der organischen Dünnschichttransistoren bestimmen.

In organischen Dünnschichttransistoren (OTFTs) befindet sich der leitende Kanal nahe der Grenzfläche zwischen dem organischen Halbleiter und dem Dielektrikum. Deswegen ist diese Grenzfläche entscheidend für das elektrische Verhalten der Transistoren. Diese Doktorarbeit hat zum Ziel, die Wirkung dieser Grenzfläche zu untersuchen, insbesondere wenn sie behandelt oder modifiziert ist. Zu diesem Zweck haben wir OTFTs fabriziert, die auf Pentacene basieren und über eine Gate-Elektrode aus dotiertem Silizum und Goldkontakte verfügen. Das Dielektrikum ist entweder eine Siliziumoxid- (SiO_2) oder eine Polyimidschicht (PI).

Die Oberfläche des Dielektrikums beeinflusst sowohl das Wachstum des Pentacenefilms auf dem Dielektrikum als auch das elektrische Verhalten des Transistors. Wir untersuchten mit Hilfe der AFM (Atomkraftmikroskopie) die Mikrostruktur der Pentacenefilm auf behandelten und unbehandelten SiO_2- und PI-Oberflächen. Abhängig von der Natur der Dielektrikumoberfläche werden Fallen oder Rekombinationszentren eingebracht, welche das Verhalten des Transistors beeinflussen. Die Transistoren wurden elektrisch charakterisiert, indem der Strom durch die Goldkontakte in Abhängigkeit der angelegten Spannungen an den Goldkontakten und dem Gatekontakt gemessen wurde. Zusätzlich wurden die Einflüsse des Kanals von denjenigen der Kontakte mittels Zweipunkt- und Vierpunktmessungen getrennt.

Wir untersuchten zuerst Transistoren mit unbehandelten Dielektrika. Dabei wurde untersucht, wie das elektrische Verhalten von der Kanallänge, der Dicke und der Mikrostruktur des Pentacenefilms abhängt. Die kurzen Kanäle ($2 - 20\mu m$) wurden durch Stencilmasken aufgedampft, die langen Kanäle ($100 - 600\mu m$) durch Stahlmasken. Die Resultate zeigen, dass Transistoren mit kurzen Kanälen durch die Kontakte limitert sind. Die Transistoren mit langen Kanälen werden durch den Kanal dominiert, folglich bestimmen die Fallen und Rekombinationszentren im Kanal das elektrische Verhalten. Die Mikrostruktur des Pentacenefilms hat einen grösseren Einfluss auf den Kontaktwiderstand als auf das Verhalten des Kanals.

Um die Auswirkungen einer modifizierten Grenzfläche zu untersuchen, müssen die Kontakteffekte minim sein. Deswegen arbeiteten wir mit Transistoren mit einem

langen Kanal. Wir behandelten die Oberflächen der Dielektrika mit Plasma oder pH-Lösungen, bevor Pentacene aufgedämpft wurde. Die Behandlungen führen zu verschiedenen Defekten an der Oberfläche. Die Defekte unterschieden sich in ihrer Wirkung: Defekte, die das Filmwachstum ändern, und solche, die das elektrische Verhalten beeinflussen, weil sie als Fallen oder Rekombinationszentren agieren.

Um den Einfluss des Dielektrikums (insbesondere dessen Oberfläche) zu minimieren passivierten wir das oxidische Dielektrikum mit einer selbstorganisierenden Molekularschicht (SAM). Die neutrale SAM funktioniert als Distanzhalter zwischen dem Dielektrikum und dem Pentacenefilm, was das elektrische Verhalten des Transistors verbessert. Die polaren SAMs tragen zusätzlich ein Dipolmoment in sich. Um den Effekt des Dipolmoments zu untersuchen, verwendeten wir eine Gruppe von Moleküle mit ähnlicher Länge, aber unterschiedlichen Dipolmomenten.

Die Hauptaussage dieser Doktorarbeit ist, dass die Natur und die Qualität der Grenzflächen zum Dielektrikum und zu den Kontakten für das elektrische Verhalten eines Transistors meistens wichtiger sind als die Mikrostruktur der Dünnfilme.

Contents

Chapter 1

Overview

Since the 1980's, plastic electronics has been one of the most important dreams of the scientific community. The study of organic field-effect transistors (OFETs) is one of the three important topics of the subject, together with organic light emitting diodes and organic solar cells. Currently, the first "commercial" OFET products are available (*RFID* tags and *e*-book readers). The technology of the near future points to flexible and large area thin-film devices fabricated by solution processes and in ambient atmosphere.

The scientific literature on organic thin-film transistors (OTFTs) is extremely abundant and often contradictory. It is still difficult to have a clear idea on the transport processes and the respective roles of interfaces and contacts, even if several comprehensive reviews have been published in the field [1, 2, 3]. For this reason, model systems help to understand the basic processes in thin-film transistors.

In this thesis, we point on interface effects and a model system is used to understand their role on transistor performance; it consists of a silicon wafer as gate electrode, silicon oxide (SiO_2) or polyimide (PI) layer as dielectric, pentacene as organic semiconductor and gold top contacts. The pentacene thin film is evaporated in a high vacuum on the top of the oxide or polymeric dielectric at different deposition conditions. The dielectric surface is modified by surface treatments or self-assembled monolayers. The transistor geometry is varied by changing the channel length, the semiconductor film thickness, and morphology.

The thesis is divided as follows Chapter 1 is an introduction to the architecture, charge transport, interface and contact effects, in the form of a literature survey. Chapter 2 describes the fabrication processes and characterization of our transistors.

In Chapter 3, the pentacene film growth on the top of the dielectric is analyzed on the basis of AFM micrographs. Grain sizes and morphology are determined by the dielectric surface and deposition conditions. Surface treatments of SiO_2 and PI can change the morphology of the final film.

The performance of transistors containing bare and untreated dielectric surfaces is analyzed in Chapter 4. The purpose was to separate the relative contributions of

the channel and the contacts. The influence of the device architecture was studied on transistors with channel lengths ranging from 2 to 600μm and with pentacene film thicknesses ranging from 10 to 80nm.

In Chapter 5, the effects of the defects sitting at the dielectric surface are presented. The dielectric surface was modified by different treatments to vary the defect nature and concentrations. Some of the defects change the transistor performance; others affect the film growth.

In Chapter 6, the dielectric oxide surface was passivated by introducing a self-assembled monolayer (SAM); the effects of a neutral SAM and a series of polar self-assembled monolayers were analyzed. The latter are SAMs with the same grafting system and similar length but the end groups and the dipole moments differ. Thus we were able to determine the effect of the dipole moment on the transistor behavior.

Chapter 2

Introduction to organic transistors

The interest in organic transistors is based on processing low-cost electronic devices on flexible substrates. The functioning of organic transistors is based on the gate field effect and a variety of materials and designs are currently possible. Because the electric output of both organic and inorganic transistors looks similar, the same parameters are used to describe the performance of the transistors. But the charge transport in organic semiconducting materials is based on different processes.
In this chapter, the different aspects of an organic transistor are highlighted. The organic semiconductor is the heart of the transistor and the electric performance is based on its ability to transport charges. The transistor is completed by the dielectric, the gate, and the contacts which influence via different ways the transistor behavior. To begin, the general functioning and architecture of organic transistors are explained; the aforementioned characteristics will then be discussed.

2.1 Organic field-effect transistors

The organic field-effect transistors are staggered devices consisting of a gate, an organic semiconductor, a dielectric and contacts. The organic semiconductor is separated from the gate electrode by a thin insulating layer, the gate dielectric (see Fig. 2.1). When a field is applied at the gate, charge carriers are induced into the organic semiconductor near to the dielectric interface, i.e. a conducting channel is formed. By applying a voltage between the source and the drain contact attached to the semiconductor, the charge carriers are driven in the channel.

The starting point of organic transistors was in the mid 1980's when the first organic field-effect transistor (OFET) was reported [4]; around the same time, the first organic light-emitting diode and photovoltaic cell were reported [5, 6]. The OFET was built according to the architecture of the inorganic FET [7].
Nowadays, the possibility for manufacturing at or near RT and on flexible substrates opens the horizon for novel products. The first "commercial" organic-electronic products are available, e.g. organic radio-frequency identification tags (*RFID* tags, down to \$0.10 each, *Organic ID*) and electrophoretic displays in *e*-book readers (*Plastic Logic*, *Polymer Vision*).

2.1.1 Electric performance

The electric performance of an OFET is analyzed by applying a gate field across the dielectric layer and measuring the current between source and drain. By the gate voltage (V_G), a gate field establishes in the dielectric layer and charges are induced in the semiconductor near to the dielectric interface and a conducting channel is formed. The charge density depends on the gate field strength and the capacitance of the dielectric layer. The charges in the channel are driven parallel and near to the dielectric surface by a voltage between the two contacts on the organic semiconductor, source and drain (drain voltage V_D).

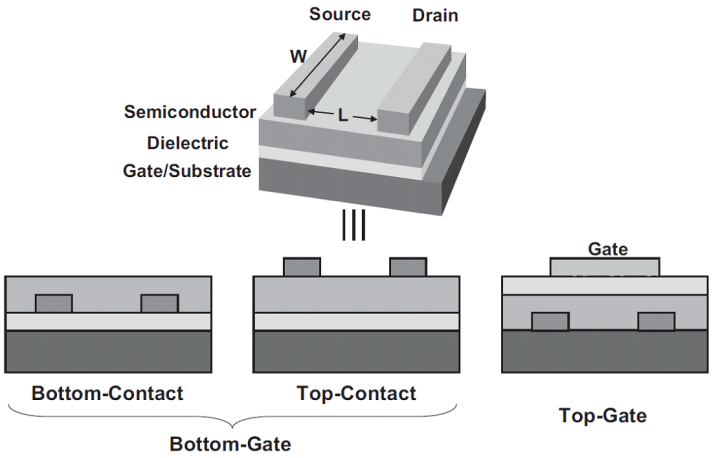

Figure 2.1: *Architectures of organic transistors: bottom contacts and top contacts with bottom gate and bottom contacts with a top gate.*

The organic field-effect transistors work essentially in the accumulation regime [3]. In depletion, shallow dopants are needed but that regime is essentially missing in organic semiconductors. Best performance is showed for undoped (semi)crystalline p-type semiconductors. N-type semiconduction is often suppressed due to stronger electron trapping and a higher sensitivity to oxygen and water.

The OFET performance is divided into two regimes (see Fig. 2.2a). In the linear regime (at small drain voltages, $|V_D| << |V_G|$), the current increases linearly with the drain voltage:

$$I_D = \frac{W}{L} \cdot C_{gate} \cdot \mu_{app} \cdot \left(V_G - V_T - \frac{V_D}{2} \right) \cdot V_D \tag{2.1}$$

where W is the channel width, L the channel length, C_{gate} the dielectric capacitance per unit area, μ_{app} the apparent mobility, V_G the gate voltage, V_T the threshold voltage and V_D the drain voltage [3, 8].

When the drain voltage is increased, a potential gradient is formed between source and drain. The source is grounded therefore the potential at the source corresponds to the gate voltage. The potential at the drain otherwise is the difference between

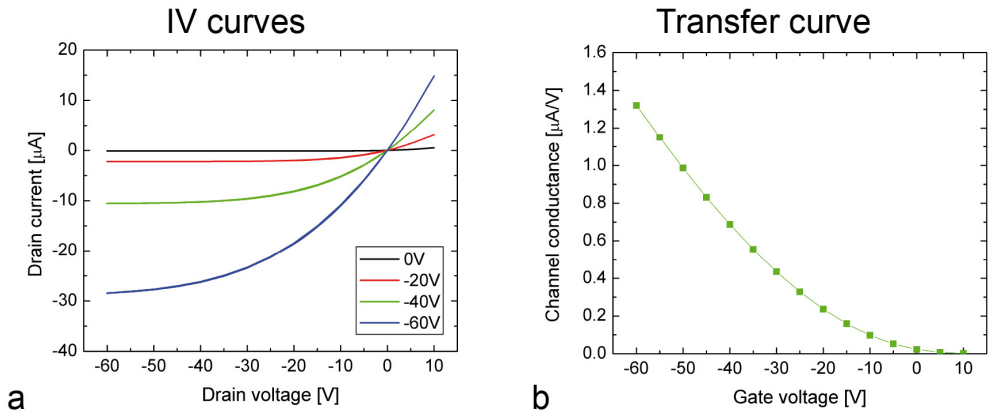

Figure 2.2: *a) Drain current vs. drain voltage for different gate voltages (IV curves) and b) channel conductance vs. gate voltage (transfer curve) for one of our pentacene thin-film transistors on SiO_2 dielectric treated by a H_2 plasma.*

the gate and the drain voltage which becomes smaller and smaller with increasing drain voltage. Thus the charge carriers near the drain are repulsed and the area is depleted. When the drain voltage reaches the value of the gate voltage, the potential close to the drain drops to zero and the channel is pinched. For further increasing of the drain voltage, the current is constant and determined by the pinched region of the channel; the OFET is in saturation. Then the drain current at saturation $I_{D,sat}$ depends by the following on the drain voltage V_D and the gate voltage V_G [3, 8]:

$$I_{D,sat} = \frac{W}{2L} \cdot C_{gate} \cdot \mu_{app} \cdot (V_G - V_T)^2 \tag{2.2}$$

The apparent mobility and the threshold voltage are extracted from the transfer curve (drain current or conductance vs. gate voltage) with equation 2.1 or 2.2 (see also Fig. 2.2b). The channel conductivity and contact resistance are determined by 2-probe and 4-probe resistance measurements.

2.1.2 Transistor architecture

The OFETs can have different architectures (see Fig. 2.1). The position of the source and drain contact can affect the transistor performance because the charge carriers are injected and extracted there. The contacts should have a resistance as low as possible to afford an effective charge injection and extraction. Mainly metals (e.g. gold, copper, platinum), but also conductive polymers (e.g. *PANI*, *PEDOT:PSS*) are used as contact materials [9, 10, 11, 12, 13]. The performance of the contacts depends on both the material's properties and the transistor processing.

The conducting channel is in the vicinity of the dielectric-semiconductor interface thus the dielectric layer can strongly influence the transistor behavior. In general, the dielectric layer should induce high charge carrier density except by the field effect. The dielectric layer should have high breakdown field, no leakage current and no pin

holes. The dielectric surface should be defect free, "perfect" and smooth and the surface chemistry convenient for the deposition of the organic semiconductor. The dielectric should be stable during fabrication and operation and compatible with the manufacturing steps for the entire device.
Many different materials are investigated. Oxide dielectrics show a large variety of static dielectric constants: e.g. SiO_2 (3.9), Al_2O_3 (9.4), Ta_2O_5 (25), TiO_2 (41) and Gd_2O_3 (50) [14, 15, 16]. The oxide dielectrics have in general reproducible surfaces therefore they are often used for comparing different semiconductors. Polymeric dielectrics offer a wide range of properties because their characteristics are tunable by the design of the monomer precursor and polymerization reaction conditions.

Organic single-crystal transistors The semiconductor in the OFETs is either in the form of a single crystal or a thin film . In the single-crystal transistors, the organic single crystal is either laminated on the dielectric-gate structure or coated with the dielectric material. The highest mobilities measured for single-crystal OFETs are $30 - 40 cm^2/Vs$ for rubrene single-crystal transistors with a vacuum gap [17]. In pentacene single-crystal transistors, until recently the largest apparent mobility reported was only $3 cm^2/Vs$ [18, 19]. The low mobility values of pentacene single-crystal transistors was attributed to the oxidation of pentacene at the crystal surface to pentacene-quinone. So the highest mobilities (up to $40 cm^2/Vs$) were measured if the thin-layer of pentacene-quinone was used as gate dielectric [20]. Air-stable n-type single-crystal OFETs are still very rare; exceptions are single-crystal transistors made of $TNCQ$ (tetra-cyano-quino-dimetane) with Au contacts which has an apparent mobility of $0.2 - 0.5 cm^2/Vs$ [17, 21].

In ultrapure single crystal OFETs, the apparent mobility was shown to be anisotropic [22, 23]. If the charge transport is trap dominated, the anisotropy disappears and the electric behavior depends on the properties of the dielectric [24, 25, 14].

Organic thin-film transistors The organic thin-film transistors (OTFTs) contain a thin semiconductor film deposited by thermal evaporation or from solution. Small molecules (e.g. pentacene and oligothiophenes) are often deposited by evaporation in high vacuum what normally brings on a crystalline film. The highest apparent mobilities for pentacene thin-film transistors were a hole mobility of $5.5 cm^2/Vs$ and an electron mobility of $0.17 cm^2/Vs$ [26, 27].

The semiconducting thin film can also be deposited from solution, e.g. by spin-coating, drop-casting or inkjet-printing. This route is used for semiconducting polymers and small soluble molecules. They can be fabricated in ambient atmosphere.

A prototype semiconducting polymer is regioregular poly(3-alkylthiophene) (e.g. $P3HT$ with a hexyl side chain) with mobilities in the range of $0.1 - 0.3 cm^2/Vs$ [28, 29]. Its promising electrical properties arise from a highly crystalline, lamellar microstructure. The apparent mobility is very sensitive on the head-to-tail regioregularity, the deposition conditions and the molecular weight [30, 31]. Mobilities up to $0.8 cm^2/Vs$ for holes and electrons were measured for polymers with a crystalline

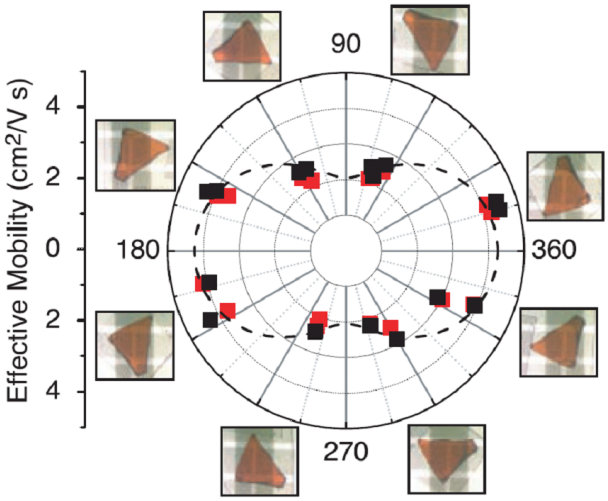

Figure 2.3: *Polar plot of the mobility at the rubrene a-b surface (angle measured between the b axis and the conducting channel). The linear and saturation mobilities (black and red squares, respectively) are similar and are seen to be coincident after each full* $360\,^\circ$ *rotation. The maximum and the minimum mobility values occur along b and a axis, respectively. The dotted line shows the fitted in-plane transformation of the mobility tensor (from Sundar et al. [22]).*

microstructure and rather complicated repeat units [32, 30].

Small molecules semiconductors are deposited from solution if they are soluble or have a soluble precursor. High apparent mobilities are achieved by using liquid crystalline molecules or soluble precursors of high-mobility semiconductors. In the precursor route, the semiconducting film is formed of a soluble precursor on a substrate with subsequent thermal or irradiative conversion into the fully conjugated form. Pentacene precursors yield apparent mobilities in the range of $0.8 - 1 cm^2/Vs$ after thermal conversion [33, 34]. *TIPS*-pentacene is an example for a small molecule with a bulky side chain which shows good molecular ordering [35]. The molecular ordering depends on the solvent and on the film deposition technique. Apparent mobilities greater than $1 cm^2/Vs$ are achieved in an OFET drop casted from a toluene solution.

2.2 Charge transport in organic semiconductors

The organic semiconductor is the heart of the organic transistor. The material's properties and the processing influence the performance of the transistor. The charge transport depends on the chemical structure and the order in the organic semiconductor. The basic models are introduced in the following section.

2.2.1 Semiconduction in crystals made of small molecules

In organic materials, conduction occurs when carriers are available and can be transferred from molecule to molecule. Relatively high transfer integrals can be found in organic molecules having electrons in π-orbitals. The π-orbitals result from the sp^2 hybridization of the atomic orbitals of a C atom. In a molecule containing π-orbitals and in the absence of strong electron-phonon interactions or strong disorder, the π-electrons are delocalized over the whole molecule. In organic semiconductors such as acenes or rubrene, the carriers (essentially delocalized over the whole molecule) are transferred from molecule to molecules thanks to transfer integrals on the order of $100meV$ or less [36, 37].
Pentacene and rubrene crystallize in a herringbone pattern (see Fig. 2.4 and 2.5). Their bare transfer integrals determined by quantum chemistry calculations are 100 and $85meV$ in the highest mobility direction, respectively [14, 38, 39].

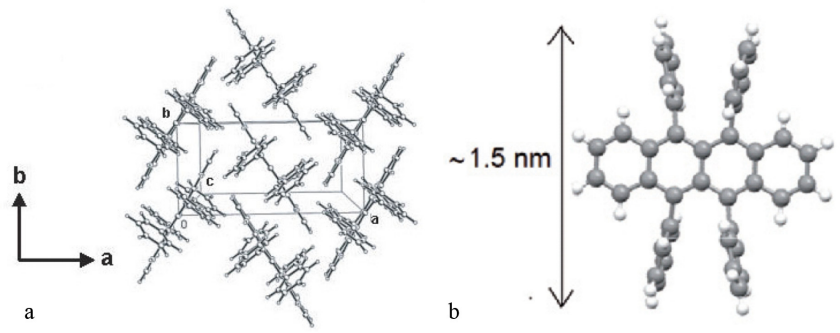

Figure 2.4: *a) The crystal structure of rubrene and b) its molecular structure (from De Boer et al. and Hasegawa et al. [17, 40]).*

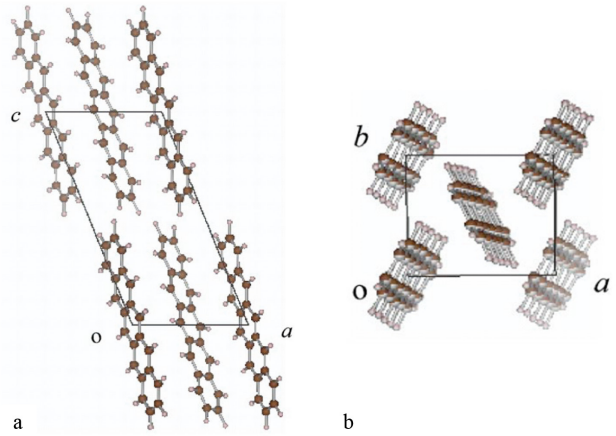

Figure 2.5: *The crystal structure of pentacene a) from side view and b) top view (from Yoshida et al. [41]).*

2.2.2 Charge transport in an organic single crystal

The mobility of ultrapure organic crystals reaches values around $10 cm^2/Vs$ at room temperature and several hundred cm^2/Vs at low temperature. They were determined by time-of-flight measurements [42]. The mobility is usually more or less anisotropic and increases upon cooling (by a power law: $\mu \propto T^{-n}$, see Fig. 2.6 for perylene and naphthalene). At lower temperatures, the mobility can decrease due to impurities or defects in the single crystal (trapping effects, see Fig. 2.6a).

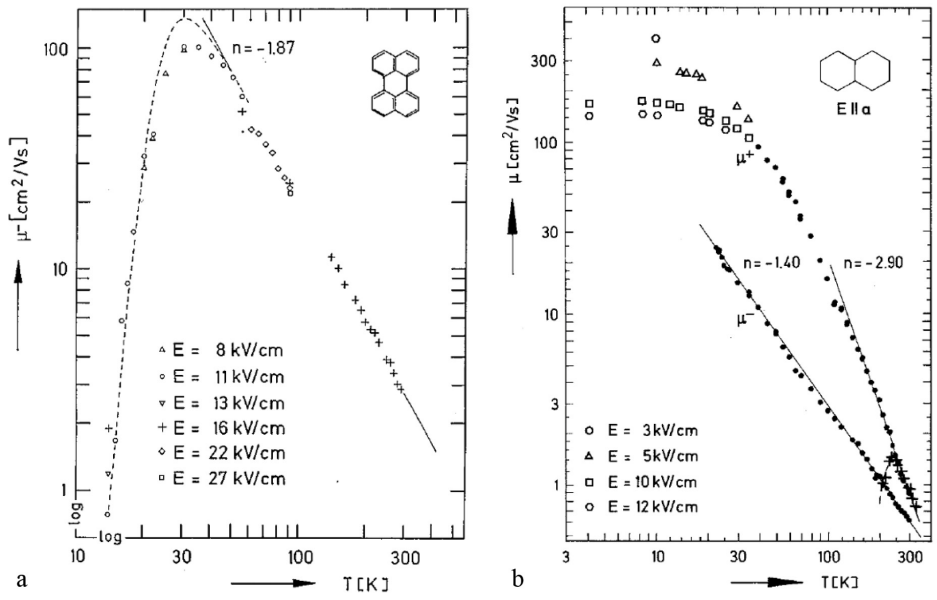

Figure 2.6: *Time-of-flight experiments: a) Electron mobilities in perylene for the electric field parallel to the crystallographic a axis and b) electron and hole mobilities in naphthalene for the electric field parallel to the crystallographic a axis (from Warta et al. [43]).*

Earlier, it was thought that the charge transport in the organic semiconductor occurs by band conduction modified by electron-phonon interactions. But the reality is more complicated because the charge carriers are not only dressed with a cloud of phonons but also with a cloud of molecular polarization.
Organic semiconductors are highly polarizable molecules (polarization energies of about $1eV$). If there is a charge carrier present on a molecular site, a polarization field establishes much faster than the carrier is transported to a neighboring molecular site. As consequence, the effective mass of the charge carrier is increased due to the formation of what is generally called a Coulomb or electronic polaron (see Fig. 2.77) [44, 45, 46].

The time scale of the different interactions determines the carrier behavior. As reference, we use the transfer integral (about 100meV) through the characteristic time of Bloch wave formation (h/J) on the order of $4 \cdot 10^{-14} s$ (see Fig. 2.8). Faster interactions such as molecular electric polarization and high-frequency intramolecular phonon modes reduce the effective transfer integrals by increasing the effective

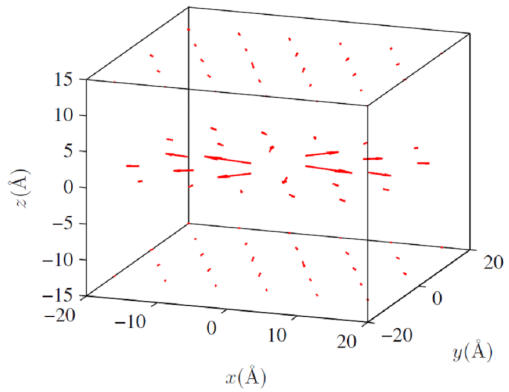

Figure 2.7: *Coulomb polaron in bulk rubrene. The carrier is located at the origin (z=0) in the high-mobility plane (a,b). The interlayer spacing is* 13.4Å *(from Konezny et al. [14]).*

mass. Slow interactions such as intermolecular phonons and trapping effects lead to a dynamical localization of the charge carrier.

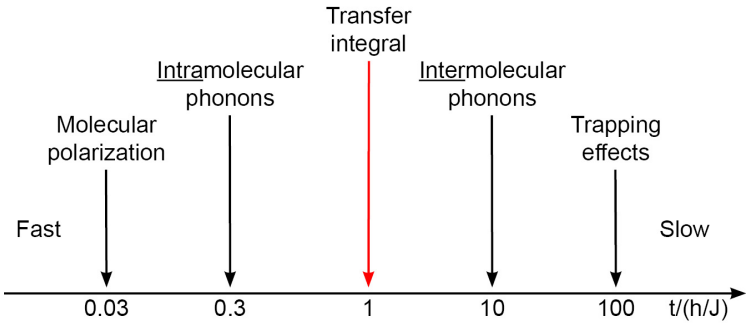

Figure 2.8: *Time scales for the different interactions relative to the characteristic time of Bloch wave formation (h/J) taken as one.*

In other words, the thermal disorder in the lattice is converted into transfer integral fluctuations and polarization fluctuations which in turn drive the carrier motion [47, 48]. That means that the charge carrier is localized in a certain landscape, but the landscape moves slowly and the charge carrier is forced to follow this motion.

2.3 In the channel of an organic transistor

The carriers that we study in the present work are confined to the channel of organic field-effect transistors. The transport in such a channel can be rather different than the transport in the perfect and bulk crystal. The carriers indeed travel in a plane of the organic semiconductor but close to the surface of a gate dielectric which is a good insulator, either an oxide or a polymer. Three different effects can result from this neighborhood: i) especially in the oxide case, the charge is coupled electrically

to the phonon modes of the dielectric; this results in the formation of a Fröhlich polaron [46, 25, 49]; ii) the charge can be trapped at numerous electroactive defects (charges and dipoles) of the dielectric surface [25, 14, 40] and iii) charge carriers can be introduced by a direct reaction of the semiconductor with a defect on the dielectric surface (charge transfer) [50].
For a charge transport in the channel, charge carriers have to be injected and extracted at the source and drain contact, respectively. The charge flow can be perturbed by several effects: i) the Schottky barrier which is formed at the contact-semiconductor interface, ii) drift/diffusion processes in the semiconductor film and iii) the access path from the contacts to the conducting film.
For organic thin-film transistors, the semiconductor layer has another structure than a bulk single crystal. The film morphology is determined by the dielectric surface and the deposition conditions and may affect the charge transport in the channel. The aspects of the dielectric, the contacts and the film morphology are discussed in the following.

2.3.1 The dielectric

The quality of the dielectric film determines the performance of the OTFT. Electroactive defects on the surface can disturb the charge transport in the conducting channel by acting as traps or charge transfer centers.

Trapping Traps capture charge carriers in the channel. If the trap depth is within a few k_BT (a shallow trap), the charge carrier is thermally released after a certain time and it travels further until it is trapped again. Only the free charge carriers contribute to the current thus the apparent mobility is reduced. This procedure is called multiple trapping and release (MTR). The simplest possible expression of the mobility was given by Hoesterey and Letson for a single trap population in atomic concentration c:

$$\mu = \frac{\mu_0}{1 + c \cdot exp\,(E_{trap}/k_BT)} \tag{2.3}$$

where μ_0 is the trap-free mobility, E_{trap} the trap depth, k_B the Boltzmann constant and T the absolute temperature [51].

For a carrier in the channel of an OFET, the charge polarizes the gate insulator in addition to the organic semiconductor (Fröhlich polaron, see Fig. 2.9). Polarization effects strongly affect the trap-limited transport, because when the carrier flies from a trap to another, it is only sensitive to the optical dielectric constants of the medium (ϵ_∞) while when the carrier waits at a trap site the static dielectric constant ϵ_S is involved. Then the trap depth is related to the difference in polarization energy between the trapped (long-lived) and the free (short-lived) state. In these conditions, the trap depth increases with the dielectric constant of the gate dielectric (see Fig. 2.10a) [14].

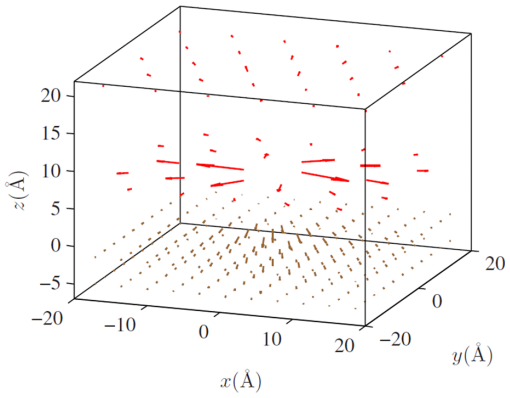

Figure 2.9: *Induced cloud of polarization due to a hole in rubrene at z=6.7Å close to a Ta_2O_5 interface at z=0 (Fröhlich polaron). The induced dipoles in the oxide (z<0) are magnified by a factor of 5 relative to those in rubrene (z>0) (from Konezny et al. [14]).*

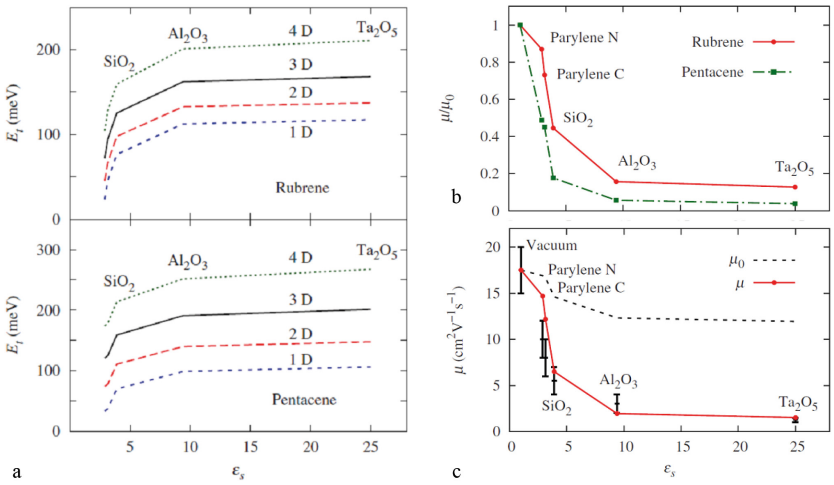

Figure 2.10: *a) Hole trap depth in rubrene and pentacene transistors due to an interface defect dipole as a function of the static dielectric constant of the gate dielectric for various dipole strengths from 1 to 4D, b) mobility reduction factor μ/μ_0 due to trapping effects in the channel of rubrene and pentacene OFETs as a function of the gate dielectric constant, and c) trap-free mobility μ_0 and trap-controlled mobility μ as functions of the gate dielectric constant. The theoretical curves are from Konezny et al. and the experimental points obtained in single-crystalline rubrene transistors are from Hulea et al. [14, 25].*

The apparent mobility depends on two ways in the dielectric constant of the gate dielectric. On one hand, it increases the effective mass of the charge carriers what decreases the transfer integral (coupling effect, see μ_0 in Fig. 2.10c). On the other hand, it changes the trap depth (trapping effect). Consequently, the apparent mobility strongly decreases with increasing dielectric constant.
The present work concerns thin-film transistors in the channel of which the mobility is always lower than $1cm^2/Vs$. In these cases, the channel is always disordered enough to promote conduction mechanisms such as trap and release or hopping.

Besides shallow traps where the thermal energy is sufficient for a release, there are deep traps which capture a charge carrier permanently. Then the threshold voltage is shifted to negative values. The apparent mobility is not affected by this type of traps [23].

Traps are very often present in the organic transistor even at the surface of single crystalline devices. They result from structural and chemical defects in the organic semiconductor and at the interface to the dielectric. The trap density in rubrene single-crystal transistors for example is $10^{10}cm^{-2}$ in the organic semiconductor (air-gap transistor) and $10^{12}cm^{-2}$ at the rubrene single crystal/SiO_2 interface [23, 52]. Traps can be introduced by exposure to X-rays, light, oxygen, moisture or gate bias stress [23, 53, 54, 55].

Charge transfer The other important process which can occur at the dielectric-semiconductor interface is the introduction of additional charges by charge transfer. When a defect on the dielectric surface reacts with a semiconductor molecule, it transfers a charge into the semiconductor near the interface (see Fig. 2.11 for pentacene). The transferred charges, called residual carriers in the following, are present in the semiconductor and form a conducting channel before a gate field is applied. Thus current flows if a source-drain voltage is applied even at zero gate fields, i.e. the transistor is on. To turn the transistor off, a positive gate voltage has to be applied; hence the threshold voltage is positive.

At high residual carrier concentrations, positive threshold voltages are proportional to the residual carrier density:

$$V_T = \frac{P_{res} \cdot |e|}{C_{gate}} \tag{2.4}$$

where P_{res} is the residual carrier density, e the electron charge and C_{gate} the capacitance of the gate dielectric per unit area [50].

The density of residual carrier can be calculated by the channel conductivity $\sigma_{channel}$ measured with a floating gate:

$$P_{res} = \frac{\sigma_{channel}}{\mu \cdot |e|} \tag{2.5}$$

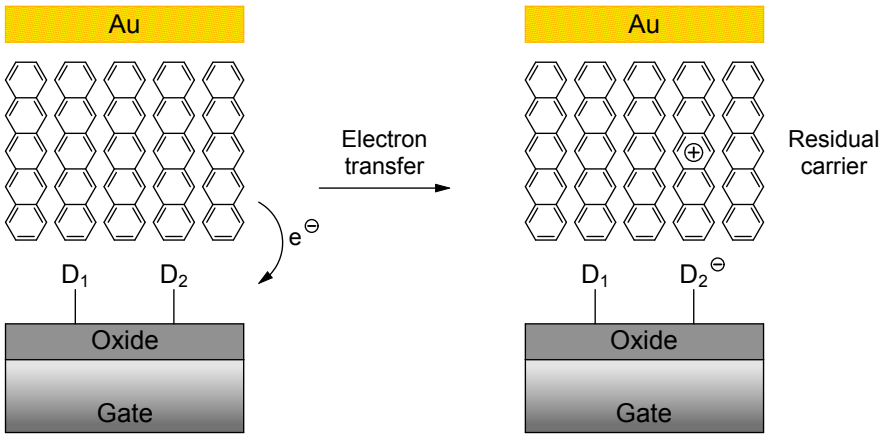

Figure 2.11: *Charge transfer at the dielectric-semiconductor interface: representation of the mechanism that produces charges (residual carriers) in the transistor channel by electron transfer from pentacene to specific defects on the oxide surface. The residual carrier is delocalized over several pentacene molecules.*

where μ is the mobility [50].

A charge transfer between a defect of the dielectric and the semiconductor is only probable if the energy level of the defect is close to the *HOMO* level of the semiconductor [56]. The defects which are responsible for a charge transfer are called charge transfer centers or recombination centers. The back reaction is not likely because the residual carrier is delocalized and the energy levels shift due to polarization energies of both the charged defect and the charged semiconductor molecule. If a charge transfer between a defect and semiconductor is probable, it occurs during the semiconductor deposition when the molecules arrive at the surface. The charged defects and dipoles on the dielectric surface can act as traps for charge carriers in the channel.

The residual carriers also affect the mobility. At elevated densities, the residual carriers screen the traps at the dielectric-semiconductor interface; thus the mobility increases with the residual carrier density. At low densities, it is vice versa. The fewer residual carriers are in the channel, the fewer charged defects are formed on the dielectric surface which act as traps. Consequently, the mobility increases with decreasing residual carrier density [57].

Similar to traps, charge transfer centers can be introduced on the dielectric surface. Surface treatment prior to the semiconductor deposition change the defect density and distribution what may form charge transfer centers. In pentacene thin-film transistors, an oxygen plasma treatment of the SiO_2 dielectric surface e.g. leads to a shift in threshold caused by residual carriers [50].

The nature and the role of the defects on the dielectric surface are one of the topics of this thesis; they were analyzed on OTFTs containing silicon oxide (SiO_2) or polyimide (PI) as dielectric (see Chapter 6). The dielectric surfaces are treated

by plasma and pH solutions for varying the defect densities.

Self-assembled monolayers The trapping and charge transfer processes can be reduced by structuring the dielectric layer (e.g. bilayers or nanocomposites) or by passivating it with a self-assembled monolayer [15, 58, 59, 60, 61, 62, 63, 64]. The SAM covers the defects and separates the dielectric from the semiconductor, thereby enhancing transistor performance (i.e. an increase in the apparent mobility, the on/off ratio and a small negative threshold) [61, 62]. The self-assembled monolayer increases apparent mobility by decoupling the semiconductor from the dielectric surface [65]. The most used monolayers are *OTS* (octadecyltriclorosilane) and *HMDS* (hexylmethyldisilozane) [61, 62, 63]. In general, these monolayers are so thin compared to the dielectric layer that the gate field is not drastically varied. The SAM acts as an energy barrier against charge transfer between the dielectric and the semiconductor; this occurs by tunneling through the monolayer [66]. Tunneling probability depends on length of aliphatic chain in the SAM. The longer the chain, the smaller tunneling probability and thus charge transfer through the SAM [67, 68, 69, 70]. There is an optimal chain length for aliphatic SAM. If the chains are too long, they are folded. The order and the density in the monolayer is reduced and the passivation effect decreased.

The performance of an organic transistor containing a monolayer strongly depends on the type of SAM which is used [18, 71, 72, 73]. The length and the chemical nature of the SAM molecules determine the effect of the SAM. Fluorinated end groups lead to a threshold shift to positive values [64, 72, 71, 74]. An NH_2 end group brings on low apparent mobility and a negative threshold [71]. The SAM covers the charge transfer centers on the dielectric surface but it can also introduce new ones. In general, that should be avoided but it can be used to control the threshold shift [75].
Due to the modified dielectric surface, the semiconductor growth on the dielectric can be changed. But in general, changes in film morphology do not dominate transistor performance [56, 72].

An alternative to bulky oxide or polymeric dielectrics are self-assembled monolayers (SAM) which are used directly as dielectric layer [76, 77]. They are thin and well-ordered what increases the capacitance of the dielectric drastically. The performance of a SAM dielectric is limited by leakage currents resulting from tunneling through the monolayer or disorder in the structure. A step further is the use of self-assembled multilayers (SAMT) to form three-dimensional crosslinked dielectrics in solution [78]. The SAMT contains highly π-polarizable dipolar layers, which enhances the dielectric constant, and preserves excellent insulator properties by crosslinked intermediate layers.

The effects of a SAM, especially the ones which carry a dipole moment, are discussed in Chapter 7.

2.3.2 Contacts

In an OFET, the charge carriers are injected and extracted at the source and drain contact, respectively. If the charge carriers are in the semiconductor, they have to be transported from the contacts to the conducting channel. All processes which hinder the injection, extraction or charge transport between the contacts and the channel are summed under the term of contact resistance (contact resistivity). This resistance is not constant and depends on the gate voltage. In an optimal transistor, the contact contribution is small (compared to the channel contribution), i.e. the performance is not limited by the contacts.

The contact resistance arises from different parts of the organic transistor: i) from the contact-semiconductor interface where a Schottky barrier is formed, ii) from the semiconductor region in the vicinity of the contacts where the charge carriers move by drift/diffusion and iii) from the semiconductor between the contacts and the conducting channel through which the charge carriers have to be transported (access path) (see Fig. 2.12).

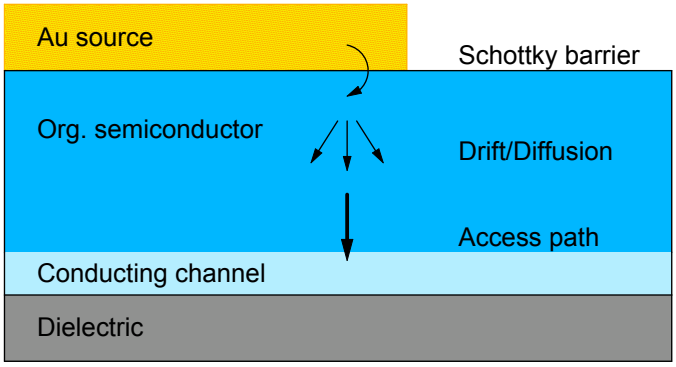

Figure 2.12: *The contributions to the contact resistance for charge carriers injected at the gold contact and transported through the organic semiconductor to the conducting channel.*

At the contact-semiconductor interface, a Schottky barrier is formed (see Fig. 2.13 for Au and pentacene). For a *p*-type semiconductor (as pentacene is normally used), the holes are injected into the *HOMO* level (electrons into the *LUMO* level in n-type semiconductors). The barrier height depends on the work function of the metal and the *HOMO*/*LUMO* level of the organic semiconductor. The applied gate field lowers the barrier height and facilitates the injection/extraction of charge carriers. In a weakly coupled system (e.g. oxidized Cu contacts and a rubrene single crystal), the charge injection and extraction can be modeled by the thermionic emission of two oppositely biased Schottky diodes (the bias-induced barrier lowering included) [79].

Tuning the work function of a contact metal is possible with a dipolar SAM on the surface demonstrated in OLED and bottom-contact OTFTs [81, 82, 83, 84].

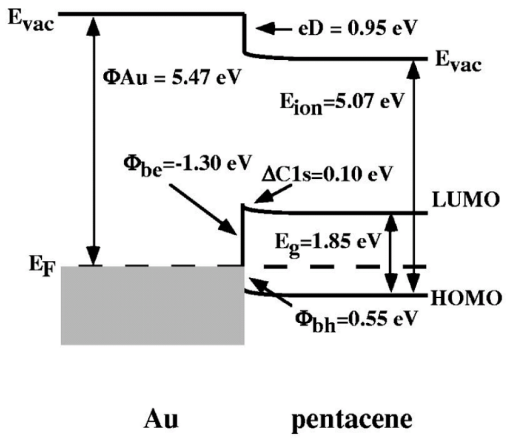

Figure 2.13: *Contact barrier at the gold-pentacene interface (measured by Schroeder et al. [80]).*

After injection, the charge carriers are near the contacts and have to travel towards the conducting channel. The drift/diffusion in the organic semiconductor near the contacts becomes important. If the drift/diffusion is slow, a space-charge field establishes and the charge injection rate is reduced. The density of injected charge carriers is then determined by the drift/diffusion in the semiconductor film [85, 86]. How fast a charge carrier is transported depends on the mobility of the semiconductor film. The higher the mobility is, the faster the charge carrier is in the channel and the smaller the contact resistance is.

The third contribution to the contact resistance is related to the access path from the contacts to the conducting channel. The access resistance is important in top-contact OTFTs where it increases with the film thickness [86]. The film morphology may influence the contact behavior by introducing disorder in the semiconductor near the contacts [11, 87].

The contact resistance is studied on OTFTs where the pentacene film has a thickness ranging from 10 to 80nm and the channel length ranging from 2 to 600μm (see Chapter 5).

2.3.3 Film morphology

The thin-film morphology of the organic semiconductor depends on the substrate surface and the processing. In thermal evaporated films, the film growth is determined by the deposition rate and the substrate temperature during deposition [88, 89]. In solution-processed depositions, the solution concentration and annealing steps change the morphology [90]. For both deposition processes, the substrate surface strongly affects the thin film growth, especially when it is treated before deposition, e.g. by a self-assembled monolayer (SAM) [89, 90, 91]. This dependence can be observed in bottom-contact transistors where the semiconductor growth is affected by the different surfaces of the contacts and the dielectric [11]. Often abrupt

changes in the film morphology are reduced by modify either the contacts or the dielectric by a SAM [92, 93, 94].

For organic thin-film transistors based on a pentacene film deposited in vacuum, there are ambiguous reports about the correlation of the film morphology and the transistor performance. On one hand, it is shown that the performance depends on the film morphology, especially on the grain size [16, 61, 62]. On the other hand, trapping or charge transfer processes at the dielectric-pentacene interface often are more important than the film morphology [56, 72].

The growth and morphology of the pentacene film on different treated and untreated SiO_2 and PI surfaces is discussed in Chapter 4. The influence of the morphology on the OTFT performance is studied for various film thicknesses and grain sizes and for surface treated SiO_2 and PI in Chapter 5 and 6.

In this chapter, we saw in many examples that the performance of an organic thin-film transistor does not only depend on the properties of the chosen materials but often also on the interaction between the different layers. The processing can strongly affect the behavior of the final transistor. This thesis is focused on the effects related to the interface between the dielectric and the organic semiconductor. Before we dive into the analysis of the different organic thin-film transistors, the fabrication and the characterization methods are explained.

Chapter 3

Fabrication & Characterization

The purpose of the present work is to study the consequences of interface modifications and device geometry on transistor performance. To this end, we decided to use primarily a transistor based on pentacene thin films with an oxide gate dielectric (SiO_2) and gold top contacts (see Fig. 3.1). Pentacene is a well-performing organic semiconductor used for thin-film transistors that can reach apparent mobilities in the range of $1cm^2/Vs$, the maximum value is $5.5cm^2/Vs$ [26, 95]. For ultrathin films (5 to 25nm), the pentacene growth has been studied extensively on oxide dielectrics [88, 89, 96]. High film quality is achieved repeatedly by optimized conditions during deposition by thermal evaporation. The top contacts are chosen to avoid morphology changes near the channel [11]. Moreover, in ultrathin-film transistors, the distance between the contact (where the charge carriers are injected or extracted) and the channel is short; therefore, the access resistance is small and does not disturb transistor performance.

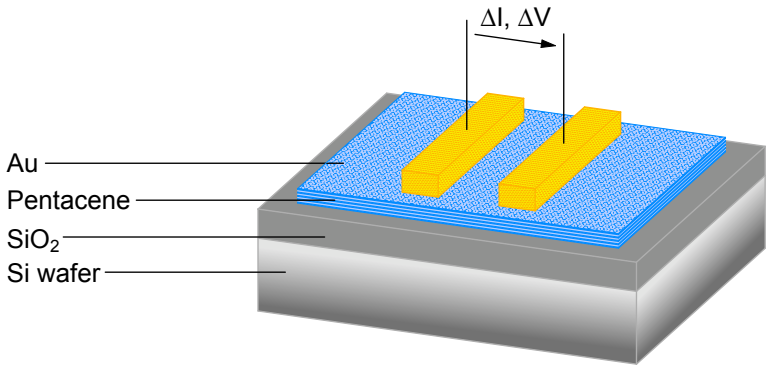

Figure 3.1: *Architecture of an organic thin-film transistor based on pentacene and with gold top contacts.*

The channel length of the thin-film transistors is in general $600\mu m$, while the channel width is $6mm$. Such a long-channel configuration is chosen to minimize the contribution of the contacts to the total resistance; i.e., the OTFT performance is dominated by the channel and not contact-limited. Some transistors were prepared with two additional contacts for separating the performance of the channel and the

contacts by comparing 2 and 4-probe measurements.
To study the effect of the contacts, we also fabricated OTFTs with channel lengths down to $2\mu m$ (aspect ratio of 10 or 20).

Thermal SiO_2 is chosen as the dielectric layer. SiO_2 has a low dielectric constant compared to other oxide dielectrics and this reduces the coupling of the charge carriers to the phonon modes of the oxide [14, 25]. Moreover, the surface of SiO_2 has been widely investigated in relation to classical silicon field-effect transistors. The surface defects on SiO_2 are well-known, especially after surface treatments. It is thus possible to analyze the effect of particular defect species on the transistor behavior. If the SiO_2 is formed on a Si wafer, the doped Si wafer can be used as substrate and gate contact.
In order to reduce the effects of carrier trapping, oxide dielectric surfaces are often covered with a self-assembled monolayer (SAM) [57, 61, 62, 63, 77]. To analyze the effect of a SAM at the pentacene-dielectric interface, a nonpolar SAm and a series of polar SAMs were introduced. The SAMs are deposited by thermal evaporation (according to a method developed by Nüesch et al [81]) to improve the monolayer quality and to avoid solvent molecules in the final monolayer.

Gold has been chosen as a contact material because it shows good performance as thermal evaporated top contacts in pentacene OTFT - even if there now exist better solutions for organic transistors [11, 12]; it is evaporated through a shadow mask on the top of the pentacene film at a substrate temperature of $-185\,^{\circ}\mathrm{C}$ to avoid diffusion into the pentacene film. For the short-channel transistors (channel lengths ranging from 2 to $20\mu m$), the stencil technique is used to define the contacts; this is a one-step technique with high resolution down to the sub-100nm range that eliminates solvent based processing steps [97, 98].

Further to the oxide dielectric (SiO_2), polyimide (PI) was used as polymeric dielectric. The PI film is spin-coated on the top of a Si wafer with a native oxide layer.

Presented in this chapter are the most important aspects of the fabrication procedures, film and contact deposition, a description of the most important surface treatment methods, a discussion of the AFM characterization of the pentacene films, and the validity of the electrical measurement procedures.

3.1 Pentacene thin film deposition

Pentacene was purchased from *Sigma-Aldrich* and twice purified in a furnace with a controlled temperature gradient to increase the purity. Pentacene was deposited by thermal evaporation under high vacuum ($< 10^{-6} mbar$). At the beginning, the rate was low ($0.2nm/min$) for slowly growing the first layers because the conducting channel in the pentacene film will be located close to the dielectric-pentacene interface. After a few nanometers were deposited, the rate was increased (up to $1nm/min$).
The substrate temperature was $55\,^{\circ}\mathrm{C}$ during the pentacene deposition, resulting in a

large grain size in the range of 5-8μm (in ultrathin films on SiO_2). For studying the effect of the film morphology, the substrate temperature was reduced to 20 °C (RT) to obtain grains with a size of 2-3μm (in ultrathin films on SiO_2). If the pentacene film is not continuous at 55 °C, the substrate temperature is also reduced to RT.

3.2 Contact patterning

The source and drain gold contacts were deposited on the top of the pentacene film by thermal evaporation through a shadow mask. The substrate temperature was held at −185 °C by cooling the substrate with liquid nitrogen during the evaporation, thereby avoiding the diffusion of gold molecules onto the pentacene film.
Transistors with a long channel are patterned by a steel shadow mask and have a channel length of 100, 200 or 600μm and a channel width of 6mm (see Fig. 3.2c). The short-channel transistors have a channel length of 2, 5, 10 or 20μm and an aspect ratio of 10 or 20; they are patterned by stencil masks made of a low-stress SiN membrane supported by bulk Si (see Fig. 3.2a, b and d). The stencil masks were fabricated by K. Sidler from the *Microsystems Laboratory 1* (Prof. J. Brugger, EPFL)[97]. An advantage of short-channel transistors is that the probability of a morphological discontinuity (from the pentacene or the dielectric layer) in the channel is lower than for long-channel transistors, especially if the grain size is in the same range as the channel length.
Some transistors (with short and long channels) were fabricated in a 4-probe configuration, thereby allowing for the measurement of the channel properties independent of the contacts (see Fig. 3.2c).

3.3 Surface treatments of the SiO_2 dielectric

To change the surface chemistry and defects, the SiO_2 dielectric surface was treated prior to the pentacene deposition. The surface treatments (plasma, pH solutions) affect both the pentacene film growth and the transistor performance [56]. Changes in the growth kinetics can be related to changes in the wettability of the surface, while mobility changes in the transfer properties result from changes in the trap distribution at the interface; in particular, charge transfer reactions appear at the interface in certain conditions.
The plasma treatments were performed at a bias voltage of $-65V$, a radio frequency power of 10W, and a constant gas pressure of $10^{-3}mbar$ with argon, oxygen and formier gas (8% of H_2 in N_2). The plasma treatments lasted two minutes and occurred immediately before pentacene was deposited.
By immersing the substrates in solutions of different pH, the ratio of -Si-OH/-Si-O^- is varied. The pH solutions consisted of ultrapure water, $NaOH$ for basic and HCl for acidic solutions, respectively. The SiO_2 substrates were immersed into the solution between 10-15s and afterwards dried by a nitrogen jet. Immediately after the pH treatment, the samples were placed into the vacuum chamber and evacuated.

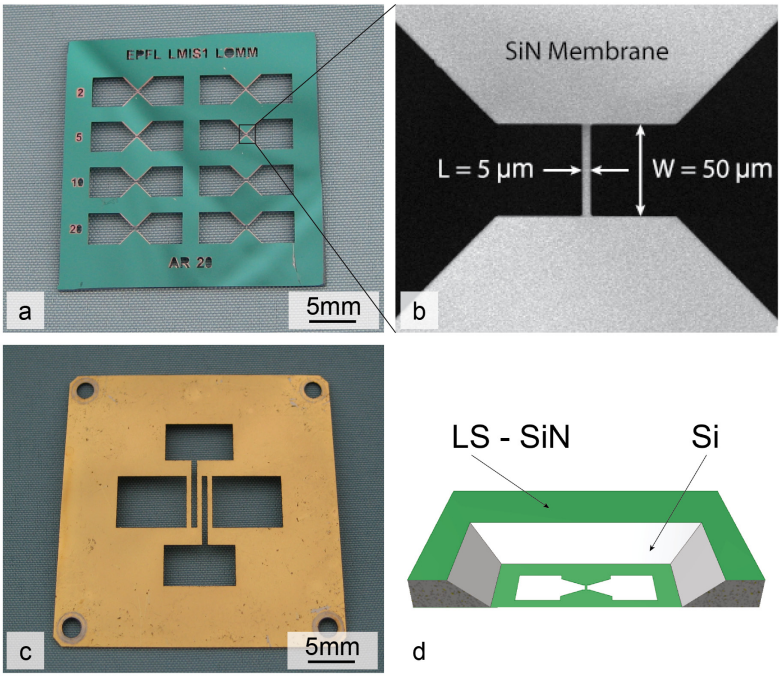

Figure 3.2: *a) Stencil mask with 8 transistors in 2-probe configuration with a channel length ranging from 2 to 20µm, b) SEM image of stencil mask for a transistor with a channel length of 5µm, c) steel shadow mask for a transistor in 4-probe configuration with a channel length of 600µm, d) schematic cross-section of a stencil mask made of a low-stress SiN membrane supported by bulk Si.*

3.4 Self-assembled monolayers

We modified the dielectric surface by self-assembled monolayers (SAMs). The neutral SAM contains an aliphatic chain. As polar SAMs, we used a series of benzoic acid derivatives. They have different end groups in the *para*-position of the benzoic acid and thus different dipole moments (see Fig. 3.3); they have, however, similar lengths and the same carboxylate grafting system.

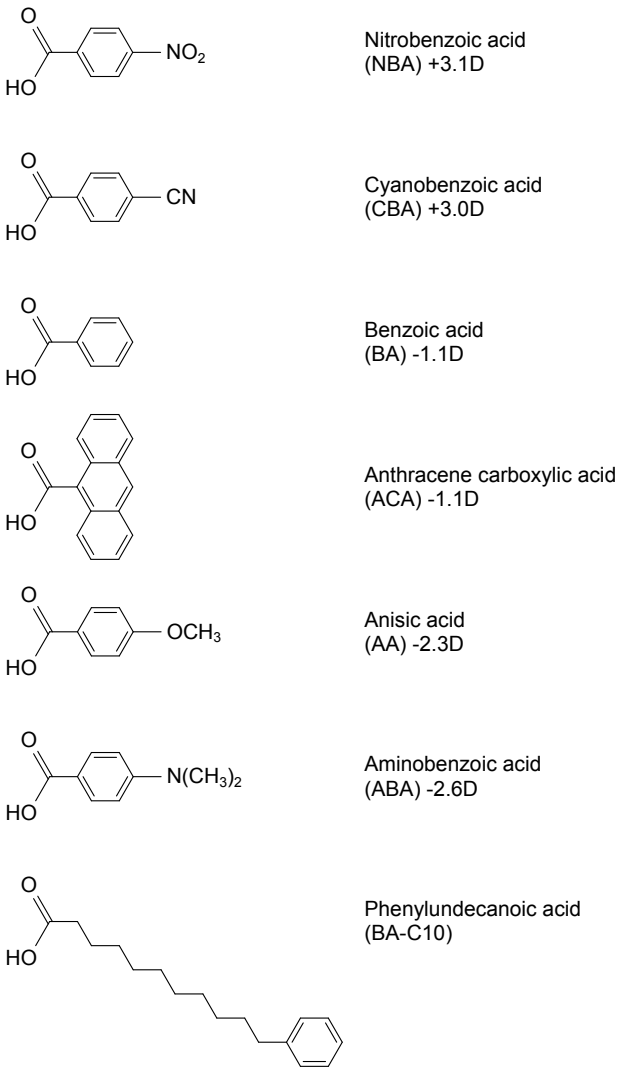

Figure 3.3: *Molecules used to form the self-assembled monolayers on the top of the oxide dielectric.*

The SAM is deposited by thermal evaporation under the same conditions as pentacene (method according to Nüesch et al. [81]). For grafting, a thin Al_2O_3 layer is required which is deposited by radio-frequency magnetron sputtering ($100W$, $-280V$, $8 \cdot 10^{-3}mbar$) on SiO_2 and has a thickness of $7nm$. The grafting occurs by the deprotonation of the acid group on the Al_2O_3, after being activated by an O_2 plasma

($10W$, $-70V$, $10^{-1}mbar$) [82] (see Fig. 3.4). In the first 10 minutes after the O_2 plasma irradiation, the main active defects are oxygen radicals what facilitate the grafting of the carboxylate groups [56]. The SAMs were deposited within these 10 minutes. To have only a monolayer on the dielectric, the ungrafted molecules are left to desorb for 30min prior to the pentacene deposition.

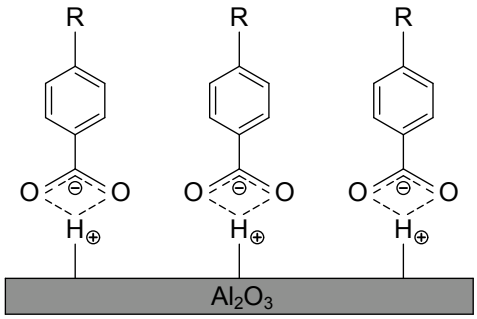

Figure 3.4: *Grafting reaction of the self-assembled monolayer on the plasma-activated oxide.*

3.5 Polymer dielectric

Beside the oxide dielectric, transistors with a polymeric dielectric were analyzed. A cyclic polyimide (PI) from the *Pyralin PI2610* series is used (purchased at *HD MicroSystems*). PI has a smaller dielectric constant decreasing the field effect and the carrier coupling effects. The PI films were prepared by K. Sidler (Prof. J. Brugger, *LMIS1*, EPFL). For this purpose, $60wt\%$ *PI2610* dissolved in N-methyl-2-pyrrolidone (NMP) is spin-coated at a speed of 5000 rpm for $40s$ to define a $230nm$ thick PI dielectric. A Si wafer covered by a native oxide layer serves as substrate. The precursor film is thermally transformed into a PI film (see Fig. 3.5). The soft bake and the hard bake are carried out at 100 °C and 300 °C, respectively. Both soft and hard bakes are done in a N_2 environment.

Pentacene was deposited at RT on the polyimide dielectric because at 55 °C, isolated islands with no connection between each other were formed. Although a continuous pentacene film at RT was obtained, the film is more ragged and consists of sub-100nm grains compared to a pentacene film deposited under the same conditions on SiO_2. In some OTFTs, the surface chemistry of PI is modified by the same plasma treatments as SiO_2, except the duration was $10s$ instead of 2 minutes to avoid the degradation of the polymer surface.

3.6 Electrical characterization

The transistor performance was measured by recording the drain current I_D vs. the drain voltage V_D at a constant gate voltage V_G, i.e. the IV curves (output curves,

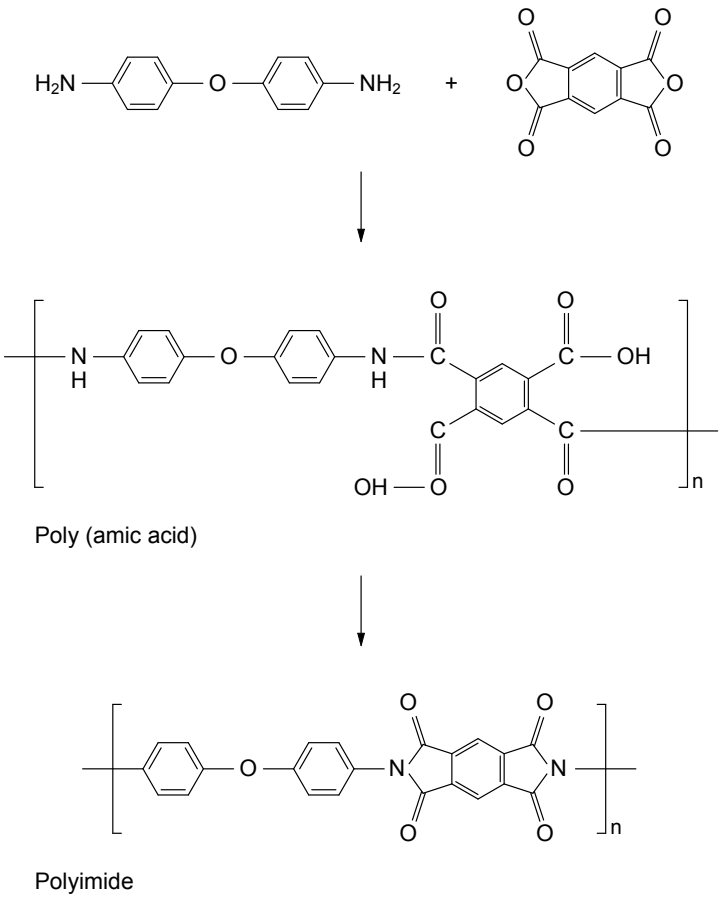

Figure 3.5: *The formation of poly (amic acid) and the transformation to polyimide.*

see Fig. 2.2a). The different regimes of the transistor performance and the behavior at zero and elevated gate voltage were scanned. From the conductance in the linear regime (the slope in $I_D(V_D)$ at $V_D = 0V$), the transfer curve is determined. The apparent mobility and the threshold voltage were calculated in the linear regime where only a few charge carriers are in the channel so the behavior of an isolated charge carrier is analyzed. The apparent mobility is determined by the slope in the transfer curve in the linear regime:

$$\mu_{app} = \frac{\partial g_D}{\partial V_G} \cdot \frac{L}{W} \cdot \frac{1}{C_{gate}} \; with \; g_D = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_D=0V} \tag{3.1}$$

where g_D is the channel conductance at $V_D = 0V$, V_D the drain voltage, I_D the drain current, V_G the gate voltage, L the channel length, W the channel width and C_{gate} the gate capacitance per unit area (see Fig. 3.6). The capacitance of the SiO_2 layer is $19.5nF/cm^2$, the one of the PI films is $11nF/cm^2$.

The threshold voltage is defined as the intersection between the gate voltage axis and the linear fit for elevated gate voltages (see Fig. 3.6) [99, 8].

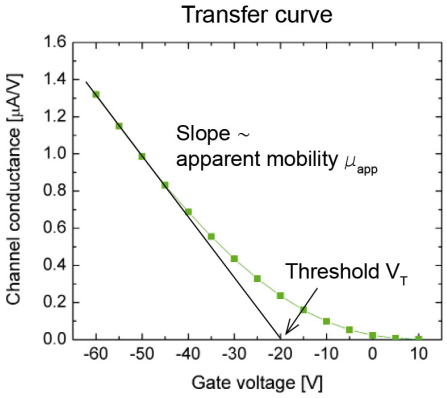

Figure 3.6: *A typical transfer curve with channel conductance g_D vs gate voltage V_G, showing the apparent mobility μ_{app} and threshold voltage V_{th}.*

The apparent mobility can also be determined in the saturation regime; then the square root of the absolute saturation drain current is plotted versus the gate voltage. The slope at elevated gate voltages is proportional to the apparent mobility in saturation:

$$\mu_{sat} = 2\left(\frac{\partial\sqrt{|I_{D,sat}|}}{\partial V_G}\right)^2 \cdot \frac{L}{W} \cdot \frac{1}{C_{gate}} \tag{3.2}$$

where $I_{D,sat}$ is the drain current if the output curve is saturated, i.e. at elevated drain voltages.

Theoretically, the apparent mobilities measured in the linear and saturation regime are identical, but they are sensitive to the trap distribution and the gate voltage and, therefore, are generally in good agreement within a factor of 2.

The difference of the apparent mobility in the linear regime versus one in saturation is shown for some examples in Table 3.1. Please notice, that we measure here apparent mobilities including contact effects. The contact resistance is not the same at high and low gate voltages.

Pentacene $[nm]$	Channel length $[\mu m]$	Dielectric	Apparent mobility (linear reg.) $[cm^2/Vs]$	Apparent mobility (saturation) $[cm^2/Vs]$	Ratio μ_{sat}/μ_{lin} $[-]$
10nm (55 °C)	$600\mu m$	SiO_2	0.17	0.14	0.81
20nm (RT)	$600\mu m$	SiO_2	0.23	0.18	0.77
20nm (55 °C)	$600\mu m$	SiO_2	0.42	0.36	0.85
40nm (RT)	$600\mu m$	SiO_2	0.71	0.56	0.78
40nm (55 °C)	$600\mu m$	SiO_2	0.72	0.60	0.83
80nm (RT)	$600\mu m$	SiO_2	0.30	0.12	0.38
20nm (RT)	$20\mu m$	SiO_2	0.70	0.62	0.89
20nm (55 °C)	$20\mu m$	SiO_2	0.95	0.98	1.03
40nm (RT)	$10\mu m$	SiO_2	1.33	1.11	0.83
40nm (55 °C)	$10\mu m$	SiO_2	1.69	1.79	1.06
80nm (RT)	$10\mu m$	SiO_2	0.98	0.56	0.59
5nm (55 °C)	$600\mu m$	BA	0.11	0.07	0.64
10nm (55 °C)	$600\mu m$	ACA	0.12	0.07	0.54
5nm (55 °C)	$600\mu m$	AA	0.12	0.07	0.58
5nm (55 °C)	$600\mu m$	ABA	0.05	0.03	0.50

Table 3.1: *Apparent mobility in linear and saturation regime for OTFTs on bare SiO_2 with different pentacene film thicknesses and substrate temperature during evaporation and OTFTs with a SAM modified oxide dielectric.*

The resistance of some of the transistors has been measured by 2 and 4 probes to separate the properties of the entire device and of the channel itself (see Fig. 3.1 and 3.7). The difference between the channel (measured by 4 probes) and the total resistance (measured by 2 probes) is the contribution of the contacts; these measurements were performed with a floating and non-floating gate. The transfer curves for the channel and the entire device are calculated from the measured resistance values at different gate voltages.

If current is flowing in the transistor at floating gate, charge carriers are already present in the semiconductor (before applying a gate field); they result from charge transfer reactions at the dielectric-pentacene interface and are called residual carriers [50]. The density of the residual carriers is approximated by:

$$P_{res} = \frac{\sigma_{channel}}{\mu_{app} \cdot |e|} \tag{3.3}$$

where $\sigma_{channel}$ is the film conductivity measured by 4 probes, μ_{app} the apparent mo-

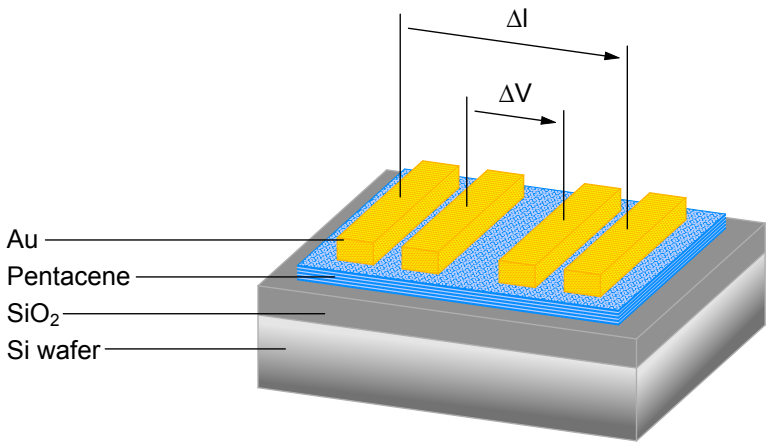

Figure 3.7: *Device architecture for conductivity measurement by 4 probes.*

bility and e the electron charge [50].

3.7 AFM images

The pentacene film morphology is imaged by an AFM (atomic force microscope, *SMENA* scanner, *NT-MDT*) in tapping mode. An overview of at least $30 \times 30 \mu m$ is taken before a typical region of the film is scanned in greater detail (see two examples in Fig. 3.8).

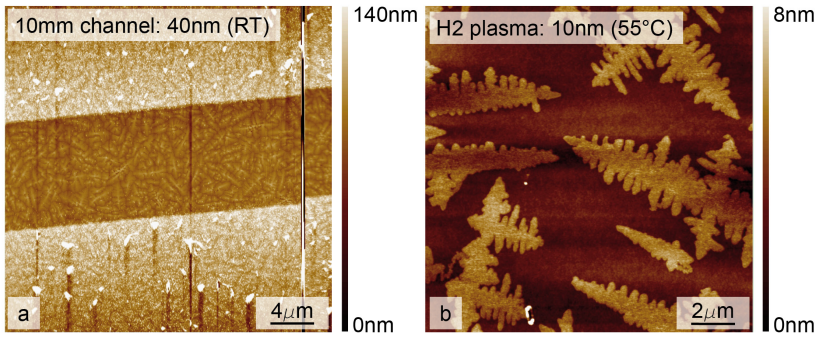

Figure 3.8: *AFM images of a) a 10µm channel with 40nm pentacene evaporated at RT on SiO_2 (defined by Au top contacts) and b) a 10nm-thin pentacene film evaporated at 55 °C on SiO_2 treated by H_2 plasma.*

3.8 Water contact angle

The wettability of the dielectric surface is measured by the water contact angle, which is related to the interfacial tensions between the solid, the liquid, and the gas phase (see Fig. 3.9). The smaller the angle is, the more hydrophilic the surface is.

The water contact angle of ultrapure water (*MilliPore*) was determined by the sessile drop method. One drop has the volume of $1.5\mu l$ and is measured 20 times within $5s$ (in average). For each sample, a minimum of six drops were analyzed at different locations.

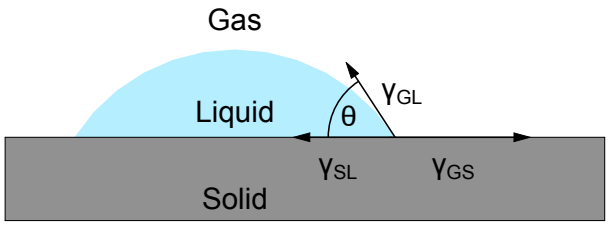

Figure 3.9: *Contact angle of a liquid droplet on a surface, θ is the contact angle, the interfacial tension between the solid and the liquid γ_{SL}, the gas and the solid γ_{GS} and the gas and the liquid γ_{GL}.*

The sample for the water contact angle measurements were fabricated by the same procedure as the corresponding OTFT, except that the fabrication was stopped before pentacene is deposited.

3.9 Conclusion

Organic thin-film transistors were fabricated based on pentacene with SiO_2 or PI dielectric and Au top contacts. The channel length ranged from 2 to $600\mu m$. Pentacene is deposited by thermal evaporation at different substrate temperatures and with different thicknesses. In some cases, the dielectric surface was modified by surface treatments. The OTFTs were analyzed by performance and conductivity measurements, the film morphology by AFM imaging.
Before we analyze the electrical performance of the transistors, we study the growth and morphology of the pentacene thin films in the next chapter.

Chapter 4

Growth & Morphology of Pentacene Thin Films

Pentacene crystallizes by aligning the molecules in their length axis resulting in a layered structure observable in the platelet-like shape of single crystals or the layers in an ultrathin film (see Fig. 4.1). Within one layer, the molecules are ordered in a herringbone pattern.

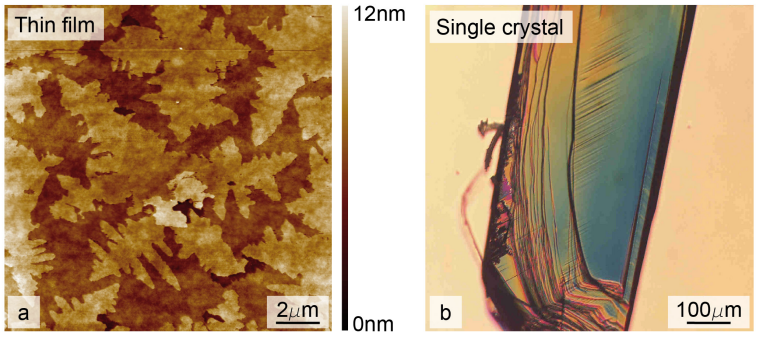

Figure 4.1: *a) AFM image of a pentacene thin film on SiO_2 (10nm in thickness, evaporated at 55 °C) and b) microscope image of a pentacene single crystal (with polarized light, from Ph. Bugnon, LOMM, EPFL).*

In bulk single crystals, the molecules are tilted by 22 ° (to the layer normal) and the interlayer distance is 14.1Å [100]. When pentacene is in the form of a thin film, several polymorphs have been identified, depending on the substrate, the substrate temperature, and the film thickness [100, 101, 41, 102]. The polymorphs differ in the interlayer distance and the tilting angles of the molecules to the layer normal and of the herringbone pattern; they are not necessarily equilibrium structures. In the thin-film phase, the molecules are almost upright on the surface and the interlayer distance is increased (see Fig. 4.2 left) [100, 102]).

The nucleation and growth of the pentacene film are also influenced by the substrate material and the substrate temperature during pentacene deposition. In addition, the nucleation density and thus the final grain size depends on the deposition

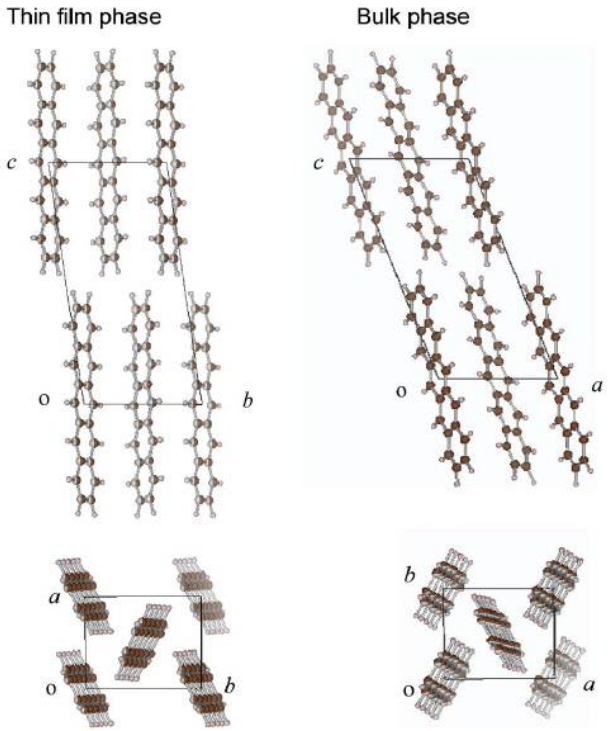

Figure 4.2: *The structure of the thin film phase (left) and the bulk phase (right) of pentacene (from Yoshida et al. [41]).*

rate.
In this chapter, we analyze the pentacene thin film growth and the morphology of the final film on the top of the dielectric layer. The effects of surface treatments and the dielectric material are studied using AFM imaging and water contact angle measurements.

4.1 Nucleation and growth of a pentacene film

The nucleation and growth of pentacene are determined by the substrate material and the deposition conditions. The nucleation density of pentacene islands depends on the deposition rate and the substrate temperature during evaporation [88, 89]. The number of pentacene islands per unit area increases if the deposition rate increases (see Fig. 4.3a). Consequently, the grain size is larger in a slowly deposited pentacene film. The substrate temperature has a reversed effect; if the substrate temperature increases, the nucleation density decreases (see Fig. 4.3b). On SiO_2 and Al_2O_3, the structure is highly dendritic at low deposition rates and becomes less ramified at higher deposition rates [89]. On *PMMA*, the nucleation density is higher and the islands are more compact.
In addition, the apparent coverage of the surface varies due to the effect of reevaporation during nucleation and growth: the effective film thickness decreases as the substrate temperature increases and the deposition rate decreases. Reevaporation is

more important on SiO_2 than on *PMMA* [89].
To achieve pentacene films with different grain sizes, the substrate temperature was held at RT and 55 °C resulting in small and large grains, respectively. In both cases, the evaporation rate is about $0.2nm/min$ at the beginning and increases to $1nm/min$ after the first few layers.

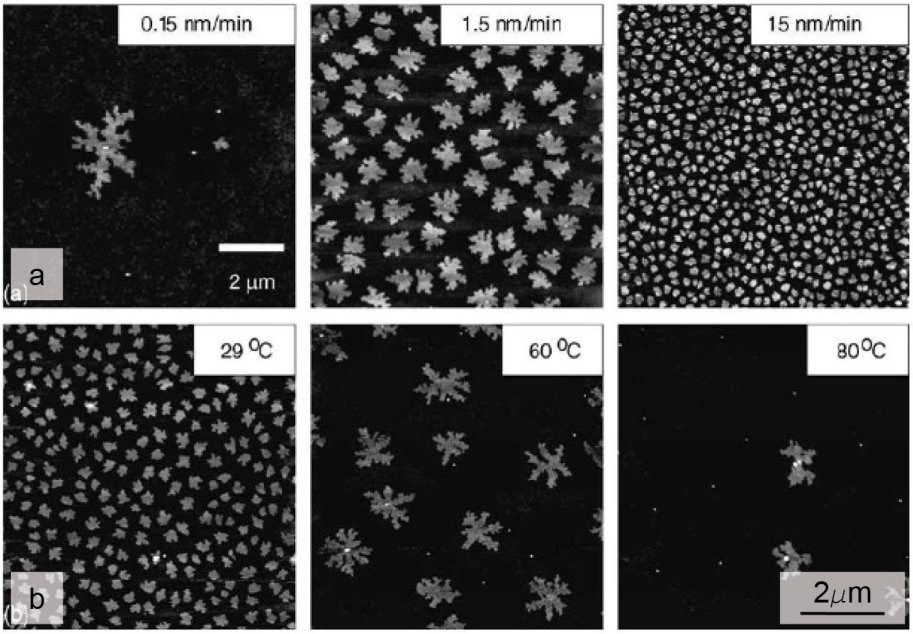

Figure 4.3: *Nucleation of pentacene film on SiO_2: AFM image of pentacene islands (a nominal thickness of 0.5nm)a) at various deposition rate for a fixed substrate temperature of* 65 °C *and b) at different substrate temperature at a fixed deposition rate of* $0.45nm/min$ *(from Pratontep et al. [88]).*

4.2 On untreated SiO_2

On bare, untreated SiO_2, the grains grow 2-dimensionally and form the first monolayer (see the incomplete first layer in Fig. 4.4). As the first monolayer is completed, the second one starts to grow (see Fig. 4.5). After a few monolayers grown layer by layer, pentacene also grows perpendicular to the dielectric surface and forms a more ragged surface (3-dimensional growth).

This change in morphology is visible in Fig. 4.6 where the film thickness changes from 10 to 80nm. For a film of 10nm in thickness, the layer-by-layer grown film is visible (see Fig. 4.6a): this part of the film is covered by a layer grown 3-dimensionally in an 80nm-thick film (see Fig. 4.6d).

The grain size is related to the substrate temperature. On the top of the 10nm-thick films, the grains have a size in the range of $2 - 3\mu m$ when deposited at RT,

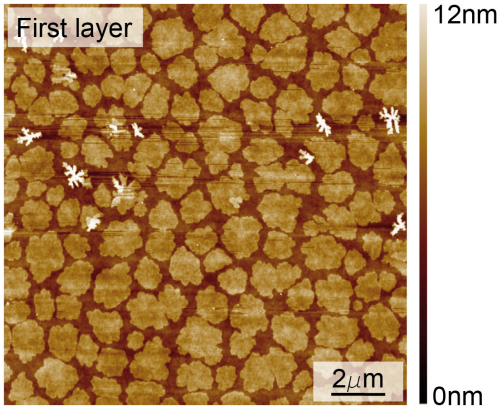

Figure 4.4: *AFM image of pentacene grown on SiO_2 at a substrate temperature of* 20 °C*: incomplete first monolayer.*

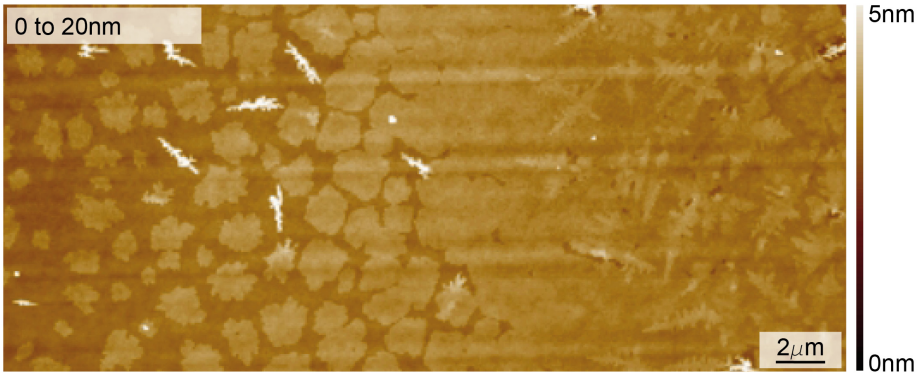

Figure 4.5: *AFM image of pentacene grown on SiO_2 at a substrate temperature of* 20 °C*: evolution of a 20nm-thick film (left: SiO_2 surface, right: 20nm pentacene).*

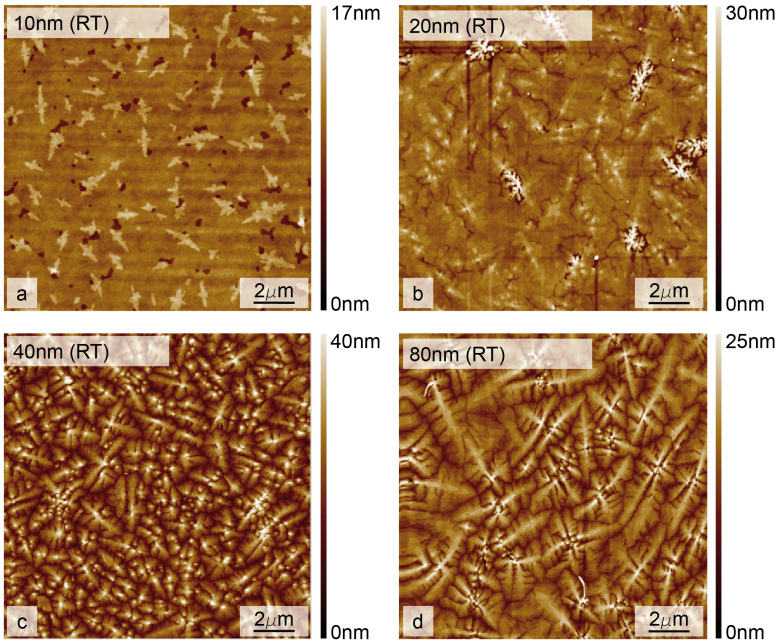

Figure 4.6: *AFM images of pentacene deposited on SiO_2 at a substrate temperature of 20 °C: the film thickness is a) 10nm, b) 20nm, c) 40nm and d) 80nm.*

while they are about $5 - 8\mu m$ in diameter at 55 °C (see Fig. 4.6a and Fig. 4.7a). On top of the 40nm-thick films, the grain size is in the submicron to $1\mu m$ range when pentacene is deposited at RT while the grains are about $2 - 3\mu m$ in diameter when deposited at 55 °C (see Fig. 4.6c and Fig. 4.7c). In addition, the grains are more compact if the film is evaporated at 55 °C while they are more dendritic on the top of films evaporated at RT (see Fig. 4.6c and d). This fact is reflected in the values of the contact resistance (top contacts): dendritic grains have a lower contact resistances than rounder grains (see in Chapter 5).

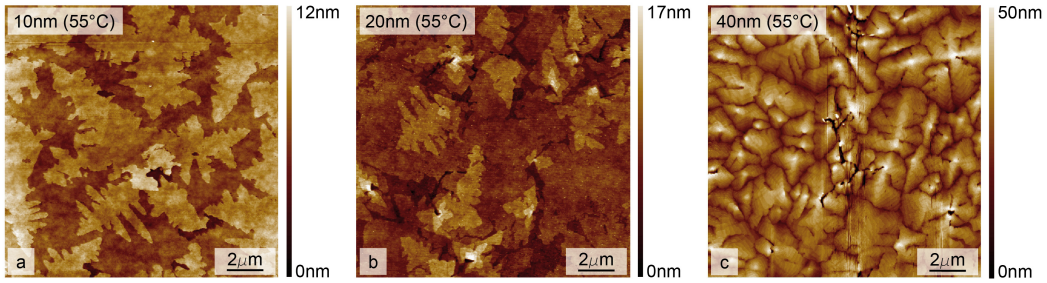

Figure 4.7: *AFM images of pentacene deposited on SiO_2 at a substrate temperature of 55 °C: the film thickness is a) 10nm, b) 20nm, and c) 40nm.*

4.3 On surface-treated SiO_2

Pentacene film growth can be affected by the dielectric surface treatments. In general, pentacene is deposited at 55 °C on surface-treated SiO_2.
Plasma treatments change the SiO_2 surface chemistry but do not significantly influence the film morphology (see Fig. 4.8). The grain size stays unchanged or is slightly increased.

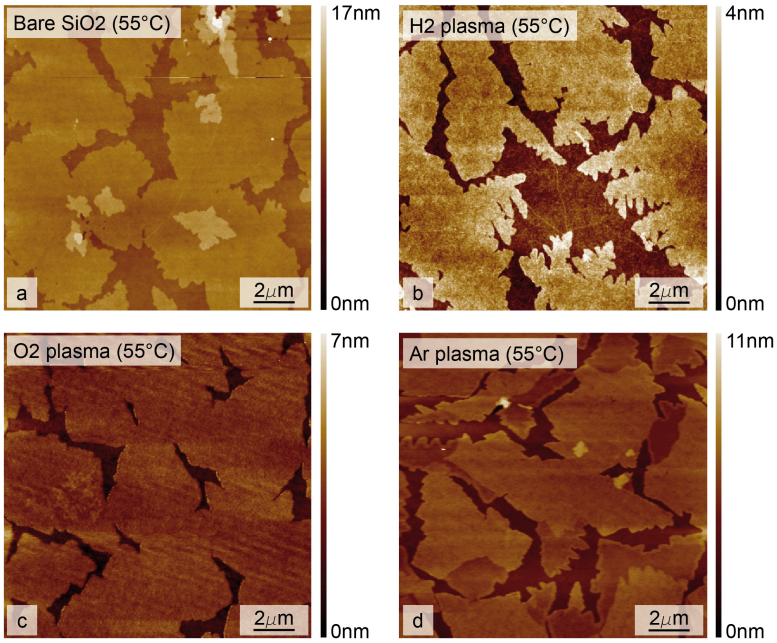

Figure 4.8: *AFM images of 10nm pentacene deposited at a substrate temperature of* 55 °C *a) on bare* SiO_2*, b) on* SiO_2 *treated by* H_2 *plasma, c) by* O_2 *plasma and d) by Ar plasma.*

The pH treatments of the SiO_2 dielectric change the surface properties by varying the $\equiv SiOH/\equiv SiO^-$ ratio on the surface. Thus the wettability changes what is visible in water contact angle measurements. The measured water contact angle is about 50 ° on the bare SiO_2 surface and stays almost unchanged for acidic and neutral pH solutions (see Fig. 4.9). For the basic pH, the water contact angle drops to about 22 °. The $\equiv SiO^-$ groups created by the basic solution lead to a more polar surface and thus to a higher wettability.

Pentacene growth on the top of the pH treated SiO_2 depends on the pH value of the solution [56]. For acidic and neutral solutions, the pentacene film grows layer by layer and the morphology is comparable with pentacene films grown on bare SiO_2 (see Fig. 4.10a). If, on the other hand, the SiO_2 substrate was immersed in a basic solution, the nucleation density is significantly increased and the growth is three-dimensional from the outset. At 55 °C, no continuous film is formed (see Fig. 4.10b and c).

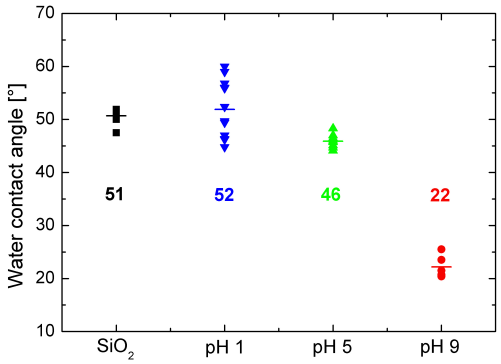

Figure 4.9: *Water contact angle of the bare SiO_2 and the pH treated SiO_2.*

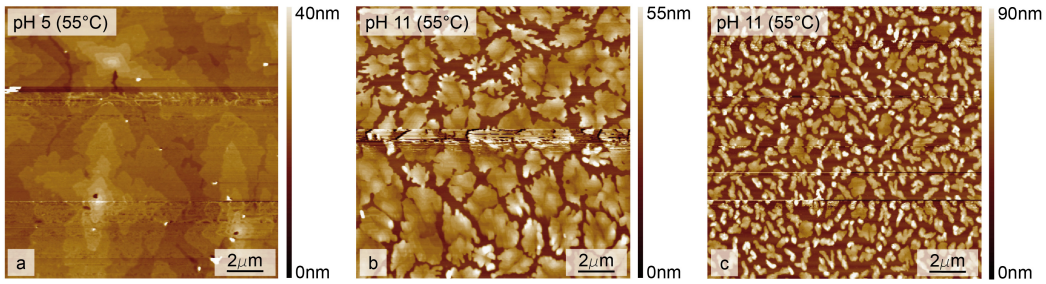

Figure 4.10: *AFM images of 10nm pentacene deposited at a substrate temperature of 55 °C on SiO_2 treated a) by ultrapure water (pH 5), b) and c) by a NaOH solution of pH 11.*

Therefore, pentacene was evaporated at RT. On the basic pH treated SiO_2, the film consists of small islands, while the film morphology after acidic and neutral treatments is similar to the one on bare SiO_2 when the substrate temperature is 20 °C (see Fig. 4.11). It becomes evident, therefore, pentacene prefers hydrophobic substrates.

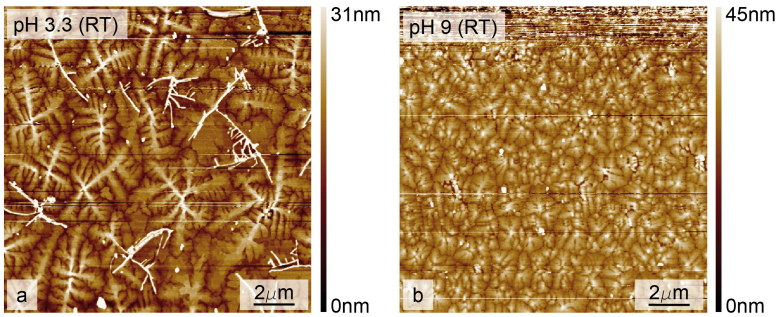

Figure 4.11: *AFM images of 10nm pentacene deposited at a substrate temperature of* 20 °C *on* SiO_2 *treated by a) the HCl solution of pH 3.3 and c) the NaOH solution of pH 9.*

The dielectric surface is also changed by a self-assembled monolayer (SAM). The SAM is deposited on the oxide dielectric by thermal evaporation. A thin Al_2O_3 layer on the top of SiO_2 is needed for the grafting reaction. The SAM changes the surface on which pentacene grows and the wettability of the surface is determined by the SAM. We measured the water contact angle on samples fabricated as the corresponding OTFTs but without pentacene and top contacts.
The measured water contact angle of the bare Al_2O_3 surface is about 75 ° (see Fig. 4.12). For the SAM containing a neutral end group (ACA, anthracene carboxylic acid), the water contact angle is in the same range as for the untreated Al_2O_3 surface (see Fig. 4.12) [1]. For a SAM carrying a nitro group as end group (NBA, nitrobenzoic acid), the water contact angle is reduced by about 10 ° while it is increased by about 10 ° for the SAM with an dimethyl-amino end group (ABA, dimethyl-aminobenzoic acid).

The change in wettability in this range does not affect pentacene growth on the top of the different SAMs. The morphology is similar for the same film thickness (see Fig. 4.13).

[1] The contact angle on ACA SAMs should be larger than that on bare Al_2O_3 because of the hydrophobicity of ACA and hydrophilicity of Al_2O_3. But the water contact angle of Al_2O_3 depends on the microstructure of the oxide film and the pH value of the distilled water [103, 104, 105]. From the surface treatments with pH solutions, we know that the ultrapure water from our *MilliPore* has about pH 5. Kuchek et al. showed that the water contact angle varies from 74 ° over 78 ° to less than 70 ° if the pH values changes from 5 to 7 [105]. This would explain why the water contact angle is high on bare Al_2O_3.

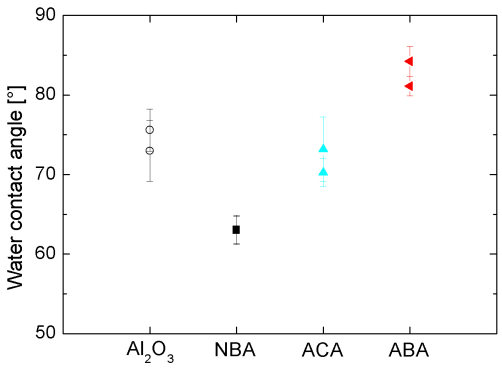

Figure 4.12: *Water contact angle of the bare Al_2O_3 oxide and the SAM modified oxide surface (measured values for two different samples and at least six different places on each sample).*

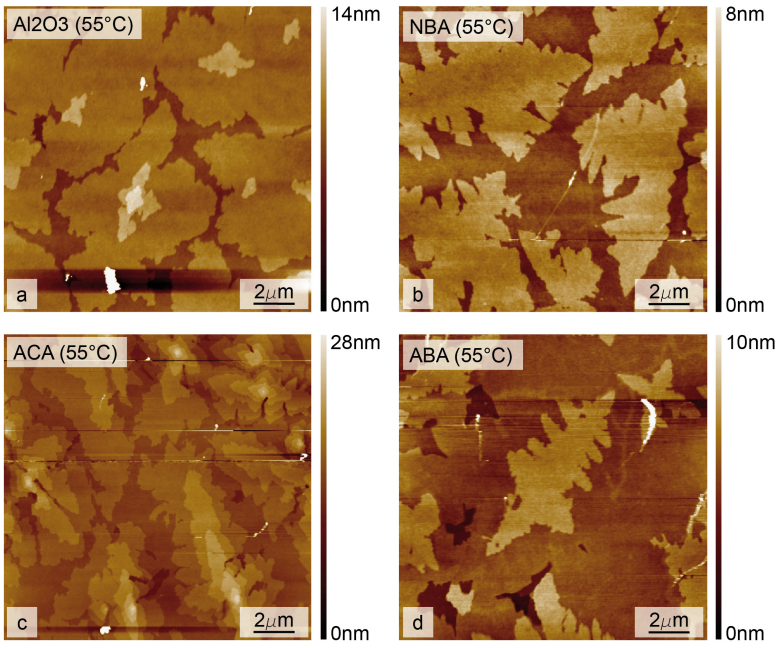

Figure 4.13: *AFM images of 10nm pentacene deposited at a substrate temperature of 55 °C a) on bare Al_2O_3 and Al_2O_3 modified by b) NBA, c) ACA and d) ABA.*

4.4 On polyimide

On polymeric surfaces, the nucleation density is often higher than on SiO_2 [89, 91, 106, 107]. Under certain deposition conditions, the first few pentacene layers are still grown layer by layer and the growth mode does not change [89, 91]. In other cases, the growth mode is three-dimensional and the nucleation density is even higher [91]. On polyimide (PI), we deposited pentacene at the substrate temperature of 20 °C. Previous depositions showed the pentacene film was not continuous at 55 °C. The first grains grow in two different modes: flat grains and fiber-like grains (see Fig. 4.14).

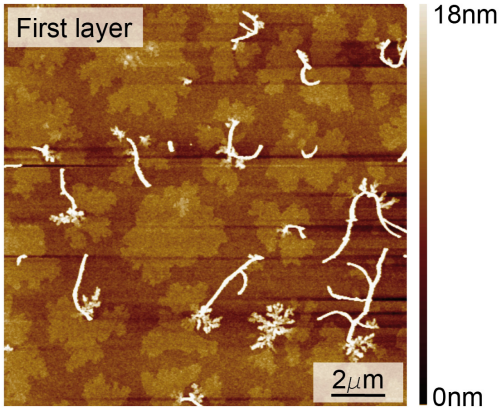

Figure 4.14: *Pentacene grown on PI at a substrate temperature of* 20 °C*: incomplete first monolayer with fiber-like grains.*

The flat grains consist of one monolayer of pentacene and have a size of about $2-3\mu m$. On the top of the flat grains, smaller grains start to grow three-dimensionally (see Fig. 4.15); bundles of grains are formed (visible as grain clusters in thicker films, see also Fig. 4.16).

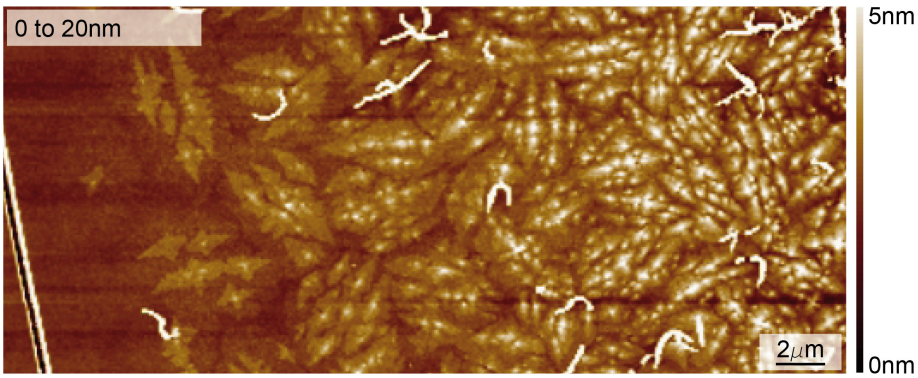

Figure 4.15: *Pentacene grown on PI at a substrate temperature of* 20 °C*: evolution of a 20nm-thick film (left: PI surface, right: 20nm pentacene).*

For film thicknesses greater than 10nm, the morphology no longer changes; the

grain size is in the sub-100nm range. The fiber-like grains form directly on the PI substrate and have a height of more than 30nm. With increasing film thickness, they are covered by the small grains. Fibers may consist of pentacene molecules that lay flat on the PI substrate, similar to the growth on clean gold surfaces [92]. In previous trials, the density and shape of the fibers depended on the deposition rate.

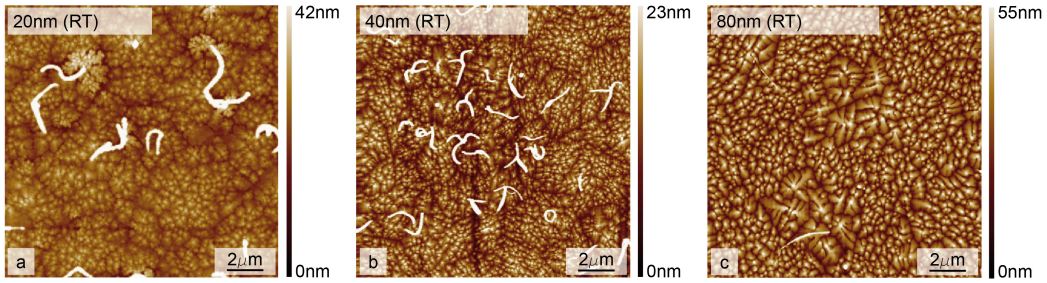

Figure 4.16: *Pentacene deposited on PI at a substrate temperature of* 20 °C*: the film thickness is a) 20nm, b) 40nm and c) 80nm.*

The PI substrate was treated by three different plasmas: H_2, O_2 and Ar plasma. The plasma treatment changes the chemistry and the morphology of the PI surface. The main interactions of plasma are etching and degradation, implantation of atoms present in the plasma near the surface and the formation of radicals in the polymer chains [108]. The wettability and the roughness after a plasma treatment are increased [109, 110, 111, 112].

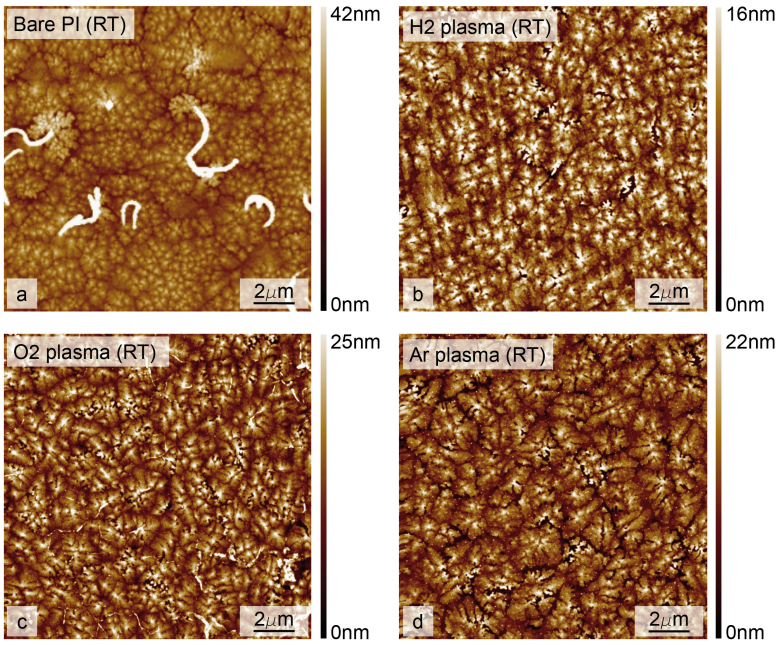

Figure 4.17: *20nm pentacene deposited at a substrate temperature of* 20 °C*: a) on bare PI and PI treated by b) H_2 plasma, c) O_2 plasma and d) Ar plasma.*

To avoid severe degradation and complete removal of the PI layer, we reduced the exposure time from 2 minutes on the oxide dielectric to 10s on the PI.
The pentacene growth on the plasma treated PI is enhanced and the type of plasma does not make a difference (see Fig. 4.17). The grain size is increased and the fiber-like grains disappear. The increased wettability has no major effect on the film morphology because it is dominated by the surface structure.

4.5 Conclusion

We deposited the pentacene thin films by thermal evaporation. The morphology of the film depends on the dielectric surface and the substrate temperature. On untreated SiO_2, pentacene grows layer by layer; the nucleation density and thus the grain size depend on the substrate temperature. The grain size in the pentacene thin films was changed by choosing a substrate temperature of either 20 °C (RT) or 55 °C (resulting in small and large grains, respectively). With increasing thickness, the film growth mode changes from layer-by-layer growth (2-dimensional growth) to 3-dimensional growth. As a consequence, the surface becomes more ragged and the grain size decreases on the top of the films compared to ultrathin films.
Surface treatment of the dielectric can affect the film morphology. On basic pH treated SiO_2, the grain size is significantly reduced and the film grows 3-dimensionally directly; a continuous pentacene film is only obtained if the substrate temperature is 20 °C. Other surface treatments (plasma treatments, SAM modification, acidic and neutral pH solutions) do not negatively influence film growth or, in some cases, they even enhance layer-by-layer growth (grain sizes up to $10\mu m$).
On polyimide substrates, a continuous film is only formed at a substrate temperature of 20 °C. The pentacene film consists of sub-100nm grains grown 3-dimensionally; underneath, the first layer is formed by flat, monolayered grains with the size of only a few μm. In thicker films, these grains are visible as clusters of small grains. Fiber-like grains also form directly on the PI surface have a height of more than 30nm, and are covered when the film thickness increases. A plasma treatment enhances the film morphology on PI by increasing the grain size and hindering the growth of the fiber-like grains.

Although there are various film morphologies, we will see in the following chapters that the film morphology plays a minor role with respect to the distribution of traps and recombination centers at the dielectric-pentacene interface. Two examples are shown in Fig. 4.18 and 4.19: the same film morphology does not mean that the transistor performance is similar and vice versa.

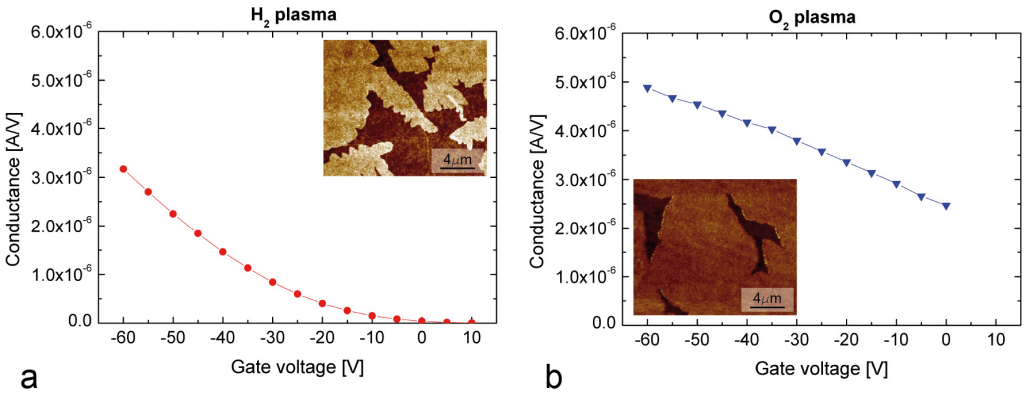

Figure 4.18: *Transfer curves of OTFTs on SiO_2 treated a) by H_2 and b) O_2 plasma, with 10nm pentacene evaporated at 55 °C (layer-by-layer growth).*

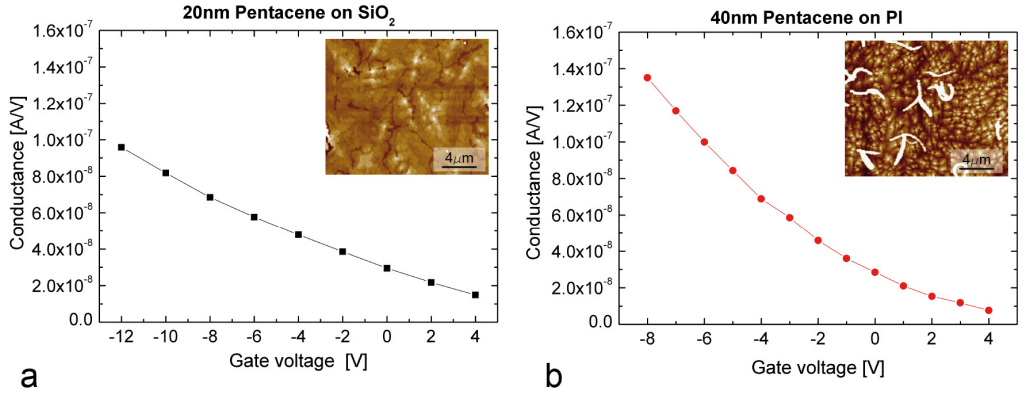

Figure 4.19: *Transfer curves of OTFTs a) on SiO_2 with 20nm pentacene (layer by layer grown) and b) on PI with 40nm pentacene (three-dimensionally grown); both pentacene films are evaporated at RT.*

Chapter 5

Transistor Geometry: The effects of channel length, pentacene film thickness and morphology

In the present chapter we study the performance of top contact pentacene thin-film transistors in relation to their architecture, i.e. the geometry of the channel and the thickness of the pentacene layer. To this end, the stencil technology developed by Katrin Sidler in the group of Prof. Jürgen Brugger (Laboratory for Microsystems 1, EPF Lausanne) was employed; with this technology, we have been able to obtain short channels down to $2\mu m$. In general, short channel sizes are preferred because they allow the design of small devices and circuits [30, 113, 114, 115]. The decrease in the channel length, however, gives more importance to the contact resistance - several authors have observed that the contact resistance dominates the characteristics of many devices [12, 25, 79, 116].
In the present thesis where the main effort concerns the study of the channel and more precisely the dielectric interface in the channel, it is necessary to first examine the role of the geometry. Therefore devices with film thicknesses from 10 to $80nm$ and with channel lengths from 2 to $600\mu m$ were studied. In addition, we have modified the microstructure of the pentacene films by the substrate temperature during deposition (RT or 55 °C, respectively) resulting in small and large grains (see Chapter 4).

5.1 Transistor geometry

The performance of an organic field-effect transistor is related to the microstructure and purity of the organic semiconductor, to the degree of order at the interface, and to the quality of the contacts [56, 90, 117]. For very short channels ($L < 5\mu m$), device performance is dominated by the Schottky barrier at the source and drain contacts [12]. For long channels ($L > 100\mu m$), the contact resistance is not determined by the barrier at the metal-organic semiconductor interface, but rather by drift/diffusion of carriers close to this interface [85, 86]. It has also been shown that the presence of a

small concentration of residual carriers can decrease the contact resistance [56].

For this work, 70 different transistors were analyzed for the effects of channel length, and pentacene film thickness and morphology. All results determined from the output and transfer curves are reported in Table 5.4, 5.5, 5.6 and 5.7 at the end of the chapter; these results are rather manifold and correlations are not straight forward, therefore, 2-probe and 4-probe measurements were performed for some of the transistors to separate the contribution of the channel and the contacts.

5.2 Channel and contact resistance

The transistors with $40nm$ pentacene show the best performance and are used for comparing the two different types of contacts. The short-channel transistors have contacts patterned by the stencil technique. The contacts of the long-channel transistors are defined by a steel mask. The channel length is 10 and $600\mu m$, respectively. The electric performance is measured by 2 and 4 probes to separate the contributions of the channel and the contacts, respectively.
In addition, the film morphology is varied. At RT, the film has grown in submicron grains with a dendritic shape [88]. If the substrate temperature is 55 °C, the grains increase in size ($2-3\mu m$ in diameter) and become more compact. The film morphology is identical for long- and short-channel transistors because the pentacene films were deposited during the same evaporation.

The output curves in Fig. 5.1 show that all transistors have a linear regime around zero drain voltage and reach saturation. At a gate voltage of $-40V$, the drain current through a transistor with a short channel ($10\mu m$ in length) is approximately twice as high as through a long-channel transistor ($600\mu m$ in length) (see Fig. 5.1).

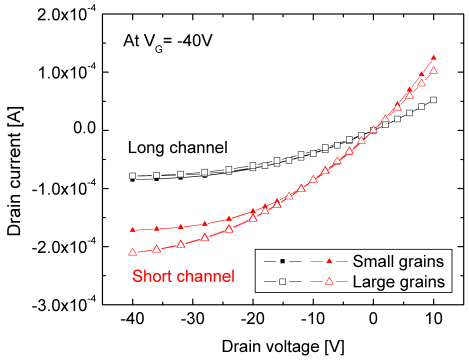

Figure 5.1: *Output curves for OTFTs with a short ($10\mu m$) or a long channel ($600\mu m$), the film morphology varies by the substrate temperature during evaporation, resulting in small and large grains (RT or 55 °C, respectively).*

The transfer characteristics in Fig. 5.2 show that the short- and long-channel

transistors behave differently. The performance of long-channel transistors is dominated by the channel and there is only a small difference between the transfer curves of the entire device and the one of the channel only (see Fig. 5.2a and b). Consequently, the apparent and channel mobility do not differ significantly (from 0.45 to $0.74 cm^2/Vs$, see Table 5.1).

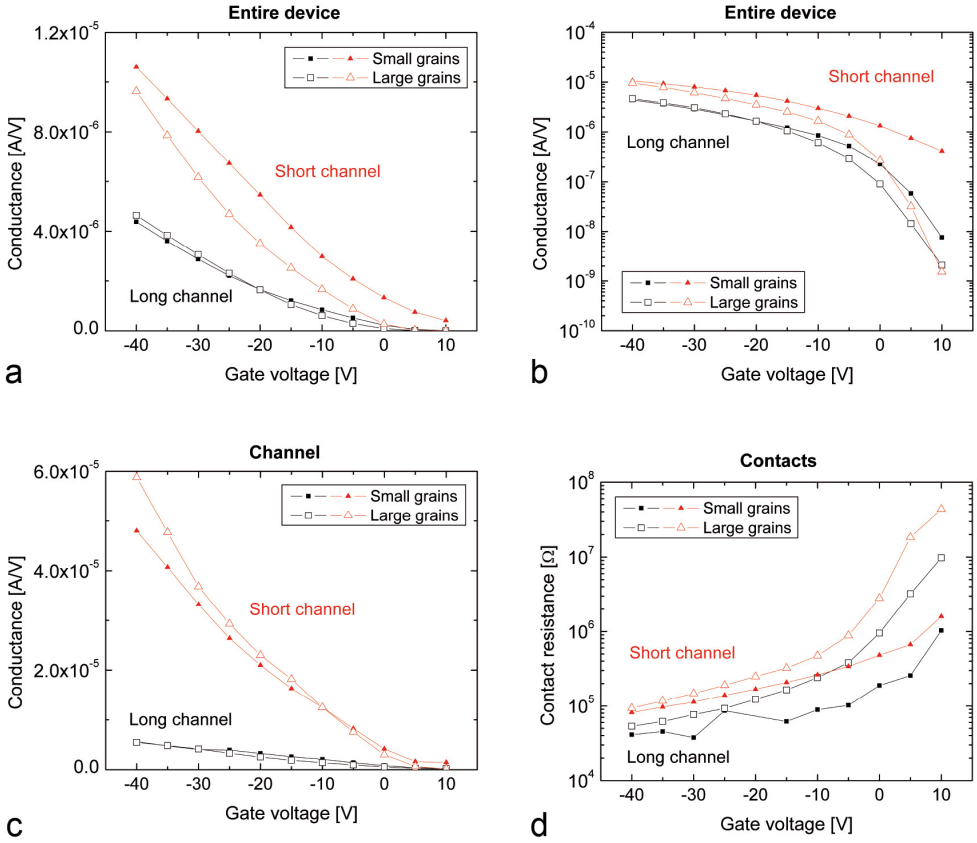

Figure 5.2: *a) and b) Transfer curves of the entire device and c) of the channel only, c) contact resistance vs. gate voltage of OTFTs with a short (10µm) and a long channel (600µm) and small or large grains (RT or 55 °C, respectively).*

In contrast, the transistors with a short channel are limited by the contacts. The channel conductance is approximately 5 times higher than the conductance of the entire device (see Fig. 5.1a and c). As expected, this behavior is reflected in the mobility values. While the apparent mobility of the entire device is in the range of $1.4 - 1.6 cm^2/Vs$, the channel mobility is more than 5 times higher and reaches $10 cm^2/Vs$. The contact resistance is 2-3 times higher in short-channel transistors than in long-channel transistors (see Table 5.1).

The 4-probe and 2-probe measurements are an excellent tool to separate the channel resistance (or conductance) from the contact resistance. Fig. 5.1d shows clearly that the contact resistance depends significantly on the gate voltage and also

	Channel		Entire device		At floating gate		
	Channel mobility $[cm^2/Vs]$	Threshold voltage $[V]$	Apparent mobility $[cm^2/Vs]$	Threshold voltage $[V]$	Total resistance $[M\Omega]$	Channel resistance $[M\Omega]$	Contact resistance $[M\Omega]$
$600\mu m$ long channel							
RT	0.59	7.3	0.45	8.3	1.39	1.26	0.14
55 °C	0.74	-1.8	0.58	-2.7	2.92	2.11	0.81
$10\mu m$ long channel							
RT	7.42	-6.9	1.39	-4.3	0.67	0.23	0.44
55 °C	10.2	-11	1.57	-11	3.15	0.33	2.82

Table 5.1: *Apparent mobility and threshold voltage for the channel only and the entire device; channel, contact and total resistance measured at floating gate for OTFTs with a short ($10\mu m$) and a long channel ($600\mu m$) and small or large grains (RT or 55 °C, respectively).*

on the grain size and morphology. Gold films evaporated on small dendritic grains always give smaller contact resistance than the same films evaporated on large grains. The dendritic shape of small grains is more favorable to low contact resistance than the round shape of large grains; this behavior is most pronounced around zero gate voltage. Large grains result in a much higher contact resistance and improve the off-state of the transistor. These results are in contradiction with the conclusions of S.H. Jin et al. obtained by the transfer line method [118].

Even more surprising is the behavior of the pentacene channel resistance in a floating gate configuration. Table 5.1 shows that pentacene films made of small grains are always more conductive than films of the same length made of large grains; this fact demonstrates that grain boundaries do not act as simple barriers but also modify the distribution of traps and recombination centers. More precisely, small dendritic grains which lead to a higher density of grain boundaries in the film induce more charge transfers at the interface of the oxide than large grains because the grain boundary line is longer. The residual carriers make the semiconductor film conductive at zero gate voltage [50]. The apparent mobility of the channel is less sensitive to the presence of residual carriers because it is determined mainly at moderate and high gate voltages. In short channels, where the carriers cross only a few grains, the mobilities are on the order of $10cm^2/Vs$ and large grains perform better than small grains (see Table 5.1). In long channels, the trap distribution at the interface is significantly modified and the apparent mobility drops to between 0.6 and $0.7cm^2/Vs$ due to defects acting mainly on the trap distribution.
Due to contact effects, the apparent mobility in the short $10\mu m$ devices made of large grains drops from 10 to $1.6cm^2/Vs$. For long channels, the effect of the contacts is much lower and the apparent mobility of the long-channel devices remains very close to 0.5 to $0.6cm^2/Vs$, the channel mobility.

One of the main purpose of this chapter was to separate the resistance of the channel from the resistance from the resistance of the contacts. This was achieved by using the 4-probe measurements. The channel resistance was determined independently of the contact resistance [50]. Then the contact resistance was determined as the difference between the values obtained by the 2-probe and the 4-probe mea-

surements. More common for determining the contact resistance is the transfer line method which uses transistors of the same batch but of different channel lengths. The contact resistance is obtained by extrapolating the resistance at zero channel length [119, 120, 121].
In Fig. 5.3, we compare the results of the 4-probe method and the transfer line method for two different batches of transistors. The two measurements coincide within a factor of two at low gate fields and 20% at large gate fields. This discrepancy is in large part due to the transfer line method which assumes a perfect homogeneity in the batch what is difficult to achieve in practice. As observed by other groups, the 4-probe method is also questionable when the potential of the inner electrodes is perturbed by the current flowing between the outer electrodes, especially for thick films when the electrodes do not penetrate enough in the channel region [85, 86]. But in this work where large effects were observed and thin films were used (20 and $40nm$), the errors on the absolute value of the contact resistance does not invalidate our conclusions.

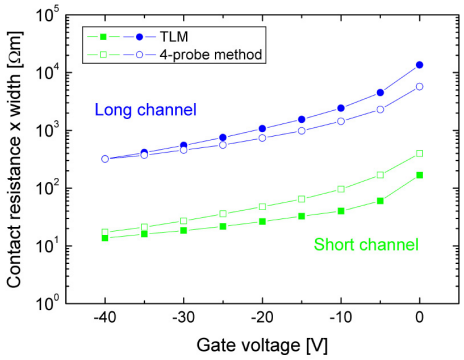

Figure 5.3: *Contact resistance (normalized to the channel width) measured by the 4-probe method (one transistor) and extrapolated by the transfer line method (5-6 transistors of the same batch). The long-channel transistors have a channel length of* $100-600\mu m$ *and a channel width of* $6mm$*; the 4-probe measurements were done for a distance between the contacts of* $600\mu m$*. The short-channel transistors have a channel length of* $2-20\mu m$ *and a channel width 10 times larger; the 4-probe measurements were done for a distance between the contacts of* $10\mu m$*. The pentacene film consists of large grains. The film thickness is* 40 *and* $20nm$ *for long-channel and short-channel transistors, respectively.*

By the stencil technology combined with 4-probe measurements, we were able to observe the gate voltage dependence of both channel and contact resistances and their different sensitivity to the film morphology. The most important results are:

- The performance of the long-channel transistors is dominated by the channel.
- The performance of the short-channel transistors is limited by the contacts.

- The contact resistance is affected by the film morphology. Large grains result in higher contact resistances, especially around zero gate voltage.
- The channel resistance is independent of the film morphology.

These findings are now applied on OTFTs with different film thicknesses. The channel lengths are 10 or $20\mu m$ for the short-channel transistors and $600\mu m$ for the long-channel transistors.

5.3 Thickness of the pentacene film

The pentacene films were deposited with thicknesses ranging from 10 to $80nm$ (see Chapter 4). The resulting grain size depends on the substrate temperature and the film thickness: $5-8\mu m$ for $10nm$ at 55 °C; $2-3\mu m$ and $3-5\mu m$ for $20nm$ at RT and 55 °C; submicron size and $2-3\mu m$ for $40nm$ at RT and 55 °C and submicron to $1\mu m$ size for $80nm$ at RT, respectively. Please notice that these are grains at the surface of the pentacene films where the contacts are deposited which do not reveal much about the size of the grains in the channel.

In general, the transfer curves show lower conductance than the ones of OTFTs with $40nm$ pentacene, independently of whether the film is thicker ($80nm$) or thinner (10 or $20nm$) (see Fig. 5.4 and 5.5).

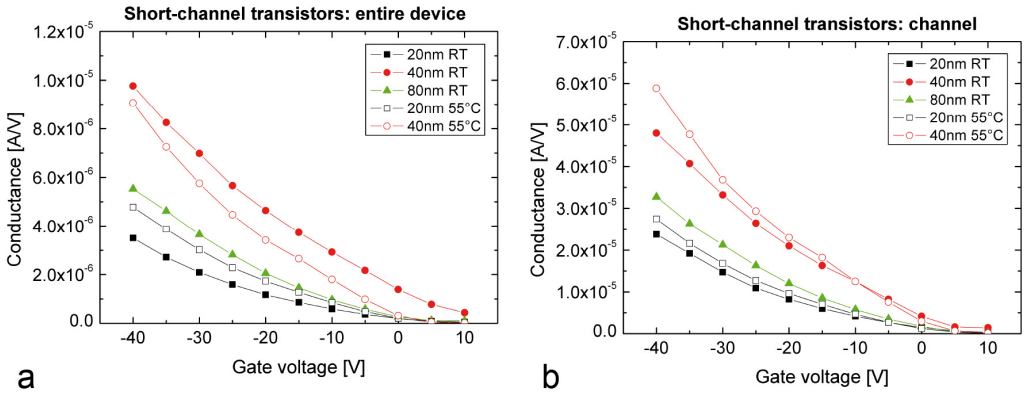

Figure 5.4: *Transfer curves for a) the entire device and b) the channel only of short-channel transistors with different film thickness and substrate temperature.*

For short-channel transistors, the grain size has the opposite effect in the OTFTs with $20nm$ pentacene than in the transistors with $40nm$ pentacene (higher conductance for large grains).
The channel conductance is about 5 times higher than for the entire device; this is reflected in the values of the apparent mobility (see Table 5.2). The OTFTs with a short channel, therefore, are contact-limited independently of the pentacene film thickness.

	Channel		Entire device		At floating gate		
	Channel mobility $[cm^2/Vs]$	Threshold voltage $[V]$	Apparent mobility $[cm^2/Vs]$	Threshold voltage $[V]$	Total resistance $[M\Omega]$	Channel resistance $[M\Omega]$	Contact resistance $[M\Omega]$
Small grains							
20nm	4.43	-13	0.65	-13	4.11	0.68	3.44
40nm	7.42	-6.9	1.39	-4.3	0.67	0.23	0.44
80nm	5.56	-10	0.94	-9.8	7.27	1.32	5.94
Large grains							
20nm	5.02	-12	0.86	-12	5.33	0.69	4.64
40nm	10.2	-11	1.57	-11	3.15	0.33	2.82

Table 5.2: *Apparent mobility and threshold voltage for the channel only and the entire device; channel, contact and total resistance measured at floating gate for OTFTs with a channel length of* $10\mu m$ *(for 80nm pentacene:* $L = 20\mu m$*).*

Long-channel transistors are dominated by the channel (see Fig. 5.5 and Table 5.3). The transfer curves of the OTFTs with $20nm$ pentacene are separated from each other unlike the transistors with $40nm$ pentacene. This is due to the different concentration of residual carriers in the channel. For large grains, the residual carrier density is with $1.1 \cdot 10^{12} cm^{-2}$ about 5 times higher than for small grains ($2.5 \cdot 10^{11} cm^{-2}$), thus the conductivity is increased. The higher residual carrier density is also reflected in the positive threshold voltage (see Table 5.5).

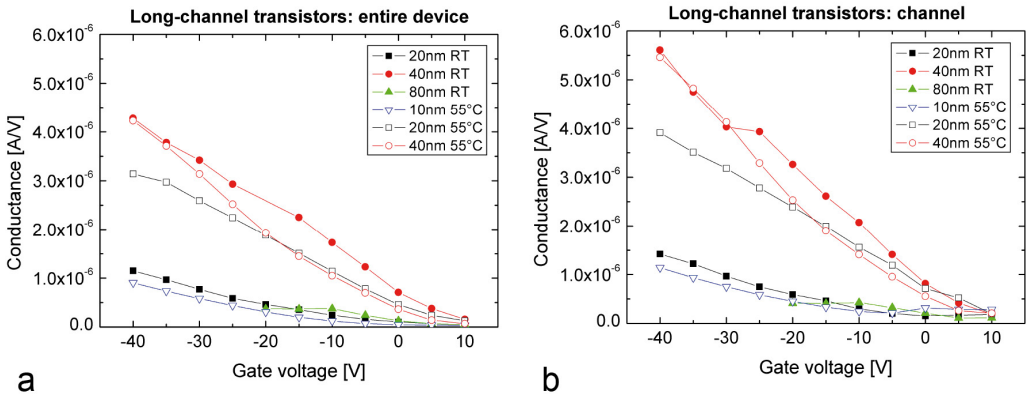

Figure 5.5: *Transfer curves for a) the entire device and b) the channel only of long-channel transistors with different film thickness and substrate temperature.*

The contact resistance for both categories of transistors is plotted in Fig. 5.6. For short channel transistors, the ratio of the contact resistance to the total resistance is essentially independent of the thickness and equal to 0.8 (see Fig. 5.7); this is due to the fact that in this case the division between contact and channel is rather artificial: the transistor consists essentially of a contact modulated by the gate.

The situation is different for long-channel transistors. In general, the ratio between the contact and the total resistances is small (in the order of 0.2), however, some of the transistors, especially at low pentacene film thicknesses, exhibit larger

	Channel		Entire device		At floating gate		
	Channel mobility $[cm^2/Vs]$	Threshold voltage $[V]$	Apparent mobility $[cm^2/Vs]$	Threshold voltage $[V]$	Total resistance $[M\Omega]$	Channel resistance $[M\Omega]$	Contact resistance $[M\Omega]$
Small grains							
20nm	0.23	-8.5	0.19	-9.4	10.5	6.87	3.59
40nm	0.59	7.3	0.45	8.3	1.39	1.26	0.14
80nm	0.11	10	0.11	73	10.2	6.37	3.85
Large grains							
10nm	0.19	-9.4	0.16	-11	38.3	6.08	32.3
20nm	0.38	13	0.37	5.9	1.34	1.09	0.25
40nm	0.74	-1.8	0.58	-2.7	2.92	2.11	0.81

Table 5.3: *Apparent mobility and threshold voltage for the channel only and the entire device; channel, contact and total resistance measured at floating gate for OTFTs with a channel length of* $600\mu m$.

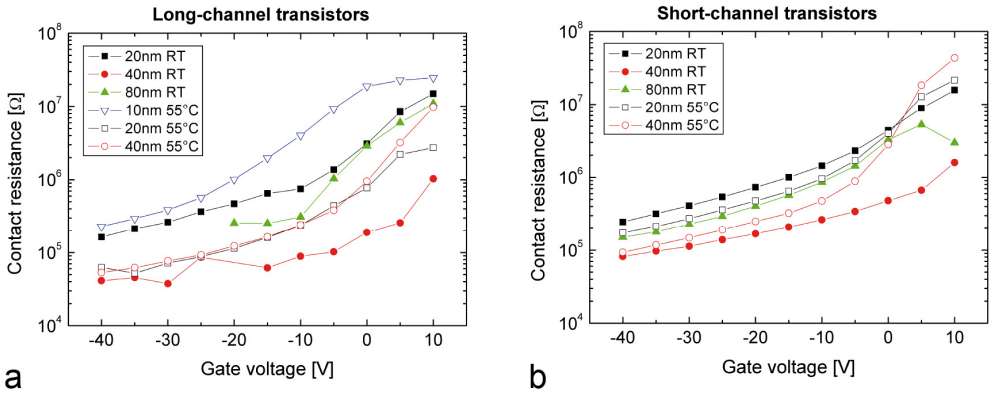

Figure 5.6: *Contact resistance vs. gate voltage a) of long-channel and b) short-channel transistors with different film thickness and substrate temperature.*

contact resistance (see Fig. 5.7a). The absolute value of the contact resistance is larger for thick films ($80nm$) than for the intermediate films ($40nm$), and this is due to the access to the channel which depends on the distance between the contact and the channel.

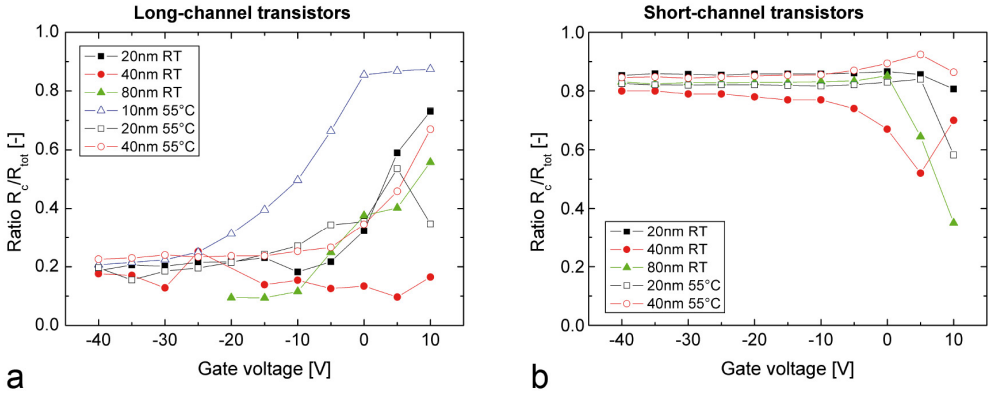

Figure 5.7: *Ratio of the contact resistance to the total resistance a) of long-channel and b) short-channel transistors with different film thickness and substrate temperature.*

In conclusion, the thickness of the pentacene film has some influence on the behavior of the transistors but the results are not easy to understand.
The ratio of the contact and total resistance is determined by the contact geometry; about 0.8 for short-channel transistors and about 0.2 for the long-channel transistors at negative gate voltages, meaning the former are contact limited and the latter are channel dominated.
For $80nm$ pentacene, the contact resistance increases due to a longer access path between the contacts and the channel. For thinner films, the contact resistance is increased due to a slower drift/diffusion near the contacts. The film morphology has some effect on the contact resistance. Around zero gate voltage, large grains improve the off-state of the transistor (lower the off-state current).

5.4 Channel length

As shown, the performance of the short-channel transistors is limited by the contacts thus the characteristic values are determined by the contacts and do not depend on the channel length (see Table 5.5); the exception is the apparent mobility which is only constant for a channel length of 10 and $20\mu m$ and decreases for smaller channel lengths (see Fig. 5.8). This shows that it is dangerous to trust too much on the values of the apparent mobilities alone.

The long-channel transistors are dominated by the channel, thus the performance can depend on the channel length; this is the case for the values of the apparent mobility and the residual carrier density which both increase with decreasing channel

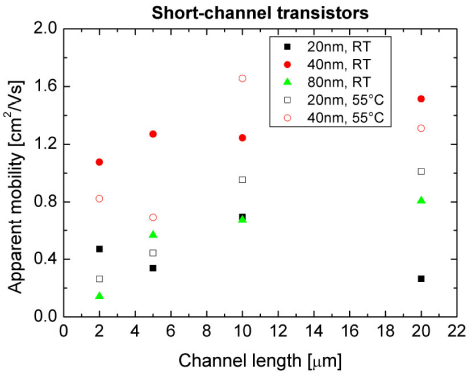

Figure 5.8: *Apparent mobility vs. channel length of short-channel transistors with small and large grains (RT and* 55 °C*, respectively).*

lengths (see Fig. 5.9).

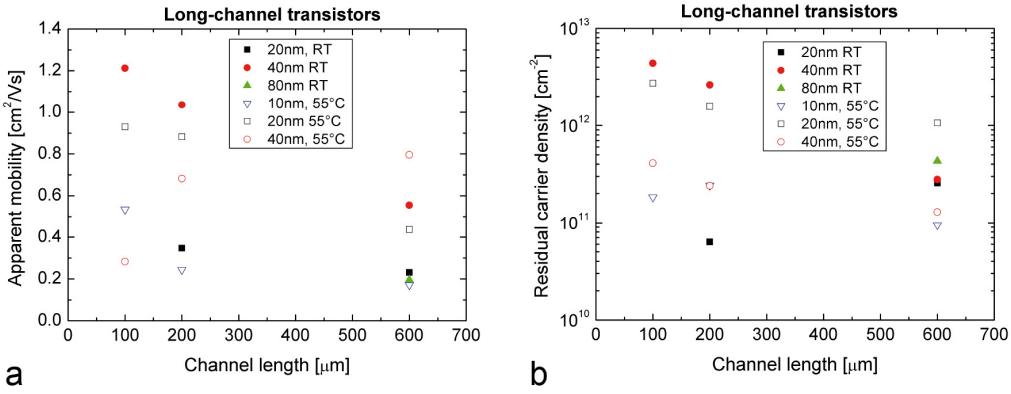

Figure 5.9: *a) Apparent mobility and b) residual carrier density vs. channel length of short-channel transistors with small and large grains (RT and* 55 °C*, respectively).*

It is interesting to establish the link between the apparent mobility and the concentration of residual carriers in the channel. This is discussed in the next section.

5.5 Traps and residual carriers

The performance of a channel-dominated OTFT depends on the traps and the residual carriers which are present at the dielectric-pentacene interface. Traps reduce the apparent mobility by MTR (multiple trapping and release by shallow traps) and the threshold voltage (by deep traps). The residual carriers shift the threshold to positive values and increase the apparent mobility by screening the traps at the interface. In addition, elevated residual carrier densities result in an increase of the device conductivity and in a decrease in the contact resistance by screening effects

at the contacts. The latter can be compared with the dependence on the gate field where the contact resistance decreases when more charge carriers are induced by the gate voltage (see Fig. 5.6).

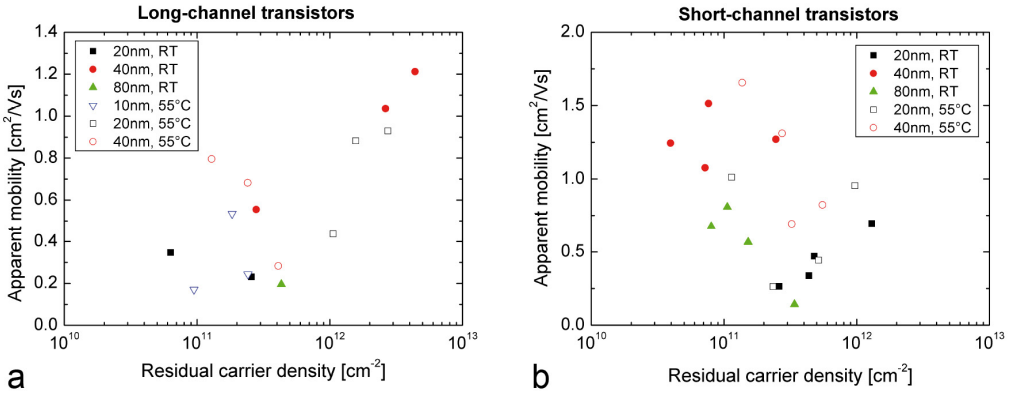

Figure 5.10: *Apparent mobility vs. residual carrier density a) of long-channel and b) short-channel transistors with small and large grains (RT and* 55 °C*, respectively).*

The performance of the long-channel transistors is dominated by the channel, thus it is affected by the residual carrier density. In Fig. 5.10a, we see a crossover between a trap limited regime at low concentrations and a residual carrier enhanced mobility at higher concentrations. The influence of the residual carriers is also observable especially in long channels (see Fig. 5.11a).

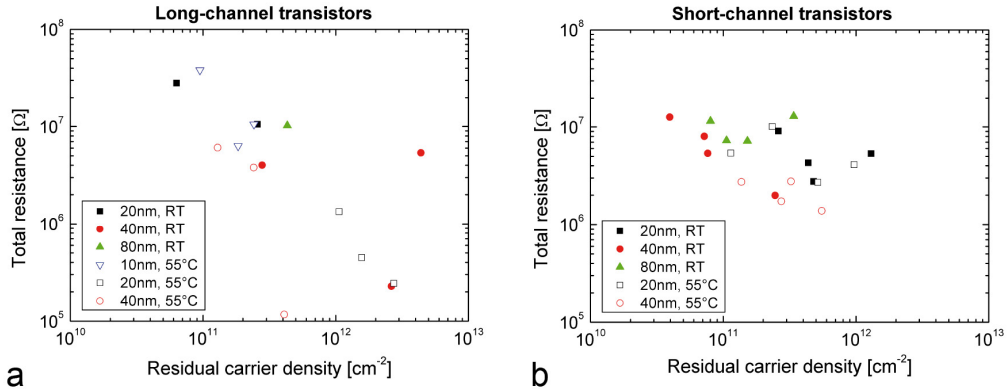

Figure 5.11: *Total resistance vs. residual carrier density a) of long-channel and b) short-channel transistors with small and large grains (RT and* 55 °C*, respectively).*

In short-channel transistors, the effect of residual carriers on the contacts seems lower, but a correlation is clearly present, especially in the 40*nm* pentacene films (see Fig. 5.10b and Fig. 5.11b).

In conclusion, the residual carrier density is one of the pertinent parameters determining the characteristics of the organic thin-film transistors.

5.6 Polyimide as dielectric layer

The change of the dielectric has several consequences in organic transistors based on pentacene. The polyimide (PI) layer we used here has a thickness of $210nm$ and a capacitance of $11nF/cm^2$; therefore, the field effect for the same gate voltage is smaller than for SiO_2 ($C_{gate} = 19.8nF/cm^2$). The polymeric surface brings on a change in the morphology of the pentacene film. The pentacene film is deposited at RT and grows three-dimensionally on the top of PI. The film morphology does not change dramatically if the film thickness is increased from 20 to $80nm$ (see Chapter 4).

The OTFTs with PI as dielectric have a channel length ranging from 2 to $20\mu m$. For longer channels, the transistors failed during measuring (break through or large leakage currents compared to the drain-source current). The transfer curves were measured between $+4$ and $-12V$ to avoid a break through. The characteristic values of the transistors with SiO_2 as dielectric were determined in the same range.

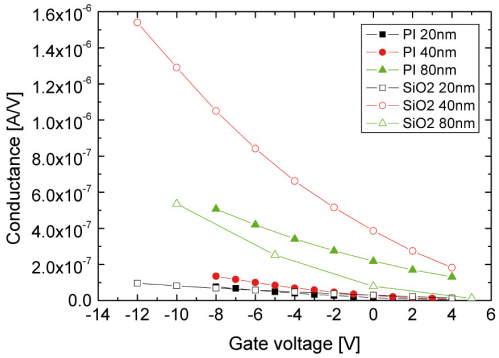

Figure 5.12: *Transfer curves of short-channel transistors with PI and SiO_2 as dielectric and different film thickness.*

On PI dielectrics, the best performance is measured for transistors with a $80nm$-thick pentacene film. The conductance is then even higher as in a transistor with SiO_2 dielectric and the same pentacene film thickness (see Fig. 5.12). For a pentacene film thickness of $10nm$, the transistors on PI and SiO_2 show almost the same performance. The best performance for all transistors was measured for a transistor with $40nm$ pentacene on SiO_2. The results are in Table 5.6 and 5.7 at the end of the chapter.

The apparent mobility and the total resistance depend on the film thickness and on the dielectric. The values are in the same range for both dielectrics if the film

thickness is 20 or 80nm (see Table 5.7). The apparent mobility increases and the conductivity decreases with increasing film thickness for PI while it has a maximum and a minimum, respectively, for SiO_2.

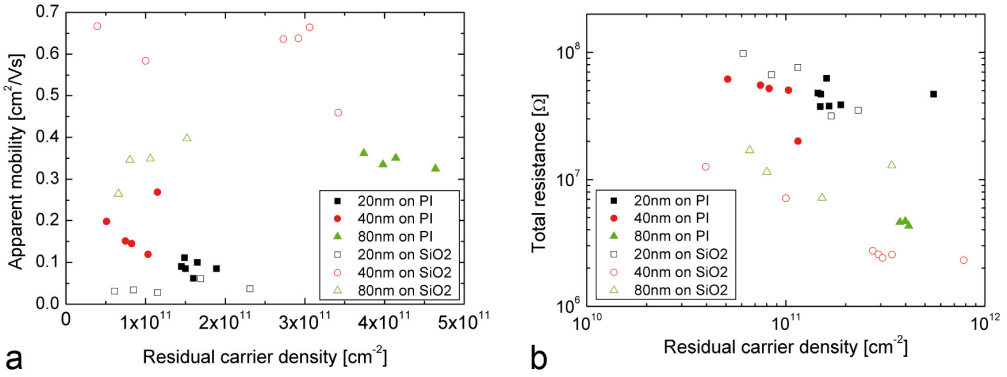

Figure 5.13: *a) Apparent mobility and b) total resistance vs. residual carrier density of short-channel transistors with PI and SiO_2 as dielectric and different film thickness.*

The apparent mobility and the total resistance are plotted versus the residual carrier density. For transistors with PI, the apparent mobility decreases with increasing residual carrier density and reaches a minimum around $2 \cdot 10^{11} cm^{-2}$, while the total resistance is almost independent of the residual carrier density. For transistors with SiO_2, the total resistance decreases with increasing residual carrier density while the apparent mobility is not correlated with the residual carrier density (see Fig. 5.13).

We know that the performance of short-channel transistors with SiO_2 as dielectric is contact limited. Consequently, the total resistance is dominated by the contact resistance which decreases with increasing residual carrier density (see Fig. 5.11b). The apparent mobility includes contact effects, thus it is not dominated by the channel (see Fig. 5.10b).
The transistors with PI as dielectric show a dependence on the residual carrier density similar to long-channel transistors on SiO_2 (see Fig. 5.10a). The OTFT performance could, therefore, be dominated by the channel. In this case, the total resistance is not dominated by the contact resistance and, at low residual carrier densities, not correlated with the residual carrier density (see Fig. 5.13). This point should be checked properly by performing 4-probe measurements. For 80nm pentacene, the values of total resistance and apparent mobility are too close to each other for deducing a tendency. In Fig. 5.13, the total resistance of the OTFTs on PI with 80nm pentacene is close to the value of the OTFTs on SiO_2 with 80nm pentacene, thus demonstrating the contribution of the contact increases, while the contact contribution becomes larger and the dielectric-pentacene interface becomes less important.

5.7 Conclusion

Organic thin-film transistors (OTFTs) were fabricated on silicon oxide (SiO_2) and polyimide (PI) dielectric. The contacts were patterned either by a stencil (short channels) or a steel mask (long channels). The substrate temperature during pentacene evaporation was either RT or 55 °C, resulting in different grain sizes. Several geometrical aspects were varied: the channel length from 2 to 600μm, the film thickness from 10 to 80nm, and the grain size from submicron to several microns in size.

The performance of OTFTs on SiO_2 depends on the contact geometry, the pentacene film thickness, and morphology. The contact geometry determines if the transistor is dominated by the channel or the contacts. The long-channel transistors ($L = 100 - 600\mu m$) are channel-dominated thus the performance depends on the trap distribution and the residual carriers at the dielectric-pentacene interface. The short-channel transistors ($L = 2 - 20\mu m$) are contact-limited, meaning the performance is determined by the contact behavior and the properties of the channel play only a minor role.
The thickness of the pentacene film affects the OTFT performance by determining the total current. The best performance is observed for transistors with 40nm pentacene. The film morphology has more influence on the contact resistance than on the channel. A film consisting of large grains results in reducing the off-state current of the transistor.

On PI, stencil masks are a good tool for patterning contacts in transistors because the risk of break through is reduced due to the shorter channel lengths. The best performance of OTFTs with a polyimide dielectric is observed at a pentacene film thickness of 80nm; the performance is even better than transistors on SiO_2 with 80nm pentacene. The apparent mobility and conductivity show less variation in the values for PI than SiO_2. There are indications that the performance in OTFTs on PI is dominated by the channels (unlike on SiO_2 where it is contact-limited); with increasing film thickness, the contact resistance becomes more important.

Measured in this chapter were transistor characteristics versus the architecture of the devices. We have observed that bare results are very difficult to interpret directly. In particular 4-probe measurements are indeed a good tool to understand the main trends in the transistor properties. Residual carrier concentrations are also important parameters often neglected in the literature.

In the following chapters, the dielectric surface is modified. For analyzing the effect of the modifications, we have chosen transistors with a channel length of 600μm because their performance is not limited by the contacts. On PI dielectric, there are additionally short-channel transistors used because they are less contact-limited (compared to short-channel OTFTs on SiO_2), and long-channel transistors could fail during characterization.

Sample N °C	Channel length	Film thickness	Grain size (evaporation temperature)	Channel width	AR
1	600μm	20nm	Small (RT)	6mm	10
2	600μm	40nm	Small (RT)	6mm	10
3	600μm	80nm	Small (RT)	6mm	10
4	600μm	10nm	Large (55 °C)	6mm	10
5	600μm	20nm	Large (55 °C)	6mm	10
6	600μm	40nm	Large (55 °C)	6mm	10
7	200μm	20nm	Small (RT)	6mm	30
8	200μm	40nm	Small (RT)	6mm	30
9	200μm	10nm	Large (55 °C)	6mm	30
10	200μm	20nm	Large (55 °C)	6mm	30
11	200μm	40nm	Large (55 °C)	6mm	30
12	100μm	40nm	Small (RT)	6mm	60
13	100μm	10nm	Large (55 °C)	6mm	60
14	100μm	20nm	Large (55 °C)	6mm	60
15	100μm	40nm	Large (55 °C)	6mm	60
16	20μm	20nm	Small (RT)	200μm	10
17	20μm	40nm	Small (RT)	200μm	10
18	20μm	80nm	Small (RT)	200μm	10
19	20μm	20nm	Large (55 °C)	200μm	10
20	20μm	40nm	Large (55 °C)	200μm	10
21	10μm	20nm	Small (RT)	100μm	10
22	10μm	40nm	Small (RT)	100μm	10
23	10μm	80nm	Small (RT)	100μm	10
24	10μm	20nm	Large (55 °C)	100μm	10
25	10μm	40nm	Large (55 °C)	100μm	10
26	5μm	20nm	Small (RT)	50μm	10
27	5μm	40nm	Small (RT)	50μm	10
28	5μm	80nm	Small (RT)	50μm	10
29	5μm	20nm	Large (55 °C)	50μm	10
30	5μm	40nm	Large (55 °C)	50μm	10
31	2μm	20nm	Small (RT)	20μm	10
32	2μm	40nm	Small (RT)	20μm	10
33	2μm	80nm	Small (RT)	20μm	10
34	2μm	20nm	Large (55 °C)	20μm	10
35	2μm	40nm	Large (55 °C)	20μm	10

Table 5.4: *Description of the measured and analyzed OTFTs on SiO_2.*

Sample N°	Apparent mobility $[cm^2/Vs]$	Threshold voltage $[V]$	Conductivity $[S\,\square]$	Residual carriers $[cm^{-2}]$	Total resistance $[\Omega]$
1	0.231	-13	$9.56{\cdot}10^{-9}$	$2.57{\cdot}10^{11}$	$1.05{\cdot}10^{7}$
2	0.555	-7.2	$2.49{\cdot}10^{-8}$	$2.79{\cdot}10^{11}$	$4.01{\cdot}10^{6}$
3	0.196	-7.3	$1.36{\cdot}10^{-8}$	$4.32{\cdot}10^{11}$	$1.02{\cdot}10^{7}$
4	0.171	-12	$2.61{\cdot}10^{-9}$	$9.49{\cdot}10^{10}$	$3.83{\cdot}10^{7}$
5	0.437	8.2	$7.46{\cdot}10^{-8}$	$1.06{\cdot}10^{12}$	$1.34{\cdot}10^{6}$
6	0.796	-10	$1.65{\cdot}10^{-8}$	$1.29{\cdot}10^{11}$	$6.07{\cdot}10^{6}$
7	0.347	-19	$1.18{\cdot}10^{-9}$	$6.33{\cdot}10^{10}$	$2.82{\cdot}10^{7}$
8	1.036	1.0	$1.46{\cdot}10^{-7}$	$2.63{\cdot}10^{12}$	$2.28{\cdot}10^{5}$
9	0.244	-9.4	$3.18{\cdot}10^{-9}$	$2.42{\cdot}10^{11}$	$1.05{\cdot}10^{7}$
10	0.882	-2.6	$7.44{\cdot}10^{-8}$	$1.57{\cdot}10^{12}$	$4.48{\cdot}10^{5}$
11	0.682	-12	$8.81{\cdot}10^{-9}$	$2.41{\cdot}10^{11}$	$3.79{\cdot}10^{6}$
12	1.212	-1.1	$1.43{\cdot}10^{-7}$	$4.39{\cdot}10^{12}$	$5.36{\cdot}10^{6}$
13	0.534	-15	$2.64{\cdot}10^{-8}$	$1.84{\cdot}10^{11}$	$6.32{\cdot}10^{6}$
14	0.929	-2.8	$6.84{\cdot}10^{-8}$	$2.74{\cdot}10^{12}$	$2.44{\cdot}10^{5}$
15	0.283	-12	$3.11{\cdot}10^{-9}$	$4.10{\cdot}10^{11}$	$1.17{\cdot}10^{5}$
16	0.264	-7.6	$1.10{\cdot}10^{-8}$	$2.60{\cdot}10^{11}$	$9.06{\cdot}10^{6}$
17	1.514	-8.0	$1.87{\cdot}10^{-8}$	$7.66{\cdot}10^{10}$	$5.36{\cdot}10^{6}$
18	0.808	-11	$1.38{\cdot}10^{-8}$	$1.06{\cdot}10^{11}$	$7.27{\cdot}10^{6}$
19	1.012	-14	$1.86{\cdot}10^{-8}$	$1.14{\cdot}10^{11}$	$5.39{\cdot}10^{6}$
20	1.311	-4.8	$5.79{\cdot}10^{-8}$	$2.74{\cdot}10^{11}$	$1.73{\cdot}10^{6}$
21	0.696	-13	$7.51{\cdot}10^{-8}$	$1.30{\cdot}10^{12}$	$5.33{\cdot}10^{6}$
22	1.244	-8.3	$7.92{\cdot}10^{-9}$	$3.96{\cdot}10^{10}$	$1.26{\cdot}10^{7}$
23	0.676	-9.7	$8.72{\cdot}10^{-9}$	$8.02{\cdot}10^{10}$	$1.15{\cdot}10^{7}$
24	0.954	-12	$1.49{\cdot}10^{-7}$	$9.69{\cdot}10^{11}$	$4.11{\cdot}10^{6}$
25	1.656	-9.4	$3.66{\cdot}10^{-8}$	$1.37{\cdot}10^{11}$	$2.73{\cdot}10^{6}$
26	0.337	-2.7	$2.37{\cdot}10^{-8}$	$4.37{\cdot}10^{11}$	$4.30{\cdot}10^{6}$
27	1.270	-6.3	$5.03{\cdot}10^{-8}$	$2.46{\cdot}10^{11}$	$1.99{\cdot}10^{6}$
28	0.567	-5.6	$1.39{\cdot}10^{-8}$	$1.52{\cdot}10^{11}$	$7.19{\cdot}10^{6}$
29	0.443	-1.2	$3.69{\cdot}10^{-8}$	$5.17{\cdot}10^{11}$	$2.71{\cdot}10^{6}$
30	0.693	-3.3	$3.61{\cdot}10^{-8}$	$3.24{\cdot}10^{11}$	$2.77{\cdot}10^{6}$
31	0.470	-5.8	$3.63{\cdot}10^{-8}$	$4.79{\cdot}10^{11}$	$2.76{\cdot}10^{6}$
32	1.076	-5.1	$1.25{\cdot}10^{-8}$	$7.21{\cdot}10^{10}$	$8.01{\cdot}10^{6}$
33	0.142	-8.3	$7.79{\cdot}10^{-9}$	$3.40{\cdot}10^{11}$	$1.29{\cdot}10^{7}$
34	0.263	-4.3	$9.91{\cdot}10^{-9}$	$2.34{\cdot}10^{11}$	$1.01{\cdot}10^{7}$
35	0.823	2.9	$7.31{\cdot}10^{-8}$	$5.52{\cdot}10^{11}$	$1.38{\cdot}10^{6}$

Table 5.5: *Characteristic values for OTFTs on SiO_2. The total resistance was measured at floating gate.*

Sample N°	Channel length	Film thickness	Dielectric	Channel width	AR
36	$20\mu m$	20nm	PI	$200\mu m$	10
37	$10\mu m$	20nm	PI	$100\mu m$	10
38	$5\mu m$	20nm	PI	$50\mu m$	10
39	$2\mu m$	20nm	PI	$20\mu m$	10
40	$10\mu m$	20nm	PI	$100\mu m$	10
41	$20\mu m$	20nm	PI	$200\mu m$	10
42	$10\mu m$	20nm	PI	$100\mu m$	10
43	$20\mu m$	20nm	PI	$200\mu m$	10
44	$20\mu m$	40nm	PI	$200\mu m$	10
45	$10\mu m$	40nm	PI	$100\mu m$	10
46	$5\mu m$	40nm	PI	$50\mu m$	10
47	$2\mu m$	40nm	PI	$20\mu m$	10
48	$10\mu m$	40nm	PI	$100\mu m$	10
49	$20\mu m$	80nm	PI	$200\mu m$	10
50	$10\mu m$	80nm	PI	$100\mu m$	10
51	$5\mu m$	80um	PI	$50\mu m$	10
52	$20\mu m$	80nm	PI	$200\mu m$	10
53	$20\mu m$	20nm	SiO_2	$200\mu m$	10
54	$10\mu m$	20nm	SiO_2	$100\mu m$	10
55	$5\mu m$	20nm	SiO_2	$50\mu m$	10
56	$2\mu m$	20nm	SiO_2	$20\mu m$	10
57	$10\mu m$	20nm	SiO_2	$100\mu m$	10
58	$5\mu m$	20nm	SiO_2	$50\mu m$	10
59	$20\mu m$	40nm	SiO_2	$200\mu m$	10
60	$10\mu m$	40nm	SiO_2	$100\mu m$	10
61	$5\mu m$	40nm	SiO_2	$50\mu m$	10
62	$20\mu m$	40nm	SiO_2	$200\mu m$	10
63	$10\mu m$	40nm	SiO_2	$100\mu m$	10
64	$20\mu m$	40nm	SiO_2	$200\mu m$	10
65	$10\mu m$	40nm	SiO_2	$100\mu m$	10
66	$20\mu m$	80nm	SiO_2	$200\mu m$	10
67	$10\mu m$	80nm	SiO_2	$100\mu m$	10
68	$5\mu m$	80nm	SiO_2	$50\mu m$	10
69	$2\mu m$	80nm	SiO_2	$20\mu m$	10
70	$20\mu m$	80nm	SiO_2	$200\mu m$	10

Table 5.6: *Description of the measured and analyzed OTFTs on PI and SiO_2. Pentacene was deposited at* 55 °C.

Sample N°	Apparent mobility $[cm^2/Vs]$	Threshold voltage $[V]$	Conductivity $[S\,\square]$	Residual carriers $[cm^{-2}]$	Total resistance $[\Omega]$
36	0.090	0.0	$2.09{\cdot}10^{-9}$	$1.45{\cdot}10^{11}$	$4.78{\cdot}10^{7}$
37	0.085	0.1	$2.10{\cdot}10^{-9}$	$1.50{\cdot}10^{11}$	$4.70{\cdot}10^{7}$
38	0.100	-0.1	$2.65{\cdot}10^{-9}$	$1.65{\cdot}10^{11}$	$3.78{\cdot}10^{7}$
39	0.085	0.4	$2.59{\cdot}10^{-9}$	$1.89{\cdot}10^{11}$	$3.68{\cdot}10^{7}$
40	0.111	-0.2	$2.67{\cdot}10^{-9}$	$1.49{\cdot}10^{11}$	$3.75{\cdot}10^{7}$
41	0.062	-0.4	$1.60{\cdot}10^{-9}$	$1.60{\cdot}10^{11}$	$6.26{\cdot}10^{7}$
42	0.021	1.1	$4.81{\cdot}10^{-9}$	$1.41{\cdot}10^{12}$	$8.32{\cdot}10^{7}$
43	0.024	3.3	$2.13{\cdot}10^{-9}$	$5.52{\cdot}10^{11}$	$4.69{\cdot}10^{7}$
44	0.151	0.1	$1.81{\cdot}10^{-9}$	$7.46{\cdot}10^{10}$	$5.52{\cdot}10^{7}$
45	0.119	-1.0	$1.98{\cdot}10^{-9}$	$1.03{\cdot}10^{11}$	$5.05{\cdot}10^{7}$
46	0.145	-2.5	$1.93{\cdot}10^{-9}$	$8.25{\cdot}10^{10}$	$5.20{\cdot}10^{7}$
47	0.269	-0.8	$4.98{\cdot}10^{-9}$	$1.15{\cdot}10^{11}$	$2.01{\cdot}10^{7}$
48	0.198	2.7	$1.63{\cdot}10^{-9}$	$5.10{\cdot}10^{10}$	$6.16{\cdot}10^{7}$
49	0.335	5.0	$2.15{\cdot}10^{-8}$	$3.98{\cdot}10^{11}$	$4.66{\cdot}10^{6}$
50	0.331	5.0	$2.34{\cdot}10^{-8}$	$4.14{\cdot}10^{11}$	$4.28{\cdot}10^{6}$
51	0.362	4.4	$2.18{\cdot}10^{-8}$	$3.74{\cdot}10^{11}$	$4.59{\cdot}10^{6}$
52	0.325	6.2	$2.43{\cdot}10^{-8}$	$4.64{\cdot}10^{11}$	$4.12{\cdot}10^{6}$
53	0.034	-4.8	$1.61{\cdot}10^{-9}$	$8.47{\cdot}10^{10}$	$6.68{\cdot}10^{7}$
54	0.037	1.5	$2.85{\cdot}10^{-9}$	$2.31{\cdot}10^{11}$	$3.50{\cdot}10^{7}$
55	0.061	0.9	$3.16{\cdot}10^{-9}$	$1.69{\cdot}10^{11}$	$3.16{\cdot}10^{7}$
56	0.022	6.0	$5.63{\cdot}10^{-9}$	$1.76{\cdot}10^{11}$	$1.78{\cdot}10^{7}$
57	0.031	-4.8	$1.02{\cdot}10^{-9}$	$6.10{\cdot}10^{10}$	$9.78{\cdot}10^{7}$
58	0.028	-3.9	$1.31{\cdot}10^{-9}$	$1.15{\cdot}10^{11}$	$7.61{\cdot}10^{7}$
59	0.636	-0.2	$3.67{\cdot}10^{-8}$	$2.73{\cdot}10^{11}$	$2.73{\cdot}10^{6}$
60	0.638	0.4	$3.91{\cdot}10^{-8}$	$2.92{\cdot}10^{11}$	$2.56{\cdot}10^{6}$
61	0.459	2.5	$3.92{\cdot}10^{-8}$	$3.42{\cdot}10^{11}$	$2.55{\cdot}10^{6}$
62	0.430	4.7	$4.32{\cdot}10^{-8}$	$7.82{\cdot}10^{11}$	$2.31{\cdot}10^{6}$
63	0.664	0.5	$4.17{\cdot}10^{-8}$	$3.06{\cdot}10^{11}$	$2.40{\cdot}10^{6}$
64	0.584	-0.5	$1.40{\cdot}10^{-8}$	$1.00{\cdot}10^{11}$	$7.16{\cdot}10^{6}$
65	0.667	-2.0	$7.92{\cdot}10^{-8}$	$3.96{\cdot}10^{11}$	$1.26{\cdot}10^{7}$
66	0.265	-1.6	$5.89{\cdot}10^{-9}$	$6.58{\cdot}10^{10}$	$1.70{\cdot}10^{7}$
67	0.346	-1.5	$8.72{\cdot}10^{-9}$	$8.02{\cdot}10^{10}$	$1.15{\cdot}10^{7}$
68	0.397	-0.5	$1.39{\cdot}10^{-9}$	$1.52{\cdot}10^{11}$	$7.19{\cdot}10^{6}$
69	0.077	-1.7	$7.79{\cdot}10^{-9}$	$3.40{\cdot}10^{11}$	$1.29{\cdot}10^{7}$
70	0.349	0.4	$1.38{\cdot}10^{-8}$	$1.06{\cdot}10^{11}$	$7.27{\cdot}10^{6}$

Table 5.7: *Characteristic values for OTFTs on PI and SiO_2. The total resistance was measured at floating gate.*

Chapter 6

The Dielectric Surfaces: Silicon Oxide & Polyimide

The surface of the dielectric is crucial for an efficient charge transport in the conducting channel located near the dielectric-pentacene interface. The surface defects of the dielectric determine the surface energy, the reactivity, the coupling and trapping properties thus the electric performance of the organic thin-film transistors (OTFTs) is influenced by the nature and order of the dielectric surface.
We have varied the defect densities on silicon oxide (SiO_2) and polyimide (PI) dielectric using surface treatments prior to the pentacene deposition. The effects of the different types of defects can be observed in the electric performance and film morphology. The defects which are responsible for the trapping and charge transfers are separated from those which determine the morphology of the pentacene film. The probability for a charge transfer is correlated with the energy level of the involved defect.

6.1 Defects on the dielectric surface

Defects are always present at the dielectric surface [23, 52]. The nature and density depend on the processing of the dielectric and the transistor. The defects perturb the order at the dielectric surface. They are also electroactive centers which strongly affect the channel formation and the charge transport. The effect of a defect species depends on its nature; some defects act as traps while others cause a charge transfer. Moreover the defects influence the pentacene film growth. On hydrophobic oxide surfaces, pentacene grows layer by layer while on polymeric or hydrophilic oxide surfaces, the film growth is three-dimensional (see Chapter 4).

6.2 Silicon oxide

6.2.1 Defects on silicon oxide

On the silicon oxide surface (SiO_2), there is a wide variety of electroactive centers, e.g. radicals, charged and non-charged diamagnetic groups. The most common de-

fects are $\equiv Si\text{-}OH$ (silanol), $\equiv Si\bullet$, $\equiv Si\text{-}O\bullet$, $\equiv Si\text{-}O\text{-}O\bullet$ (oxygen-centered and oxygen-free radicals), $\equiv Si\text{-}Si\equiv$, $\equiv Si\text{-}O\text{-}O\text{-}Si\equiv$ (peroxy group) and $\equiv Si\text{-}H$ (silicon hydride) (see Fig. 6.1a). The balance between the defects can be changed by surface treatments.
Plasma treatments control radical and non-radical species. The former is unstable, the latter stable with time. The created species depend on the type of plasma (see Figure 6.1a).
If the substrate is immersed in aqueous solutions, the ratio of $\equiv Si\text{-}OH$ and $\equiv Si\text{-}O^-$ is varied depending on the pH value of the solution (see Fig. 6.1b). In basic solutions, the silanol groups ($\equiv Si\text{-}OH$) deprotonate and become negatively charged ($\equiv Si\text{-}O^-$). Due to the pH, the ratio between silicate ($\equiv Si\text{-}O^-$) and silanol ($\equiv Si\text{-}OH$) varies. The counterion from the solution stabilizes the charge at the surface.

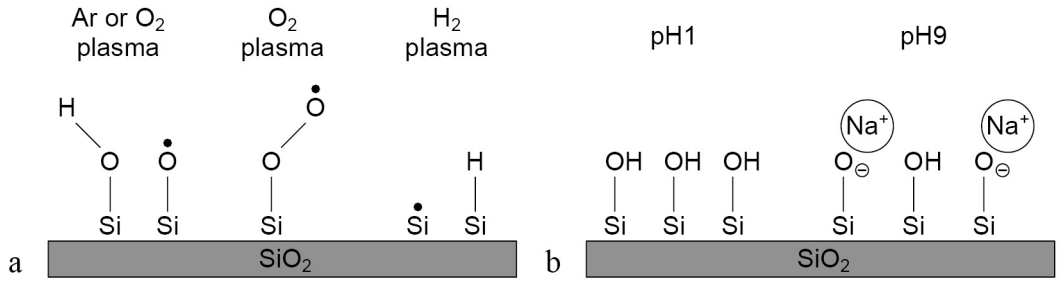

Figure 6.1: *Defect species created a) by plasma treatments and b) by immersion in solutions with different pH values.*

In the present work, we have used both plasma treatments and pH solutions to vary the different defect concentrations at the oxide dielectric interface.

6.2.2 Transistor performance

The OTFT performance is strongly determined by the type of plasma and pH treatment used for treating the dielectric surface. The SiO_2 surface is treated by Ar, O_2 and H_2 plasma and by aqueous solutions with pH values from 0.5 to 9. The transistors on SiO_2 treated by Ar or O_2 plasma have elevated current, positive threshold, elevated residual carrier density, and a linear transfer curve (see Fig. 6.2a, c and Table 6.1). The electrical performance is determined by the presence of residual carriers. On the contrary, H_2 plasma and pH treatments lead to a performance comparable to the one of untreated transistors: small current, negative threshold, non-linear transfer curve and a saturation regime at elevated drain voltage (see Fig. 6.2 and Table 6.1). The transport properties are determined by the trap distribution.

On plasma-treated SiO_2, pentacene grows layer by layer as on bare SiO_2; thus the defects created by the plasma treatments (Ar, H_2 and O_2 plasma) do not change the film growth (see Chapter 4). After immersion in pH solutions, the film morphology depends on the pH because the wettability changes with the ratio of $\equiv Si\text{-}OH/\equiv Si\text{-}O^-$. On basic treated SiO_2 (mainly $\equiv Si\text{-}O^-$), the pentacene film grows 3-dimensionally in small islands. After the other pH treatments, the film grows layer

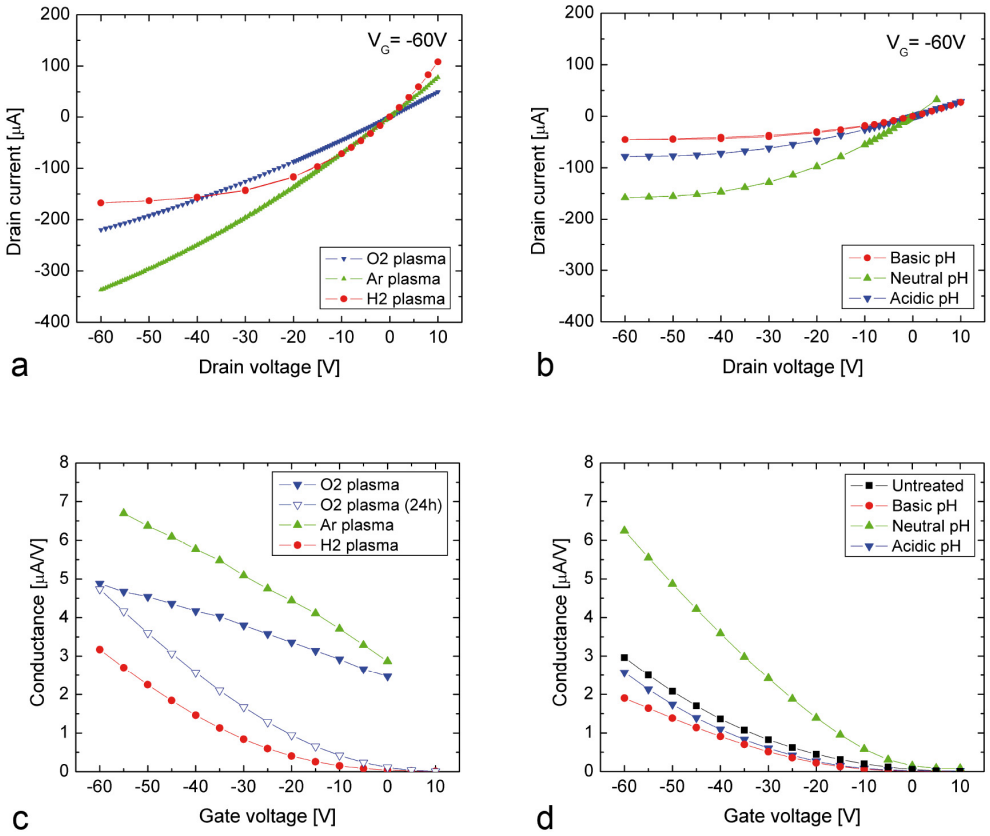

Figure 6.2: *Output (a, b) and transfer curves (c, d) of OTFTs with a SiO_2 dielectric treated by plasmas (a, c) and by pH solutions (b, d).*

by layer. The microstructure of the pentacene film plays a minor role compared to the trap distribution and the charge transfer centers. The same film morphology does not mean that the transistor performance is the same (see Chapter 4).

	Residual carriers $[cm^{-2}]$	Threshold voltage $[V]$	Apparent mobility $[cm^2/Vs]$	Film conductivity $[S\,\square]$	Contact resistance $[\Omega]$
Untreated	$8.4 \cdot 10^{11}$	-27	0.33	$4.1 \cdot 10^{-8}$	$1.2 \cdot 10^{7}$
pH=0.5	$6.7 \cdot 10^{11}$	-30	0.30	$3.2 \cdot 10^{-8}$	$1.1 \cdot 10^{7}$
pH=5	$2.6 \cdot 10^{11}$	-15	0.65	$2.8 \cdot 10^{-8}$	$9.0 \cdot 10^{6}$
pH=9	$7.2 \cdot 10^{11}$	-25	0.24	$2.8 \cdot 10^{-8}$	$1.8 \cdot 10^{7}$
H_2 plasma	$3.4 \cdot 10^{11}$	-24	0.56	$2.8 \cdot 10^{-8}$	$1.3 \cdot 10^{7}$
Ar plasma	$1.0 \cdot 10^{13}$	>50	0.32	$5.2 \cdot 10^{-7}$	$1.0 \cdot 10^{5}$
O_2 plasma	$1.2 \cdot 10^{13}$	>50	0.22	$4.2 \cdot 10^{-7}$	$1.5 \cdot 10^{5}$
O_2 plasma (24h)	$3.0 \cdot 10^{11}$	-17	0.38	$1.8 \cdot 10^{-8}$	$8.2 \cdot 10^{6}$

Table 6.1: *Characteristic values of OTFTs with a SiO_2 dielectric treated by plasma or pH solutions.*

6.2.3 Defects and charge transfer

The defects which are responsible for the charge transfer appear in the residual carrier density. If there is a high number of charge transfer centers, there are many residual carriers in the channel.
After H_2 plasma treatment ($\equiv Si\bullet$, $\equiv Si\text{-}H$), no additional residual carriers are measured, thus the defects $\equiv Si\bullet$ and $\equiv Si\text{-}H$ are not involved in charge transfer although a radical species is formed. Plasma treatments with Ar ($\equiv Si\text{-}OH$, $\equiv Si\bullet$, $\equiv Si\text{-}O\bullet$) and O_2 (additionally $\equiv Si\text{-}O\text{-}O\bullet$) lead to an increase in residual carrier density. Some or all of these defects, therefore, act as charge transfer centers. The role of the defects is distinguished by their temporal stability. The radical species disappear with time while the silanol groups ($\equiv Si\text{-}OH$) remain on the surface. If pentacene is deposited 24h after the O_2 plasma treatment, the radicals are annihilated and transformed into silanol groups. The transistors fabricated after this treatment have a residual carrier density comparable to those of an untreated transistor (see Table 6.1). That means that the O-centered radicals are responsible for the charge transfer between the dielectric surface and pentacene.
The Ar plasma does not introduce oxygen molecules but there are so many O atoms at the SiO_2 surface that many O-centered radicals are formed. Thus the effect of the Ar plasma is similar to the O_2 plasma.

6.2.4 Energy levels

There are possibilities to transfer electrons from the pentacene layer to surface defects of the oxide dielectric interface. The charge transfer probability depends on the fact that the energy difference between the acceptor level (electron affinity) and the donor level (ionization potential) is small. The ionization potential of pentacene is $6.6eV$ in vapor phase [122]. The ionization potential is also determined by ultraviolet photoelectron spectroscopy (UPS); thereby it is measured for electrons in

the excited state and includes the polarization energy. In the case of pentacene, the molecule is easily polarizable; the polarization energy is about $1.5eV$ [46]. Therefore the ionization potential determined in the gas phase (for a neutral molecule) is more relevant for the charge transfer at the SiO_2-pentacene interface.
The electron affinities of $\equiv$*Si-Si*$\equiv$, $\equiv$*Si-H*$\bullet$, $\equiv$*Si-OH* and $\equiv$*Si*$\bullet$ are between 2.2 and $4.5eV$ (see Table 6.2). Thus the probability of a charge transfer is low. On the contrary, the electron affinities of $\equiv$*Si-O*$\bullet$ and $\equiv$*Si-O-O*$\bullet$ are between 5.4 and $7.1eV$, respectively, and a charge transfer is highly probable. The peroxy group $\equiv$*Si-O-O-Si*$\equiv$ is also a candidate ($5.2eV$) but this defect is not distinguishable by plasma and pH treatments.

	Electron affinity $[eV]$	Residual carriers $[cm^{-2}]$
$\equiv$*Si-O-O*$\bullet$, $\equiv$*Si-O*$\bullet$	$5.5 - 7.1$	$0.36 - 1.2 \cdot 10^{13}$
$\equiv$*Si-OH*	$\approx$ 4	$2.6 - 6.7 \cdot 10^{11}$
$\equiv$*Si*$\bullet$	4.5	$3.4 \cdot 10^{11}$
$\equiv$*Si-H*	$\approx$ 3	$3.4 \cdot 10^{11}$
$\equiv$*Si-Si*$\equiv$	$\approx$ 2.2	
$\equiv$*Si-O-O-Si*$\equiv$	$\approx$ 5.2	

Table 6.2: *Electron affinities for defects on SiO_2 and the residual carrier density measured in the corresponding OTFTs.*

The transfer of the electron occurs from the neutral pentacene molecule to the neutral radical. Afterwards, the charged defect is localized at the interface and a hole delocalizes between the pentacene molecules. Both pentacene and the oxide network are polarized and the polarization energies shift the energy levels; therefore, the charge transfer is irreversible and a back reaction is not likely.

6.2.5 Contact resistance, apparent mobility and threshold voltage

In the previous chapter we saw, that the performance of OTFTs on untreated SiO_2 is affected by the number of residual carriers in pentacene. The plasma treatments result in a large range of residual carriers caused by charge transfer reactions. For O_2 and Ar plasma treated OTFTs, the residual carrier density is elevated and therefore, the apparent mobility increases with residual carrier density (see Fig. 6.3). The contact resistance decreases at the same time; it reaches about $0.1M\Omega$ at 10^{13} residual carriers per cm^2 (see Fig. 6.4). For such elevated residual carriers as after O_2 and Ar plasma, a strong dependence of the threshold voltage on the residual carrier density is expected; however, there are several transistors with a negative threshold voltage (see Fig. 6.5). A reason could be that the plasma treatments introduce, besides the residual carriers, deep traps that have the opposite effect on the threshold.

The performance of the transistors on SiO_2 treated by H_2 plasma or immersed in pH solutions (independent of the pH value) is dominated by the presence of traps.

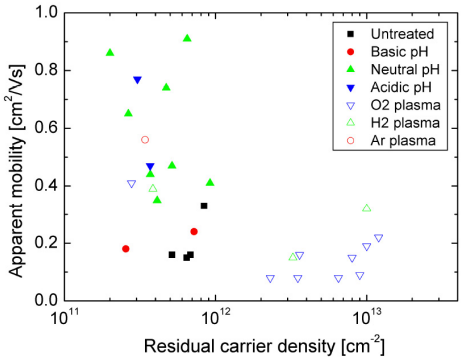

Figure 6.3: *Apparent mobility vs. residual carrier density for pH treated and plasma treated transistors.*

After Ar and O_2 plasma treatments, the electric performance is determined by the residual carriers and deep traps.

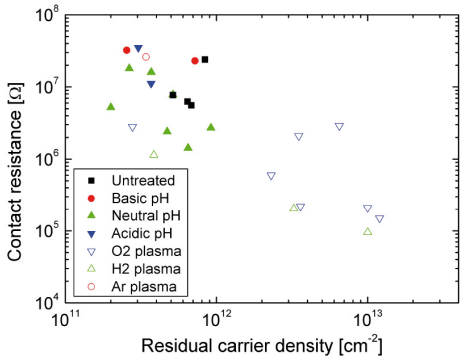

Figure 6.4: *Contact resistance vs. residual carrier density for pH treated and plasma treated transistors.*

In pH-treated transistors, the residual carrier density is at a maximum $10^{12}cm^{-2}$, i.e. it is low, and thus the threshold voltage does not depend on the residual carrier density (see Fig. 6.5). The apparent mobility decreases when the residual carrier density increases; the lowest values were measured at about $10^{12}cm^{-2}$ (see Fig. 6.3). The contact resistance decreases with increasing residual carrier density (see Fig. 6.3).

In conclusion, the OTFT performance is determined by the treatments of the SiO_2 surface prior to the pentacene deposition. O-centered radicals (introduced by O_2 and Ar plasma) cause charge transfer reactions and thereby introduce residual carriers into pentacene which determine the electric behavior of the transistors. O-free radicals, silanol (also deprotonated) and silicon hydride groups (introduced by

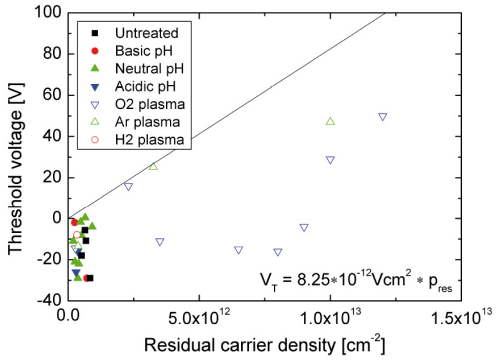

Figure 6.5: *Threshold voltage vs. residual carrier density for pH-treated and plasma-treated transistors. The slope of the straight line is calculated by the capacitance of the dielectric, $C_{gate} = 19.8nF/cm^2$ for SiO_2 (according to Daraktchiev et al. [50]).*

H_2 plasma and pH treatments) do not change the electric performances which resembles those of an OTFT on untreated SiO_2 dielectric. The apparent mobility and the contact resistance depend on the residual carrier density, while the threshold voltage is in some cases negative even for elevated residual carrier densities.
The pentacene film morphology is affected by deprotonated silanol groups (after basic pH treatment), but the morphology change does not perturb the electric behavior of the OTFT.

6.3 Polyimide

Polyimide (PI) as dielectric layer brings on a change in the properties of the OTFT (see Chapter 4 and 5). The pentacene film grows three-dimensionally on the top of PI. The electric performance is changed and the OTFTs are more sensitive to breakthrough and high leakage currents than transistors with an oxide dielectric. Therefore, the OTFTs with PI as dielectric were fabricated using also short channel lengths and with a pentacene film evaporated at RT.
We observed that the use of a plasma treatment on the polyimide surface was a good way to improve the performance of transistors made on polyimide. Therefore, the PI surface is treated by O_2, Ar and H_2 plasma, the same procedure as on SiO_2 except that the exposure time is reduced to 10s instead of 2 minutes in order to avoid a degradation of the polymeric layer.

6.3.1 Defects on the polyimide surface

A plasma treatment changes the chemistry and the morphology of the PI surface. The main effects of plasma are the etching and degradation and the formation of radicals in the polymer chains [108]. The element composition is changed by the im-

plantation of plasma atoms which form new functionalities at the polymeric surface. The plasma treatments increase the wettability (contact angle and surface energy decrease) and both the morphology and surface roughness are drastically changed [110, 111, 112]. The wettability is significantly enhanced due to oxidations and the introduction of polar groups. After O_2 and Ar plasma, the imide circles are opened by the implantation of carboxylate groups (-$COOH$); the density of carboxylate groups is higher after O_2 plasma. If the O_2 plasma activated PI is covered with a Cu/Ti layer, a chemical bond is formed between titanium and the PI surface [123]. We do not know the electron affinity of the carboxylate group on PI, however it can be estimated by the ionization potential of the species that reacts with it, for instance titanium with an ionization potential of $6.8eV$. Thus the electron affinity of the carboxylate group is estimated to be in the same range.

Ion bombardment results in the implantation of molecules and broken bonds in the PI film; similar effects occur during the plasma treatment and therefore, the species introduced by ion bombardment are also candidates for being formed during plasma treatments with the same atoms. The bombardment of a PI layer with O_2^+ ions results in an increase in carbonyl groups ($=C=O$) which decreases the contact angle [109]. If the activated PI layer is covered with copper, an electron transfer occurs from copper to the carbonyl group. The ionization energy of copper is $7.7eV$ [124], thus the electron affinity of the carbonyl group has to be close to this value. After Ar^+ ion bombardment, the density of carbonyl groups is reduced, and amides and anions are formed [125]. An Ar^+ ion activated PI layer does not react with aluminium [126].

The exact structure of the PI used here is not declared by *HD Microsystems*, therefore, there could be additional entities formed by unknown side groups.

If pentacene is deposited on the plasma treated PI surface, charge transfer reactions may occur. It is probable if the energy level different is small, i.e. if the electron affinity of the species on PI is close to the ionization potential of unpolarized pentacene.
The plasma treatments lead to a slightly increased grain size and the disappearance of the fiber-like grains on bare PI (see Chapter 4). The increase in wettability after Ar and O_2 plasma does not disturb the film growth because it is dominated by the surface roughness which already leads to a 3-dimensional growth.

6.3.2 Transistor performance

The performance of the OTFTs with PI as dielectric depends on the plasma treatments (see Fig. 6.6 and Table 6.3). After O_2 plasma treatment, the OTFTs show the highest values of apparent mobility, residual carrier density and conductivity and the lowest values of total resistance. The threshold is shifted to values higher than 20V.

If PI is treated by H_2 plasma, the apparent mobility, residual carrier density, and conductivity are lowered, the threshold is small and negative and the total resistance

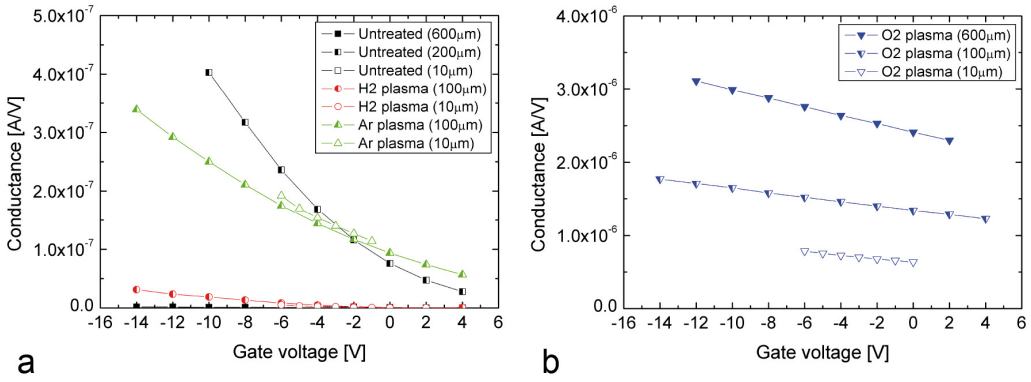

Figure 6.6: *a) Transfer curves of OTFTs with untreated and plasma treated PI dielectrics, b) transfer curves of OTFTs with PI treated by O_2 plasma.*

elevated. The values of *Ar* plasma treated OTFTs are in between.

	Channel length $[\mu m]$	Apparent mobility $[cm^2/Vs]$	Threshold voltage $[V]$	Conductivity $[S\ \square]$	Residual carriers $[cm^{-2}]$	Total resistance $[\Omega]$
Untreated	600	0.001	-2.0	$2.3 \cdot 10^{-10}$	$1.4 \cdot 10^{12}$	$5.3 \cdot 10^{7}$
Untreated	200	0.329	0.9	$9.5 \cdot 10^{-10}$	$1.8 \cdot 10^{11}$	$3.5 \cdot 10^{6}$
Untreated	10	0.085	0.1	$2.1 \cdot 10^{-9}$	$1.5 \cdot 10^{11}$	$4.7 \cdot 10^{7}$
H_2 plasma	600			$1.9 \cdot 10^{-9}$		$5.1 \cdot 10^{7}$
H_2 plasma	100	0.025	-3.1	$2.8 \cdot 10^{-10}$	$7.0 \cdot 10^{10}$	$5.9 \cdot 10^{7}$
H_2 plasma	10	0.010	-1.3	$4.2 \cdot 10^{-10}$	$2.7 \cdot 10^{11}$	$1.2 \cdot 10^{8}$
Ar plasma	600			$1.8 \cdot 10^{-9}$		$5.6 \cdot 10^{7}$
Ar plasma	100	0.189	2.4	$1.6 \cdot 10^{-9}$	$4.0 \cdot 10^{11}$	$1.0 \cdot 10^{7}$
Ar plasma	20	0.126	7.2	$8.8 \cdot 10^{-9}$	$4.3 \cdot 10^{11}$	$5.6 \cdot 10^{7}$
O_2 plasma	600	0.555	27	$1.7 \cdot 10^{-7}$	$2.0 \cdot 10^{12}$	$5.7 \cdot 10^{5}$
O_2 plasma	100	0.560	43	$1.4 \cdot 10^{-8}$	$3.1 \cdot 10^{11}$	$1.2 \cdot 10^{6}$
O_2 plasma	10	0.253	22	$6.4 \cdot 10^{-8}$	$1.6 \cdot 10^{12}$	$7.8 \cdot 10^{5}$

Table 6.3: *Characteristic values for OTFTs with untreated and plasma treated PI dielectrics.*

The performance of transistors with untreated *PI* varies strongly. For long channels, the transistors are either "good" or "bad", while the variation is much smaller for short-channel transistors (see Fig. 6.6 and 6.8).

The transistor performance is independent of the channel length (see Fig. 6.7). The exceptions are the values of apparent mobility in O_2 plasma-treated transistors. The apparent mobilities of long-channel transistors are almost twice as high as the ones for short-channel transistors. The change in the characteristic values arises from the different surface treatments (see Fig. 6.8).

For long-channel transistors, the channel and contact resistance are determined separately by conductivity measurements at floating gate. They were also mea-

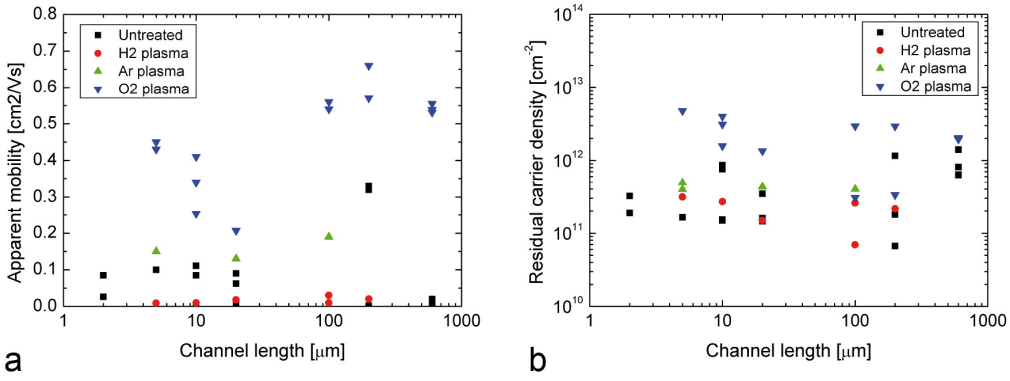

Figure 6.7: *a) Apparent mobility and b) residual carrier density vs. channel length of OTFTs with untreated and plasma treated PI dielectrics.*

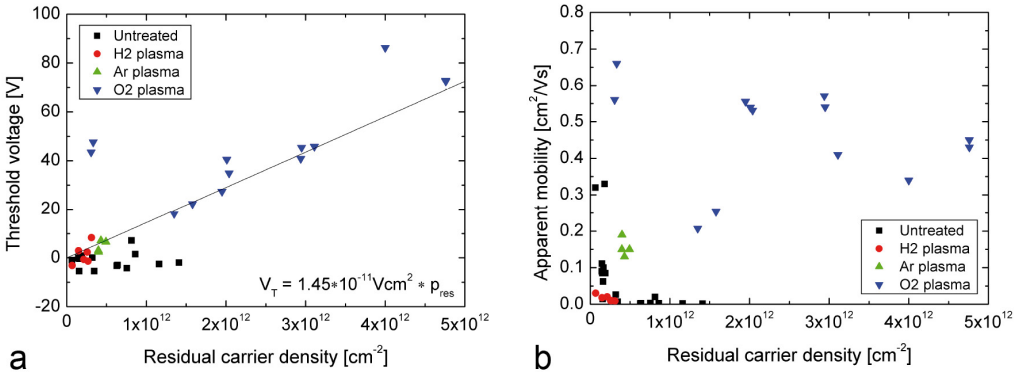

Figure 6.8: *a) Conductivity and b) apparent mobility vs. residual carrier density of OTFTs with untreated and plasma treated PI dielectrics.*

sured if the transistor shows no transistor response in the measuring range of the gate voltage due to the elevated resistances. The values are similar for untreated PI and after H_2 and Ar plasma treatment (in the range of $R_{channel} = 10^7\Omega$ and $R_{contact} = 4 \cdot 10^7\Omega$), and the contact contribution is high ($R_{contac}/R_{tot} = 0.8$). The performance is contact limited at floating gate (see Table 6.4).
The transistors on PI treated by O_2 plasma have a much smaller resistances and the performance is dominated by the channel (Ratio of $R_{contac}/R_{tot} = 0.1$).

	Total resistance	Channel resistance	Contact resistance	Ratio R_C/R_{tot}
Untreated	$5.3 \cdot 10^7$	$8.9 \cdot 10^6$	$4.4 \cdot 10^7$	0.83
H_2 plasma	$5.1 \cdot 10^7$	$1.1 \cdot 10^7$	$4.0 \cdot 10^7$	0.78
Ar plasma	$5.6 \cdot 10^7$	$1.4 \cdot 10^7$	$4.2 \cdot 10^7$	0.74
O_2 plasma	$5.7 \cdot 10^5$	$5.2 \cdot 10^5$	$5.5 \cdot 10^4$	0.10

Table 6.4: *Total, film and contact resistance of long-channel transistors ($L = 600\mu m$) measured at floating gate.*

6.3.3 Energy levels

By the O_2 plasma treatment, many residual carriers are introduced into pentacene and the Ar and H_2 plasma cause less charge transfer (see Fig. 6.7b).

The charge transfer centers are species introduced by the plasma treatments. The O_2 plasma increases the number of carboxylate and carbonyl groups which have an electron affinity close to 6.8 and $7.7eV$, respectively (see Table 6.5). Thus, it is likely they react with the pentacene molecules and introduce residual carriers into pentacene film. The electron affinity is estimated by the metal atoms which react with the activated PI surface.

Surface species	Plasma treatment	Electron affinity	Reactivity
Carboxylate ($-COOH$)	O_2, Ar plasma	Close to $6.8eV$	With Ti
Carbonyl ($=C=O$)	O_2 plasma	Close to $7.7eV$	With Cu
Amide	Ar plasma		With H_2O

Table 6.5: *Surface species created by plasma treatments on the top of polyimide dielectric.*

After the Ar plasma, carboxylate groups are formed on PI but the number is lower than after O_2 plasma treatment. The carbonyl groups are removed and therefore, their density decreases. Charge transfer centers are formed, but at a reduced concentration compared to after O_2 plasma treatment. That can be seen in the significantly lower residual carrier density of Ar plasma treated transistors (see Figure 6.7b). On SiO_2 otherwise, the effect of the Ar plasma is similar to the one on O_2 plasma due to the higher density of oxygen on the oxide surface.

After H_2 plasma treatment, the residual carrier density is low, i.e. only a few charge transfer reactions occur, therefore, the effect of the H_2 plasma is most likely the passivation of reactive species on PI.

6.3.4 Apparent mobility and threshold voltage

The O_2 plasma introduces many residual carriers into pentacene, thus the performance should be dominated by the residual carriers, and the measured threshold voltages are proportional to the residual carrier density (slope of $1.45 \cdot 10^{-11} V cm^2$ with a gate capacitance C_{gate} of $11 nF/cm^2$ of PI, see eq. 3.3, see Fig. 6.9a). For the other transistors, the residual carrier densities are low and the threshold voltages are close to zero. A different behavior is observed for untreated PI: the threshold voltages are close to zero although the residual carrier densities reach values higher than $10^{12} cm^{-2}$.

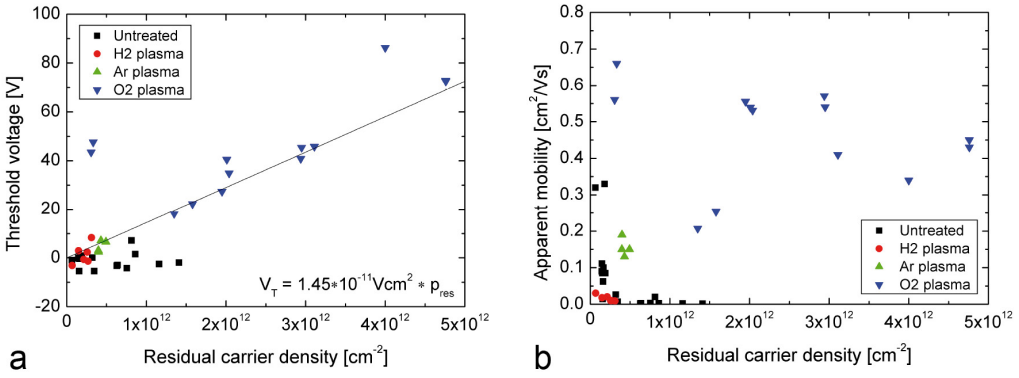

Figure 6.9: *a) Threshold voltage and b) apparent mobility vs. residual carrier density of OTFTs with untreated and plasma treated PI dielectrics.*

For H_2 plasma-treated and untreated transistors, the apparent mobility increases with decreasing residual carrier density (see Fig. 6.9b). After O_2 plasma treatment, the apparent mobility increases with the residual carrier density (above $10^{12} cm^{-2}$) before it becomes constant at $3 \cdot 10^{12}$ residual carriers per cm^2. The values of Ar plasma treated transistors are too close together to affirm the correlation.

The OTFTs on O_2 plasma treated PI show an electric performance dominated by the residual carriers. The performance of transistors on H_2 plasma treated PI are dominated by traps; after Ar plasma treatment, the transistors are in between.

6.4 Conclusion

The organic thin-film transistors were fabricated with silicon oxide (SiO_2) or polyimide (PI) as a dielectric surface. The nature of the dielectric surface was modified by pH solutions and plasma treatments. The introduced defects are separated by their effect on the transistors.
In OTFTs on SiO_2, oxygen-centered radicals (formed by O_2 or Ar plasma) act as charge transfer centers and introduce residual carrier centers into pentacene. Consequently, the electric performance of the OTFTs is determined by the residual carriers. The threshold voltage indicates that deep traps are also created by the O_2 plasma. Deprotonated silanol (after immersion in basic pH solutions) otherwise change the pentacene film growth from the layer-by-layer mode to the 3-dimensional mode; the electrical performance is not affected. For the other defects (oxygen-free radicals, silicon hydride and silanol groups) and surface treatments (H_2 plasma, neutral and acidic pH solutions), the electric performance and the pentacene film morphology is similar to the transistors on untreated SiO_2, i.e. dominated by traps.

On PI, the plasma treatments lead to a variation in residual carrier density. The highest values were measured after O_2 plasma treatment, the lowest after H_2 plasma. The values after Ar plasma treatment are in between. The O_2 plasma introduces carboxylate and carbonyl groups which most likely act as charge transfer centers. The performance is dominated by the residual carriers. The Ar plasma forms carboxylate (in a smaller density than O_2 plasma) and amid groups, but reduces the number of carbonyl groups resulting in a decrease in the residual carrier density. The performance is in an intermediate regime between residual carrier and trap domination. The H_2 plasma decreases the residual carrier density; the performance is dominated by traps.
The pentacene film morphology is slightly improved (removal of the fiber-like grains) by the plasma treatments, but the film growth is still dominated by the PI roughness (3-dimensional growth mode).

The nature of the dielectric surface determines the electric performance of the transistors, thus the dielectric surface should be treated with caution. To overcome this, the dielectric surface can be passivated by a self-assembled monolayer. In the next chapter, the effect of self-assembled monolayers at the dielectric-pentacene interface is analyzed.

Chapter 7

Self-Assembled Monolayers

For organic thin-film transistors on SiO_2, performance is related to the nature of the SiO_2 surface and can be overcome by passivating the oxide by a self-assembled monolayer (SAM). The SAM separates the organic semiconductor and the oxide and covers the defects on the oxide (see Fig. 7.1). The effect of the SAM on transistor performance depends on the length and the chemical nature of the SAM molecules.

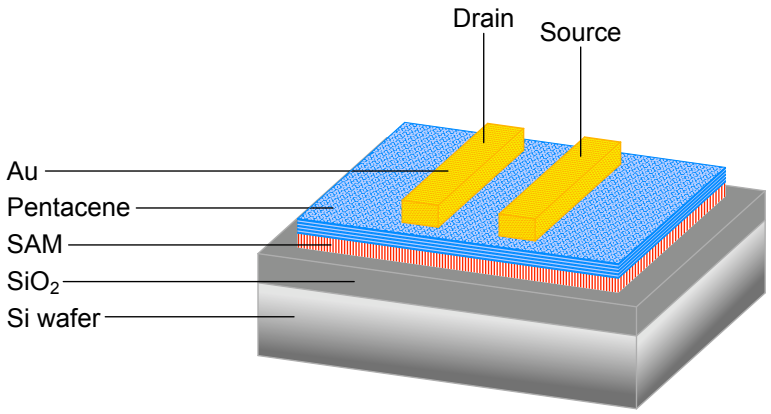

Figure 7.1: *OTFT architecture with a SAM at the dielectric-pentacene interface.*

We introduced neutral and polar SAMs at the oxide-pentacene interface of OTFTs with long channels. The polar SAMs are benzoic acid derivatives carrying a dipole moment. The neutral SAM is a long aliphatic chain with a benzene as end group. The effect of a monolayer on the threshold, apparent mobility and concentration of residual carriers is analyzed. The monolayer introduces a new surface and the growth mode of the semiconductor film deposited on it can also change. The molecules used are presented in Fig. 7.2.

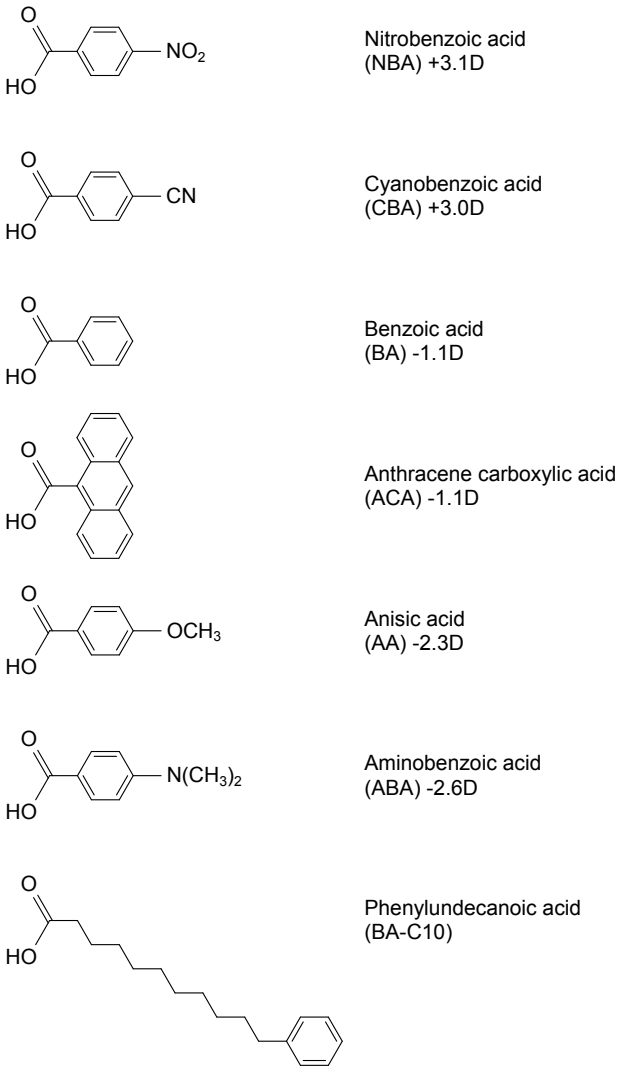

Figure 7.2: *Molecules which are used to form the self-assembled monolayers on the top of the oxide dielectric.*

7.1 A neutral self-assembled monolayer

A SAM at the dielectric-semiconductor interface passivates the oxide dielectric. If the SAM is neutral (i.e. consists of an aliphatic chain and/or a benzene structure), the monolayer can be described as a spacer. The spacer increases the distance between the charge carrier in the semiconductor and the defects on the oxide surface. The trapping energy of the traps on the oxide is then decreased and, as a consequence, the apparent mobility is increased.

The effect of a neutral SAM is demonstrated by a benzoic acid with a $10C$ long aliphatic chain (*BA-C10*). The transistors contain a 10nm thick pentacene film (evaporated at 55 °C) and have a channel length of $600\mu m$. The untreated dielectric is SiO_2. For a successful grafting of *Ba-C10*, an additional thin Al_2O_3 layer is needed (see Chapter 3).
The performance of the *BA-C10* modified OTFT is strongly enhanced and the drain current is about 8 times higher (see Fig. 7.3).

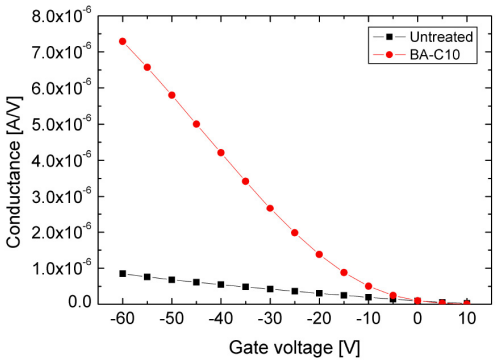

Figure 7.3: *Transfer curves for OTFTs with untreated and BA-C10 modified oxide dielectric.*

The SAM modification brings on a strong increase in apparent mobility and a drop in residual carrier density. It is a result of the fact that *BA-C10* is relatively long thus the coupling and trapping effects are reduced and the charge transfer probability is low (see Table 7.1). At gate voltages above zero, the drain currents are smaller after the SAM modification, thus the off-state of the transistor is improved.

	Apparent mobility $[cm^2/Vs]$	Film conductivity $[S\,\square]$	Threshold voltage $[V]$	Residual carriers $[cm^{-2}]$	Channel resistance $[\Omega]$	Contact resistance $[\Omega]$
Untreated	0.08	$1.70 \cdot 10^{-8}$	-7	$1.29 \cdot 10^{12}$	$5.90 \cdot 10^{6}$	$4.04 \cdot 10^{6}$
BA-C10	0.79	$1.11 \cdot 10^{-8}$	-13	$8.65 \cdot 10^{10}$	$9.02 \cdot 10^{6}$	$2.32 \cdot 10^{7}$

Table 7.1: *Characteristic values for OTFTs with untreated and SAM modified oxide dielectric, respectively.*

In conclusion, the introduction of a long, neutral self-assembled monolayer neutralizes the effects of the dielectric surface resulting in strong enhancement of the transistor performance.

7.2 Polar self-assembled monolayers

A polar monolayer does not only act as spacer but also introduces an internal field due to the dipole moment. Charge transfers across the SAM are also affected by the internal field. Depending on the dipole moment, the charge transfer is enhanced or hindered. Due to the polar end groups, the surface wettability can change and in turn affect the morphology of the semiconductor film. The polar end groups can also act as charge transfer centers, thereby resulting in an increase in residual carrier density.

From an electrical point of view, the dipolar lattice induces both an average shift and a modulation of the potential experienced by a charge. The amplitude of the modulation depends on the distance between the molecules of the SAM and the thickness of the monolayer. If the distance between the molecules is large compared to the SAM thickness, the modulation is high and charge carriers in the organic semiconductor are trapped in the potential wells. In the case of perfect order in the layer, this potential introduces a new periodicity which is in general different from the pentacene periodicities. For shorter distances, the modulation is low with respect to the thermal excitation k_BT and the potential shift is constant. In the case of anthracene carboxylic acid, the surface concentration of the molecules is $2 \cdot 10^{14} cm^{-2}$ and the SAM thickness is $6\mathring{A}$. The modulation of the surface potential for a SAM with the same concentration and thickness, but a dipole moment of $+3D$, was calculated by Marie-Noëlle Bussac and plotted in Fig 7.4a (see also in section 7.4.1). The amplitude of the modulation is within 1% of the trapping energy of a single dipole with +3D at the oxide-pentacene interface (160 and $190meV$ for SiO_2 and Al_2O_3, respectively) [14]; this value is much smaller than the thermal energy and, therefore, no trapping occurs. For smaller dipole moments and higher surface concentrations, the amplitudes are even smaller; thus the SAMs used introduce a potential shift.
To complete, the surface potential is calculated for a case when trapping occurs; this monolayer has a thickness of $4\mathring{A}$, a dipole moment of $+3D$ and a surface concentration of $5 \cdot 10^{13} cm^{-2}$ (see Fig. 7.4).

The organic thin-film transistors with a polar SAM were fabricated with an oxide dielectric modified by benzoic acid derivatives (see Fig. 7.1). An Al_2O_3 layer is necessary for the grafting of the monolayer [81]. The channel length is $600\mu m$ and the width $6mm$. The long-channel geometry guaranties that the transistors are not limited by the contacts.
The pentacene film was evaporated at 55 °C and has a thickness of $5 - 10nm$. The films were grown layer by layer; the film morphology was not affected by the change in wettability due to the SAM (see Chapter 4).

The molecules were chosen to form a series of SAMs which differ by the end group

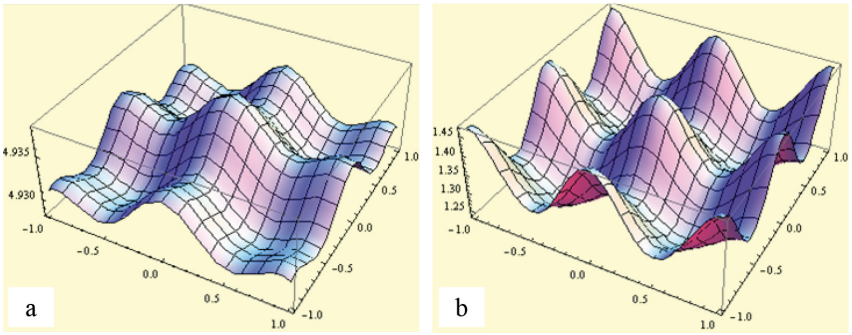

Figure 7.4: *a) Modulation of the surface potential due to a self-assembled monolayer at the oxide-pentacene interface with a dipole moment of $+3D$, a monolayer thickness of $6Å$ and a surface concentration of $2{\cdot}10^{14}cm^{-2}$ (calculated by Marie-Noëlle Bussac). The z-axis is the amplitude of the modulation. In this case, the SAM introduces a potential shift but it does not cause trapping. b) Example for a SAM which causes trapping, with a thickness of $4Å$, a dipole moment of $+3D$ and a surface concentration of $5 \cdot 10^{13}cm^{-2}$. The x-axis and y axis are normalized by the distance between the SAM molecules, the z-axis by the trapping energy of a single dipole moment of $+3D$ at the oxide-pentacene interface.*

on the *para* position. The dipole moments vary between -2.6 to $+3.1D$ (directed from the -*COOH* group to the *para* position). Benzoic acid (BA) is used as neutral SAM ($-1.1D$). Nitrobenzoic acid (NBA) and cyanobenzoic acid (CBA) are the positive SAMs (+3.1 and $+3.0D$, respectively). Anisic acid (AA) and dimethyl-aminobenzoic acid (ABA) have a negative dipole moment (-2.3 and $-2.6D$, respectively). For having a second neutral SAM, anthracene carboxylic acid is used ($-1.1D$). The dipole moments contain the contribution from the grafting group -*COOH* ($-1.1D$) [81].

7.2.1 Transistor performance

The performance of the OTFTs strongly depends on the SAMs, and is reflected in the output and transfer curves (see Fig. 7.5). While the OTFTs modified by a negative SAM (AA and ABA) reach saturation at a drain and gate voltage of $-60V$, the transistors modified by a positive SAM (NBA and CBA) do not reach saturation.

In the transfer curves, the channel conductance is more than 20 times higher after the modification with NBA ($+3.1D$) than with ABA ($-2.6D$). Due to these variations in OTFT performance, the apparent mobility varies from 0.03 to $0.32cm^2/Vs$, the film conductivity from 0.1 to $70 \cdot 10^{-8}S$ □, the residual carrier density from 0.6 to $15 \cdot 10^{12}cm^{-2}$ and the threshold voltage from -16 to $110V$ (details in Table 7.2).

Similar tendencies in threshold voltage were observed by Kobayashi et al., Takeya et al. and Pernstich et al. [64, 71, 72, 74]. It is proposed that the effect of the SAM depends on the dipole moment but no exact correlation is yet found; one reason could be that the SAM molecules used in these works have different length and the transistor performance also depends on the length of the aliphatic chain in the SAM

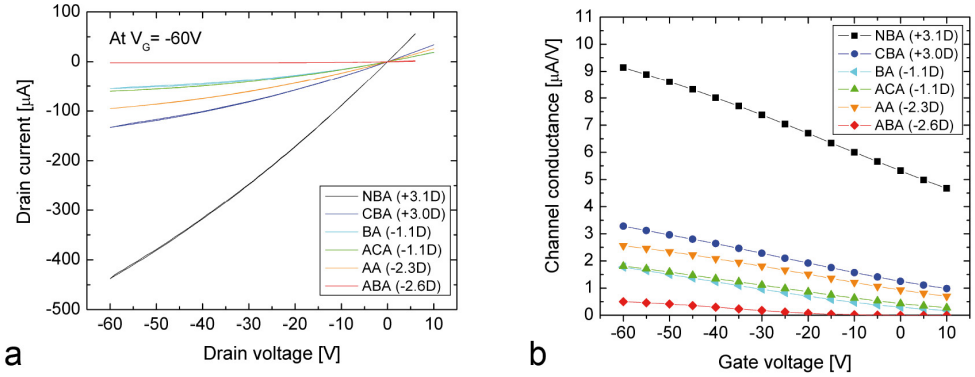

Figure 7.5: *a) Output and b) transfer curves of OTFTs containing a polar SAM.*

	Apparent mobility $[cm^2/Vs]$	Film conductivity $[S\,\square]$	Threshold voltage $[V]$	Residual carriers $[cm^{-2}]$	Contact resistance $[\Omega]$
Positive SAMs					
NBA (+3.1D)	$0.25 - 0.32$	$5.0 - 6.6 \cdot 10^{-7}$	$75 - 110$	$1.2 - 1.5 \cdot 10^{13}$	$2.5 - 5.2 \cdot 10^{4}$
CBA (+3.0D)	$0.12 - 0.16$	$1.0 - 1.5 \cdot 10^{-7}$	$34 - 43$	$5.1 - 5.5 \cdot 10^{12}$	$1.4 - 2.2 \cdot 10^{5}$
Neutral SAMs					
BA (-1.1D)	$0.11 - 0.17$	$2.2 - 4.4 \cdot 10^{-8}$	$2 - 6$	$1.3 - 1.6 \cdot 10^{12}$	$0.5 - 1.0 \cdot 10^{6}$
ACA (-1.1D)	$0.07 - 0.12$	$1.0 - 4.5 \cdot 10^{-8}$	-16–20	$0.6 - 1.3 \cdot 10^{12}$	$0.2 - 3.5 \cdot 10^{6}$
Negative SAMs					
AA (-2.3D)	$0.12 - 0.19$	$3.2 - 3.5 \cdot 10^{-8}$	$-4 - 12$	$1.4 - 7.1 \cdot 10^{12}$	$0.3 - 1.9 \cdot 10^{6}$
ABA (-2.6D)	$0.03 - 0.05$	$1.0 - 1.5 \cdot 10^{-8}$	-12–-8	$1.2 - 2.7 \cdot 10^{12}$	$3.0 - 3.8 \cdot 10^{7}$

Table 7.2: *Characteristic Values of SAM modified OTFTs.*

[68, 69, 70].

For transistors modified with BA and ACA, the values of apparent mobility and threshold voltage are in the same range as the values for other short derivatives of benzene and anthracene [63, 57, 74, 72, 73].

7.2.2 Threshold voltage shift

The dipole moment of the SAM influences the threshold in two ways. On the one hand, it causes a shift in the gate potential in the channel by accumulating or repulsing the charge carriers at dielectric-pentacene interface. This part of the threshold shift is proportional to the dipole moment.
On the other hand, the dipole moment of the SAM influences the charge transport between the dielectric and pentacene; it controls the tunnel probability through the SAM. The charges transferred to pentacene cause a threshold shift to positive values. At high positive threshold voltages, it is proportional to the residual carrier density:

$$V_T = \frac{P_{res} \cdot |e|}{C_{gate}} \tag{7.1}$$

where P_{res} is the residual carrier density, e the electron charge and C_{gate} the capacitance of the dielectric per unit area [50].

When plotted, the threshold values are proportional to the residual carrier density (see Figure 7.6). The slope of the fitted line ($8.41 \cdot 10^{-12} V cm^2$) is close to theoretical value ($8.25 \cdot 10^{-12} V cm^2$), as calculated from equation 7.1 ($C_{gate} = 19.5 nF/cm^2$). Except for very small residual carrier densities, the threshold shift results from the residual carriers. One part of the shift (about $-14V$) is independent of the residual carrier density.

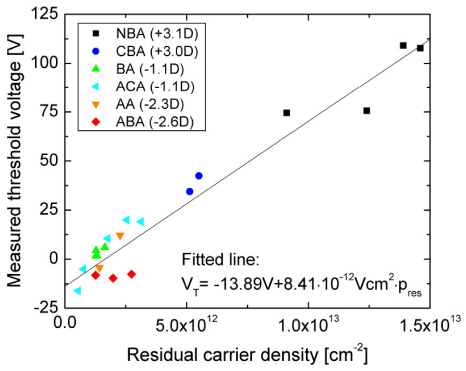

Figure 7.6: *Measured threshold voltage vs. residual carrier density of OTFTs containing a polar SAM.*

In general, the residual carriers can also result from a direct reaction between pentacene and SAM molecules. A direct reaction is not likely, however, because the energy difference between the HOMO level of unpolarized pentacene ($-6.6eV$ [122]) and the LUMO level of the SAM (-1.5 to $-3.3eV$, [127, 128]) is larger than $3.2eV$. The residual carriers, therefore, result from a charge transfer between the defects on the oxide surface and pentacene through the monolayer [56].

The gate potential due to the SAM changes the threshold voltage and is calculated by:

$$\Delta V_{SAM} = \frac{N \cdot D}{\epsilon_0 \cdot \epsilon_{SAM}} \tag{7.2}$$

where N is the surface density, D the dipole moment, ϵ_{SAM} the dielectric constant of the adsorbed molecules and ϵ_0 the vacuum permittivity.

For the used benzoic acids, the surface density N is $4 \cdot 10^{14} cm^{-2}$ and the dielectric constant ϵ_{SAM} is 5.3 (except for ACA where $N = 2 \cdot 10^{14} cm^{-2}$) [81]. A dipole moment of $1D$ causes a potential shift of about $0.28V$. The potential range for the used dipole moments is -0.74 to $+0.88V$ and these values are too small to explain the shift in threshold voltage measured between $-16V$ to more than $+100V$ (see Table 7.2). Consequently, the gate potential shift is not the major effect of the SAM in our transistors.

7.2.3 Residual carriers in the channel

At the untreated oxide-pentacene interface, the charge transfer occurs due to defects on the oxide surface [50]. The charge transfer probability depends on the energy difference between the HOMO level of pentacene and the energy level of the defect on the oxide (see Chapter 6, [56]).

If a SAM is introduced at the interface, the defects and the pentacene molecules are separated, the energy barrier against tunneling becomes larger [66] and the charge transfer probability decreases (see Fig. 7.7). In the case where the SAM molecules carry a dipole moment, the energy level of the defect and the HOMO level of pentacene are shifted relative to one another by the internal field of the SAM (see Fig. 7.8).

The monolayers consist of molecules with similar lengths so the energy barrier was estimated at approximately the same length. The barrier height is determined by the LUMO level of the SAM. Because they are low (between -1.5 and $-3.3eV$, [127, 128]) and the difference to the level of the defect and the HOMO level of pentacene is large, we estimate that all barriers have essentially the same height. The energy barriers, therefore, only vary by the dipole moment of the SAM and the internal field creates a shift in levels causing a change in the energy difference between the pentacene molecule and the defect (see Fig. 7.8). An increase in the charge transfer is observed at the contact-organic semiconductor interface if a SAM with a

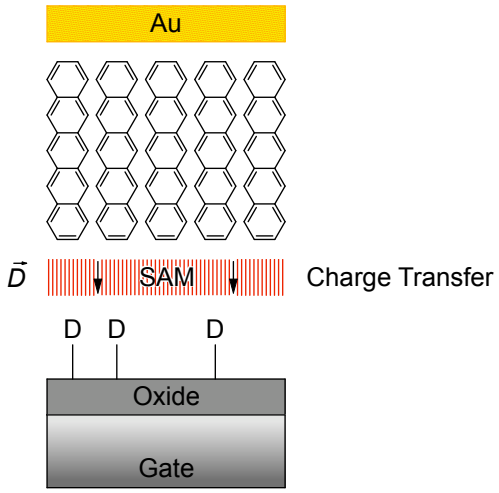

Figure 7.7: *Charge transfer between pentacene and defects at the dielectric-pentacene interface across the SAM that carries a dipole moment.*

nitro group is inserted, compared to a neutral SAM [81, 83].

7.2.4 Charge transfer through the monolayer

The residual carriers are introduced into pentacene by a charge transfer across the SAM. The more probable a charge transfer is, the more residual carriers are introduced. The charge transfer probability P is, therefore, proportional to the concentration of residual carriers:

$$P \propto \frac{P_{res}}{N_{pen}} \tag{7.3}$$

where P_{res} is the residual carrier density and N_{pen} the surface density of pentacene.

It is important to notice that there is no equilibrium of the carrier distribution at the dielectric surface because a back reaction is impossible.
For determining the energy level of the defect responsible for the charge transfer, we use the theory of electronic transfer from R.A. Marcus [129]. According to Marcus, the probability of a charge transfer depends exponentially on the difference of the energy levels between the initial and the final state and the reorganization energy of the system. In this case, the energy levels are the acceptor level of the defect on the dielectric surface and the HOMO level on the unpolarized pentacene molecule. The reorganization energy includes the deformation effects of both pentacene molecule and defect. The charge transfer probability is calculated by:

$$P \propto exp\left(\frac{-\left(\Delta E_{SAM} + \Delta E_0 - \lambda\right)}{4\lambda \cdot k_B T}\right) \tag{7.4}$$

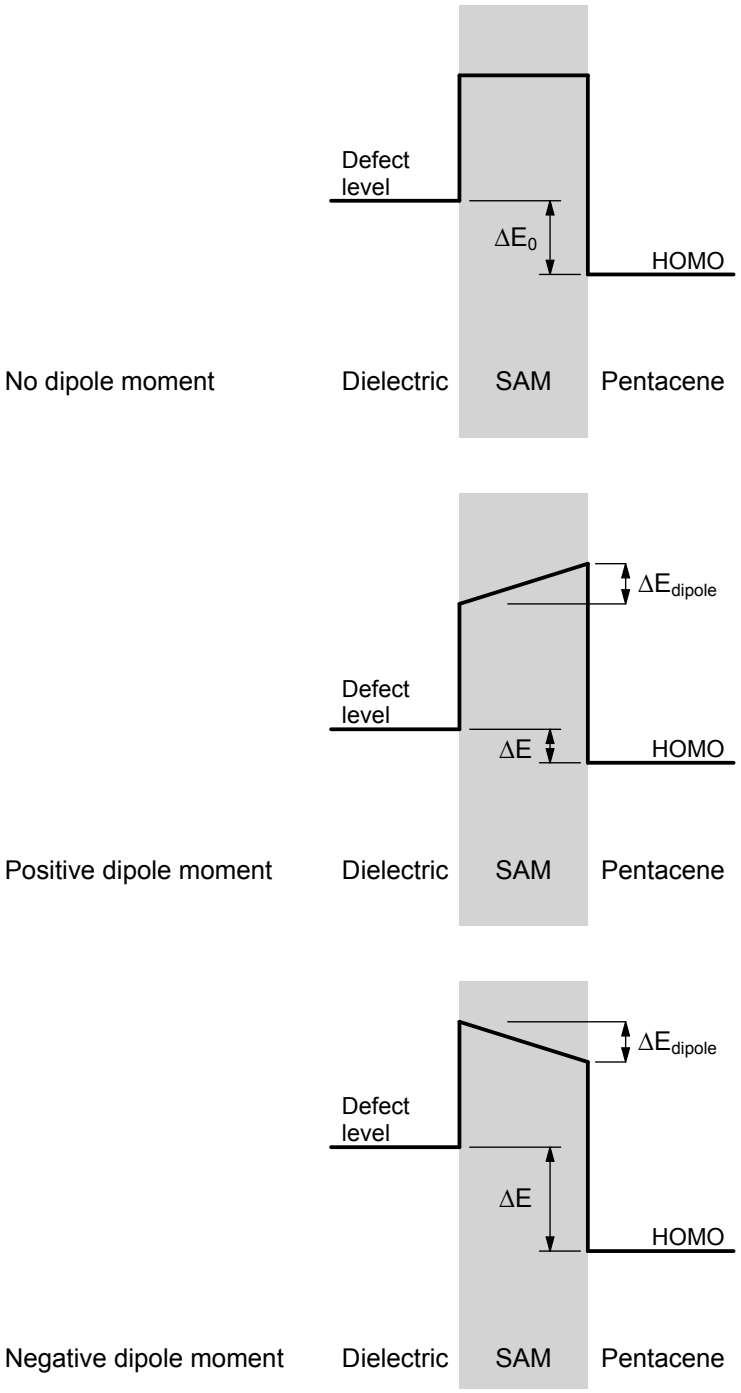

Figure 7.8: *The SAM as energy barrier between pentacene and the defect.*

where ΔE_{SAM} is the energy shift due to the dipole moment in the SAM; ΔE_0 the difference between the energy level of the defect and the HOMO level of pentacene ($E_{defect} - E_{HOMO,pen}$), and λ the reorganization energy, k_B the Boltzmann coefficient and T the absolute temperature [129].

The energy shift depends on the dipole moment and the molecular length:

$$\Delta E_{SAM} = \frac{-2D\beta}{|e|\,L \cdot \sqrt{1 - \left(\frac{-D}{|e|L}\right)^2}} \tag{7.5}$$

where D is the total dipole moment of the SAM molecule, β the transfer integral across the molecule, e the electron charge and L the molecular length (detailed calculation in section 7.4.2).

Based on Marcus, the following values are used to fit the charge transfer probability: transfer integral $\beta = 1eV$ [130] and the molecular length $L = 6\mathring{A}$ [131] for all SAM molecules; the surface density $N_{pen} = 4 \cdot 10^{14} cm^{-2}$ [132] and HOMO level $E_{HOMO} = -6.6eV$ for pentacene [122] and the reorganization energy $\lambda = 0.5eV$ [133]. The surface density of the ACA monolayer is $2 \cdot 10^{14} cm^{-2}$; for the other SAMs $4 \cdot 10^{14} cm^{-2}$.
The measured transfer probability P_{res}/N_{pen} is plotted versus the calculated energy shift ΔE_{SAM} due to the dipole moment (see Fig. 7.9).

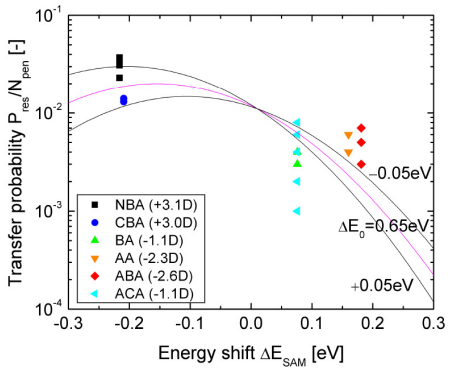

Figure 7.9: *Energy shift due to the dipole moment in the SAM vs. the charge transfer probability.*

By fitting, we deduced an energy level difference ΔE_0 of $0.65eV$ and a defect level ΔE_{defect} of $-5.95eV$. In chapter 6, we found that the O-centered radicals on SiO_2 have energy levels between -5.5 and $-7.1eV$. Suarez et al. showed that the effect of the O_2 plasma is similar on Al_2O_3 and SiO_2 and deduced that the same defects are responsible for the charge transfer [56]. Here we used an O_2 plasma for the SAM grafting, and O-centered radicals are formed on the oxide surface.

7.2.5 Contact resistance and apparent mobility

The contact resistance and the apparent mobility depend on the residual carrier density. Screening effects due to the residual carriers resulted in an increase in the apparent mobility and a decrease in contact resistance (see Fig. 7.10). The transistors are dominated by the presence of residual carriers; exceptions are OTFTs modified by ABA which are limited by the contacts.

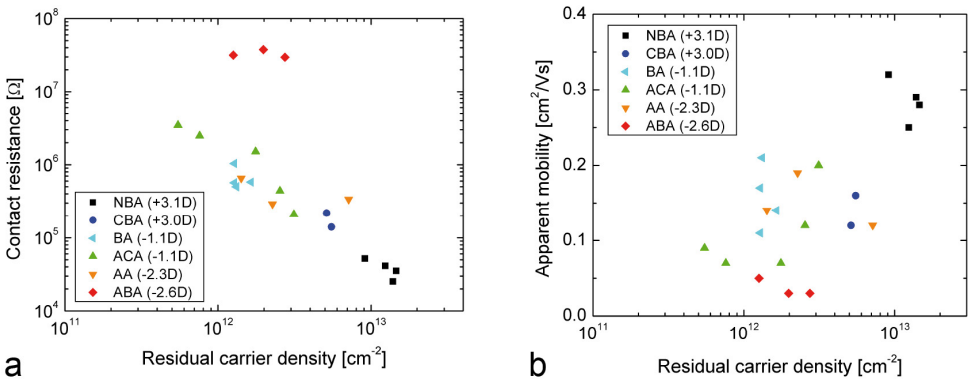

Figure 7.10: *a) Contact resistance and b) apparent mobility vs. residual carrier density of OTFTs modified by polar SAMs.*

In conclusion, the performance of OTFTs modified by polar SAMs is determined by the number of residual carriers. The internal field due to the dipole moment controls the charge transfer through the SAM. The modification with NBA ($+3.1D$) results in the highest values of apparent mobility, threshold voltage, and the lowest values of contact resistance. The modification with ABA ($-2.6D$) has the opposite effect.
The residual carriers could also result from a direct reaction with the end group of the SAM molecule, but such a reaction is not probable because the difference between the HOMO level of pentacene and the LUMO level of the SAM molecules is too large.
The internal field of the SAM also shifts the gate potential. The shifts for the used benzoic acid derivatives are in the range of -1 to $+1V$ which is too small to explain the measured threshold voltages (-16 to $+100V$).

7.3 Conclusion

Organic thin-film transistors (OTFTs) were fabricated with oxide dielectrics modified by self-assembled monolayers (SAMs). The SAM decouples pentacene from the oxide dielectric, covers the defects on the dielectric surface, and acts as an energy barrier against charge transfer through the monolayer. The OTFTs were modified by a neutral SAM (a benzoic acid with a long aliphatic chain) and by a series of polar SAMs (benzoic acid derivatives).
The neutral SAM acts as a spacer between the oxide dielectric and pentacene and dramatically enhances the transistor performance. The apparent mobility is increased while the residual carrier density and the off current are reduced.
The polar SAMs introduce a dipole moment and the internal field due to the dipole moment controls the charge transfer through the SAM. For a positive dipole moment, the charge transfer probability and thus the residual carrier density increase while they are decreased for a negative dipole moment. Consequently, the performance of the OTFTs is dominated by the residual carriers (except the transistors modified by ABA ($-2.6D$) which are contact limited). A potential shift due to the internal field of the SAM and direct reactions of the SAM molecules with pentacene are eliminated as major effect of the monolayers.

7.4 Calculation to the effects of a monolayer

7.4.1 Change in trapping energy

A monolayer at the pentacene-oxide interface separates the charge carrier in pentacene from the traps (defects) on the oxide surface what decreases the trapping energy. If the monolayer consists of dipoles, a potential is added. First the effect of a spacer is calculated, than the potential due to dipoles.

Trapping energy due to a single dipole in a classic model

The charge q in pentacene is trapped by a single dipole p on the oxide surface (a defect). The interaction energy between the dipole and the charge is calculated by:

$$E_{pq} = -\frac{pq}{4\pi\epsilon_0(z \pm b)^2}\frac{1}{\epsilon*} \tag{7.6}$$

where z is the distance between the charge and the interface, b is the distance between the dipole and the interface ($+b$ if the dipole is in the oxide, $-b$ if it is in pentacene).

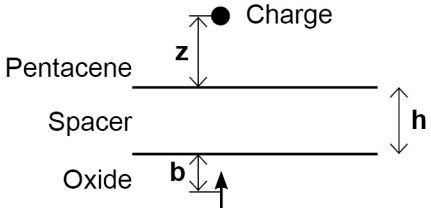

Figure 7.11: *A monolayer as spacer between a dipole in the oxide and a charge in pentacene.*

If the dipole is in the oxide:

$$\frac{1}{\epsilon^*} = \frac{2}{(\epsilon_r + \epsilon_s)} \tag{7.7}$$

where ϵ^* is the relative dielectric constant of pentacene and ϵ_s the static dielectric constant of the oxide.

If the dipole is in pentacene, the field is the sum of the field created by the dipole p situated at $-b$ and the field created in pentacene by a dipole $p' = p(\epsilon_s - \epsilon_r)/(\epsilon_s - \epsilon_r)$ at $+b$.

$$\frac{1}{\epsilon^*} = \frac{2\epsilon_s}{\epsilon_r(\epsilon_r + \epsilon_s)} \tag{7.8}$$

In the limit where $b = 0$, the field is equal to $p + p'$.

The used numeric values are:

Dipole	$p = 0.2082qD$ (in $q\mathring{A}$)
	$D = 3D$
Charge	$q = 1$ for an electron
	$z = 6.6\mathring{A}$
Pentacene	$\epsilon_r = 3.58$
SiO_2	$\epsilon_s = 3.9$, $\epsilon_\infty = 2.1$
Al_2O_3	$\epsilon_s = 9.4$, $\epsilon_\infty = 3$

If the dipole center is in pentacene, the interaction energy E_{pq} is $-60.135meV$ in pentacene/SiO_2 and $-83.524meV$ in pentacene/Al_2O_3. If the dipole center is in the oxide, the interaction energy E_{pq} is $-55.2meV$ in pentacene/SiO_2 and $-31.81meV$ in pentacene/Al_2O_3.
At the interface, it is independent of the oxide ($E_{pq} = -57.67meV$).

The trapping energy E_t as it relates to the difference in polarization energy ΔE_p between the trapped and free states must be defined with careful consideration of the timescales involved. The trapped state of the charge is a long-lived state. Calculation of the polarization energy in this case therefore requires the static dielectric constant ϵ_s. It is also important to make the appropriate corrections to the polarization energy that take into account the lattice relaxation energy E_b. For the short-lived transport or transfer states associated with the free state of the carrier, ϵ_∞ is more appropriate and the lattice relaxation corrections do not apply. The difference between the polarization energy of the charge alone in a short-lived state and the polarization energy of the charge interacting with the dipole trap in a long-lived state is then

$$|E_p(\epsilon_s) - E_p(\epsilon_\infty)| = \frac{q^2}{8\pi\epsilon_0(z+h)} \frac{(\epsilon_s - \epsilon_\infty)}{(\epsilon_r + \epsilon_\infty)(\epsilon_r + \epsilon_s)} \tag{7.9}$$

and the trapping energy E_t calculated with respect to the edge of the band is

$$E_t = |E_p(\epsilon_s) - E_p(\epsilon_\infty)| + |E_{pq}| + E_b - 2J' \tag{7.10}$$

where J' is the transfer integral.

In pentacene/SiO_2:

$$|E_p(\epsilon_s) - E_p(\epsilon_\infty)| = \frac{6.6\mathring{A}}{(z+h)} \cdot 46.21meV \tag{7.11}$$

In pentacene/Al_2O_3:

$$|E_p(\epsilon_s) - E_p(\epsilon_\infty)| = \frac{6.6\mathring{A}}{(z+h)} \cdot 81.73meV \tag{7.12}$$

In pentacene, the intermolecular and intramolecular relaxation energy is $E_b = 180meV$ (absolute value) [134]. The transfer integrals are $J' = 57.205meV$ for pentacene/SiO_2 and $J' = 57.395meV$ for pentacene/Al_2O_3. If the dipole is at the interface, the interaction energy E_{pq} is $-55.67meV$.

In pentacene/SiO_2:

$$E_t = \frac{D}{3}\left(46.21\frac{6.6}{(z+h)} + 57.67\frac{6.6^2}{(z+h)^2} + 65.59\right) meV \tag{7.13}$$

In pentacene/Al_2O_3:

$$E_t = \frac{D}{3}\left(81.73\frac{6.6}{(z+h)} + 57.67\frac{6.6^2}{(z+h)^2} + 65.21\right) meV \tag{7.14}$$

Without a spacer/monolayer ($z = 6.6\mathring{A}$, $h = 0$), we found a trapping energy E_t of $169.46meV$ in pentacene/SiO_2 and $204.61meV$ in pentacene/Al_2O_3. These values are similar to the results of the discret simulation of Konezny et al. ($E_t = 158.7$ and $190.7meV$, respectively) [14].

Trapping effect due to a dipole layer in a classic model

Instead of a single dipole, a dipole layer situated on a square lattice is introduced at the interface. The charge q is situated in pentacene at (x, y, z) (lattice constant d). The dipoles are at a distance h of the oxide-pentacene interface. The coordinates of the dipoles are by the form of (md, kd, h), the integers m and k vary from $-\infty$ to $+\infty$.

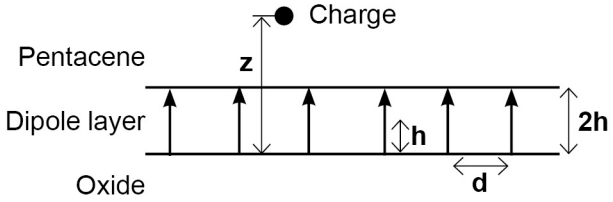

Figure 7.12: *A monolayer consisting of dipoles at the interface between the oxide and pentacene.*

The interaction energy E_{pq} between the dipole layer and the charge is calculated by:

$$E_{pq} = -\sum_{m,k} \frac{pq}{4\pi\epsilon_0}\frac{1}{\epsilon*}\frac{(z-h)}{[(z-h)^2 + (x-md)^2 + (y-kd)^2]^2} \tag{7.15}$$

where z is the distance between the charge and the interface.

The field is the sum of the field created by the dipole p at (md, kd, h) and the field created in pentacene by the dipole $p' = p(\epsilon_s - \epsilon_r)/(\epsilon_s + \epsilon_r)$ at $(md, kd, -h)$.

$$\frac{1}{\epsilon^*} = \frac{2\epsilon_s}{\epsilon_r(\epsilon_r + \epsilon_s)} \tag{7.16}$$

where ϵ_r is the relative dielectric constant in pentacene and ϵ_s the static dielectric constant in the oxide.
In the limit where $h = 0(+)$, the field is created by $p + p'$.

In pentacene/(SiO_2):

$$E_{pq} = -\sum_{m,k} 60.135 \cdot \frac{D}{3} \cdot \frac{6.6^2(z-h)}{[(z-h)^2 + (x-md)^2 + (y-kd)^2]^{3/2}} \tag{7.17}$$

In pentacene/(Al_2O_3):

$$E_{pq} = -\sum_{m,k} 83.524 \cdot \frac{D}{3} \cdot \frac{6.6^2(z-h)}{[(z-h)^2 + (x-md)^2 + (y-kd)^2]^{3/2}} \tag{7.18}$$

The interaction energy can be described by the modulation function g:

$$g(x, y, z-h, d) = \sum_{m,k} \frac{D}{3} \frac{6.6^2(z-h)}{[(z-h)^2 + (x-md)^2 + (y-kd)^2]^{3/2}} \tag{7.19}$$

For one dipole of $D = 3D$ at the interface, g is equal to 1.

Effects of the dipole layer The effect of the dipole layer at the pentacene-oxide interface depends on the distribution of the dipoles. The dipoles are situated in a square lattice (lattice constant d), the charge-dipole distance is $(z - h)$. The geometric effect is included in the modulation function $g(x, y, z - h)$.

1. The dipole layer suppresses trapping by oxide defects because it separates the charge from the interface (for $h > 5\mathring{A}$).

2. If the lattice constant d of the dipole layer is smaller than $(z - h)$, the layer introduces an additional potential $\pm V_{Dipole}$ depending the dipole orientation.

3. If the lattice constant d is larger than $(z - h)$, the dipoles modulate the potential V_{Dipole}, the higher the amplitude the more they depart. The charges in pentacene are trapped in the potential wells. The radius of the potential wells is in the order of $d/2$.

4. Considering the numeric values associated to the pentacene/ SiO_2 and pentacene/ Al_2O_3 interfaces, one can speak of trapping if the modulation $g(x, y)$ exceeds ± 0.4 what results from distances between the dipoles of $d > (z - h)$.

7.4.2 Energy level shift due the dipole moment

A self-assembled monolayer at the pentacene-dielectric interface acts as energy barrier against tunneling. For polar SAMs, the dipole moment introduces an energy level shift which is deduced here.

The dipole moment between two sites 1 and 2 depends on the distance d between the sites and their charges:

$$D(t) = \frac{q_2(t) - q_1(t)}{2} d \tag{7.20}$$

where $q_1(t)$ and $q_2(t)$ are the charges at time t on site 1 and 2, respectively, and d the distance between site 1 and 2.
Therefore, the average dipole moment for an electron switching between site 1 and 2 is:

$$D = \langle D(t) \rangle = e\frac{d}{2}(\mathcal{P}_1 - \mathcal{P}_2) \tag{7.21}$$

where e is the electron charge, $\mathcal{P}_1$ and $\mathcal{P}_2$ the probability that the electron is on site 1 or 2, respectively.

The Hamiltonian $\hat{H}$ for the transfer of an electron from site 1 to site 2 with the energy difference $\Delta E = 2\mathcal{E}$ can be written by:

$$\hat{H} = \begin{pmatrix} \mathcal{E} & \beta \\ \beta & -\mathcal{E} \end{pmatrix} \tag{7.22}$$

where β is the transfer integral between site 1 and 2.

The Eigenvectors are:

$$\begin{cases} |+\rangle = \sqrt{\frac{1}{2} - \frac{\mathcal{E}}{\sqrt{\mathcal{E}^2+\beta^2}}}\,|1\rangle + \sqrt{\frac{1}{2} + \frac{\mathcal{E}}{\sqrt{\mathcal{E}^2+\beta^2}}}\,|2\rangle = a\,|1\rangle + b\,|2\rangle \\ |-\rangle = \sqrt{\frac{1}{2} + \frac{\mathcal{E}}{\sqrt{\mathcal{E}^2+\beta^2}}}\,|1\rangle - \sqrt{\frac{1}{2} - \frac{\mathcal{E}}{\sqrt{\mathcal{E}^2+\beta^2}}}\,|2\rangle = b\,|1\rangle - a\,|2\rangle \end{cases} \tag{7.23}$$

The average dipole moment results from equation 7.21 and 7.23.

$$D = e\frac{d}{2}(\mathcal{P}_1 - \mathcal{P}_2) = e\frac{d}{2}(aa^* - bb^*) = \frac{e\,d\,\mathcal{E}}{\sqrt{\mathcal{E}^2 + \beta^2}} \tag{7.24}$$

where a^* and b^* are the conjugated values of a and b.

For the charge transfer across a SAM molecule at dielectric-pentacene interface, site 1 is the energy level of the defect on the dielectric surface and site 2 the HOMO level of pentacene. As distance between defect and pentacene molecule, the length of the SAM molecule is taken. Then the energy difference ΔE_{SAM} in the SAM molecule due to the dipole moment is calculated by using equation 7.24:

$$\Delta E_{SAM} = 2\mathcal{E} = \frac{-2D\beta}{|e|\, L \cdot \sqrt{1 - \left(\frac{-D}{|e|L}\right)^2}} \tag{7.25}$$

where D is the dipole moment in the SAM molecule, L the length of the SAM molecule and e the electron charge.

Chapter 8

Conclusion

Organic thin-film transistors have given rise to thousands of articles trying to establish correlations between the fabrication parameters and the characteristics of the devices. A research performed on Scifinder, the data base of the American Chemical Society, resulted in more than 7400 articles containing the concept "organic thin-film transistors"[1]. Because this literature is not only confusing but very often contradictory, even the best research groups working in this field in the world cannot claim that they have really understood how an organic thin-film transistor works. One important example is the correlation between the apparent mobility and the microstructure of the organic thin film. Amongst 10 different works on pentacene thin-film transistors, 7 claim that the mobility increases with increasing grain size [62, 96, 135, 136, 137, 138, 139] and 3 claim the contrary [61, 140, 141].
In the present thesis, we have attempted to understand a bit more the transport properties of organic thin-film transistors by trying to separate the relative effects of the contact, of the dielectric interface and of the morphology. Even if the main questions have not yet been solved, this work is a significant contribution to the field.

The transistors which we have dealt with show apparent mobilities between 0.1 and $1cm^2/Vs$. This is a range where trap and release processes at defects in the channel are the main limitation to charge transport [14]. In this respect, it is not surprising that engineering the dielectric interface of the transistors becomes an important issue in device fabrication.
We have done an important effort to identify the main electro active defects on the oxide surface which could act as traps in the channel. A part of the electroactive defects are unstable at the time scale of a few minutes, i.e. the time in which they establish their electroactive character in the channel is short. During this time, it would have been difficult to characterize the defects without changing their character by methods which are normally used for characterizing oxide surfaces (i.e. photoemission). For this reason, we have preferred to take advantage of the perfect description of the defects on the SiO_2 that can be found in the literature and to focus on the changes in the electric properties of the interface. There are even papers giving the electron affinities of these defects [49, 73, 85, 142, 143, 144, 145, 146, 147, 148, 149, 150].

Our work was concentrated on modifying the population of these defects accord-

[1] 7443 articles on 1st November 2010.

ing different treatments and concluding on their role at the dielectric-semiconductor interface. In fact, we were able to identify three groups of defects:

- The deprotonated silanol groups change the wetting properties of the oxide surface and thus the morphology of the thin film. In many cases, they do not change significantly the charge transport properties in the pentacene layers.
- The silicon hydride and silanol groups act as traps.
- The oxygen-centered radicals act as recombination centers, i.e. they are responsible for the transfer of residual carriers into the conducting channel.

The importance of charge transfer reactions at the interface is often underestimated in the literature and we hope to have addressed this subject seriously. In particular, we have shown that at high positive threshold voltages (larger than a few volts), the threshold voltage is proportional to the concentration of residual carriers in the channel while at low positive threshold fields other dipolar contributions may emerge.

The respective roles of the contacts and of the channel were also addressed in the present work by using stencil masks to define short channels down to $2\mu m$ and 4-probe and 2-probe measurements to characterize both the contact and channel resistance. We found that gold contacts made on small-grain pentacene film exhibit lower resistances than on large-grain films what is in contradiction with the conclusions of Sung Hun Jin et al. [118] obtained by the transfer line method. Our results are probably the proof that surface defects are mainly charge transfer centers to the pentacene crystallites: the contact resistance is not perfect-surface limited, but the defects of the surface play a positive role on the transfer across the barrier and in the pentacene film near the contacts.

Self-assembled monolayers (SAMs) have been extensively used to improve the mobility in the channel by modifying the trap distribution in the channel (almost 300 references on Scifinder [2] where the concepts "self-assembled monolayers" and "organic transistor" were closely associated with one another). A large variety of SAM molecules were used, but the reported results are often confusing because the effect of a SAM depends on its length and its chemical nature including the grafting group. Comparative studies were mainly reported concerning the length of the SAM molecules. For aliphatic SAMs, some authors found that the longer the SAM is, the higher the apparent mobility is [72, 151, 152] while others reported a maximum value of the apparent mobility, but the optimal SAMs lengths are not consistent and varies between 8 and 18 carbon atoms (grafting group excluded) [69, 70, 68, 137, 153]. Contradictory results are published for the threshold voltage; it increases [72, 151], it decreases [69, 70] or it remains unchanged [152] with increasing chain length. The fluorination of an aliphatic monolayer results in a threshold shift to positive values; an increase [71, 154] as well as a decrease in apparent mobility [64, 72] is reported.

[2] 286 articles on 1st November 2010.

These examples show that the effect of the self-assembled monolayer is not yet exactly predictable, especially if the SAM carries a non-aliphatic end group.

We focused on molecules which can be grafted from the vapor phase and which carry an electrical dipole moment of a few Debyes. Although an ordered dipolar layer shifts the gate potential by a value of $0.3V$ per Debye, we have shown that this effect is not the most important here. The main role of the self-assembled layer is to passivate the dielectric surface with respect to the charge transfer reactions towards the organic semiconductor. Now the charge transfer depends on the dipole which modulates the possibility of tunneling across the monolayer. It is important to notice that there is no equilibrium of the carrier distribution at the dielectric surface because a back reaction is impossible. Each time a carrier is transferred to the organic semiconductor, it polarizes the lattice by such a large value $(1-2eV)$ [14, 134] that a coming back is impossible and the residual carrier is delocalized in the channel towards the source-drain circuit. In this respect, the resistance to tunneling across the monolayer determines the actual concentration of residual carriers. This is the key concept that we have developed in our tunneling model.

We have also fabricated and measured transistors made on a polyimide dielectric. Due to the smaller capacitance of the polyimide layer (compared to the SiO_2 dielectric), it could be expected that the induced charge densities are smaller at the same gate voltage and thus the apparent mobility values should be smaller. In addition, the grain size of the pentacene film on polyimide is in sub-$100nm$ range while it is 100 times larger on SiO_2 $(2-3\mu m)$. So it is surprising to observe that the channel mobility is on the order of $0.1-0.2cm^2/Vs$, the same values that were obtained on a SiO_2 dielectric. That shows that polymeric dielectrics are not a priori worse, but their interface towards the organic semiconductor strongly affects the electric performance; enhancements result from carefully treating the polymer surface.

At the end of this conclusion, I would like to give a few advices to a PhD student working on the optimization of organic thin-film transistors:

- Significant scientific results can be only obtained in long-channel transistors.
- Do not care too much about the grain size of your organic semiconductor film.
- Do care about the semiconductor-dielectric interface: it is important to avoid defects and dipoles at the interface. For this reason, oxides are not always the best choice.
- A small concentration of residual carriers always increases the mobility and decreases the contact resistance.
- Use at least one parameter, besides the apparent mobility, for characterizing your devices. The residual carrier density can be very helpful.

Chapter 9

Curriculum vitae

12/2010	**Doctoral Degree**, École Polytechnique Fédérale de Lausanne (EPFL), Switzerland
09/2007 - 12/2010	Thesis on organic transistors in the Laboratory of Optoelectronics of Molecular Materials
	Prof. Libero Zuppiroli, EPFL
	Assistant "Introduction to material science" (1st year course)
06/2007	**Masters Degree in Material Science and Engineering**, Eidgenössische Technische Hochschule Zürich (ETHZ), Switzerland
11/2006 - 06/2007	Master thesis on the mechanical behavior of seashells, Prof. Ralph Spolenak, ETHZ
04/2006 - 10/2006	Master studies in Material Science and Engineering at ETHZ
	Master projects on filled polysiloxane films (Dr. Christiane Loewe, Empa Dübendorf) and on vesicles functionalization (Prof. Janos Vörös, ETHZ)
01/2006 - 03/2006	Internship in the R&D laboratory for polymers at Omya, Oftringen, Switzerland
09/2005 - 12/2005	Master exchange semester at Kungliga Tekniska Högskolan Stockholm (KTH), Sweden
06/2005	**Bachelor Degree in Material Science and Engineering**, ETHZ
09/2002 - 07/2005	Bachelor studies in Material Science and Engineering
	Bachelor thesis on polyethylene films (Prof. Paul Smith, ETHZ)
05/2002	**Matura Typus C** (Science and mathematics)
	Kantonsschule Alpenquai Luzern, Switzerland
1997 - 2002	High school with focus on science and mathematics, Kantonsschule Alpenquai Luzern, Switzerland
1996 - 1997	Apprenticeship as electronic technician, Telekom in Kriens, Switzerland
1986 - 1996	Kindergarten, primary and secondary school in Kriens, Switzerland

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