Organic Pentacene Thin Film Transistors on Flexible Substrates Fabricated by Stencil Lithography

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Abstract

This thesis presents the fabrication and characterization of organic thin film transistors (TFTs) on flexible polymer substrates and the development of compliant stencil lithography to significantly improve the patterning resolution on full-wafer scale.

Polymers and organic semiconductors have gained increasing attention during the last years. Today, organic semiconductors are envisioned as a viable alternative to traditional TFTs based on inorganic materials. Organic TFTs can be a solution for device flexibility, cost-efficient fabrication, low-temperature processing and large area patterning. However, up to now they cannot keep up with the performance of TFTs based on single-crystalline inorganic semiconductors because of their low switching speeds. Due to the sensitivity of polymers and organic semiconductors to solvents and high temperatures, stencil lithography is a promising patterning technique for such materials.

Stencil lithography is based on the principle of the shadow mask technique, which is a parallel process with high spatial resolution down to submicrometer scale. It is a solvent-free patterning method without need of elevated temperatures. The stencil is aligned and clamped to the substrate and the required material is deposited through the stencil. Finally the stencil is removed, resulting in a patterned substrate. A typical stencil is made of low-stress silicon nitride (SiN) membranes supported by bulk silicon (Si). The membranes are released by combined dry and wet etching and contain design-specific micro- and nanoapertures.

Stencil lithography was used to pattern titanium-gold (Ti-Au) wires on flexible polymer substrates. The wire resistivity was analyzed by 2-point and 4-point measurements and was found to be comparable with the resistivity of a Ti-Au thin film on a Si wafer.

Stencil lithography was also applied to fabricate organic TFTs on a rigid Si sub-

strate as the back gate contact. Polyimide (PI) or silicon dioxide (SiO_2) was used as the dielectric layer while pentacene was tested as the organic semiconductor. Source-drain (S/D) Au top contacts were patterned by stencil lithography defining transistor channel lengths down to 5 µm. Pentacene TFTs with different film thicknesses were characterized on both dielectrics. The organic TFT fabrication on rigid Si substrates was used to evaluate pentacene films deposited on a PI dielectric. They have shown continuous pentacene films and similar characteristics compared to SiO_2 as the dielectric layer.

In a next step pentacene TFTs on a flexible 12 µm thin PI substrate were fabricated on full-wafer scale using a Si wafer as a rigid support. The gate contacts were patterned locally and PI was used as the dielectric material. Pentacene and S/D Au contacts were patterned by applying aligned full-wafer stencil lithography for channel lengths down to 2.5 µm. The yield of 72 pentacene TFTs was as high as 91.5 % and the average apparent mobility μ was $(5.0 \pm 0.7) \cdot 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$. The pentacene TFTs have been characterized both before and after peeling the flexible PI film off the rigid Si support, showing a to (83 ± 4) % reduced apparent mobility μ.

Pentacene TFTs were also characterized during and after exposing the PI substrate to tensile stress. It was found that uniaxial stretching experiments reduced the apparent mobility μ to (71 ± 3) % when the applied strain ϵ was increased to 2.6 %. After releasing the applied strain ϵ the apparent mobility μ recovered partially to (81 ± 4) % of its initial value. Cycling strain applied to the PI substrate changed the apparent mobility μ distinctively within the first 1000 cycles compared to the reference TFTs. Further stretching cycles decreased the performance of stretched pentacene TFTs similar as the reference TFTs. After 28'000 cycles of 2.7 % applied strain ϵ the apparent mobility μ was reduced to (42 ± 3) %. In parallel to the mentioned experiment, a degradation of the pentacene film over time was monitored. The apparent mobility μ was significantly reduced to (61 ± 2) % of its initial value.

A known drawback in stencil lithography is the so-called blurring, which is the loss of resolution during the pattern transfer. The main cause of the blurring is the gap between the stencil membrane and the substrate surface. The origin of the gap has several reasons such as the non-planarity of the substrate or different curvatures

of stencil and substrate on full-wafer scale. The variation of the wafer curvature due to unsymmetrical patterning of front- and backside of the wafer was monitored during stencil fabrication. One of the major finding is that an increased curvature of the stencil results in an increased gap and therefore reduces the resolution of stencil lithography.

Therefore, a more sophisticated stencil based on compliant membranes is proposed in order to minimize the gap and improve the resolution of pattern transfer on full-wafer scale. Compliant membranes are mechanically decoupled from a rigid Si frame by means of four non-planar cantilevers. Compliant membranes are protruding parts, which adapt to the surface independently in order to reduce the gap between a membrane and its substrate. Finite element method (FEM) simulations have shown that compliant membranes can vertically deflect 40 µm, which is a typical maximal gap that can occur between stencil membrane and substrate. Microapertures were defined using ultraviolet (UV) lithography and nanoapertures, down to 200 nm in diameter, using focused ion beam (FIB). An aluminum (Al) layer was evaporated through compliant and non-compliant membranes on a Si wafer. Subsequent scanning electron microscopy (SEM) characterizations have shown that the use of a compliant stencil improves significantly the resolution on large area. The geometrical blurring was 95 % and the halo more than 75 % smaller compared to standard (i.e. non-compliant) full-wafer stencil lithography.

The results of this thesis demonstrate stencil lithography as a reliable fabrication method for metallic microstructures and organic pentacene TFTs on flexible PI substrates and represent a breakthrough towards improved resolution in full-wafer compliant stencil lithography.

Keywords Stencil lithography, flexible substrate, polyimide (PI), organic thin film transistor (OTFT), organic semiconductor, pentacene, flexible electronics, compliant stencil lithography

Résumé

Ce travail de thèse présente la fabrication et la caractérisation de transistors organiques à couche mince (TFT[1]) sur des substrats polymériques flexibles et le développement de la lithographie par stencil adaptable afin d'améliorer la résolution sur tout un wafer.

Les polymères et les semi-conducteurs organiques ont gagné un intérêt croissant depuis plusieurs années. Aujourd'hui les semi-conducteurs organiques sont considérés comme une alternative prometteuse aux TFTs traditionnels à base inorganique. Les TFTs organiques pourraient être une solution pour des unités flexibles, une fabrication à coûts réduits, des procédés à basse température et la structuration de grandes surfaces. Ils ne peuvent cependant pas rivaliser avec les performances des TFTs à base inorganique à cause de leurs basses vitesses de couplage. En raison de la sensibilité des polymères et des semi-conducteurs organiques aux solvants et aux hautes températures, la lithographie par stencil est une technique prometteuse pour de tels matériaux.

La lithographie par stencil est basée sur le principe de masques durs qui est un procédé parallèle, ayant une résolution au dessous du micromètre. C'est une technique sans solvants et qui ne nécessite pas de températures élevées. Le stencil est aligné et fixé sur le substrat et le matériau nécessaire est déposé à travers. Finalement, le stencil est retiré, laissant le substrat structuré. Un stencil typique se compose de membranes de nitrure de silicium (SiN) à faible stress tenues par un cadre de silicium (Si). Les membranes du stencil, qui contiennent les micro et nano ouvertures, sont ensuite libérées par une combinaison de gravure sèche et humide.

La lithographie par stencil a été utilisée pour structurer des fils de titan-or (Ti-Au) sur des substrats polymériques flexibles. La résistivité des fils a été analysée

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[1] l'acronyme anglais du transistors à couche mince est selon thin film transistor TFT

par des mesures à 2-pointes et à 4-pointes et correlée avec la résistivité d'une couche mince de Ti-Au sur wafer de Si.

La lithographie par stencil a aussi permis la fabrication de TFTs organiques sur substrats rigides de Si servant de grille arrière. Le polyimide (PI) ainsi que l'oxyde de silicium (SiO_2) ont servi de diélectrique pendant que le pentacène a été testé comme semi-conducteur organique. Les contacts de la source et du drain (S/D) on été structurés par lithographie par stencil définissant des longueurs de canaux de transistors descendant jusqu'à 5 µm. Des TFTs avec différentes couches de pentacène ont été caractérisés sur les deux diélectriques. La fabrication des TFTs organiques sur substrat rigide de Si a été utilisée pour l'évaluation des couches de pentacène sur PI. Ses performances électriques ont été comparées avec SiO_2; comme diélectrique.

Par la suite, des TFTs de pentacène sur substrat flexible de PI ont été fabriqués sur un wafer de Si complèt, en l'utilisant comme support rigide. Les contacts de la grille ont été structurés localement et le PI utilisé comme diélectrique. Le pentacène et les contacts S/D ont été structurés sur tout le wafer en utilisant la lithographie par stencil avec alignement pour définir des canaux de transistors descendants jusqu'à 2.5 µm. Le rendement de 72 TFTs de pentacène a atteint les 91.5 % et la mobilité apparente μ moyenne les $(5.0 \pm 0.7) \cdot 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$. Les TFTs de pentacène ont été caractérisés avant et après leur détachement du wafer de Si. La mobilité apparente à été réduite à (83 ± 4) %.

Les TFTs de pentacène ont aussi été caractérisés pendant et après l'application d'une tension mécanique. Une tension uniaxiale de 2.6 % a réduit la mobilité apparente μ à (71 ± 3) % de sa valeur initiale. Revenant en position de repos, la mobilité apparente μ est remontée jusqu'à (81 ± 4) %. La tension appliquée cycliquement a largement diminué la mobilité apparente μ pendent les 1000 premiers cycles. Les cycles suivants ont diminué la performance des TFTs de pentacène de la même manière que les TFTs de référence. Après 28'000 cycles d'une tension de 2.7 %, la mobilité apparente μ a été réduite à (42 ± 3) %. En parallèle des expériences mentionnées, la dégradation d'une couche de pentacène a été analysée. La mobilité apparente μ a été réduite à (61 ± 2) %.

Le désavantage principal de la lithographie par stencil est le blurring; élargissement des structures déposées. La cause principale du blurring est l'espace entre la mem-

brane et le substrat. L'origine de cet espace est la mauvaise planéité du wafer ou des diverses courbures du stencil et du substrat. Les variations de courbure d'un wafer à cause de la structuration asymétrique des faces avant et arrière ont été analysées. Une augmentation de la courbure du substrat induit un espace plus large entre le substrat et le stencil et diminue la résolution de la lithographie.

Un stencil plus sophistiqué, basé sur des membranes adaptables est proposé pour diminuer l'espace et améliorer la résolution sur le wafer complèt. Les membranes adaptables sont découplées du cadre de Si avec quatre leviers hors-plan. Les membranes dépassent le cadre de Si et s'adaptent à la surface du substrat. La méthode des éléments finis (FEM[2]) a montré que les membranes adaptables peuvent se déplacer de 40 µm, ce qui est typiquement l'espace maximum entre la membrane et le substrat. Les ouvertures micrométriques sont structurées par photolithographie et les ouvertures nanométriques, jusqu'à 200 nm, par sonde ionique focalisée (FIB[3]). Une couche d'aluminium (Al) a été évaporée à travers les membranes adaptables et standardes. La microscopie électronique à balayage (SEM[4]) a montré que la résolution est alors nettement améliorée. Le blurring causé par la géométrie est réduit de 95 % et le blurring causé par le halo est diminué d'au moins 75 % par rapport à la lithographie par stencil standard.

Les résultats de cette thèse montrent que la lithographie par stencil est une méthode intéressante pour la structuration des métaux et des TFTs organiques de pentacène sur substrats de PI flexibles. De plus, la lithographie par stencil adaptable apporte une amélioration considérable sur la résolution sur tout le wafer.

Mots-clefs Lithographie par stencil, substrat flexible, polyimide, transistor organique à couche mince (OTFT), semi-conducteur organique, pentacène, électronique flexible, lithographie par stencil adaptable

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[2] l'acronyme anglais de la méthode des éléments finis est selon finite element method FEM

[3] l'acronyme anglais de la sonde ionique focalisée est selon focused ion beam FIB

[4] l'acronyme anglais de la microscopie électronique à balayage est selon scanning electron microscopie SEM

Preface

This thesis is an assignment to obtain the degree of "Docteur ès Sciences" at the Swiss Federal Institute of Technology Lausanne (EPFL). Since May 2006, I am working as a PhD student in the group of Microsystems Laboratory (LMIS1) at EPFL, Switzerland. Many people supported me immensely for the realization of this work.

I would like to thank my thesis supervisor Prof. Dr. Jürgen Brugger for offering me a position in his cheerful group and giving me much freedom to realize my ideas.

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Katrin Sidler
Lausanne, October 8, 2010

Glossary

Symbols

A	Cross section	[m^2]
b_G	Geometrical blurring	[m]
b_H	Blurring due to halo	[m]
c	Capacitance of dielectric layer	[F/m^2]
d	Distance from source to substrate	[m]
d_A	Aperture diameter	[m]
d_C	Diameter of center part	[m]
d_S	Source diameter	[m]
d_T	Total diameter	[m]
E	Young's modulus	[Pa]
g	Gap	[m]
g_D	Channel conductance	[S] or [Ω^{-1}]
g_m	Transconductance	[S] or [Ω^{-1}]
I_D	Drain current	[A]
I_{on}	On current	[A]
I_{off}	Off current	[A]
l	Length	[m]
L	TFT channel length	[m]
r	Bending radius of a wafer	[m]
r_0	Initial wafer bending radius	[m]
R	Electrical resistance	[Ω]
t	Thickness	[m]
V_D	Drain voltage	[V]

V_G	Gate voltage	[V]
V_T	Threshold voltage	[V]
w	Width	[m]
W	TFT channel width	[m]
ϵ	Strain	[-] or [%]
κ	Wafer curvature	[1/m]
κ_0	Initial wafer curvature	[1/m]
μ	Apparent mobility	[m^2/Vs]
μ_0	Initial apparent mobility	[m^2/Vs]
μ_R	Reference apparent mobility	[m^2/Vs]
μ/μ_0	Relative apparent mobility	[-] or [%]
μ_R/μ_{R0}	Reference relative apparent mobility	[-] or [%]
ρ	Electrical resistivity	[Ωm]
σ	Stress	[Pa]
#sq	Number of squares	[-]

Acronyms

AFM	Atomic force microscopy
Al	Aluminum
Ar	Argon
Au	Gold
Cr	Chromium
CH_3COOH	Acetic acid
CMOS	Complementary metal-oxide-semiconductor
CVD	Chemical vapor deposition
D	Drain
DC	Direct current
DIBL	Drain-induced barrier lowering
e-beam	Electron beam
FEM	Finite element method
FET	Field-effect transistor
FIB	Focused ion beam
G	Gate
Ge	Germanium
H_2O	Water
H_3PO_4	Phosphoric acid
HF	Hydrofluoric acid
HNO_3	Nitric acid
I_2	Iodine
KI	Potassium iodide
KOH	Potassium hydroxide
LCD	Liquid crystal display
LPCVD	Low-pressure chemical vapor deposition
LS-SiN	Low-stress silicon nitride
MIM	Metal-insulator-metal
MOSFET	Metal-oxide semiconductor field-effect transistor
N_2	Nitrogen

NMP	N-methyl-2-pyrrolidone
O_2	Oxygen
PDMS	Polydimethylsiloxane
PECVD	Plasma enhanced chemical vapor deposition
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PI	Polyimide
Pt	Platinum
S	Source
S/D	Source-drain
SEM	Scanning electron microscopy
Si	Silicon
SiN	Silicon nitride
SiO_2	Silicon dioxide
SOI	Silicon-on-insulator
Ti	Titanium
TFT	Thin film transistor
UV	Ultraviolet

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1 Introduction

This chapter gives a motivation and an overview on the state of the art of flexible electronics based on organic materials and on stencil lithography as patterning technique. The objectives and the outline of this thesis are separately described.

1.1 Motivation

Flexible electronics based on organic materials are of large interest due to several reasons. Bendable and rollable devices are expected to be attached on any curved surface, which opens new possibilities for implantable or mobile applications. The mechanical flexibility reduces the sensitivity to external shock and small storage space is needed while the device unused. In addition, flexible materials would allow a high-throughput roll-to-roll fabrication, which is envisioned for a cost-efficient production. First applications are already available on the market, such as Readius®, a pocket e-reader with a flexible monochrome 5-inch display [1].

The integration of large flexible electronic circuits is still a challenge as the fabrication of thin film transistors (TFTs) with organic materials is limited among others by two critical issues: *i) The upper working temperature* and *ii) The incompatibility with solvents.* Certain polymers and organic semiconductors do not withstand standard processing steps. Lithography with resist coating and baking at high temperatures degrades the sensitive materials. Therefore, alternative fabrication methods have to be applied. Shadow mask technique also known as stencil lithography is an attractive method for resistless processing without elevated temperatures. However, due to the so-called blurring, it is a resolution-limited patterning technique. Addressing the blurring improves probably the most important drawback in stencil lithography.

Such an achievement increases the reliability and resolution for the patterning of both inorganic and organic materials by stencil lithography. Furthermore, it would open new possibilities for resistless and cost-effective fabrication of nanometer scale structures

1.2 Flexible Electronics

Flexible electronics started by flexible wiring of separated electronic components. Flexible wiring is well established and widely applied in consumer products. Laptops, cameras and some mobile phones often include an adjustable display for improved handling. Such bendable connections are commonly fabricated by screen printed carbon or silver inks. The printed inks are laminated in polymers to maintain the performance.

During the last years flexible electronics received increasing attention since patterning methods for miniaturization improved and polymer materials were applied. Research on flexible electronics often concentrates on the fabrication of TFTs and flexible connections as basic elements for more complex electronics. In particular, polymers and organic semiconductors are of great interest for large arrays of TFTs [2–7]. Polymer materials compared to rigid materials with a much higher Young's modulus enable devices to be flexible and to better withstand stress and strain under mechanical load.

1.2.1 Conducting Wires on Flexible Substrates

Miniaturized electrical connections on flexible substrates are fabricated by buckling a brittle inorganic material. A stretchable configuration with silicon (Si) components on flexible polydimethylsiloxane (PDMS) was obtained by patterning freestanding Si ribbons in the top Si layer of a silicon-on-insulator (SOI) wafer by conventional lithographic processing. Bringing a prestrained layer of PDMS in contact with the ribbons leads to bond the materials. Peeling back the PDMS, with the ribbons bonded on its surface, and then releasing the prestrain, causes the PDMS to relax back to its unstrained state. This relaxation leads to the spontaneous formation of well-controlled, highly periodic, stretchable wavy structures in the ribbons (Figure 1.1) [8]. Kim *et al.* applied a similar fabrication technique for serpentine bridge designs with extreme stretchability on a PDMS substrate [9, 10]. The bridges were used as flexible interconnects between rigid complementary metal-oxide-semiconductor (CMOS) inverters (Figure 1.2). Park *et al.* patterned Si ribbons on plastic substrates and characterized their performance under bending strain [11]. Depending on the Si thickness, three major failures modes were observed at high bending strains: cracking, slipping, and delamination. The mechanical reliability was improved by encapsulating the Si structures at the neutral mechanical plane. Stretchable electrodes with a buckling pattern for flexible interconnection of rigid TFTs have also been realized without prestretching the PDMS substrate [12, 13]. Gold (Au) interconnections were evaporated through a shadow mask onto a PDMS substrate and applied with a stretchable inverter (Figure 1.3) [12].

The reversible stretchability of 200 µm wide Au stripes on PDMS was shown by Lacour *et al.* [14]. Au stripes on PDMS were exposed to cycling strain up to 32 %. Subsequently, a percolation network of microcracks was observed in the Au films. The microcrack pattern allowed a film elongation with small and elastic strain and therefore reproducible electrical conduction. In PDMS embedded Au conductors were obtained by photolithography with a minimum feature size of 10 µm [15]. The Au conductors remained functional after 1D and 2D stretching. Another approach of elastic interconnects was realized on a nanopatterned elastomeric substrate [16]. An array of pyramidal hillocks was patterned on a PDMS film. Au conductors were then defined through a polyimide (PI) shadow mask with different orientations to the array. The change of resistance during stretching was dependent on the orientation of the Au conductor with respect to the array but retained the conduction.

1.2.2 Inorganic and Organic TFTs on Flexible Substrates

Beside electrical interconnections, TFTs are the basic element for electronic circuits. TFTs on flexible substrates are commonly realized with non-crystalline Si or

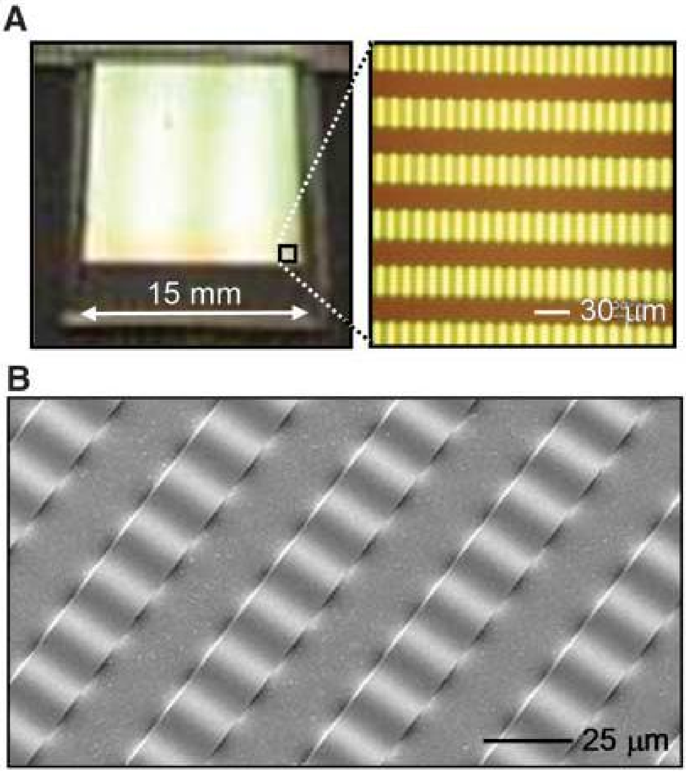


Figure 1.1: A) Optical illustrations of a large-scale aligned array of wavy, single-crystal silicon (Si) ribbons on polydimethylsiloxane (PDMS). B) Scanning electron microscopy (SEM) illustration of wavy Si ribbons. The wavelengths and amplitudes of the wave structures are highly uniform across the array. Images reproduced from [8].

organic semiconductors. Lee *et al.* laminated a PI film on a rigid glass substrate and deposited amorphous Si by plasma enhanced chemical vapor deposition (PECVD) [17]. The deposition was carried out below 200°C in order to prevent damage to the PI substrate. The amorphous Si is used as an inorganic semiconductor for TFTs in flexible displays applications. Amorphous Si was also applied on flexible polyethylene naphthalate (PEN) substrates [18]. TFTs and photodiodes were fabricated on a flat surface. A dedicated pixel design allowed a wide range of curved shapes by combination of cutting, bending and stretching the device after fabrication. For high performance Kim *et al.* included single-crystalline Si in flexible CMOS devices

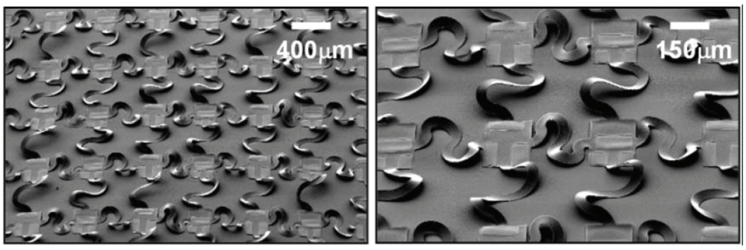


Figure 1.2: Stretchable serpentine shaped bridges between complementary metal-oxide-semiconductor (CMOS) inverters on a PDMS substrate. Images reproduced from [9].

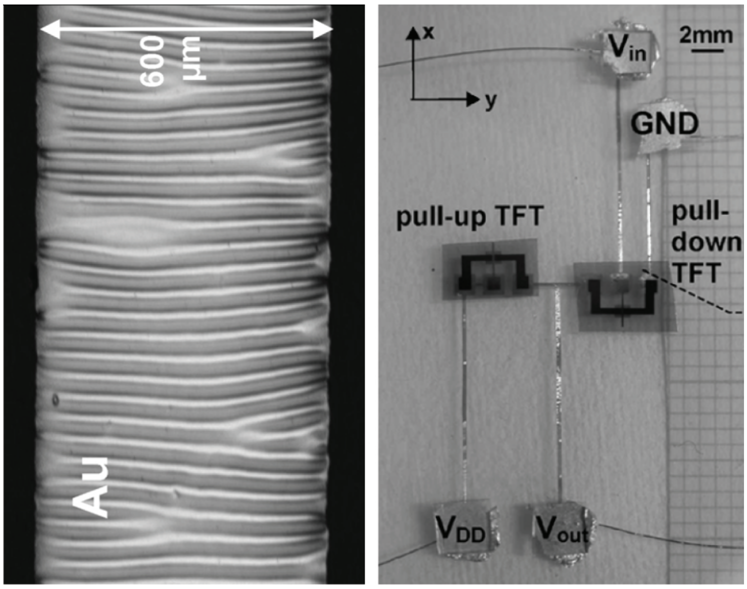


Figure 1.3: Left: Wavy metal electrode directly patterned on a PDMS film. Right: Inverter composed of stretchable interconnections and rigid thin film transistors (TFTs). Images reproduced from [12].

[19]. Therefore n- and p-doped Si ribbons with integrated contacts are printed on a PI layer. The multilayer designs combine layouts at the neutral strain position with wavy structural configurations.

Inorganic TFTs generally have good time stability but high process temperatures of amorphous Si (ca. 360°C) are often incompatible with flexible polymer substrates. Organic semiconductors can be processed close to room temperature and their electrical performance is comparable with amorphous Si [20]. Additionally, organic semiconductors are expected to be low-cost in fabrication. Gowrisanker *et al.* developed a low-temperature process flow and combined pentacene as organic and amorphous Si as inorganic semiconductor on a PEN substrate [21]. P- and n-channel devices were fabricated for logic operations at a temperature below 120°C and 180°C, respectively. Sekitani *et al.* embedded organic TFTs at the neutral strain position between two flexible polymer films [22, 23]. Pentacene TFTs were fabricated on a PI substrate and encapsulated with parylene. This setup can largely suppress strain-induced changes in the TFTs characteristics.

1.2.3 Applications of Flexible Electronics

In 2002, Toshiba has developed a flexible low-temperature polysilicon TFT liquid crystal display (LCD) [24]. The 8.4-inch full-color display is made of thin glass layers attached to a flexible film. The flexible display can be bent down to a radius of 20 cm.

Bendable and rollable electronics are often distinguished from stretchable electronics. Stretchable electronics can additionally endure large elastic deformations with no or little decrease of its performance. One of the most interesting applications of stretchable electronics is the so-called artificial skin devices. Capacitive sensors embedded in silicone rubber act as pressure sensor and are aimed to be integrated in stretchable electronic skin [25]. The integration of piezoelectric and pyroelectric elements on a polymer film and in combination with transistors leads to a pressure and temperature sensing skin [26]. Ko *et al.* have presented photodetectors with stretchable interconnects, which were mounted on a PDMS film and placed on a hemispherical glass lens [27]. The device was used as a electronic eye camera for high resolution imaging. This method was also used for curvilinear electronic test structures [28]. The test structures were conformably wrapped around a finger tip model (Figure 1.4).

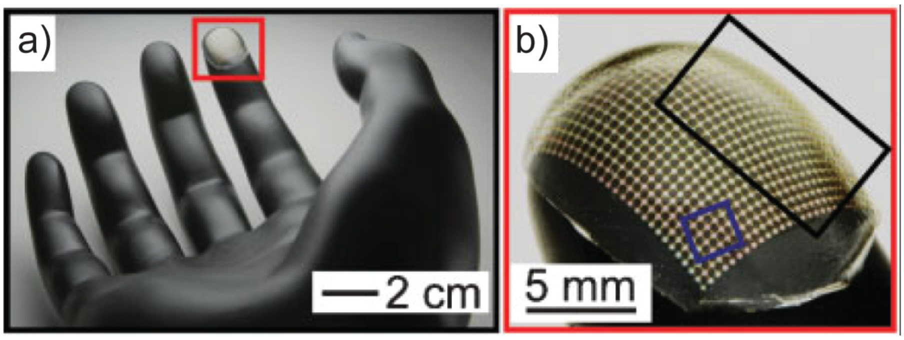


Figure 1.4: a) Mesh circuit on a plastic substrate mounted onto the tip of a human finger model. b) Zoom of a). Images reproduced from [28].

Research on flexible electronics is ongoing and studies for future concepts are already done. The Nokia Research Center and the Cambridge Nanoscience Centre have developed the Morph Concept [29]. The Morph Concept technology focuses on mobile applications and aims to integrate components such as flexible materials, self-cleaning surfaces, transparent electronics or solar absorption. Overall, reduced costs and more functionality on smaller space are envisioned.

1.3 Organic Electronics

Electronics based on organic materials is a promising thin film technology for a variety of applications [30]. Today, organic semiconductors are envisioned as a viable alternative to traditional TFTs based on inorganic materials. Organic TFT can be a solution for large area patterning, device flexibility, low-temperature processing and also cost-efficient fabrication [31]. Apparent mobilities of TFTs with a variety of organic semiconductors are close to amorphous Si [20]. But due to this relatively low mobility, organic TFT cannot keep up with the performance of TFTs based on single-crystalline inorganic semiconductors, such as Si and germanium (Ge). Therefore, organic TFTs are not suitable for applications involving high switching speeds.

1.3.1 Organic TFT Design

An organic TFT is made of three electrodes, an insulating film and an organic semiconducting film. Source (S) and drain (D) electrodes are in direct contact with the semiconducting film. The insulating film separates the source-drain (S/D) electrodes and the semiconductor from the gate (G) contact. The architecture of an organic TFT is often given by the fabrication process, i.e. assembling all components in a working device. The two architectures of bottom and top S/D electrodes are widely established. In both cases the gate contact is coated with the insulating film. If the insulating material (e.g. silicon dioxide (SiO_2)) withstands micro- and nanopatterning methods, S/D contacts can be directly patterned on the film. In that case the organic semiconductor is deposited at the end. This approach leads to a bottom contact configuration, which has a high resolution in the channel definition (Figure 1.5 a). Some organic insulating materials (e.g. polymers) do not withstand all processing methods including solvents or high temperatures. Therefore, the organic semiconducting material is deposited directly on the insulating film and S/D contacts are defined by stencil lithography or shadow mask technique [32]. This architecture is the so-called top contact configuration (Figure 1.5 b). It has been reported that the top contact configuration has generally a lower contact resistance compared to the bottom contact configuration [33–35]. This is likely because of a higher crystallinity of the organic semiconductor deposited on a planar surface.

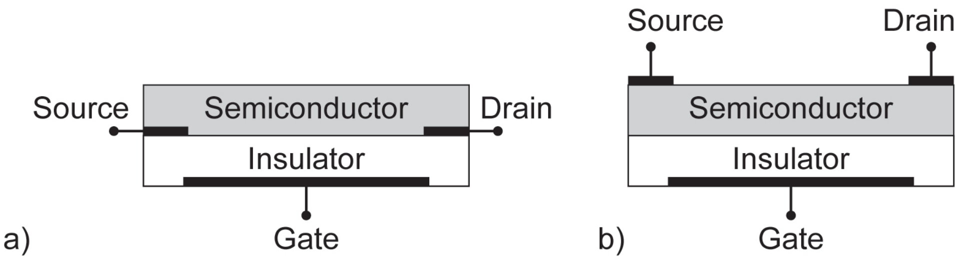


Figure 1.5: a) Bottom contact and b) top contact configuration of an organic TFT.

1.3.2 Acenes-Based Organic Semiconductors

The characteristics of organic semiconductors strongly depend on their physical properties. Usually, organic semiconductors are formed by conjugated molecules. Conjugated molecules contain alternating single and double bonds of carbon atoms. The atomic orbital in carbon are hybridized in sp^2. This hybridization results in three in plane degenerated orbital and a remaining unhybridized p_z orbital. The sp^2 bond is known as a sigma (σ) bond, which gives the stability of the molecule. The p_z bond is perpendicular to the sp^2 plane and known as a pi (π) bond (Figure 1.6) [36]. The overlapping of p_z orbital gives an additional bond between neighboring molecules. This π bond induces a delocalization of the π electrons along the molecule. Under an externally applied electronic field, the π electrons move and an electronic dipole is created. This allows the molecules to interact among each other and form a more or less regular molecular solid.

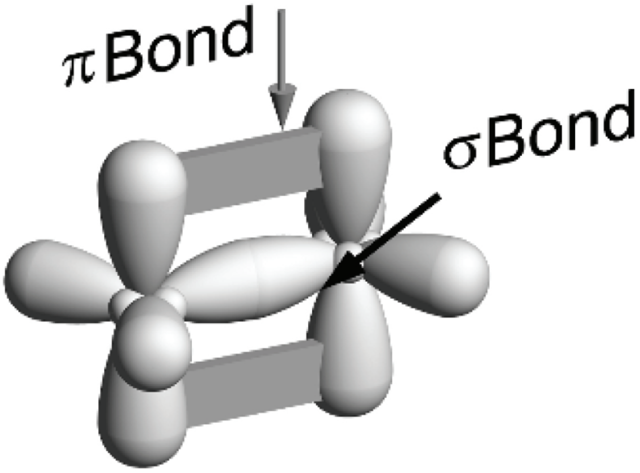


Figure 1.6: Schematic orbital illustration of a double carbon bond. This hybridization results in σ and π bonds. Image reproduced from [36].

Several research laboratories concentrate on acenes based organic semiconductors. The acenes are assemblies of fused benzene rings. Some of the acenes assemblies form planar, rigid molecules with relatively fixed arrangements of atoms (Figure 1.7). Several semiconducting acenes form polycrystalline films when deposited on a surface. Organic films with a high polycrystallinity result in a better overall performance of the organic TFT as π bonds of single molecules overlap [36]. Among the acenes pentacene is commonly used as organic semiconductor. It is commercially available as a purple-blue powder with different purification grades. Five linear connected benzene rings form a pentacene molecule (Figure 1.8). Pentacene can be either used as a single crystal [37] or, more commonly; it is thermally evaporated to define a thin film. Thin films of pentacene assemble as crystalline grains on smooth surfaces (Figure 1.9) [38–43]. Pentacene thin films are widely used for organic TFT applications [2, 5, 7, 44–47]. The electrical performance of organic pentacene TFTs strongly depends on the fabrication process and the design. Maximal mobilities of pentacene based TFTs have reached 5 to 5.5 cm^2/Vs [48, 49], which is still several magnitudes lower than mobilities of Si or Ge based TFTs.

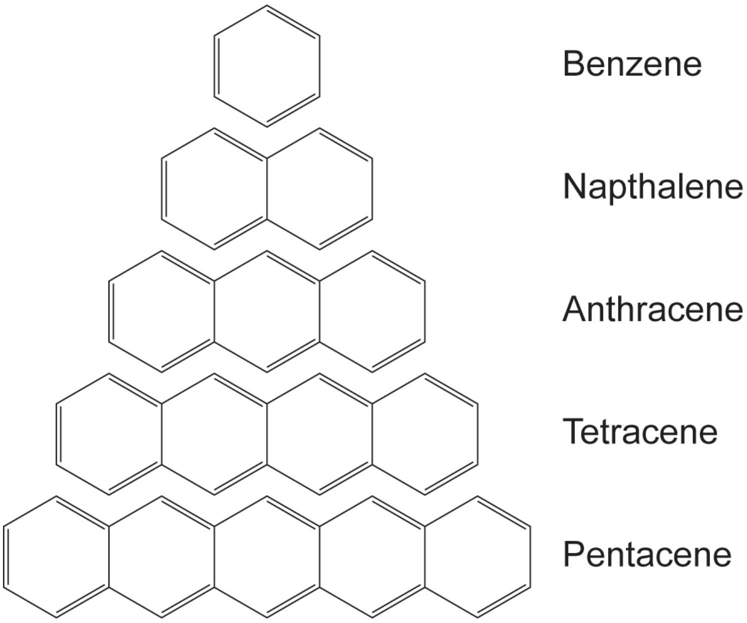


Figure 1.7: Schematic illustration of acenes. Acenes contain fused benzene rings and can assemble in planar and rigid molecules.

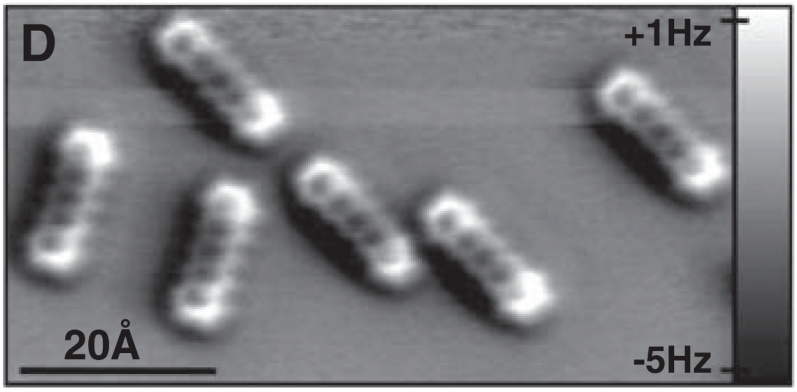


Figure 1.8: Pentacene molecules imaged by atomic force microscopy (AFM) in constant height mode. Image reproduced from [50].

1.3.3 TFT Applications with Organic Semiconductors

Organic semiconductors were included in electronics before research was focusing on flexible devices. The first organic field-effect transistor (FET) was achieved in 1986 [51]. Tsumura *et al.* realized an organic FET with Si as a back gate, SiO_2 as the dielectric layer, the polymer polythiophene as the semiconducting material and Au for S/D contacts. The device performance was optimized by controlling the doping levels of the polymer. Shortly after, the interest in organic semiconductors increased as an organic solar cell [52] and a organic light emitting diode [53] were realized. The development of organic ring oscillators [54] and code generators [55] followed a few years later. First rigid displays with organic semiconductors were fabricated by Philips Research [56]. Afterwards, Huitema *et al.* have fabricated an organic display with different grey levels for monochrome images on a rigid glass substrate (Figure 1.10) [57].

An advantage of organic semiconductors is the low process temperature, which is favorable for a large range of polymers [58]. Additionally, the mechanical properties of organic semiconductors are compatible with rollable electronics [59]. Organic semiconductors on plastic substrates for flexible display applications followed rapidly after the first achievements on rigid substrates [60–62]. Recently, Sekitani

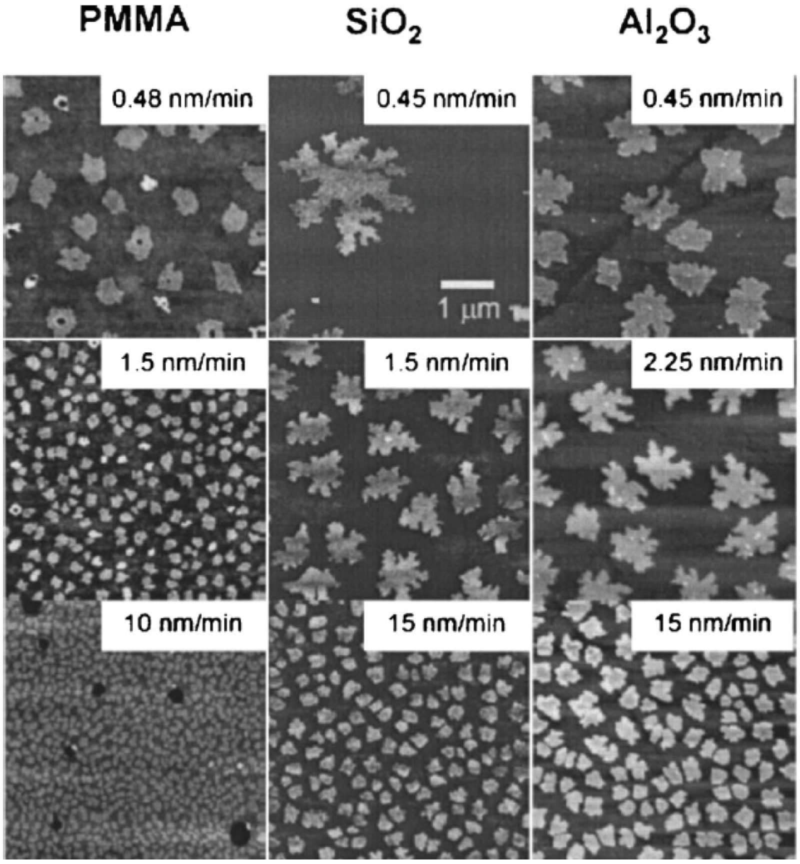


Figure 1.9: Crystalline pentacene grains deposited on polymeric and inorganic substrates imaged by AFM. Different deposition rates have an impact on the pentacene morphology. Image reproduced from [42].

et al. achieved stretchable organic light emitting diodes using printable elastic conductors [46]. Carbon nanotubes were used as dopant of the ink to print flexible interconnects on a PDMS film. The organic transistors had a channel length of 20 µm (Figure 1.11). Someya *et al.* applied organic semiconductors on large-area networks [63, 64]. A conformal network with integrated pressure and temperature sensors can be wrapped around a curved surface and used for artificial skin applications of future robots (Figure 1.12). The sensors are built of pentacene transistors and have channel lengths down to 50 µm. Kato *et al.* realized a large-area flexible

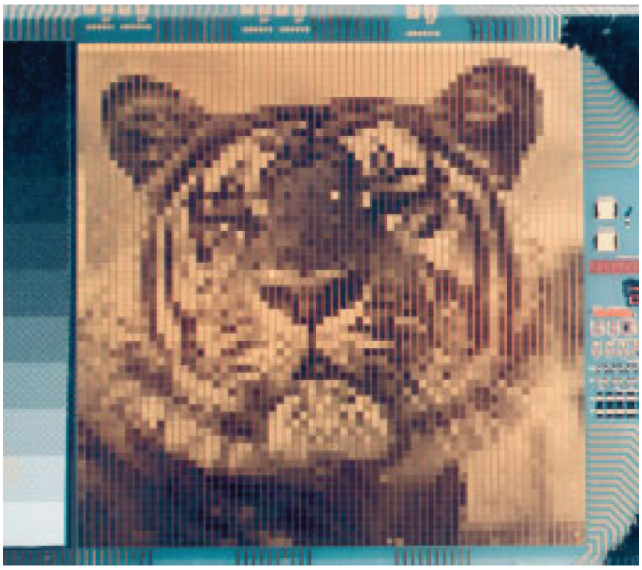


Figure 1.10: Organic display for monochrome imaging on a rigid glass substrate. Image reproduced from [57].

ultrasonic imaging system using organic transistors [65]. An array of sensing cells comprising ultrasonic transducers and organic transistors allows a 3D imaging.

Due to the incompatibility with solvents and high temperature processes, metal contacts on poly-crystalline pentacene films are usually patterned by shadow mask technique or stencil lithography. The following Section 1.4 summarizes advantages and challenges in stencil lithography.

1.4 Stencil Lithography

Stencil lithography is a shadow mask technique [66] that offers an alternative way of patterning in submicrometer resolution [67–71]. Deshmukh *et al.* have etched nanometric holes and lines in a silicon nitride (SiN) membrane and transferred the pattern onto a substrate (Figure 1.13). Brugger *et al.* fabricated in a SiN membrane a nanosieve and applied it for the patterning of chromium-gold (Cr-Au) dots (Figure 1.14). The main advantages of stencil lithography are solvent-free process-

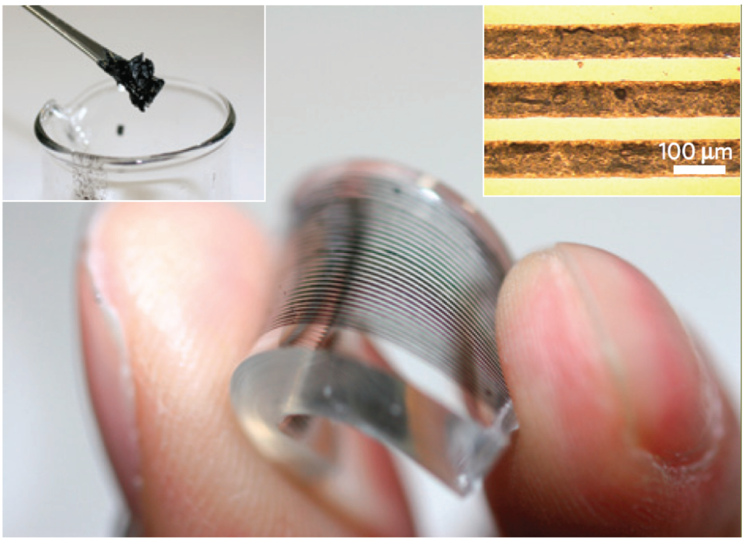


Figure 1.11: Printed elastic conductors on a PDMS sheet. The insets show carbon nanotubes used as the ink dopant dispersed in paste and printed elastic conductors without applied stress. Images reproduced from [46].

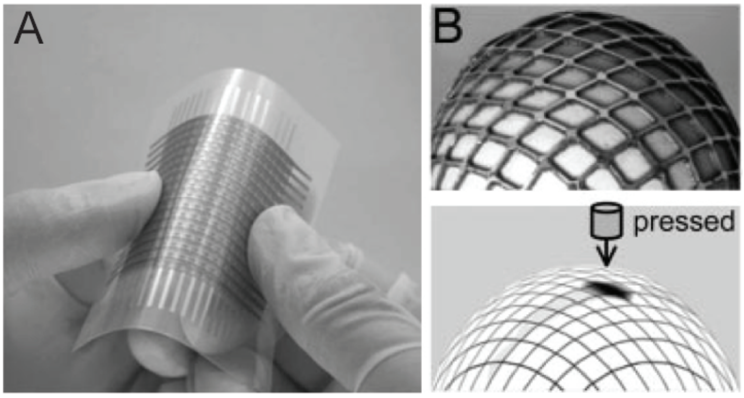


Figure 1.12: A) Organic transistors are used to realize an array of pressure sensors for artificial skin applications. Image reproduced from [63]. B) Top: A pressure sensor matrix put on an egg. Each node of the matrix contains a pressure sensor. Bottom: Spatial distribution of pressure. Images reproduced from [64].

ing, no need for elevated temperatures or energy radiations and the reproducibility of nanopatterning. Therefore, stencil lithography broadens processing methods on uneven, thermally sensitive or chemically fragile surfaces. Stencil lithography based fabrication of patterning nanodots and nanowires and of metallic structures on polymer substrates has been previously demonstrated [72–77]. Vazquez Mena *et al.* have fabricated aluminum (Al) and Au nanowires using full-wafer stencil lithography (Figure 1.15). In addition, it is possible to align stencils to an already structured substrate, which has been used as a CMOS post process to fabricate mass sensors [78]. Stencil lithography has mainly been used for thin film deposition, but it has also been applied for plasma etching [79, 80] and ion implantation [81]. Villanueva *et al.* have applied stencil lithography for etching 200 nm wide cantilevers made of 100 nm thick low-stress SiN (Figure 1.16).

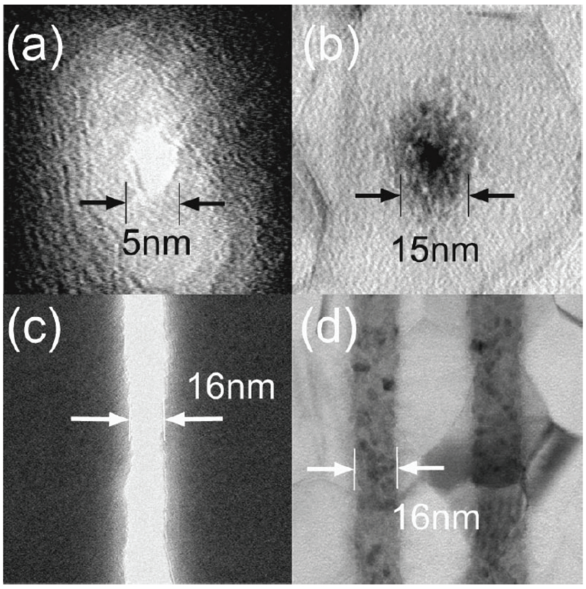


Figure 1.13: a) A 5 nm hole in a silicon nitride (SiN) membrane. b) A 10 nm thick erbium dot deposited through the hole shown in a). c) 16 nm wide slit in a SiN membrane. d) A 10 nm thick 16 nm wide and erbium line deposited through the slit shown in c). Images reproduced from [69].

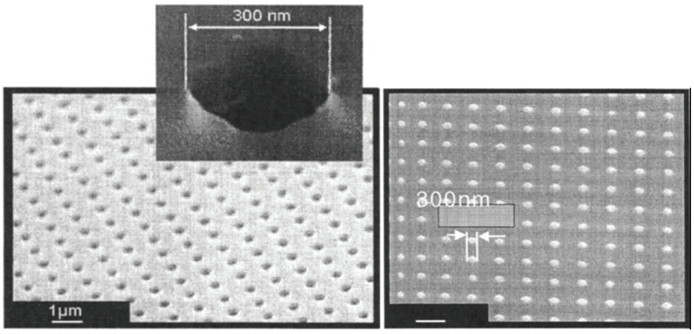


Figure 1.14: Left: SiN nanosieve with 300 nm periodic apertures. The inset shows a single aperture in a SiN membrane. Right: Corresponding periodic array of 300 nm chromium-gold (Cr-Au) dots, 30 nm thick. Images reproduced from [70].

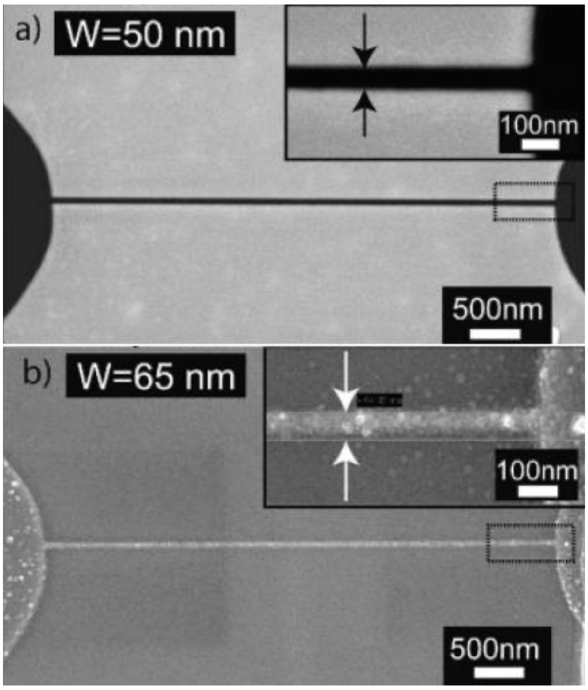


Figure 1.15: a) Stencil aperture 50 nm wide and b) corresponding aluminum (Al) nanowire 65 nm wide. Image reproduced from [75].

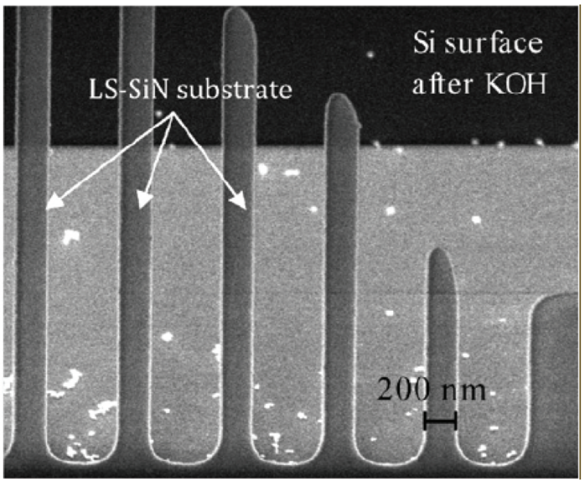


Figure 1.16: Stencil lithography applied for etching thin films. 200 nm wide cantilevers made of 100 nm thick low-stress SiN. Image reproduced from [80].

Due to the straight forward application of stencil lithography and the demonstration that it is a reliable patterning technique, research heads to overcome its limiting challenges. Current limitations in stencil lithography are related to the resolution and the reproducibility of the pattern transfer [82]. The three most important limitations are the clogging, the membrane stability and the blurring. A typical stencil is made of thin low-stress SiN membranes, which are supported by bulk Si. The membranes are patterned with design specific micro- and nanoapertures and released by successive dry and wet etching processes [82]. During evaporation, the material is also accumulated on the walls of the apertures reducing their size and eventually clogging them. Although this might affect the transfer of thick layers, it does not affect the reusability of the membranes. The initial membrane aperture dimensions can be recovered using wet chemical etching solutions [74, 83]. The material that is deposited on the membrane material induces some mechanical stress. This stress can cause deformations that are maximized depending on the shape of the apertures and on the size of the membranes. In order to reduce pattern transfer deformation, mechanical stabilization of delicate membrane designs can be used [84]. Finally, blurring is the loss of dimensions caused by dispersion of the deposited material.

The blurring was recognized since the first depositions through shadow masks [66]. The main cause of blurring is the existing gap between the stencil membrane and the substrate [83]. Such a gap is always present and might have different origins, such as different curvatures of stencil and substrate, stress-deformed membranes or a potential non-planarity of the substrate surface prevent the stencil from a close contact with the substrate. Such a gap is in the range of several micrometers up to tens of micrometers and causes a loss of resolution. Compared to the membrane aperture d_A, the deposited structure is enlarged in two manners. First, the gap g causes a geometrical blurring b_G (Figure 1.17) [85]. Second, the blurring is enhanced by surface diffusion causing a thin halo b_H around a center structure (Figure 1.17) [85, 86].

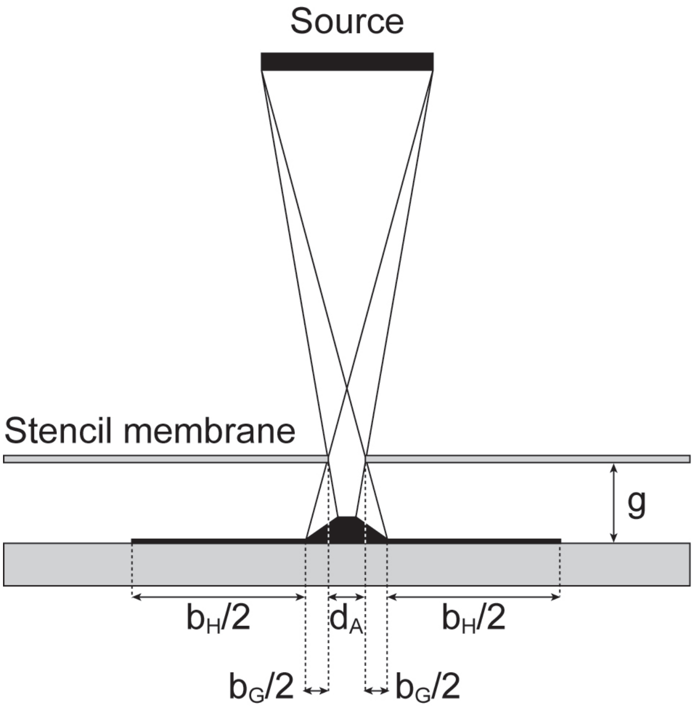


Figure 1.17: Structures deposited by stencil lithography are, compared to the membrane aperture diameter d_A, enlarged due to a geometrical blurring b_G and a blurring due to a halo b_H. The origin of the blurring is the gap g between the stencil membrane and the substrate surface.

1.5 Objectives

Within this thesis two main objectives are aimed.

The first objective is the fabrication and characterization of pentacene based TFTs on flexible polymer substrates. It is aimed to develop a reliable full-wafer fabrication process to handle flexible substrates and deal with the constraints of organic materials. In parallel, a focus is put on the miniaturization of the TFT channel dimensions. It is further envisioned to study the aging behavior of pentacene TFTs after the device fabrication is completed. In addition, the electrical performance needs to be tested under mechanically applied load in order to characterize the fabricated pentacene TFTs as a basic element for flexible electronics.

The second objective is the development of a compliant stencil in order to improve the resolution of the pattern transfer on full-wafer scale. A novel stencil geometry including a rigid frame and decoupled membranes is envisioned. The decoupled membranes adapt to the substrate surface and minimize the gap and blurring on full-wafer scale. A simulation by finite element method (FEM) predicts the mechanical behavior of the compliant stencil. Standard micro- and nanomachining processes are applied and optimized to obtain the envisioned improvement in resolution of submicrometer scale in stencil lithography.

1.6 Thesis Outline

This thesis is organized in five chapters.

After this introduction in Chapter 1, Chapter 2 gives an overview on the stencil fabrication. Different methods for the membrane release are explained. In addition, the change of the wafer curvature during the stencil fabrication is analyzed due to its effect on the gap between membrane and substrate.

Chapter 3 concentrates on the patterning of metal wires on polymer substrates. Wire test structures for 2-point and 4-point measurements were patterned on different polymer substrates. The resistivity of the test structures as well as of a thin film is measured and compared.

Chapter 4 is divided in four sections. Section 4.1 points out the method how TFT specific parameters were extracted. Section 4.2 presents the fabrication and electrical characterization of rigid pentacene TFT with PI and SiO_2 as a dielectric layer. Section 4.3 concentrates on the fabrication of pentacene TFTs on a flexible PI substrate applying aligned full-wafer stencil lithography. The pentacene TFTs were electrically characterized after peeling the PI substrate off the rigid support. Finally, Section 4.4 shows the change of the apparent mobility over time, by peeling the TFT off the rigid support and under mechanical load.

Chapter 5 introduces to the compliant stencil lithography. The challenges in a high resolution pattern transfer are explained. The fabrication process of a compliant stencil is shown and statistics on the pattern transfer are taken.

Finally, Chapter 6 summarizes the obtained results, an overall conclusion is taken and an outlook for future objectives is given.

2 Stencil Design and Fabrication

This chapter presents different approaches of a stencil fabrication process and the change of the wafer curvature during processing. The choice of a specific stencil fabrication process depends on its application. The characterization of the wafer curvature can be used to reduce the gap between a stencil membrane and a substrate. The gap has a main influence on the resolution of the pattern transfer in stencil lithography.

2.1 Stencil Fabrication Methods

The fabrication of freestanding membranes supported by bulk material can be realized in different manners and with several materials. Due to the geometrical stability and the simplicity of the fabrication methods, micro- and nanostencils are often made of low-stress SiN membranes supported by bulk Si. Membrane apertures in micrometer and nanometer scale are commonly defined using ultraviolet (UV) lithography and electron beam (e-beam) lithography, respectively. Full-wafer stencils can be cut into chips after fabrication, if needed. Designed breaking points in the supporting Si provide the stencil to be cleaved at the aimed position by applying pressure with a diamond pen.

Stencils used within this thesis were fabricated following two typical process flows. Both process flows contain low-stress SiN as membrane material and bulk Si as a rigid support. The stencil fabrication process consists of an aperture patterning and a membrane release step. Details of the aperture patterning as well as two types of membrane release processes are described in the following subsections.

2.1.1 Aperture Patterning

The stencil fabrication starts with a 100 mm Si wafer (Figure 2.1 a). If needed, membrane stabilization is defined by etching grooves on the frontside into the Si (Figure 2.1 b). The approximately 2 µm deep and wide grooves are patterned by dry etching. The prestructured Si wafer is coated with low-stress SiN by low-pressure chemical vapor deposition (LPCVD) (Figure 2.1 c). The deposition of the low-stress SiN defines the membrane thickness. The optimal thickness depends on the size of each freestanding membrane as well as on the aperture design. The membrane thickness is usually between 100 nm and 1 µm. On the frontside, membrane apertures are defined in the low-stress SiN layer by lithography and dry etching (Figure 2.1 d). The backside patterning depends on the method for the final membrane release. The membrane release is either done by wet etching or with a combination of wet and dry etching processes.

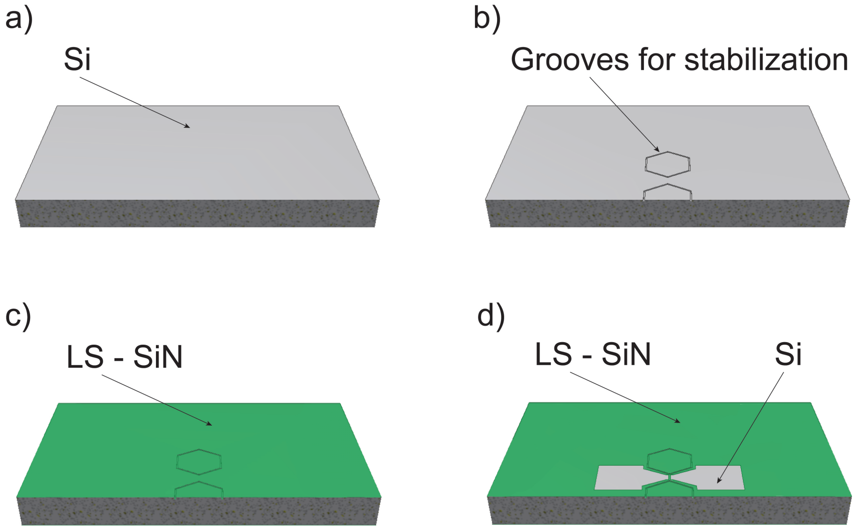


Figure 2.1: Section view of a stencil fabrication process where the membrane apertures are defined on the frontside. a) The fabrication process starts with a 100 mm Si wafer. b) Grooves for membrane stabilization can be etched into the Si by dry etching. c) The Si wafer is coated with low-stress SiN by low-pressure chemical vapor deposition (LPCVD). d) The membrane apertures are defined in the low-stress SiN by lithography and dry etching.

2.1.2 Membrane Release by Wet Etching

A membrane release by potassium hydroxide (KOH) wet etching allows parallel processing of several stencils. But the density of freestanding membranes on the wafer is limited by the characteristic KOH etching of Si, since the (111) Si plane and the thickness of the wafer determine a minimum distance between each membrane.

Following this approach, UV lithography defines backside openings in the low-stress SiN layer. A backside alignment to the previously defined membrane apertures is needed. Subsequent dry etching transfers the pattern into the SiN (Figure 2.2 a, b). Finally, KOH wet etching chemistry releases the stencil membranes (Figure 2.2 c).

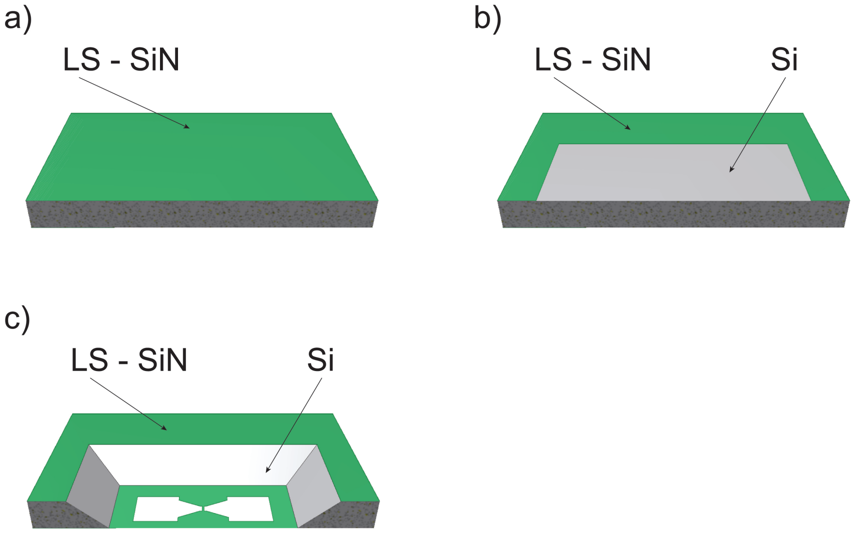


Figure 2.2: Section view of a stencil backside where the membrane is released by wet etching. Note: This is the backside of a stencil, which is already processed on the frontside as illustrated in Figure 2.1. a) Si wafer coated with low-stress SiN and previously defined membrane apertures. b) Backside openings are defined in the low-stress SiN layer by ultraviolet (UV) lithography and dry etching. c) Stencil membranes are released by potassium hydroxide (KOH) wet etching.

2.1.3 Membrane Release by Combined Dry and Wet Etching

Alternatively to a wet etching release, a combination of dry and wet etching can be applied. This approach allows of higher density of membranes on full-wafer scale. But due to the dry etching process step the membrane release is a partially serial process.

Carrying out this release method, a hard mask which is inert against the etching process has to be defined on the backside of the previously patterned wafer. A film of 500 nm Al is deposited by evaporation or sputtering (Figure 2.3 a, b). UV lithography defines backside openings of the stencil. Dry etching transfers the pattern into the Al (Figure 2.3 c) and low-stress SiN layer successively (Figure 2.3 d). The patterned Al layer is now used as a hard mask to etch the Si vertically by dry etching. The etching is carried out until less than 100 µm Si is left (Figure 2.3 e). The Al hard mask is then removed using an Al wet etch solution made of phosphoric, acetic and nitric acid (H_3PO_4 85 % : CH_3COOH 100 % : HNO_3 70 %, 5 : 3 : 75) (Figure 2.3 f). Finally, the remaining Si is removed by KOH wet etching to release the membranes (Figure 2.3 g).

2.2 Wafer Curvature Variations during Stencil Fabrication

The curvature of a wafer is changing during each step of the stencil fabrication. During fabrication, the surface stress of the wafer is changing as material is deposited or removed from the wafer surface [87]. The change of stress causes wafer curvature variations that happens all the time during processing. The curvature variations are usually not considered as they do not have an impact on most applications. In stencil lithography, the wafer curvature has a significant influence on the gap between a stencil membrane and the substrate surface and therefore on the resolution of the pattern transfer.

Three 525 µm thick and three 380 µm thick Si wafers were used to monitor the variation of curvature. Since the purpose of these experiments is to analyze the

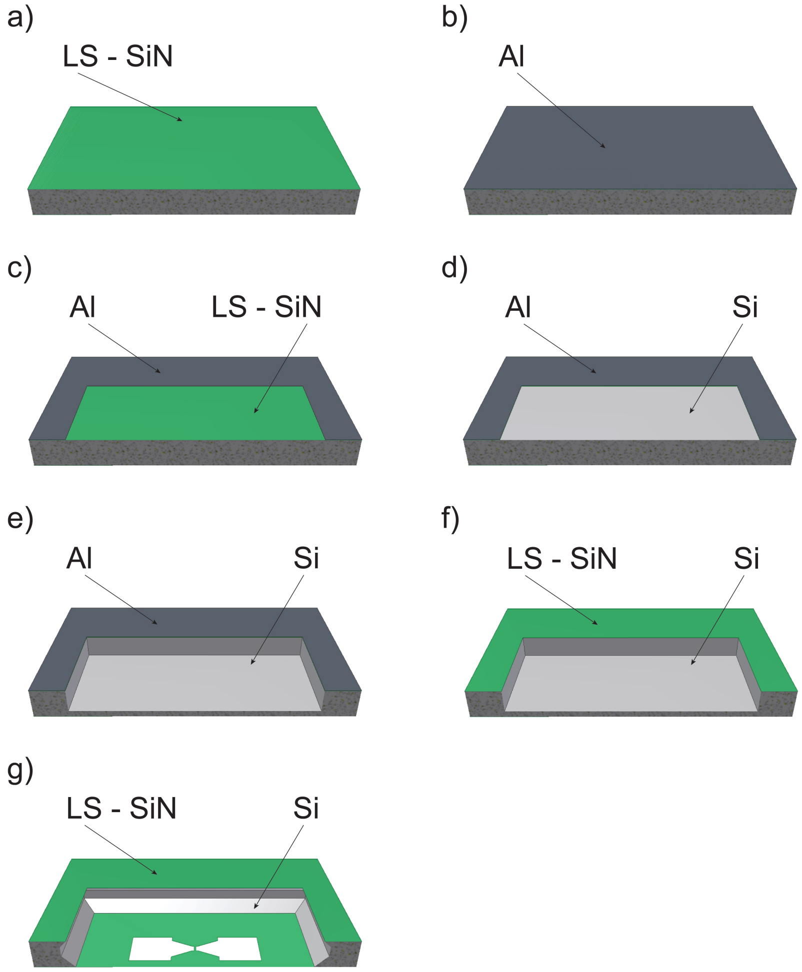


Figure 2.3: Section view of a stencil backside where the membrane is released by combined dry and wet etching. Note: This is the backside of a stencil, which is already processed on the frontside as illustrated in Figure 2.1. a) Si wafer is coated with low-stress SiN and previously defined membrane apertures. b) An Al layer is deposited on the backside either by evaporation or sputtering. c) Backside openings for the membrane release are defined in the Al layer. d) The pattern of the backside openings is transferred into the low-stress SiN. e) The patterned Al layer is used as a hard mask to etch the Si vertically. f) The Al layer is removed using an Al etch solution. g) Stencil membranes are released by KOH wet etching.

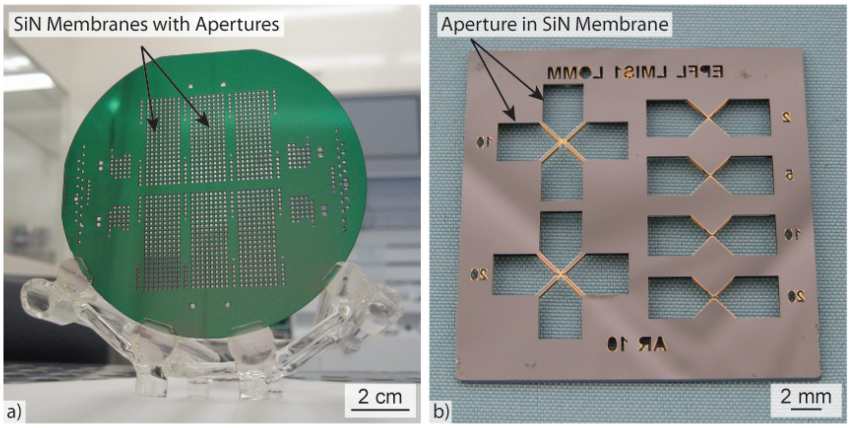


Figure 2.4: a) Example of a 100 mm full-wafer stencil. The membranes are released by KOH wet etching. b) Example of a chip-size stencil. The membranes are released by combined dry and wet etching.

wafer's curvature variations, the membrane stabilization step (Figure 2.1 b) was not applied. The membrane release was obtained by wet etching (cf. Subsection 2.1.2).

A 500 nm thin low-stress SiN layer was deposited on a Si wafer by LPCVD. The initial bending radius r_0 of the Si wafer was measured. The bending radius measurements were taken for two perpendicular orientations across the full wafer using a KLA-Tencor® thin-film stress-measurement system. The low-stress SiN on the backside of the wafer was patterned. The radius measurements were repeated in the same manner on the frontside of the wafer. Membrane apertures were then patterned in the low-stress SiN on the frontside of the wafer. The bending radius r was remeasured. Finally, the stencil membranes were released by wet etching and the bending radius measurements were repeated.

The curvature κ of the stencil during processing was extracted from the bending radius measurements. The curvature κ is defined as $1/r$ and the initial curvature κ_0 as $1/r_0$, respectively. The relative change of curvature $\kappa - \kappa_0$ was calculated and used for comparison. The curvature κ changed during each fabrication step. The relative wafer curvature change $\kappa - \kappa_0$ was increased after the backside patterning of the low-stress SiN layer, but the subsequent frontside patterning decreased the curvature change. The final membrane release increased again the relative change of curvature $\kappa - \kappa_0$ (Figure 2.5). The relative change of curvature $\kappa - \kappa_0$ had less impact on 525 µm thick Si wafers compared to thinner Si wafers. At the end of the stencil fabrication the relative change of curvature $\kappa - \kappa_0$ of 380 µm thick Si wafer increased by $(4.5 \pm 0.1) \cdot 10^{-3}\,\mathrm{m}^{-1}$ and $(2.1 \pm 0.1) \cdot 10^{-3}\,\mathrm{m}^{-1}$ for 525 µm thick Si wafer, respectively. In some cases this relative change of curvature $\kappa - \kappa_0$ made the wafer change its bending orientation. An initial negative curvature $\kappa < 0$ turned to a positive curvature $\kappa > 0$.

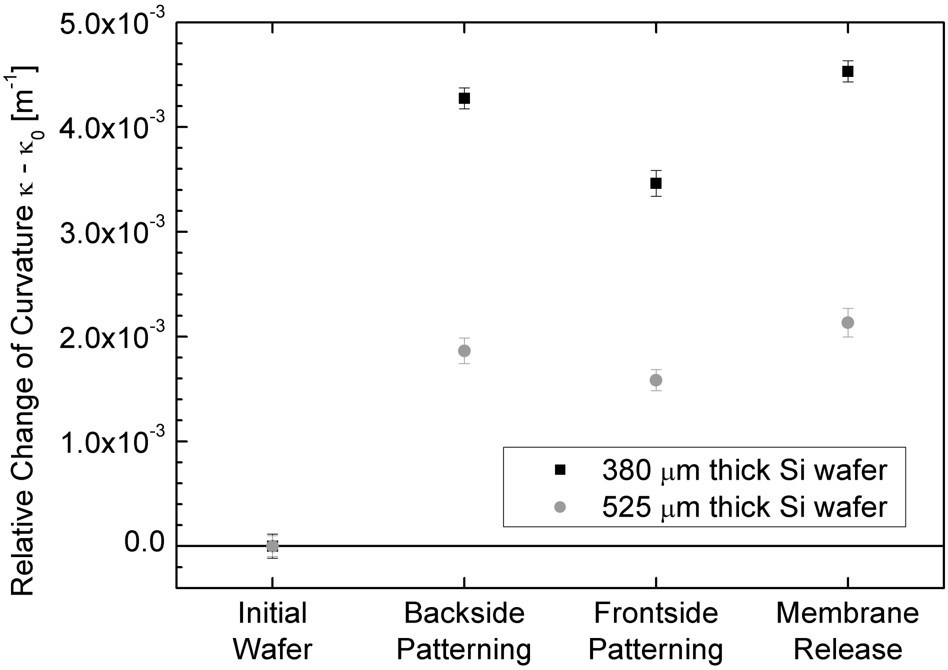


Figure 2.5: The variation of the relative change of wafer curvature $\kappa - \kappa_0$ was monitored after each stencil fabrication step.

Measurements of the bending radius r have shown how the wafer curvature κ changes during the stencil fabrication. The wafer curvature κ is related to the induced stress of a thin film on a substrate [87]. In the case of a stencil the SiN layer applies a compressive stress to the Si wafer. The patterning of stencil apertures on the frontside and openings on the backside modifies the induced stress. This modified stress causes the change of the wafer curvature κ. In addition, the etching for the membrane release reduces the stability of the Si wafer. The wafer curvature κ changes as the induced stress of the SiN layer has a higher influence.

2.3 Conclusion

Micro- and nanostencils can be fabricated in several ways applying standard patterning techniques. Large membranes with a critical aperture design are more reliable with membrane stabilization. The membrane release by KOH wet etching is a parallel processing, which is useful for the fabrication of several stencils. A higher density of freestanding membranes on a wafer can be obtained by a combined dry and wet etching release. Overall, the most suitable fabrication technique strongly depends on the stencil application.

The wafer curvature κ of a stencil is modified during each fabrication step. After the stencil fabrication, the relative change of curvature $\kappa - \kappa_0$ is increased by $(4.5 \pm 0.1) \cdot 10^{-3}\,\mathrm{m}^{-1}$ for 380 µm thick Si wafer and $(2.1 \pm 0.1) \cdot 10^{-3}\,\mathrm{m}^{-1}$ for 525 µm thick Si wafer. A stencil as flat as possible can be obtained taking into account the wafer curvature κ. A flat stencil minimizes the gap between a stencil membrane and a substrate and improves the resolution of the pattern transfer.

3 Metal Wires on Polymer Substrates

This chapter presents results of stencil lithography applied on polymer substrates. Wire test structures as a basic element for flexible electronics were designed for 2-point and 4-point measurements. The test structures were patterned with titanium (Ti) and Au on PEN, polyethylene terephthalate (PET) and PI as flexible polymer substrates. The electrical characterization was used to extract the wire resistivity.

3.1 Stencil Design

Stencil chips of 6 mm × 6 mm including three membranes were fabricated. The 500 nm thin low-stress SiN membranes include rims for stabilization and the membrane release was done by KOH wet etching chemistry (cf. Subsection 2.1.2). The membrane apertures were designed for electrical resistance measurements, and consist of two types of electrical test structures. First, 2-point test structures for standard resistance measurements were included. These test structures contain straight wires with different dimensions. The wires are connected to a contact pad on each end (Figure 3.1 a). Second, stencil membranes include wires structures with several contacts along them. This design allows 4-wire measurements of varying wire lengths (Figure 3.1 b).

The theoretical resistance R of a metal wire is given by:

$$R = \rho \frac{l}{A} = \rho \frac{l}{wt} \tag{3.1}$$

where ρ is the resistivity of the wire material, l the length, A the cross section, w the width and t the thickness of the wire. The aperture design of the electrical test structures takes into account the ratio between the length and the width of a

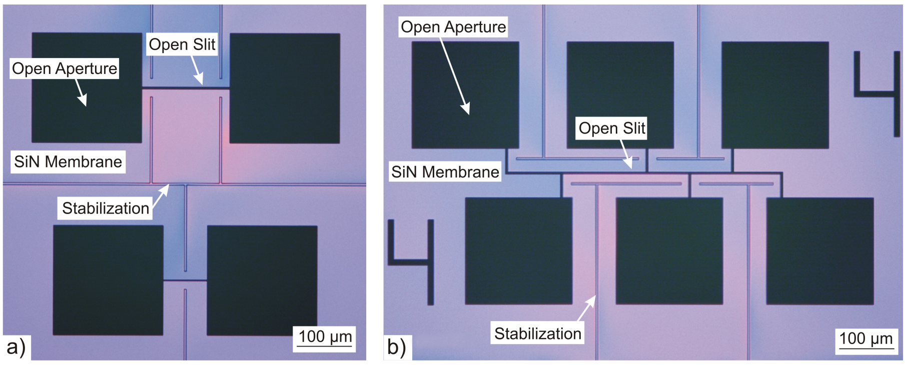


Figure 3.1: Optical illustrations of stencil apertures in a 500 nm thin low-stress SiN membrane including rims for stabilization. The design contains straight wires structures with various dimensions and contact pads for a) 2-point measurements and b) 4-point measurements of varying wire lengths.

wire. This ratio is a dimensionless number and represents the number of squares $\#sq$ along the wire (Figure 3.2).

$$\#sq = \frac{l}{w} \tag{3.2}$$

Substituting Equation 3.2 into Equation 3.2 the theoretical resistance R of a metal wire in respect of the number of squares $\#sq$ is now given by:

$$R = \rho \frac{\#sq}{t} \tag{3.3}$$

If the number of squares is kept constant but the width and the length is modified, the same resistance is expected to be measured. The thickness of the wires is assumed to be constant as all measured wires are fabricated in the same evaporation step. The wire design for both 2-point and 4-point measurements contains number of squares of 20, 40, 60 or 80. The wire widths are either 2 µm, 4 µm or 6 µm.

3.2 Polymer Substrates

PEN, PET and PI were used as polymer substrates for stencil lithography. The polymer films were obtained from Goodfellow®. Density, Young's Modulus, tensile

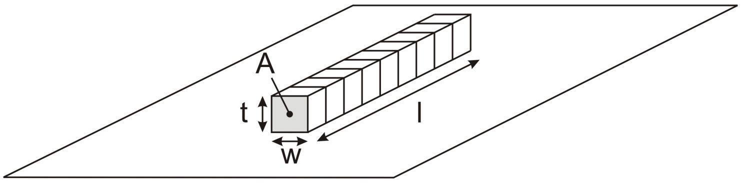


Figure 3.2: Schematic illustration of a wire. The ratio between the length l and the width w represents the number of squares along the wire. t is the thickness and A is the cross-section of the wire.

strength and film thickness of the polymer substrates are summarized in Table 3.1.

	Density (g/cm^3)	Young's Modulus (GPa)	Tensile Strength (MPa)	Film Thickness (μm)
PEN	1.36	5 - 5.5	200	125
PET	1.3 - 1.4	2 - 4	190 - 260	175
PI	1.42	2.5	230	125

Table 3.1: Mechanical properties of polymer substrates used for stencil lithography.

The polymer films were manually cut with scissors in substrates of approximately 6 mm × 6 mm. The polymer substrates were then cleaned before patterning the metal test structures by stencil lithography. The substrates were dipped into a soft soap and rinsed with deionized water. Subsequently, the substrates were rinsed in acetone followed by ethanol. Finally, the substrates were dried under a nitrogen (N_2) flow.

3.3 Patterning by Chip-Size Stencil Lithography

After cleaning (cf. Section 3.2) the polymer substrates the patterning by stencil lithography was done with the shortest possible delay. Therefore, a chip-sized stencil was positioned on a polymer substrate (Figure 3.3 a). The stencil and substrate were put into a stencil holder including a spring which clamped the substrate to the stencil membrane (Figure 3.3 b). 10 nm Ti as an adhesion layer and a 150 nm Au thin film were deposited through the stencil on the polymer substrate by e-beam evaporation (Figure 3.3 c). After the evaporation, the stencil and the stencil holder were removed, leaving the pattern on the polymer layer (Figure 3.3 d, Figure 3.4).

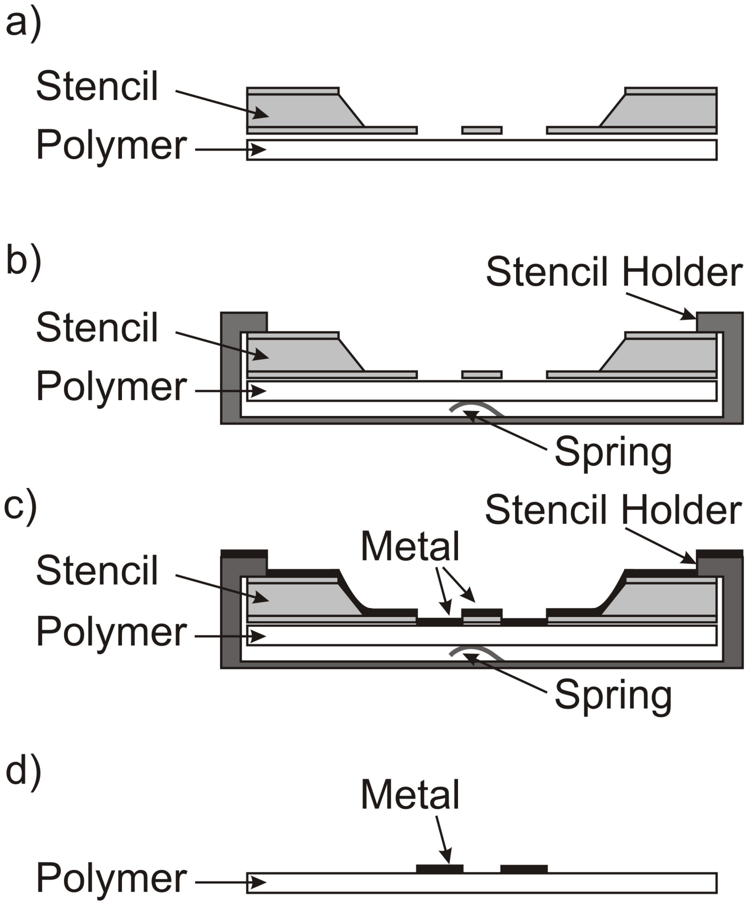


Figure 3.3: Process flow showing the schematic of the cross section for stencil lithography on polymer substrates. a) The stencil was placed on the polymer substrate. b) A stencil holder with a spring pressed the stencil membrane to the polymer substrate. c) Electron beam (e-beam) evaporation of metal transferred the pattern onto the substrate. d) The stencil and the stencil holder were removed, leaving the transferred pattern on the polymer layer.

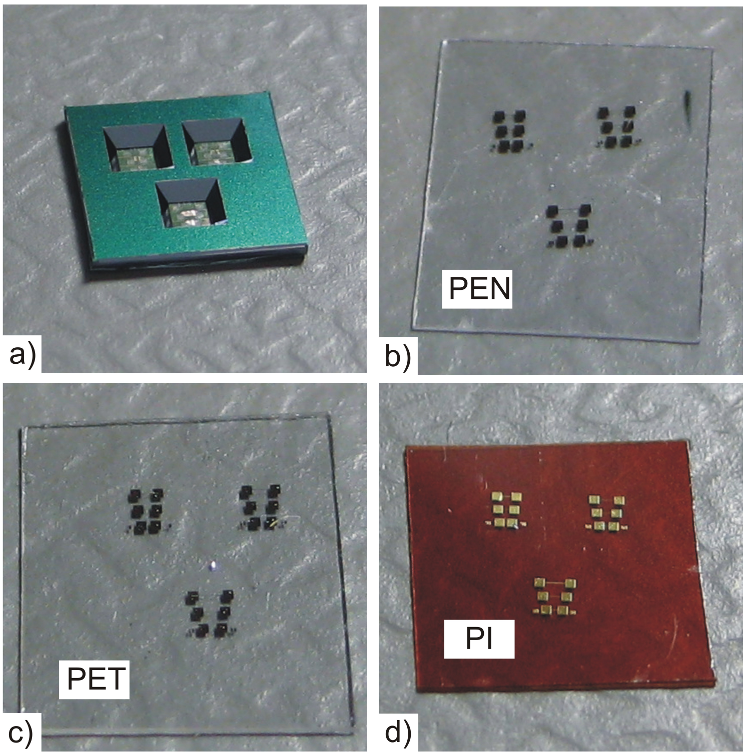


Figure 3.4: a) Optical illustrations of a 6 mm x 6 mm stencil chip with three membranes including apertures for electrical test structures. The stencil was applied to pattern titanium (Ti) - Au test structures on b) polyethylene naphthalate (PEN), c) polyethylene terephthalate (PET) and d) polyimide (PI).

3.4 Characterization

After evaporation, optical inspections revealed that the electrical test structures were successfully patterned on polymer substrates by stencil lithography (Figure 3.5). After the electrical characterization, the devices were coated by sputtering with an approximately 20 nm thin carbon layer to avoid charging while measuring their dimensions by scanning electron microscopy (SEM) (Figure 3.5). Due to the variation of the local gap between the stencil membrane and the polymer substrate, the wires are broader than the stencil apertures. The maximal observed broadening was approximately 200 nm from which a maximum gap of 20 µm is inferred.

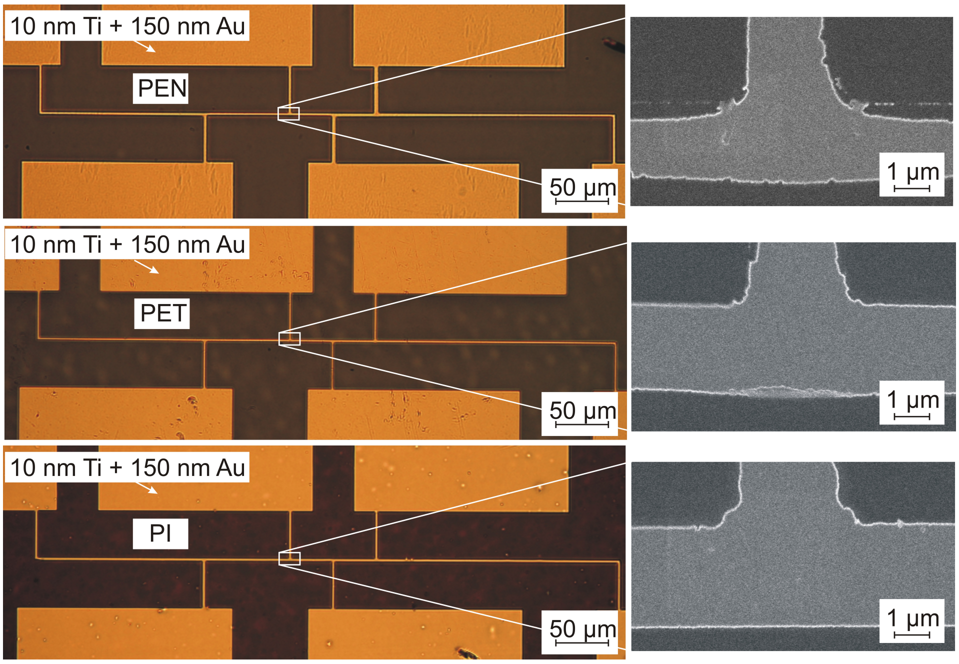


Figure 3.5: Optical illustrations on the left show evaporated test structures on polymer substrates for 4-point measurements. SEM illustrations show a zoom of a junction from the test structure.

3.4.1 2-Point Measurements

2-point measurements were carried out using the straight wires with contact pads on polymer substrates. A voltage was applied and the change in current was recorded to calculate the resistance of each wire. Afterwards, the width of each wire was measured. From the measured width, the exact number of squares along the wires was extracted. Figure 3.6 shows the resistance R vs. the number of squares $\#sq$ of straight wires. The intercept for each fit is set to be the contact resistance, which is the measured resistance across 2-points on the same pad. A linear analysis of the data was used to calculate the resistivity ρ of the Ti-Au film on each polymer substrate. The mean value on PEN was $(3.1 \pm 0.1) \cdot 10^{-8}\,\Omega$m, on PET was $(3.0 \pm 0.1) \cdot 10^{-8}\,\Omega$m and on PI was $(3.4 \pm 0.2) \cdot 10^{-8}\,\Omega$m (Table 3.2).

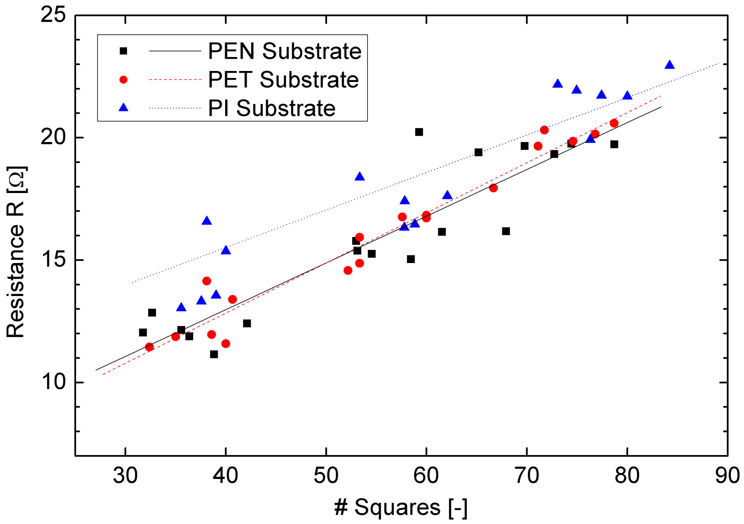


Figure 3.6: Graph shows R vs. $\#sq$ of straight wires on polymer substrates. From the slope of a linear analysis, the resistivity ρ of the wires was obtained to be $(3.1 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$ for PEN, $(3.0 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$ for PET and $(3.4 \pm 0.2) \cdot 10^{-8}\,\Omega\mathrm{m}$ for PI.

3.4.2 4-Point Measurements

To distinguish the contact resistance between the measuring probes and the polymer substrate, 4-point measurements were carried out using the test structures with six contact pads along a wire. Using the probe station an increasing current was applied on the outer pads of the test structure and the voltage drop over two contact pads was recorded. In addition, the width of the wire sections was measured to calculate the number of squares. Figure 3.7 shows the resistance R vs. the number of squares $\#sq$ of the electrical test structures on the polymer substrates. A linear analysis of the data was used to calculate the resistivity ρ of the Ti-Au film on each polymer substrate. The mean value of the data on PEN was $(3.3 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$, on PET was $(4.0 \pm 0.2) \cdot 10^{-8}\,\Omega\mathrm{m}$ and on PI was $(3.3 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$ (Table 3.2).

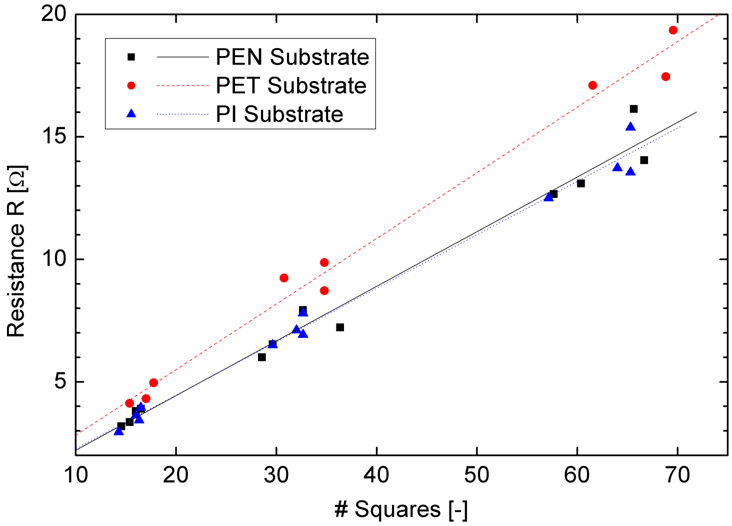


Figure 3.7: Graph shows R vs. $\#sq$ of electrical test structures on polymer substrates. From the slope of a linear analysis, the resistivity ρ of the wires obtained to be $(3.3 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$ for PEN, $(4.0 \pm 0.2) \cdot 10^{-8}\,\Omega\mathrm{m}$ for PET and $(3.3 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$ for PI.

	Resistivity ρ extracted from 2-point measurements	4-point measurements
PEN	$(3.1 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$	$(3.3 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$
PET	$(3.0 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$	$(4.0 \pm 0.2) \cdot 10^{-8}\,\Omega\mathrm{m}$
PI	$(3.4 \pm 0.2) \cdot 10^{-8}\,\Omega\mathrm{m}$	$(3.3 \pm 0.1) \cdot 10^{-8}\,\Omega\mathrm{m}$

Table 3.2: By 2-point and 4-point measurements extracted Ti-Au wire resistivities on PEN, PET and PI.

3.4.3 Ti-Au Thin Film

As a comparison resistivity ρ measurements were carried out on a Si wafer coated with a Ti-Au thin film. The film deposition was done by e-beam evaporation under identical conditions as previous Ti-Au wires were patterned. Using a 4-point measuring system a resistivity ρ of $(3.06 \pm 0.01) \cdot 10^{-8}\,\Omega\mathrm{m}$ was obtained.

3.5 Conclusion

Ti-Au wire test structures were successfully patterned by stencil lithography on polymer substrates. The dimensions of the wires were measured using SEM and appeared larger than designed. 2-point and 4-point measurement of the Ti-Au wire test structures have shown ohmic behavior. The resistivity on each polymer substrate was analyzed. The extracted values for the Au resistivity on all substrates corresponded to the measured value of a Ti-Au thin film on a Si wafer. These results show that stencil lithography is a suitable technique to pattern metals on polymer films.

4 Organic Pentacene Thin Film Transistors

This chapter presents the electrical characterization of TFTs and the development of pentacene TFTs on flexible substrates fabricated by stencil lithography. The fabrication of pentacene TFTs on flexible substrates is divided into three parts. First pentacene films on different substrates were characterized by atomic force microscopy (AFM). Rigid pentacene TFTs were fabricated and electrical characteristics were taken. Second, pentacene TFTs were defined on flexible substrates and electrically characterized. Finally pentacene TFTs on flexible substrates were optimized and electrically characterized under tensile stress.

4.1 Electrical Characterization of TFTs

The electrical DC (direct current) characterization of organic TFTs was done by the use of metal-oxide semiconductor field-effect transistor (MOSFET) characterization methods. Output characteristics were taken by applying a constant voltage V_G to the gate electrode to form a conducting channel (Figure 4.1). In parallel, a sweeping voltage V_D is applied between the drain and source electrode to obtain a current I_D across the channel. The output characteristics I_D vs. V_D of working organic TFTs have a typical appearance (Figure 4.2). For drain voltages $\left|V_D\right| << \left|V_G\right|$ the I_D is proportional to the voltage V_D. This area is called linear regime. When $\left|V_G\right| < \left|V_D\right|$ the drain current I_D saturates at a certain level independent on the drain voltage V_D. This area is called saturation regime.

Transfer characteristics were taken by applying a constant voltage V_D at the drain

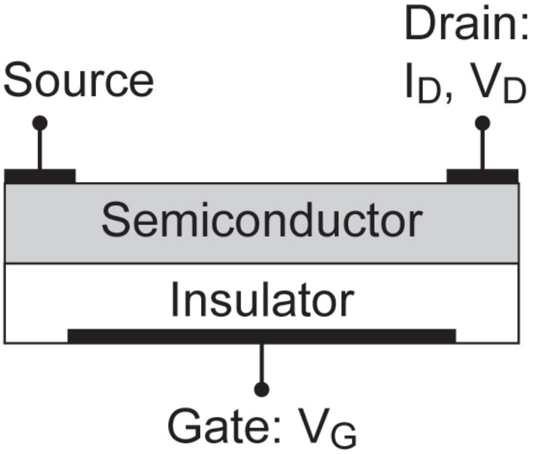


Figure 4.1: Schematic illustration of a TFT with indicated source (S), drain (D) and gate (G) contacts. Applying drain voltage V_D and gate voltage V_G and monitoring the drain current I_D are needed to characterize a TFT.

electrode. In parallel, a sweeping voltage V_G is applied at the gate electrode and the drain current I_D is monitored (Figure 4.2). The output characteristics I_D vs. V_D of working TFTs have a typical appearance with a linear regime at lower gate voltage V_G (Figure 4.3). Transfer characteristics were used to extract TFT typical parameters such as the apparent mobility μ, the transconductance g_m, the I_{on}/I_{off} ratio and the extrapolated threshold voltages V_T. The parameter extraction was done following the approach of Ghibaudo [88].

The apparent mobility μ was extracted by first calculating the transconductance g_m. The transconductance g_m is given by $\partial I_D/\partial V_G$ [89]. Using the transconductance g_m a function can be defined:

$$\frac{I_D}{\sqrt{g_m}} = \left(\frac{W}{L}\, c\, \mu\, V_D\right)^{1/2} (V_G - V_T) \tag{4.1}$$

where I_D is the drain current, g_m the transconductance, W the channel width, L the channel length, c the capacitance of the dielectric, V_G the gate voltage and V_T the threshold voltage of a TFT. From the plot $(I_D/\sqrt{g_m})$ vs. V_G of Equation 4.1,

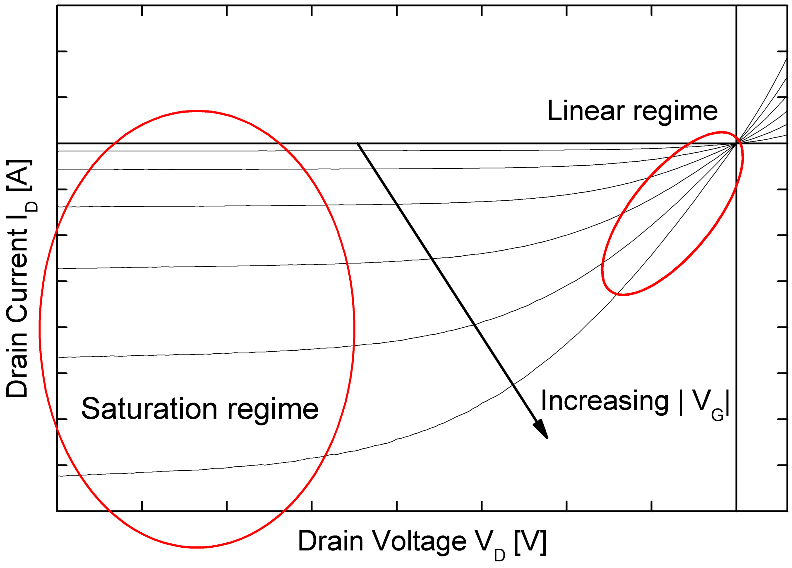


Figure 4.2: Typical output characteristic of a pentacene TFT. In the linear regime where $|V_D| << |V_G|$ the drain current I_D is proportional to the voltage V_D. In the saturation regime the drain current I_D saturates at a certain level independent on the drain voltage V_D.

the slope can be extracted as $\Delta(I_D/\sqrt{g_m})/\Delta V_G$ at lower gate voltage V_G.

$$\frac{\Delta\left(\frac{I_D}{\sqrt{g_m}}\right)}{\Delta V_G} = \left(\frac{W}{L}\; c\; \mu\; V_D\right)^{1/2} \tag{4.2}$$

Using Equation 4.2 the apparent mobility μ can be extracted independent of the threshold voltage V_T.

$$\mu = \left(\frac{\Delta\left(\frac{I_D}{\sqrt{g_m}}\right)}{\Delta V_G}\right)^2 \frac{L}{W\; c\; V_D} \tag{4.3}$$

The I_{on}/I_{off} ratio was extracted by plotting the drain current I_D of the transfer characteristics in logarithmic scale. The I_{on}/I_{off} ratio can be determined by counting the difference of decades in drain current I_{on}/I_{off} between zero and maximum gate voltage V_G.

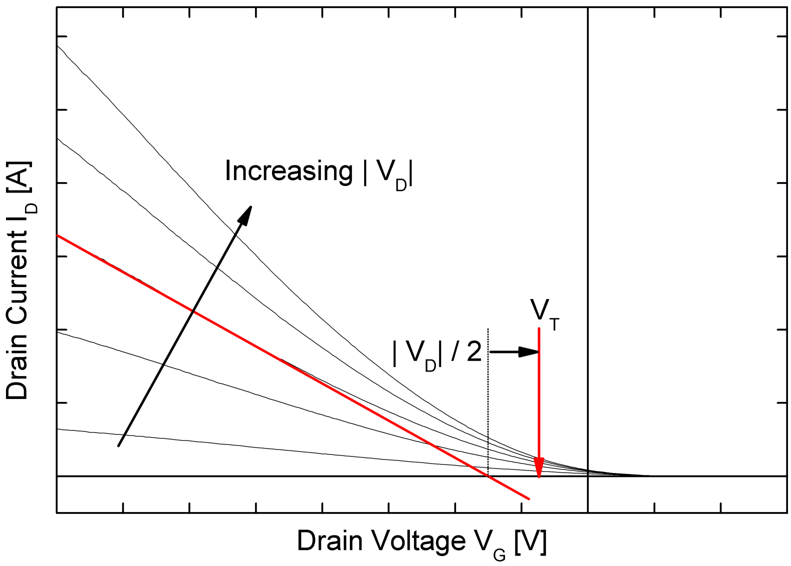


Figure 4.3: Typical transfer characteristic of a pentacene TFT. Transfer characteristics were used to extract TFT typical parameters.

Finally, the threshold voltage V_T was extracted by a linear analysis of the transfer characteristics at lower gate voltage V_G. The intercept of the linear fit on the V_G-axis minus $V_D/2$ is taken at the threshold voltage V_T (Figure 4.3).

In reality, the performance of organic TFTs is limited by the S/D contact resistance (Appendix A). Nevertheless, the presented calculations allow the extraction of the apparent mobility μ even tough an ideal TFT is assumed. The mobility of the channel is larger compared to the calculated value.

4.2 Pentacene TFTs with a PI or SiO_2 Dielectric and S/D Top Contacts

This section presents the fabrication and characterization of organic pentacene TFTs with S/D top contacts. A rigid Si wafer was chosen as the back gate contact. PI and SiO_2 as reference material were used as the dielectric layer. S/D top contacts were patterned by stencil lithography.

4.2.1 Pentacene Top Contact TFT Fabrication

Pentacene TFTs were fabricated using PI or SiO_2 as dielectric material. The fabrication started with a p-doped Si wafer (Figure 4.4 a). The Si wafer was coated with the dielectric material either PI or SiO_2. For PI as a dielectric layer, PI2610 from HD MicroSystems^{TM} was used. 60 wt% PI2610 + n-methyl-2-pyrrolidone (NMP) was spin coated at a speed of 5000 rpm for 40 s to define a 230 nm thick PI dielectric (Figure 4.4 b). The soft bake and the hard bake were carried out at 100°C for 180 s and 300°C for 2.5 h, respectively. Both hard and soft bake were done in a N_2 environment. For SiO_2 as a dielectric layer, 200 nm SiO_2 was grown on the Si wafer by thermal oxidation. The Si wafers with the dielectric layer were cut into samples of 2.5 cm × 2.5 cm. A sample with PI and a sample with SiO_2 as dielectric were loaded into a vacuum chamber pumped down to 10^{-6} mbar. Thermally evaporated pentacene was simultaneously deposited on both samples (Figure 4.4 c). Pentacene evaporations of 80 nm, 40 nm and 20 nm were carried out while keeping the substrate at room temperature. After the pentacene deposition, a stencil was placed on each sample for patterning S/D contacts (Figure 4.5 a). The stencil consist low-stress SiN as membrane material and bulk Si as membrane support. The membrane release was done following the approach of a combined dry and wet etching of the Si (cf. Subsection 2.1.3). The stencil design contains apertures to pattern S/D contacts. The S/D contacts define pentacene TFT channels in an aspect ratio of channel width to channel length $W/L = 10$ (Figure 4.5 b). The available channel lengths were 5 µm, 10 µm and 20 µm. The stencil-substrate configuration was mounted into a vacuum chamber. At a pressure of 10^{-7} mbar, 25 nm Au was evaporated through the stencil to define S/D contacts (Figure 4.4 d). During the Au evaporation, the substrates were cooled by liquid N_2 reducing the diffusion of Au into the pentacene layer. Finally, the stencil is removed, leaving S/D top contacts on the pentacene layer.

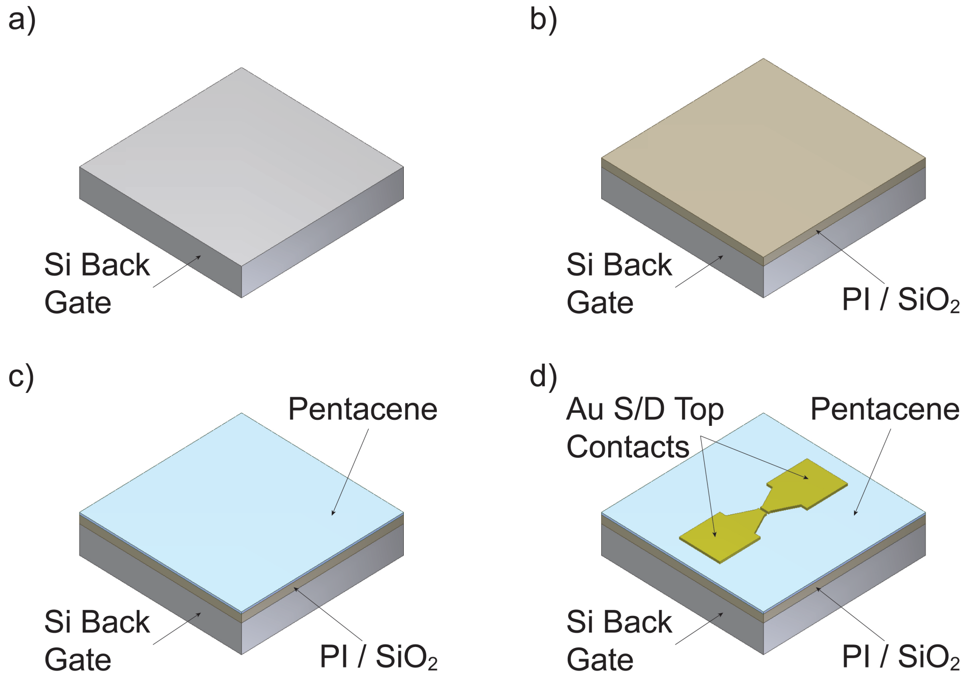


Figure 4.4: Schematic illustration of the pentacene TFT fabrication process with a Si wafer as a back gate. a) The fabrication process started with p-doped Si wafer. b) The Si wafer was coated with 230 mm PI or 200 nm silicon dioxide (SiO_2) as dielectric layer. c) 80 nm, 40 nm or 20 nm pentacene was thermally evaporated. d) A stencil was placed on the sample and 25 nm Au was evaporated to define source-drain (S/D) top contacts.

4.2.2 AFM and Electrical Characterization of Pentacene TFTs

The pentacene film growth on PI and SiO_2 was characterized by means of AFM. An AFM scan was taken at the edge of the sample where the pentacene film thickness transition can be observed. The sample holder as a mechanical mask shielded

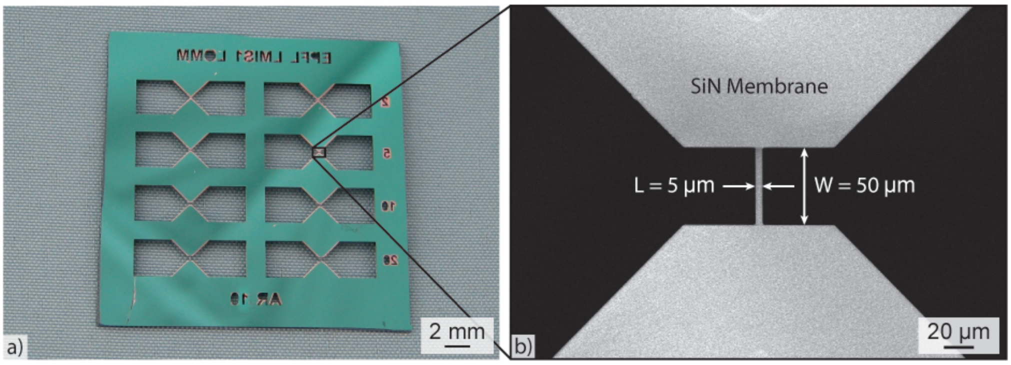


Figure 4.5: a) 2.5 cm × 2.5 cm stencil chip for S/D patterning of eight pentacene TFTs. b) Stencil membrane magnified by SEM. The apertures define a 5 µm long and 50 µm wide channel.

partially the pentacene deposition thus single layers of pentacene and the creation of pentacene grains could be observed (Figure 4.6). Pentacene films on PI and SiO$_2$ show a continuous layer transition where single pentacene grains touch each other. Pentacene grains on SiO$_2$ are larger compared to pentacene grains on PI. On SiO$_2$ pentacene forms a continuous film within the first layer of evaporated pentacene whereas on PI, multiple layers are needed to create a continuity of a pentacene film.

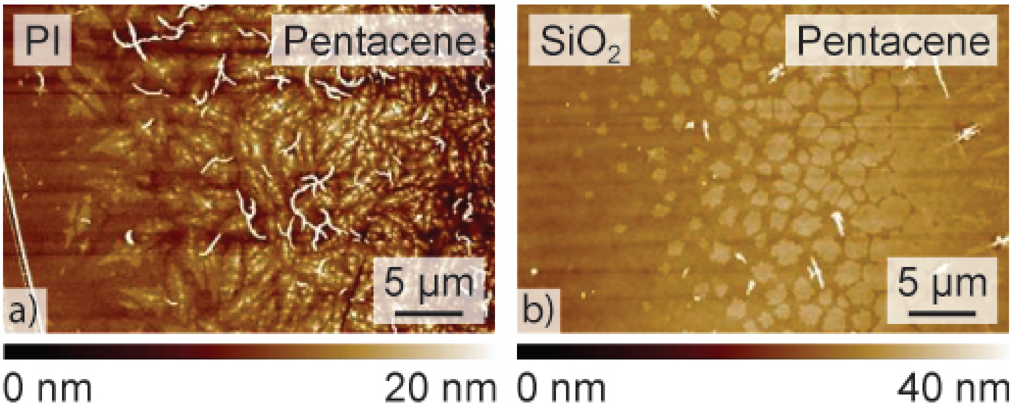


Figure 4.6: AFM illustrations of the film transition of 20 nm thermally evaporated pentacene. a) Pentacene depositied on PI. b) Pentacene deposited on SiO$_2$.

AFM scans of pentacene films close to the pentacene TFT channel location were taken on samples with PI and SiO_2 as a dielectric. An area of 15 µm × 15 µm was scanned in all cases (Figure 4.7). An 80 nm thick pentacene film on PI showed a continuous film (Figure 4.7 a). Most pentacene grains were approximately 500 nm in diameter and few reached a size up to 2 µm with a dendrite-like character. Pentacene grains of a 80 nm thick film on SiO_2 were larger compared to the PI substrate (Figure 4.7 b). The pentacene grains had dendrite shape and pronounced terraces of single monolayers. A 40 nm thick pentacene film on PI showed smaller grains in comparison with the 80 nm thick film (Figure 4.7 c). The grains were in contact and had an approximate size of 400 nm. Some pentacene film defects were visible as single fibres, which were probably covered for thicker pentacene layers. 40 nm pentacene on SiO_2 resulted in several micrometer large grains (Figure 4.7 d). The dendrite-like shape and the terrace structure were visible. 20 nm pentacene on PI had similar characteristics as a 40 nm thick pentacene film (Figure 4.7 e). The single grains touched each other and were approximately 400 nm in size. Some film defects appeared as single fibres. A 20 nm thick pentacene film on SiO_2 showed a continuous film with grains of several micrometers in size (Figure 4.7 f). The dendrite-like shape and the terrace structure of the grains were still visible.

Pentacene TFTs on both PI and SiO_2 dielectrics and with different pentacene film thicknesses were characterized electrically and the apparent mobility μ was extracted. Pentacene films were 80 nm, 40 nm or 20 nm thick and S/D contacts defined a 5 µm, 10 µm or 20 µm long channel. The measurements were taken under an argon (Ar) atmosphere and the measurement setup was shielded from light. The output characteristics have shown a linear regime close to zero drain voltage V_D and saturated at negative drain voltages V_D (Figure 4.8). In addition, the channel conductance g_D was extracted by $\partial I_D/\partial V_D$ [89].

TFTs with 80 nm pentacene on PI and SiO_2 have shown similar characteristics of channel conductance g_D vs. gate voltage V_G (Figure 4.9). The extracted apparent mobilities μ and the channel conductance g_D for TFTs with PI as a dielectric were slightly higher than the apparent mobilities μ of TFTs with SiO_2 as the dielectric

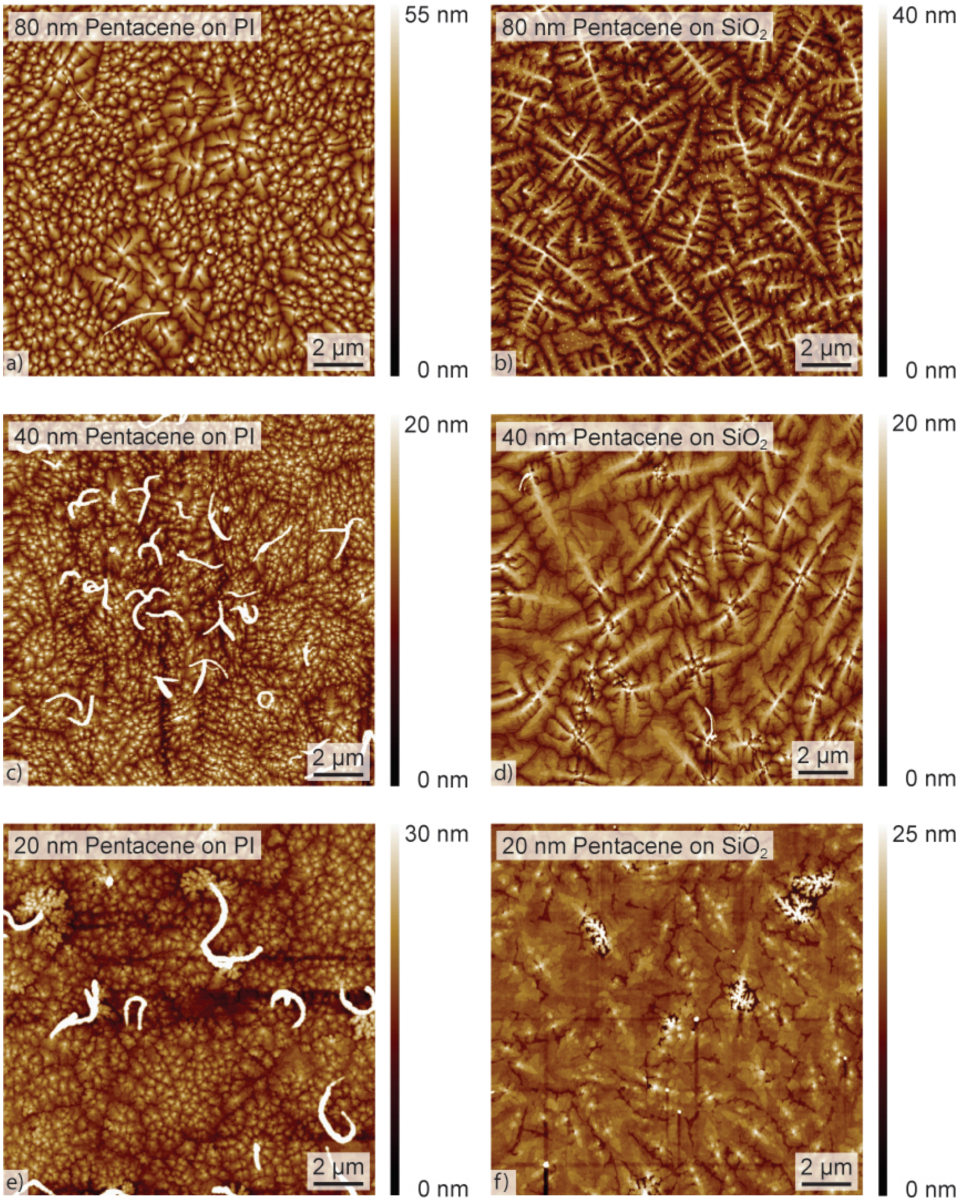
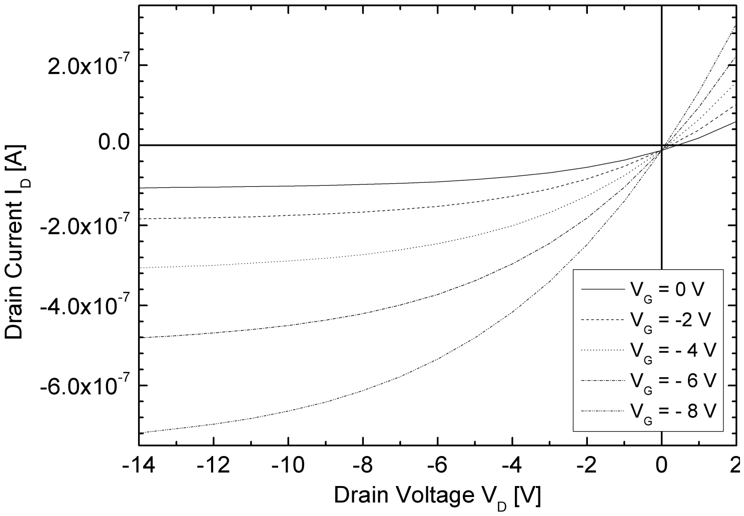
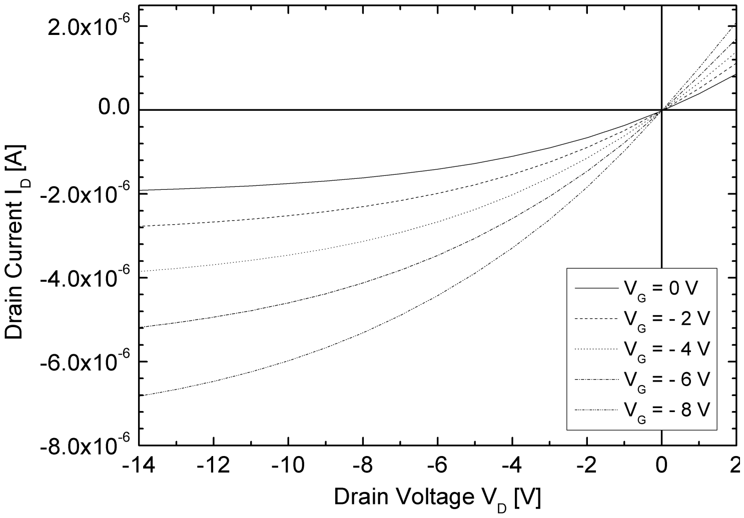


Figure 4.7: AFM illustrations of thermally evaporated pentacene films. a) 80 nm pentacene on PI. b) 80 nm pentacene on SiO_2. c) 40 nm pentacene on PI. d) 40 nm pentacene on SiO_2. e) 20 nm pentacene on PI. f) 20 nm pentacene on SiO_2.



(a) I_D–V_D output characteristics of a pentacene TFT with PI as the dielectric layer.



(b) I_D–V_D output characteristics of a pentacene TFT with SiO_2 as the dielectric layer.

Figure 4.8: Electrical characteristics of TFTs with a 20 µm long channel and 40 nm pentacene.

layer.

TFTs with 40 nm pentacene have shown different electrical characteristics for PI and SiO$_2$ as dielectric layer (Figure 4.10). SiO$_2$ as the dielectric material resulted in a distinctively higher channel conductance g_D than with PI. In addition, the extracted apparent mobility μ for TFTs with SiO$_2$ was higher compared to TFTs with PI.

Finally, TFTs with a 20 nm thick pentacene layer have shown characteristics of working TFTs but the extracted apparent mobility μ was lower compared to thicker pentacene film thicknesses. The channel conductance g_D of TFTs on PI and SiO$_2$ had a similar order of magnitude (Figure 4.11).

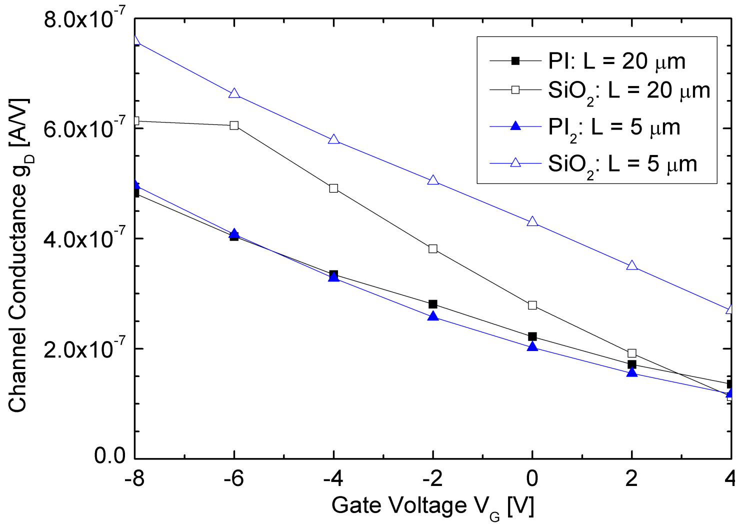


Figure 4.9: Channel conductance g_D vs. gate voltage V_G of pentacene TFTs including a PI or SiO$_2$ dielectric layer. The pentacene film thickness was 80 nm.

Typical apparent mobilities μ of pentacene TFTs with a 5 µm long channel are summarized in Table 4.1.

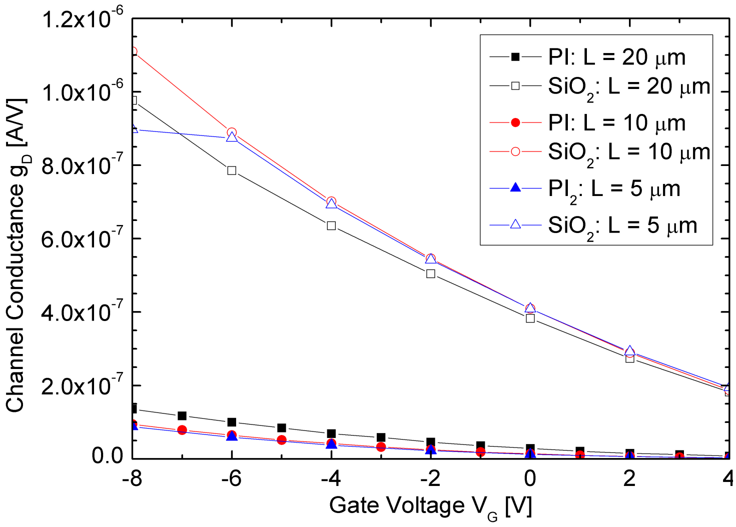


Figure 4.10: Channel conductance g_D vs. gate voltage V_G of pentacene TFTs including a PI or SiO_2 dielectric layer. The pentacene film thickness was 40 nm.

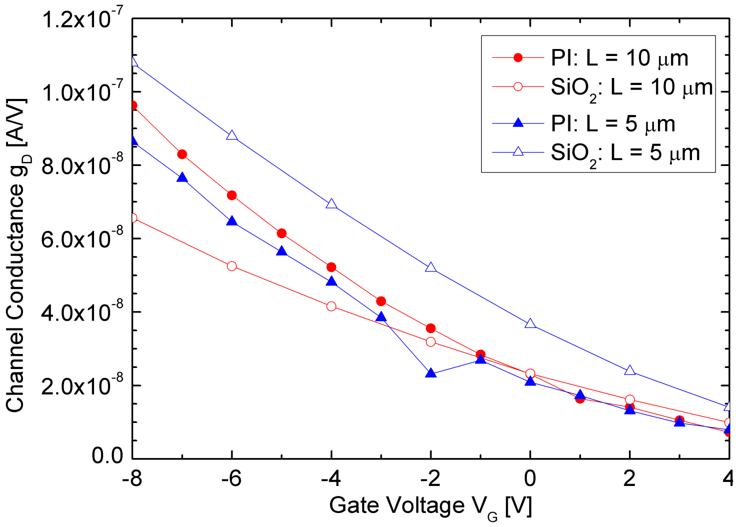


Figure 4.11: Channel conductance g_D vs. gate voltage V_G of pentacene TFTs including a PI or SiO_2 dielectric layer. The pentacene film thickness was 20 nm.

Pentacene film thickness	Apparent mobility μ PI dielectric	 SiO_2 dielectric
80 nm	$0.36\,cm^2/Vs$	$0.28\,cm^2/Vs$
40 nm	$0.15\,cm^2/Vs$	$0.46\,cm^2/Vs$
20 nm	$0.10\,cm^2/Vs$	$0.06\,cm^2/Vs$

Table 4.1: Apparent mobilities μ of pentacene TFTs with a 5 µm long and 50 µm wide channel. The dielectric was made of PI or SiO_2 and the pentacene film thicknesses were 80 nm, 40 nm or 20 nm.

4.2.3 Analysis of Pentacene Films on PI and SiO_2 Dielectrics

Pentacene layers on different substrates and with several film thicknesses were characterized by AFM. The deposited layers have shown different film morphologies on PI and SiO_2. It has been previously observed that the pentacene film morphology largely depends on the characteristics of the substrate surface [43, 90–92] as well as on the substrate temperature and pentacene deposition rate [40, 41].

Pentacene films were continuous on both substrates independent on the film thickness as working TFTs were obtained in all cases. The electrical measurements on the fabricated devices have shown typical characteristics of working organic TFTs. Depending on the dielectric material and on the pentacene thickness the performance was changing. The properties of the dielectric layer have an impact on the channel formation while a gate voltage V_G is applied. A thin dielectric layer is usually aimed as lower gate voltages V_G are needed to form a conducting channel. A high dielectric capacitance c improves the TFT performance by increasing the amount of induced charges in the conducting channel [89]. The electrical performance of pentacene TFTs with SiO_2 as dielectric layer was expected to be higher than pentacene TFTs with PI as dielectric layer since the measured capacitance of PI was $1.10 \cdot 10^{-8}\,F/cm^2$ and of SiO_2 $1.95 \cdot 10^{-8}\,F/cm^2$, respectively. Within the carried out experiments, pentacene TFTs made of SiO_2 and 40 nm pentacene have shown the highest performance. On the contrary, a better performance of TFTs with PI as dielectric layer and 80 nm pentacene were obtained compared to SiO_2 (Table 4.1).

This result indicates that the electrical performance not only depends on the capacitance *c*. Other effects such as the film morphology [43, 93, 94], the dielectric surface [92], the device processing [95] and especially the contact resistance [96] (Appendix A) have a high influence on the electrical performance of organic TFTs.

In conclusion, working pentacene TFTs with a Si back gate, PI or SiO_2 dielectric layers and Au top contacts were obtained. S/D contacts for channels down to 5 µm were defined by stencil lithography. The pentacene TFTs had typical working characteristics with similar behaviors. The carried out experiments have shown that a PI dielectric with a lower capacitance *c*, compared to a SiO_2, does not necessarily has a lower electrical performance. A sufficient electrical performance was also obtained with PI as dielectric layer. It is assumed that the electrical performance is mainly limited by the S/D contact resistance. The best TFT performance with PI as dielectric was obtained with an increased pentacene film. Thus, for the next experiments on pentacene TFTs on flexible substrates, the pentacene film thickness is not optimized for especially thin semiconducting layers.

4.3 Pentacene TFTs on a Flexible Substrate

The previous section 4.2 described the fabrication and characterization of pentacene TFTs on a rigid substrate with Si as the back gate contact and PI or SiO_2 as the dielectric layer. Au top contacts were patterned by chip-size stencil lithography. This section concentrates on the realization of pentacene TFTs on a flexible PI substrate. The experiments include aligned full-wafer stencil lithography for locally patterned pentacene and S/D contacts definition.

4.3.1 Pentacene TFT Fabrication on Flexible PI Substrates

Organic TFTs were fabricated using PI as both flexible substrate and gate dielectric material, Au pads as contacts for gate, source and drain, and pentacene as the organic semiconductor (Figure 4.12 a, Figure 4.12 b). A rigid wafer was used to handle the flexible PI substrate through all the processing steps. Stencil lithography enables solvent-free local patterning of pentacene followed by the deposition of the Au S/D top contacts.

Two full-wafer stencils with different designs were fabricated to locally pattern pentacene and to define S/D as top contacts. The stencils were made of a 100 mm Si wafer and 500 nm low-stress SiN as membrane material. The membranes were released by KOH wet etching (cf. Subsection 2.1.2). The full-wafer stencils included alignment marks to position stencil apertures relative to the patterned gate contacts on the substrate (Figure 4.12 c). A customized MA/BA6 SUSS MicroTec tool was used for stencil alignment, with an alignment accuracy around 2 µm. The membrane apertures for local pentacene patterning were rectangles, few micrometers larger than the channel dimensions. Membrane apertures for S/D top contacts defined channel lengths of 3 µm to 20 µm and channel widths of 3 µm to 50 µm (Figure 4.12 d).

The pentacene TFTs were fabricated using a full-wafer stencil-based process. The fabrication started with a 100 mm Si wafer as a rigid substrate to support all the processing steps (Figure 4.13 a). The Si wafer was spin coated with PI (PI2611

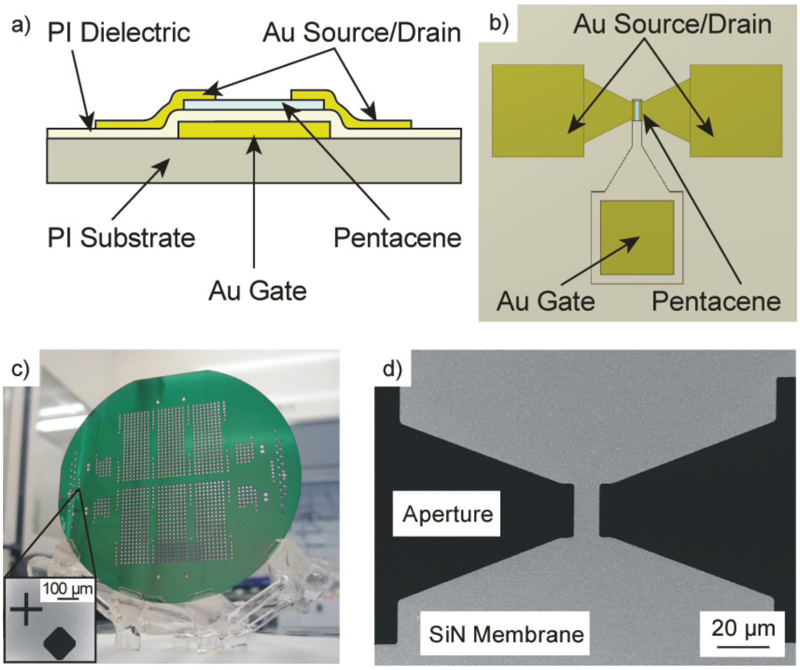


Figure 4.12: a) Schematic cross section of a pentacene TFT on a flexible 12 µm thin PI substrate. PI is used as gate dielectric, pentacene as organic semiconductor, Au as gate and S/D top contacts. b) Schematic top view of a pentacene TFT on a flexible PI substrate including S/D and gate contacts. Pentacene is locally patterned above the gate contact. c) Full-wafer stencil made of a Si wafer and low-stress SiN as membrane material. Inset: Stencil lithography alignment marks. d) Apertures in a low-stress SiN membrane to pattern S/D top contacts.

from HD MicroSystems^{TM}) at a speed up to 1000 rpm for 40 s to obtain a 12 µm thin layer (Figure 4.13 b). The soft bake was carried out at 100°C for 180 s and the hard bake at 300°C for 2.5 h, respectively. Both hard and soft bake were done in a N_2 environment. Gate contact pads are defined by standard lift-off processing using UV lithography. 10 nm Ti as an adhesion layer and 100 nm Au as gate material were evaporated by means of e-beam (Figure 4.13 c). 60 wt% PI2610 + NMP was spin coated at a speed of 5000 rpm for 40 s to define a 230 nm thick dielectric (Figure 4.13 d). The soft bake and the hard bake were also carried out at 100°C for 180 s and 300°C for 2.5 h, respectively. The dielectric thickness was measured at several places on the wafer and found to be uniform within 12 nm. UV lithography and oxygen (O_2) plasma were then used to open the contact pad of the gate electrode (Figure 4.13 e). A second lift-off processing patterned 10 nm thin Ti adhesion pads for S/D contacts (Figure 4.13 f). A full-wafer stencil with apertures for pentacene deposition was aligned to the prepatterned substrate. 45 nm pentacene was thermally evaporated and deposited locally through the aligned stencil above the gate contacts using a vacuum chamber at room temperature (Figure 4.13 g). After removing the stencil, a second full-wafer stencil was aligned and 100 nm thin Au electrodes as S/D contacts were deposited through the membrane apertures by e-beam evaporation (Figure 4.13 h). The second stencil was removed from the substrate. After pentacene and Au stencil depositions, both stencils were cleaned of the remaining material before further use. The pentacene is removed by exposing the stencil to O_2 plasma at 500 W for 10 min. The Au film on the second stencil is removed using a Au etch solution made of potassium iodide, iodine and water ($KI : I_2 : H_2O$, 3 : 1 : 96) [74, 83]. Both stencils were used for four evaporation-cleaning cycles, and remained functional. The adhesion of the PI as a flexible substrate to the Si carrier wafer has been optimized to stand all processing, while being low enough to allow simple detachment by peeling off the film in a reliable way (Figure 4.13 i, 4.14).

4.3.2 Electrical Pentacene TFT Characterization

The gate dielectric was independently tested using dedicated designs on the same wafer as the transistors. Metal-insulator-metal (MIM) structures were fabricated to test the 230 nm thick PI layer as gate dielectric. The MIM contact pads are made of Au and have a size of 150 µm × 150 µm. The characterization of the gate dielectric was done by measurements of capacitance and leakage current vs. applied voltage of the mentioned test structures. A dielectric strength of $2.3 \cdot 10^6$ V/cm and a leakage current on the order of 10^{-9} A/cm^2 were obtained up to fields of $2 \cdot 10^6$ V/cm. A relative permittivity $\epsilon_{r,PI} = 2.6 \pm 0.2$ of the PI was extracted.

Pentacene TFTs of various channel widths and lengths (Figure 4.15) were characterized electrically. The output and transfer characteristics of a transistor with

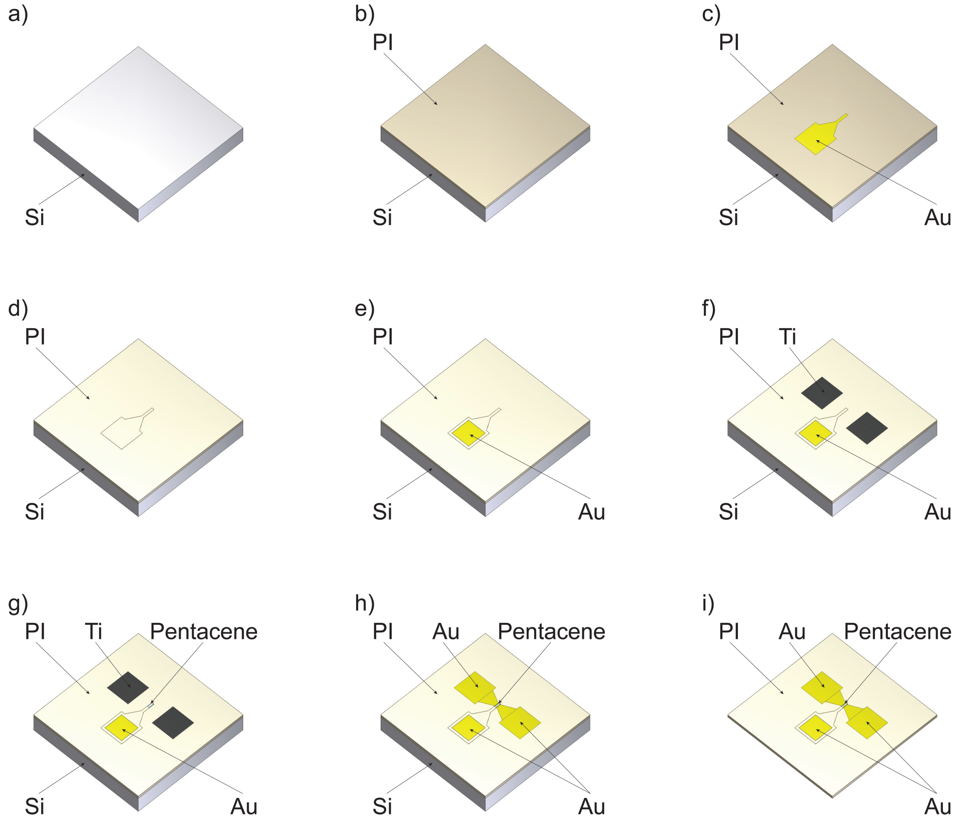


Figure 4.13: Schematic illustration of a flexible pentacene TFT. a) The fabrication process started with a 100 mm Si wafer. b) The Si wafer was spin coated with PI to obtain a 12 µm thin layer. c) Ti-Au gate contact pads are defined by lift-off processing. d) 60 wt% PI2610 + n-methyl-2-pyrrolidone (NMP) was spin coated to define a 230 nm thick dielectric. e) UV lithography and oxygen (O_2) plasma were used to open the contact pad of the gate electrode. f) Lift-off processing patterned thin Ti adhesion pads for S/D contacts. g) A full-wafer stencil with apertures for pentacene deposition was aligned to the prepatterned substrate. The pentacene was thermally evaporated locally through an aligned stencil above the gate contacts using a vacuum chamber at room temperature. h) A second full-wafer stencil was aligned and thin Au electrodes as S/D contacts were deposited through the membrane apertures by e-beam evaporation. i) The adhesion of the PI as a flexible substrate to the Si carrier wafer was low enough to allow simple detachment by peeling off the film.

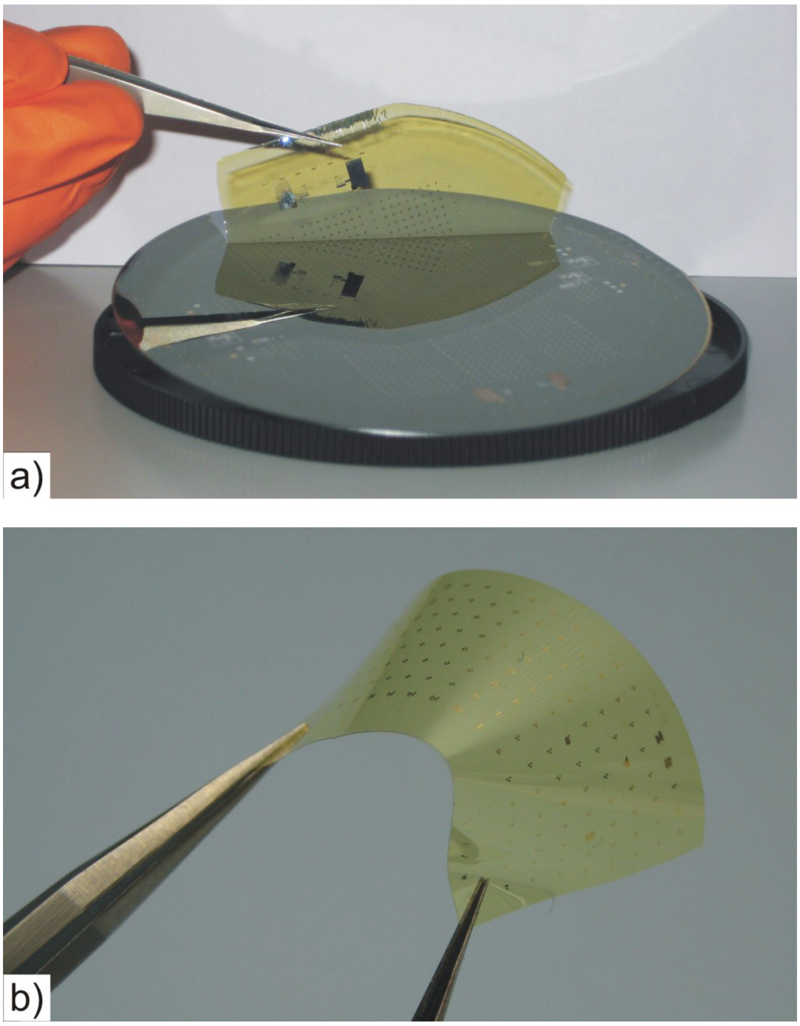


Figure 4.14: a) Pentacene TFTs on a flexible 12 µm thin PI substrate are peeled off the Si wafer after processing. b) Peeled off pentacene TFTs on a flexible PI substrate.

a channel length $L = 10\,\mu\text{m}$ and a channel width of $W = 20\,\mu\text{m}$ showed satisfactory levels of drain current I_D, with typical transistor-like behavior in the linear and saturation regimes (Figure 4.16). In addition, gate and drain biases required to be higher than 15 V to obtain an on-current of 5 nA/µm or higher. From the transfer characteristics the extracted apparent mobility μ of pentacene TFTs on flexible PI substrates was lower than of previously fabricated pentacene TFTs using Si as a rigid back gate (cf. Section 4.2). The extracted apparent mobility μ of fabricated pentacene TFTs on flexible substrates was $5.6 \cdot 10^{-2}\,\mathrm{cm^2/Vs}$ and extrapolated threshold voltage V_T was $-3.8\,\mathrm{V}$. After detaching the PI substrate including pentacene TFTs off the wafer, the TFT apparent mobility μ slightly decreased to $5.3 \cdot 10^{-2}\,\mathrm{cm^2/Vs}$, whereas the threshold voltage V_T stayed constant.

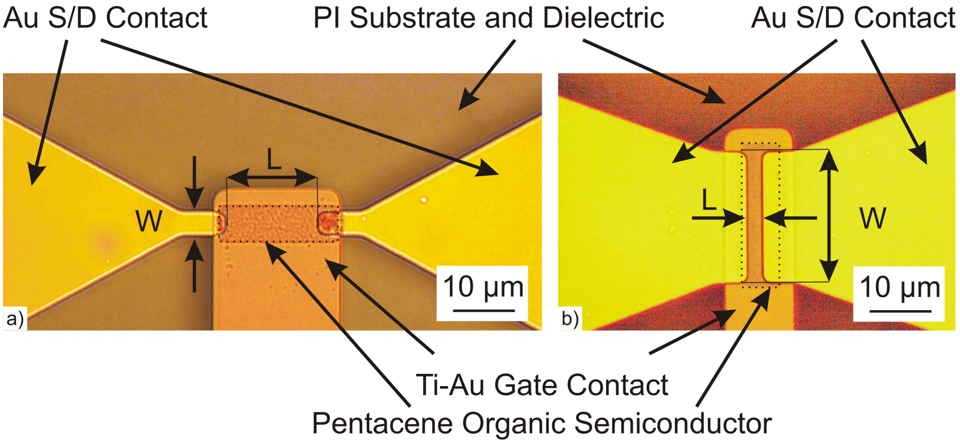
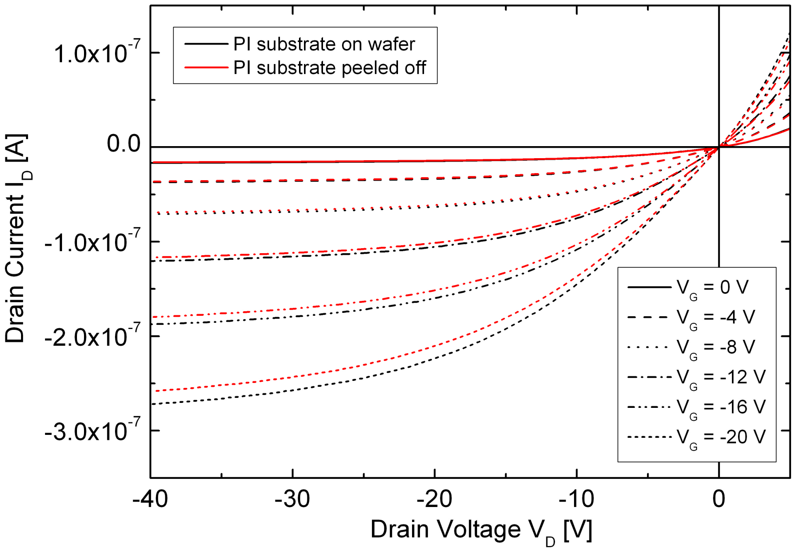


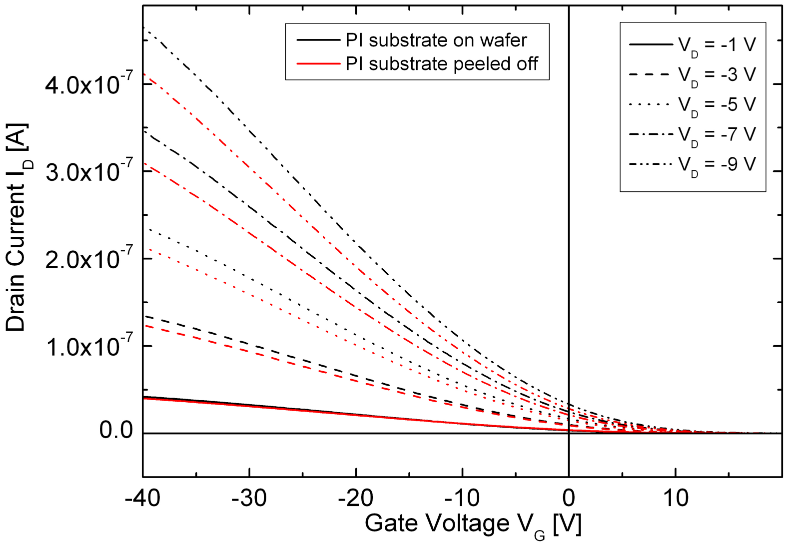
Figure 4.15: Two pentacene TFTs fabricated by a stencil lithography-based process. The dotted line guides the eye where pentacene was locally patterned above the gate contact. S/D top contacts were aligned to the gate contact.

Channel dimensions of $L > W$ have been realized to explore the possibilities of stencil lithography. The output and transfer characteristics of such a transistor with $L = 10\,\mu\mathrm{m}$ and $W = 3\,\mu\mathrm{m}$ peeled off the wafer showed transistor-like behavior and the drain current I_D scaled down with the channel width W (Figure 4.17). From the transfer characteristics the extracted apparent mobility μ of such a pentacene TFTs was $3.3 \cdot 10^{-2}\,\mathrm{cm^2/Vs}$ and the extrapolated threshold voltage V_T is $-3.2\,\mathrm{V}$.

A pentacene TFT with $L = 4\,\mu\mathrm{m}$ and $W = 50\,\mu\mathrm{m}$ was fabricated to push the limit to shorter channel lengths with S/D top contact configuration. The characterization of such a pentacene TFT showed as the previous examples transistor-like behavior and a sufficient level of drain current I_D (Figure 4.18). The extracted apparent

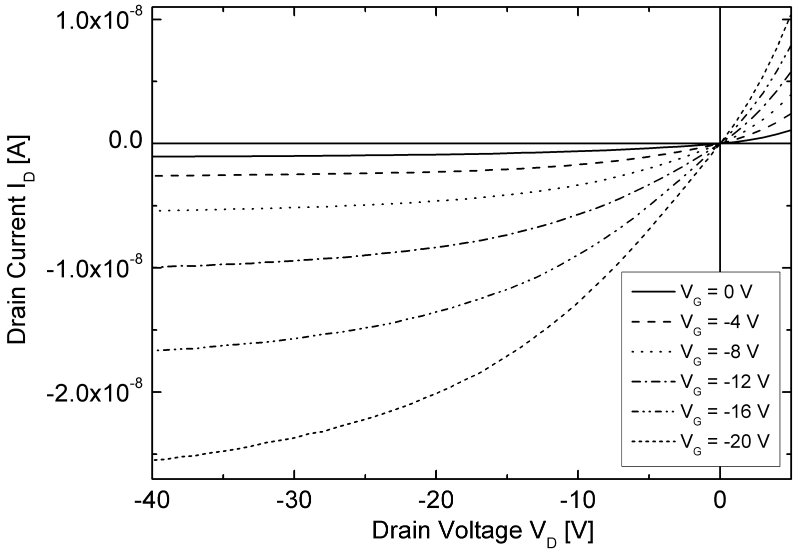


(a) I_D–V_D output characteristics

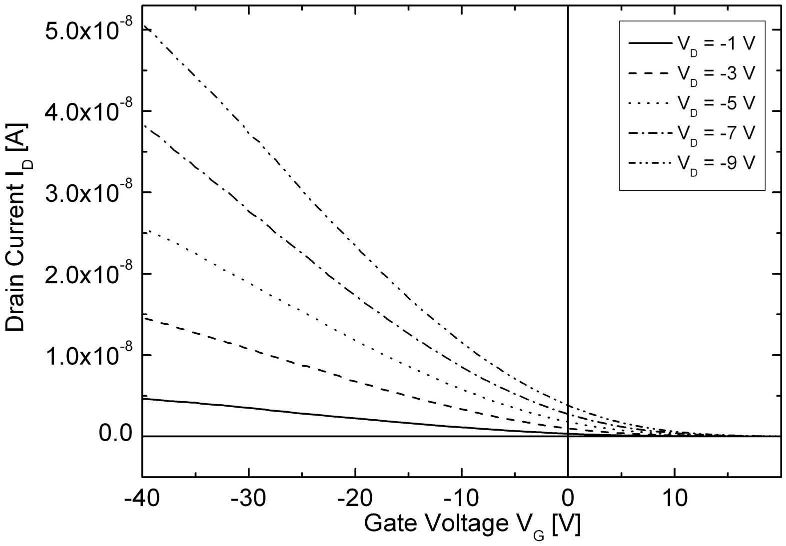


(b) I_D–V_G transfer characteristics

Figure 4.16: Electrical characteristics of a pentacene TFT of 10 µm channel length and 20 µm channel width before and after peeling the PI substrate off the Si wafer.



(a) I_D–V_D output characteristics



(b) I_D–V_G transfer characteristics

Figure 4.17: Electrical characteristics of a pentacene TFT of 10 µm channel length and 3 µm channel width after peeling the PI substrate off the Si wafer.

mobility μ was $3.9 \cdot 10^{-2}\,\mathrm{cm^2/Vs}$, and threshold voltage V_T was $-3.0\,\mathrm{V}$. Drawbacks of this pentacene TFT were a less dominant saturation regime in the output characteristics, which were probably caused by defects in the pentacene layer.

Finally, a pentacene TFT with the same channel length $L = 4\,\mu\mathrm{m}$ and a narrower channel width $W = 20\,\mu\mathrm{m}$ was characterized. This device showed a linear regime but saturation did not occur above a gate voltage of $V_G = -40\,\mathrm{V}$. Nevertheless, transfer characteristics have transistor-like behavior. The extracted apparent mobility μ was $0.8 \cdot 10^{-2}\,\mathrm{cm^2/Vs}$ and the extrapolated threshold voltage V_T was $-2.5\,\mathrm{V}$, respectively.

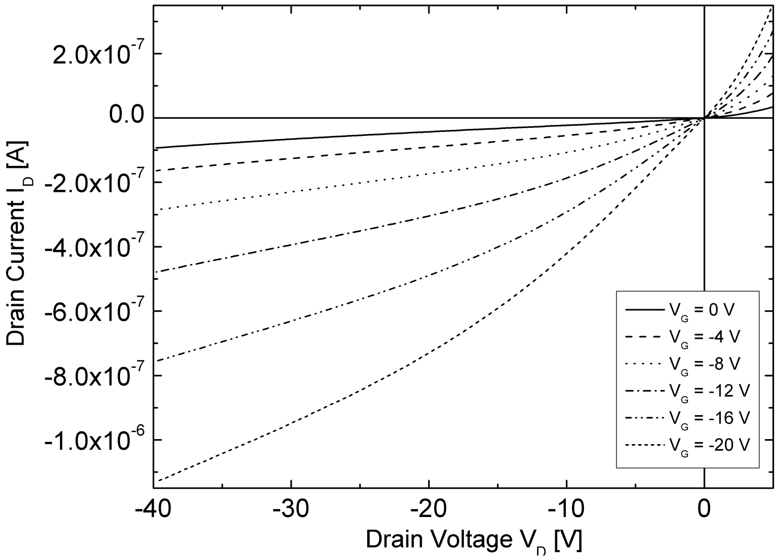
Low-field mobilities μ, transconductances g_m, I_{on}/I_{off} ratios and extrapolated threshold voltages V_T from the presented pentacene TFTs transfer characteristics are summarized in Table 4.2.

	on wafer	peeled off	peeled off	peeled off	peeled off
Channel length (µm)	10	10	10	4	4
Channel width (µm)	20	20	3	50	20
Apparent mobility μ ($\mathrm{cm^2/Vs}$)	$5.6 \cdot 10^{-2}$	$5.3 \cdot 10^{-2}$	$3.3 \cdot 10^{-2}$	$3.9 \cdot 10^{-2}$	$0.8 \cdot 10^{-2}$
Transconductance g_m (S)	$6.4 \cdot 10^{-9}$	$5.8 \cdot 10^{-9}$	$0.2 \cdot 10^{-9}$	$4.3 \cdot 10^{-9}$	$0.4 \cdot 10^{-9}$
I_{on}/I_{off}	$\sim 10^4$	$\sim 10^4$	$\sim 7 \cdot 10^3$	$\sim 10^3$	$\sim 4 \cdot 10^2$
Extrapolated V_T (V)	-3.8	-3.8	-3.2	-3.0	-2.5

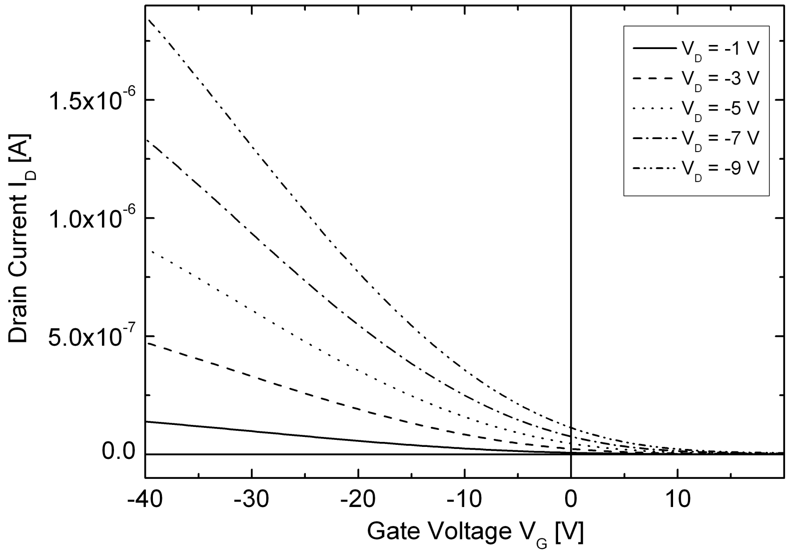
Table 4.2: Summarized physical parameters extracted from pentacene TFTs transfer characteristics.

4.3.3 Discussion

Applying full-wafer stencil lithography, working pentacene TFT on flexible PI substrates with channel lengths down to $3\,\mu\mathrm{m}$ and locally patterned gate contacts were obtained. While classical TFT designs consider channel dimensions with $L < W$,



(a) I_D–V_D output characteristics



(b) I_D–V_G transfer characteristics

Figure 4.18: Electrical characteristics of a pentacene TFT of 4 µm channel length and 50 µm channel width after peeling the PI substrate off the Si wafer.

in the previously described experiments, channel dimensions of $L > W$ have also been included to explore the possibilities of stencil lithography. The fabrication of S/D for short but wide channels ($L < W$) poses stability issues for the SiN bridge between the stencil apertures. Therefore, longer but narrower channel dimensions have a higher chance of survival for stencil membranes. Inspections at the end of the stencil fabrication process have shown that the SiN bridges between S/D for channel lengths of 1 µm did not withstand the processing. However, membranes with apertures for longer channels were stable enough and survived all processing. Electrical characterization of TFTs with channels shorter than 3 µm but intact bridges often showed leakage between S/D contacts. The electrical connection between the S/D contacts was a result of the enlargement of the transferred stencil apertures to the substrate, known as blurring [85].

The alignment accuracy of a full-wafer stencil to a substrate is limited by several issues. First, the curvatures of the stencil and the substrate are different. Every step of the process flow changes the internal stress of the wafers and modifies their curvature. Therefore, the lateral positions of the patterned structures in the stencil and the substrate deviated slightly from the design. Second, the alignment of a stencil with respect to the substrate was limited by the 2 µm accuracy of the customized MA/BA6 SUSS MicroTec machine. These constraints resulted in a non-uniform alignment over the full-wafer substrate. Although a good alignment could be obtained locally, asymmetric alignment of pentacene and S/D contacts was observed at other locations on the same wafer.

Threshold voltages V_T change in the previously described experiments for the different channel widths and lengths. The threshold voltage V_T increases towards positive values with decreasing channel lengths. This behavior is similar to short-channel effects in Si MOSFET devices. This is based on a drain-induced barrier lowering (DIBL), where a lower gate voltage is required to create a channel [97]. DIBL-like behavior of pentacene TFT has been reported for a channel width of 100 µm and channel lengths between 5 µm and 50 µm [98]. The presented work showed this phenomenon occurs also for channels as narrow as 20 µm.

4.3.4 Conclusion

A successful fabrication of organic transistors using a 12 µm thin flexible substrate, a 230 nm thick PI dielectric, locally patterned pentacene and S/D top contacts by aligned full-wafer stencil lithography was obtained. However, improvements are needed as the electrical TFT performance was dependent on the location on the wafer. Transistors with channel lengths from 3 µm to 20 µm showed typical transistor-like behavior. Though, when scaling channel lengths below 5 µm some TFT characteristics became noisy. The pentacene TFTs on the flexible PI substrate maintain their functionality after being peeled off from the rigid Si wafer. The apparent mobility μ of pentacene TFTs on flexible substrates was lower compared to fabricated pentacene TFTs with Si as a back gate. The maximum extracted apparent mobility μ of pentacene TFTs is $5.3 \cdot 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$, and the minimum threshold voltage V_T $-2.5\,\mathrm{V}$, respectively.

4.4 Pentacene TFTs on a Flexible Substrate Exposed to Tensile Strain

The previous section 4.3 focused on the fabrication of pentacene TFTs on flexible substrates and their electrical performance after peeling the PI substrate off the rigid Si wafer. This section concentrates on the yield of working pentacene TFTs patterned on flexible PI substrates and on the uniformity of the apparent mobility across the wafer. A study of the pentacene degradation over time is included for TFTs attached to the rigid Si wafer. In addition the reliability of pentacene TFTs is observed under mechanical load. Controlled tensile strain is applied to the flexible PI substrate for single stretching and cycling experiments.

4.4.1 Pentacene TFT Fabrication for Tensile Stress Experiments

Pentacene TFTs were fabricated following the process flow as described in section 4.3.1. Few modifications in the process flow were made to optimize the performance of the pentacene TFTs. The TFT design was modified to guarantee a precise alignment of each component. Instead of 10 nm Ti and 100 nm Au, 10 nm Ti as adhesion layer and 50 nm platinum (Pt) as gate material was used. Pt has a lower surface roughness compared to Au, which is favorable for future pentacene deposition. The reduced gate thickness allows more homogeneous step coverage by the dielectric layer. The pentacene deposition was carried out in a pentacene dedicated evaporation chamber. The deposited pentacene thickness was slightly increased to ensure a continuous layer. The design and location of membrane apertures for S/D patterning were optimized to increase the membrane stability. Finally, the thickness of the S/D Au contacts was decreased to 80 nm.

4.4.2 Stretching Setup

Tensile Stress Tester TST350

The tensile stress tester TST350 of Linkam Scientific Instruments Ltd. was used to carry out the following experiments. A sample is mounted with clamps to movable jaws of the TST350. Tensile stress is applied to the sample by moving the jaws uniaxially apart (Figure 4.19). The motor coupled to the jaws applies a maximal force of (20 ± 0.1) N and moves the jaws between 1 µm/s and 1000 µm/s. The TST350 is software controlled. Jaw movement, time and applied force are available for readout.

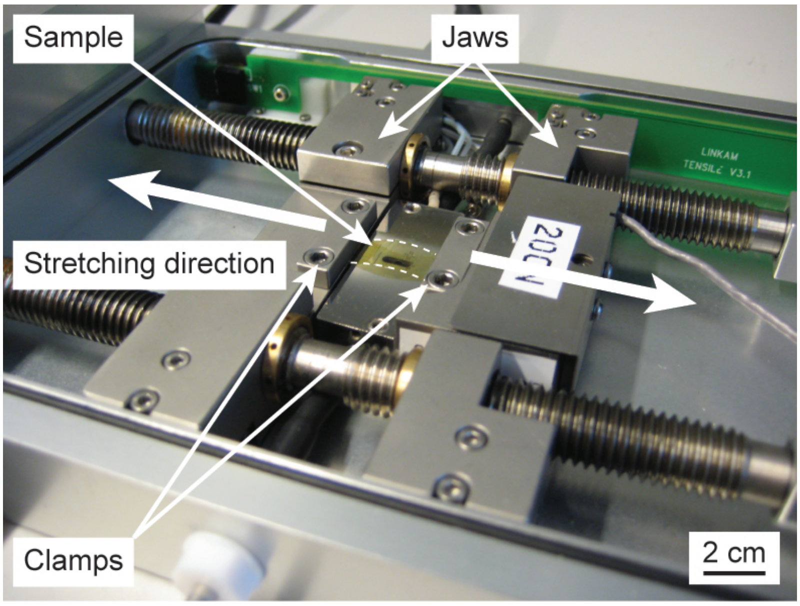
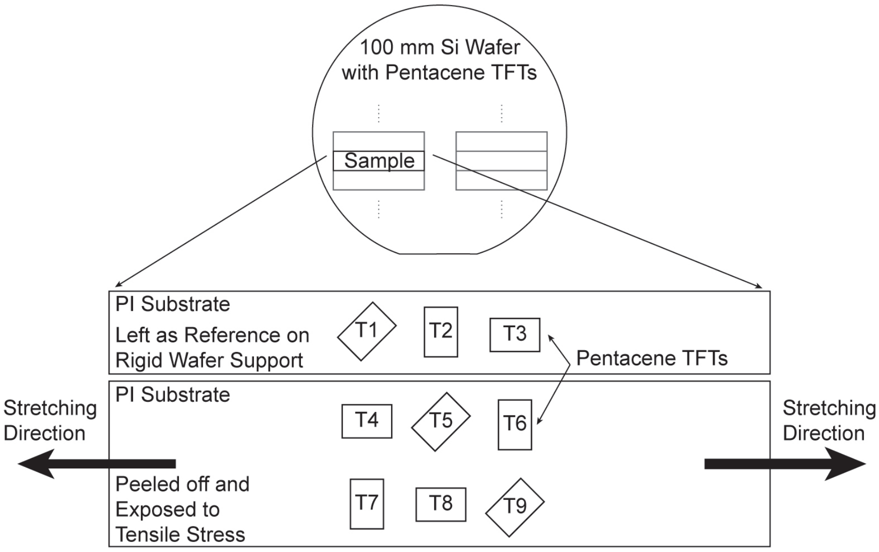


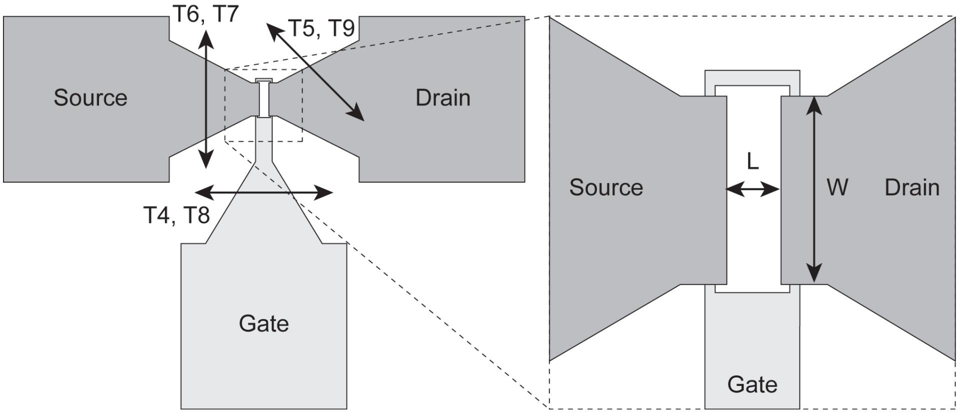
Figure 4.19: A sample is mounted on a tensile stress tester TST350 of Linkam Scientific Instruments Ltd. The sample is mounted by two clamps fixed to movable jaws. An uniaxial stress is applied by moving the jaws in the stretching direction. Note: Dashed lines identify the sample.

Sample and TFT Design for Tensile Strain Experiments

The sample design containing several pentacene TFTs was adapted in size for tensile stress experiments. Several samples were fabricated on full-wafer scale. A sample is approximately 28 mm × 7.5 mm large and includes nine identical pentacene TFTs with different orientations (Figure 4.20 a). The channel of a TFT is either 0°, 45° or 90° rotated with respect to the stretching direction (Figure 4.20 b). For tensile stress experiments six pentacene TFTs were peeled off the Si wafer and mounted to the TST350. Three pentacene TFTs were left as a reference on the Si wafer.



(a) Design of a sample for tensile stress experiments. Several samples are included on full-wafer scale. A sample includes nine TFTs including different orientations with respect to the stretching direction. Six TFTs (T4 - T9) were exposed to tensile stress whereas three TFTs (T1 - T3) stayed as reference on the rigid Si wafer.



(b) Design of a pentacene TFT. T4 to T9 show the corresponding stretching direction of each TFT. W and L indicate the channel width and the channel length of the pentacene TFT.

Figure 4.20: Sample and pentacene TFT design for tensile stress experiments.

Every sample contained a specific TFT channel design. Two different ratios of channel width W to channel length L were considered. The ratio W/L was either set to 2 or 5. Channel lengths L were chosen between 2.5 µm and 20 µm (Figure 4.20 b).

4.4.3 Tensile and Electrical Characterization of Pentacene TFTs

Young's Modulus of PI Substrate

The Young's modulus E of the fabricated PI as a substrate was first characterized. A rectangular PI film was peeled off the Si wafer and mounted to the TST350. A linear increasing force was applied to the PI sample in order to stretch the sample uniaxially. The force was amplified until mechanical failure appeared. The Young's modulus E was extracted as the slope of the linear regime of stress σ vs. strain ϵ (Figure 4.21). A Young's modulus E of (7.1 ± 0.7) GPa was extracted. In comparison 8.5 GPa as Young's modulus is provided by HD MicroSystems™ for PI films made of PI2611 [99].

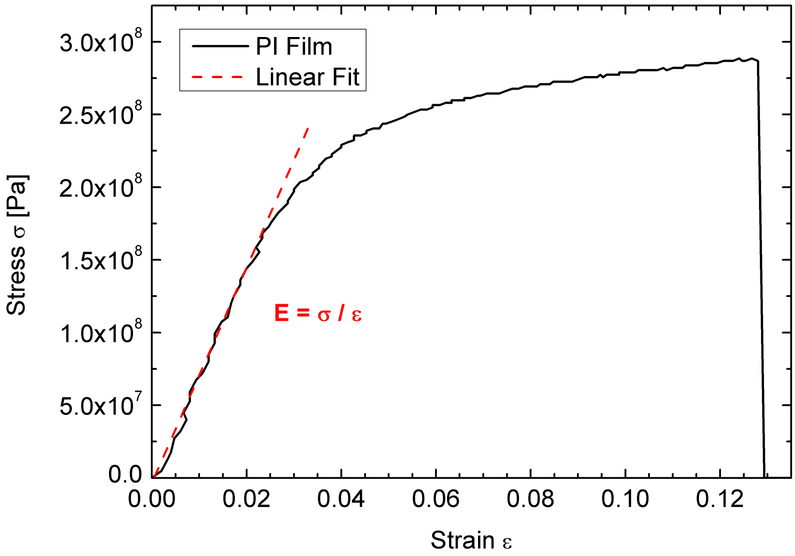


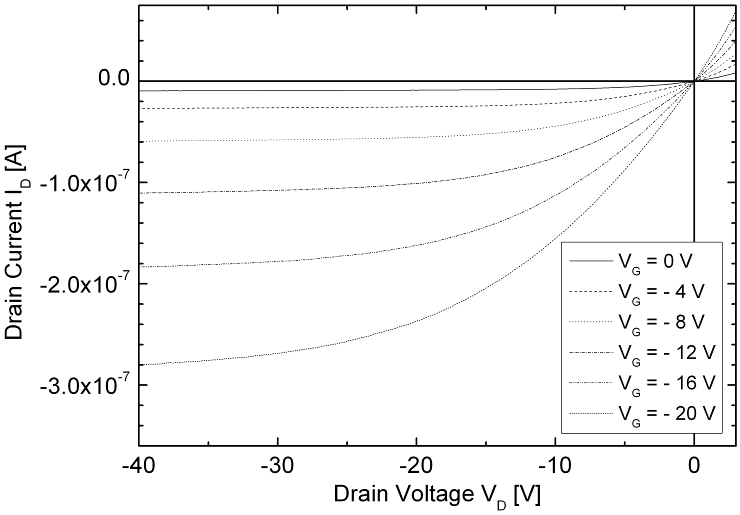
Figure 4.21: Stress σ vs. strain ϵ of a PI substrate. The Young's modulus E of (7.1 ± 0.7) GPa was extracted as the slope of the linear regime.

Pentacene TFTs before Peeling the PI Substrate of the Rigid Si Wafer

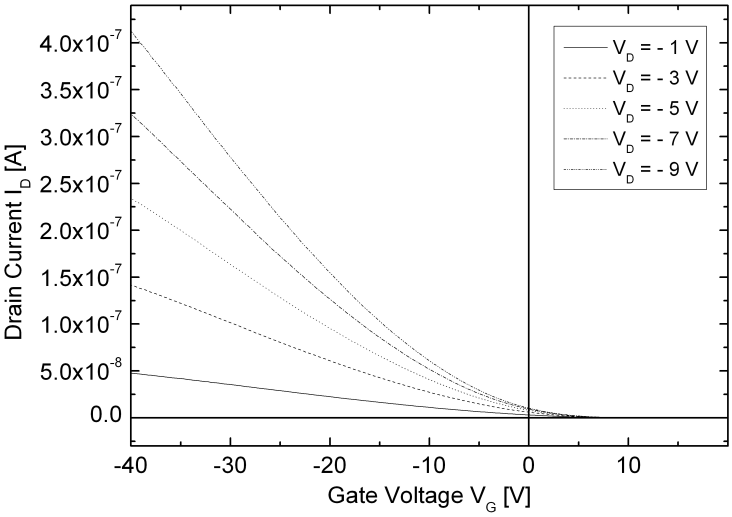
The pentacene TFTs of various channel dimensions were electrically characterized before peeling the PI samples off the rigid Si wafer. All measurements were taken using a probe station placed inside a Faraday cage and shielded from light. Transfer and output characteristics of 72 pentacene TFTs were taken and the apparent mobility μ was extracted. Output characteristics of working pentacene TFTs have a linear regime around zero drain voltage V_D and reach saturation at lower negative drain voltages V_D (Figure 4.22 a). Transfer characteristics show a linear regime at lower negative gate voltages V_G (Figure 4.22 b).

The yield of working pentacene TFTs on full-wafer scale was 91.5 %. Over full-wafer scale an average apparent mobility μ of $(5.0 \pm 0.7) \cdot 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$ was obtained. Few non-functional pentacene TFTs showed high leakage between S/D contacts and saturation did not occur. SEM inspections showed that the corresponding stencil membranes to pattern S/D contacts did not sustain the processing (Figure 4.23). These stencil membranes were broken and resulted in a patterned shortcut between S/D contacts.

A set of pentacene TFTs with different channel dimensions were left on the Si wafer to study the degradation of pentacene over time. Transfer and output characteristics were taken shortly after the completion of the sample fabrication and an initial average apparent mobility μ_0 of $(5.3 \pm 0.1) \cdot 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$ was extracted. The electrical characterization and the extraction of the mobility μ were repeated approximately every 52 days. Between the measurements the pentacene TFTs were stored in a static protected box shielded from light and kept at ambient conditions. 55 days, 102 days and 152 days after finishing the sample fabrication the relative apparent mobility μ/μ_0 of pentacene TFTs decreased to (76 ± 3) %, (64 ± 2) % and (61 ± 2) %, respectively (Figure 4.24). After 216 days the relative apparent mobility μ/μ_0 was further reduced to (53 ± 1) % of its initial value.



(a) I_D–V_D output characteristics.



(b) I_D–V_G transfer characteristics.

Figure 4.22: Electrical output and transfer characteristics of a pentacene TFT of 10 µm channel length and 20 µm channel width. The PI sample is attached to a rigid Si wafer.

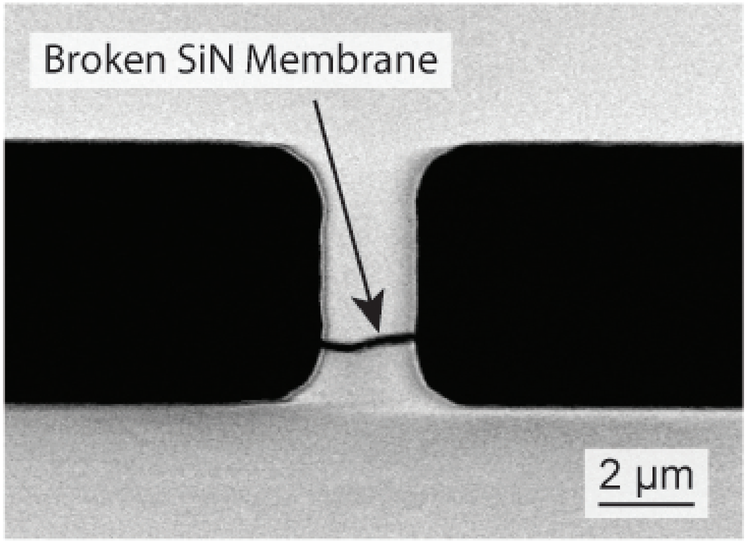


Figure 4.23: Broken low-stress SiN stencil membrane for patterning S/D contacts. The membrane design did not sustain the processing.

Pentacene TFTs Peeled off the Rigid Si Wafer

After characterizing the pentacene TFTs on the Si wafer electrically, the PI substrate was cut into the approximate sample size. Tweezers were used to manually peel the sample including pentacene TFTs off the Si wafer. The sample was then mounted to the TST350 and the pentacene TFTs were again characterized for controlling their functionality. Electrical characterizations on the TST350 were taken by mounting the TST350 on the probe station inside the light-shielding Faraday cage (Figure 4.25).

Transfer and output characteristics of pentacene TFTs with a 20 μm long and 40 μm wide channel were taken before and after peeling the sample off the Si wafer. After peeling off, the pentacene TFTs remained functional with output characteristics including a linear regime around zero drain voltage V_D and saturation at lower negative drain voltages V_D. The extracted initial apparent mobility μ_0 of pentacene TFTs attached to the Si wafer was $(4.7 \pm 0.1) \cdot 10^{-2}\,\mathrm{cm^2/Vs}$. After peeling the sample off the Si wafer and fixing to the TST350, the apparent mobility μ decreased to

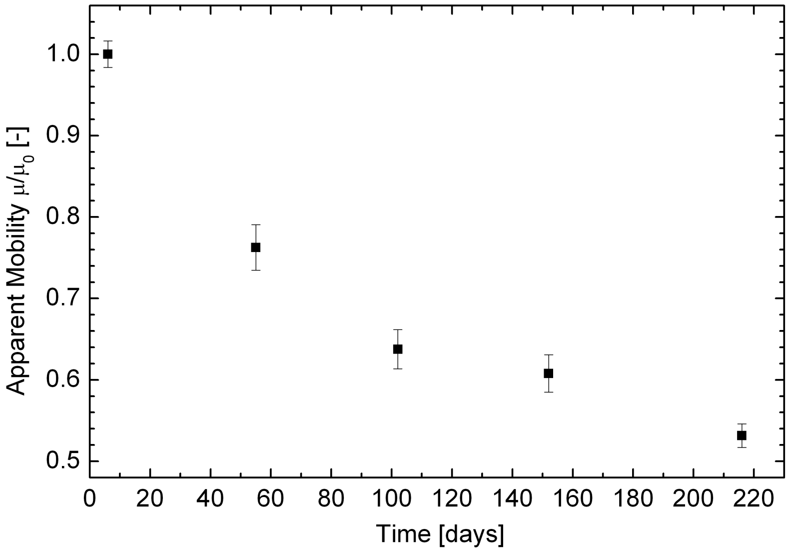


Figure 4.24: The performance of pentacene TFTs stored at ambient conditions decreases over time. After 216 days the relative apparent mobility μ/μ_0 decreased to (53 ± 1) % of its initial value.

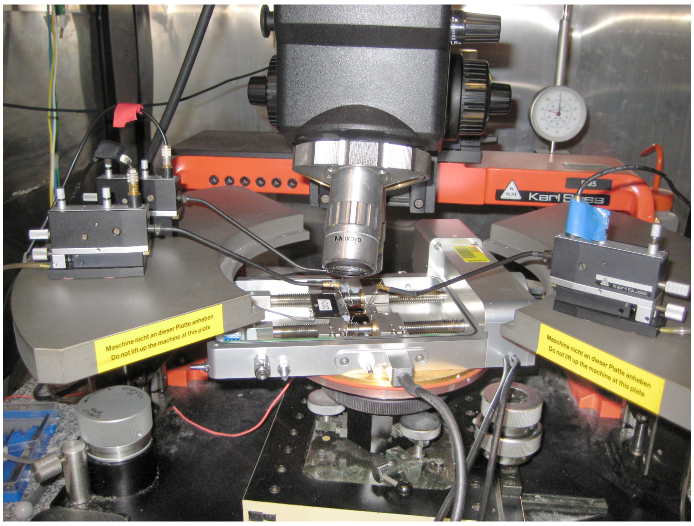
$(3.9 \pm 0.1) \cdot 10^{-2}\,\text{cm}^2/\text{Vs}$. This corresponds to a relative apparent mobility μ of (83 ± 4) % (Table 4.3). The electrical characterization did not show any dependence on the location or orientation of the pentacene TFTs.

Pentacene TFTs	Relative apparent mobility μ/μ_0 (%)	Apparent mobility μ (cm^2/Vs)
on wafer	100 ± 4	$(4.7 \pm 0.1) \cdot 10^{-2}$
peeled off	83 ± 4	$(3.9 \pm 0.1) \cdot 10^{-2}$

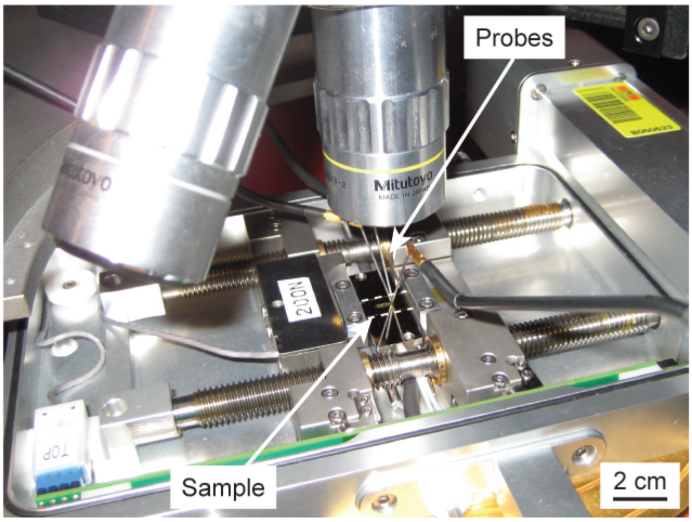
Table 4.3: Decreasing pentacene TFT performance after peeling the sample off the wafer.

Pentacene TFTs Under Step-by-Step Applied Strain

The sample as previously described including pentacene TFTs with 20 μm long and 40 μm wide channels was fixed to the TST350. A uniaxial strain ϵ was applied to the



(a) The TST350 was mounted on a probe station. The probe station was placed inside a light-shielding Faraday cage.



(b) Probes accessed the contact pads of the pentacene TFTs for electrical characterization while the sample was mounted to the TST350. Note: Dashed lines identify the sample.

Figure 4.25: Electrical characterizations of pentacene TFTs were taken while the sample was fixed to the TST350.

PI substrate and the electrical characterization was taken. The strain ϵ was increased step-by-step and the change of the apparent mobility μ was monitored with respect to the initial measurement on the TST350 (Figure 4.26). First, 0.6 % strain ϵ was applied but did not affect the performance largely. The relative apparent mobility μ/μ_0 changed slightly to (97 ± 4) % of its initial value on the TST350. A raise of the applied strain ϵ to 1.3 % decreased the relative apparent mobility μ/μ_0 to (87 ± 3) %. A further increase of the applied strain ϵ to 2 % reduced the relative apparent mobility μ/μ_0 to (82 ± 3) %. The maximal applied strain ϵ of 2.6 % reduced the relative apparent mobility μ/μ_0 to (71 ± 3) %. Releasing the applied strain ϵ to 1.3 %, the relative apparent mobility μ/μ_0 partially recovered to (74 ± 3) % of its initial value. The pentacene TFTs remained functional after the total release of the applied strain ϵ (Figure 4.27). The relative apparent mobility μ/μ_0 recovered to (81 ± 4) %. The change of the apparent mobility μ occurred independent to the TFT location and orientation.

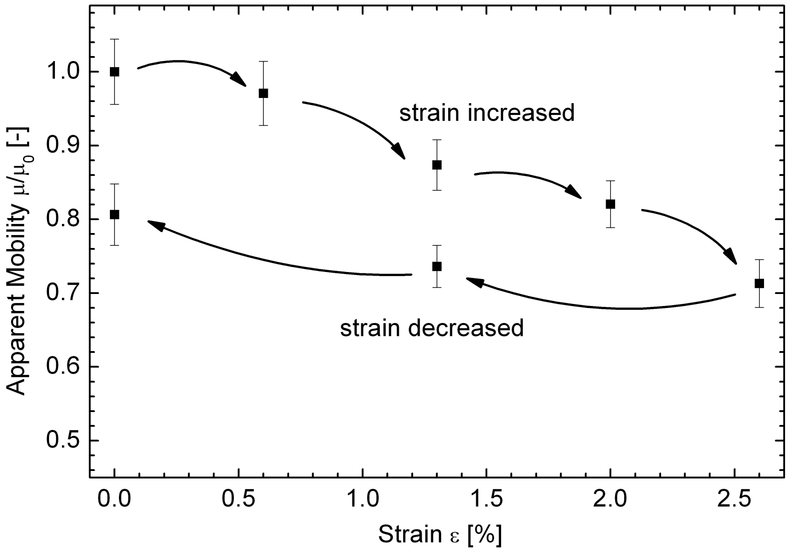
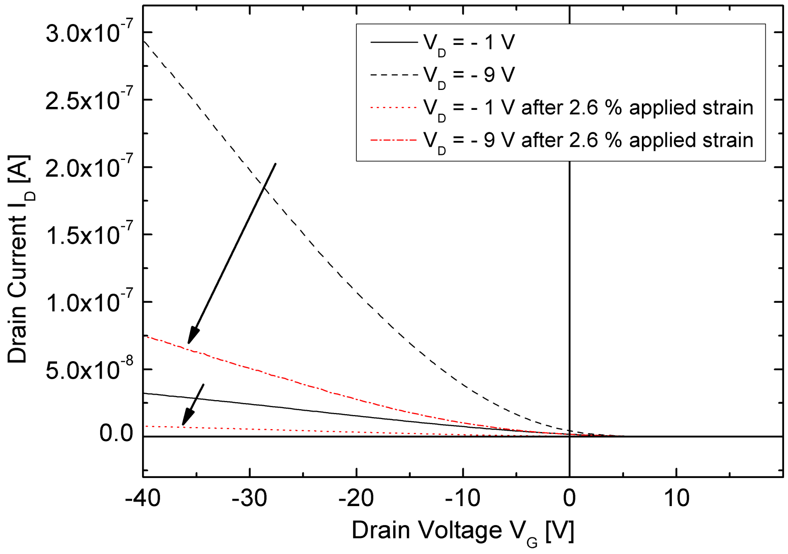
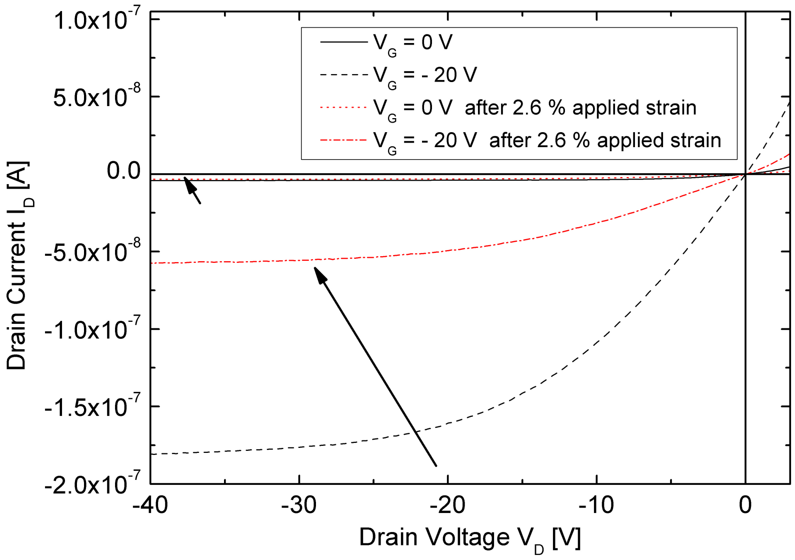


Figure 4.26: Pentacene TFTs with a 20 µm long and 40 µm wide channel were exposed step-by-step to uniaxial strain ϵ. The relative apparent mobility μ/μ_0 decreased to (71 ± 3) % of its initial value while 2.6 % strain was applied. After the release of the applied strain ϵ, the relative apparent mobility μ/μ_0 recovered to (81 ± 4) %.



(a) I_D–V_D output characteristics.



(b) I_D–V_G transfer characteristics.

Figure 4.27: Electrical output and transfer characteristics of a pentacene TFT before and after applying 2.6 % strain. The pentacene channel is 20 µm long and 40 µm wide.

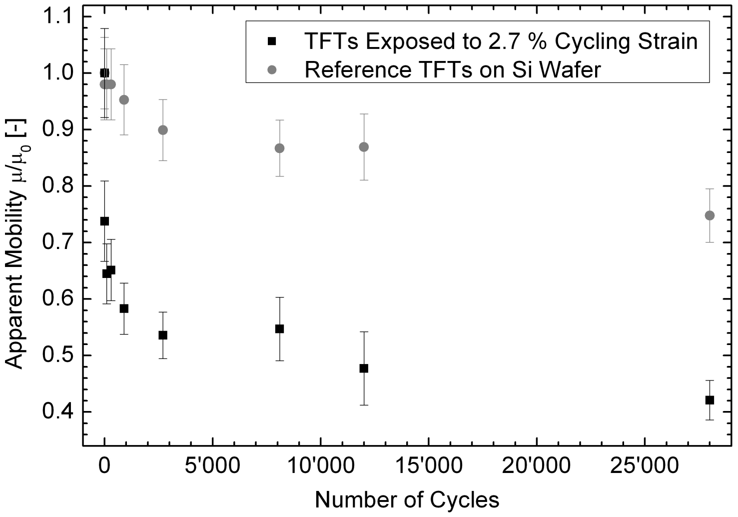
Pentacene TFTs Under Cycling Strain

A sample including pentacene TFTs with a 10 µm long and 20 µm wide channel was fixed to the TST350. Independently, three pentacene TFTs with identical channel dimensions were left on the Si wafer for reference (Figure 4.20 a). Transfer and output characteristics were taken and the apparent mobility μ was extracted. A strain ϵ of 2.7 % was applied to the PI substrate by moving the jaws at a speed of 40 µm/s. The strain ϵ was subsequently released. The PI substrate was exposed to several cycles of increasing and decreasing strain ϵ up to 2.7 %. After a defined number of cycles the electrical characteristics were taken and the change of the relative apparent mobility μ/μ_0 was monitored (Figure 4.28 a). The relative apparent mobility μ/μ_0 decreased within the first 1000 cycles significantly down to (58 ± 4) % of its initial value. Further experiments up to 28'000 cycles of 2.7 % applied strain ϵ reduced the relative apparent mobility μ/μ_0 down to (42 ± 3) % but every pentacene TFTs remained functional. The change in the apparent mobility μ did not have any dependence on the location and orientation of the pentacene TFT.

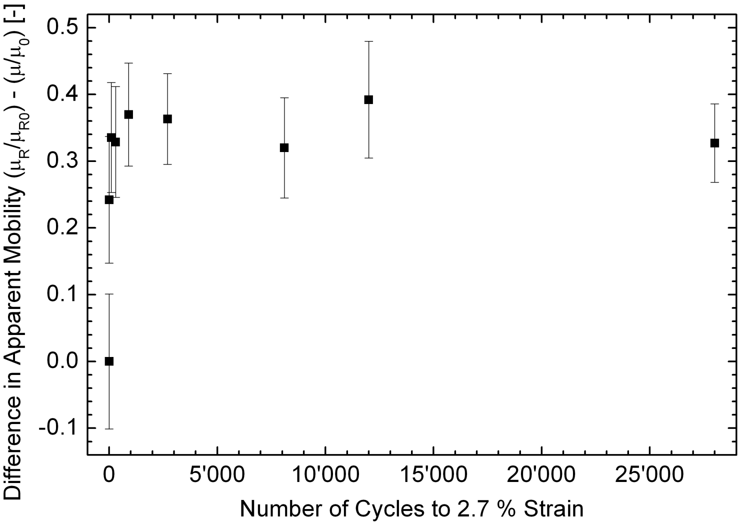
Parallel to the cycling experiments, the characterization of reference pentacene TFTs on the Si wafer were carried out to exclude the influence due to air and moisture. Within the time frame of the cycling strain experiments, the relative apparent mobility μ_R/μ_{R0} of the reference TFTs decreased to (75 ± 5) %. The difference in the relative apparent mobility $\mu_R/\mu_{R0}-\mu/\mu_0$ of the stretched TFTs and the reference TFTs was calculated to exclude the influence of air and moisture. After a few stretching cycles, the difference in the relative apparent mobility $\mu_R/\mu_{R0}-\mu/\mu_0$ increased significantly. Nevertheless, after roughly 1000 cycle the difference in the relative apparent mobility $\mu_R/\mu_{R0} - \mu/\mu_0$ stabilized at approximately 35 % (Figure 4.28 b).

4.4.4 Discussion

The optimized fabrication process of pentacene TFTs on full-wafer scale improved the yield of 72 TFTs to 91.5 %. In comparison to previous experiments (Section 4.3), the performance of pentacene TFTs was independent on the location of the



(a) Change of the relative apparent mobility μ/μ_0 due to cycling strain.



(b) Difference of the relative apparent mobility $\mu_R/\mu_{R0} - \mu/\mu_0$ between stretched and reference TFTs.

Figure 4.28: A sample including pentacene TFTs with a 10 μm long and 20 μm wide channel was exposed to cycling uniaxial strain. The strain went up to 2.7 % and released subsequently.

wafer. The semi-conducting quality of pentacene patterned by stencil lithography did not show any dependence on the size of the patterned area. Pentacene TFTs of all channel dimensions showed uniform electrical characteristics.

The electrical characterization of pentacene TFTs attached to a Si wafer has been repeated approximately every 50 days. The pentacene TFTs were stored in a light shielding box at ambient conditions between the measurements. During each electrical characterization a decrease of the apparent mobility μ was observed. It has been widely reported that the performance of pentacene TFTs critically depends on the environmental storage conditions [100–104]. Exposure to moisture and air are responsible for the degradation of pentacene based TFTs. Oxygen and water molecules diffuse into the pentacene layer and cause defects that changes its electrical performance.

After fabrication pentacene TFTs were successfully peeled off the rigid Si wafer. A decrease of the pentacene TFTs performance has been monitored after detaching the sample. The relative apparent mobility μ/μ_0 was reduced to (83 $\pm$ 4) % of its initial value. The decrease of the apparent mobility μ was probably caused by the manual detachment of the sample. Peeling the sample off the Si wafer by the use of tweezers induced an uncontrolled strain to the pentacene film on the PI substrate. In addition, peeling the PI substrate off the Si wafer can release due to fabrication eventually accumulated stress in the sample. It is assumed that the detachment of the sample formed microcracks in the pentacene film and reduced the performance of the TFTs.

Uniaxial stretching experiments reduced the relative apparent mobility μ/μ_0 to (71 $\pm$ 3) % when the applied strain ϵ was increased step-by-step up to 2.6 %. After releasing the applied strain ϵ the relative apparent mobility μ recovered partially to (81 $\pm$ 4) % of its initial value. The change of the apparent mobility μ was independent on the location and orientation of the pentacene TFT. Yet, uniaxial stretching experiments of pentacene based TFTs have not been published. But the phenomenon of reduced performance was observed while applying strain by bending the pentacene TFTs [3, 22, 23, 105, 106]. Pentacene TFTs on flexible polymer substrates were placed on the outside and inside of a cylindrical tube in order to apply tension or compression to the pentacene film. Sekitani *et al.* showed that an applied tensile strain of 2 % decreases the relative mobility to approximately 85 % of its initial value without applied strain. The reduction of the apparent mobility μ occurred with little dependence on the orientation of the pentacene TFT. The independence on the orientation was explained by the fact that the conducting path from source to drain electrode is formed by coupled pentacene grain chains oriented in random directions [3]. The results of Sekitani *et al.* agree very well with the data obtained within the described experiments where the relative apparent mobility μ/μ_0 decreased to (82 ± 3) % while a strain ϵ of 2 % was applied.

Continuous cycling experiments where a strain ϵ of 2.7 % was applied to the pentacene TFTs have shown at the beginning a distinctive decrease of the apparent mobility μ. Reference pentacene TFTs without applied strain were characterized simultaneously to control the pentacene TFT degradation over time. After the first stretching cycle the performance of the pentacene TFT could not be reestablished. Sekitani *et al.* have published that the source-drain current with an applied compressive strain below 1.4 % was reversible [3]. Within the previously described experiments a tensile strain ϵ was applied, which was significantly higher. It is assumed that the applied tensile strain ϵ modified the pentacene film permanently as the apparent mobility μ could not be reestablished. Up to roughly 1000 cycles, the apparent mobility μ of the stretched sample decreased faster than the apparent mobility μ of the reference sample. Above 1000 cycles the difference was approximately constant. This indicates that after a certain amount of cycles the degradation of the pentacene film due to air and moisture had a higher impact compared to the degradation due to the applied strain ϵ.

The decrease of the relative apparent mobility μ/μ_0 with respect to the carried out experiments are summarized in Table 4.4.

Pentacene TFTs on a PI substrate	Relative apparent mobility μ/μ_0 (%)
216 days after fabrication	53 ± 1
after peeling off the Si wafer	83 ± 4
exposed 2.6 % strain	71 ± 3
after 28'000 cycles to 2.7 % applied strain	42 ± 3

Table 4.4: The decrease of the relative apparent mobility μ/μ_0 with respect to the different experiments.

4.4.5 Conclusion

The fabrication of pentacene TFTs on flexible substrates was successfully improved. In particular, a better alignment of full-wafer stencils and a more stable pentacene deposition increased the yield of working devices. The electrical characterization of 72 pentacene TFTs fabricated on full-wafer scale resulted in a yield of 91.5 %. TFTs with channel lengths from 2.5 µm to 20 µm showed output and transfer characteristics with linear and saturation regimes. The average apparent mobility μ was $(5.0 \pm 0.7) \cdot 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$.

Pentacene TFTs on flexible PI substrates are sensitive to air, moisture and mechanical load. Over time, the electrical performance of the pentacene TFTs decreased due to exposure to air and moisture. 216 days after fabrication, the relative apparent μ/μ_0 was reduced to (53 ± 1) %. The mechanical release of the PI substrate from the rigid Si wafer influenced the functionality of the devices. After peeling off, the pentacene TFTs remained functional but the relative apparent mobility μ/μ_0 was reduced to (83 ± 4) %. Step-by-step applied strain to the PI substrate including the pentacene TFTs also affected the electrical performance. The apparent mobility μ was reduced under the applied strain. The devices maintain their functionality and the apparent mobility μ recovered partially after releasing the applied strain. Cycling strain applied to the PI substrate reduced the apparent mobility μ distinctively within the first 1000 cycles compared to the reference TFTs. Further stretching cycles decreased the performance of stretched pentacene TFTs similar as the reference TFTs. It is assumed that the exposure to air and moisture had a higher impact than the applied strain.

In conclusion, two mechanical manipulations had a high impact on the performance of the pentacene TFTs. The apparent mobility μ was primarily influenced by peeling the TFTs off the rigid Si wafer and the first cycles of applied strain. Peeling the sample off the rigid Si wafer and the first applied strain reduces the apparent mobility μ most. In addition, the degradation of the pentacene film due to air and moisture had a serious effect on the performance of the pentacene TFTs. Nevertheless, after all manipulations the functionality of the pentacene TFTs was maintained.

4.5 Conclusion on Pentacene TFTs

Pentacene TFTs on flexible substrates were obtained within three steps and investigated systematically. First, an initial study on pentacene TFTs with a rigid Si back gate, PI or SiO_2 dielectric layers and Au top contacts was carried out. S/D contacts for channels down to 5 µm were patterned by chip-size stencil lithography. The pentacene TFTs with PI as the dielectric material presented similar performances compared to TFTs with SiO_2 as the dielectric material. The electrical characterization showed that PI is a suitable candidate for pentacene TFTs in comparison with SiO_2. Thus, PI was used as the dielectric material within the next step to obtain pentacene TFTs on a flexible substrate. The fabrication of organic transistors using a 12 µm thin flexible substrate, a 230 nm thick PI dielectric, locally patterned pentacene and S/D top contacts by aligned full-wafer stencil lithography was successfully done. However, improvements are needed as the electrical TFT performance was dependent on the location on the wafer. Transistors with channel lengths down to 3 µm showed typical transistor-like behavior. Though, when scaling channel lengths below 5 µm some TFT characteristics became noisy. The pentacene TFT on the flexible PI substrate maintain their functionality after being peeled off from the rigid Si wafer. The fabrication of pentacene TFTs on flexible substrates was successfully improved. In particular, a better alignment of full-wafer stencils and a more stable pentacene deposition increased the yield of working devices. The electrical characterization of 72 pentacene TFTs fabricated on full-wafer scale resulted in a yield of 91.5 %. TFTs with channel lengths from 2.5 µm to 20 µm showed typical output and transfer characteristics with linear and saturation regimes. The average apparent mobility μ was $(5.0 \pm 0.7) \cdot 10^{-2}\,\mathrm{cm^2/Vs}$. Pentacene TFTs on flexible PI substrates were sensitive to air, moisture and mechanical load. Exposure to air and moisture decreased the electrical performance of the pentacene TFTs over time. Mechanical load due to the release of the PI substrate from the rigid Si wafer influenced the functionality of the devices. After peeling off, the pentacene TFTs remained functional but the apparent mobility μ was reduced. Step-by-step applied strain to the PI substrate including the pentacene TFTs also affected the electrical performance. The apparent mobility μ was reduced under the applied strain.

The devices maintained their functionality and the apparent mobility μ recovered partially after releasing the applied strain. Cycling strain applied to the PI substrate reduced the apparent mobility μ distinctively within the first 1000 cycles compared to the reference TFTs. Further stretching cycles decreased the performance of stretched pentacene TFTs similar as the reference TFTs. It is assumed that the exposure to air and moisture had a higher impact than the applied strain.

In conclusion, pentacene TFTs on rigid and flexible substrates were successfully fabricated. Continuous improvement of aligned stencil lithography increased the yield of pentacene TFTs on flexible PI substrates. The electrical characterization has shown how air, moisture and mechanical load degraded the pentacene film and reduced the TFT performance. However, the functionality of the pentacene TFTs was maintained. Three experiments had a significantly high impact on the performance. The apparent mobility μ was primarily influenced by the exposure to ambient conditions, peeling the TFTs off the rigid Si wafer and the first cycles of applied strain.

5 Compliant Stencil Lithography

This chapter presents the fabrication and characterization of freestanding membranes for compliant stencil lithography. The working principle is explained and FEM simulations were carried out on the vertical displacement of compliant membranes. The fabrication process of a compliant stencil is shown and statistics on the pattern transfer were taken.

5.1 Principle of Compliant Stencil Lithography

The blurring in stencil lithography is the loss of resolution due to the pattern transfer (cf. Section 1.4). This is mainly caused by the gap g between the stencil membrane and the substrate surface. The origin of the gap g has several reasons such as the non-planarity of the substrate or different curvatures of the stencil and substrate. The deposited structures are, compared to the membrane aperture diameter d_A, enlarged due to a geometrical blurring b_G and a blurring due to a halo b_H (Figure 5.2 a). The enlarged structure includes a central thick part d_C surrounded by a thin halo and has a total diameter d_T.

A reduction of the gap g between stencil membrane and substrate can be obtained by the application of a chip-size stencil. The curvature of a chip-size stencil has less influence on the gap due to the outer dimensions of the stencil. On the contrary, full-wafer stencil lithography allows a large-area patterning and the alignment of the stencil to the substrate. A solution is proposed to minimize the gap between stencil membrane and substrate on 100 mm full-wafer scale. Compliant low-stress SiN stencil membranes are mechanically decoupled from the rigid Si frame by means of four protruding low-stress SiN cantilevers, which support the free standing sten-

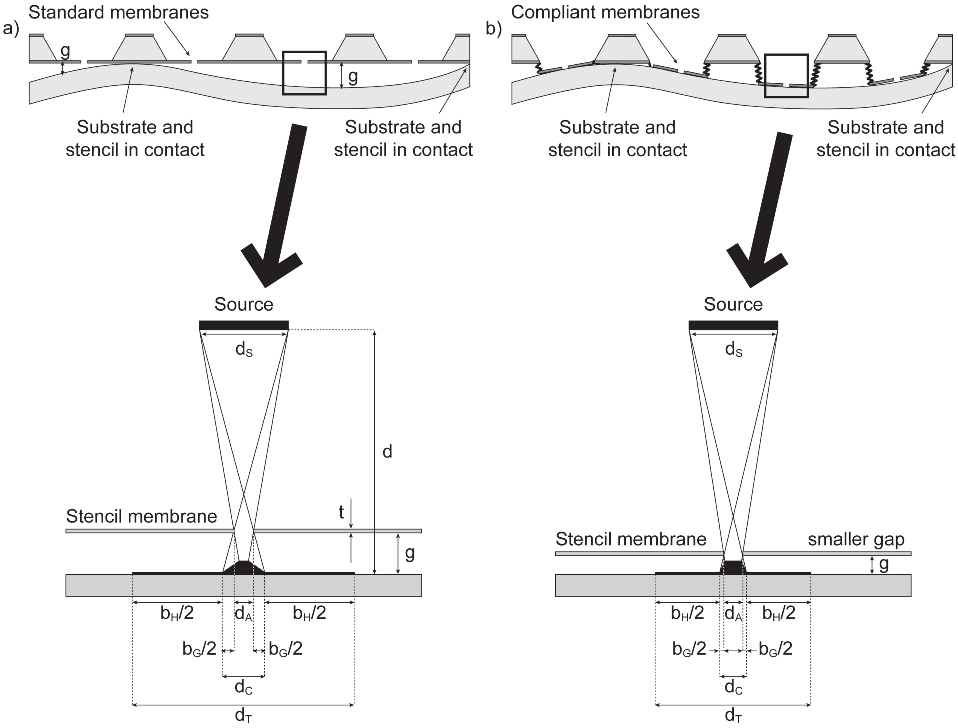


Figure 5.1: Structures deposited by stencil lithography are, compared to the membrane aperture diameter d_A, enlarged due to a geometrical blurring b_G and a blurring due to a halo b_H. The enlarged structure includes a central thick part d_C, a thin halo around and has a total diameter d_T. The blurring is determined by the stencil and substrate curvature, which results in a gap g. a) In a standard stencil configuration the gap g strongly depends on the location of the wafer. The gap g is several micrometers up to tens of micrometers big. b) In a compliant stencil configuration, mechanically uncoupled membranes adapt to the substrates curvature. Therefore, the geometrical blurring and the blurring due to the halo are minimized.

cil membranes. Compliant membranes adjust independently and reduce locally the gap all over the wafer (Figure 5.2 b). Standard (i.e. non-compliant) and compliant membranes are included in the same full-wafer stencil and used to pattern submicrometer Al structures on a Si wafer. The geometrical blurring and the halo of the deposited Al structures are analyzed.

5.2 FEM Simulation on the Displacement of a Compliant Membrane

Previous studies indicated that the gap between two 100 mm full-wafers typically ranges up to 40 µm [75]. In order to overcome this distance, the chosen approach includes the fabrication of protruding low-stress SiN membranes connected to a rigid Si frame by 4 non-planar low-stress SiN cantilevers (Figure 5.2). This geometry is preferred due to the simplicity of the fabrication process and to its mechanically linear behavior, as shown by FEM.

Two sets of FEM simulations were carried out on 500 nm thin low-stress SiN structures, using Ansys® 11.0. First, a parametric study was performed changing the width of the membrane-supporting cantilevers. The membranes were 1000 µm × 1000 µm large and supported by four protruding low-stress SiN cantilevers. The four cantilevers were 192 µm long and either 800 µm or 200 µm wide. A linear increasing load was applied to the frontside of the membrane surface. The membrane deflection and deformation was simultaneously monitored. An applied load on compliant membranes supported by 800 µm wide cantilevers had a high impact on the planarity of the membrane. The membrane appeared buckled as the membrane center deflected significantly more than the borders. A membrane supported by 200 µm wide cantilevers gave a more planar response and deflected 40 µm under the applied load.

The second parametric study was performed changing the length of the cantilevers supporting the membranes. The chosen cantilever width was 200 µm as the previous study showed good performance. The cantilever length ranged from 250 µm to 150 µm. Again, a linear increasing load was applied to the frontside of the compliant membrane until a 40 µm deflection was observed (Figure 5.3). Depending on the length of the supporting cantilevers, the necessary applied force ranged from 25 µN to 72 µN. The applied force resulted in an elastic constant of a compliant membrane configuration of 0.6 N/m to 1.6 N/m. Scaling a single membrane configuration up to a full-wafer stencil with 400 compliant membranes, a total force of 30 mN is suf-

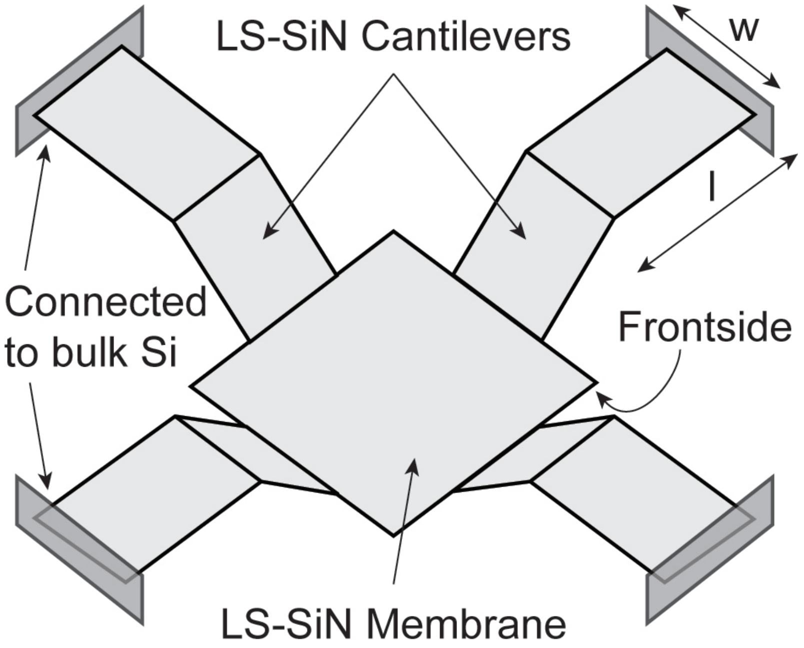


Figure 5.2: Schematic illustration of a compliant low-stress SiN membrane with four non-planar low-stress SiN cantilevers.

ficient to deflect all membranes by 40 µm or, in other words, minimizing gaps for all membranes.

In conclusion of the performed simulations, the maximal induced stress due to the applied load on the compliant membranes was below the yield of strength of low-stress SiN, i.e. compliant membranes deflected sufficiently without damaging the structure. Membranes supported with 200 µm wide cantilevers were chosen as the deflection has a more planar response. Simulations on different cantilever lengths did not conclude in a preferred geometry. Therefore, 150 µm, 200 µm and 250 µm long cantilevers were included in the design. A soft clamping mechanism of stencil and substrate is sufficient as an applied total force of a few mN deflects all compliant membranes on full-wafer scale. A low applied force also prevents a bending of substrate or stencil wafer.

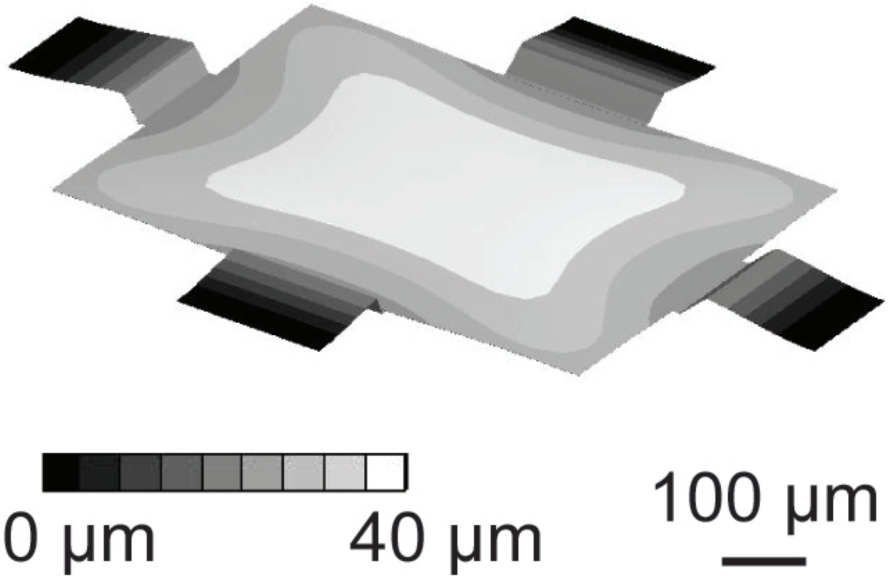


Figure 5.3: Result from a finite element method (FEM) simulation showing that a square membrane supported by four 200 µm long and 500 nm thick cantilevers deflects 40 µm under a load of 45 µN. Note that a 40 µm deflection was chosen because experimental evidences have shown this to be a typical maximum value for the gap.

5.3 Fabrication Process

Standard and compliant membranes were fabricated on the same stencil. Standard membranes were used as a reference and located between compliant membranes. The fabrication of standard and compliant membranes started with a 100 mm Si wafer (Figure 5.4 a). The Si wafer was coated with 200 nm SiN by LPCVD. Squares of SiN were left on the wafer after UV photolithography and subsequent dry etching. The wafer was exposed to KOH to define 40 µm high mesa structures (Figure 5.4 b). The SiN mask was removed by hydrofluoric acid (HF) etching and a 500 nm thick low-stress SiN film was deposited by LPCVD (Figure 5.4 c). Backside openings of the compliant membranes for the final etching in KOH were then defined by photolithography and dry etching (Figure 5.4 d). An optimized lithography on the frontside with its 40 µm high mesa structures was performed with a 14 µm thick resist layer. The patterned resist outlines membrane supporting cantilevers on the KOH slope and membrane apertures in micrometer size. Within the same UV lithography, apertures of compliant membranes were defined on top of the mesas and apertures of standard, non-compliant membranes between the mesas. Dry etching followed the photolithography to transfer the pattern into the SiN (Figure 5.4 e). Due to the mesa structures the resist thickness was not constant all over the wafer, which resulted in a different resolution of membrane apertures on top and between the mesa structures. Finally, a backside etching in KOH released the membranes from the bulk Si (Figure 5.4 f, Figure 5.5 a and Figure 5.5 b). After releasing, arrays of dot shaped nanoapertures were defined on compliant and non-compliant membranes by focused ion beam milling (FIB) (5.4 g, Figure 5.5 c). Overall, 22 compliant membranes and 11 standard membranes as reference were FIB patterned across a full-wafer stencil (Figure 5.5 d). Nominal diameters of the nanoapertures on each membrane are 200 nm, 300 nm, 400 nm and 500 nm respectively.

5.4 Setup for Compliant Stencil Lithography

The full-wafer stencil with both standard and compliant membranes was approached to a 100 mm Si wafer. The approach of the stencil to the substrate is a critical step when there are compliant membranes out of plane compared to the bulk Si support. A manual approach might induce shear stress between the compliant membranes and the substrate. The shear stress together with evaporation-caused heating may release at any time during evaporation. An uncontrolled shear stress release results in a significant distortion of the transferred patterns. Thus, a MA/BA6 SUSS MicroTec tool, optimized for stencil alignment, was used to approach the compliant membranes vertically and apply mechanical clamping of stencil and substrate.

The stencil-substrate configuration was placed under an optical white light microscope. The 500 nm thin low-stress SiN membranes are transparent to white light and a quantitative estimation of the gap between membrane and substrate was possible. By changing the focus from the micrometric apertures in the standard membranes to the substrate, the size of the gap was evaluated. Over full-wafer scale a gap of more than 20 µm was observed between standard membranes and substrate. On

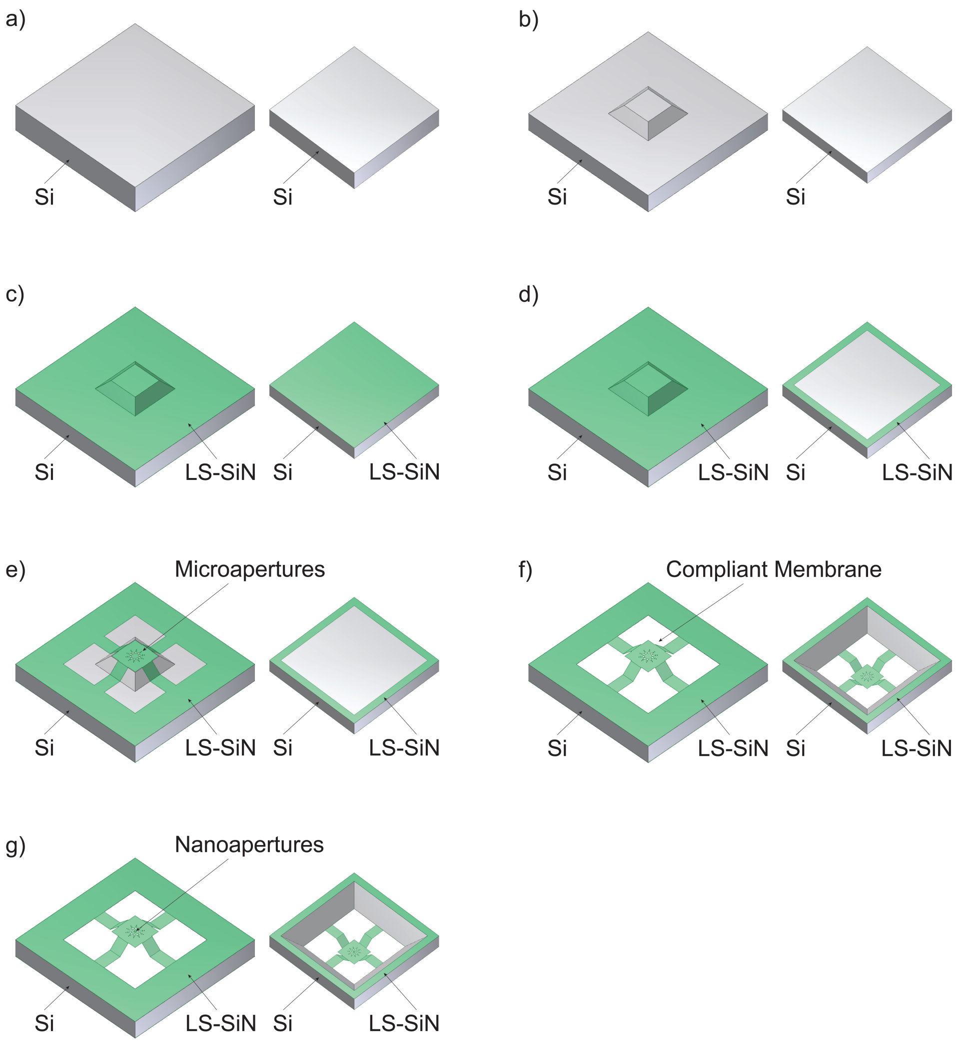


Figure 5.4: Schematic frontside view (left) and backside view (right) of the process flow for a compliant stencil membrane. a) The process started with a 100 mm Si wafer. b) 40 µm high mesa structures were etched by KOH using SiN as a mask. c) The Si wafer was coated by low-stress SiN. d) Backside openings were defined by UV lithography and dry etching chemistry. e) Non-planar SiN beams and microapertures were patterned by UV lithography. f) Compliant membranes were released by KOH etching. g) Finally, nanoapertures were defined by focused ion beam (FIB).

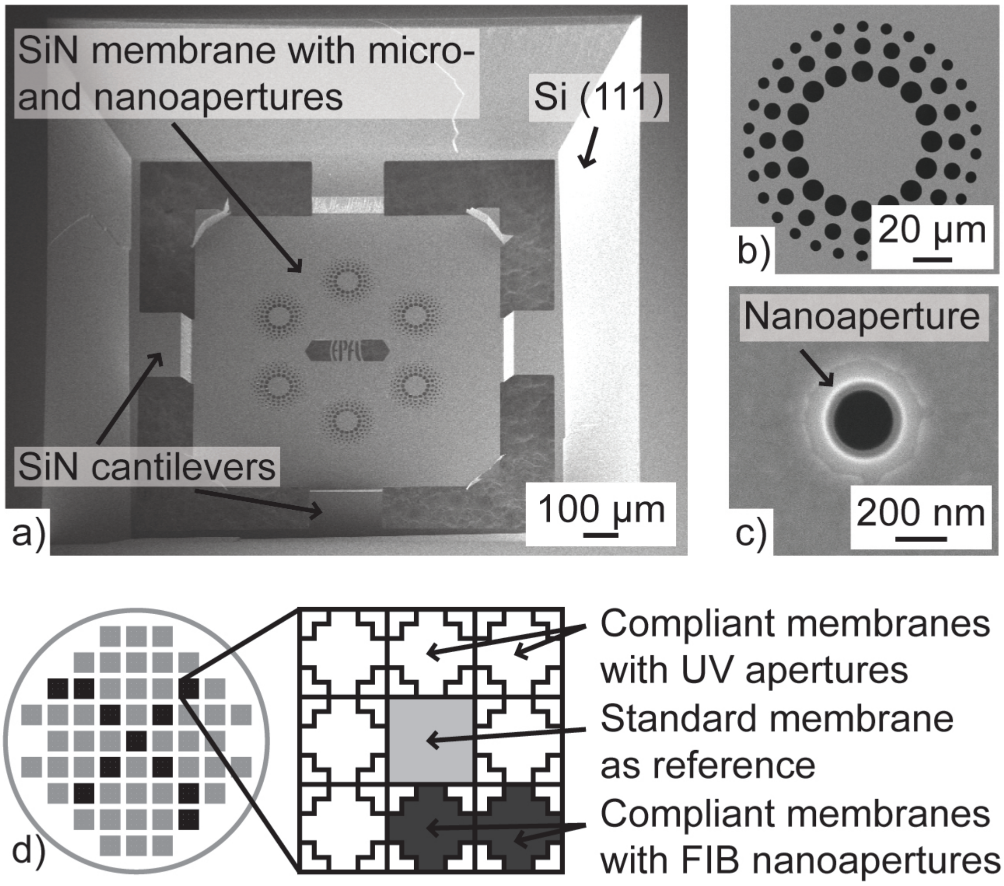


Figure 5.5: a) SEM illustration of a compliant stencil membrane shows the backside of a membrane with micro- and nanoapertures. The freestanding low-stress SiN membrane is decoupled from a rigid Si frame by four low-stress SiN cantilevers. b) SEM illustration of membrane apertures defined by UV lithography on a low-stress SiN membrane. Note that these micrometer apertures were defined between 40 µm high mesa structures. c) SEM illustration of a nanoaperture in a low-stress SiN membrane. The aperture was defined using FIB. d) Schematic illustration of nanoapertures arrangement across a full-wafer stencil. The design contains 22 compliant membranes and 11 standard (i.e. non-compliant), non compliant membranes with nanoapertures patterned by FIB.

the contrary, compliant membranes and substrate appeared simultaneously in focus. Interference fringes were observed in all compliant membranes approached to the Si substrate (Figure 5.6 a). The interference fringes point out that the compliant membranes were closer than 2 µm to the substrate [107]. The performance of the compliant membranes configuration was also inspected by SEM. The flexible cantilevers were deflected upwards while the membrane was touching the surface (Figure 5.6 b).

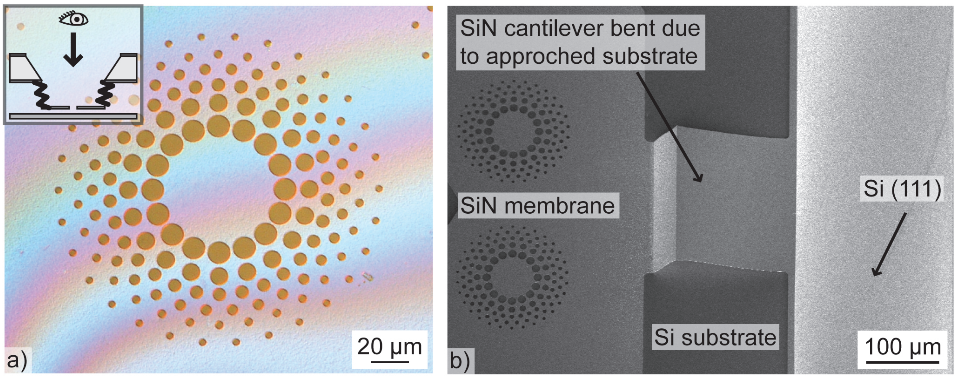


Figure 5.6: a) Optical illustration taken through a compliant SiN membrane placed on a Si substrate. Fringes appear where the membrane is closer than 2 µm to the substrate. Inset: Schematic illustration of the observation setup. b) SEM illustration of a deflected beam of a compliant stencil membrane in contact with a Si wafer. The beam bending is comparable to the FEM simulations in Figure 5.3.

The stencil-substrate configuration was mounted above the center of an Al source inside a vacuum chamber. The chamber was pumped down to a pressure of 10^{-6} mbar. A 50 nm thick Al film was deposited by e-beam evaporation through the stencil onto the Si wafer. The Al deposition rate was 4 Å/s. Subsequently, the stencil was removed from the substrate leaving the patterned Al on the Si wafer.

5.5 Characterization of the Resolution in Compliant Stencil Lithography

SEM inspections were used to characterize the geometrical blurring b_G and the blurring due to the halo b_H of Al structures deposited through both standard and compliant membranes. The diameter of the center part d_C and the diameter of the total structure d_T were measured to extract both blurring contributions of the deposited structure (Figure 5.2).

The geometrical blurring b_G is defined as the difference in diameter of the measured center part d_C and the measured stencil aperture d_A.

$$b_G = d_C - d_A \tag{5.1}$$

The blurring due to the halo b_H is defined as the difference of the measured total structure diameter d_T and the measured diameter of the center part d_C.

$$b_H = d_T - d_C \tag{5.2}$$

Thin Al layers onto a Si substrate show very low contrast. In order to characterize the total diameter d_T, the contrast was enhanced by performing a short and anisotropic dry etching of the Si. The high selectivity of Al to the etching chemistry ensures that the metal pattern was unaffected. After the Si etching the Al structures on the substrate presented distinctly a center part and a thin halo around (Figure 5.7).

Both blurring contributions of Al structures patterned by standard and compliant membranes were characterized separately. The geometrical blurring b_G did not show any dependence on the aperture diameter d_A for depositions through standard and compliant membranes (Figure 5.8). The geometrical blurring b_G due to standard membranes was (113 ± 34) nm. On the other hand, the geometrical blurring b_G caused by compliant membranes was distinctly smaller, (10 ± 10) nm, and approaches the limit imposed by the used measurement technique. In average, the geometrical blurring b_G due to compliant membranes was 95 % smaller compared to standard membranes.

The blurring due to the halo b_H due to standard membranes indicated a dependence on the aperture diameter d_A (Figure 5.9). A linear fit analysis of the data

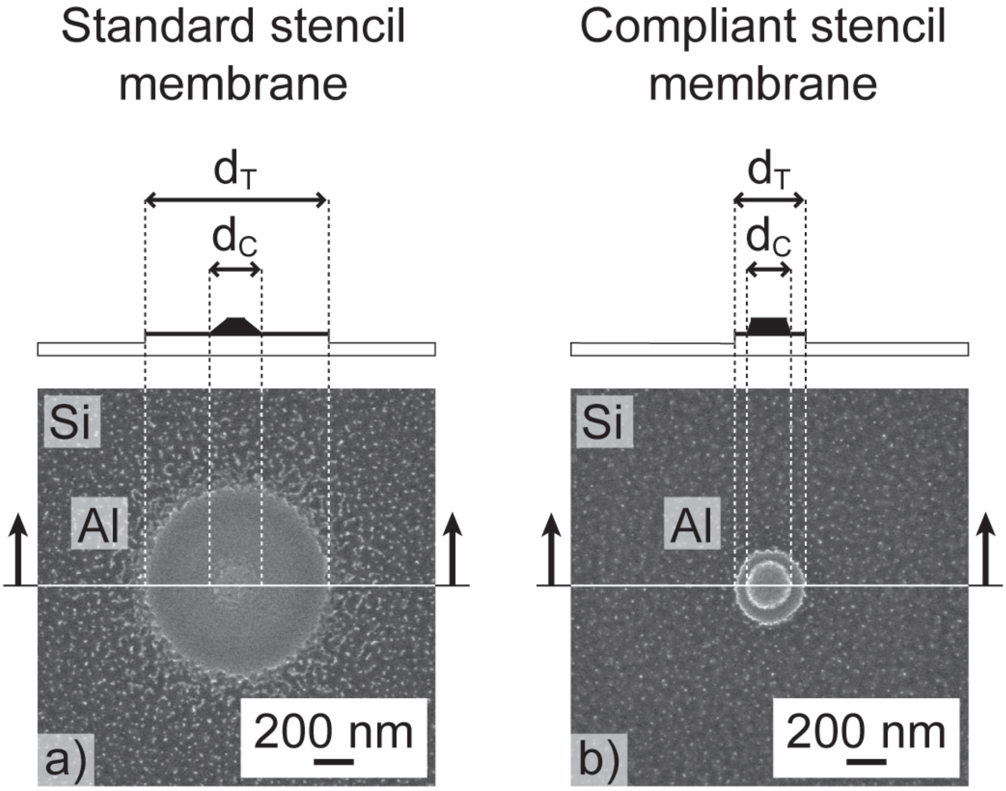


Figure 5.7: a) Top: Schematic cross section of an Al structure deposited through a standard stencil membrane. The gap g between stencil membrane and substrate determines the blurring. After deposition, the Si was etched for 15 s to enhance the contrast between the Al structure and the Si wafer. Bottom: Corresponding SEM illustration of a 50 nm thick Al structure patterned by standard stencil lithography. The diameter of the total structure d_T and the diameter of the center structure d_C are indicated by dashed lines. b) Top: Schematic cross section of an Al structure deposited through a compliant stencil membrane. The reduced gap g determines a minimized blurring. After deposition, the Si was etched for 15 s to enhance the contrast between the Al structure and the Si wafer. Bottom: Corresponding SEM illustration of a 50 nm thick Al structure patterned by compliant stencil lithography. The diameter of the total structure d_T and the diameter of the center structure d_C are indicated by dashed lines.

pointed out the relation of halo b_H vs. aperture diameter d_A.

$$b_H = (1.4 \pm 0.1)\ d_A + (170 \pm 50)\ \text{nm} \tag{5.3}$$

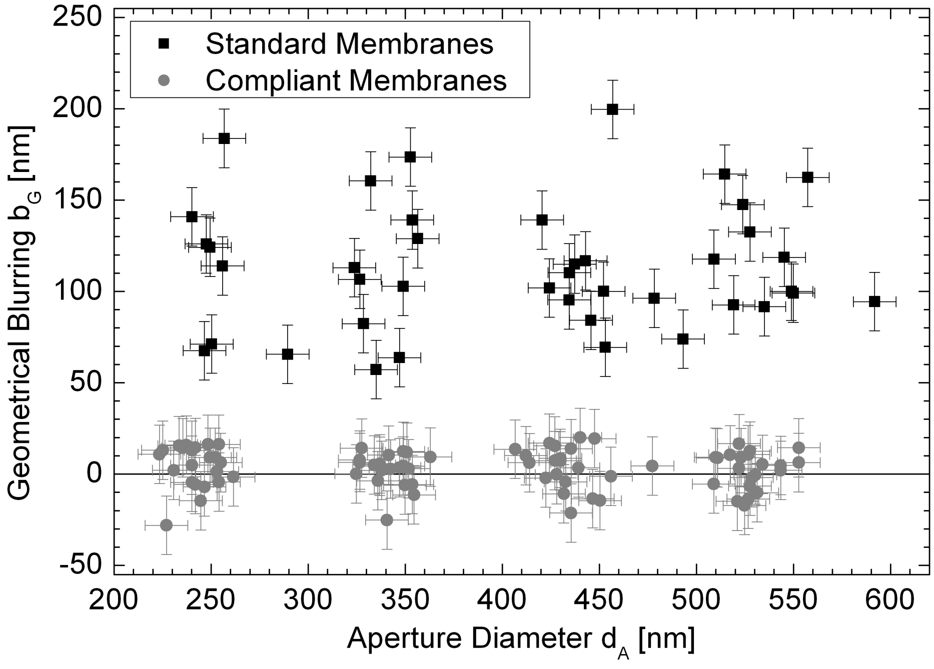


Figure 5.8: Graph comparing the geometrical blurring b_G vs. the aperture diameter d_A on the stencil membrane. The values were obtained from standard and compliant membranes. A 95 % reduction of the geometrical blurring b_G was observed in all cases. The geometrical blurring b_G remained approximately constant as it did not depend on the aperture diameter d_A.

Finally, the average blurring due to the halo b_H of Al structures patterned through compliant membranes was extracted. The result did not show any dependence on the aperture diameter d_A. The blurring due to the halo b_H of compliant membranes was (110 ± 15) nm (Figure 5.9). This resulted in a reduction of the halo of at least 75 % for apertures diameters d_A larger than 200 nm.

5.6 Discussion

FEM simulations of a specific compliant membrane design have shown that the minimum applied force to deflect all membranes is approximately 30 mN. The mechanical clamping system of stencil and substrate is a key issue to apply the necessary force.

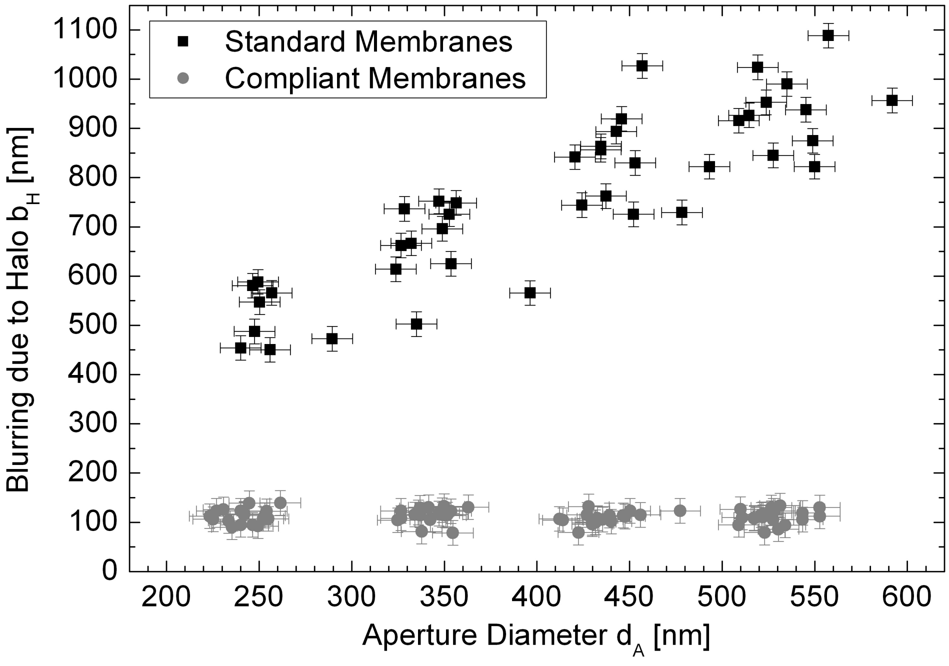


Figure 5.9: Graph comparing the halo b_H vs. the aperture diameter d_A on the stencil membrane. The values were obtained from standard and compliant membranes. A clear reduction of the halo b_H due to compliant membranes was observed in all cases. The halo b_H for compliant membranes remained constant and it did not depend on the aperture diameter d_A. Whereas the halo b_H for standard membranes depended linearly on aperture diameter d_A.

Due to an appropriate clamping system all the compliant membranes deflected and overcame the non-planarity of stencil and substrate. The characterization of the deposited structures resulted in an approximately constant blurring. Neither the geometrical blurring b_G nor the halo b_H showed any correlation to the location of the aperture within the wafer or its size. This confirmed a sufficient clamping mechanism, which allowed the compliant membranes to minimize the gap. FEM simulations have also shown that the dependence of the necessary clamping force with the supporting-cantilever length is negligible, which opens the possibility for a reduction in the size of such cantilevers, and therefore an increase of the density of the patterned area on full-wafer scale. In fact, the data confirmed the FEM result by not showing a change in the behavior for the different cantilever length tried in the experiment.

The geometrical blurring b_G in stencil lithography strongly depends on the gap g between stencil membrane and substrate, the source diameter d_S, the distance d between substrate and source, the membrane thickness t and the aperture size d_A (Figure 5.2 a) [85].

$$b_G = \frac{g(d_S + d_A) + d_A d - d_S \frac{t}{2}}{d + \frac{t}{2}} - d_A \tag{5.4}$$

The source diameter d_S and the distance d between substrate and source and the membrane thickness were constant parameters within the frame of these experiments. Apertures diameters d_A were nominally between 200 nm and 500 nm. Optical microscope measurements of the gap g, have reproducibly given higher values than 20 µm for standard membranes, whereas the appearance of interference fringes concluded to a gap g below 2 µm for compliant membranes. Following Equation 5.4, a value of b_G larger than 90 nm is expected for standard membranes, while a value of about 10 nm is expected for compliant membranes. Blurring characterizations of both configurations have shown a geometrical blurring b_G of (10 ± 10) nm and (113 ± 34) nm, respectively. Considering the error of the measurements, the result matches well into the theoretical model [85]. The previously described measurements of the gap g between stencil membrane and substrate showed that the compliant stencil configuration approached to the substrate surface. The geometrical blurring of compliant membranes was in all cases distinctively smaller compared to standard membranes. In average the geometrical blurring b_G decreased by 95 % on full-wafer scale. Gap measurements and geometrical blurring characterization have given evidence that compliant membranes reduced the gap and were closer to the substrate surface.

The blurring due to the halo has been previously observed in stencil lithography [85, 86]. The halo is caused by surface diffusion and mainly depends on the deposition parameters. The deposited material, the substrate temperature, the gap between stencil and substrate as well as the aperture dimension influence the size of the halo. This agrees with the experimental observation in [85]. Standard membranes with a gap g of more than 20 µm caused an aperture diameter d_A dependent halo $b_H = (1.4 \pm 0.1)\, d_A + (170 \pm 50)$ nm. Smaller apertures resulted in a smaller halo and vice versa. Compliant membranes have shown a constant halo b_H of (110 ± 15) nm due to their proximity to the substrate. As for the geometrical blurring b_G, the halo of compliant membranes was explicitly smaller than the halo of standard membranes.

5.7 Conclusion

The geometrical blurring and the blurring due to the halo have been investigated in standard and compliant stencil lithography. Standard and compliant membranes with nanoaperture arrays were fabricated on the same stencil. FEM simulations of a compliant membrane have shown that the total force necessary to deflect compliant membranes on full-wafer scale is very small. Gap measurements between stencil membrane and substrate surface were distinctively smaller in a compliant stencil configuration compared to a standard configuration. Gaps below 2 µm were obtained by the use of a compliant membrane, which confirmed the membrane flexibility. Evaporated Al was used to present the difference in blurring. The blurring of deposited structures is largely minimized due to a compliant stencil configuration. The characterizations of the deposited Al structures showed a largely minimized blurring. The geometrical blurring was decreased by 95 % and the blurring due to the halo by more than 75 %. These measurements proved that compliant membranes were in close contact with the substrate and adapted to its surface. The clearly reduced blurring was consistent on full-wafer scale. The mechanical clamping setup was appropriate as the blurring did not show any dependence on the cantilever length. In conclusion, with a compliant stencil configuration submicrometer stencil lithography becomes reliable patterning technique on full-wafer scale.

6 Summary, Conclusion and Outlook

6.1 Summary

Within this thesis, the following results were obtained:

1. Stencil lithography was applied to pattern Ti-Au wire test structures on flexible polymer substrates. The resistivity of the wires was analyzed by 2-point and 4-point measurements and between $3.0 \cdot 10^{-8}\,\Omega\text{m}$ and $4.0 \cdot 10^{-8}\,\Omega\text{m}$. The result was found to be comparable with the resistivity of a Ti-Au thin film on a Si wafer.

2. Pentacene TFTs were fabricated with a rigid Si back gate, PI or SiO_2 dielectric layers and Au top contacts. S/D contacts for channels down to 5 µm were patterned by chip-size stencil lithography. Electrical characterization has shown working pentacene TFTs on both dielectrics and with various pentacene film thicknesses. The output characteristics showed a typical linear and saturation regime. The maximal apparent mobility μ on PI was $0.36\,\text{cm}^2/\text{Vs}$ and on SiO_2 $0.46\,\text{cm}^2/\text{Vs}$, respectively.

3. Pentacene TFTs on a flexible PI substrate were fabricated with a local gate contact and aligned full-wafer stencil lithography for pentacene and S/D contact patterning. Electrical characterizations have shown transistor-like behavior. The pentacene TFTs maintained their performance after being peeled off the rigid Si support.

4. The developed process flow for pentacene TFTs on a flexible PI substrate was optimized and a 91.5 % yield of working devices was obtained on full-

wafer scale. The average apparent mobility μ was $(5.3 \pm 0.1) \cdot 10^{-2}\,\mathrm{cm^2/Vs}$ for channel lengths between $2.5\,\mu\mathrm{m}$ and $20\,\mu\mathrm{m}$.

5. The stability of the pentacene TFTs on a flexible substrate over time and under applied stress was monitored. The aging of the devices was analyzed while storing in a light-shielding box under ambient conditions. 216 days after fabrication, the relative apparent mobility μ/μ_0 was reduced to (53 ± 1) %. Peeling the PI substrate off the Si wafer reduced μ/μ_0 to (83 ± 4) %. Step-by-step applied strain up to 2.6 % decreased μ/μ_0 to (71 ± 3) %. The performance partially recovered to (81 ± 4) % after releasing the applied strain to the PI substrate. Cycling experiments of applied strain up to 2.7 % reduced the performance significantly. After 28'000 cycles μ/μ_0 remained (42 ± 3) % of its initial value.

6. Stencils were fabricated with different membrane release methods. A release by wet etching and by combined dry and wet etching was applied for chip-size and full-wafer stencils.

7. Wafer curvature variations during stencil fabrication were analyzed. The measurements have shown that the relative change of curvature $\kappa - \kappa_0$ increased due to asymmetric patterning of the stencil wafer front- and backside. An high wafer curvature of the stencil influences the gap that is the main cause for the loss of resolution in stencil lithography.

8. A compliant stencil configuration has been developed in order to minimize the blurring and increase the pattern transfer resolution. The improved resolution of compliant stencil lithography was shown by evaporating Al through the stencil onto a Si wafer. The geometrical blurring b_G was 95 % and the blurring due to the halo b_H more than 75 % smaller in compliant stencil lithography compared to standard stencil lithography. Standard membranes and compliant membranes supported by four protruding cantilevers were fabricated on full-wafer scale. FEM simulations were carried out to calculate the total force necessary to deflect compliant membranes on full-wafer scale.

6.2 Conclusion

Stencil lithography has shown to be a reliable patterning method for Ti-Au wire test structures on flexible polymer substrates. 2-point and 4-point measurement of the Ti-Au wire test structures have shown ohmic behavior. The extracted values for the Au resistivity on all polymer substrates corresponded to the measured value of a Ti-Au thin film on a Si wafer. Thus, stencil lithography was applied to achieve pentacene TFTs on a flexible PI substrate. An initial study of pentacene TFTs on a rigid Si substrate has shown working devices with PI and SiO_2 as dielectric layers. Stencil lithography was used to define S/D top contacts for TFT channel lengths down to 5 µm. The electrical characterization showed that PI is a suitable candidate for pentacene TFTs in comparison with SiO_2. Pentacene TFTs on a 12 µm thin flexible PI substrate were realized by aligned full-wafer stencil lithography for locally patterned pentacene and S/D top contacts. The pentacene TFTs on the flexible PI substrate maintained their functionality after being peeled off the rigid Si wafer. However, improvements were needed as the electrical TFT performance was dependent on the location on the wafer. An improved stencil alignment and a more stable pentacene deposition increased the yield of 72 pentacene TFTs on flexible substrates to 91.5 %. Pentacene TFTs with channel lengths down to 2.5 µm showed transistor-like characteristics with a linear and a saturation regime. The average apparent mobility μ was $(5.0 \pm 0.7) \cdot 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$. Mechanical manipulations and exposure to air and moisture decreased the electrical performance of the pentacene TFTs. Nevertheless, the functionality of the pentacene TFTs was maintained. It was demonstrated that three experiments have a significantly high impact on the performance. The apparent mobility μ was primarily influenced by the exposure to ambient conditions, peeling the TFTs off the rigid Si wafer and the first cycles of applied strain.

The study of the wafer curvature variations revealed that the different stencil fabrication steps make a significant contribution. Considering the wafer curvature can reduce the gap between the stencil membrane and the substrate surface. Hence, the blurring of the structures deposited by stencil lithography is reduced.

It was demonstrated that compliant stencil lithography improves the resolution of deposited structures. The geometrical blurring was reduced by 95 % and the blurring due to the halo by more than 75 %. This clearly minimized blurring was consistent on full-wafer scale. The resolution of standard full-wafer stencil lithography is mainly limited by the gap between stencil membrane and substrate surface. In a compliant stencil configuration, gap measurements between stencil membranes and the substrate surface were distinctively smaller compared to a standard configuration. Gaps below 2 μm were obtained by the use of a compliant membrane, which confirms the ability of the membranes to adapt to the substrate surface. The blurring of Al structures deposited through compliant membranes was largely minimized. These results demonstrate that submicrometer stencil lithography with a compliant stencil configuration becomes a reliable patterning technique on full-wafer scale.

6.3 Outlook

The obtained results within this thesis lead to future objectives and open new possibilities to apply stencil lithography for the fabrication of organic TFTs on flexible substrates.

Organic TFT channel dimensions down to 2.5 μm were successfully obtained. Applying submicrometer patterning techniques for stencil aperture definition can further reduce TFT channel dimensions. Several aspect ratios of the channel width to channel length would provide minimum channel dimensions for reliable membrane aperture designs.

Stencil lithography has demonstrated to be a reliable patterning technique for pentacene on flexible substrates. Other organic semiconductors can be patterned by evaporation through an aligned stencil. This opens the possibility for more complex architectures. Inverters or ring oscillators can be designed by combining organic p- and n-type semiconductors. This leads to organic circuit electronics on flexible substrates.

A significant drawback of pentacene TFTs is the decreasing electrical performance while storing at ambient conditions. The encapsulation of pentacene TFTs on flexible substrates could slow down the degradation of the pentacene films over time. The encapsulation material needs to be a diffusion barrier for air and moisture. The deposition has to be a solvent-free process at low temperature in order to avoid any damage of the pentacene film. For example, the polymer parylene could be used as a conformal encapsulation layer. Parylene is deposited at room temperature by chemical vapor deposition (CVD) [108]. After encapsulation, investigations have to be taken on the adhesion between the parylene and the PI layer. In addition, openings in the encapsulation layer have to be patterned in order to access S/D and gate contacts. An encapsulation layer may also reduce the impact to the pentacene film due to mechanical load.

The patterning of nanoapertures in compliant membranes was done by cost intensive FIB milling and provides room for improvement. High throughput patterning technologies such as deep-UV, nanoimprint or e-beam lithography can be applied for more cost-efficient aperture definition. A process flow considering the topography of the 40 µm high mesa structures needs to be developed.

As compliant stencil lithography improves the resolution on full-wafer scale, the alignment of compliant membranes to a prepatterned substrate could be addressed. The combination of apertures for pentacene and S/D contacts on compliant membranes with the alignment of full-wafer stencils could lead to smaller organic TFTs on flexible substrates.

Appendix

A Manuscript Submitted to Organic Electronics

The Effects of Channel Length and Film Microstructure on the Performance of Pentacene Transistors

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With the use of the stencil lithography, we fabricated pentacene thin-film transistors prepared on SiO_2 gate dielectrics with channel lengths ranging from 2 µm to 600 µm. By performing 4-probe measurements on these field-effect transistors, we were able to separate the respective contributions of the channel and the contacts to the transistor performance. The contact resistance depends strongly on the gate voltage and on the grain size and morphology. On the contrary, the channel carrier mobility is essentially independent of the microstructure. The low-field mobility in the channel is 0.5 $\mathrm{cm^2/Vs}$ to 0.6 $\mathrm{cm^2/Vs}$ in long-channel transistors and reaches 10 $\mathrm{cm^2/Vs}$ in short-channel transistors.

Keywords Organic thin-film transistor, contact resistance, pentacene film morphology

Introduction

The performance of an organic field-effect transistor is related to the microstructure and purity of the organic semiconductor[1,2], to the degree of order at the interface[3] and to the quality of the contacts. The need to miniaturize the organic electronic circuit and the use of standard lithographic methods has led to smaller and smaller channel length[4,5,6,7]. Several authors have observed that in such cases, the contact resistance dominates the device characteristics[8,9,10,11]. For very short channels (L $< 5\,\mu$m), the Schottky barrier at the source and drain contacts dominates device

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performance[12]. For long channels (L > 100 µm), the contact resistance is not determined by the barrier at the metal-organic semiconductor interface, but rather drift/diffusion of carriers close to this interface[13,14]. It has also been shown that the presence of a small concentration of residual carriers produced by doping the channel can decrease the contact resistance[15].

In the present work, we fabricated a series of pentacene thin-film transistors with channel lengths ranging from 2 µm to 600 µm. For this purpose, we have applied stencil lithography, which is a one-step technique with high resolution down to the sub-100 nm range thus eliminating solvent-based processing steps[16]. In this large range of channel lengths, the transistor performance changes from contact limited to channel dominated. We investigated the influence of the pentacene film morphology on the contact and channel performance by separating their contributions. This was made possible using 4-probes measurements.

Methods

The organic thin-film transistors (OTFTs) are based on pentacene as organic semiconductor and fabricated by high-vacuum deposition in top-contact configuration (Figure A.1 a). Heavily boron-doped Si wafers (resistivity of 0.1 Ωcm to 0.5 Ωcm) were used as substrates and served also as gate contacts. The wafer was coated with a thermal SiO_2 layer (200 nm in thickness).

Pentacene was deposited by thermal evaporation in a high-vacuum chamber at a rate of about 1 nm/min ($p < 10^{-7}$ mbar). The film thickness was 40 nm. The

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[12] cf. Footnote 9

[13] P. V. Pesavento, R. J. Chesterfield, C. R. Newman, C. D. Frisbie, "Gated four-probe measurements on pentacene thin-film transistors: Contact resistance as a function of gate voltage and temperature," *Journal of Applied Physics*, vol. 96, no. 12, pp. 7312-7324, 2004.

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[15] cf. Footnote 3

[16] cf. Footnote 3

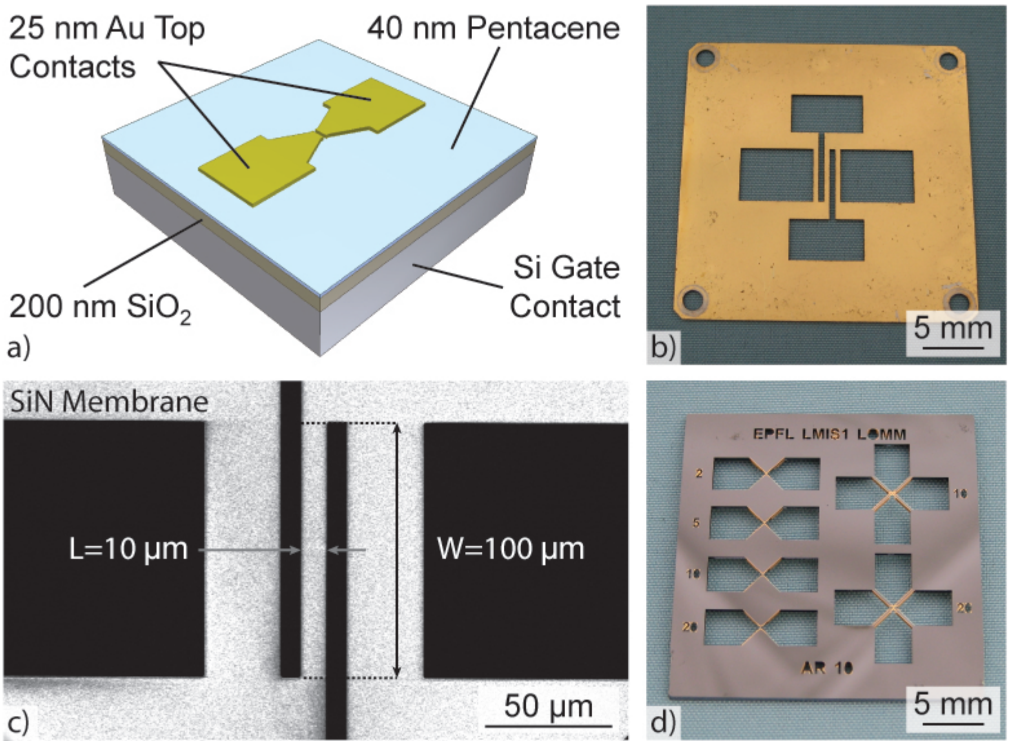

Figure A.1: a) OTFT architecture b) Metallic shadow mask for a channel length of 600 µm (4-probe configuration) c) SEM illustration of a stencil for a 4-probe configuration (white: low-stress SiN membrane) d) Stencil with two 4-probe and four 2-probe configurations.

substrate temperature is either 20°C (room temperature) or 55°C. The growth processes lead to different grain sizes (small grains at room temperature, larger grains at 55°C, Figure A.2). The film morphology is imaged by AFM in semi-contact mode (NT-MDT with a SMENA scanner). Pentacene was purchased at Fluka and twice purified in a furnace with a temperature gradient.

The gold top contacts were deposited by thermal evaporation under high vacuum ($p < 10^{-7}$ mbar) and have a thickness of 25 nm. The substrate was cooled to the temperature of liquid nitrogen (−185°C) during evaporation to avoid gold diffusion into pentacene.

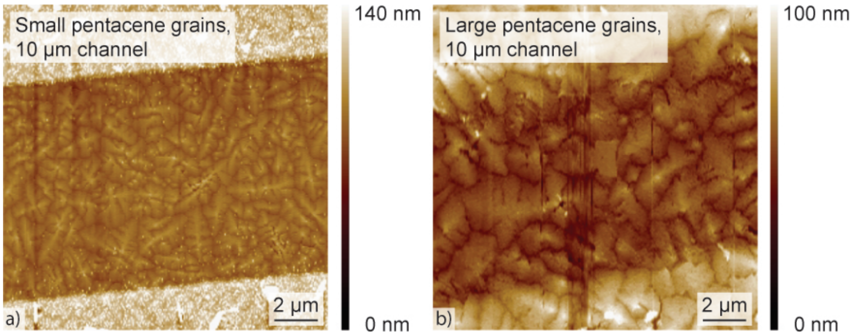

Figure A.2: AFM images of OTFTs with a channel length of 10 µm. Pentacene is evaporated a) at room temperature and b) at 55°C (substrate temperature), which results in small and large grains, respectively. The gold contacts define the channel on the top and on the bottom and have a thickness of 20 nm to 25 nm.

OTFTs with different contact geometry were fabricated. Contacts for long-channel transistors were patterned by a metallic shadow mask (Figure A.1 b). The channel has a length of 100, 200 and 600 µm and a width of 6 mm. A stencil was used to define the contacts for short-channel transistors (Figure A.1 c, Figure A.1 d). The stencils are made of a low-stress SiN membrane supported by bulk Si. The channel aspect ratio is 10 and includes the channel lengths of 2, 5, 10 and 20 µm.

The resistance of the OTFTs was characterized by 2-probe and 4-probe measurements (Keithley 236 source measure unit). By means of 4-probe measurements, the channel resistance was determined independently of the contact resistance[17]. A current is applied between the two outer electrodes while a voltage drop is measured between the inner electrodes. Using 2 probes, the properties of the entire device are measured. The contact resistance, therefore, was equal to the difference of the values measured by 2 and 4 probes; these measurements were made with a floating and a non-floating gate.

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The OTFTs were characterized by measuring output and transfer curves (Keithley 4200 SCS) under Argon atmosphere (after at least 4 h under vacuum). Drain and gate voltages were swept between 10 V and −40 V while the drain and gate currents were measured. The apparent mobilities were determined by the slope of the transfer curves measured in the linear regime. The threshold voltage is the intercept between the gate voltage axis and the linear fit of the transfer curve for high negative gate voltages[18,19].

Results

On the top of SiO_2, the morphology of the 40 nm thick pentacene film depends on the substrate temperature during pentacene deposition (as shown in Figure A.2 for two OTFTs with a channel length of 10 µm). At room temperature, the film has grown in submicron grains with a dendritic shape[20]. If the substrate temperature is 55°C, the grains increase in size (2 µm to 3 µm in diameter) and become more compact.

The film morphology is identical for long- and short-channel transistors because the pentacene films are deposited during the same evaporation.

The output curves in Figure A.3 show that all transistors have a linear regime around zero drain voltage and reach saturation. At a gate voltage of −40 V, the drain current through a transistor with a short channel (10 µm in length) is about twice as high as through a long-channel transistor (600 µm in length, Figure A.3).

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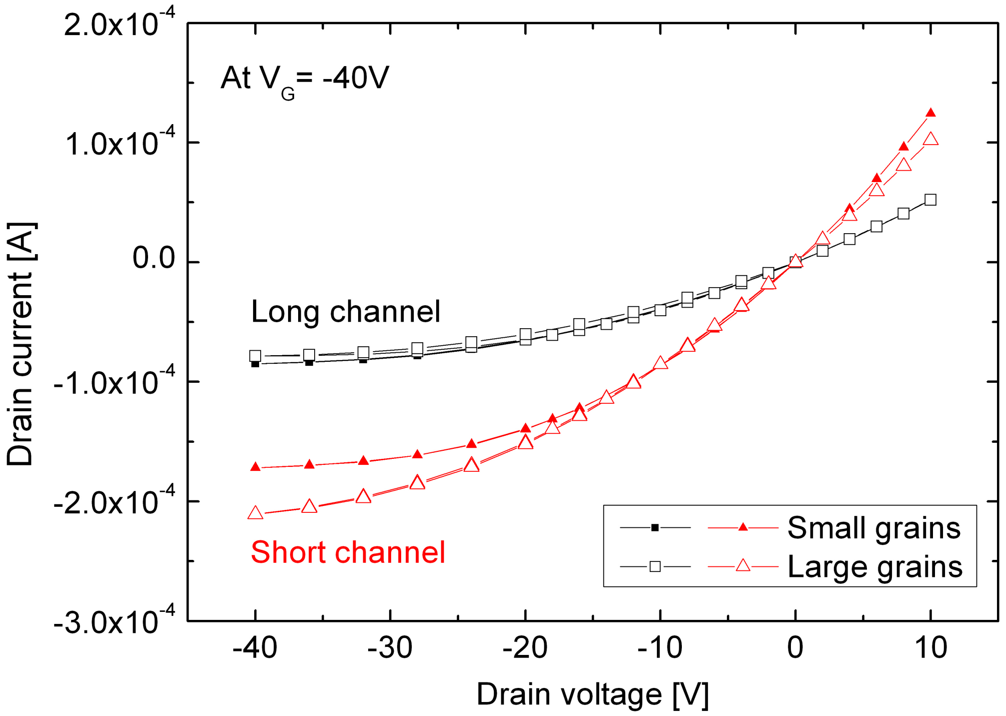
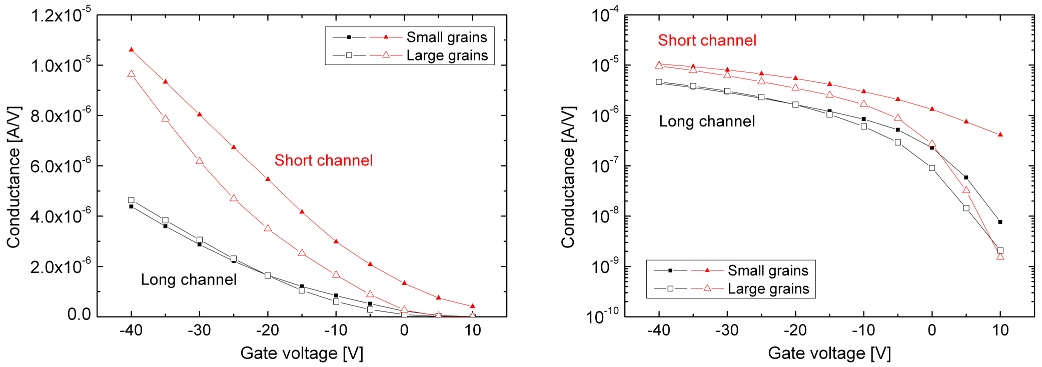


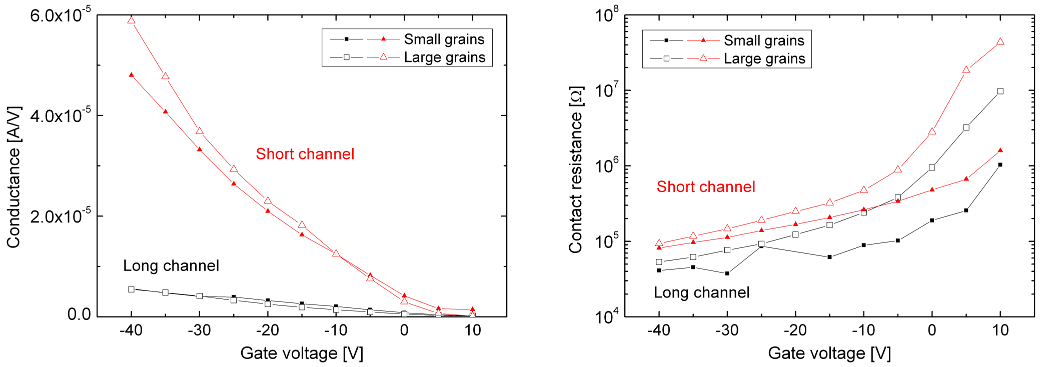
Figure A.3: Output curves of OTFTs with long and short channels (600 µm and 10 µm, respectively) and different film morphologies (small and large grains). The gate was polarized at a voltage of −40 V.

The transfer characteristics in Figure A.4 show that the short- and long-channel transistors behave differently. The performance of long-channel transistors is dominated by the channel what is shown in the small difference between the transfer curves of the entire device and the one of the channel only (Figure A.4 a, Figure A.4 b). Consequently, the apparent and channel mobility do not differ significantly (from 0.45 to 0.74 cm^2/Vs, Table A.1).

In contrast, the transistors with a short channel (2 µm - 20 µm) are limited by the contacts. The channel conductance is approximately 5 times higher than the conductance of the entire device (Figure A.4 a, Figure A.4 c). As expected, this behavior is reflected in the mobility values. While the apparent mobility of the



(a) Entire device (b) Entire device



(c) Channel (d) Contacts

Figure A.4: ransfer curves a) and b) of the entire device and c) of the channel, d) contact resistance depending on the applied gate voltage for OTFTs with long and short channels (600 µm and 10 µm, respectively) and different film morphologies (small and large grains, respectively). The samples are the 4-probe devices of Table A.1.

entire device is in the range of 1.0 to 1.5 cm^2/Vs, the apparent mobility of the channel is more than 5 times higher, and reaches 10 cm^2/Vs. The contact resistance is 2 - 3 times higher in short-channel transistors than in long-channel ones (Table A.1).

Channel		Entire device		At floating gate		
Apparent mobility (cm^2/Vs)	Threshold voltage (V)	Apparent mobility (cm^2/Vs)	Threshold voltage (V)	Total resistance (MΩ)	Channel resistance (MΩ)	Contact resistance (MΩ)
Long channel (600 µm), small grains (0.2 µm - 0.5 µm)						
0.59	7.3	0.45	8.3	1.39	1.26	0.14
Long channel (600 µm), large grains (2 µm - 3 µm)						
0.74	-1.8	0.58	-2.7	2.92	2.11	0.81
Short channel (10 µm), small grains (0.2 µm - 0.5 µm)						
7.42	-6.9	1.39	-4.3	0.67	0.23	0.44
Short channel (10 µm), small grains (2 µm - 3 µm)						
10.2	-10.8	1.57	-10.8	3.15	0.33	2.82

Table A.1: Characteristic values for the entire device and the channel.

Discussion

The 4-probe and 2-probe measurements are an excellent tool to separate the channel resistance (or conductance) from the contact resistance. The most important results of this work are those summarized in Figure A.4 c, Figure A.4 d and Table A.1. Figure A.4 d shows clearly that the contact resistance depends significantly on the gate voltage and also on the grain size and morphology. Gold films evaporated on small dendritic grains always give smaller contact resistances than the same films evaporated on large grains. The dendritic shape of small grains is more favorable to low contact resistance than the round shape of large grains.

Even more surprising is the behavior of the pentacene channel resistance in a floating gate configuration. Table A.1 shows that pentacene films made of small grains are always more conductive than films of the same length made of large grains; this fact demonstrates that grain boundaries do not act as simple barriers but also modify the trap distribution. More precisely small dendritic grains which lead to a higher density of grain boundaries in the film induce more charge transfers at the interface

	Apparent mobility (cm^2/Vs)	Conductivity (10^{-8} S□)	Threshold voltage (V)	Total resistance (MΩ)
Long channels, small grains (0.2 µm - 0.5 µm)				
600 µm	0.45	7.2	8.3	1.39
200 µm	1.04	14.3	1.0	0.23
100 µm	1.21	14.6	-1.1	0.12
Short channels, small grains (0.2 µm - 0.5 µm)				
20 µm	1.51	17.1	-1.4	0.58
10 µm	1.39	14.9	-4.3	0.67
5 µm	1.27	5.0	-6.3	2.0
2 µm	1.08	1.3	-5.1	8.0
Long channels, large grains (2 µm - 3 µm)				
600 µm	0.58	3.4	-2.7	2.92
200 µm	0.68	0.88	-12	3.78
100 µm	0.28	0.31	-12	5.36
Short channels, large grains (2 µm - 3 µm)				
20 µm	1.31	5.79	-4.8	1.73
10 µm	1.57	3.17	-10.8	3.15
5 µm	0.69	3.61	-3.3	2.77
2 µm	0.82	7.31	2.9	1.38

Table A.2: Characteristic values for OTFT with different channel lengths. The apparent mobility refers to the entire device and contains hidden contributions due to the contacts (cf. Table A.1). The conductivity results from 2-probes measurements with a floating gate; they reflect the presence of a density of residual carriers in the channel.

of the oxide than large grains because the grain boundary line is longer. By charge transfers, additional charges (residual carriers) are transferred to the semiconductor film which make it conductive at zero gate voltage[21]. These charge transfer reactions explain why at short channel lengths the channel conductance is not linear with the channel length.

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[21] cf. Footnote 17

The apparent mobility of the channel is less sensitive to the presence of residual carriers because it is determined mainly at high and moderate gate voltages. In short channels, where the carriers cross only a few grains, the mobilities are on the order of 10 cm^2/Vs and large grains perform better than small grains (Table A.1). In long channels, the trap distribution at the interface is significantly modified and the apparent mobility drops to between 0.6 and 0.7 due to defects acting mainly on the trap distribution.

Due to contact effects, the apparent mobility in the short 10 μm devices made of large grains drops from 10 to 1.6 cm^2/Vs. For long channels, the effect of the contacts is obviously much lower and the apparent mobility of the long-channel devices remains very close to 0.5 cm^2/Vs to 0.6 cm^2/Vs due to the apparent mobility in the channel (0.6 cm^2/Vs - 0.7 cm^2/Vs).

The transistors which were compared in this work have been fabricated with pentacene layers of 40 nm thick. For the sake of clarity, we have not presented here the results obtained for 20 nm- and 40 nm-thick pentacene layers; however, we observed essentially the same behavior for all thicknesses. It is worth mentioning that the thickness of 40 nm represents a sort of optimum. The channel mobilities in both 20 nm and 80 nm transistors are 20 % lower.

Conclusion

Pentacene thin-film transistors have given rise to a very large number of studies in the literature, which are not always consistent with each other. The use of the stencil technology together with 4-probe measurements has partly clarified the surprising behavior of the apparent mobility with the pentacene grain size and the channel length. In fact, the contact resistance and the channel resistance are both gate voltage dependent and can vary in an opposite way with grain size and morphology. In pentacene transistors prepared directly on an oxide gate, the interface traps and charge transfer centers dominate the transport. Although they belong essentially to the oxide, their activity is very often related to the presence of the grain boundaries of the pentacene dendritic grains. It is worth mentioning that a self-assembled monolayer reduces the morphology dependence by separating the interface traps and charge transfer centers from the pentacene film (surface passivation).

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