Very High Density Microelectrode Array with Monolithically Integrated Readout Circuits

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***Abstract*—This paper presents the hardware realization and modeling of high-density microelectrode arrays including both microelectronic readout amplifiers as well as three-dimensional microelectrodes forming a fully integrated CMOS compatible system enabling research in electrophysiology. The presented chip offers the highest density of microprobes, reported in literature, all of which can be accessed through on-chip amplifiers, using a time-multiplexing scheme. An accurate model of the electrode interface including noise performance is also presented.**

I. INTRODUCTION

Microelectrode arrays (MEAs) are becoming increasingly useful tools in electrophysiology experiments, enabling monitoring the electrical activity of acute neural tissues or cell cultures *in-vitro*. Commercial systems typically operate with 64-channels, and a limited resolution, where the microelectrode pitch is at 60 µm [1]. Recent research results have demonstrated the possibility of achieving a significant resolution increase [2], [3], while increasing the number of channels, mostly using time multiplexing [4]. Three-dimensional microprobes have been demonstrated to increase the electrical coupling in read-mode [5], and a similar improvement can be expected to occur in stimulation-mode, resulting from a better concentration of the electric field which can be achieved by a proper geometrical design of the electrode tip. Three-dimensional electrodes have been proposed in [6], and fabricated through conventional micro-machining technology. The microfabrication of micrometer-resolution 3D tip probes using conventional techniques has been previously demonstrated in [7], where a CMOS compatible post-fabrication is used to construct very dense microelectrodes on the top of a bulk chip, only integrating connectivity, as a first attempt to approach the density of a commercial integrated circuit.

This paper presents an original fabrication technique of a MEA and its amplification circuits based on standard fabrication of CMOS circuits, followed by post-fabrication steps based on oxide recession to uncover the very-high density three-dimensional electrodes. Circuit developments are presented in Section II, and the microelectrode fabrication and results is presented in Section III. The electric model of the interface system consisting of the neural cell, the electrolyte and electrode, also including the amplifier is shown in Section IV.

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II. CMOS READOUT CIRCUITS

A. Chip Design

Six 200µm × 200µm pools consisting of electrodes with different shapes and densities have been realized on a single chip, in order to evaluate the proposed 3D multi-electrode array. All electrodes are built on top of the drain contacts of minimum-sized NMOS transistors which act as switches to select/deselect the corresponding electrode, as schematically depicted in Fig. 1. Two address decoders generate vertical and horizontal controlling signals to select the desired electrode individually, and channel the sensed neural signals to one of the 48 bio-amplifiers, integrated on-chip.

Pillar electrodes are composed of a stack of M1 (Metal 1) up to M5 patches, and all the intermediate vias, as shown in Fig. 2. The minimum size of these electrodes is limited by the size of via4-5 and the density is bounded by the density of the NMOS switches. Two pools of pillar electrodes with different densities have been developed.

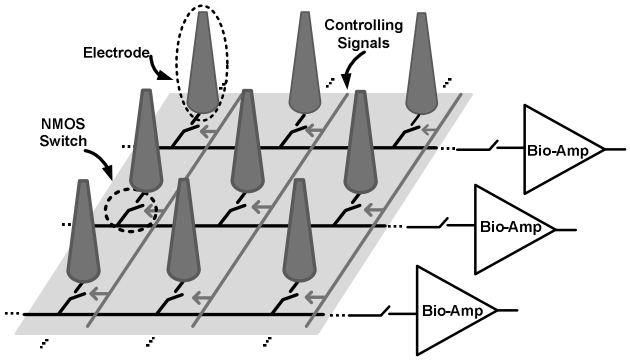
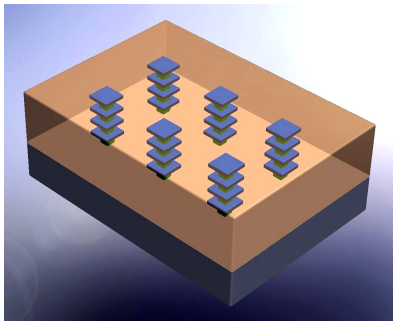
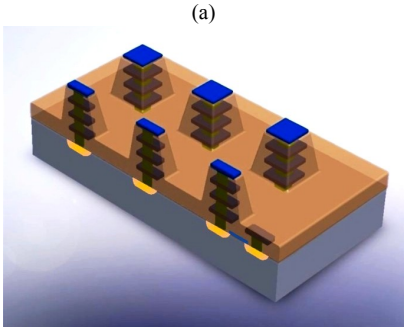


Figure 1. High density MEA, including the access transistor and amplifiers.



(a)



(b)

Figure 2. Conceptual view of the MEA fabrication. (a) Stacks of vias and metal are burried in SiO2, (b) overview and cross-section after oxide removal. Two lower metal layers are preseved for local routing (not shown here).

Flat electrodes are formed from three metal layers only, while the upper one, M3, is widened to increase the sensing surface of the electrodes. Pyramid shaped electrodes with 45° angle are made of M1 up to M5 with different widths and lengths while the intermediate vias provide electrical connections. The inverted pyramid electrodes have no tips and their sensing surface is the side-walls and the bottom of an inverted pyramid. The spacing between the pools is 50 µm, that is filled with M6 which has the role of shielding to isolate the pools from each other and other circuitry. Table I summarizes the electrode densities of the individual pools.

TABLE I. ELECTRODE DENSITIES OF THE POOLS

Pool Type	Density (# of electrodes / mm^2)
Dense pillar electrodes	295,200
Wide flat electrodes	40,000
Pyramid electrodes	22,500
Flat electrodes	295,200
Sparse pillar electrodes	11,025
Inverted pyramid electrodes	7,225

B. *Bio-Amplifier Design*

The choice of a bio-amplifier is crucial in this design because it can affect the measured performance of the MEAs. Moreover, the primary goal is to integrate as many amplifiers as possible on the chip to increase the number of recording sites. To this aim, the bio-amplifier with low-frequency suppression proposed in [8] has been utilized. Fig. 3 depicts the schematic of the bio-amplifier where a Miller integrator consisting of amplifier A_2, capacitor C_I, and high-resistance

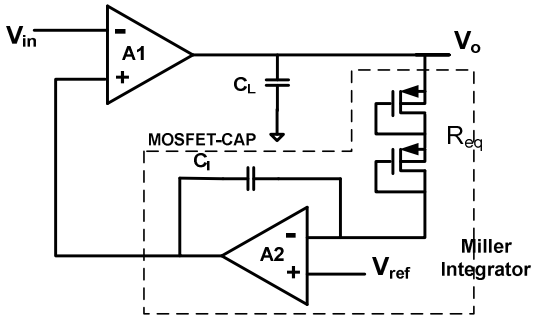


Figure 3. Bio-amplifier with low-frequency suppression.

R_{eq} is connected between the output node and positive input of the main amplifier to cancel out low frequency input voltages. The high-resistance R_{eq} consists of two diode-connected PMOS transistors with exponential I-V characteristics. It can be shown that the upper cut-off frequency, the lower cut-off frequency, and the mid-band gain of the bio-amplifier are as follows:

$$f_{hp}=1/(R_{eq}C_I) \quad (1)$$

$$f_{lp}=1/(\omega_{p1}) \quad (2)$$

$$\text{Gain}=A_{10} \quad (3)$$

where ω_{p1} and A_{10} denote the dominant pole and the low frequency gain of A1, respectively. The main amplifier, A_1, uses a simple low-noise current mirror OTA while the integrating amplifier, A_2, has a two-stage lead-compensated topology to reach higher gain. Extra effort has been spent to obtain very low-noise performance under low power consumption condition. Since the oxide recession technique is used to fabricate the electrodes, Metal-to-Metal (MiM) capacitors which normally occupy upper metal layers are avoided and MOSFET capacitors have been utilized to implement all the capacitors in the design. Furthermore, due to a large DC drop over the integrating capacitor, C_I, the linearization method proposed in [9] is used.

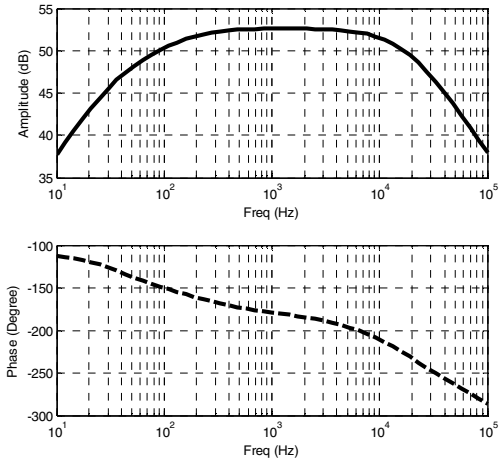


Figure 4. Simulated phase and frequency response of the bio-amplifier.

TABLE II. BIO-AMPLIFIER SPECIFICATIONS

Parameters	Simulation Results
Mid-band gain	53dB
Upper cut-off frequency	24.3 kHz
Lower cut-off frequency	82 Hz
Input-referred noise	13.5 μV_{rms}
Technology	0.18 µm-CMOS
Supply voltage	1.8 V
Supply Current	8.6 µA
Area	165µm x 230µm

The simulated phase and frequency response of the bio-amplifier is depicted in Fig. 4, and its specifications are summarized in Table II.

III. ARRAY OF CMOS COMPATIBLE MICROPROBES

Enabling the fabrication of a MEA system consisting in a single die dictates that all fabrication steps needed to realize the electrode array must be compatible with the CMOS process, and its stringent constraints in terms of thermal budget. A standard 0.18µm CMOS fabrication process has been used to fabricate biosensor chips.

Inductively coupled plasma dry etching is applied to remove the top silicon nitride Si_3N_4 passivation layer, as well as the silicon dioxide SiO_2 isolation layers. Oxide recession is performed uniformly over a single die mounted on a sacrificed carrier wafer. Oxide is recessed only over the pools where various microprobe structures have to be revealed. All surrounding microelectronic circuits are developed using metal layers strictly running underneath M3; a coverage of M6 and M5 guarantees full protection of these devices. The chip bonding pads are located on the periphery, and are not shielded. Subsequently, a coating must be realized to create the dielectrics covering the microelectrodes. The result after oxide recession to M3 is shown in Fig. 5. In Fig. 5(b) and 5(c), pillar microelectrodes with very small (*nanometer-scale*) tip radius and micrometer-resolution pitch are formed. Fig. 5(a) and 5(d) show inverted pyramidal and pyramidal-shaped electrodes, respectively.

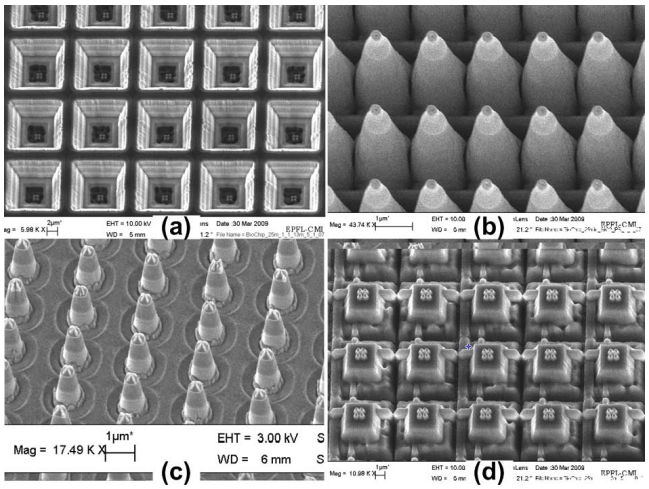


Figure 5. SEM microphotographs. (a) Inverted pyramide shaped, (b) and (c) pillar-shaped, and (d) pyramidal shaped microelectrodes.

IV. ELECTRICAL MODELING OF THE MICROELECTRODES

An electrical model of the cell-electrode interface for recording neural activity from high-density MEAs has been developed by the authors [5], with the goal of enabling the co-simulation of the cell-electrode interface with the CMOS circuits. However, this electrical model has been developed for standard Pt electrode arrays, and the electrode impedance needs to be adapted in this work. It is now described as

$$Z_{el}(j\omega) = \frac{1 + j\omega R_{spread} C_{el}}{j\omega C_{el}} \quad (4)$$

where R_{spread} is the spreading resistance, and C_{el} is the electrode capacitance. The numerical values given in [10] are considered. In particular, the dielectric constant of the electrode ε_r is equal to 45, and the dielectric thickness d_r of the electrode is considered to be 40 nm.

The amplitude of the transfer function $H(s) = V_S(s)/V_M(s)$ versus the electrode radius is depicted in Fig. 6 for different frequencies corresponding to the frequency range of neural activity. $V_M(s)$ is the electrical potential in the neural cell, and $V_S(s)$ is the potential which is sensed by the amplification stage. A typical cell diameter of 20 µm, and a cell-electrode distance of 70 nm are considered. Furthermore, the load impedance is modeled by a 8 pF capacitance. This value represents the gate capacitance of the input transistor in the amplification stage. As shown in Fig. 6, for an electrode radius of 10 µm, the voltage drop from V_M to V_S is equal to 25-70 dB depending on the frequency. For smaller electrodes, this value increases dramatically. However, if the voltage drop is larger than 80 dB, V_S is smaller than 10 µV upon recording an action potential. The potential that is sensed is thus smaller than the noise level of typical amplification stages. Therefore, for high-density MEAs, neural activity recording becomes very challenging and amplification stages with very low noise characteristics are mandatory.

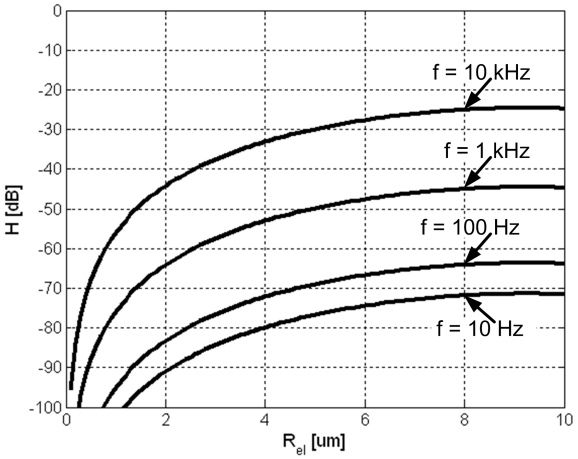


Figure 6. Amplitude of the transfer function $H(s) = V_S(s)/V_M(s)$ versus the electrode radius for different frequencies of V_M corresponding to the frequency range of neural activity.

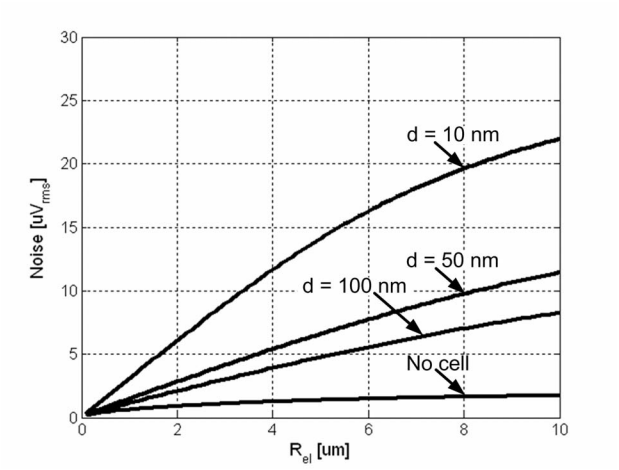


Figure 7. Cell-electrode output noise versus the electrode radius with and without a cell covering the electrode. The bandwidth 80 Hz – 25 kHz is considered for the output referred noise calculation.

A cell-electrode noise model has also been developed by the authors [11]. The equivalent noise of the cell-electrode interface at node V_S needs to be calculated in order to be able to compare the electrode and electrolyte solution noise with the noise of the CMOS circuitry. Furthermore, the noise at the cell-electrode interface is modeled as thermal noise [12]. Thus, for the case where no cell lies on top of the electrode, the electrode noise spectral density at node V_S is expressed as in (5). For the second possible case, where one cell entirely covers the surface of the electrode, the electrode and electrolyte solution noise spectral density at node V_S is described as in (6).

$$V_{S,noise} = \frac{Z_{load}}{Z_{el} + Z_{load}} \sqrt{4kTR_N} \quad \left[\frac{V}{\sqrt{Hz}}\right] \qquad (5)$$

$$V_{S,noise} = \frac{Z_{load}}{Z_{el} + R_{seal} + Z_{load}} \sqrt{4kT\left(R_N + R_{seal}\right)} \quad \left[\frac{V}{\sqrt{Hz}}\right] (6)$$

where Z_{load} is the load impedance; R_{seal} is the seal resistance, and R_N is the real part of the electrode impedance.

The cell-electrode interface output noise, with a spectral density expressed in (5) and (6), is depicted in Fig. 7, where it is related to the electrode size. The considered physical and electrical parameters are identical to those used in Fig. 6. The output noise is observed to increase with the electrode size. Furthermore, noise is higher when a cell lies on top of the electrode, with the amplitude dependent on the cell-electrode distance. For typical adhesion on the electrode surface, which is modeled as a cell-electrode distance of 50 nm, the cell-electrode interface output noise is as large as 11.5 μV_{rms} for an electrode diameter of 20 µm. This value is in the same order of magnitude as the total input referred noise of the amplification stage, as depicted in Table II. Thus in this case, the cell-electrode interface noise cannot be neglected when designing CMOS-based MEAs. However, when designing high-density MEAs with electrode diameters smaller than 5 µm, the cell-electrode noise is much smaller than the input referred noise of the bio-amplifier, and can thus be neglected. This characteristic compensates the decrease of the amplitude of the transfer function for very small electrodes, as depicted in Fig. 6. Thus, an optimum electrode size must be experimentally measured in order to obtain the highest possible signal-over-noise ratio.

V. CONCLUSION

Very-high density MEAs are fabricated exploiting the exceptional structural density offered by regular CMOS processes, and subsequently removing oxide to reveal submicron-scale microelectrodes. The presented bio-chip has six pools, and all electrodes can individually be connected to one of 48 readout channels. With a maximal electrode density of 295,200/mm^2 electrodes and micrometer-resolution pitch, this chip enables MEA measurements with the highest electrode density that is currently reported in literature.

REFERENCES

[1] Multi Channel Systems MCS GmbH, http://www.multichannelsystems.com (accessed on October 8, 2009)

[2] B. Eversmann *et al.*, "A 128 x 128 CMOS biosensor array for extracellular recording of neural activity," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2306-2317, Dec. 2003.

[3] U. Frey, U. Egert, F. Heer, S. Hafizovic, and A. Hierlemann, "Microelectronic system for high-resolution mapping of extracellular electric fields applied to brain slices," *Biosens. Bioelectron.*, vol. 24, no. 7, pp. 2191-2198, Mar. 2009.

[4] U. Frey *et al.*, "An 11k-electrode 126-channel high-density microelectrode array to interact with electrogenic cells," in *Proc. IEEE ISSCC 2007*, pp. 158-593.

[5] N. Joye, A. Schmid, and Y. Leblebici, "An electrical model of the cell-electrode interface for high-density microelectrode arrays," in *Proc. 30th Annu. Int. IEEE EMBS Conf.*, pp. 559-562, 2008.

[6] M. O Heuschkel, M. Fejtl, M. Raggenbass, D. Bertrand, and P. Renaud, "A three-dimensional multi-electrode array for multi-site stimulation and recording in acute brain slices," *J. Neurosci. Methods*, vol. 114, pp. 135-148, Mar. 2002.

[7] N. Joye, A. Schmid, and Y. Leblebici, "Three-dimensional silicon-based MEA with high spatial resolution," in *Proc. 6th Int. Meeting on Substrate-Integrated Microelectrodes*, pp. 310-313, 2008.

[8] B. Gosselin, M. Sawan, and C. A. Chapman, "A low-power integrated bioamplifier with active low-frequency suppression," *IEEE Trans. On Biomedical Circuits and Systems*, vol. 1, pp. 184-192, no. 3, September 2007.

[9] T. Tille, J. Sauerbrey, and D. Schmitt-Landsiedel, "A 1.8-V MOSFET-nly ΣΔ Modulator UsingSubstrate Biased Depletion-Mode MOS apacitorsin Series Compensation," *IEEE Journal of Solid-State Circuits*, vol. 36, pp.1041-1047, no. 7, July 2001.

[10] F. Hofmann *et al.*, "Technology aspects of a CMOS neuro-sensor: back end process and packaging," in *Proc. ESSDERC*, pp. 167-170, 2003.

[11] N. Joye, A. Schmid, and Y. Leblebici, "A cell-electrode interface noise model for high-density microelectrode arrays," in *Proc. 31th Annu. Int. IEEE EMBS Conf.*, pp. 3247-3250, 2009.

[12] M. Voelker and P. Fromherz, "Nyquist noise of cell adhesion detected in a neuron-silicon transistor," *Physical Review Letters*, vol. 96, no. 22, June 2006.