Double-gate pentacene thin-film transistor with improved control in subthreshold region

Dimitrios Tsamados[1,*], Nenad V. Cvetkovic[1], Katrin Sidler[2], Jyotshna Bhandari[1], Veronica Savu[2], Juergen Brugger[2] and Adrian M. Ionescu[1]
Nanoelectronic Devices Laboratory (Nanolab), [2]Microsystems Laboratory (LMIS1)
Ecole Polytechnique Fédérale de Lausanne
CH 1015, Lausanne, Switzerland

Abstract— In this work double-gate pentacene TFT architecture is proposed and experimentally investigated. The devices are fabricated on a polyimide substrate based on a process that combines three levels of stencil lithography with standard photolithography. Similarly to the operation of a conventional double-gate silicon FET, the top-gate bias modulates the threshold voltage of the bottom-gate transistor and significantly improves the transistor subthreshold swing and leakage current. Moreover, the double gate TFT shows good promise for the enhancement of I_{ON}/I_{OFF}, especially by the control of I_{OFF} in devices with poor top interfaces.

Keywords: Double-gate, pentacene, organic TFT, stencil lithography

*Corresponding author: Dimitrios Tsamados, EPFL-Nanolab, EPFL station 11, ELB 334, 1015, Lausanne, Switzerland, dimitrios.tsamados@epfl.ch

I. INTRODUCTION

Organic thin-film transistors have gained a lot of attention in the last years, especially devices with pentacene as the semiconductor active layer. Various architectures have appeared, combining bottom-gate or top-gate electrodes [1] with top or bottom source and drain. The main goal of these approaches is to improve the electrostatic control of the gate over the pentacene conductive channel as well as to diminish the contact resistances at the source and drain regions [2].

In this work we present a double-gate (DG) architecture of pentacene TFTs with top-contacted source and drain regions fabricated on an organic flexible substrate using relatively thin gate dielectrics (<230 nm polyimide or parylene-D). Previous works have used either bottom-contact architectures or top-contact but with long channels (~100 μm) and thick dielectrics (350 nm-1.4 μm) [3, 4]. As it will be demonstrated in the following paragraphs the top gate can be used to successfully suppress any parasitic top-interface channel and greatly ameliorate both the leakage current levels and the subthreshold swing by modulating the threshold voltage of the bottom-gate transistor.

II. FABRICATION

In view of further miniaturization and process improvements we adopted a previously reported aligned stencil lithography process [5, 6] as a clean, resistless, in-vacuum patterning technique for organic electronic devices on plastic substrates. A typical stencil is composed of low-stress silicon nitride (SiN) membranes, which contain

design-specific micro-apertures. The membranes are released by wet etching chemistry and finally supported by bulk silicon (Si). The stencil is aligned and clamped to the substrate, the required material is deposited through the stencil, and finally the stencil is removed, leaving the substrate patterned.

Stencils

Full wafer stencils with different designs were fabricated to locally pattern pentacene and to define S/D as top contacts. The stencils are fabricated on 100 mm Si wafer and 500 nm low-stress silicon nitride for the mask membranes. The full-wafer stencils include alignment marks to position stencil apertures relative to the patterned gate contacts on the substrate. Membrane apertures for local pentacene patterning are rectangular and apertures for S/D top contacts define channel lengths of 3 μm to 20 μm and channel widths of 3 μm to 50 μm.

The fabricated double-gate organic thin-film transistors (DG OTFTs) are structures composed of several thin layers, described in Fig. 1, in the order of their successive processing: a) thick polyimide substrate, platinum layer for the bottom-gate electrode, b) bottom-gate dielectric layer (thin polyimide), c) thin film of pentacene, d) gold for source and drain electrodes, e) top-gate dielectric layer (thin parylene-D) and f) platinum layer for the top-gate electrode.

DG OTFTs are fabricated using a combination of standard photolithography and stencil lithography method [7]. The first step is the deposition of a 12-μm-thick polyimide substrate (flexible once delaminated from the handle wafer, see Fig. 3) on a Si-wafer by spin-coating, as shown in Fig. 2b. The substrate is then soft-baked at 70 ºC to remove the solvent and hard-baked for 4.5 h at 300 ºC in order to gain sufficient level of polymerization. In the following step, the bottom-gate metal consisting of a

10-nm-thick Ti adhesion layer and a 50-nm-thick Pt layer is patterned by lift-off (using an EVG150 coater and developer system and an e-beam Leybold Optics Lab 600H evaporator, Fig. 2c). Next, a thin layer of polyimide (~230 nm, Fig. 2d) is deposited as the bottom-gate dielectric by spin-coating, followed by soft-baking and hard-baking (polyimide 60 wt% PI2610 + n methyl-2-pyrrolidone, spin-coating at 5000 rpm for 40 s). Another standard photolithography step for defining the location of the vias for the bottom gate contacts is performed followed by dry etching through the vias in oxygen plasma with a STS Multiplex Inductively Coupled Plasma (ICP) Reactive Ion Etcher (Fig. 2e). Source and drain 10-nm-thick Ti adhesion pads are deposited by e-beam metal evaporation and lift-off method (Fig. 2f). The following step is the deposition of the active semiconductor material, triple-purified 100-nm-thick pentacene, which is done by evaporation at room temperature through an aligned stencil in a Kurt J. Lesker thermal evaporator with 5 Å/min evaporation rate and at a pressure of 2.7×10^{-7} mbar (Fig. 2g). A second aligned stencil is used for e-beam evaporation of a 100-nm-thick Au layer to pattern the source and drain contacts (Fig. 2h). The top-gate dielectric layer (200-nm-thick parylene-D) is deposited by a CVD process in Comelec C-30-S parylene deposition system (Fig. 2i). Parylene-D has not be used for the bottom gate dielectric due to problems with poor adhesion of the layer on the underlying thick-polyimide substrate. Deposition of 300 nm-thick Pt top gate is done by another e-beam metal evaporation through a third aligned stencil (Fig. 2j). To avoid the degradation of the pentacene-dielectric interface [8] all the fabrication process steps are done with the smallest possible delay. Every step, except evaporation of pentacene, is done in a cleanroom environment. Electrical characterization of devices is performed by contacting the pads through the thin top-gate dielectric layer. This method is performed

with very good repeatability and reliability and simplifies the processing as it avoids a supplementary patterning step of the top-gate dielectric. In future implementations an additional etching step will be added to open the contact pads.

III. DOUBLE-GATE OTFT TRANSFER CHARACTERISTICS

Electrical characterization of devices is performed using a Microtech Cascade probing system. The effect of the double-gate architecture on the transfer characteristics of pentacene TFTs has been investigated. In Fig. 4 and Fig. 5 a typical drain current versus bottom-gate voltage transfer characteristic of a double-gate pentacene TFT is shown in linear and semi-log scale, respectively, with the top-gate bias as a parameter, at constant drain voltage. The experimental data show that the top gate bias has a small effect on the "on" current but a strong influence on the threshold voltage, which is shifted towards more negative values when the top-gate bias (V_{Gtop}) is swept from negative to positive values (see Fig. 6). Moreover, the sub-threshold slope is greatly improved when the top-gate bias is changed from negative values to positive ones (see Fig. 7). The I_{ON}/I_{OFF} is accordingly increased with increasing V_{Gtop} (I_{OFF} in this case is the drain current at bottom-gate bias, V_{Gbot}, equal to zero, see Fig. 8). There is also a significant impact of the top gate bias on the leakage current (I_{LEAK}, i.e. the minimum current observed in the subthreshold region) of the device, which decreases when the top-gate bias is increased from -20 V to +10 V. Finally, we observe that the leakage current of the fabricated devices is lower than 1 fA/µm, a very low value (at the detection limit of the parameter analyzer, Agilent 4156, for a device with W=5µm, L=4µm) with a corresponding ratio, I_{ON}/I_{LEAK}, of approximately 10^7.

Drain current, I_D

Comparing the above results with the I_D-V_G characteristic of a device without a top gate the beneficial impact of both the passivation with parylene-D and the control of the top interface with the biasing of the top gate can be noted. In Fig. 9 we observe the considerably higher leakage current I_{LEAK} (~10^{-10} A/μm) of an unpassivated pentacene TFT at positive bottom-gate bias (e.g. @ V_{Gbot} = +20 V). The impact of the processing for the passivation and the deposition of the top gate on the I_{ON} seems to be limited, although a reduction of this current by a factor ranging from 2 to 3 is noted. It is also interesting to observe the transfer characteristics of the transistor formed by the top-gate electrode. In Fig. 10 the I_D-V_{Gtop} curve of the top interface transistor is presented with the bottom gate bias as a parameter. We can notice that for positive bottom-gate bias and for negative top-gate bias the current in the device is quite high with values that can reach 10^{-10} A/μm. Similar orders of magnitude for the current have been observed in Fig. 9 for positive bottom-gate bias for the devices that were not passivated by parylene-D and without a top gate.

Sub-threshold swing, S

Regarding the subthreshold swing, $S = [d\log I_D/dV_G]^{-1}$, it's value is reduced after the addition of the top gate, even at zero top gate bias. In all of the cases studied S has been extracted using the average slope between two different levels of current in log scale (10^{-15} A/μm and 10^{-10} A/μm) due to the non-pure exponential nature of the subthreshold region. As it can be observed in Fig. 5 and 7 the subthreshold swing is modulated by the top-gate bias V_{Gtop}, increasing for negative V_{Gtop} and reduced for positive values of it. This effect shows the importance of the control of the top interface of the pentacene

layer to the operation of the OTFT, especially in a relatively thick layer as the one used in this study (100 nm).

Threshold voltage, V_T

In figure Fig. 6 the dependence of the pentacene TFTs threshold voltage on the V_{Gtop} value is presented. Two methods have been used to extract V_T: i) by extrapolation on the linear-linear I_D-V_G characteristic (at maximum transconductance) at the linear regime and ii) by assuming $V_{T,ID} = V_G$ at constant current level I_D. The extrapolated threshold voltage ($V_{T,ext}$) always remains negative and it moves monotonically towards less negative values as V_{Gtop} is swept from positive to negative values. In the case of $V_{T,ext}$ we can distinguish a change of slope at around -5 V, but the general trend for both $V_{T,ext}$ and $V_{T,ID}$ is the linear dependence on V_{Gtop}. This effect has also been observed by Iba et al. [4] in pentacene double-gate TFTs where V_T stabilizes for higher negative values. This constant $\Delta V_T/\Delta V_{Gtop}$ at positive V_{Gtop} is not observed in our case although the electric field has the same intensity as in the case of Iba et al. (~1 MV/cm). In some cases higher values of electric field have been applied but the parylene-D dielectric (thickness of 200 nm) broke down destroying the samples. The slope of the V_T-V_{Gtop} curve in Fig. 6 from V_{Gtop} = 10 V to -5 V is within the range 0.30-0.33.

Low field carrier mobility, μ_0

The carrier mobility in pentacene of both the bottom-gate and top-gate interfaces has been extracted using a standard method (extrapolation of the threshold voltage on a linear plot of $I_D \times g_m^{-0.5}$ as a function of V_{Gbot}) applied for silicon MOSFETs [9] assuming that there is no dependence of the contact resistances at the source and drain on the gate voltage. Due to higher noise on the top-gate interface the values for the mobility present a significant dispersion for various bottom-gate biases. There is a 2 to

4 orders of magnitude difference in mobility between the bottom and the top interfaces with the bottom interface presenting a much higher mobility of approximately 1-2 x 10^{-2} cm^2 V^{-1} s^{-1}. The bottom-channel mobility does not depend on the top-gate bias as it can be observed in Fig. 11 and this is a behavior that has also been reported by Iba et al. in similar device architectures. In addition, it has been observed that the mobility in pentacene depends on the longitudinal electric field applied between the source and drain. In Fig. 12 the field-effect mobility of the bottom interface is plotted as a function of the square root of the effective longitudinal field between the source and drain electrodes.

IV. DISCUSSION

The effect of the top gate observed in the transfer characteristics of the OTFTs in this study is a confirmation that in pentacene layers used in OTFTs, the top interface (or the typically not gated one) can play a significant role in terms of threshold voltage, subthreshold swing, “off” and leakage current.

From the observations of the transfer characteristics of the top and the bottom transistors as well as of the transfer characteristics of unpassivated devices we deduce that the top interface of unpassivated pentacene OTFTs can greatly contribute to the leakage current observed for positive bottom-gate voltages. It is possible that the termination of the chemical bonds of the pentacene molecules of the top interface is favorable to the creation of a parasitic top channel in devices without passivation (or a top gate architecture) resulting in transistors that practically cannot be switched off. On the other hand, the current on the top transistor does not contribute much to the "on"

current of the whole device as it can be seen in Fig. 7. The top channel of the transistor has very low field-effect mobility possibly due to the higher roughness of the interface and the formation of microcrystallites of pentacene [3]. Fig. 7 also suggests that the top-interface could not be used as a functional transistor as the I_{ON} is small and the whole performance would be extremely poor. The top surface of deposited pentacene for DG organic TFTs is usually of low quality in the case of evaporated pentacene [4] as well as in devices where the organic semiconductor is spin-coated [3]. It is interesting to note that the top-interface field-effect mobility in this work is in very good agreement with values reported in [4].

Regarding the effect of the top-gate bias on bottom-channel threshold voltage V_T for the devices studied in this work, it is difficult to attribute the shift of V_T to the simple electrostatic effect of the two gate dielectrics as described by Iba et al. in [4] even in the case when the pentacene capacitance is taken into account. The slope $\Delta V_T/\Delta V_{Gtop}$ in Fig. 6 is found to be 0.30-0.33 whereas the value of the capacitor ratio C_X/C_{bot} (see Appendix for details) is 0.68 when the semiconductor capacitance is taken into account. It is possible that interface-states capacitance should be taken into account in the calculations. Assuming an homogeneous distribution $N_{it,top}$ of interface states in the energy gap of pentacene at the top interface it is possible to explain the discrepancy between $\Delta V_T/\Delta V_{Gtop}$ and C_X/C_{bot}. An interface-states concentration in the range of 3.2 to $3.8 \times 10^{11} cm^{-2}\ eV^{-1}$ can bring the slope $\Delta V_T/V_{Gtop}$ within the extracted values (0.30-0.33, the higher the concentration the lower the slope, also see Appendix). It is worth noting that partial depletion of the pentacene layer alone cannot explain the lower slope $\Delta V_T/\Delta V_{Gtop}$ because in that case the depleted layer of pentacene would be thinner (i.e. higher C_{penta}) leading to an even higher C_X/C_{bot} ratio. If both partial depletion and

interface states are considered then the constant slope $\Delta V_T/\Delta V_{Gtop}$ could not be explained when the top interface goes from accumulation to depletion as both C_{penta} and $C_{it,top}$ should change at the same time in order to keep the ratio C_X/C_{bot} constant, a case that it highly improbable as C_X/C_{bot} depends on C_{penta} and $C_{it,top}$ in different ways ($C_{it,top}$ in parallel with C_{penta}).

Another important observation is the significant improvement of the subthreshold swing with the modulation of the top-interface conductivity. The less the top interface becomes conductive the more the subthreshold swing diminishes. That could be attributed to the interface states' occupation at the "top" interface. As V_{Gtop} is swept from positive (depleted top layer of pentacene) to negative values (accumulated top layer) interface traps get filled and C_{it} starts to interfere with C_{penta} increasing the subthreshold swing of the device I_D-V_{Gbot} characteristics as the negative factor in the formula of subthreshold swing S is decreased (see formula 5.5.18 in [14], also reported in the Appendix). The values of the subthreshold swing are still high even in the best case (~3.5 V/dec), but one has to bear in mind that the dielectric used for the bottom gate is a low-k one (polyimide) and with quite large thickness (~230 nm) and this is an important factor for the generally high values of the subthreshold swing. Interface states at the bottom-interface could also be present and further increase the subthreshold swing.

Regarding the dependence of the mobility of the bottom channel on the longitudinal electric field, similar behavior has been reported before [10]. In OTFTs with polycrystalline or amorphous organic semiconductor films a Poole-Frenkel behavior in the charge transport of the organic material is believed to be at the origin of the increasing mobility with the square root of the longitudinal electric field. Models based

on the polaron hoping mechanism of conduction have been proposed by other research groups [11, 12].

V. CONCLUSION

In this work double-gate architecture for pentacene TFTs fabricated on flexible substrate has been reported. Three aligned levels of stencil lithography have been used along with standard photolithography to successfully fabricate the devices. Although the mobility reported here is lower than the one reported in the literature for other DG devices or single-gate devices (e.g. in [4] or in [15] where buffer layers like PMMA have been used) the importance of the top interface of pentacene in the operation of OTFTs has been demonstrated by the control of this interface with a top gate electrode. Furthermore, the size of devices reported in this work is reduced compared to [4] by a factor of 20 (5μm channel length vs. 100μm with dielectric thickness 3 times lower compared to [4]). It has been shown that the top-gate bias has a strong influence on the subthreshold region of transfer characteristics, which are greatly enhanced in terms of leakage current as well as of subthreshold swing. The threshold voltage of the bottom-gate transistor is modulated by the top-gate bias, decreasing simultaneously with the subthreshold swing improvement, which enables a much lower voltage operation of the transistor. This is a strong indication that the top interface quality along with the formation of a parasitic transistor channel in single-gate pentacene TFTs can result in high values of leakage current and the poor performance of the devices in the subthreshold region. Although the top interface gives rise to significant leakage currents, it appears that it is difficult to be used efficiently for a functional top-gate transistor as the mobility and, consequently, I_{ON} of that interface remains low. Finally,

the increasing mobility values with the square root of the longitudinal field is an indication that the conduction mechanism in the bottom interface could be described by a polaron hoping model and that the deposited pentacene film is polycrystalline.

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APPENDIX

The DG organic TFT can be divided in three capacitive regions starting from the top-gate electrode down to the bottom-gate electrode. C_{top}, C_{penta} and C_{bot} are the capacitances per unit area of the top-gate dielectric (parylene, relative permittivity of 3.1, [4]), pentacene (relative permittivity of 4, [13]) and bottom-gate dielectric (polyimide, relative permittivity of 3.8, [4]). According to [4] $\frac{\Delta V_T}{\Delta V_{Gtop}} = \frac{C_X}{C_{bot}}$ where $C_X = \frac{C_{top} C_{penta}}{C_{top} + C_{penta}}$. In our case, $\frac{C_X}{C_{bot}} \approx 0.68$ whereas $\frac{\Delta V_T}{\Delta V_{Gtop}} \leq 0.33$. This result suggests that the capacitance of the interface states at the top interface should be taken into account to better explain the modulation of the bottom-channel threshold voltage by the top-gate bias. Based on the derivation of $\frac{\Delta V_T}{\Delta V_{Gtop}}$ in [14] (discussion on p.133, equation 5.3.12 in [14]) when interface traps are present on the top interface we get the following

expression (bottom gate interface states do not interfere in the modulation of V_T by V_{Gtop}):

$$V_{T,top\_depl} = V_{T,top\_acc} - \frac{C_{penta}C_{top}}{C_{bot}(C_{penta} + C_{top} + C_{it,top})}(V_{Gtop} - V_{Gtop\_acc}), \text{ where } C_{it,top} = q\,N_{it,top}.$$

Also based on the expression of the subthreshold swing (SS) proposed in [14] (formula 5.5.18, page 155) SS is increased when $C_{it,top}$ increases as the negative factor in the expression decreases:

$$S \propto \left[\left(1 + \frac{C_{it,bot}}{C_{bot}} + \frac{C_{penta}}{C_{bot}}\right) - \frac{\frac{C_{penta}^2}{C_{bot}C_{top}}}{1 + \frac{C_{it,top}}{C_{top}} + \frac{C_{penta}}{C_{top}}}\right]$$

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FIGURE CAPTIONS

Figure 1: Schematic cross section of a double-gate pentacene thin-film transistor with the thicknesses of the different layers constituting the device.

Figure 2: Figure 2: Processing steps for the fabrication of the double-gate pentacene TFTs.

Figure 3: Organic TFTs on a flexible 12 μm thin PI substrate are peeled off the Si wafer after processing.

Figure 4: Typical transfer characteristic of a double-gate pentacene TFT. A modulation of the "on" current of the device is observed by the top-gate bias, although it remains limited. The current in the graph is normalized by the device's width, W.

Figure 5: Transfer characteristic of a pentacene TFT in semi-log scale. The subthreshold swing is greatly enhanced by applying a positive top-gate bias and completely depleting the top layer of pentacene. The current in the graph is normalized by the device's width, W.

Figure 6: Bottom-channel threshold voltage V_T as a function of the top-gate bias V_{Gtop}. Two methods have been used to extract V_T: i) by extrapolation on the linear-linear I_D-V_G characteristic (at maximum transconductance, inset figure) at the linear regime and ii) by assuming $V_{T,ID} = V_G$ at constant current level I_D. This slope ranges from 0.3 to 0.33. The value of 0.33 is much lower than the ratio C_X/C_{bot} (see Appendix) suggesting that the capacitance of the interface states should be taken into account in the calculation.

Figure 7: Curve showing the modulation of the bottom-channel subthreshold swing as a function of the top-gate bias. The average slope between two different current levels (10^{-15} A/μm and 10^{-10} A/μm) has been used for the calculation of the subthreshold swing due to the non-purely exponential nature of the characteristic in the subthreshold region.

A value lower than 3.5 V/dec is reported for V_{Gtop} = 10V (when the top-channel is not accumulated and can be considered completely blocked).

Figure 8: Bottom-channel drain current "on"-"off" ratio I_{ON}/I_{OFF} as a function of top-gate bias V_{Gtop}. It should be noted that I_{OFF} in this case is considered to be the bottom-channel drain current at bottom-gate bias equal to 0V. Positive V_{Gtop} is acts beneficially to this ratio by increasing it by almost two orders of magnitude.

Figure 9: I_D-V_G characteristic of a pentacene TFT without top dielectric (unpassivated) and gate electrode. The main characteristic is the relatively high current for positive gate bias indicating the reduced capability of the gate to control the top pentacene interface and switch the parasitic channel off.

Figure 10: Top-channel transistor I_D-V_G characteristic (V_D = -10V in this case) with the bottom-gate bias as a parameter. For positive bottom gate biases the current still remains relatively high in the top channel. This is an indication that the origin of the high leakage current in unpassivated devices is in the parasitic top-interface channel that cannot be switched off by the (bottom) gate.

Figure 11: Bottom-channel mobility as a function of the top-gate bias. Mobility remains almost constant with V_{Gtop} showing no dependence on the top-gate electric field. Similar behavior has been reported by Iba et al. in [4] and in almost identical double-gate pentacene TFT architecture.

Figure 12: Mobility dependence on the longitudinal effective electric field between the source and drain for a double-gate pentacene TFT. The general trend is an increasing mobility with the square root of the longitudinal field.