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Organic thin film transistors on flexible polyimide substrates fabricated by full-wafer stencil lithography

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ABSTRACT

This paper presents new results on miniaturized pentacene thin film transistors (TFTs) fabricated on a spin coated polyimide (PI) film. Patterning steps, which are vital for the integrity and electrical performance of organic TFTs, were done using resistless shadow-mask lithography with two high precision MEMS fabricated stencils, thus avoiding solvents and high temperature processes. Both pentacene and source–drain (S/D) electrodes were directly patterned through stencils with high accuracy on wafer scale. The TFTs have been characterized before and after peeling the flexible PI film off the rigid surface, showing full transistor functionality in both cases.

1. Introduction

Polymers enable devices to be flexible and to better withstand stress and strain under mechanical load. Polymer substrates and organic semiconductors are of great interest for large arrays of thin film transistors (TFTs). Flexible TFTs and circuits have been widely reported during the last few years [1–5], with transistor channel lengths down to 20 μm [6]. In view of further miniaturization and process improvements we adopted a previously reported aligned stencil lithography process [7,8] as a clean, resistless, in-vacuum patterning technique for organic electronic devices on plastic substrates. Stencil lithography is based on the principle of the shadow-mask technique, which is a parallel process with high spatial resolution, down to sub-micron scale [9–11]. A typical stencil includes low-stress silicon nitride (SiN) membranes which contain design-specific micro- and nanoapertures. The membranes are released by wet etching chemistry and finally supported by bulk silicon (Si). The stencil is aligned and clamped to the substrate, the required material is deposited through the stencil, and finally the stencil is removed, leaving the substrate patterned.

2. Fabrication

Organic TFTs were fabricated using polyimide (PI) as both flexible substrate and gate dielectric material, gold (Au) pads as contacts for gate, source and drain, and pentacene as the organic semiconductor (Fig. 1a and b). A rigid wafer is used to handle the flexible PI substrate through all the processing steps. Stencil lithography enables solvent-free local patterning of pentacene followed by the deposition of the Au source–drain (S/D) top contacts.

2.1. Stencil

Two full-wafer stencils with different designs were fabricated to locally pattern pentacene and to define S/D as top contacts. The stencils are made of a 10 cm Si wafer and 500 nm low-stress SiN as membrane material. The full-wafer stencils include alignment marks to position stencil apertures relative to the patterned gate contacts on the substrate (Fig. 1c). A customized MA/BA6 SUSS MicroTec machine is used as a stencil aligner, with an alignment accuracy around 2 μm. The membrane apertures for local pentacene patterning are rectangles, few micrometers larger than the channel dimensions. Membrane apertures for S/D top contacts define channel lengths of 3–20 μm and channel widths of 3–50 μm (Fig. 1d).

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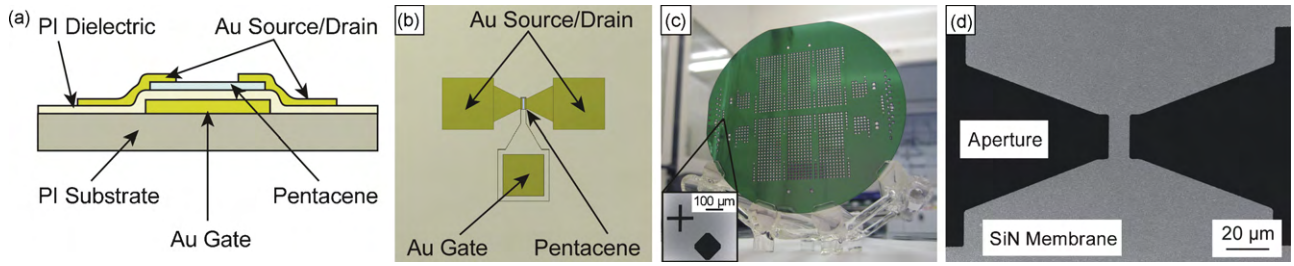

Fig. 1. (a) Schematic cross section of an organic TFT on a flexible PI substrate. PI is used as gate dielectric, pentacene as organic semiconductor, Au as gate and S/D top contacts. (b) Schematic top view an organic TFT on a flexible PI substrate including S/D and gate contacts. Pentacene is locally patterned above the gate contact. (c) Full-wafer stencil made of a Si wafer and low-stress SiN as membrane material. Inset: Stencil lithography alignment marks. (d) Apertures in a low-stress SiN membrane to pattern S/D top contacts.

2.2. Device

The flexible TFTs are fabricated using a full-wafer stencil-based process. The fabrication starts with a 10 cm Si wafer as a rigid substrate to support all the processing steps. The Si wafer is spin coated with PI (PI2611 from HD MicroSystems) at a speed up to 1000 rpm for 40 s to obtain a 12 μm thin layer. The soft bake is carried out at 100 °C and the hard bake at 300 °C, respectively. Both hard and soft bake are done in a N_2 environment. Gate contact pads are defined by standard lift-off processing using UV lithography. 10 nm Ti as an adhesion layer and 100 nm Au as gate material are evaporated by means of e-beam. 60 wt% PI2610 + NMP (n-methyl-2-pyrrolidone) is spin coated at a speed of 5000 rpm for 40 s to define a 230 nm thick dielectric. The soft bake and the hard bake are also carried out at 100 and 300 °C, respectively. The dielectric thickness was measured at several places on the wafer and found to be uniform within 12 nm. UV lithography and O_2 plasma are then used to open the contact pad of the gate electrode. A second lift-off processing patterns 10 nm thin Ti adhesion pads for S/D contacts. A full-wafer stencil with apertures for pentacene deposition is aligned to the pre-patterned substrate. The deposition of pentacene represents a critical step. This very sensitive organic semiconductor cannot be exposed to high temperature or chemical solvents. Thus, stencil lithography is the only viable way to date for local patterning as well as for any further processing steps. The pentacene is thermally evaporated locally through an aligned stencil above the gate contacts using a vacuum chamber at room temperature. After removing the stencil, a second full-wafer stencil is aligned and 100 nm thin Au electrodes as S/D contacts are deposited through the membrane apertures by e-beam evaporation. The second stencil is removed from the substrate. After pentacene and Au stencil depositions, both stencils are cleaned of the remaining material before further use. The pentacene is removed by exposing the stencil to an O_2 plasma at 500 W for 10 min. The Au film on the second stencil is removed using a Au etch solution [12–13]. Both stencils were used for four evaporation–cleaning cycles, and remained functional.

The adhesion of the PI as a flexible substrate to the Si carrier wafer has been optimized to stand all processing, while being low enough to allow simple detachment by peeling off the film in a reliable way (Fig. 2).

3. Characterization

The gate dielectric was independently tested using dedicated designs on the same wafer as the transistors. Metal–insulator–metal (MIM) structures were fabricated to test the 230 nm thick PI layer as gate dielectric. The MIM contact pads are made of Au and have a size of 150 μm × 150 μm. The characterization of the gate dielectric was done by measurements of capacitance and leakage current vs. applied voltage of the mentioned test structures. A dielectric strength of 2.3×10^6 V/cm and a leakage current on the order of 10^{-9} A/cm^2 were obtained up to fields of 2×10^6 V/cm. A relative permittivity $\varepsilon_{r,PI} = 2.6 \pm 0.2$ of the PI was extracted.

Pentacene TFTs of various channel widths and lengths (Fig. 3) were characterized electrically. The output and transfer DC characteristics of a transistor with a channel length $L = 10$ μm and a channel width of $W = 20$ μm show satisfactory levels of drain current I_D, with classical MOSFET-like behavior in the linear and saturation regimes (Fig. 4). Due to the relatively thick and low-permittivity PI gate dielectric the gate coupling to the TFT channel is not strong and, consequently, the sub-threshold slope is higher than needed for faster electronic circuits. In addition, gate and drain biases need to be higher than 15 V to achieve an on-current of 5 nA/μm or higher. From the DC transfer characteristics the extracted low-field mobility μ of fabricated pentacene TFTs is 5.6×10^{-2} cm^2/V s and extrapolated threshold voltage V_T is −3.8 V. After detaching the PI substrate including pentacene TFTs off the wafer, the TFT low-field mobility μ slightly decreased to 5.3×10^{-2} cm^2/V s, whereas the threshold voltage V_T stayed constant.

Channel dimensions of $L > W$ have been realized to explore the possibilities of stencil lithography. The output and transfer DC characteristics of such a transistor with $L = 10$ μm and $W = 3$ μm peeled off the wafer show MOSFET-like behavior and the drain current scales down with the channel width (Fig. 5). From the DC transfer characteristics the extracted low-field mobility μ of such a pentacene TFTs is 3.3×10^{-2} cm^2/V s and the extrapolated threshold voltage V_T is −3.2 V.

A pentacene TFT with $L = 4$ μm and $W = 50$ μm is pushing the limit to shorter channel lengths with S/D top contact configuration. The characterization of such a pentacene TFT shows as the previous examples MOSFET-like behavior and a sufficient level of drain current (Fig. 6). The extracted low-field mobility μ is 3.9×10^{-2} cm^2/V s, and threshold voltage V_T is −3.0 V. Drawbacks of this pentacene TFT are a less dominant saturation regime in the output characteristics which are probably caused by defects in the pentacene layer.

Finally, a pentacene TFT with the same channel length $L = 4$ μm and a narrower channel width $W = 20$ μm is characterized. This device shows a linear regime but saturation does not occur above a gate voltage of $V_G = -40$ V. Nevertheless, transfer characteristics have MOSFET-like behavior. The extracted low-field mobility μ is 0.8×10^{-2} cm^2/V s and the extrapolated threshold voltage V_T is −2.5 V, respectively.

Low-field mobilities μ, transconductances g_m, I_{on}/I_{off} ratios and extrapolated threshold voltages V_T from the presented pentacene TFTs DC transfer characteristics were extracted using the approach of Ghibaudo [14] and they are summarized in Table 1.

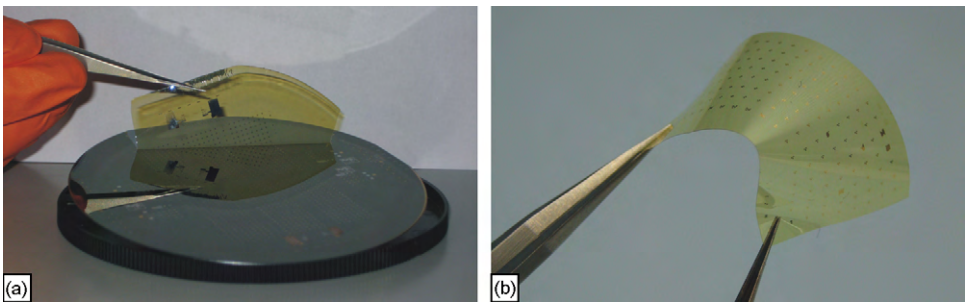

Fig. 2. Organic TFTs on a flexible 12 μm thin PI substrate are peeled off the Si wafer after processing.

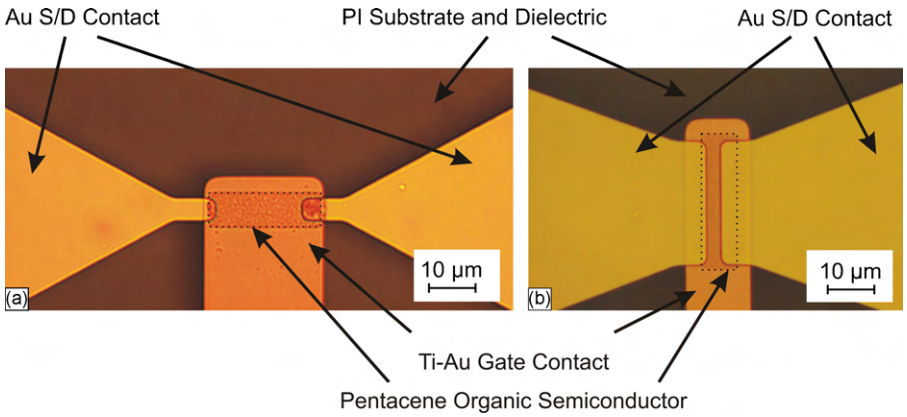

Fig. 3. Two organic TFT fabricated by a stencil-based process. The dotted line guides the eye where pentacene is locally patterned above the gate contact. S/D top contacts are aligned to the gate contact.

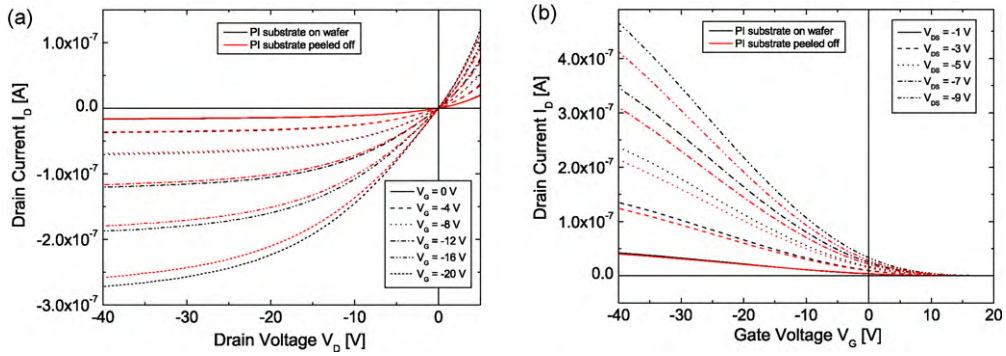

Fig. 4. (a) I_D–V_D output characteristics and (b) I_D–V_G transfer characteristics of a pentacene TFT of 10 μm channel length and 20 μm channel width before and after peeling the PI substrate off the Si wafer.

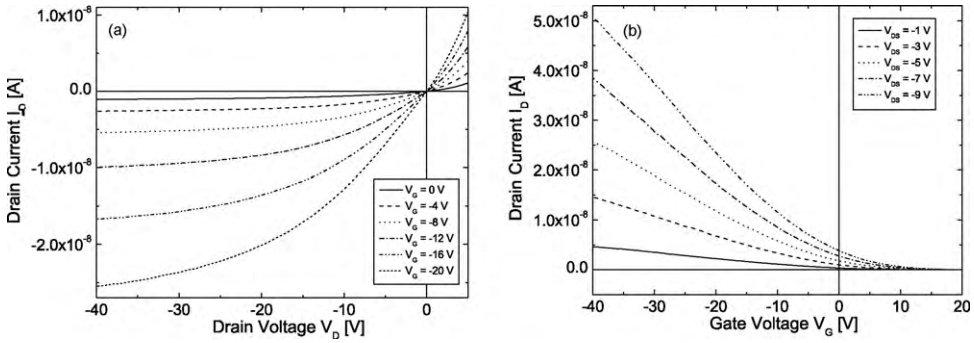

Fig. 5. (a) I_D–V_D output characteristics and (b) I_D–V_G transfer characteristics of a pentacene TFT of 10 μm channel length and 3 μm channel width after peeling the PI substrate off the Si wafer.

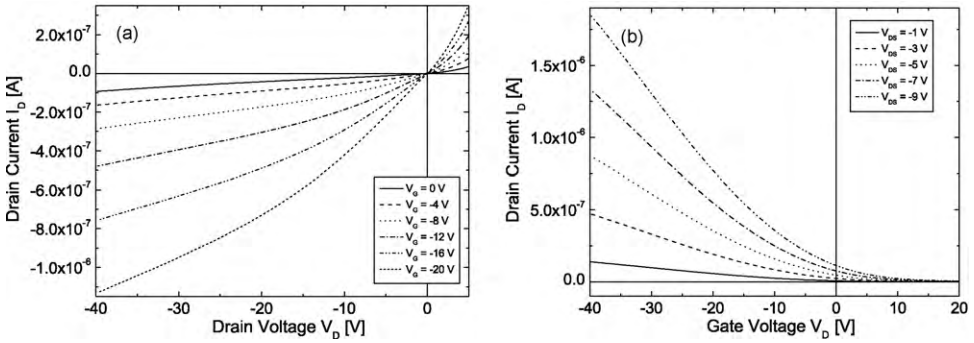

Fig. 6. (a) I_D–V_D output characteristics and (b) I_D–V_G transfer characteristics of a pentacene TFT of 4 μm channel length and 50 μm channel width after peeling the PI substrate off the Si wafer.

Table 1
Summarized physical parameters extracted from pentacene TFTs DC transfer characteristics.

Channel length [μm]	10	10	10	4	4
Channel width [μm]	20	20	3	50	20
	On wafer	Peeled off	Peeled off	Peeled off	Peeled off
Low-field mobility μ [cm^2/V s]	5.6×10^{-2}	5.3×10^{-2}	3.3×10^{-2}	3.9×10^{-2}	0.8×10^{-2}
Transconductance g_m [S]	6.4×10^{-9}	5.8×10^{-9}	0.2×10^{-9}	4.3×10^{-9}	0.4×10^{-9}
I_{on}/I_{off}	$\sim 10^4$	$\sim 10^4$	$\sim 7 \times 10^3$	$\sim 10^3$	$\sim 4 \times 10^2$
Extrapolated V_T [V]	−3.8	−3.8	−3.2	−3.0	−2.5

4. Discussion

Applying full-wafer stencil lithography we obtained working organic TFT on flexible substrates with channel lengths down to 3 μm. While classical TFT designs consider channel dimensions with $L < W$, in our experiments, channel dimensions of $L > W$ have also been included to explore the possibilities of stencil lithography. The fabrication of S/D for short but wide channels ($L < W$) poses stability issues for the SiN bridge between the stencil apertures. Therefore, shorter but wider bridges have a higher chance of survival. Inspections at the end of the stencil fabrication process have shown that the SiN bridges between S/D for channel lengths of 1 μm did not withstand the processing. However, membranes with apertures for longer channels were stable enough and survived all processing. Electrical characterization of TFTs with channels shorter than 3 μm but intact bridges often showed leakage between S/D contacts. The electrical connection between the S/D contacts is a result of the enlargement of the transferred stencil apertures to the substrate, known as blurring [15].

The alignment accuracy of a full-wafer stencil to a substrate is limited. First, the curvatures of the stencil and the substrate are different. Every step of the process flow changes the internal stress of the wafers and modifies their curvature. Therefore, the lateral positions of the patterned structures in the stencil and the substrate deviates slightly from the design. Second, the alignment of a stencil with respect to the substrate is limited by the 2 μm accuracy of the customized MA/BA6 SUSS MicroTec machine. These constraints result in a non-uniform alignment over the full-wafer substrate. Although a good alignment can be achieved locally, asymmetric alignment of pentacene and S/D contacts is observed at other locations on the same wafer.

Threshold voltages V_T change for the different channel widths and lengths used in our experiments. The threshold voltage V_T increases towards positive values with decreasing channel lengths. This behavior is similar to short-channel effects in Si MOSFET devices. This is based on a drain-induced barrier lowering (DIBL), where a lower gate voltage is required to create a channel [16]. DIBL-like behavior of pentacene TFT has been reported for a channel width of 100 μm and channel lengths between 5 and 50 μm [17]. Our work shows this phenomenon occurs also for channels as narrow as 20 μm.

5. Conclusion and outlook

We succeeded in fabricating organic transistors using a 12 μm thin flexible substrate, a 230 nm thick PI dielectric, locally patterned pentacene and S/D top contacts by aligned full-wafer stencil lithography. Transistors with channel lengths from 3 to 20 μm showed good MOSFET-like behavior. However, when scaling channel lengths below 5 μm some TFT characteristics started to become noisy, and also dependent on the device location on the wafer. We are currently investigating in depth the uniformity across the wafer and identifying the parameters influencing it. The organic TFT on the flexible PI substrate maintain their functionality after being peeled off from the rigid Si wafer. The maximum extracted low-field mobility μ of pentacene TFTs is 5.3×10^{-2} cm^2/V s, and the minimum threshold voltage V_T −2.5 V, respectively.

In view of improving the transistor characteristics, a double-gate configuration is in progress [18]. Future investigations also concentrate on the reliability of organic TFTs under mechanical load. Controlled tensile strain will be applied to the flexible PI substrate for single stretching and cycling experiments.

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Biographies

Katrin Sidler received her MSc degree in mechanical engineering from the Swiss Federal Institute of Technology Zurich (ETH), Switzerland in 2006. To carry out her master thesis she temporarily worked at the Department of Micro and Nanotechnology, Technical University of Denmark (DTU). After her studies, she joined the Microsystems Laboratory at Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland where she is currently working towards her PhD degree. Her research topic is stencil lithography applied to flexible polymer substrates and the development of compliant stencil lithography.

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Veronica Savu graduated from California Institute of Technology (Caltech) in 2000 in Physics. She continued her studies at Yale University, where she received two consecutive Hoge Fellowships and earned her PhD in Physics in 2007 working on superconducting single optical photon detectors. After her PhD she pursued her post-doctoral research at Ecole Polytechnique Fédérale de Lausanne (EPFL). In 2008 she was awarded a 3-year Swiss National Science Foundation (SNSF) Ambizione individual grant promoting junior researchers across disciplines. Her professional interests are focused on experimental techniques for the characterization of nanodevices and novel nanotechnology fabrication methods, including stencil lithography.

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