Microelectronic Engineering 87 (2010) 1561–1565

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs

M. Najmzadeh [a,*], L. De Michielis [a], D. Bouvet [a], P. Dobrosz [b], S. Olsen [b], A.M. Ionescu [a]

[a] Nanoelectronic Devices Laboratory, Swiss Federal Institute of Technology (EPFL), CH-1015 Lausanne, Switzerland
[b] Newcastle University, School of Electrical, Electronics and Computer Engineering, Newcastle, UK

ARTICLE INFO

Article history:
Received 14 September 2009
Received in revised form 5 November 2009
Accepted 8 November 2009
Available online 12 November 2009

Keywords:
Local oxidation
Local lateral uniaxial tensile stress
Local mobility enhancement
Gate-all-around
Strain engineering
Si nanowires

ABSTRACT

In this work we present for the first time correlation of lateral uniaxial tensile strain and *I–V* characteristics of GAA Si NW n-MOSFET, all measured on the same device. Micro-Raman spectroscopy is employed for direct strain measurement on devices to exploit the main sources of process-induced strain, found to be accumulation of mechanical potential energy in the Si NWs during local oxidation and releasing it in the form of local lateral uniaxial tensile stress in the Si NW by out-of-plane mechanical buckling as well as lateral in-plane elongation during stripping the hard mask and the grown oxide.

A triangular GAA Si NW with 0.6 GPa peak of lateral uniaxial tensile stress, fabricated using this bulk top-down technology, exhibits promising improvements e.g. of the normalized drain current (I_D/W_{eff}) up to 38%, of the transconductance (g_m/W_{eff}) up to 50%, of the low field mobility by 53% with a peak of 64% in the peak stress region, compared to a reference device. The mobility extraction originally takes into account the measured strain profile in the channel.

© 2009 Elsevier B.V. All rights reserved.

1. Introduction

Strain engineering has been used for the 90 nm technology node and beyond to enhance the device performance during aggressive CMOS downscaling. It has been shown that uniaxial compressive and uniaxial tensile stresses along the ⟨1 1 0⟩ channel orientation with (1 0 0) channel surface are the most helpful stresses to provide higher mobility of carriers in pMOS and nMOS devices, respectively [1]. For planar devices, several local strain engineering techniques e.g. embedded epitaxial films in the S/D, CESL and stress memorization technique (SMT) have been used to induce uniaxial tensile or compressive stress along the channel [1,2]. However, scalability of the local stressor technologies parallel to the scalability of the channel is an issue.

Due to having the best possible electrostatistics in multi-gate devices e.g. Fin-FET and gate-all-around (GAA) devices and therefore, improved subthreshold slope, immunity to the issues regarding short channel effect and optimized power consumption, these architectures have represented a better scalability than planar bulk and SOI devices and therefore, are the promising candidates during aggressive CMOS downscaling. To solve the issues regarding degradation of carrier mobility for ultra-thin-body devices because of quantum mechanical confinement [3] and increased surface roughness scattering, strain engineering should be reconsidered. Including strain in the channel of multi-gate devices is a bit challenging and until now, only three techniques have been reported to make a GAA uniaxially tensile strained architecture from three dimensional suspended channels: OIS (oxidation-induced strain) [4,5] and metal gate strain [6] as local strain engineering techniques and finally, suspending the strained Si NWs from a strained substrate (SSDOI wafer) [7] as a global strain engineering technique. In this work, we focus on OIS only to prepare suspended uniaxially tensile strained Si NWs from bulk Si using local oxidation and hard mask/spacer technology to finally make GAA strained devices.

2. Built-in tensile stress analysis in Si NW during process to make GAA suspended uniaxially tensile strained Si NW n-MOSFET

The process flow to make ≈100 nm wide suspended uniaxially tensile strained triangular Si NWs with ⟨1 1 0⟩ direction from a (1 0 0) bulk Si wafer is described in details in an earlier work [5]. Fig. 1 represents the summary of this process to finally make a GAA n-MOSFET architecture together with the evolution of built-in stress during the important steps while Fig. 2 represents the actual suspended Si NWs after each step.

About zero initial biaxial strain value (ε_i) was found in the attached Si NWs to the substrate (a Si rib). Suspending the Si NW using isotropic dry Si etching temporarily induces a huge amount of tensile strain ($\varepsilon_{\mathrm{Si-HM}}$) up to 2.6% by in-plane lateral elongation as well as possible out-of-plane buckling perhaps due to relax-

* Corresponding author. Tel.: +41 21 693 7356; fax: +41 21 693 3640.
E-mail address: Mohammad.Najmzadeh@epfl.ch (M. Najmzadeh).

0167-9317/$ - see front matter © 2009 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2009.11.024

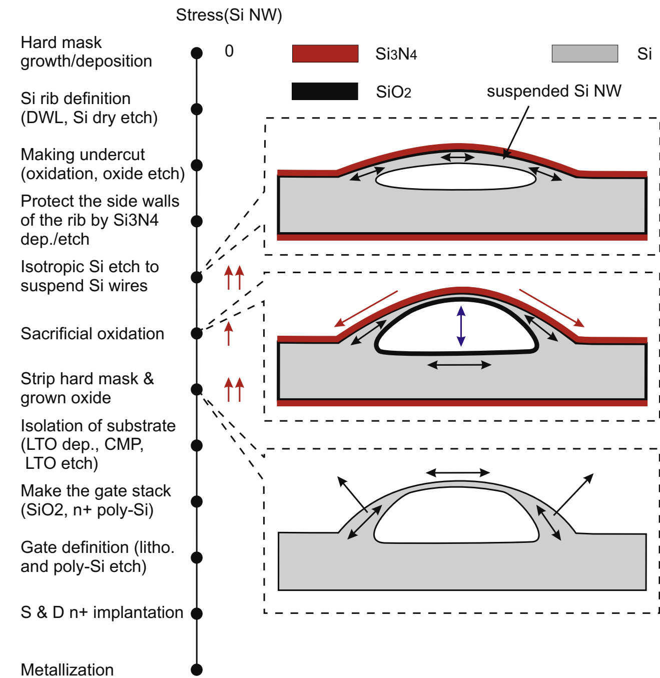

Fig. 1. Built-in Strain analysis during the process flow to make GAA uniaxially tensile strained Si NW n-MOSFET from bulk Si. The black arrows represent tensile stress in Si. The red arrows represent restrictions on out-of-plane mechanical buckling because of tensile hard mask. The blue arrow represents upward vertical forces because of the grown ring of oxide under the Si NW. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

ations of tensile stress in the Si_3N_4 hard mask across the Si NW as well as on the pads close to the anchor parts. Heating up the wafer to reach the oxidation temperature diminishes a significant amount of this temporary strain by α factor ($\alpha > 1$) due to visco-elastic relaxation of stress in the thin film layers of the hard mask at high temperature as well as geometrical reconfiguration of the Si NW during oxidation. Thermal oxidation at high temperature induces a biaxial tensile stress into the Si NW, called growth strain (ε_g), due to lattice expansion during oxidation. The increase in the level of tensile strain will be continued during cooling down the wafer to room temperature due to mismatch on thermal expansion coefficient of Si and SiO_2. The corresponding induced biaxial tensile strain to the Si NW is called thermal strain (ε_{th}). A small accumulation of tensile strain in suspended Si nano-beams, called $\varepsilon_{\text{OIS-SF}}$, is also reported in Ref. [8] due to possible injection of self-interstitial Si atoms during oxidation to the oxidation front. However, as reported in Ref. [9], this strain value cannot exceed 0.012% after consumption of e.g. 90% of the thickness of 50 μm long Si beams. Therefore, the nominal value of tensile strain in the Si NW after the oxidation step can be calculated by:

$$\varepsilon_{xx} + \varepsilon_{yy} = \varepsilon_i + \frac{\varepsilon_{\text{Si-HM}}}{\alpha} + \beta(\varepsilon_g + \varepsilon_{th}) + \varepsilon_{\text{OIS-SF}} \tag{1}$$

The grown ring of oxide under the Si NW (see Fig. 1) may also help to induce more lateral uniaxial tensile strain than expected to the Si NW due to the upward vertical forces during oxidation and during cooling down causing consideration of a β factor ($\beta \geqslant 1$).

According to Ref. [5], actual strain measurements on the Si NWs with the tensile hard mask on top after the oxidation step represent saturation of the tensile strain to about 0.5–0.6% because of restriction on mechanical displacement of the Si NW due to doubly-clamped design (restriction on lateral in-plane elongation) and the tensile hard mask (restriction on out-of-plane displacement) causing storage of mechanical potential energy in the Si NW during the oxidation step. During stripping the hard mask and the grown oxide, the sources of strain because of hard mask, growth and thermal strain disappear [5] but the Si NW elongates more to release the stored mechanical potential energy causing an increase by 3–5 factor in the strain level of the Si NW (for 850 °C oxidation temperature; see Fig. 3 for details). At this stage, the lateral uniaxial tensile strain in the Si NW can be calculated by:

$$\varepsilon_{xx} \approx \varepsilon_{xx} + \varepsilon_{yy} = \varepsilon_i + \varepsilon_{\text{OIS-SF}} + \varepsilon_{\text{OIS-pot}} \tag{2}$$

where $\varepsilon_{\text{OIS-pot}}$ represents the increase in strain during the stripping step because of the stored mechanical potential energy during oxidation.

After this stage, we believe that the possible further change in the strain level of the Si NW after the further thin film deposition and etching steps (e.g. LTO, poly-Si) can be on the order of the possible errors due to the process variation from wire to wire and from run to run and also negligible in comparison to 2.6 GPa stress peak, obtained after the stripping step. Similar thermal properties of poly-Si gate and Si NW also can avoid accumulation of thermal stress during or after gate stack deposition.

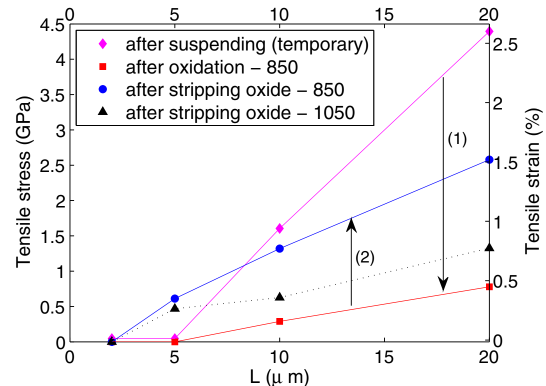

Fig. 3. Variation of tensile stress level (the peak of stress along Si NWs) vs. wire length) after wet oxidation at 850 °C (1) and after stripping the hard mask and the grown oxide (2). To get highly strained Si NWs after the stripping step, the oxidation should be performed below $T_g(SiO_2) = 960$ °C [5].

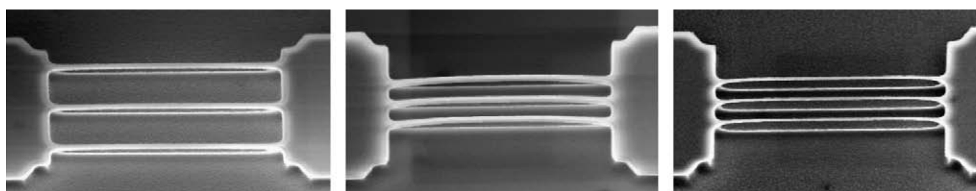

Fig. 2. SEM pictures of comparable three parallel suspended 20 μm long Si NWs on three wafers after different process steps: a tensile hard mask on top before oxidation (left), after oxidation (middle) and after the stripping step (right), representing reproducibility and controllability of the local strain technique on a single wafer as well as on different wafers.

3. Strain characterization using micro-Raman

A micro-Raman spectroscopy setup with 0.2 cm^{-1} nominal resolution was employed to directly measure stress along and across the Si NWs at 20 °C by 43.5 MPa nominal stress resolution. A laser beam with 514.5 nm wavelength was focused on the Si NW and due to having a penetration depth (762 nm) higher than the thickness of the Si NW (≈100 nm), two peaks from both non-strained bulk Si and strained Si NW were detectable in the Raman spectra. A fitting procedure with 0.07 cm^{-1} nominal resolution (corresponding to 15 MPa stress resolution) was used to extract the place of the two peaks in the spectra and finally, the shift in the wavenumber ($\Delta\omega$) was translated to tensile stress by:

$$\sigma_{xx} + \sigma_{yy}\ [\text{GPa}] = -\frac{\Delta\omega\ [\text{cm}^{-1}]}{4.596} \quad (3)$$

Line scanning along and across the Si NWs as well as area mapping was used to find out the peak of stress along each Si NW after each process step and finally, provide comparable inputs for further built-in stress analysis.

4. Electrical characterization of GAA suspended uniaxially tensile strained Si NW n-MOSFET

Similar strained Si NWs, fabricated earlier from low doped $\approx 6 \times 10^{16}$ cm^{-3} p-type bulk Si using the same process with oxidation at 1000 °C, were used for micro-Raman and electrical characterizations after isolation, gate stack growth/deposition (SiO_2/poly-Si), implantation and metallization steps. The electrical characterization was carried out at room temperature by wafer probe testing using a Microtech Cascade probe station and an HP 4155B Semiconductor Parameter Analyzer.

Fig. 6 represents normalized transfer and transconductance characteristics of the bended device in Fig. 4 with the stress profile in Fig. 5, versus a non-bended one. According to the figure, the enhancements in normalized I_D and normalized transconductance are up to 38% and 50%, respectively. As it is shown in Fig. 6, the both enhancements decrease by increasing overdrive voltage ($V_{GS} - V_T$). It is worth mentioning that the observed 0.19 V downshift in the threshold voltage of the strained device is due to the strain-induced change in the electron affinity, band gap and valence band density of states of the Si channel [10].

The extracted low field mobility using $I_D/\sqrt{g_m}$ method [11,12] represents 53% enhancement in average electron mobility, for the strained device in comparison to the non-strained one. Due to having one (100) face and two slanted non-well defined faces in the triangular GAA Si NW n-MOSFET and by considering the fact that the highest possible electron mobility enhancement belongs to (100) surface n-MOSFET under ⟨110⟩ uniaxial tensile strain [1], the highest possible local electron mobility enhancement due to strain in the triangular GAA structure is calculated using the actual strain profile, directly measured using micro-Raman spectroscopy through the gate stack, in Fig. 5 and an experimental curve including electron mobility enhancement factor for (100) surface n-MOSFET vs. ⟨110⟩ uniaxial tensile strain in [13], representing a peak of 54% enhancement in nominal local electron mobility, and afterward, plotted in Fig. 7 (curve B). However, the experimental electron mobility of the suspended architecture represents even 10% more than the average of our highest possible local mobility enhancement expectation due to uniaxial tensile strain because

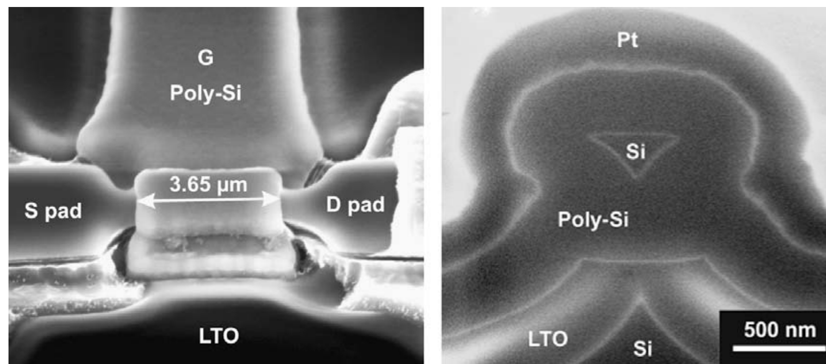

Fig. 4. SEM picture of a GAA Si NW n-MOSFET (left); cross-section of the GAA triangular wire close to one of its anchors (right).

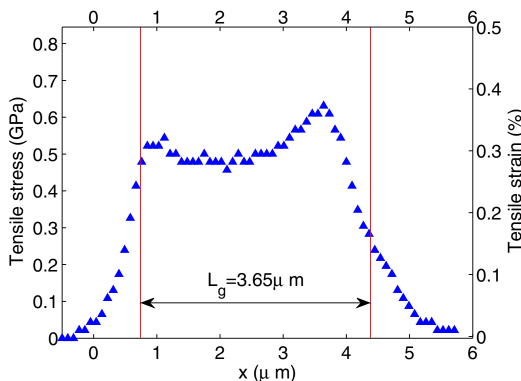

Fig. 5. Stress profile along the 5 μm long Si NW presented in Fig. 4 after the gate stack deposition step.

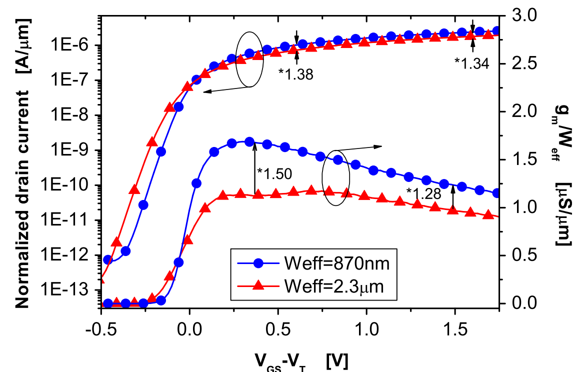

Fig. 6. Transfer and transconductance characteristics of strained and non-strained 5 μm long Si NW devices at $V_{DS} = 50$ mV (the smaller W_{eff} corresponds to the strained device). For the strained device: $V_T = -0.0384$ V, SS = 64 mV/dec; for the non-strained device: $V_T = +0.1525$ V, SS = 66 mV/dec.

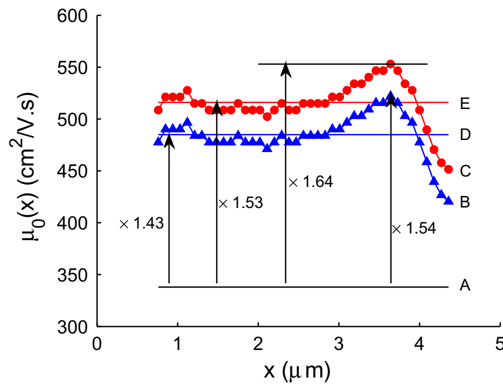

Fig. 7. Local mobility enhancement along the channel: Tri-gate non-strained Si NW (A); effect of local tensile strain on local mobility (nominal) (B); actual local mobility along the suspended channel (C); average of nominal local mobility along the channel (D); found experimental mobility in the GAA suspended Si NW n-MOSFET (E).

of local volume inversion and corner effect [14], possible higher electron mobility enhancement factor than expected due to having a lower doping level in our wafer in comparison to the used doping level in [13], possible cross-section variation along the channel and parallel operation of a parasitic MOSFET via the bulk [15]. Finally, by considering the positive contribution of all the mentioned electron mobility boosters together for the suspended architecture, the actual local electron mobility along the channel of the suspended Si NW is plotted in Fig. 7 showing a peak of 64% mobility enhancement (curve C) in comparison to the non-strained device.

5. Discussion

The shorter wires fabricated from this bulk top-down platform are thicker because of the pattern dependency of the isotropic Si etching process and therefore, less strained due to their higher critical load for buckling. To scale down this local stressor technique, the isotropic Si etching step, used to suspend the wires from bulk, should be prolonged to thin down the shorter wires to e.g. 300 nm before the oxidation step to finally get e.g. 50 nm thick Si NW after the sacrificial oxidation step. This solution offers strained Si NWs with shorter lengths but less variation in the wire length is possible on a wafer due to consuming all the longer Si NWs in the Si etching and the sacrificial oxidation steps (see Fig. 8).

The suspended uniaxially tensile strained Si NWs can be also fabricated using a SOI top-down Si NW platform to immune against the pattern dependency of the process. In this platform, due to defining the first wire shapes by e-beam lithography but not spacer technology/isotropic Si etching, the initial thickness and the width of the wires before the oxidation step are independent of the wire length. In this case, performing a short sacrificial oxidation can accumulate mechanical potential energy to the Si NWs that can be released in a stripping step. Simple calculations show that the critical load for buckling of a 2 μm long and 10 nm thick Si NW fabricated from the SOI platform is the same as a 20 μm long and 100 nm thick Si NW fabricated from the bulk platform with e.g. 2.6 GPa peak of tensile stress and perhaps, a similar stress peak can be obtained in the new Si NW ($\sigma_{cr} = \frac{\pi^2}{3} \cdot E \cdot \left(\frac{t}{L}\right)^2$ [9]; E: Young's modulus; t: thickness; L: length). However, several parameters e.g. percentage of oxidation of the Si NW, oxidation conditions, etc. also influence the value of the stored mechanical potential energy and therefore, should be taken into account as the parameters that can even optimize the final strain value in the Si NW after the stripping step.

Another approach to make scaled devices is making a short device only at the strain peak region of the Si NW using LTO to isolate the substrate, open up only the middle part of the wire and finally, gate stack deposition, implantation and metallization (see Fig. 9).

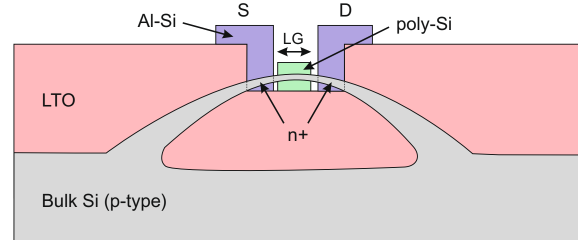

Fig. 9. Device implementation with short channel length centered on the Si NW region with a peak of e.g. 2.6 GPa lateral uniaxial tensile stress.

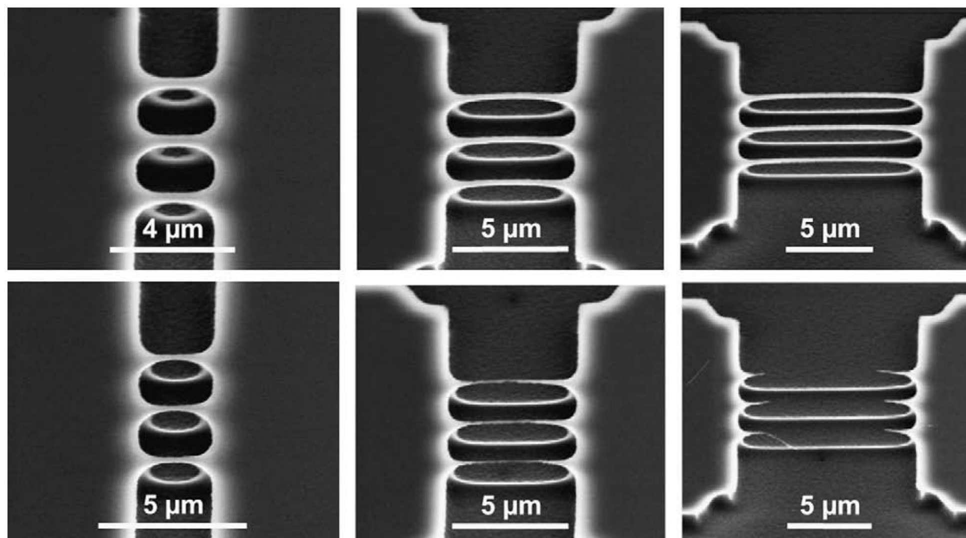

Fig. 8. The Si NWs with strain peaks represented in Fig. 3 after the stripping step (up); the Si NWs after about 25% prolongation of the isotropic Si etching step and afterward the same oxidation and stripping steps (bottom). After this prolongation, the shorter wires are buckled more, validating the scalability potential of the local oxidation technique. However, the longer wires were consumed completely during the etching and oxidation steps and therefore, less variation in wire length is possible on a single wafer.

6. Conclusion

Local oxidation accompanied by hard mask technology was used as a local stressor technology to induce local lateral uniaxial tensile stress up to 2.6 GPa to the suspended Si NWs, fabricated using a bulk top-down Si NW platform. The strained Si NWs were processed further to provide GAA uniaxially tensile strained devices. Two strained and non-strained Si NWs were electrically characterized and the actual strain profile, measured directly on the electrically characterized GAA Si NW via poly-Si using micro-Raman spectroscopy, was used to extract local mobility enhancement along the channel.

Acknowledgment

The authors thank K.E. Moselund and V. Pott for the enlighten discussions. This work is partially funded by the Nanosil European network of excellence (FP7).

References

[1] M. Chu et al., Annual Review of Materials Research 39 (2009) 203.
[2] K. Ota et al., Tech. Digest IEDM 27 (2002).
[3] K. Uchida et al., Tech. Digest IEDM 633 (2001).
[4] K.E. Moselund et al., Tech. Digest IEDM 191 (2007).
[5] M. Najmzadeh et al., Microelectronic Engineering 86 (2009) 1961.
[6] N. Singh et al., Electron Device Letters 28 (2007) 558.
[7] P. Hashemi et al., ECS Transactions 16 (2008) 57.
[8] A.M. Pyzyna et al., MEMS 189 (2004).
[9] A.M. Pyzyna, Thermal Oxidation-induced Strain in Silicon Nanobeams, Ph.D. Thesis, UCSB, 2005.
[10] J.S. Lim et al., IEEE Electron Device Letters 25 (2004) 731.
[11] G. Ghibaudo, Electronics Letters 24 (1988) 543.
[12] G. Ghibaudo, Microelectronic Engineering 39 (1997) 31.
[13] S.E. Thompson et al., Tech. Digest IEDM 1 (2006).
[14] K.E. Moselund et al., ESSDERC 359 (2006).
[15] V. Pott et al., IEEE Transactions on Nanotechnology 7 (2008) 733.